Single-Phase Controller with Integrated Driver for VR12.5 and VR12.6 Mobile CPU Core Power Supply

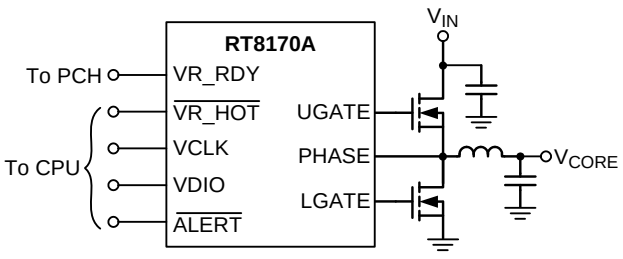
General Description

The RT8170A is a single phase CPU power controller with one integrated driver for VR12.5 and VR12.6 compliant. The RT8170A adopts the G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT8170A also features a quick response mechanism for optimized AVP performance during load transient. The RT8170A supports mode transition function with various operating states. A Serial VID (SVID) interface is built in the RT8170A to communicate with Intel VR12.5 and VR12.6 compliant CPU. The RT8170A supports VID on-the-fly function with different slew rates. By utilizing the G-NAVP™ topology, the operating frequency of the RT8170A varies with VID, load current and input voltage to further enhance the efficiency even in CCM. Besides the G-NAVP™, the CCRCOT (Constant Current Ripple Constant On Time) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.5V to 3.04V with 10mV per step. The RT8170A integrates a high accuracy ADC for platform setting functions, such as no-load offset and over-current protection level. The RT8170A provides VR ready output signals. It also features complete fault protection functions including Over-Voltage (OV), Under-Voltage (UV), Negative-Voltage (NV), Over-Current (OC) and Under-Voltage Lockout (UVLO). The RT8170A is available in the WQFN-32L 4x4 small foot print package.

Features

- **Intel VR12.5 and VR12.6 Serial VID Interface Compatible Power Management States**
- **Single Phase PWM Controller with Integrated Driver**
- **G-NAVP™ Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Single Phase**
- **Fast transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, UVP, OCP, UVLO**
- **Programmable DVID Slew Rate**
- **DVID Enhancement**
- **RoHS Compliant and Halogen Free**

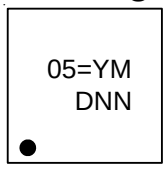
Simplified Application Circuit



Applications

- VR12.5 and VR12.6 Intel Core Supply
- Notebook CPU Core Supply
- AVP Step-Down Converter

Marking Information



05= : Product Code

YMDNN : Date Code

Ordering Information

RT8170A □□

Package Type
QW : WQFN-32L 4x4 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

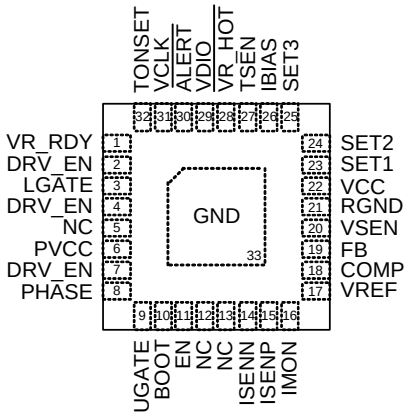
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



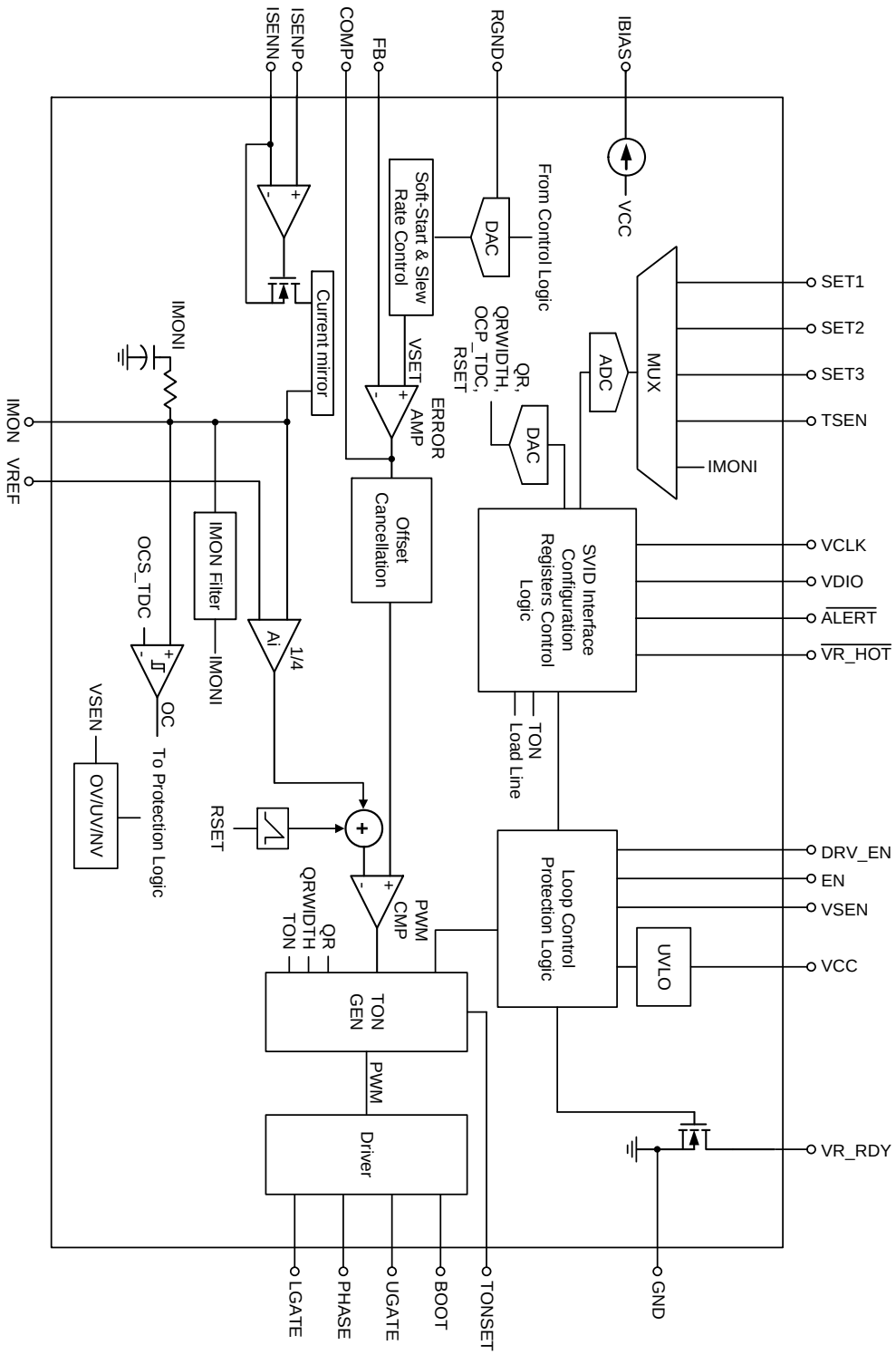
WQFN-32L 4x4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VR_RDY	VR Ready Indicator.
2, 4, 7	DRV_EN	Internal Driver Enable Control. These pins must be connected together and will go low at PS4.
3	LGATE	Low-Side Gate Drive Output. This pin drives the Gate of low-side MOSFET.
5, 12, 13	NC	No Internal Connection.
6	PVCC	Driver Power. Connect this pin to GND by a minimum 2.2μF ceramic capacitor.
8	PHASE	Switch Node of High-Side Driver. Connect the pin to high-side MOSFET Source with the low-side MOSFET Drain and the inductor.
9	UGATE	High-Side Gate Drive Output. Connect the pin to the Gate of high-side MOSFET.
10	BOOT	Bootstrap Supply for High-Side Gate Driver.
11	EN	VR Enable Control Input.
14	ISENN	Negative Current Sense Input.
15	ISENP	Positive Current Sense Input.
16	IMON	CPU CORE Current Monitor Output. This pin outputs a voltage proportional to the output current. Do not connect a bypass capacitor from this pin to GND or the VREF pin.
17	VREF	Fixed 0.6V Output Reference Voltage. This voltage is only used to offset the output voltage of the IMON pin.
18	COMP	CORE VR Compensation Node. This pin is error amplifier output pin.
19	FB	Negative Input of the Error Amplifier. This pin is for output voltage feedback to controller.

Pin No.	Pin Name	Pin Function
20	VSEN	VR Voltage Sense Input. This pin is connected to the terminal of VR output voltage.
21	RGND	Return Ground for VR. This pin is the negative node of the differential remote voltage sensing.
22	VCC	Supply Voltage Input. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor should be placed as close to the PWM controller as possible.
23	SET1	1st Platform Setting. Platform can use this pin to set DVID compensation time, RSET, DVID compensation width and OCS.
24	SET2	2nd Platform Setting. Platform can use this pin to set ICCMAX, QRTH and QRWIDTH.
25	SET3	3rd Platform Setting. Platform can use this to set Anti-overshoot function, zero load-line, DVID slew rate, RSET selection at PS0 and PS1, Anti-Overshoot enhancement and ZCD threshold.
26	IBIAS	Internal Bias Current Setting. Connect a 100kΩ resistor from this pin tied to GND to set the internal current. Don't connect a bypass pass capacitor from this pin to GND.
27	TSEN	Thermal Sense Input for CORE VR.
28	$\overline{\text{VR\_HOT}}$	Thermal Monitor Output. (Active Low)
29	VDIO	VR and CPU Data Transmission Interface.
30	$\overline{\text{ALERT}}$	SVID Alert. (Active low)
31	VCLK	Synchronous Clock from the CPU.
32	TONSET	On-time Setting. An on-time setting resistor is connected from this pin to input voltage.
33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

The RT8170A adopts the G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also have fast transient response. When current feedback signal reaches COMP signal, the RT8170A generates an on-time width to achieve PWM modulation.

TON GEN

Generate the PWM signal sequentially according to the phase control signal from the Loop Control Protection Logic.

SVID Interface/Configuration Registers/Control Logic

The interface that receives the SVID signal from CPU and sends the relative signals to Loop Control Protection Logic to execute the action by CPU.

The registers save the pin setting data from ADC output.

The Control Logic controls the ADC timing and generates the digital code of the VID that is relative to VSEN.

Loop Control Protection Logic

It controls the power on sequence and the protection behavior.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the PVCC and VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of VSET according to the SetVID fast or SetVID slow.

Table 1. VR12.5 and VR12.6 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	0	0	0	0	0	1	01	0.500
0	0	0	0	0	0	1	0	02	0.510
0	0	0	0	0	0	1	1	03	0.520
0	0	0	0	0	1	0	0	04	0.530
0	0	0	0	0	1	0	1	05	0.540
0	0	0	0	0	1	1	0	06	0.550
0	0	0	0	0	1	1	1	07	0.560
0	0	0	0	1	0	0	0	08	0.570
0	0	0	0	1	0	0	1	09	0.580
0	0	0	0	1	0	1	0	0A	0.590
0	0	0	0	1	0	1	1	0B	0.600
0	0	0	0	1	1	0	0	0C	0.610
0	0	0	0	1	1	0	1	0D	0.620
0	0	0	0	1	1	1	0	0E	0.630
0	0	0	0	1	1	1	1	0F	0.640
0	0	0	1	0	0	0	0	10	0.650
0	0	0	1	0	0	0	1	11	0.660
0	0	0	1	0	0	1	0	12	0.670
0	0	0	1	0	0	1	1	13	0.680
0	0	0	1	0	1	0	0	14	0.690
0	0	0	1	0	1	0	1	15	0.700
0	0	0	1	0	1	1	0	16	0.710
0	0	0	1	0	1	1	1	17	0.720
0	0	0	1	1	0	0	0	18	0.730
0	0	0	1	1	0	0	1	19	0.740
0	0	0	1	1	0	1	0	1A	0.750
0	0	0	1	1	0	1	1	1B	0.760
0	0	0	1	1	1	0	0	1C	0.770
0	0	0	1	1	1	0	1	1D	0.780
0	0	0	1	1	1	1	0	1E	0.790
0	0	0	1	1	1	1	1	1F	0.800
0	0	1	0	0	0	0	0	20	0.810
0	0	1	0	0	0	0	1	21	0.820
0	0	1	0	0	0	1	0	22	0.830
0	0	1	0	0	0	1	1	23	0.840
0	0	1	0	0	1	0	0	24	0.850
0	0	1	0	0	1	0	1	25	0.860
0	0	1	0	0	1	1	0	26	0.870
0	0	1	0	0	1	1	1	27	0.880
0	0	1	0	1	0	0	0	28	0.890

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	1	0	1	0	0	1	29	0.900
0	0	1	0	1	0	1	0	2A	0.910
0	0	1	0	1	0	1	1	2B	0.920
0	0	1	0	1	1	0	0	2C	0.930
0	0	1	0	1	1	0	1	2D	0.940
0	0	1	0	1	1	1	0	2E	0.950
0	0	1	0	1	1	1	1	2F	0.960
0	0	1	1	0	0	0	0	30	0.970
0	0	1	1	0	0	0	1	31	0.980
0	0	1	1	0	0	1	0	32	0.990
0	0	1	1	0	0	1	1	33	1.000
0	0	1	1	0	1	0	0	34	1.010
0	0	1	1	0	1	0	1	35	1.020
0	0	1	1	0	1	1	0	36	1.030
0	0	1	1	0	1	1	1	37	1.040
0	0	1	1	1	0	0	0	38	1.050
0	0	1	1	1	0	0	1	39	1.060
0	0	1	1	1	0	1	0	3A	1.070
0	0	1	1	1	0	1	1	3B	1.080
0	0	1	1	1	1	0	0	3C	1.090
0	0	1	1	1	1	0	1	3D	1.100
0	0	1	1	1	1	1	0	3E	1.110
0	0	1	1	1	1	1	1	3F	1.120
0	1	0	0	0	0	0	0	40	1.130
0	1	0	0	0	0	0	1	41	1.140
0	1	0	0	0	0	1	0	42	1.150
0	1	0	0	0	0	1	1	43	1.160
0	1	0	0	0	1	0	0	44	1.170
0	1	0	0	0	1	0	1	45	1.180
0	1	0	0	0	1	1	0	46	1.190
0	1	0	0	0	1	1	1	47	1.200
0	1	0	0	1	0	0	0	48	1.210
0	1	0	0	1	0	0	1	49	1.220
0	1	0	0	1	0	1	0	4A	1.230
0	1	0	0	1	0	1	1	4B	1.240
0	1	0	0	1	1	0	0	4C	1.250
0	1	0	0	1	1	0	1	4D	1.260
0	1	0	0	1	1	1	0	4E	1.270
0	1	0	0	1	1	1	1	4F	1.280
0	1	0	1	0	0	0	0	50	1.290
0	1	0	1	0	0	0	1	51	1.300

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	0	1	0	0	1	0	52	1.310
0	1	0	1	0	0	1	1	53	1.320
0	1	0	1	0	1	0	0	54	1.330
0	1	0	1	0	1	0	1	55	1.340
0	1	0	1	0	1	1	0	56	1.350
0	1	0	1	0	1	1	1	57	1.360
0	1	0	1	1	0	0	0	58	1.370
0	1	0	1	1	0	0	1	59	1.380
0	1	0	1	1	0	1	0	5A	1.390
0	1	0	1	1	0	1	1	5B	1.400
0	1	0	1	1	1	0	0	5C	1.410
0	1	0	1	1	1	0	1	5D	1.420
0	1	0	1	1	1	1	0	5E	1.430
0	1	0	1	1	1	1	1	5F	1.440
0	1	1	0	0	0	0	0	60	1.450
0	1	1	0	0	0	0	1	61	1.460
0	1	1	0	0	0	1	0	62	1.470
0	1	1	0	0	0	1	1	63	1.480
0	1	1	0	0	1	0	0	64	1.490
0	1	1	0	0	1	0	1	65	1.500
0	1	1	0	0	1	1	0	66	1.510
0	1	1	0	0	1	1	1	67	1.520
0	1	1	0	1	0	0	0	68	1.530
0	1	1	0	1	0	0	1	69	1.540
0	1	1	0	1	0	1	0	6A	1.550
0	1	1	0	1	0	1	1	6B	1.560
0	1	1	0	1	1	0	0	6C	1.570
0	1	1	0	1	1	0	1	6D	1.580
0	1	1	0	1	1	1	0	6E	1.590
0	1	1	0	1	1	1	1	6F	1.600
0	1	1	1	0	0	0	0	70	1.610
0	1	1	1	0	0	0	1	71	1.620
0	1	1	1	0	0	1	0	72	1.630
0	1	1	1	0	0	1	1	73	1.640
0	1	1	1	0	1	0	0	74	1.650
0	1	1	1	0	1	0	1	75	1.660
0	1	1	1	0	1	1	0	76	1.670
0	1	1	1	0	1	1	1	77	1.680
0	1	1	1	1	0	0	0	78	1.690
0	1	1	1	1	0	0	1	79	1.700
0	1	1	1	1	0	1	0	7A	1.710

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	1	1	1	0	1	1	7B	1.720
0	1	1	1	1	1	0	0	7C	1.730
0	1	1	1	1	1	0	1	7D	1.740
0	1	1	1	1	1	1	0	7E	1.750
0	1	1	1	1	1	1	1	7F	1.760
1	0	0	0	0	0	0	0	80	1.770
1	0	0	0	0	0	0	1	81	1.780
1	0	0	0	0	0	1	0	82	1.790
1	0	0	0	0	0	1	1	83	1.800
1	0	0	0	0	1	0	0	84	1.810
1	0	0	0	0	1	0	1	85	1.820
1	0	0	0	0	1	1	0	86	1.830
1	0	0	0	0	1	1	1	87	1.840
1	0	0	0	1	0	0	0	88	1.850
1	0	0	0	1	0	0	1	89	1.860
1	0	0	0	1	0	1	0	8A	1.870
1	0	0	0	1	0	1	1	8B	1.880
1	0	0	0	1	1	0	0	8C	1.890
1	0	0	0	1	1	0	1	8D	1.900
1	0	0	0	1	1	1	0	8E	1.910
1	0	0	0	1	1	1	1	8F	1.920
1	0	0	1	0	0	0	0	90	1.930
1	0	0	1	0	0	0	1	91	1.940
1	0	0	1	0	0	1	0	92	1.950
1	0	0	1	0	0	1	1	93	1.960
1	0	0	1	0	1	0	0	94	1.970
1	0	0	1	0	1	0	1	95	1.980
1	0	0	1	0	1	1	0	96	1.990
1	0	0	1	0	1	1	1	97	2.000
1	0	0	1	1	0	0	0	98	2.010
1	0	0	1	1	0	0	1	99	2.020
1	0	0	1	1	0	1	0	9A	2.030
1	0	0	1	1	0	1	1	9B	2.040
1	0	0	1	1	1	0	0	9C	2.050
1	0	0	1	1	1	0	1	9D	2.060
1	0	0	1	1	1	1	0	9E	2.070
1	0	0	1	1	1	1	1	9F	2.080
1	0	1	0	0	0	0	0	A0	2.090
1	0	1	0	0	0	0	1	A1	2.100
1	0	1	0	0	0	1	0	A2	2.110
1	0	1	0	0	0	1	1	A3	2.120

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	1	0	0	1	0	0	A4	2.130
1	0	1	0	0	1	0	1	A5	2.140
1	0	1	0	0	1	1	0	A6	2.150
1	0	1	0	0	1	1	1	A7	2.160
1	0	1	0	1	0	0	0	A8	2.170
1	0	1	0	1	0	0	1	A9	2.180
1	0	1	0	1	0	1	0	AA	2.190
1	0	1	0	1	0	1	1	AB	2.200
1	0	1	0	1	1	0	0	AC	2.210
1	0	1	0	1	1	0	1	AD	2.220
1	0	1	0	1	1	1	0	AE	2.230
1	0	1	0	1	1	1	1	AF	2.240
1	0	1	1	0	0	0	0	B0	2.250
1	0	1	1	0	0	0	1	B1	2.260
1	0	1	1	0	0	1	0	B2	2.270
1	0	1	1	0	0	1	1	B3	2.280
1	0	1	1	0	1	0	0	B4	2.290
1	0	1	1	0	1	0	1	B5	2.300
1	0	1	1	0	1	1	0	B6	2.310
1	0	1	1	0	1	1	1	B7	2.320
1	0	1	1	1	0	0	0	B8	2.330
1	0	1	1	1	0	0	1	B9	2.340
1	0	1	1	1	0	1	0	BA	2.350
1	0	1	1	1	0	1	1	BB	2.360
1	0	1	1	1	1	0	0	BC	2.370
1	0	1	1	1	1	0	1	BD	2.380
1	0	1	1	1	1	1	0	BE	2.390
1	0	1	1	1	1	1	1	BF	2.400
1	1	0	0	0	0	0	0	C0	2.410
1	1	0	0	0	0	0	1	C1	2.420
1	1	0	0	0	0	1	0	C2	2.430
1	1	0	0	0	0	1	1	C3	2.440
1	1	0	0	0	1	0	0	C4	2.450
1	1	0	0	0	1	0	1	C5	2.460
1	1	0	0	0	1	1	0	C6	2.470
1	1	0	0	0	1	1	1	C7	2.480
1	1	0	0	1	0	0	0	C8	2.490
1	1	0	0	1	0	0	1	C9	2.500
1	1	0	0	1	0	1	0	CA	2.510
1	1	0	0	1	0	1	1	CB	2.520
1	1	0	0	1	1	0	0	CC	2.530

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	0	0	1	1	0	1	CD	2.540
1	1	0	0	1	1	1	0	CE	2.550
1	1	0	0	1	1	1	1	CF	2.560
1	1	0	1	0	0	0	0	D0	2.570
1	1	0	1	0	0	0	1	D1	2.580
1	1	0	1	0	0	1	0	D2	2.590
1	1	0	1	0	0	1	1	D3	2.600
1	1	0	1	0	1	0	0	D4	2.610
1	1	0	1	0	1	0	1	D5	2.620
1	1	0	1	0	1	1	0	D6	2.630
1	1	0	1	0	1	1	1	D7	2.640
1	1	0	1	1	0	0	0	D8	2.650
1	1	0	1	1	0	0	1	D9	2.660
1	1	0	1	1	0	1	0	DA	2.670
1	1	0	1	1	0	1	1	DB	2.680
1	1	0	1	1	1	0	0	DC	2.690
1	1	0	1	1	1	0	1	DD	2.700
1	1	0	1	1	1	1	0	DE	2.710
1	1	0	1	1	1	1	1	DF	2.720
1	1	1	0	0	0	0	0	E0	2.730
1	1	1	0	0	0	0	1	E1	2.740
1	1	1	0	0	0	1	0	E2	2.750
1	1	1	0	0	0	1	1	E3	2.760
1	1	1	0	0	1	0	0	E4	2.770
1	1	1	0	0	1	0	1	E5	2.780
1	1	1	0	0	1	1	0	E6	2.790
1	1	1	0	0	1	1	1	E7	2.800
1	1	1	0	1	0	0	0	E8	2.810
1	1	1	0	1	0	0	1	E9	2.820
1	1	1	0	1	0	1	0	EA	2.830
1	1	1	0	1	0	1	1	EB	2.840
1	1	1	0	1	1	0	0	EC	2.850
1	1	1	0	1	1	0	1	ED	2.860
1	1	1	0	1	1	1	0	EE	2.870
1	1	1	0	1	1	1	1	EF	2.880
1	1	1	1	0	0	0	0	F0	2.890
1	1	1	1	0	0	0	1	F1	2.900
1	1	1	1	0	0	1	0	F2	2.910
1	1	1	1	0	0	1	1	F3	2.920
1	1	1	1	0	1	0	0	F4	2.930
1	1	1	1	0	1	0	1	F5	2.940

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	1	1	0	1	1	0	F6	2.950
1	1	1	1	0	1	1	1	F7	2.960
1	1	1	1	1	0	0	0	F8	2.970
1	1	1	1	1	0	0	1	F9	2.980
1	1	1	1	1	0	1	0	FA	2.990
1	1	1	1	1	0	1	1	FB	3.000
1	1	1	1	1	1	0	0	FC	3.010
1	1	1	1	1	1	0	1	FD	3.020
1	1	1	1	1	1	1	0	FE	3.030
1	1	1	1	1	1	1	1	FF	3.040

Table 2. Standard Serial VID Commands

Code	Commands	Master Payload Contents	Slave Payload Contents	Description
00h	not supported	N/A	N/A	N/A
01h	SetVID_Fast	VID code	N/A	1. Set new target VID code, VR jumps to new VID target with slew rate set by SET3 pin. 2. Set VR_Settled when VR reaches target VID voltage.
02h	SetVID_Slow	VID code	N/A	1. Set new target VID code, VR jumps to new VID target with programmable slew rate through register 2Ah as a fraction of the fast slew rate. 2. Set VR_Settled when VR reaches target VID voltage.
03h	SetVID_Decay	VID code	N/A	1. Set new target VID code, VR jumps to new VID target, but does not control the slew rate. The output voltage decays at a rate proportional to the load current. 2. Low side MOSFET is not allowed to sync current. 3. ACK 11b when target higher than current VOUT voltage. 4. ACK 10b when target lower than current VOUT voltage.
04h	SetPS	Byte indicating power states	N/A	1. Set power state. 2. ACK 11b when not support. 3. ACK 10b even slave not change configuration. 4. ACK 11b for still running SetVID command. 5. VR remains in lower state when receiving SetVID (decay).
05h	SetRegADR	Pointer of registers in data table	N/A	1. Set the pointer of the data register. 2. ACK 11b for address outside of support. 3. NAK 01b for SetADR (all call).
06h	SetReg DAT	New data register content	N/A	1. Write the contents to the data register. 2. NAK 01b for SetReg (all call).
07h	GetReg		Specified Register Contents	1. Slave returns the contents of the specified register as the payload. 2. ACK 11b for non support address. 3. NAK 01b for GetReg (all call).
08h to 1Fh	not supported	N/A	N/A	N/A

Table3. SVID Data and Configuration Register

Index	Register Name	Description	Access	Default
00h	Vendor ID	Vendor ID	RO, Vendor	1Eh
01h	Product ID	Product ID	RO, Vendor	84h
02h	Product Revision	Product Revision	RO, Vendor	00h
05h	Protocol ID	SVID Protocol ID	RO, Vendor	02h
06h	Capability	Bit mapped register, identifies the SVID VR Capabilities and which of the optional telemetry register is supported.	RO, Vendor	81h
10h	Status_1	Data register containing the status of VR.	R-M, W-PWM	00h
11h	Status_2	Data register containing the status of transmission.	R-M, W-PWM	00h
12h	Temperature Zone	Data register showing temperature zone that has been entered.	R-M, W-PWM	00h
15h	IOUT	At PS0 to PS2, IOUT report data from ADC sense IMON voltage. When power state at PS3, the IOUT report data is fix to 04h.	R-M, W-PWM	00h
1Ch	Status_2_lastread	The register contains a copy of the status_2.	R-M, W-PWM	00h
21h	ICC Max	Data register containing the ICC max the platform supports. Binary format in A IE 64h = 100A.	RO, Platform	7Dh
22h	Temp Max	Data register containing the temperature max the platform supports. Binary format in °C IE 64h = 100°C.	RO, Platform	64h
24h	SR-fast	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/μS IE 0Ch = 12mV/μs.	RO	0Ch
25h	SR-slow	Data register containing the capability of slow slew rate. Binary format in mV/μS IE 03h = 3mV/μS.	RO	03h
2Ah	Slow Slew Rate Selector	The register is programmed by master and set the slow slew rate.	RW, Master	02h
2Bh	PS4 Exit Latency	Data register containing the latency of exiting PS4.	RO	7Fh
2Ch	PS3 Exit Latency	Data register containing the latency of exiting PS3.	RO	3Fh
2Dh	Enable to Ready for SVID	Data register containing the latency from Enable assertion to the VR being ready to accept an SVID command.	RO	BFh
30h	VOUT Max	The register is programmed by master and sets the maximum VID.	RW, Master	D5h
31h	VID Setting	Data register containing currently programmed VID.	RW, Master	00h
32h	Power State	Register containing the current programmed power state.	RW, Master	00h
33h	Offset	Set offset in VID steps.	RW, Master	00h
34h	Multi VR Configuration	Bit mapped data register which configures multiple VRs behavior on the same bus.	RW, Master	00h
35h	Pointer	Scratch pad register for temporary storage of the SetRegADR pointer register.	RW, Master	30h

Notes :

RO = Read Only

RW = Read/Write

R-M = Read by Master

W-PWM = Write by PWM Only

Vendor = Hard Coded by VR Vendor

Platform = Programmed by the Master

PWM = Programmed by the VR Control IC

Absolute Maximum Ratings (Note 1)

- VCC, PVCC to GND ---------- –0.3V to 6V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET to GND ---------- –0.3V to 28V
- BOOT to PHASE ---------- –0.3V to 6.5V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns ---------- –8V to 38V
- LGATE to GND
  - DC ---------- (GND – 0.3V) to (PVCC + 0.3V)
  - < 20ns ---------- (GND – 5V) to (PVCC + 5V)
- UGATE to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 20ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  - WQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W
  - WQFN-32L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, PVCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	V_{EN} = H, No switching	--	4.1	--	mA
Supply Current at PS3	I_{VCC_PS3}	V_{EN} = H, No switching	--	2.7	--	mA
Supply Current at PS4	I_{VCC_PS4}	V_{EN} = H, No switching	--	--	200	μA
Power Supply Voltage	PVCC		4.5	--	5.5	V
Power Supply Current	I_{PVCC}		--	80	--	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference and DAC						
DAC Accuracy	V_{FB}	V_{DAC} = 1.5V – 2.3V	–0.5	0	0.5	% of VID
		V_{DAC} = 1V – 1.49V	–8	0	8	mV
		V_{DAC} = 0.5V – 0.99V	–10	0	10	
PVCC Power On Reset (POR)						
POR Threshold	V_{POR_r}	PVCC Rising	--	4.2	4.5	V
	V_{POR_f}	PVCC Falling	3.5	3.84	--	
POR Hysteresis	V_{POR_HYS}		--	360	--	mV
Slew Rate						
Dynamic VID Slew Rate	SR	SetVID slow pin, setting SR = 00	3	3.3	3.75	mV/μs
		SetVID slow pin, setting SR = 01	6	6.6	7.5	
		SetVID slow pin, setting SR = 10	9	9.9	11.25	
		SetVID slow pin, setting SR = 11	12	13.2	15	
		SetVID fast pin, setting SR = 00	12	13.2	15	
		SetVID fast pin, setting SR = 01	24	26.4	30	
		SetVID fast pin, setting SR = 10	36	39.6	45	
		SetVID fast pin, setting SR = 11	48	52.8	60	
EA Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ	70	--	--	Db
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5Pf	4	5	--	MHz
Slew Rate	SR_{EA}	C_{LOAD} = 10Pf (Gain = –4, R_F = 47kΩ, V_{OUT} = 0.5V to –3V)	5	--	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
Maximum Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Load Line Current Gain Amplifier						
Input Offset Voltage	V_{ILOFS}	V_{IMON} = 1V	–5	--	5	mV
Current Gain	A_{ILGAIN}	$V_{IMON} - V_{VREF}$ = 1V, $V_{FB} = V_{COMP}$ = 1.75V	--	1/4	--	A/A
Current Sensing Amplifier						
Input Offset Voltage	V_{OSCS}		–0.8	--	0.8	mV
Impedance at Positive Input	R_{ISENP}		1	--	--	MΩ
Current Mirror Gain	A_{MIRROR}	I_{IMON} / I_{SENN}	0.97	1	1.03	A/A
Current Sensing Voltage	V_{CS}		–9	--	150	mV
TON Setting						
TONSET Pin Voltage	V_{TON}	I_{RTON} = 20μA, V_{DAC} = 1.7V	1.6	1.7	1.8	V
On-Time Setting	T_{ON}	I_{RTON} = 20μA, V_{DAC} = 1.7V	450	500	550	ns
Input Current Range	I_{RTON}	V_{DAC} = 1.7V	6	--	100	μA
Minimum Off-time	T_{OFF}	V_{DAC} = 1.7V	--	250	--	ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS							
IBIAS Pin Voltage		V_{IBIAS}	R_{IBIAS} = 100kΩ	1.85	2	--	V
Protections							
Under Voltage Lockout Threshold		V_{UVLO}		4.1	4.3	4.45	V
		ΔV_{UVLO}	Falling edge hysteresis	--	200	--	mV
Over Voltage Protection Threshold		V_{OV}	VID higher than 1.5V	VID + 300	VID + 350	VID + 400	mV
			VID lower than 1.5V	1800	1850	1900	
Under Voltage Protection Threshold		V_{UV}	Respect to VID voltage	–400	–350	–300	mV
Negative Voltage Protection Threshold		V_{NV}		–100	–70	--	mV
EN and VR_RDY							
EN Input Voltage	Logic-High	V_{IH}		0.7	--	--	V
	Logic-Low	V_{IL}		--	--	0.3	
Leakage Current of EN				–1	--	1	μA
VR_RDY Delay		T_{VR_RDY}	V_{SEN} = VBoot to VR_RDY High	3	4.5	6	μs
VR_RDY Pull Low Voltage		V_{PGOOD}	I_{VR_RDY} = 10mA	--	--	0.13	V
Serial VID and $\overline{VR\_HOT}$							
VCLK, VDIO		V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
		V_{IL}		--	--	0.45	
Leakage Current of VCLK, VDIO, $\overline{ALERT}$ and $\overline{VR\_HOT}$		I_{LEAK_IN}		–1	--	1	μA
VDIO, $\overline{ALERT}$ and $\overline{VR\_HOT}$ Pull Low Voltage			I_{VDIO} = 10mA	--	--	0.13	V
			$I_{\overline{ALERT}}$ = 10mA				
			$I_{\overline{VR\_HOT}}$ = 10mA				
V_{REF} and V_{BOOT}							
V_{REF} Voltage		V_{REF}		0.55	0.6	0.65	V
V_{BOOT} Voltage		V_{BOOT}	V_{BOOT} Voltage set to 1.7V	1.692	1.7	1.708	V
ADC							
Digital IMON Set		V_{IMON}	V_{IMON} – V_{IMON_INI} = 1.6V	252	255	258	Decimal
			V_{IMON} – V_{IMON_INI} = 0.8V	125	128	131	
			V_{IMON} – V_{IMON_INI} = 0V	0	0	3	
Update Period of IMON		T_{IMON}		--	200	--	μs
TSEN Threshold for Tmp_Zone [7] transition		V_{TSEN}	100°C	--	1.887	--	V
TSEN Threshold for Tmp_Zone [6] transition		V_{TSEN}	97°C	--	1.837	--	V
TSEN Threshold for Tmp_Zone [5] transition		V_{TSEN}	94°C	--	1.784	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSEN Threshold for Tmp_Zone [4] transition	V_{TSEN}	91°C	--	1.729	--	V
TSEN Threshold for Tmp_Zone [3] transition	V_{TSEN}	88°C	--	1.672	--	V
TSEN Threshold for Tmp_Zone [2] transition	V_{TSEN}	85°C	--	1.612	--	V
TSEN Threshold for Tmp_Zone [1] transition	V_{TSEN}	82°C	--	1.551	--	V
TSEN Threshold for Tmp_Zone [0] transition	V_{TSEN}	75°C	--	1.402	--	V
Update Period of TSEN	t_{TSEN}		--	50	--	μs
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 0.403V	58	64	70	Decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 0.806V	122	128	134	
	$C_{ICCMAX3}$	V_{ICCMAX} = 1.6V	248	256	260	
Driver Enable Driving Capability						
DRV_EN Source Resistance	$R_{DRV\_EN\_SRC}$		--	--	30	Ω
DRV_EN Sink Resistance	$R_{DRV\_EN\_SNK}$		--	--	10	Ω
Switching Time						
UGATE Rise Time	t_{UGATEr}	3nF load	--	8	--	ns
UGATE Fall Time	t_{UGATEf}	3nF load	--	8	--	ns
LGATE Rise Time	t_{LGATEr}	3nF load	--	8	--	ns
LGATE Fall Time	t_{LGATEf}	3nF load	--	4	--	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	Outputs Unloaded	--	20	--	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	Outputs Unloaded	--	20	--	ns
Output						
UGATE Driver Source Resistance	$R_{UGATEsr}$	100mA Source Current	--	1	--	Ω
UGATE Driver Sink Resistance	$R_{UGATEsk}$	100mA Sink Current	--	1	--	Ω
LGATE Driver Source Resistance	$R_{LGATEsr}$	100mA Source Current	--	1	--	Ω
LGATE Driver Sink Resistance	$R_{LGATEsk}$	100mA Sink Current	--	0.5	--	Ω

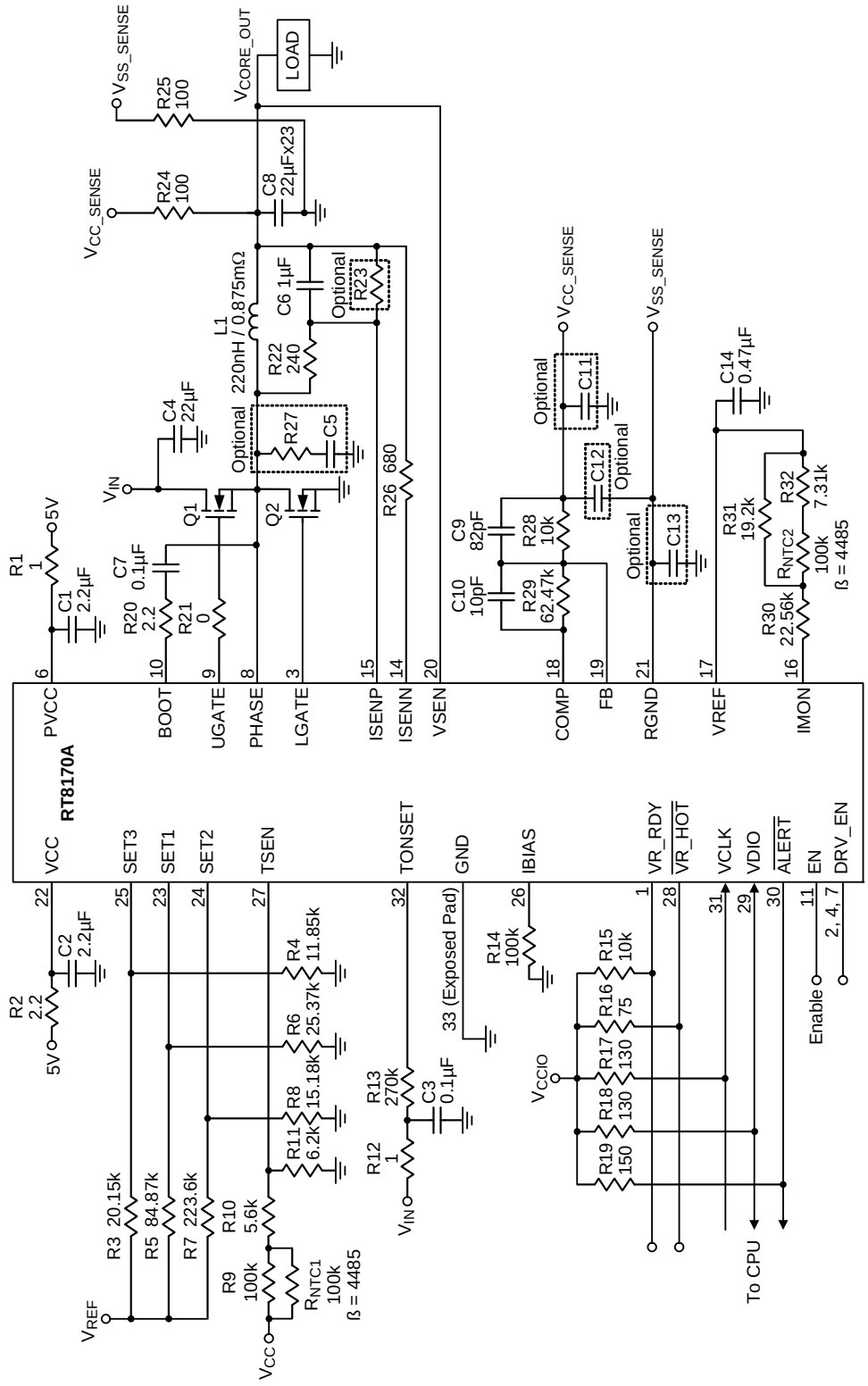
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

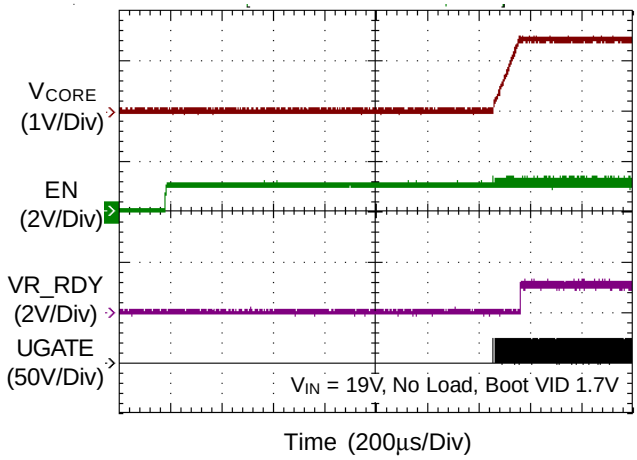
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

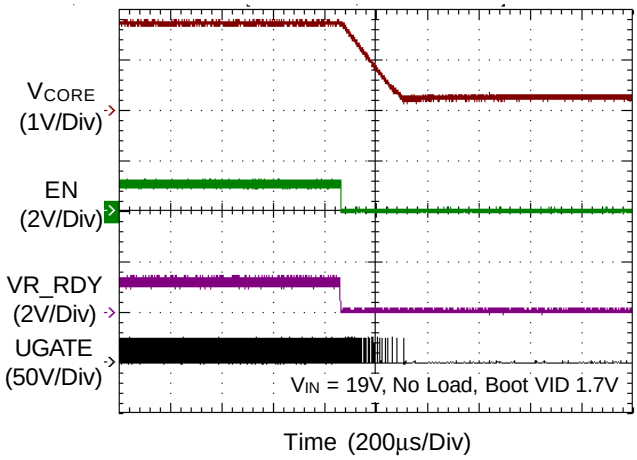


Typical Operating Characteristics

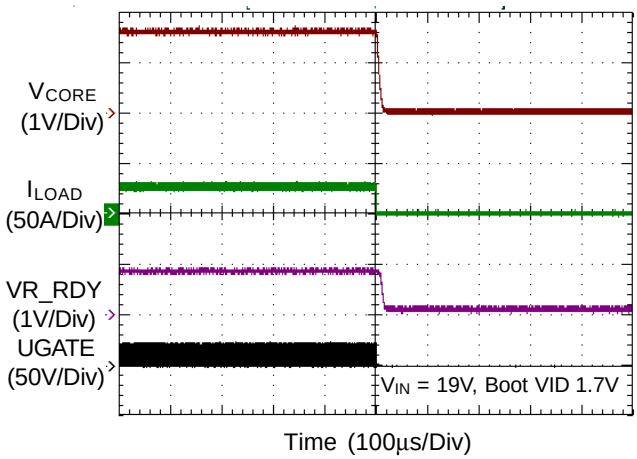
CORE VR Power On from EN



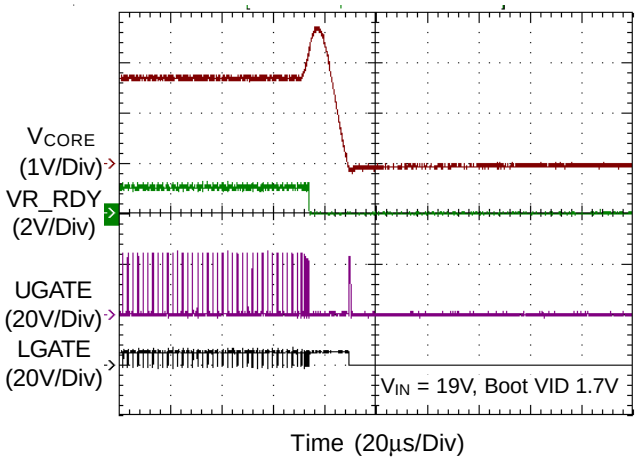
CORE VR Power Off from EN



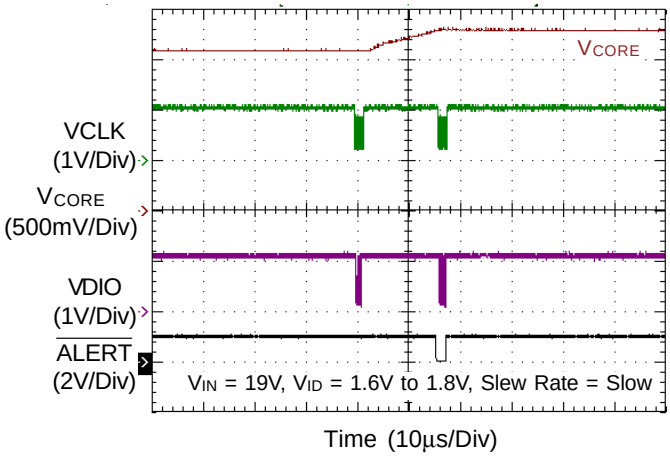
CORE VR OCP



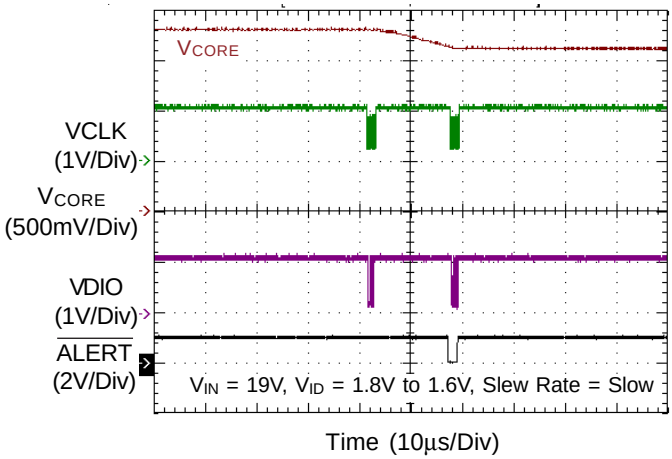
CORE VR OVP



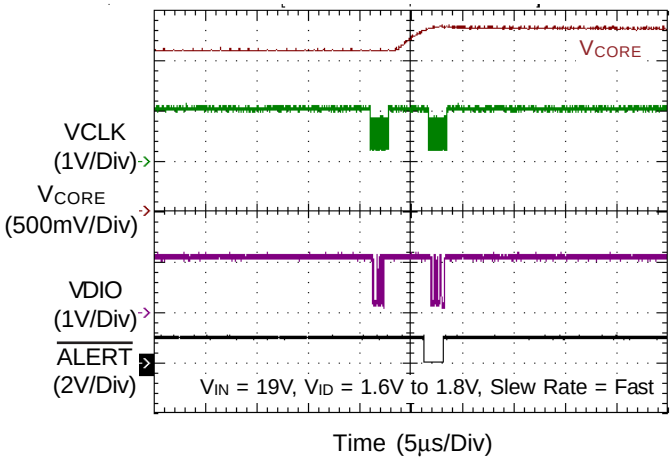
CORE VR Dynamic VID Up



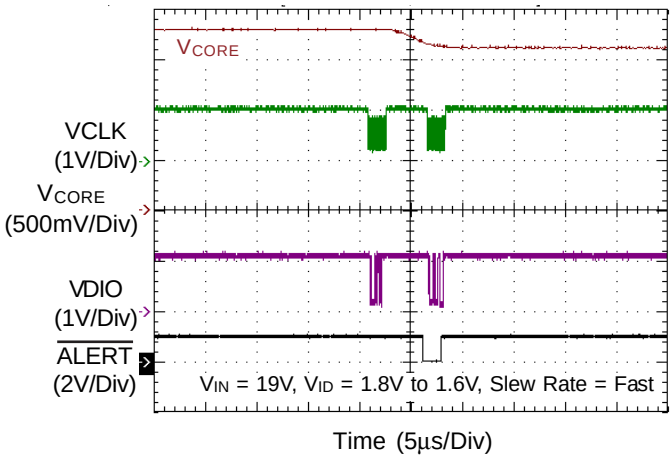
CORE VR Dynamic VID Down



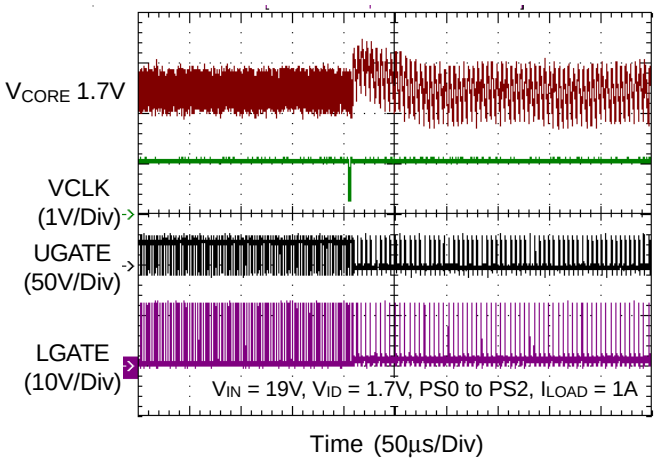
CORE VR Dynamic VID Up



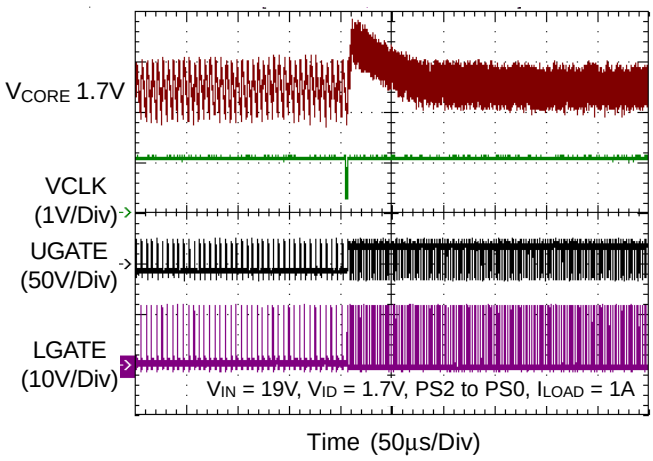
CORE VR Dynamic VID Down



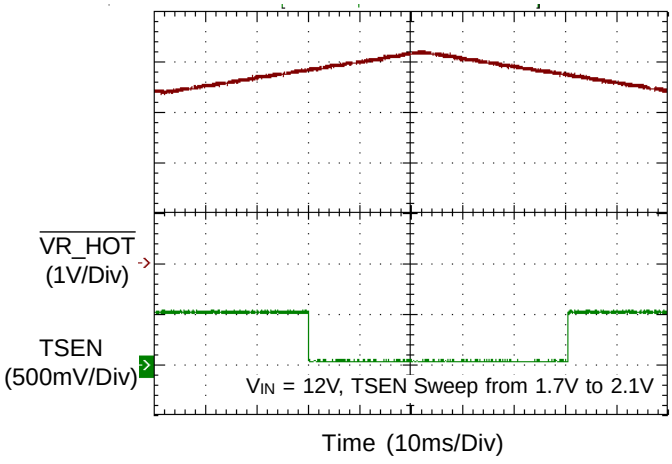
CORE VR Mode Transient



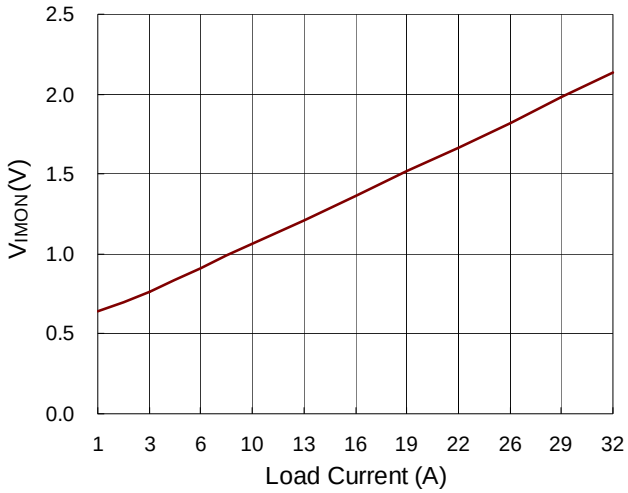
CORE VR Mode Transient



CORE VR Thermal Monitoring



VIMON vs. Load Current



Applications information

The RT8170A is a single phase synchronous Buck controller designed to meet Intel VR12.5 and VR12.6 compatible CPU specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save a total number of pins for easily using and increasing PCB space utilization.

G-NAVP™ Control Mode

The RT8170A adopts the G-NAVP™ controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. For the RT8170A, when current feedback signal reaches comp signal to generate an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms in continuous conduct mode (CCM).

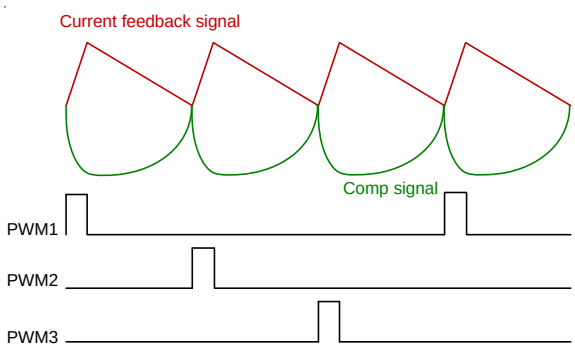


Figure 1 (a). G-NAVP™ Behavior Waveforms in CCM in Steady State

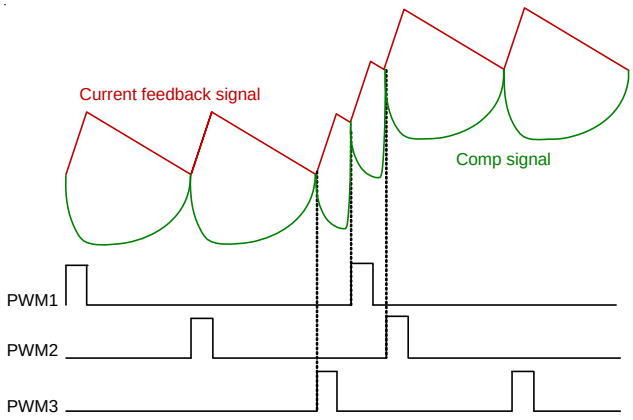


Figure 1 (b). G-NAVP™ Behavior Waveforms in CCM in Load Transient

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. The RT8170A can operate in Diode Emulation Mode (DEM) in order to improve light load efficiency. In DEM operation, the behavior of the low-side MOSFET needs to work like a diode, that is, the low-side MOSFET will be turned on when the phase voltage is a negative value, i.e. the inductor current follows from Source to Drain of low-side MOSFET. The low-side MOSFET will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. The positive voltage threshold (ZCD threshold) of low-side MOSFET turn off is set by the SET3 pin in Table 9. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching losses will be reduced to improve efficiency in light load condition.

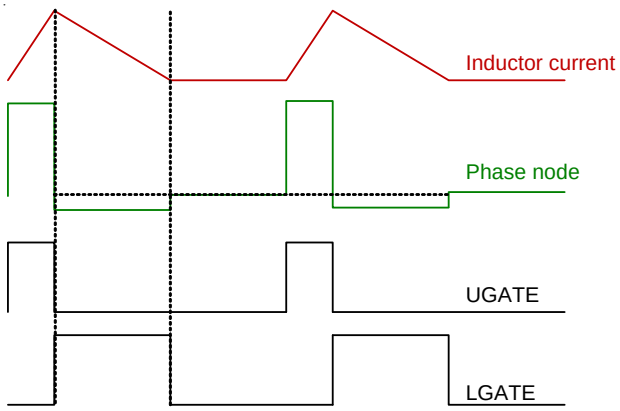
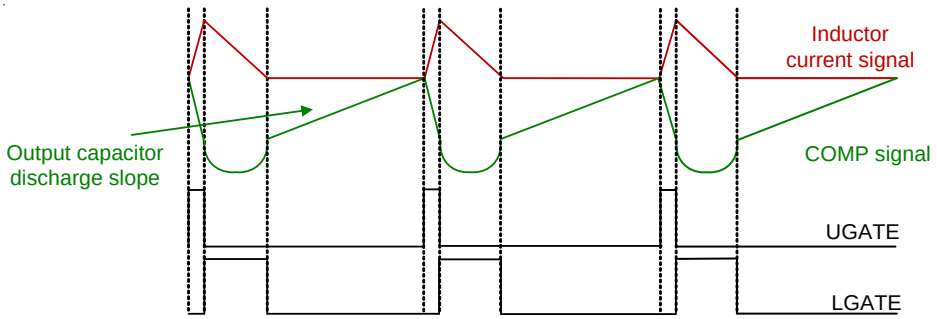
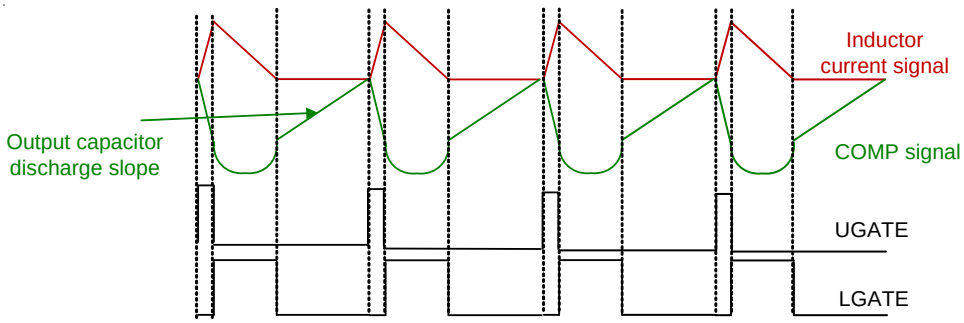


Figure 2. Diode Emulation Mode (DEM) in Steady State



(a) Lighter Load Condition in DEM.

Capacitor discharge slope is lower than Figure 3 (b).



(b) Load Increased Condition in DEM.

Capacitor discharge slope is Higher than Figure 3 (a).

Figure 3. G-NAVP™ Operation in DEM.

Switching Frequency (TON) Setting

The RT8170A is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time with input voltage and VID code to obtain a constant current ripple. So that the output voltage ripple can be controlled nearly like a constant as different input and output voltage change. Connect a resistor R_{TON} between input terminal and the TONSET pin to set the on-time width.

$$T_{ON} = \frac{R_{TON} \times C \times 0.55}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 2.2V)$$

$$T_{ON} = \frac{R_{TON} \times C \times V_{DAC} / 4}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 2.2V)$$

Where C = 18.2pF. By using the relationship between T_{ON} and f_{SW}, the switching frequency f_{SW} is :

$$f_{SW(MAX)} = \left(\frac{1}{T_{ON(MAX)}}\right) \times \left(\frac{V_{DAC(MAX)}}{V_{IN(MAX)}}\right)$$

Where

$F_{SW(MAX)}$ is the maximum switching frequency.

$V_{DAC(MAX)}$ is the maximum VDAC of application.

$V_{IN(MAX)}$ is the maximum application input voltage.

$T_{ON(MAX)}$ is derived from TON equation with maximum parameters ($V_{IN(MAX)}$, $V_{DAC(MAX)}$).

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence, the loading current increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Per Phase Current Sense

In the RT8170A, the current signal is used for load-line setting and OC (Over Current) protection. The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in the Figure 4. When inductance and DCR time constant is equal to R_XC_X filter network time constant, a voltage I_{LX} x DCR will drop on C_X to generate inductor current signal. According to the Figure 4, the ISENN is as follows :

$$ISENN = \frac{I_{LX} \times DCR}{R_{CSx}}$$

Where LX / DCR = R_XC_X is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, a NTC resistor should add in the resistor network in the IMON pin to achieve DCR thermal compensation.

If 3 x I_{CCMAX} x DCR is larger than 150mV, the current sense method II is recommended to prevent current sense amplifier from being saturated. According to Figure 5, the R_X is as follows : $R_X = R_{X1}$ // R_{X2}

The resistance accuracy of R_{CSx} is recommended to be 1% or higher.

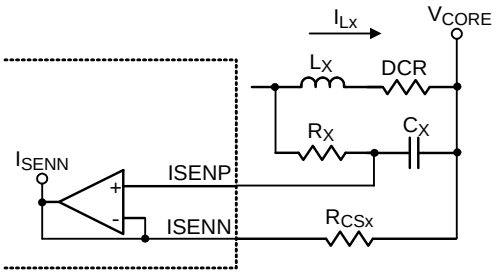


Figure 4. Lossless Current Sense Method I

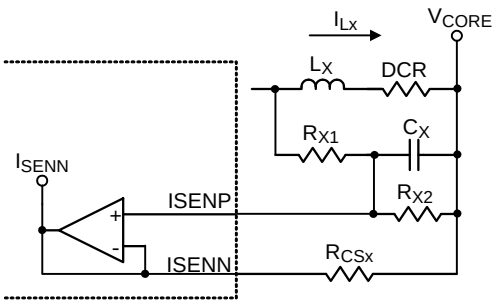


Figure 5. Lossless Current Sense Method II

Total Current Sense

Total current sense method is a patented topology, unlike conventional current sense method requiring a NTC resistor in per phase current loop for thermal compensation. The RT8170A adopts the total current sense method requiring only one NTC resistor for thermal compensation, and NTC resistor cost can be saved by using this method. Figure 6 shows the total current sense method which connects the resistor network between the IMON and VREF pins to set a part of current loop gain for load-line (droop) setting and set accurate over current protection.

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times I_{L1}$$

R_{EQ} includes a NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

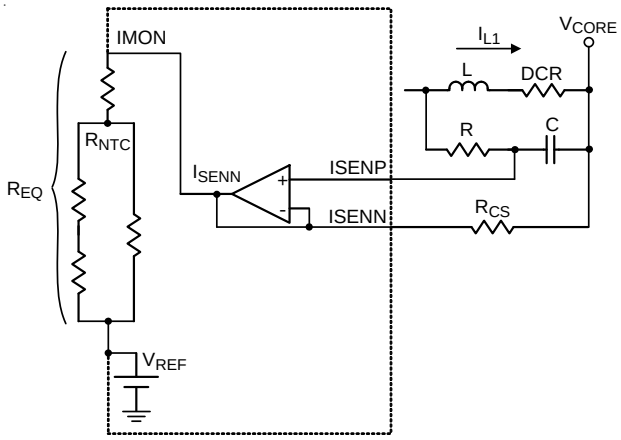


Figure 6. Total Current Sense Method

Load-Line (Droop) Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current I_{CC} and output voltage V_{CORE} as shown in Figure 7. Figure 8 shows the voltage control and current loop. By using both loops, the load-line (droop) can easily be set. The load-line set equation is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{4} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} \ (m\Omega)$$

The load-line can be set to zero by SET3 pin.

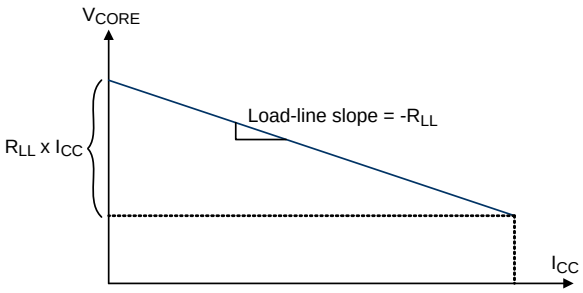


Figure 7. Load-Line (Droop)

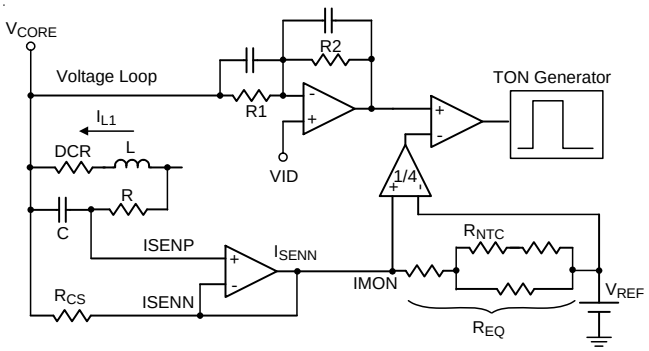


Figure 8. Voltage Loop and Current Loop

Compensator Design

The compensator of the RT8170A doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to achieve constant output impedance design for Intel VR12.5 and VR12.6 ACLL specification. The one pole one zero compensator is shown as Figure 9, the transfer function of compensator should be designed as the following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range :

$$G_{CON}(s) \approx \frac{A_I}{R_{LL}} \times \frac{1 + \frac{s}{\pi \times fsw}}{1 + \frac{s}{\omega_{ESR}}}$$

Where A_I is current loop gain, R_{LL} is load-line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1 / (C_{OUT} x ESR). Then, the C1 and C2 should be designed as follows :

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}}$$

$$C2 = \frac{C_{OUT} \times ESR}{R2}$$

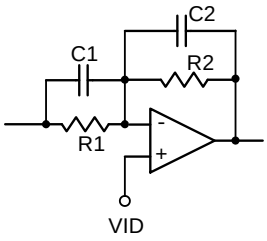


Figure 9. Type I Compensator

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, the SET[1:3] pins adopt the multi-function pin setting mechanism in the RT8170A. Figure 10 illustrates this operating mechanism. The voltage at VREF pin will be pulled up to 3.2V after power ready (POR). First, external voltage divider is to set the function1 and then internal current source 80μA is to set the function2. The setting voltage of function1 and function2 can be represented as follows :

$$V_{FUNCTION1} = \frac{R2}{R1 + R2} \times 3.2V$$

$$V_{FUNCTION2} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$$

All function setting will be done within 500μs after power ready (POR), and the voltage at VREF pin will fix to 0.6V after all function setting over.

If $V_{FUNCTION1}$ and $V_{FUNCTION2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{3.2V \times V_{FUNCTION2}}{80\mu A \times V_{FUNCTION1}}$$

$$R2 = \frac{R1 \times V_{FUNCTION1}}{3.2V - V_{FUNCTION1}}$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SETx resistor network for the RT8170A.

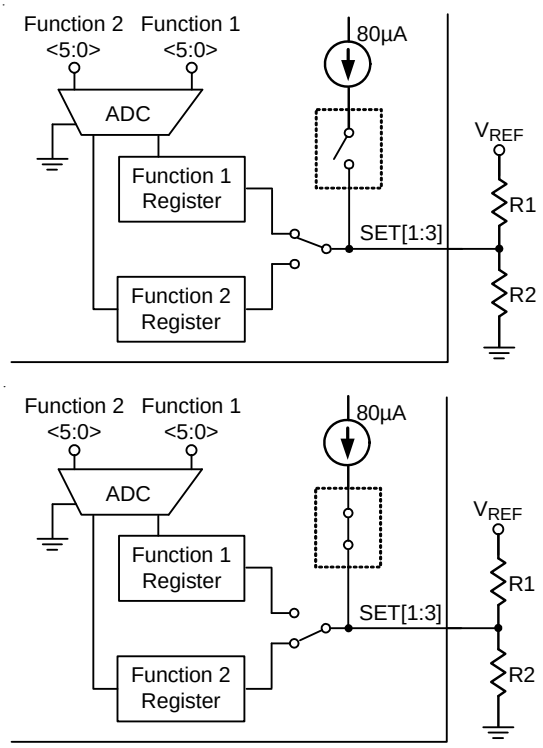
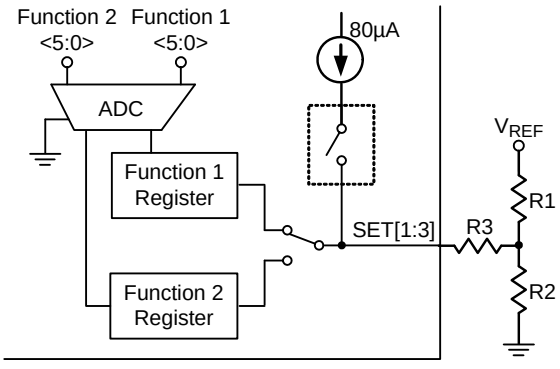


Figure 10. Multi-Function Pin Setting Mechanism

Connecting a R3 resistor from the SET[1:3] pin to the middle node of voltage divider can help to fine tune the set voltage of function 2, which does not affect the set voltage of function 1. The Figure 11 shows the setting method and the set voltage of function 1 and function 2 can be represented as :

$$V_{FUNCTION1} = \frac{R2}{R1 + R2} \times 3.2V$$

$$V_{FUNCTION2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1 + R2} \right)$$



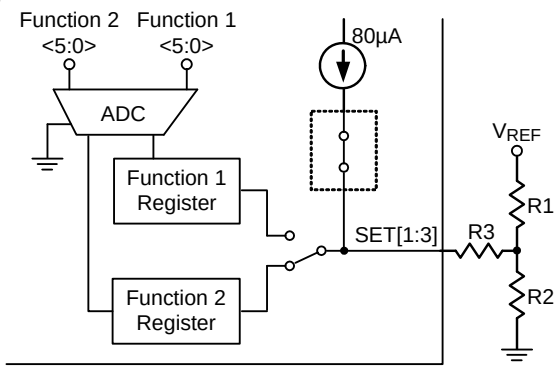


Figure 11. Multi-Function Pin Setting Mechanism with a R3 resistor to fine tune the set voltage of function 2

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, output voltage generate undershoot to fail specification. The RT8170A has a Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can enlarge the on time of PWM signal at instantaneous step-up transient load to restrain the output voltage drooping, Figure 12 shows the QR behavior.

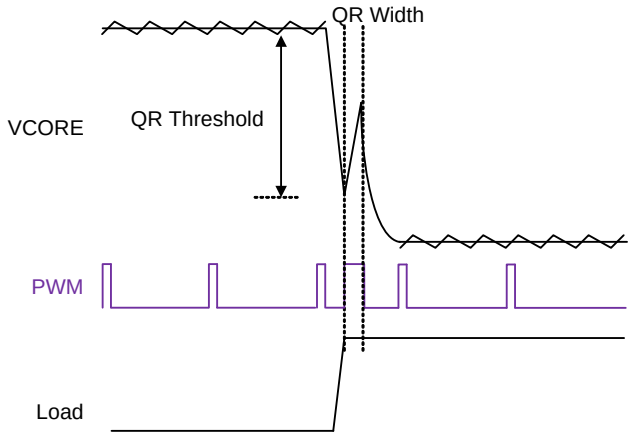


Figure 12. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at the VSEN pin that is shown in Figure 13. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 10. A proper QR mechanism set can meet different applications. The SET2 pin is a multi-function pin which can set QR threshold, QR width and ICCMAX.

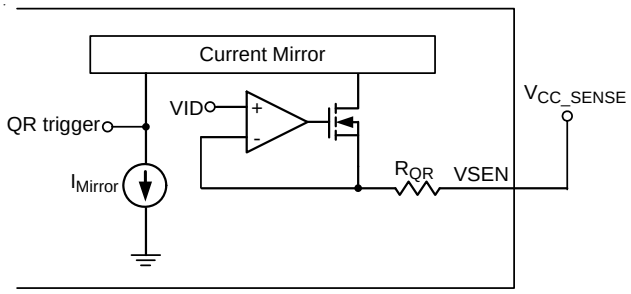


Figure 13. Simplified QR Trigger Schematic

An internal current source 80μA is used in multi-function pin setting mechanism. For example, 20mV QR threshold and 2.66 x TON QR width are set. According to Table 4, the set voltage should be between 0.4504V and 0.4723V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

In the Table 4, there are some "No Use" marks at QRWIDTH section. It means that user should not use it to avoid the possibility of shift digital code due to tolerance concern.

Table 4. SET2 Pin Setting for QR Threshold and QR Width

$V_{QR\_SET} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						QR Threshold	QR Width (%TON)
Min	Typical	Max	unit	QR_TH <2:0>	QRWIDTH <2:0>		
0.000	10.948	21.896	mV	000	000	Disable	No Use
25.024	35.973	46.921	mV		001		310%
50.049	60.997	71.945	mV		010		266%
75.073	86.022	96.970	mV		011		222%
100.098	111.046	121.994	mV		100		178%
125.122	136.070	147.019	mV		101		134%
150.147	161.095	172.043	mV		110		88%
175.171	186.119	197.067	mV		111		No Use
200.196	211.144	222.092	mV	001	000	15mV	No Use
225.220	236.168	247.116	mV		001		310%
250.244	261.193	272.141	mV		010		266%
275.269	286.217	297.165	mV		011		222%
300.293	311.241	322.190	mV		100		178%
325.318	336.266	347.214	mV		101		134%
350.342	361.290	372.239	mV		110		88%
375.367	386.315	397.263	mV		111		No Use
400.391	411.339	422.287	mV	010	000	20mV	No Use
425.415	436.364	447.312	mV		001		310%
450.440	461.388	472.336	mV		010		266%
475.464	486.413	497.361	mV		011		222%
500.489	511.437	522.385	mV		100		178%
525.513	536.461	547.410	mV		101		134%
550.538	561.486	572.434	mV		110		88%
575.562	586.510	597.458	mV		111		No Use
600.587	611.535	622.483	mV	011	000	25mV	No Use
625.611	636.559	647.507	mV		001		310%
650.635	661.584	672.532	mV		010		266%
675.660	686.608	697.556	mV		011		222%
700.684	711.632	722.581	mV		100		178%
725.709	736.657	747.605	mV		101		134%
750.733	761.681	772.630	mV		110		88%
775.758	786.706	797.654	mV		111		No Use
800.782	811.730	822.678	mV	100	000	30mV	No Use
825.806	836.755	847.703	mV		001		310%
850.831	861.779	872.727	mV		010		266%
875.855	886.804	897.752	mV		011		222%
900.880	911.828	922.776	mV		100		178%
925.904	936.852	947.801	mV		101		134%
950.929	961.877	972.825	mV		110		88%
975.953	986.901	997.849	mV		111		No Use

$V_{QR\_SET} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$						QR Threshold	QR Width (%TON)
Min	Typical	Max	unit	QR_TH <2:0>	QRWIDTH <2:0>		
1000.978	1011.926	1022.874	mV	101	000	35mV	No Use
1026.002	1036.950	1047.898	mV		001		310%
1051.026	1061.975	1072.923	mV		010		266%
1076.051	1086.999	1097.947	mV		011		222%
1101.075	1112.023	1122.972	mV		100		178%
1126.100	1137.048	1147.996	mV		101		134%
1151.124	1162.072	1173.021	mV		110		88%
1176.149	1187.097	1198.045	mV		111		No Use
1201.173	1212.121	1223.069	mV	110	000	40mV	No Use
1226.197	1237.146	1248.094	mV		001		310%
1251.222	1262.170	1273.118	mV		010		266%
1276.246	1287.195	1298.143	mV		011		222%
1301.271	1312.219	1323.167	mV		100		178%
1326.295	1337.243	1348.192	mV		101		134%
1351.320	1362.268	1373.216	mV		110		88%
1376.344	1387.292	1398.240	mV		111		No Use
1401.369	1412.317	1423.265	mV	111	000	45mV	No Use
1426.393	1437.341	1448.289	mV		001		310%
1451.417	1462.366	1473.314	mV		010		266%
1476.442	1487.390	1498.338	mV		011		222%
1501.466	1512.414	1523.363	mV		100		178%
1526.491	1537.439	1548.387	mV		101		134%
1551.515	1562.463	1573.412	mV		110		88%
1576.540	1587.488	1598.436	mV		111		No Use

Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop to cause that DVID performance is deteriorated by this induced charge current, the phenomenon is called droop effect. The droop effect is shown in Figure 14. When VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

The RT8170A provides a DVID compensation function. A virtual charge current signal can be established by the SET1 pin to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 16. Figure 15 shows the operation of canceling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal is generated in FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

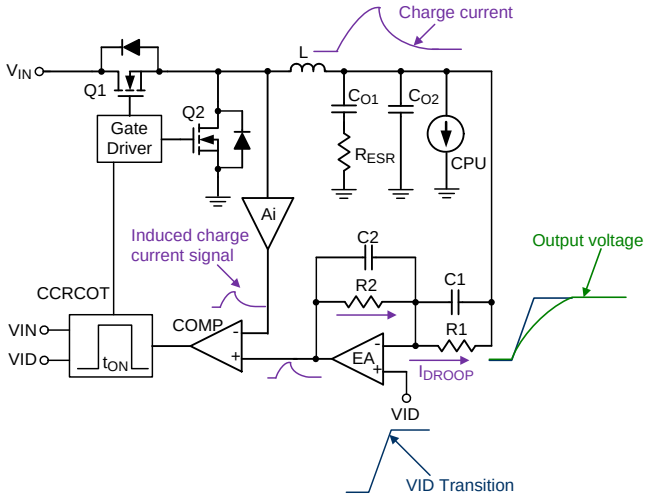


Figure 14. Droop Effect in VID Transition

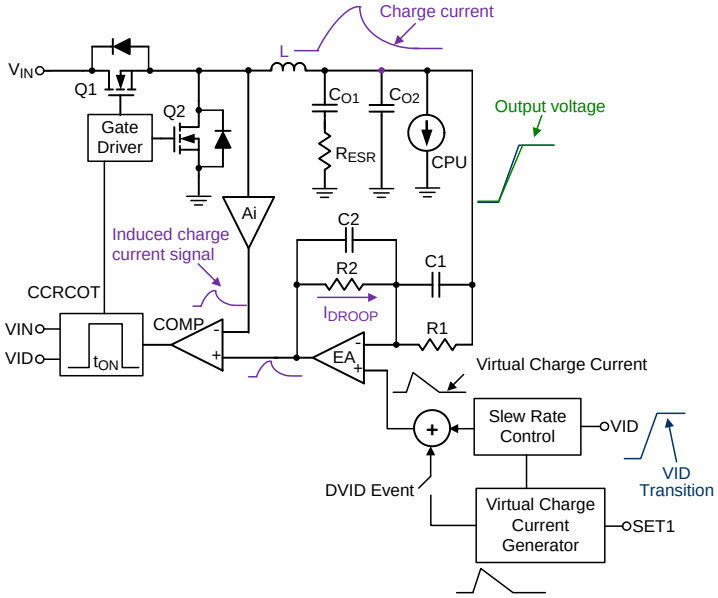


Figure 15. DVID Compensation

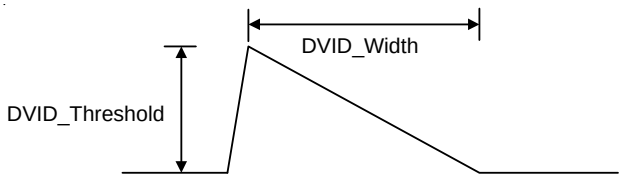


Figure 16. Definition of Virtual Charge Current Signal

Table 5 and Table 6 show the DVID_Threshold and DVID_Width settings in SET1 pin. For example, 25mV DVID_Threshold and 72µs DVID_Width are designed (OCP sets as 100% ICCMAX, and RSET sets as 100% Ramp current). The DVID_Threshold is set by an external voltage divider to set and the DVID_Width is set by an internal current source 80µA by the multi-function pin setting mechanism. According to the Table 5 and Table 6, the DVID_Threshold set voltage should be between 0.225V and 0.247V and the DVID_Width set voltage should be between 0.125V and 0.147V. Please note that a high accuracy resistor is needed for this setting, <1% error tolerance is recommended.

The RT8170A also provides a programmable DVID slew rate function. The DVID slew rate can be set by SET3 pin. Table 8 shows the DVID_Slew Rate setting in SET3 pin. For example, 13.2mV/µs is designed (Disable Anti-Overshoot and zero load-line function). The DVID_Slew Rate setting is set by external voltage divider. According to Table 8, the DVID_Slew Rate set voltage should be between 0.125V and 0.172V.

Table 5. SET1 Pin Setting for DVID_Threshold

$V_{DVID\_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						DVID_Threshold	OCP = %ICCMAX
Min	Typical	Max	unit	DVID_TH <2:0>	OCS <2:0>		
0.000	10.948	21.896	mV	000	000	85mV	No Use
25.024	35.973	46.921	mV		001		100%
50.049	60.997	71.945	mV		010		110%
75.073	86.022	96.970	mV		011		120%
100.098	111.046	121.994	mV		100		130%
125.122	136.070	147.019	mV		101		140%
150.147	161.095	172.043	mV		110		150%
175.171	186.119	197.067	mV		111		No Use
200.196	211.144	222.092	mV	001	000	75mV	No Use
225.220	236.168	247.116	mV		001		100%
250.244	261.193	272.141	mV		010		110%
275.269	286.217	297.165	mV		011		120%
300.293	311.241	322.190	mV		100		130%
325.318	336.266	347.214	mV		101		140%
350.342	361.290	372.239	mV		110		150%
375.367	386.315	397.263	mV		111		No Use
400.391	411.339	422.287	mV	010	000	65mV	No Use
425.415	436.364	447.312	mV		001		100%
450.440	461.388	472.336	mV		010		110%
475.464	486.413	497.361	mV		011		120%
500.489	511.437	522.385	mV		100		130%
525.513	536.461	547.410	mV		101		140%
550.538	561.486	572.434	mV		110		150%
575.562	586.510	597.458	mV		111		No Use
600.587	611.535	622.483	mV	011	000	55mV	No Use
625.611	636.559	647.507	mV		001		100%
650.635	661.584	672.532	mV		010		110%
675.660	686.608	697.556	mV		011		120%
700.684	711.632	722.581	mV		100		130%
725.709	736.657	747.605	mV		101		140%
750.733	761.681	772.630	mV		110		150%
775.758	786.706	797.654	mV		111		No Use
800.782	811.730	822.678	mV	100	000	45mV	No Use
825.806	836.755	847.703	mV		001		100%
850.831	861.779	872.727	mV		010		110%
875.855	886.804	897.752	mV		011		120%
900.880	911.828	922.776	mV		100		130%
925.904	936.852	947.801	mV		101		140%
950.929	961.877	972.825	mV		110		150%
975.953	986.901	997.849	mV		111		No Use

$V_{DVID\_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$						DVID_Threshold	OCP = %ICCMAX
Min	**Typical**	**Max**	**unit**	**DVID_TH <2:0>**	**OCS <2:0>**		
1000.978	1011.926	1022.874	mV	101	000	35mV	No Use
1026.002	1036.950	1047.898	mV		001		100%
1051.026	1061.975	1072.923	mV		010		110%
1076.051	1086.999	1097.947	mV		011		120%
1101.075	1112.023	1122.972	mV		100		130%
1126.100	1137.048	1147.996	mV		101		140%
1151.124	1162.072	1173.021	mV		110		150%
1176.149	1187.097	1198.045	mV		111		No Use
1201.173	1212.121	1223.069	mV	110	000	25mV	No Use
1226.197	1237.146	1248.094	mV		001		100%
1251.222	1262.170	1273.118	mV		010		110%
1276.246	1287.195	1298.143	mV		011		120%
1301.271	1312.219	1323.167	mV		100		130%
1326.295	1337.243	1348.192	mV		101		140%
1351.320	1362.268	1373.216	mV		110		150%
1376.344	1387.292	1398.240	mV		111		No Use
1401.369	1412.317	1423.265	mV	111	000	15mV	No Use
1426.393	1437.341	1448.289	mV		001		100%
1451.417	1462.366	1473.314	mV		010		110%
1476.442	1487.390	1498.338	mV		011		120%
1501.466	1512.414	1523.363	mV		100		130%
1526.491	1537.439	1548.387	mV		101		140%
1551.515	1562.463	1573.412	mV		110		150%
1576.540	1587.488	1598.436	mV		111		No Use

Table 6. SET1 Pin Setting for DVID_Width

$V_{DVID\_Width} = \frac{R2}{R1+R2} \times 3.2V$						RSET % 543k R_{TON}	DVID_Width
Min	Typical	Max	unit	RSET <3:0>	DVID_WTH <1:0>		
0.000	10.948	21.896	mV	0000	00	83%	No Use
25.024	35.973	46.921	mV		01		72µs
50.049	60.997	71.945	mV		10		96µs
75.073	86.022	96.970	mV		11		No Use
100.098	111.046	121.994	mV	0001	00	100%	No Use
125.122	136.070	147.019	mV		01		72µs
150.147	161.095	172.043	mV		10		96µs
175.171	186.119	197.067	mV		11		No Use
200.196	211.144	222.092	mV	0010	00	117%	No Use
225.220	236.168	247.116	mV		01		72µs
250.244	261.193	272.141	mV		10		96µs
275.269	286.217	297.165	mV		11		No Use
300.293	311.241	322.190	mV	0011	00	133%	No Use
325.318	336.266	347.214	mV		01		72µs
350.342	361.290	372.239	mV		10		96µs
375.367	386.315	397.263	mV		11		No Use
400.391	411.339	422.287	mV	0100	00	150%	No Use
425.415	436.364	447.312	mV		01		72µs
450.440	461.388	472.336	mV		10		96µs
475.464	486.413	497.361	mV		11		No Use
500.489	511.437	522.385	mV	0101	00	167%	No Use
525.513	536.461	547.410	mV		01		72µs
550.538	561.486	572.434	mV		10		96µs
575.562	586.510	597.458	mV		11		No Use
600.587	611.535	622.483	mV	0110	00	183%	No Use
625.611	636.559	647.507	mV		01		72µs
650.635	661.584	672.532	mV		10		96µs
675.660	686.608	697.556	mV		11		No Use
700.684	711.632	722.581	mV	0111	00	200%	No Use
725.709	736.657	747.605	mV		01		72µs
750.733	761.681	772.630	mV		10		96µs
775.758	786.706	797.654	mV		11		No Use
800.782	811.730	822.678	mV	1000	00	217%	No Use
825.806	836.755	847.703	mV		01		72µs
850.831	861.779	872.727	mV		10		96µs
875.855	886.804	897.752	mV		11		No Use
900.880	911.828	922.776	mV	1001	00	233%	No Use
925.904	936.852	947.801	mV		01		72µs
950.929	961.877	972.825	mV		10		96µs
975.953	986.901	997.849	mV		11		No Use

$V_{DVID\_Width} = \frac{R2}{R1+R2} \times 3.2V$						RSET % 543k R_{TON}	DVID_Width
Min	**Typical**	**Max**	**unit**	**RSET <3:0>**	**DVID_WTH <1:0>**		
1000.978	1011.926	1022.874	mV	1010	00	250%	No Use
1026.002	1036.950	1047.898	mV		01		72µs
1051.026	1061.975	1072.923	mV		10		96µs
1076.051	1086.999	1097.947	mV		11		No Use
1101.075	1112.023	1122.972	mV	1011	00	267%	No Use
1126.100	1137.048	1147.996	mV		01		72µs
1151.124	1162.072	1173.021	mV		10		96µs
1176.149	1187.097	1198.045	mV		11		No Use
1201.173	1212.121	1223.069	mV	1100	00	283%	No Use
1226.197	1237.146	1248.094	mV		01		72µs
1251.222	1262.170	1273.118	mV		10		96µs
1276.246	1287.195	1298.143	mV		11		No Use
1301.271	1312.219	1323.167	mV	1101	00	300%	No Use
1326.295	1337.243	1348.192	mV		01		72µs
1351.320	1362.268	1373.216	mV		10		96µs
1376.344	1387.292	1398.240	mV		11		No Use
1401.369	1412.317	1423.265	mV	1110	00	317%	No Use
1426.393	1437.341	1448.289	mV		01		72µs
1451.417	1462.366	1473.314	mV		10		96µs
1476.442	1487.390	1498.338	mV		11		No Use
1501.466	1512.414	1523.363	mV	1111	00	333%	No Use
1526.491	1537.439	1548.387	mV		01		72µs
1551.515	1562.463	1573.412	mV		10		96µs
1576.540	1587.488	1598.436	mV		11		No Use

Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response, no beat frequency issue in high repetitive load frequency operation and low BOM cost. Hence, ripple based control usually has no good noise immunity. The RT8170A provides a ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 17 shows the ramp compensation.

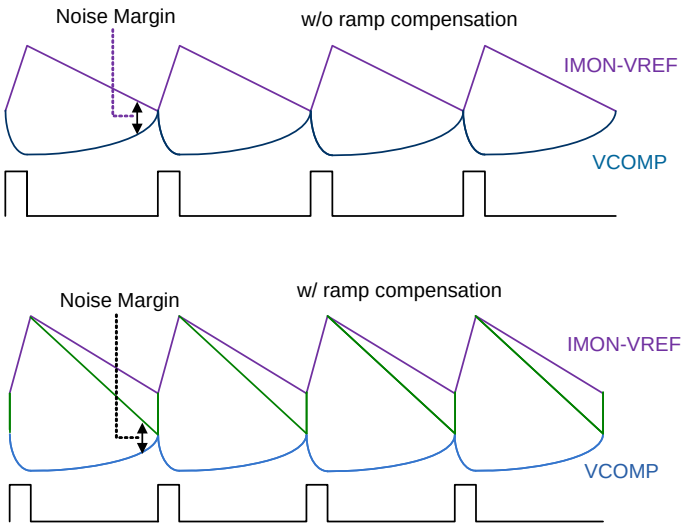


Figure 17. Ramp Compensation

For the RT8170A, the ramp compensation also needs to be considered during mode transition from PS0/1 to PS2. For achieving smooth mode transition into PS2, a proper ramp compensation design is necessary. Since the ramp compensation needs to be proportional to the on-time, in others words, the ramp compensation is dependent on R_{TON} design. The Table 6 shows the relationship between R_{TON} and ramp compensation. For example, when designed R_{TON} is 271kΩ, the RAMP is set as $\frac{543k}{271k} \times 100\%$.

The ramp compensation can be selected for VR12.5 or VR12.6 application at PS0 and PS1 by SET3 pin. For VR12.5 application, the ramp compensation value is 1/3 of VR12.6 application at PS0 and PS1.

Current Monitor, IMON

The RT8170A includes a current monitor (IMON) function which can be used to detect over current protection and the maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

The calculation for IMON – VREF voltage is shown as below :

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times I_{L1}$$

Where I_{L1} is output current and for the definitions of DCR, R_{CS} and R_{EQ}, refer to Figure 7.

Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by the SET2 pin. ICCMAX register is set by an external voltage divider by the multi-function mechanism. The Table 7 shows the ICCMAX setting in the SET2 pin. For example, I_{CCMAX} = 32A, the V_{ICCMAX} needs to be set as 0.203 typically. Additionally, $V_{IMON} - V_{REF}$ needs to be set as 1.6V when I_{L1} = 32A. The ICCMAX alert signal will be pulled to low level if $V_{IMON} - V_{REF}$ = 1.6V.

Table 7. SET2 Pin Setting for ICCMAX

$V_{ICCMAX} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
0.000	3.128	6.256	mV	0	A
12.512	15.640	18.768	mV	2	A
25.024	28.152	31.281	mV	4	A
37.537	40.665	43.793	mV	6	A
50.049	53.177	56.305	mV	8	A
62.561	65.689	68.817	mV	10	A
75.073	78.201	81.329	mV	12	A
87.586	90.714	93.842	mV	14	A
100.098	103.226	106.354	mV	16	A
112.610	115.738	118.866	mV	18	A
125.122	128.250	131.378	mV	20	A
137.634	140.762	143.891	mV	22	A
150.147	153.275	156.403	mV	24	A
162.659	165.787	168.915	mV	26	A
175.171	178.299	181.427	mV	28	A
187.683	190.811	193.939	mV	30	A
200.196	203.324	206.452	mV	32	A
212.708	215.836	218.964	mV	34	A
225.220	228.348	231.476	mV	36	A
237.732	240.860	243.988	mV	38	A
250.244	253.372	256.500	mV	40	A
262.757	265.885	269.013	mV	42	A
275.269	278.397	281.525	mV	44	A
287.781	290.909	294.037	mV	46	A
300.293	303.421	306.549	mV	48	A
312.805	315.934	319.062	mV	50	A
325.318	328.446	331.574	mV	52	A
337.830	340.958	344.086	mV	54	A
350.342	353.470	356.598	mV	56	A
362.854	365.982	369.110	mV	58	A
375.367	378.495	381.623	mV	60	A
387.879	391.007	394.135	mV	62	A
400.391	403.519	406.647	mV	64	A
412.903	416.031	419.159	mV	66	A
425.415	428.543	431.672	mV	68	A
437.928	441.056	444.184	mV	70	A
450.440	453.568	456.696	mV	72	A
462.952	466.080	469.208	mV	74	A
475.464	478.592	481.720	mV	76	A
487.977	491.105	494.233	mV	78	A
500.489	503.617	506.745	mV	80	A

$V_{ICCMAX} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
513.001	516.129	519.257	mV	82	A
525.513	528.641	531.769	mV	84	A
538.025	541.153	544.282	mV	86	A
550.538	553.666	556.794	mV	88	A
563.050	566.178	569.306	mV	90	A
575.562	578.690	581.818	mV	92	A
588.074	591.202	594.330	mV	94	A
600.587	603.715	606.843	mV	96	A
613.099	616.227	619.355	mV	98	A
625.611	628.739	631.867	mV	100	A
638.123	641.251	644.379	mV	102	A
650.635	653.763	656.891	mV	104	A
663.148	666.276	669.404	mV	106	A
675.660	678.788	681.916	mV	108	A
688.172	691.300	694.428	mV	110	A
700.684	703.812	706.940	mV	112	A
713.196	716.325	719.453	mV	114	A
725.709	728.837	731.965	mV	116	A
738.221	741.349	744.477	mV	118	A
750.733	753.861	756.989	mV	120	A
763.245	766.373	769.501	mV	122	A
775.758	778.886	782.014	mV	124	A
788.270	791.398	794.526	mV	126	A
800.782	803.910	807.038	mV	128	A
813.294	816.422	819.550	mV	130	A
825.806	828.935	832.063	mV	132	A
838.319	841.447	844.575	mV	134	A
850.831	853.959	857.087	mV	136	A
863.343	866.471	869.599	mV	138	A
875.855	878.983	882.111	mV	140	A
888.368	891.496	894.624	mV	142	A
900.880	904.008	907.136	mV	144	A
913.392	916.520	919.648	mV	146	A
925.904	929.032	932.160	mV	148	A
938.416	941.544	944.673	mV	150	A
950.929	954.057	957.185	mV	152	A
963.441	966.569	969.697	mV	154	A
975.953	979.081	982.209	mV	156	A
988.465	991.593	994.721	mV	158	A
1000.978	1004.106	1007.234	mV	160	A
1013.490	1016.618	1019.746	mV	162	A

$V_{ICCMAX} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
1026.002	1029.13	1032.258	mV	164	A
1038.514	1041.642	1044.770	mV	166	A
1051.026	1054.154	1057.283	mV	168	A
1063.539	1066.667	1069.795	mV	170	A
1076.051	1079.179	1082.307	mV	172	A
1088.563	1091.691	1094.819	mV	174	A
1101.075	1104.203	1107.331	mV	176	A
1113.587	1116.716	1119.844	mV	178	A
1126.100	1129.228	1132.356	mV	180	A
1138.612	1141.740	1144.868	mV	182	A
1151.124	1154.252	1157.380	mV	184	A
1163.636	1166.764	1169.892	mV	186	A
1176.149	1179.277	1182.405	mV	188	A
1188.661	1191.789	1194.917	mV	190	A
1201.173	1204.301	1207.429	mV	192	A
1213.685	1216.813	1219.941	mV	194	A
1226.197	1229.326	1232.454	mV	196	A
1238.710	1241.838	1244.966	mV	198	A
1251.222	1254.350	1257.478	mV	200	A
1263.734	1266.862	1269.990	mV	202	A
1276.246	1279.374	1282.502	mV	204	A
1288.759	1291.887	1295.015	mV	206	A
1301.271	1304.399	1307.527	mV	208	A

$V_{ICCMAX} = \frac{R2}{R1+R2} \times 3.2V$				ICCMAX	Unit
Min	Typical	Max	Unit		
1313.783	1316.911	1320.039	mV	210	A
1326.295	1329.423	1332.551	mV	212	A
1338.807	1341.935	1345.064	mV	214	A
1351.320	1354.448	1357.576	mV	216	A
1363.832	1366.960	1370.088	mV	218	A
1376.344	1379.472	1382.600	mV	220	A
1388.856	1391.984	1395.112	mV	222	A
1401.369	1404.497	1407.625	mV	224	A
1413.881	1417.009	1420.137	mV	226	A
1426.393	1429.521	1432.649	mV	228	A
1438.905	1442.033	1445.161	mV	230	A
1451.417	1454.545	1457.674	mV	232	A
1463.930	1467.058	1470.186	mV	234	A
1476.442	1479.570	1482.698	mV	236	A
1488.954	1492.082	1495.210	mV	238	A
1501.466	1504.594	1507.722	mV	240	A
1513.978	1517.107	1520.235	mV	242	A
1526.491	1529.619	1532.747	mV	244	A
1539.003	1542.131	1545.259	mV	246	A
1551.515	1554.643	1557.771	mV	248	A
1564.027	1567.155	1570.283	mV	250	A
1576.540	1579.668	1582.796	mV	252	A
1589.052	1592.180	1595.308	mV	254	A

Anti-Overshoot Function

When DVID slew rate increases or the transient load step-down become quite large, loop response is difficult to meet energy transfer so that output voltage generates overshoot to fail specification. The RT8170A has Anti-Overshoot function being able to help improve this issue. The VR will turn off low side MOSFET when output voltage ramps up to the target VID (ALERT signal be pulled low), or when output voltage overshoot is quite large. This function can be enabled/disabled by SET3 pin, and enabled when DVID slew rate is set beyond 26.4mV/µs.

The RT8170A also has Anti-Overshoot enhancement function to improve the transient performance. When this function is enable, the UG signal will be masked when Anti-Overshoot is triggered to reduce the overshoot during the transient load step-down.

Table 8. SET3 Pin Setting for DVID Slew Rate

$V_{DVID\_Slew\ Rate} = \frac{R1}{R1+R2} \times 3.2V$				Anti-Overshoot	Zero Load Line	DVID_Slew Rate
Min	Typical	Max	unit			
25.024	35.973	46.921	mV	Disable	Disable	13.2mV/μs
125.122	136.070	147.019	mV			26.4mV/μs
225.220	236.168	247.116	mV			39.6mV/μs
325.318	336.266	347.214	mV			52.8mV/μs
425.415	436.364	447.312	mV		Enable	13.2mV/μs
525.513	536.461	547.410	mV			26.4mV/μs
625.611	636.559	647.507	mV			39.6mV/μs
725.709	736.657	747.605	mV			52.8mV/μs
825.806	836.755	847.703	mV	Enable	Disable	13.2mV/μs
925.904	936.852	947.801	mV			26.4mV/μs
1026.002	1036.950	1047.898	mV			39.6mV/μs
1126.100	1137.048	1147.996	mV			52.8mV/μs
1226.197	1237.146	1248.094	mV		Enable	13.2mV/μs
1326.295	1337.243	1348.192	mV			26.4mV/μs
1426.393	1437.341	1448.289	mV			39.6mV/μs
1526.491	1537.439	1548.387	mV			52.8mV/μs

Table 9. SET3 Pin Setting for ZCD_Threshold

$V_{ZCD\_Threshold} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$				RSET Application	Anti-Overshoot Enhancement	ZCD_TH
Min	Typical	Max	unit			
0.000	10.948	21.896	mV	VR12.6	Disable	0.75mV
50.049	60.997	71.945	mV			1.5mV
100.098	111.046	121.994	mV			2.25mV
150.147	161.095	172.043	mV			3mV
200.196	211.144	222.092	mV			3.75mV
250.244	261.193	272.141	mV			4.5mV
300.293	311.241	322.190	mV			5.25mV
350.342	361.290	372.239	mV			6mV
400.391	411.339	422.287	mV		Enable	0.75mV
450.440	461.388	472.336	mV			1.5mV
500.489	511.437	522.385	mV			2.25mV
550.538	561.486	572.434	mV			3mV
600.587	611.535	622.483	mV			3.75mV
650.635	661.584	672.532	mV			4.5mV
700.684	711.632	722.581	mV			5.25mV
750.733	761.681	772.630	mV			6mV
800.782	811.730	822.678	mV	VR12.5	Disable	0.75mV
850.831	861.779	872.727	mV			1.5mV
900.880	911.828	922.776	mV			2.25mV
950.929	961.877	972.825	mV			3mV
1000.978	1011.926	1022.874	mV			3.75mV
1051.026	1061.975	1072.923	mV			4.5mV
1101.075	1112.023	1122.972	mV			5.25mV
1151.124	1162.072	1173.021	mV			6mV
1201.173	1212.121	1223.069	mV		Enable	0.75mV
1251.222	1262.170	1273.118	mV			1.5mV
1301.271	1312.219	1323.167	mV			2.25mV
1351.320	1362.268	1373.216	mV			3mV
1401.369	1412.317	1423.265	mV			3.75mV
1451.417	1462.366	1473.314	mV			4.5mV
1501.466	1512.414	1523.363	mV			5.25mV
1551.515	1562.463	1573.412	mV			6mV

Over-Current Protection

RT8170A provides Over-Current Protection (OCP) which is set by SET1 pin. The OCP threshold setting can refer to ICCMAX current in Table 7. For example, if ICCMAX is set as 32A, users can set voltage by using the external voltage divider in the SET1 pin as 0.486V typically if DVID_Threshold = 35mV, then 38.4A OCP (120% x ICCMAX) threshold will be set. When output current is higher than the OCP threshold, OCP is latched with a 40µs delay time to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs. After dynamic VID transition, OCP is masked for 80µs.

Output Over-Voltage Protection

An OVP condition is detected when the VSEN pin is 350mV more than VID. When OVP is detected, the upper gate voltage UGATE is pulled low and the lower gate voltage LGATE is pulled high, OVP is latched with a 0.5µs delay time to prevent false trigger.

Negative Voltage Protection

Since the OVP latch continuously turns on low-side MOSFET of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.05V after triggering OVP, the VR will trigger NVP to turn off low-side MOSFET of the VR while the high-side MOSFET remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on low-side MOSFET. Therefore, the output voltage may bounce between 0V and –0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

Under-Voltage Protection

When the VSEN pin voltage is 350mV less than VID, a UVP will be latched. When UVP latched, both the UGATE and LGATE will be pulled-low. A 3µs delay is used in UVP detection circuit to prevent false trigger. Besides, the UVP function is masked when dynamic VID transient occurs. After dynamic VID transition, UVP is masked for 80µs.

Under-Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold 4.1V (min), the VR will trigger UVLO. The UVLO protection forces high-side MOSFET and low-side MOSFET off by shutting down internal PWM logic drivers.

Power Ready (POR) Detection

During start-up, the RT8170A will detect the voltage at the voltage input pins : V_{CC}, EN and PVCC. When V_{CC} > 4.1V and PVCC > 4V, the RT8170A will recognize the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT8170A will enter start-up sequence. If the voltage at any voltage pin drops below low threshold (POR = low), the RT8170A will enter power down sequence and all functions will be disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin is recommended.1ms (max) after the chip has been enabled, the SVID circuitry will be ready. All protection latches (OVP, OCP, UVP) will be cleared only by VCC. The condition of V_{EN} = low will not clear these latches. Figure 18 and Figure 19 show the POR detection and the timing chart for POR process, respectively.

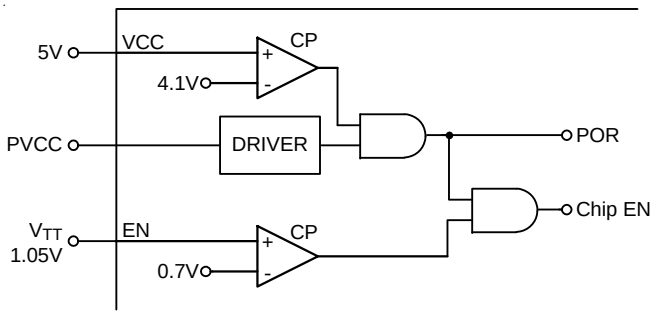


Figure 18. POR Detection

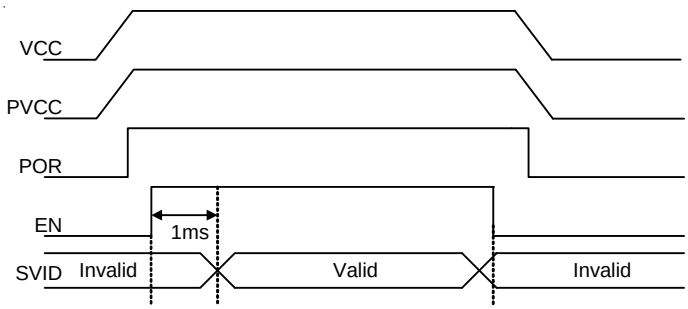


Figure 19. Timing Chart for POR Process

Precise Reference Current Generation, IBIAS

Analog circuits need very precise reference voltage/current to drive/set these analog devices. The RT8170A provides a 2V voltage source at the IBIAS pin, and a 100kΩ resistor is required to be connected between the IBIAS pin and analog ground to generate a very precise reference current. Through this connection, the RT8170A will generate a 20μA current from the IBIAS pin to analog ground, and this 20μA current will be mirrored inside the RT8170A for internal use. The IBIAS pin can only be connected with a 100kΩ resistor to GND for internal analog circuit use. The resistance accuracy of this resistor is recommended to be 1% or higher. Figure 20 shows the IBIAS setting circuit.

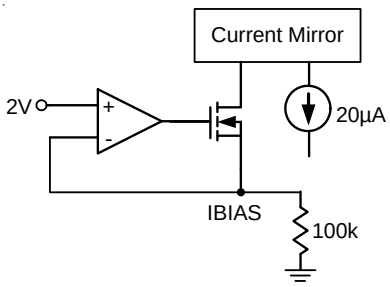


Figure 20. IBIAS Setting Circuit

TSEN and $\overline{\text{VR\_HOT}}$

The $\overline{\text{VR\_HOT}}$ signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in the TSEN pin exceeds 1.887V, the $\overline{\text{VR\_HOT}}$ signal will be pulled low to notify CPU that the thermal protection needs to work. According to Intel VR definition, $\overline{\text{VR\_HOT}}$ signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 21, to design the voltage divider elements (R1, R2 and NTC) so that V_{TSEN} = 1.887V at 100°C. The resistance accuracy of TSEN network is recommended to be 1% or higher.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R1 // R_{NTC(100°C)}\right]} = 1.887V$$

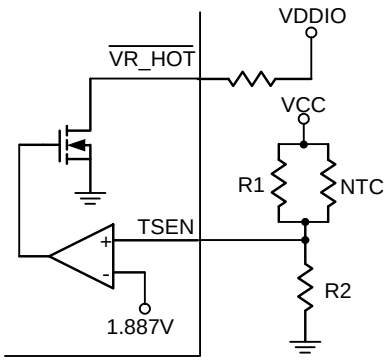


Figure 21. $\overline{\text{VR\_HOT}}$ Circuit

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connecting RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

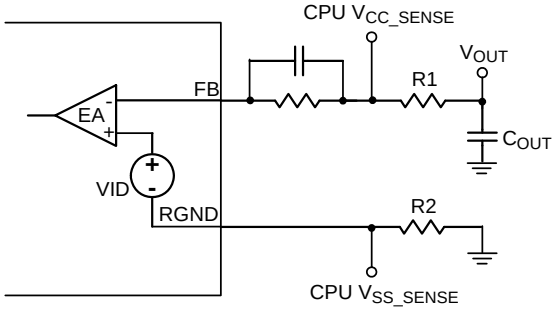


Figure 22. Remote Sensing Circuit

Current Loop Design in Details

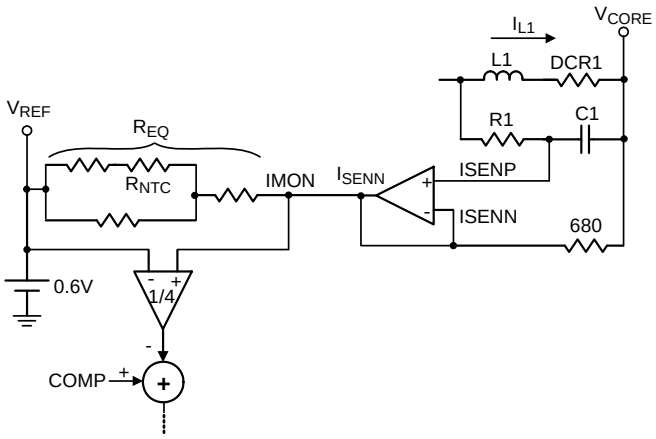


Figure 23. Current Loop Structure

Figure 23 shows the whole current loop structure. The current loop plays an important role in RT8170A that can decide ACLL performance, DCLL accuracy and ICCMAX accuracy. For ACLL performance, the correct compensator design is assumed, if RC network time constant matches inductor time constant L_X / DCR_X, an expected load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_X / DCR_X, V_{CORE} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_X / DCR_X, a worst V_{CORE} waveform will sag to create an undershoot to fail the specification. Figure 24 shows the variety of R_XC_X constant corresponding to the output waveforms.

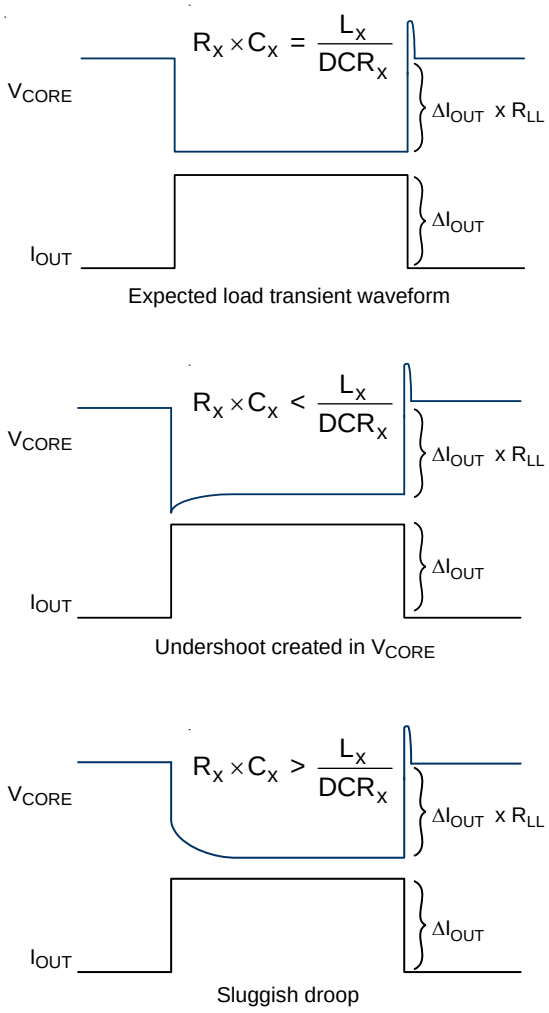


Figure 24. All Kind of R_XC_X Constants

For DCLL performance and ICCMAX accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition then DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between the IMON and REF pins is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as follows :

Step1 : Given the three system temperature T_L, T_R and T_H, at which are compensated.

Step2 : Three equations can be listed as

$$\frac{DCR\,(T_L)}{680} \times \sum_{i=1}^{1} i_{Li} \times R_{EQ}(T_L) = 1.6$$

$$\frac{DCR\,(T_R)}{680} \times \sum_{i=1}^{1} i_{Li} \times R_{EQ}(T_R) = 1.6$$

$$\frac{DCR\,(T_H)}{680} \times \sum_{i=1}^{1} i_{Li} \times R_{EQ}(T_H) = 1.6$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR\,(T) = DCR\,(25°C) \times \left[1 + 0.00393\,(T - 25)\right]$$

(2) $R_{EQ}(T)$ is the equivalent resistor of the resistor network with a NTC thermistor

$$R_{EQ}(T) = R_{IMON1} + \left\{R_{IMON2} \,//\, \left[R_{IMON3} + R_{NTC}(T)\right]\right\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}\,(T) = R_{NTC}\,(25°C) \times e^{\beta\left(\frac{1}{T+273} - \frac{1}{298}\right)}$$

β is in the NTC thermistor datasheet.

Step3 : Three equations and three unknowns, R_{IMON1}, R_{IMON2} and R_{IMON3} can be found out unique solution.

$$R_{IMON1} = K_{TR} - \frac{R_{IMON2} \times (R_{NTCTR} + R_{IMON3})}{R_{IMON2} + R_{NTCTR} + R_{IMON3}}$$

$$R_{IMON2} = \sqrt{\left[K_{R3}^2 + K_{R3}(R_{NTCTL} + R_{NTCTR}) + R_{NTCTL} R_{NTCTR}\right]\alpha_{TL}}$$

$$R_{IMON3} = -R_{IMON2} + K_{R3}$$

Where :

$$\alpha_{TH} = \frac{K_{TH} - K_{TR}}{R_{NTCTH} - R_{NTCTR}}$$

$$\alpha_{TL} = \frac{K_{TL} - K_{TR}}{R_{NTCTL} - R_{NTCTR}}$$

$$K_{R3} = \frac{(\alpha_{TH} / \alpha_{TL})R_{NTCTH} - R_{NTCTL}}{1-(\alpha_{TH} / \alpha_{TL})}$$

$$K_{TL} = \frac{1.6}{G_{CS(TL)} \times I_{CC\text{-}MAX}}$$

$$K_{TR} = \frac{1.6}{G_{CS(TR)} \times I_{CC\text{-}MAX}}$$

$$K_{TH} = \frac{1.6}{G_{CS(TH)} \times I_{CC\text{-}MAX}}$$

Design Step :

The RT8170A Excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures for RT8170A design, first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain the RT8170A design procedure :

	V_{CORE} Specification
Input Voltage	19V
No. of Phases	1
VBoot	1.7V
$V_{DAC(MAX)}$	1.8V
ICCMAX	32A
ICC-DY	27A
ICC-TDC	14A
Load Line	2mΩ
Fast Slew Rate	52.8mV/μs
Max Switching Frequency	600kHz

In Shark Bay VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are as follows :

Output Inductor : 220nH/0.875mΩ

Output Ceramic Capacitor : 22μF/0805 (23pcs max sites on top side)

(1)Initial Settings :

- RT8170A initial voltage is 1.7V
- IBIAS needs to connect a 100kΩ resistor to ground.

(2)Loop Design :

- On time setting : Using the specification, T_{ON} is

  $$t_{ON} = \frac{1}{f_{SW(MAX)}} \times \frac{V_{DAC(MAX)}}{V_{IN}} = 158n(s)$$

  The on time setting resistor R_{TON} = 270kΩ
- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform, R_xC_x time constant needs to match L_X/DCR_X per phase. C_x = 1μF is set, then

  $$R_X = \frac{L_X}{1\mu F \times DCR_X} = 240\Omega$$
- IMON resistor network design : T_L = 25°C, T_R = 50°C and T_H = 100°C are decided, NTC thermistor = 100kΩ @25°C, β = 4485 and ICCMAX = 32A. According to the sub-section "Current Loop Design in Details", R_{IMON1} = 22.56kΩ, R_{IMON2} = 19.2kΩ and R_{IMON3} = 7.31kΩ can be decided. The R_{EQ} (25°C) = 38.85kΩ.
- Load-line design : 2mΩ droop is required, because R_{EQ} (25°C) is decided, the voltage loop Av gain is also decided by the following equation :

  $$R_{LL} = \frac{A_V}{A_I} = \frac{\frac{1}{4} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} \ (m\Omega)$$

Where DCR (25°C) = 0.875mΩ, R_{CS} = 680Ω and R_{EQ} (25°C) = 38.85kΩ. Hence the $A_V = R_2 / R_1$ = 6.25 can be obtained. R_1 = 10kΩ usually is decided, so R_2 = 62.47kΩ.

- SET1 resistor network design : First the DVID compensation parameters need to be decided. The DVID_TH can be calculated as the following equation :

  $$V_{DVID\_TH} = LL \times C_{OUT} \times \frac{DVID}{dt}$$

Where LL is load-line, C_{OUT} is total output capacitance and DVID/dt is DVID fast slew rate. Thus V_{DVID_TH} = 15mV is needed in this case. And DVID_Width is chosen as 72μs typically. Next, OCP threshold is designed as 1.5 x ICCMAX. Last, RAMP = 543kΩ / R_{TON} = 200%, 200% is set. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.737 = \frac{R2}{R1 + R2} \times 3.2V$$

$$1.562 = 80\mu A \times \left(\frac{R1 \times R2}{R1 + R2}\right)$$

R1 = 84.87kΩ, R2 = 25.37kΩ.

- SET2 resistor network design : the QR mechanism parameters need to be designed first. Initial QR_TH is designed as 35mV and QR_Width is designed as 1.34 x T_{ON}. The ICCMAX is designed as 32A. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$0.203 = \frac{R2}{R1 + R2} \times 3.2V$$

$$1.137 = 80\mu A \times \left(\frac{R1 \times R2}{R1 + R2}\right)$$

R1 = 223.6kΩ, R2 = 15.18kΩ.

- SET3 resistor network design : first, the DVID_Slew Rate needs to be selected. Assume 52.8mV/μs is selected. The zero load line and is disabled and enable Anti-Overshoot function and Anti-Overshoot enhancement. The ZCD threshold is chosen as 3.75mV typically and RSET application is set to VR12.6. By using above information, the two equations can be listed by using multi-function pin setting mechanism :

$$1.137 = \frac{R2}{R1 + R2} \times 3.2V$$

$$0.611 = 80\mu A \times \left(\frac{R1 \times R2}{R1 + R2}\right)$$

R1 = 20.15kΩ, R2 = 11.85kΩ

(3) Protection Settings :

- OVP/UVP protections : When the VSEN pin voltage is 350mV higher than VID, the OVP will be latched. When the VSEN pin voltage is 350mV lower than VID, the UVP will be latched.
- TSEN and $\overline{\text{VR\_HOT}}$ design : Using the following equation to calculate related resistances for $\overline{\text{VR\_HOT}}$ setting.

$$V_{TSEN} = V_{CC} \times \frac{R2}{R2 + \left[R_{NTC(100°C)} \,//\, R1\right]} = 1.887V$$

Choosing R1 = 100kΩ and an NTC thermistor R_{NTC} (25°C) = 100kΩ and its β = 4485. When temperature is 100°C, the R_{NTC}(100°C) = 4.85kΩ.Then R2 = 2.8kΩ can be calculated.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.8°C/W) = 3.59W for WQFN-32L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 25 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

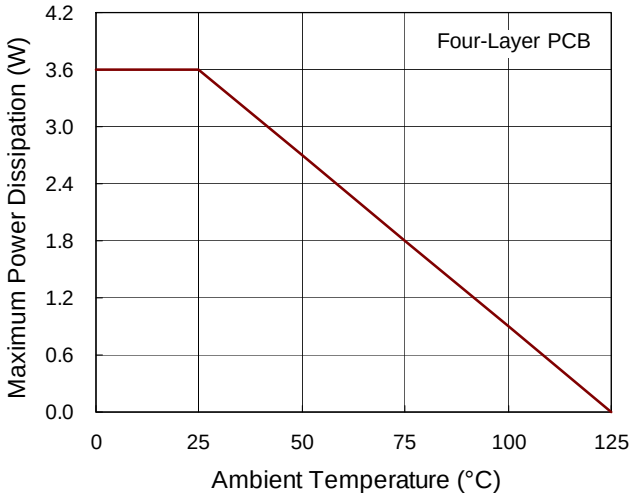


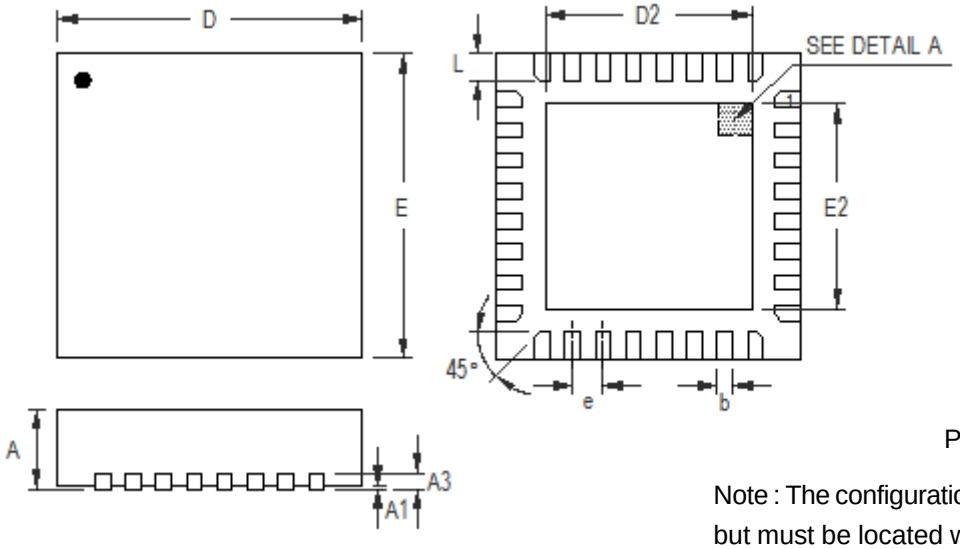
Figure 25. Derating Curve of Maximum Power Dissipation

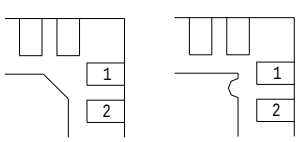
Layout Considerations

PCB layout is critical to achieve low switching losses and stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for the optimum PCB layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to let the inductor charging path be longer than the discharging path.
- Place the current sense component close to the controller. ISENP and ISENN connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high speed switching nodes away from sensitive analog areas (COMP, FB, ISENP, ISENN, etc...)
- Connect the exposed pad to the ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

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