Design Guidelines for RT7302 and RT7304 PSR LED Driver

Abstract

RT7302 and RT7304 are constant current LED drivers with active power factor correction (PFC). They support high power factor across a wide range of line voltages, and drive the converter in the quasi-resonant (QR) mode to achieve higher efficiency. By using primary side regulation (PSR), RT7302/RT7304 control the output current accurately without the need of a shunt regulator or opto-coupler at the secondary side, reducing the external component count, the cost, and the size of the driver board.

This application note presents a step by step design guideline for an isolated single stage constant current LED driver with PFC using the RT7302. The guideline can also be applied to RT7304.

The design example in this application note describes an 18W LED driver with slim form-factor, suitable for T8 LED tube applications, but the same design can also be used in LED bulb or other form factor applications.

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1. Introduction

RT7302 and RT7304 are constant current LED drivers with active power factor correction (PFC). They support high power factor across a wide range of line voltages, and drive the converter in the quasi-resonant (QR) mode to achieve higher efficiency. By using primary side regulation (PSR), RT7302/RT7304 control the output current accurately without a shunt regulator or opto-coupler at the secondary side, reducing the external component count, the cost, and the size of the LED driver board. RT7304 embeds comprehensive protection functions for robust designs, including LED open circuit protection, LED short circuit protection, output diode short circuit protection, VDD under voltage lockout (UVLO), VDD over-voltage protection (VDD OVP), over-temperature protection (OTP), and cycle-by-cycle current limitation. RT7304 is available in a cost effective SOT-23-6 package.

RT7302 has the same basic functionality as RT7304, but integrates more features, including fast startup via high voltage pin, PWM dimming, and input voltage feed-forward compensation. RT7302 is available with SOP-8 package.

This application note presents a step by step design guideline for an isolated single stage constant current LED driver with PFC using the RT7302. The design guideline can also be applied to RT7304.

The design example in this application note is an 18W LED driver with slim form-factor, suitable for T8 LED tube applications.

Figure 1. Picture of the 18W evaluation board with a typical T8 LED assembly
2. RT7302 Basic Operation

Figure 2 shows RT7302 in a typical flyback converter topology with input voltage ($V_{in}$).

![Flyback Application Circuit](image)

Figure 2

When main switch Q1 is turned on with a fixed on-time $t_{on}$, the peak current $I_{L_{pk}}$ of the magnetic inductor $L_m$ can be calculated by the following equation:

$$I_{L_{pk}} = \frac{V_{in}}{L_m} \times t_{on}$$

If the input voltage is the output voltage of the full-bridge rectifier with sinusoidal input voltage $V_{in_{pk}} \sin(\theta)$, the inductor peak current $I_{L_{pk}}$ can be expressed as the following equation:

$$I_{L_{pk}} = \frac{V_{in_{pk}} |\sin(\theta)| \times t_{on}}{L_m}$$

When the converter operates in critical-conduction mode (CRM) with constant on-time control, the envelope of the peak inductor current will follow the input voltage waveform in-phase. Thus, high power factor can be achieved. The minimum on time is set by the upper divider resistor of the ZCD network $R_{ZCD1}$.

Quasi resonant switching is achieved by sensing the auxiliary winding zero current condition and a smart internal valley detection circuit. Switch-on of the MOSFET will always happen at a valley of the resonant voltage, thereby reducing switching losses and EMI. The ZCD pin is also used to sense output OVP condition, set by $R_{ZCD2}$. 
The primary peak current is sensed by measuring the voltage across the MOSFET source resistor via the CS pin. An internal leading edge blanking circuit removes any spikes from this signal. A current variation due to a propagation delay is compensated by the CS pin internal current source and the external series resistor \( R_{PC} \).

The MULT pin is used for sensing the input peak voltage, and controls the ramp for T-on generation. The line voltage sense is used as feed-forward to adjust the ramp for constant COMP voltage over line voltage. This improves the regulation, eases compensation and achieves accurate maximum power limit over the full mains range. This is especially important for full range LED driver designs.

RT7302 HV pin will quickly charge the capacitor connected to the VDD pin during start-up. After start-up, the HV pin is disconnected, and the VDD is supplied by the auxiliary winding. This method ensures fast start-up without extra power dissipation in the bleeder resistor during normal operation.

**Design Procedure:**

The basic design sequence is as following:

Define Input and output conditions → Calculate input power → Transformer design, Calculate N ratio, Primary inductance, Primary and secondary winding turns → Current sense resistor \( (R_{CS}) \), bridge rectifier, MOSFET parameters, Output diode parameters → Minimum ton setting \( (R_{ZCD1}) \) → OVP setting \( (R_{ZCDS}) \) → Propagation delay setting \( (R_{PC}) \) → Feed-forward compensation \( (R_M, R_{M2}) \)

The RT7302 design tool can be used to quickly determine the component values. Chapter 3 contains a detailed step by step design description for the 18W reference design.
3. Design of an 18W LED Driver for T8 Applications

The LED driver example for this section is the 18W T8 LED driver evaluation board, see Figure 3.

Figure 3. The board measures 230x18x10mm and will fit in most narrow tube T8 housing behind the LED board.

Requirement specification for this design:

- Input range: 90V ~ 264V\text{ac}
- LED load: 45V / 400mA
- Efficiency >85% at 120V / 230V\text{ac}
- PF: > 0.95 and THDi < 15% (meet IEC61000-3-2 class C & D)

Step 1. Input and Output Conditions

The input and output conditions are listed as follows:

- maximum AC input voltage $V_{\text{ac, max}}$, 264V\text{ac}
- minimum AC input voltage $V_{\text{ac, min}}$, 90V\text{ac}
- line frequency $f_{\text{line}}$, 50Hz / 60Hz
- average output current $I_o$, 400mA
- minimum average output voltage $V_{o, \text{min}}$, 43V
- maximum average output voltage $V_{o, \text{max}}$, 47V

LED string is using 14 high power LEDs with total dynamic resistance of 14Ω

Estimated maximum average input power $P_{\text{in, max, est}}$ can be expressed as:

$$P_{\text{in, max, est}} = \frac{V_{o, \text{max}} \times I_o}{\eta}$$

where $\eta$ is the estimated efficiency.

The efficiency is estimated at 85%, the input power will become: $47 \times 0.4 / 0.85 = 22.12$W.

Estimated peak current transfer ratio of the transformer (CTR\text{TX1}) can be expressed as

$$\text{CTR}_{\text{TX1}} = \frac{l_{\text{SEC, PK}}}{l_{\text{PRI, PK}}} \times \frac{N_s}{N_p}$$
where \( I_{\text{SEC, pk}} \) is the peak current of secondary side, \( I_{\text{PRI, pk}} \) is the peak current of the primary side, \( N_S \) is the turn’s number of the secondary winding, and \( N_P \) is the turn’s number of the primary winding. CTR_{TX1} can be estimated to be 0.9.

The reflected output voltage \( V_{ro} \) can be express as

\[
v_{ro} = N_P \cdot \left( V_{o, \text{max}} + V_f \right)
\]

where \( V_f \) is the forward voltage of output diode. \( V_{ro} \) is recommended to be within 95 ~125V.

In the example: Set \( V_{ro} = 125V \).

Min. VDD supply voltage at max. output voltage \( V_{DD, Vomax, min} \) can be derived as

\[
V_{DD, Vomax, min} = V_{o, \text{max}} \cdot V_{TH, OFF, max} \cdot 130%
\]

where \( V_{TH, OFF} \) is the falling under voltage lockout (UVLO) threshold voltage of the controller.

VDD supply voltage at max. output voltage \( V_{DD, max} \) must be within \( V_{DD, Vomax, min} \sim V_{DD, OVP, min} \).

In the example:

\( V_{o, \text{max}} = 47V, V_{o, \text{min}} = 43V, V_{TH, OFF, max} = 10V, V_{DD, Vomax, min} = 14.2V \)

Set \( V_{DD, max} = 20V \).

Output Capacitor \( C_{OUT} \) Calculation:

The output capacitor value will determine the amount of voltage ripple on the LED string. This voltage ripple, together with the dynamic resistance of the LED string will determine the current ripple through the LED string and this will cause 100Hz or 120Hz light flicker.

In this example the maximum allowed LED current ripple amplitude is set at 340mA for a ripple percentage of 42%. The LED string uses 14 LEDs and has total dynamic resistance of 14Ω: \( V_{OUT} \) ripple = 0.34A*14 Ω = 4.76Vpp. The transformer secondary winding current can estimated having a low frequency ripple of double the line frequency and low frequency peak to peak amplitude of double the average output current. The output capacitor value can now be calculated:

\[
C_{OUT} = \frac{I_{OUT, PP}}{V_{OUT, PP} \cdot 2 \cdot \pi \cdot f}
\]
where $I_{OUT\_PP}$ is 2x the average LED current, and $V_{OUT\_PP}$ is the allowed AC output voltage ripple and $f$ is double line frequency. Calculating for 50Hz line frequency: $C_{OUT} = 2^{*}0.4/(4.76^{*}2^{*}\pi^{*}100) = 267\mu F$. For less LED current ripple, the $C_{OUT}$ value needs to be increased. But when LED strings with higher dynamic resistance are used, the $C_{OUT}$ value can be reduced.

**Step 2. Transformer Design**

Ideal turn’s ratio of primary to secondary windings can be expressed as

$$\frac{N_p}{N_s} = \frac{V_o}{V_{o\_max} + V_f}$$

In the example:

$V_o = 125V$, $V_{o\_max} = 47V$, $V_f = 0.7V$, $N_p/N_s = 2.62$

Ideal turn’s ratio of secondary to auxiliary windings can be expressed as

$$\frac{N_s}{N_A} = \frac{V_{o\_max}}{V_{DD\_max}}$$

In the example:

$V_{o\_max} = 47V$, $V_{DD\_max} = 20V$, $N_s/N_A = 2.35$

The maximum on time of the MOSFET $t_{on\_max}$ can be expressed

$$t_{on\_max} = D_{on\_max} \cdot \frac{1}{f_{s\_min}}$$

in which $f_{s\_min}$ is the minimum switching frequency.

The duty ratio of the MOSFET $D_{on}$ can be expressed

$$D_{on\_max} = \frac{V_o}{V_o + V_{ac\_min\_pk}}$$

The primary-side inductance $L_m$ can be derived as

$$L_m = \frac{t_{on}}{2f_{o}} \cdot \frac{N_p}{N_s} \cdot CTR_{TX1} \cdot \frac{1}{2f_{line}} \cdot \int_{0}^{1} \frac{V_{ac}(t)^2}{V_o + V_{ac}(t)} \cdot dt$$

Thus, $L_m$ can be obtained after the minimum switching frequency $f_{s\_min}$ is determined.
In the example:
Set $f_{s_{\text{min}}} = 54\text{kHz}$, $V_{ro} = 125\text{V}$, $V_{ac_{\text{min pk}}} = 127\text{V}$,
Obtain $t_{on_{\text{max}}} = 8.68\mu\text{s}$ and $L_m = 899\mu\text{H}$
The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_{P_{\text{min}}} > \frac{I_{P_{\text{pk}}} \cdot L_m}{B_{\text{max}} \cdot A_e}$$

where $A_e$ is the cross-sectional area of the core in $m^2$, and $B_{\text{max}}$ is the maximum flux density in Gauss.

In the example:
$I_{P_{\text{pk}}} = 1.23\text{A}$, $L_m = 899\mu\text{H}$, EDR-28 core is chosen and its $A_e = 88m^2$.
Set $B_{\text{max}} = 2950\text{ Gauss}$. Obtain $N_{P_{\text{min}}} > 42.5$ turns.
Now all the parameters of transformer are determined, including $N_{P_{\text{min}}}$, $N_P/N_S$, $N_S/N_A$ and $L_m$.
$N_P = 43T$, $N_S = 43/2.62 = 16.4T$, choose $16T$, $N_A = 16/2.35 = 6.8T$, choose $7T$.

**Step 3. Current Sense Resistor Determination**

Current sense resistor $R_{CS}$ can be determined as the following equation:

$$R_{CS} = \frac{1}{2} \times N_P \times \frac{K_{CC}}{I_{O}} \times CTR_{TX1}$$

where $K_{CC}$ is a reference in the controller.

In the example:
Actual $N_P/N_S = 2.69$, $K_{CC} = 0.25$, $I_{O} = 0.4A$, $CTR_{TX1} = 0.9$, 
The current sense resistor $R_{CS}$ will become $(1/2)*2.69*(0.25/0.4)*0.9 = 0.79 \Omega$.

**Step 4. Bridge Rectifier Determination**

The maximum reverse voltage of the bridge rectifier $V_{RRM_{\text{max}}}$ can be expressed as:

$$V_{RRM_{\text{max}}} = \sqrt{2} \cdot V_{ac_{\text{max}}}$$

The maximum forward current of the bridge rectifier $I_{BR_{\text{max}}}$ can be expressed as:
\[ I_{BR\_max} = \frac{P_{in\_max}}{V_{ac\_min}} \]

In the example:

\[ V_{RRM\_max} = \sqrt{2} \cdot 264 = 373V \]

\[ I_{BR\_max} = 22.12/90 = 0.25A \]

A 600V / 1A diode bridge will provide sufficient de-rating, including inrush current and voltage surge.

**Step 5. MOSFET Determination**

The maximum drain-to-source voltage stress of the MOSFET \( V_{DS\_max} \) is given as:

\[ V_{DS\_max} = V_{RRM\_max} + V_{clamp} \]

in which \( V_{clamp} \) is the maximum voltage on the snubber and it must be higher than \( V_{op} \).

The maximum drain-to-source current stress of the MOSFET \( I_{DS\_max} \) is given as:

\[ I_{DS\_max} = \sqrt{2} \cdot V_{ac\_min} \cdot \frac{\text{ton}\_max}{L_m} \]

In the example:

Set \( V_{clamp} = 160V \)

\[ V_{DS\_max} = 373 + 160 = 533V : \text{for sufficient de-rating, choose at least 650V rated MOSFET.} \]

\[ I_{DS\_max} = I_{P\_pk} = 1.23A : \text{MOSFET R}_{\text{ds(on)}} \text{ selection depends on thermal aspects. In this small T8 design, a 4A MOSFET with } R_{\text{ds(on)}} \text{ of 1.8Ω was selected, which can be used without heat-sink.} \]

**Step 6. Output Diode and Auxiliary Diode Determination**

The maximum reverse voltage stress of the output diode \( V_{Do\_max} \) can be expressed as:

\[ V_{Do\_max} = V_{RRM\_max} \frac{N_S}{N_P} + V_{O\_OVP} \]

where \( V_{O\_OVP} \) is the output over voltage level.

The maximum average forward current stress of the output diode \( I_{Do\_max} \) can be expressed as:
\[ I_{D_{\text{max}}} = I_0 \]

In the example:

Set \( V_{O\_\text{OVP}} = 61V \)

\[ V_{D_{\text{max}}} = \frac{373}{2.62} + 61 = 203V \]

\[ I_{D_{\text{max}}} = I_0 = 0.4A \]

Diodes with higher current rating can be chosen for higher efficiency.

The maximum reverse voltage stress of the auxiliary diode \( V_{D_{a_{\text{max}}}} \) can be expressed as:

\[ V_{D_{a_{\text{max}}}} = V_{RRM_{\text{max}}} \cdot \frac{N_A}{N_P} + V_{D_{D\_OVP}} \]

where \( V_{D_{D\_OVP}} \) is the VDD over voltage level.

The maximum average forward current stress of the output diode \( I_{D_{a_{\text{max}}}} \) can be expressed as:

\[ I_{D_{a_{\text{max}}}} = I_{D_{D_{\text{max}}}} \]

in which \( I_{D_{D_{\text{max}}}} \) is the maximum supply current for the controller.

In the example:

\[ V_{D_{D\_OVP}} = 27V \]

\[ V_{D_{a_{\text{max}}}} = \frac{373}{(2.62 \cdot 2.35)} + 27 = 87.8V \]

\[ I_{D_{a_{\text{max}}}} = I_{D_{D_{\text{max}}}} = 5mA \]

**Step 7. Minimum On-Time Setting**

\( RT7302 \) limits a minimum on-time \( t_{on\_\text{min}} \) for each switching cycle. The \( t_{on\_\text{min}} \) is a function of the sample-and-hold ZCD current \( I_{ZCD\_SH} \) as following:

\[ t_{on\_\text{min}} \cdot I_{ZCD\_SH} = 405 \text{ p\cdot sec\cdot A (typ.)} \]

\( I_{ZCD\_SH} \) can be expressed as:

\[ I_{ZCD\_SH} = \frac{V_{N\_P}}{R_{ZCD1} \cdot N_P} \]

Thus, \( R_{ZCD1} \) can be determined by:
In addition, the current flowing out of ZCD pin must be lower than 2.5mA (typ.). Thus, the \( R_{ZCD1} \) is also determined by:

\[
R_{ZCD1} > \sqrt{2} \cdot \frac{V_{ac \_max}}{2.5\_m} \cdot \frac{N_A}{N_P}
\]

In the example:

\[
R_{ZCD1} > \sqrt{2} \cdot \frac{264}{2.5\_m} \cdot \frac{N_A}{N_P} = 24.2k\Omega
\]

Set \( R_{ZCD1} = 60k\Omega \)

When \( V_{in} = 10V \), \( t_{on \_min} = 405p \cdot 60k \cdot (2.62 \cdot 2.35) / 10 = 14.9\mu s \)

In general, longer \( t_{on \_min} \) can slightly improve THDi. However, if \( t_{on \_min} \) is too long, it will induce a current resonance at \( V_{in} \) zero crossing, worsening THDi. Thus, \( t_{on \_min} \) can be properly defined according to the measured THDi.

**Step 8. Output Over-Voltage Protection Setting**

Output OVP is achieved by sensing the knee voltage on the auxiliary winging. Thus, \( R_{ZCD1} \) and \( R_{ZCD2} \) can be determined by the equation as:

\[
V_{O \_OVP} = \frac{N_A}{N_S} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 3.1V \text{ (typ.)}
\]

In the example:

Set \( V_{O \_OVP} = 61V \)

It can be calculated that \( R_{ZCD2} = 7.9k\Omega \)

**Step 9. Propagation Delay Compensation Design**

The \( V_{CS} \) deviation (\( \Delta V_{CS} \)) caused by propagation delay effect can be derived as:

\[
\Delta V_{CS} = \frac{V_{in} \cdot t_d \cdot R_{CS}}{L_m}
\]

in which \( t_d \) is the delay period which includes the propagation delay of \( RT7302 \) and the turn-off transition of the main MOSFET.

The sourcing current from CS pin of \( RT7302 \) \( I_{CS} \) can be expressed as:
\[ I_{CS} = K_{PC} \cdot V_{in} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{ZCD1}} \]

where \( K_{PC} \) is a constant value in the controller. \( R_{PC} \) can be designed by:

\[
R_{PC} = \frac{\Delta V_{CS}}{I_{CS}}
= \frac{t_d \cdot R_{CS} \cdot R_{ZCD1} \cdot N_P}{L_m \cdot K_{PC} \cdot N_A}
\]

\( t_d \) is estimated to be around 150ns

In the example:
\[
R_{PC} = 150n^*0.74^*60k/(899\mu^*0.02)^*(2.62^*2.35) = 2.3k\Omega
\]

The delay period \( t_d \) is varied with the parasitic capacitance of MOSFET, the gate driving capability, and the propagation delay of the controller. Thus, \( t_d \) cannot be estimated accurately, and \( R_{PC} \) may need to be modified according to the measured output current. If the output current increases when \( V_{in} \) rises, \( R_{PC} \) should be increased. If the output current decreases with \( V_{in} \) rises, \( R_{PC} \) should be decreased.

### Step 10. Feed-Forward Compensation Design (Only for RT7302)

The COMP voltage, \( V_{COMP} \), can be derived from the following equations.

\[
\frac{1}{2} \left( V_{MULT_{pk}} \right)^2 \times \frac{t_{on} + t_{off}}{t_s} \times Gm_{ramp} \times t_{on} = C_{ramp} \times V_{COMP}
\]

\[
V_{MULT_{pk}} = V_{in_{pk}} \times \frac{R_{M2}}{R_{M1} + R_{M2}}
\]

\( V_{MULT_{pk}} \) is the peak voltage on the MULT pin. \( Gm_{ramp} \) is the trans-conductance of the ramp generator, and its typical value is 2.5μA/V. \( C_{ramp} \) is the capacitance of the ramp generator, and its typical value is 6.5pF. When the converter operates at CRM, \( (t_{on} + t_{off}) / t_s = 1 \). \( V_{COMP_{min}} \) is recommended be within 1.2 ~ 1.5V, and \( R_{M2} \) is recommended to be within 30 ~ 60kΩ. Thus, the voltage divider resistors \( R_{M1} \) and \( R_{M2} \) can be determined according to the above parameters.
In the example:
\[ t_{on,max} = 8.68\mu s. \]
Set \[ V_{COMP,min} = 1.2V, \]
Obtain \[ V_{MULT,pk} = 0.85V. \]
Set \[ R_{M2} = 43k\Omega, \]
It can be calculated that \[ R_{M1} = 6.4M\Omega. \]

4. Design Tool Explanation

The RT7302 design tool and RT7304 design tool can be used as quick way to determine the component values. The content is similar to the step by step design as described in Chapter 3. In the design tool, users input operation parameters into "Yellow Grid". According to the key-in parameter, the design tool will automatically generate the results in Pink Grid".

Table 1 below shows the entered data and calculation results for the 18W T8 reference design.
### Table 1. Design tool data

#### Step 1: Input and output conditions definition
- Min. AC input voltage $V_{in,min}$: 90 Vrms
- Max. AC input voltage $V_{in,max}$: 204 Vrms
- Line frequency $f_{line}$: 50 Hz
- Average output current $I_{o}$: 6.4 A
- Min. average output voltage $V_{o,min}$: 43.8 V
- Max. average output voltage $V_{o,max}$: 47.4 V
- Max. average output power $P_{o,max}$: 143 W
- Estimated efficiency $\eta$: 85 %
- Estimated peak current transfer ratio (CTR) of the transformer $(TK)$ $P_{max}$/$(f_{line})/P_{in}$: 90 %
- Estimated half of the resonant period of the primary-side inductance $L_{p}$ and parasitic capacitance of MOSFET $Q_{o}$: 1.06 μs
- Estimated deviation of the detected inductance discharge time $T_{d}$: 0.29 μs
- Estimated mean, average input power $P_{in,mean}$: 22.36 W
- Forward voltage of output diode $V_{f}$: 8.7 V
- Max. voltage of $V_{DSS}/V_{DSS}': 130 V
- Min. VDD supply voltage at $V_{in}=V_{DSS}/V_{DSS}': 14.3 V
- VDD supply voltage at $V_{in}=V_{DSS}/V_{DSS}': 20 V

#### Step 2: Transformer (TX) design
1. Turns ratio determination
   - Ideal turns ratio of primary to secondary winding $N_{P}/N_{S}$: 7.62
   - Ideal turns ratio of primary to auxiliary winding $N_{P}/N_{A}$: 2.36
2. Inductance design
   - The lowest switching frequency $f_{SW,min}$: 14.6 kHz
   - Duty ratio of the peak of the min. AC input voltage $D_{in,min}$: 1.47
   - Factor(f) at the min. AC input voltage $F(f)_{min}$: 33.13
   - Primary-side Inductance $L_{p}$: 334.5 μH
3. Current Stress Calculation (Min. AC input voltage and full load)
   - Max. peak current of the primary winding $I_{p,max}$: 1.29 A
   - RMS current of the primary winding $I_{p}$: 0.56 A
   - Max. peak current of the secondary winding $I_{s,max}$: 2.50 A
   - RMS current of the secondary winding $I_{s}$: 1.312 A
4. Structure design
   - Max. magnetic flux density $B_{max}$: 2050 Gauss
   - Cross sectional area of core $A_{c}$: 50 mm²
   - Min. turns number of the primary winding $N_{P}$: 42.5
   - Turns number of the primary winding $N_{P}$: 47
   - Turns number of the auxiliary winding $N_{A}$: 16
   - Actual $N_{P}/N_{A}$: 2.95
   - Actual $N_{P}/N_{S}$: 3.26

#### Step 3: Current Sense Resistor ($R_{sense}$) Determination
- Ideal current sense resistor $R_{sense}$: 0.71 Ω
- Selected current sense resistor $R_{sense}$: 0.71 Ω
- Actual average output current $I_{avg}$: 6.42 A
- Max. CS peak voltage $V_{CS,peak}$: 0.36 V
- Ratio of the $V_{CS,peak}$ to $V_{in,peak}$ $V_{CS,peak}/V_{in,peak}$: 1.04

#### Step 4: Bridge Rectifier (BD) Determination
- Max. reverse voltage of the bridge rectifier $V_{BR,peak}$: 372 V
- Min. forward current of the bridge rectifier $I_{BR,peak}$: 0.25 A

#### Step 5: MOSFET ($Q_o$) Determination
- Max. voltage on the snubber $V_{snubber}$: 100.98 V
- Max. $D$-to-$S$ voltage stress of the MOSFET $V_{DS}$: 132.8 V
- Max. $D$-to-$S$ current stress of the MOSFET $I_{DS}$: 1.328 A

#### Step 6: Output diode ($D_{out2}$) and Auxiliary Diode ($D_{aux}$) Determination
- Min. reverse voltage stress of the output diode $V_{DSS}$: 206.7 V
- Max. average forward current stress of the output diode $I_{DSS}$: 6.96 A
- Max. reverse voltage stress of the auxiliary diode $V_{Daux}$: 7.4 V
- Max. average forward current stress of the auxiliary diode $I_{Daux}$: 5.09 A

#### Step 7: Min. on time Design
- High-side resistor of the ZCD resistor-divider $R_{ZCD}$: 24.35 kΩ
- $R_{F}$: 60.9 kΩ
- Min. on time $t_{on}$: 14.3 μs

#### Step 8: OVP Setting
- Ratio of the output OV to max. output voltage $V_{OV,peak}/V_{DSS}$: 1.38
- Output over-voltage threshold $V_{ov}$: 44.1 V
- Low-side resistor of the ZCD resistor-divider $R_{ZCD}$: 7.37 kΩ

#### Step 9: Propagation Delay Compensation Design
- IC propagation delay: MOSFET turn-off transition $t_{OFF}$: 150 ns
- Propagation delay compensation resistor $R_{comp}$: 3.2 Ω

#### Step 10: Feed-Forward Compensation Design
- Recommended Min. COMP voltage $V_{comp,min}$: 1.35 V
- Recommended Min. MULT voltage $V_{mult,min}$: 5.65 V
- Low-side resistor of the MULT resistor-divider $R_{comp}$: 43 kΩ
- High-side resistor of the MULT resistor-divider $R_{comp}$: 54 kΩ

#### Step 11: Recommended Component Value
- High-voltage start-up resistor $R_{start}$: 10 - 72 kΩ
- External GATE-to-GND resistor $R_{G}$: 10 - 72 kΩ
- Gate resistor between GATE pin and MOSFET Q1 pin $R_{G}$: 10 - 150 kΩ
- Resistor in series with the diode $R_{d}$: 19 - 150 kΩ
- Parallel resistor of the MOSFET snubber $R_{comp}$: 100 - 290 kΩ
- Series resistor of the MOSFET snubber $R_{comp}$: 100 - 290 kΩ
- VDD decoupling capacitor $C_{DC}$: 10 - 22 μF
- Compensation capacitor between the COMP and GND pins $C_{comp}$: 1 - 4.7 μF
- Filter capacitor between the MULT and GND pins $C_{mult}$: 10 - 150 μF
- Filter capacitor between the ZCD and GND pins $C_{ZCD}$: 10 - 150 μF
- Capacitor of the MOSFET snubber $C_{comp}$: 1 - 2.2 μF
5. Circuit Diagram of the Evaluation Board

The circuit diagram of the evaluation board is shown in Figure 4 below.

![Circuit Diagram of the Evaluation Board](image)

Figure 4. Schematic of the 18W T8 LED driver reference design

RV1 is added for line surge protection. LX2, CX1 and LX1 are added to reduce Line conducted EMI. L1 and LX3 are added to reduce radiated EMI.

The full BOM is shown in table 2 below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
<th>Reference</th>
<th>Part/Value</th>
<th>Type</th>
<th>Vendor</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>F1</td>
<td>T1.25A/300V</td>
<td>SS-5F-2P</td>
<td>Littlefuse</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>RV1</td>
<td>7N471K</td>
<td>TVS-2P</td>
<td>Thinking</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>LX2</td>
<td>30mH</td>
<td>LRS-T14</td>
<td>Abliss</td>
<td>T12.7<em>7.92</em>4.9(μi=10000)</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>CX1</td>
<td>0.1μF</td>
<td>CFS-12X12</td>
<td>Shiny Space</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>LX1</td>
<td>5mH</td>
<td>LDS-D9X12</td>
<td>Mag. layers</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>BD1</td>
<td>1A/600V</td>
<td>DB-1A</td>
<td>GW</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>C4</td>
<td>0.1μF/500V</td>
<td>CFS-11X10</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>R6, R7, R9</td>
<td>2.2MΩ</td>
<td>0805</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>R19</td>
<td>43kΩ</td>
<td>0603</td>
<td>RALEC</td>
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<tr>
<td>10</td>
<td>1</td>
<td>C6</td>
<td>22nF/50V</td>
<td>0603</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>C7</td>
<td>2.2μF/25V</td>
<td>0805</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>R22</td>
<td>0Ω</td>
<td>0603</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>-----</td>
<td>----</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>R8</td>
<td>10kΩ</td>
<td>1206</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>R2</td>
<td>140kΩ</td>
<td>1206</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>D2</td>
<td>FM4007</td>
<td>SOD123</td>
<td>Willas</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>1</td>
<td>C2</td>
<td>2.2nF/1kV</td>
<td>1206</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>R13</td>
<td>200Ω</td>
<td>0805</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>D4</td>
<td>1N4148</td>
<td>SOD-123</td>
<td>Willas</td>
<td></td>
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<tr>
<td>19</td>
<td>1</td>
<td>Q1</td>
<td>4A/650V</td>
<td>TO-220</td>
<td>IPS</td>
<td>FTA04N65D</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>C9</td>
<td>100pF/1kV</td>
<td>1206</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>LX3</td>
<td>T3.5<em>3</em>1.4</td>
<td>---</td>
<td>King core</td>
<td>On Source pin of Q1</td>
</tr>
<tr>
<td>22</td>
<td>3</td>
<td>R15, R16, R17</td>
<td>2.21Ω</td>
<td>1206</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>R14</td>
<td>2kΩ</td>
<td>603</td>
<td>RALEC</td>
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</tr>
<tr>
<td>24</td>
<td>1</td>
<td>C10</td>
<td>470pF/1kV</td>
<td>1206</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>1</td>
<td>CY1</td>
<td>1000pF/250Vac</td>
<td>CAP-10mm</td>
<td>Murata</td>
<td></td>
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<tr>
<td>26</td>
<td>1</td>
<td>R10</td>
<td>60kΩ</td>
<td>0603</td>
<td>RALEC</td>
<td></td>
</tr>
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<td>27</td>
<td>1</td>
<td>R18</td>
<td>8.06kΩ</td>
<td>0603</td>
<td>RALEC</td>
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</tr>
<tr>
<td>28</td>
<td>1</td>
<td>C5</td>
<td>22pF</td>
<td>0603</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>1</td>
<td>D3</td>
<td>BAV21</td>
<td>SOD-123</td>
<td>Willas</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>1</td>
<td>R11</td>
<td>82Ω</td>
<td>0603</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>1</td>
<td>EC2</td>
<td>33μF/50V</td>
<td>CES-5X11</td>
<td>Rubycon</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>1</td>
<td>T1</td>
<td>EDR28</td>
<td>EDR28</td>
<td>Abliss</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>1</td>
<td>U1</td>
<td>RT7302</td>
<td>SOP-8</td>
<td>Richtek</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>1</td>
<td>D1</td>
<td>SF26</td>
<td>DO-15</td>
<td>Willas</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>1</td>
<td>R1</td>
<td>33Ω</td>
<td>1206</td>
<td>RALEC</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>1</td>
<td>C1</td>
<td>220pF/1kV</td>
<td>1206</td>
<td>Murata</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>1</td>
<td>EC1</td>
<td>270μF/63V</td>
<td>CES-10X25</td>
<td>Rubycon</td>
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<tr>
<td>38</td>
<td>1</td>
<td>L1</td>
<td>110μH</td>
<td>LR-T9</td>
<td>Abliss</td>
<td>T9<em>5</em>3(μi=10000)</td>
</tr>
<tr>
<td>39</td>
<td>1</td>
<td>R4</td>
<td>200kΩ</td>
<td>1206</td>
<td>RALEC</td>
<td></td>
</tr>
</tbody>
</table>
Transformer design: The transformer design specification is shown in Figure 5.

<table>
<thead>
<tr>
<th>Transformer Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Size: EDR-28</td>
</tr>
<tr>
<td>Material: PC40</td>
</tr>
<tr>
<td>Bobbin/PINS: Horizontal / 7pins</td>
</tr>
<tr>
<td>Primary inductor: (± 5%) 920μH</td>
</tr>
<tr>
<td>Leakage inductor: 30μH</td>
</tr>
</tbody>
</table>

**Electrical:**

**Winding Specifications:**

<table>
<thead>
<tr>
<th>Winding No</th>
<th>PIN</th>
<th>Wire</th>
<th>Turns</th>
<th>Winding Type</th>
<th>Tape Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>3 → 4</td>
<td>0.27μ̈</td>
<td>28T</td>
<td>Close winding</td>
<td>2 Layers</td>
</tr>
<tr>
<td>N2</td>
<td>6 → 7</td>
<td>Triple wire 0.3μ̈</td>
<td>16T</td>
<td>Close winding</td>
<td>2 Layers</td>
</tr>
<tr>
<td>N3</td>
<td>1 → 2</td>
<td>0.12μ̈ x 4 parallel</td>
<td>7T</td>
<td>Close winding</td>
<td>1 Layer</td>
</tr>
<tr>
<td>N4</td>
<td>4 → 5</td>
<td>0.27μ̈</td>
<td>15T</td>
<td>Close winding</td>
<td>1 Layer</td>
</tr>
</tbody>
</table>

**Figure 5. Transformer specification**

The primary side formed by sandwich structure is used to reduce the leakage inductance of the transformer, improving the efficiency and the output current regulation. To improve radiation EMI, the maximum voltage swing which is on pin 3 of the transformer, should be at the most inner side. To meet the safety standard, Triple wire at the secondary side is normally adopted for providing insulation.
6. Electrical Performance Measurements

Table 3 below shows the LED driver input and output parameters over the full mains voltage range.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>60Hz</td>
<td>90</td>
<td>21.54</td>
<td>45.75</td>
<td>405</td>
<td>18.53</td>
<td>86.02%</td>
<td>0.9960</td>
<td>6.37</td>
</tr>
<tr>
<td>60Hz</td>
<td>100</td>
<td>21.24</td>
<td>45.78</td>
<td>405</td>
<td>18.54</td>
<td>87.29%</td>
<td>0.9960</td>
<td>6.68</td>
</tr>
<tr>
<td>60Hz</td>
<td>110</td>
<td>21.03</td>
<td>45.80</td>
<td>404</td>
<td>18.50</td>
<td>87.98%</td>
<td>0.9954</td>
<td>7.03</td>
</tr>
<tr>
<td>60Hz</td>
<td>120</td>
<td>20.87</td>
<td>45.83</td>
<td>403</td>
<td>18.47</td>
<td>88.50%</td>
<td>0.9950</td>
<td>7.24</td>
</tr>
<tr>
<td>60Hz</td>
<td>132</td>
<td>20.73</td>
<td>45.86</td>
<td>402</td>
<td>18.44</td>
<td>88.93%</td>
<td>0.9944</td>
<td>7.53</td>
</tr>
<tr>
<td>50Hz</td>
<td>180</td>
<td>20.60</td>
<td>46.00</td>
<td>401</td>
<td>18.45</td>
<td>89.54%</td>
<td>0.9908</td>
<td>7.51</td>
</tr>
<tr>
<td>50Hz</td>
<td>200</td>
<td>20.60</td>
<td>46.07</td>
<td>400</td>
<td>18.43</td>
<td>89.46%</td>
<td>0.9886</td>
<td>7.02</td>
</tr>
<tr>
<td>50Hz</td>
<td>220</td>
<td>20.64</td>
<td>46.15</td>
<td>400</td>
<td>18.46</td>
<td>89.44%</td>
<td>0.9851</td>
<td>6.73</td>
</tr>
<tr>
<td>50Hz</td>
<td>230</td>
<td>20.69</td>
<td>46.23</td>
<td>400</td>
<td>18.49</td>
<td>89.38%</td>
<td>0.9832</td>
<td>6.82</td>
</tr>
<tr>
<td>50Hz</td>
<td>240</td>
<td>20.75</td>
<td>46.31</td>
<td>400</td>
<td>18.52</td>
<td>89.27%</td>
<td>0.9811</td>
<td>6.99</td>
</tr>
<tr>
<td>50Hz</td>
<td>264</td>
<td>20.90</td>
<td>46.44</td>
<td>400</td>
<td>18.58</td>
<td>88.88%</td>
<td>0.9738</td>
<td>7.86</td>
</tr>
</tbody>
</table>

Current regulation = 1.23%

$\Delta$Efficiency = 3.52%

Maximum PF = 0.996

Minimum PF = 0.974

As can be seen, the current line regulation is excellent. Driver efficiency meets the target easily, and Power Factor and THDi are fully in line with regulations for lighting applications.

The figures in Table 4 show voltage and current waveforms during various operation conditions:
Table 4. Measured waveforms during various operation conditions

Start-up

Vin = 90Vac: T-start = 630msec  
Vin = 264Vac: T-start = 210msec

Input waveform

Vin = 90Vac  
Vin = 264Vac

Output waveform

Vin = 90Vac  
Vin = 264Vac
**Harmonic content of input current: (IEC61000-3-2)**

Vin = 110Vac: passes Class C and D  
Vin = 230Vac: passes Class C and D

**Conduction EMI**

Vin = 230V-L  
Vin = 230V-N

The demo board passes conducted and radiated EMI at 120V and 230Vac
7. PCB Layout Information

The PCB layout of the reference design is shown in Figure 6 below. It is build from double-sided FR-4 material and uses a narrow form-factor to make it suitable to fit into narrow T8 enclosures.

To minimize EMI, current loops of the gate drive, snubber circuit, output diode and main MOSFET switching loop should be kept as small as possible. Ground of the IC, sense resistor, aux winding and Y-capacitor should all go to one central ground point on the input capacitor ground. Capacitors on the IC COMP pin, ZCD pin and MULT pin should be as close as possible to the IC.

![PCB Layout Diagram]

Figure 6. PCB Layout
8. Summary

With the help of this step by step design guide and the RT7302 design tool, the user is able to quickly design a LED driver that fulfills the requirements for high performance offline LED drivers. The absence of secondary side sensing greatly simplifies the mechanical design, and allows small form-factor PCB design.

When all guidelines are followed, the design should fulfill EMI and pass the surge tests. Although this reference design is for an 18W LED driver, RT7302 can be used in a wide range of LED driver designs, ranging from 8W ~ 60W.

### Related Parts

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
<th>Datasheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT7302</td>
<td>Primary-Side-Regulation Dimmable LED Driver Controller with Active PFC</td>
<td>📄Datasheet</td>
</tr>
<tr>
<td>RT7304</td>
<td>Primary-Side-Regulation Dimmable LED Driver Controller with Active PFC</td>
<td>📄Datasheet</td>
</tr>
</tbody>
</table>

### Next Steps

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