

# Speaker Amplifier with Speaker Protection

## General Description

The RT5509 is a mono BTL class-D amplifier with cutting-edge speaker protection algorithm. Also, a built-in DC-DC step-up converter is used to provide efficient power for class-D amplifier. I<sup>2</sup>S interface supports two different audio sources while a pair of auxiliary DATAI/O is used for stereo mode or pass-through application. Chip information including gain, speaker protection output or current sense is able to be monitored via DATAO through proper register setting. Speaker protection provides mechanical / thermal protection with accuracy of 10%/±10°C of rated limit.

## Ordering Information

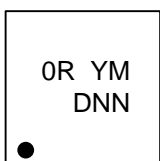
RT5509□  
 □ Package Type  
 WSC : WL-CSP-48B 3.04x2.99 (BSC)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information



0R : Product Code  
 YMDNN : Date Code

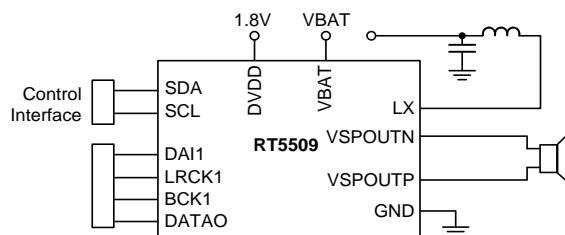
## Features

- **Class-D Speaker AMP**
  - ▶ 4.3W Output Power @ 9.5V, 8Ω Load, THD < 1%
  - ▶ 0/3/6/9/12/15/18dB Boost Gain
  - ▶ 20μV Output Noise @ 0dB Gain
- **Boost Converter**
  - ▶ Adaptive Boost for Speaker, Boost from Battery Supply Up to Programmed Voltage, Max 9.5V
  - ▶ Power Modes : Adaptive Boost, Fixed Boost, Bypass Mode
  - ▶ Switching Frequency 2MHz, Maximum Output Current 1.5A
  - ▶ Support CCM / DCM Compensation, Feedback AD
  - ▶ Digital Part : Voltage Loop in Boost Mode
- **Digital**
  - ▶ Digital Audio Interface Support I<sup>2</sup>S, Left-Justified, Right-Justified
  - ▶ I<sup>2</sup>S Sampling Rate Support Up to 48kHz, 24-bit
  - ▶ Digital Filter, Digital Volume, DRC/Noise Gate
  - ▶ Speaker Protection
  - ▶ Speaker Amplitude Estimation Accuracy : Error < 10%
  - ▶ BI Calibration Function
  - ▶ Temperature Sensing
  - ▶ Speaker Temperature Estimation Accuracy : Error < ±10°C

## Applications

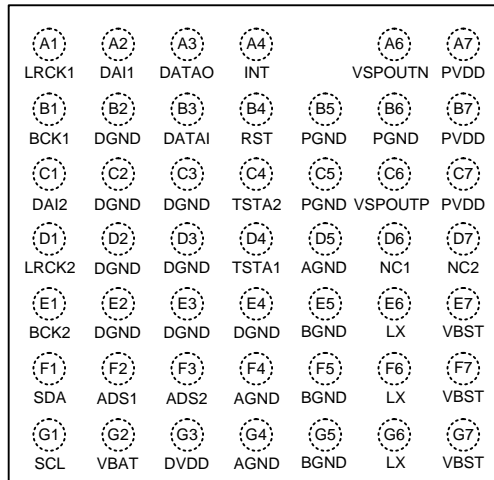
- Smart Phone
- Tablet

## Simplified Application Circuit



Pin Configuration

(TOP VIEW)



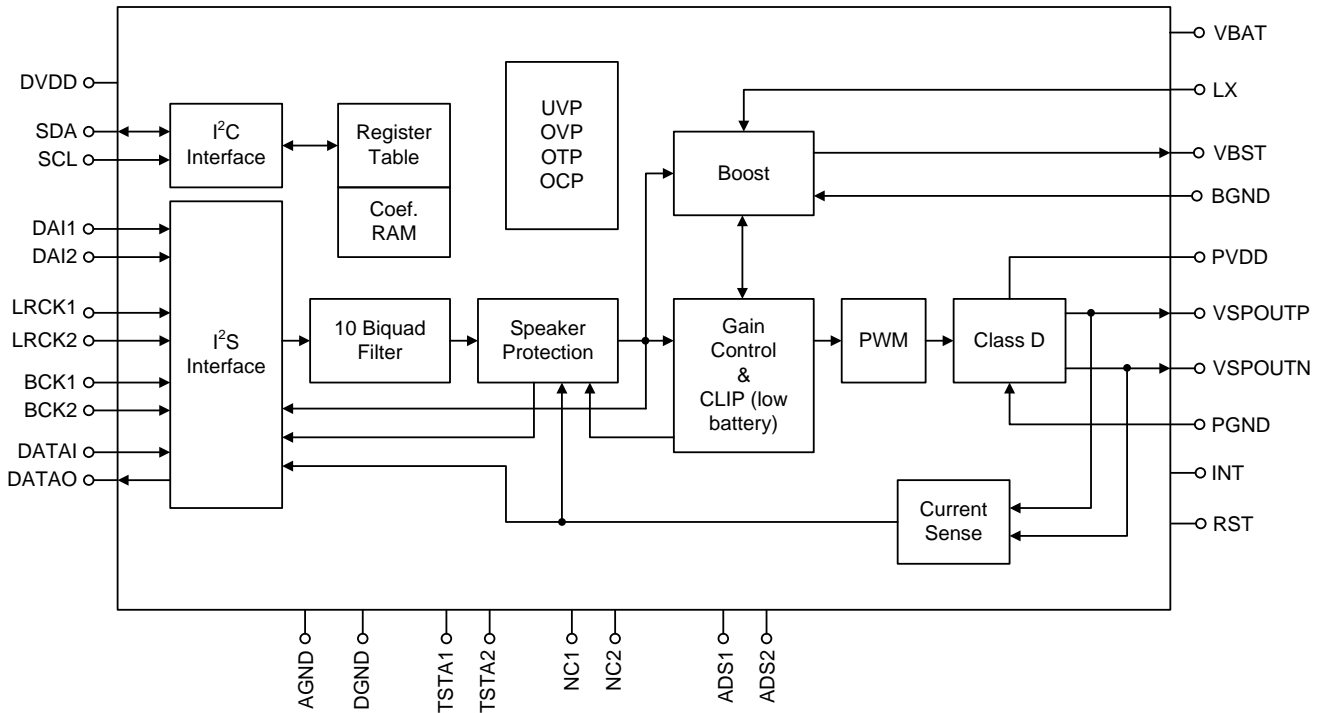
WL-CSP-48B 3.04x2.99 (BSC)

Functional Pin Description

| Pin No. | Pin Name | Type | Pin Function                    |
|---------|----------|------|---------------------------------|
| A1      | LRCK1    | I    | I <sup>2</sup> S word select 1. |
| A2      | DAI1     | I    | I <sup>2</sup> S data input 1.  |
| A3      | DATAO    | O    | I <sup>2</sup> S data output.   |
| A4      | INT      | O    | Interrupt output.               |
| A6      | VSPOUTN  | O    | Class-D inverting output.       |
| A7      | PVDD     | P    | Class-D supply voltage.         |
| B1      | BCK1     | I    | I <sup>2</sup> S Bit clock 1.   |
| B2      | DGND     | G    | Digital / Analog ground.        |
| B3      | DATAI    | I    | I <sup>2</sup> S data input 3.  |
| B4      | RST      | I    | Reset input.                    |
| B5      | PGND     | G    | Power ground.                   |
| B6      | PGND     | G    | Power ground.                   |
| B7      | PVDD     | P    | Class-D supply voltage.         |
| C1      | DAI2     | I    | I <sup>2</sup> S data input 2.  |
| C2      | DGND     | G    | Digital ground.                 |
| C3      | DGND     | G    | Digital ground.                 |
| C4      | TSTA2    | O    | Test output 2 / short to GND.   |
| C5      | PGND     | G    | Power ground.                   |
| C6      | VSPOUTP  | O    | Class-D non-inverting output.   |
| C7      | PVDD     | P    | Class-D supply voltage.         |
| D1      | LRCK2    | I    | I <sup>2</sup> S word select 2. |

| Pin No. | Pin Name | Type | Pin Function                     |
|---------|----------|------|----------------------------------|
| D2      | DGND     | G    | Digital ground.                  |
| D3      | DGND     | G    | Digital ground.                  |
| D4      | TSTA1    | O    | Test output 1/ short to GND.     |
| D5      | AGND     | G    | Analog ground.                   |
| D6      | NC1      |      | No internal connection.          |
| D7      | NC2      |      | No internal connection.          |
| E1      | BCK2     | I    | I <sup>2</sup> S bit clock 2.    |
| E2      | DGND     | G    | Digital ground.                  |
| E3      | DGND     | G    | Digital ground.                  |
| E4      | DGND     | G    | Digital ground.                  |
| E5      | BGND     | G    | Boosted ground.                  |
| E6      | LX       | P    | Boost converter input.           |
| E7      | VBST     | O    | Boosted supply voltage.          |
| F1      | SDA      | I/O  | I <sup>2</sup> C data.           |
| F2      | ADS1     | I    | Address select 1.                |
| F3      | ADS2     | I    | Address select 2.                |
| F4      | AGND     | G    | Analog ground.                   |
| F5      | BGND     | G    | Boosted ground.                  |
| F6      | LX       | P    | Boost converter input.           |
| F7      | VBST     | O    | Boosted supply voltage.          |
| G1      | SCL      | I    | I <sup>2</sup> C clock.          |
| G2      | VBAT     | I    | Battery supply sense input.      |
| G3      | DVDD     | P    | Digital / Analog supply voltage. |
| G4      | AGND     | G    | Analog ground.                   |
| G5      | BGND     | G    | Boosted ground.                  |
| G6      | LX       | P    | Boost converter input.           |
| G7      | VBST     | O    | Boosted supply voltage.          |

Functional Block Diagram



**Absolute Maximum Ratings** (Note 1)

- VBST, PVDD ----- -0.3 to 13V
- VSPOUTP, VSPOUTN, LX ----- -0.3 to 13V
- VSPOUTP, VSPOUTN, LX ----- -1.4 to 16V (Note 6)
- VBAT ----- -0.3 to 6V
- DVDD ----- -0.3 to 2.5V
- LRCK, BCK, DATA I/O, ADS1, ADS2 ----- -0.3 to (DVDD + 0.3V)
- SCL, SDA ----- -0.3 to 6V
- RST ----- -0.3 to (DVDD + 0.3V)
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C
  - WL-CSP-48B 3.04x2.99 (BSC) ----- 3.7W
- Package Thermal Resistance (Note 2)
  - WL-CSP-48B 3.04x2.99 (BSC), θ<sub>JA</sub> ----- 27°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ----- 2kV

**Recommended Operating Conditions** (Note 4)

- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

**Electrical Characteristics**

(VBAT = 3.6V, DVDD = 1.8V, T<sub>A</sub> = 25°C, unless otherwise specified)

| Parameter                      | Symbol                    | Test Conditions  | Min  | Typ | Max | Unit |
|--------------------------------|---------------------------|--|------|-----|-----|------|
| <b>Power Supplies</b>          |                           |  |      |     |     |      |
| Digital Supply Voltage         | DVDD                      |  | 1.71 | 1.8 | 2   | V    |
| Speaker Amp Supply Voltage     | PVDD                      |  | 2.7  | 3.6 | 9.5 | V    |
| Battery Supply Voltage         | VBAT                      |  | 2.7  | 3.6 | 5.5 | V    |
| Boost Converter Output Voltage | VBST                      |  | 2.7  | --  | 9.5 | V    |
| Shutdown Current (VBAT)        | I <sub>SD_VBAT</sub>      | DVDD = 1.8V  | 0    | 1   | 5   | μA   |
| Leakage Current (VBAT)         | I <sub>LEAKAGE_VBAT</sub> | DVDD = 0V  | 0    | 1   | 5   | μA   |
| Leakage Current (DVDD)         | I <sub>LEAKAGE_DVDD</sub> | VBAT = 2.7 to 5.5V, DVDD = 1.8V, BCK = LRCK = DAI = 0V | 0    | 8   | 20  | μA   |
| Offset Voltage                 | V <sub>OS</sub>           | PVDD = 3.6V  | 0    | 2   | 6   | mV   |

| Parameter   | Symbol                    | Test Conditions   | Min        | Typ  | Max        | Unit |
|---|---------------------------|---|------------|------|------------|------|
| <b>DAC to Stereo Speaker Amplifier</b>                              |                           |   |            |      |            |      |
| Signal to Noise Ratio   | SNR                       | PVDD = 9.5V, THD+N < 1%, Gain = 12dB, A-Weighting                       | 92         | 100  | 108        | dB   |
| Noise level   | Vn                        | Gain = 0dB, A-Weighting   | 15         | 20   | 25         | μV   |
|   |                           | Gain = 12dB, A-Weighting  | 35         | 40   | 45         |      |
|   |                           | Gain = 18dB, A-Weighting  | 55         | 60   | 65         |      |
| Maximum Output Power  | Po                        | 1kHz, PVDD = 3.6V, 8Ω load + 22μH, THD + N = 1%                         | 0.6        | 0.65 | 0.7        | W    |
|   |                           | 1kHz, PVDD = 9.5V, 8Ω load + 22μH, THD + N = 1%                         | 4.2        | 4.3  | 4.4        |      |
| THD+N   |                           | 1kHz, Po = 350mW, 8Ω load + 22μH  | -90        | -75  | -50        | dB   |
| PSRR  |                           | 217Hz ripple = 200mVpp  | -85        | -75  | -65        | dB   |
| Quiescent Current (VBAT)  | I <sub>Q_VBAT</sub>       | Normal operation, DSP, speaker protection bypassed                      | 1          | 3    | 5          | mA   |
| Quiescent Current (DVDD)  | I <sub>Q_DVDD</sub>       | Normal operation, DSP, speaker protection bypassed                      | 6          | 12   | 18         | mA   |
|   |                           | Normal operation, DSP, speaker protection activated                     | 12         | 18   | 24         |      |
| Output Power Efficiency   | η                         | P <sub>O</sub> = 2.5W, including DC to DC converter, 100Hz audio signal | 70         | 76   | 80         | %    |
| <b>I<sup>2</sup>C Interface Electrical Characteristics</b> (Note 5) |                           |   |            |      |            |      |
| SDA, SCL Input Threshold  | V <sub>IH</sub>           |   | 0.7 x DVDD | --   | --         | V    |
|   | V <sub>IL</sub>           |   | --         | --   | 0.3 x DVDD |      |
| Pull-Down Current   | I <sub>FO2</sub>          |   | --         | 2    | --         | μA   |
| Digital Output Low (SDA)  | V <sub>OL</sub>           | I <sub>PULLUP</sub> = 3mA   | --         | --   | 0.4        | V    |
| Clock Operating Frequency   | f <sub>SCL</sub>          |   | --         | --   | 400        | kHz  |
| Bus Free Time Between Stop and Start Condition                      | t <sub>BUF</sub>          |   | 1.3        | --   | --         | μs   |
| Hold Time After (Repeated) Start Condition                          | t <sub>HD,STA</sub>       |   | 0.6        | --   | --         | μs   |
| Repeated Start Condition Setup Time                                 | t <sub>SU,STA</sub>       |   | 0.6        | --   | --         | μs   |
| Stop Condition Time   | t <sub>SU,STD</sub>       |   | 0.6        | --   | --         | μs   |
| Data Hold Time  | t <sub>HD,DAT (OUT)</sub> |   | 225        | --   | --         | ns   |
| Input Data Hold Time  | t <sub>HD,DAT (IN)</sub>  |   | 0          | --   | 900        | ns   |
| Data Setup Time   | t <sub>SU,DAT</sub>       |   | 100        | --   | --         | ns   |
| Clock Low Period  | t <sub>LOW</sub>          |   | 1.3        | --   | --         | μs   |
| Clock High Period   | t <sub>HIGH</sub>         |   | 0.6        | --   | --         | μs   |

| Parameter   | Symbol    | Test Conditions | Min       | Typ | Max       | Unit |
|---|-----------|-----------------|-----------|-----|-----------|------|
| Clock Data Fall Time  | $t_F$     |                 | 20        | --  | 300       | ns   |
| Clock Data Rise Time  | $t_R$     |                 | 20        | --  | 300       | ns   |
| Spike Suppression Time  | $t_{SP}$  |                 | --        | --  | 50        | ns   |
| <b>I<sup>2</sup>S Interface Electrical Characteristics</b> (Note 5) |           |                 |           |     |           |      |
| High-Level Input Voltage  | $V_{IH}$  |                 | 0.7x DVDD | --  | --        | V    |
| Low-Level Input Voltage   | $V_{IL}$  |                 | --        | --  | 0.3x DVDD | V    |
| Setup Time, LRCK to SCLK Rising Edge                                | $t_{su1}$ |                 | 10        | --  | --        | ns   |
| Hold Time, LRCK from SCLK Rising Edge                               | $t_{h1}$  |                 | 10        | --  | --        | ns   |
| Setup Time, SDIN to SCLK Rising Edge                                | $t_{su2}$ |                 | 10        | --  | --        | ns   |
| Hold Time, SDIN from SCLK Rising Edge                               | $t_{h2}$  |                 | 10        | --  | --        | ns   |
| Rise/Fall Time for SCLK/LRCLK                                       | $t_r$     |                 | --        | --  | 8         | ns   |

**Note 1.** Continuously stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured under natural convection (still air) at  $T_A = 25^\circ\text{C}$  with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Guaranteed by design.

**Note 6.** The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

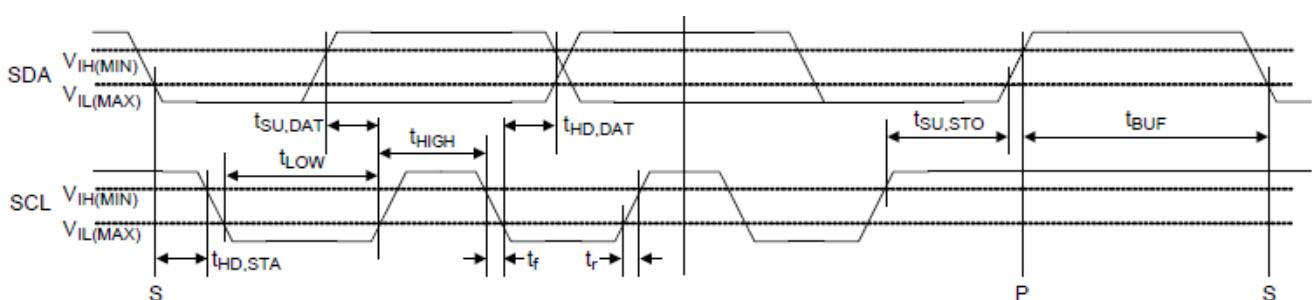


Figure 1. I<sup>2</sup>C Interface Trimming Diagram

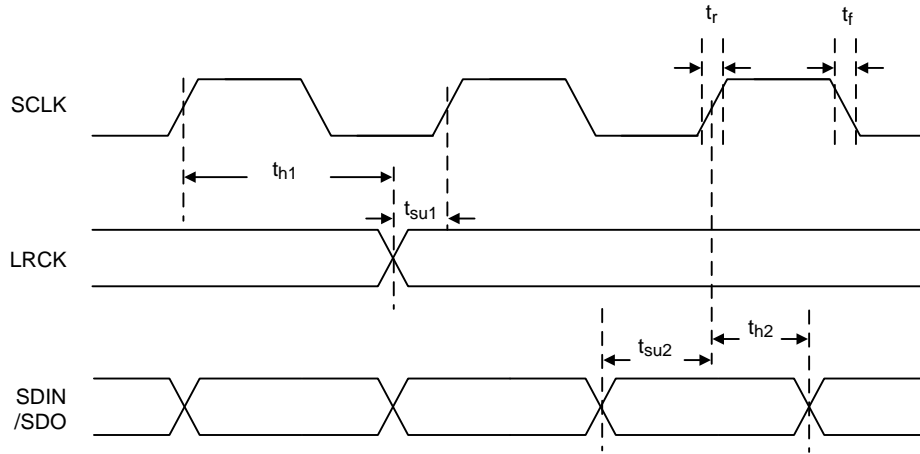


Figure 2. Timing Diagram of Slave Mode I<sup>2</sup>S Interface



**Typical Application Circuit**

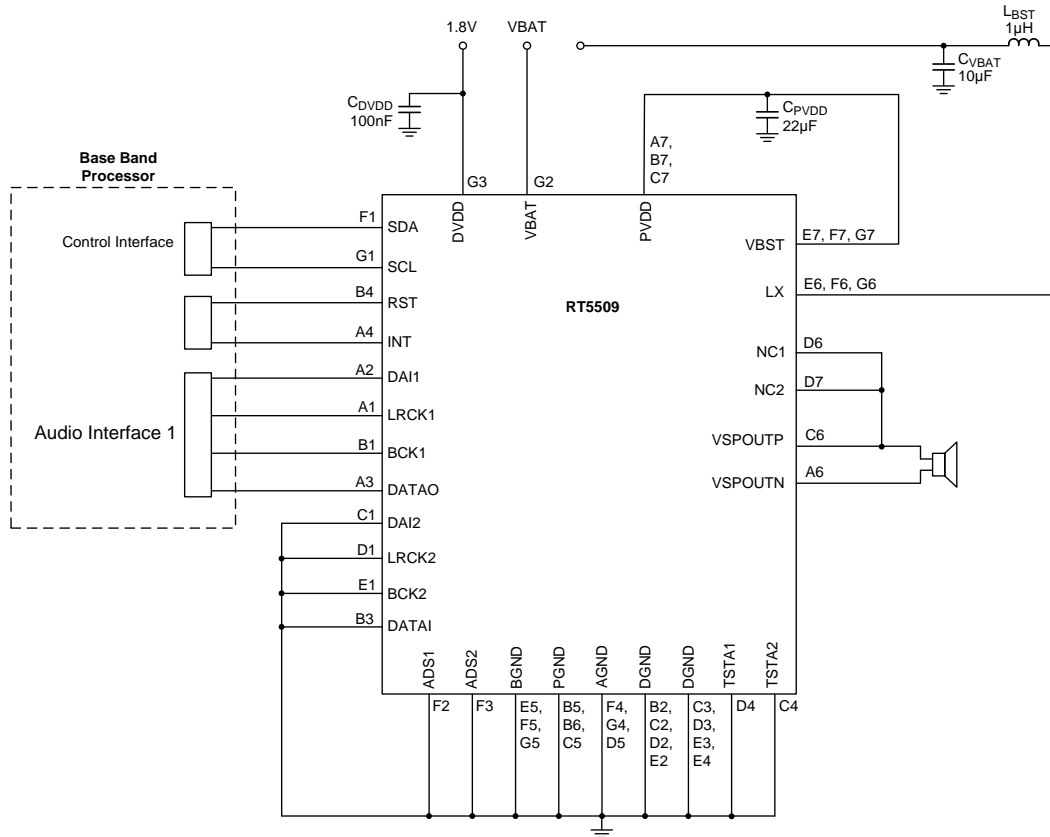


Figure 3. Mono Mode Application Circuit

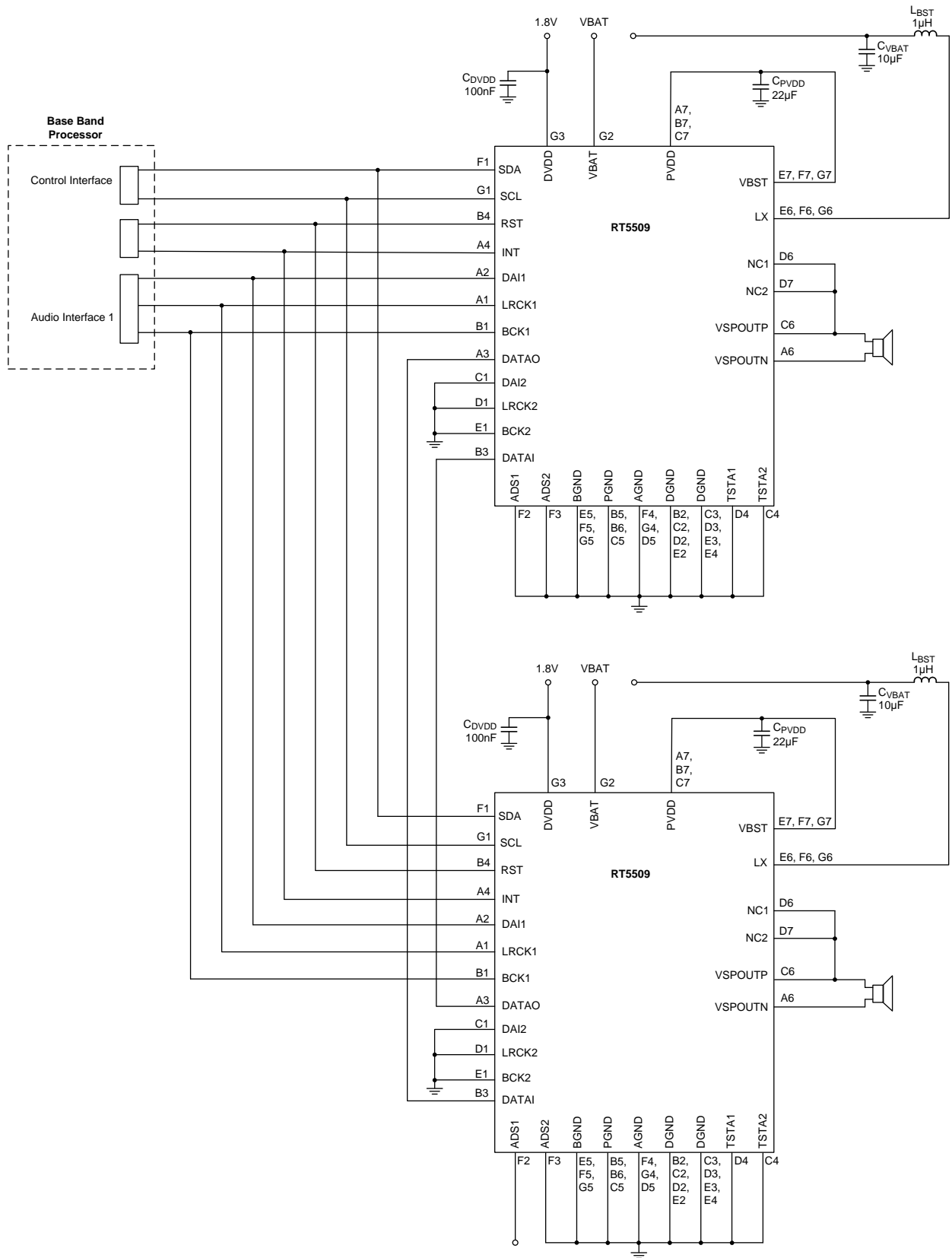
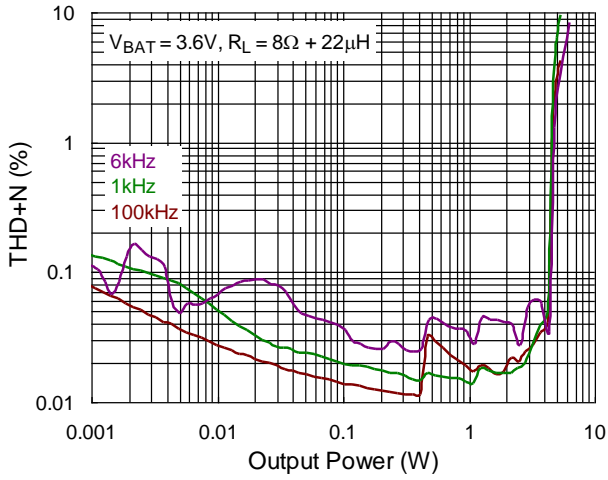


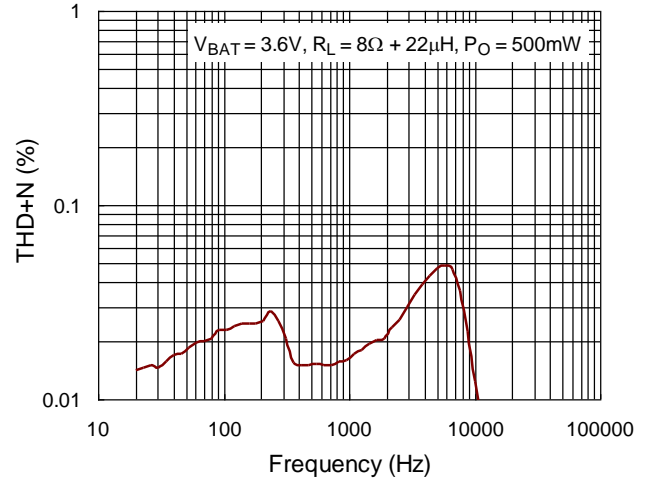
Figure 4. Stereo Mode Application Circuit

**Typical Operating Characteristics**

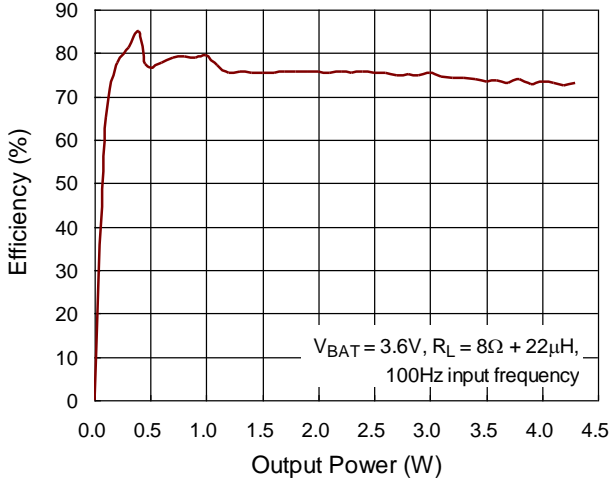
**THD+N vs. Output Power**



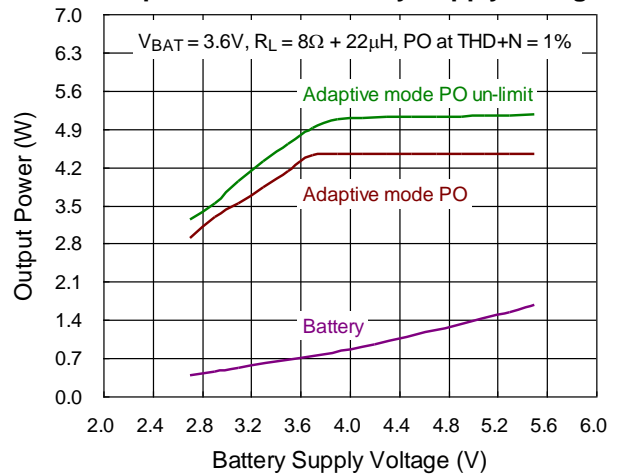
**THD+N vs. Frequency**



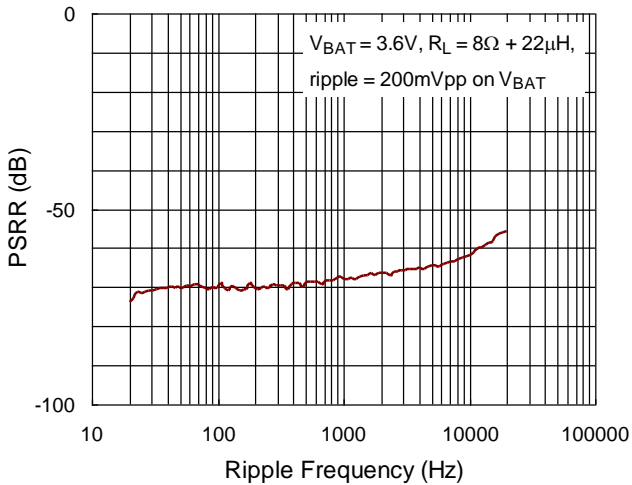
**Efficiency vs. Output Power**



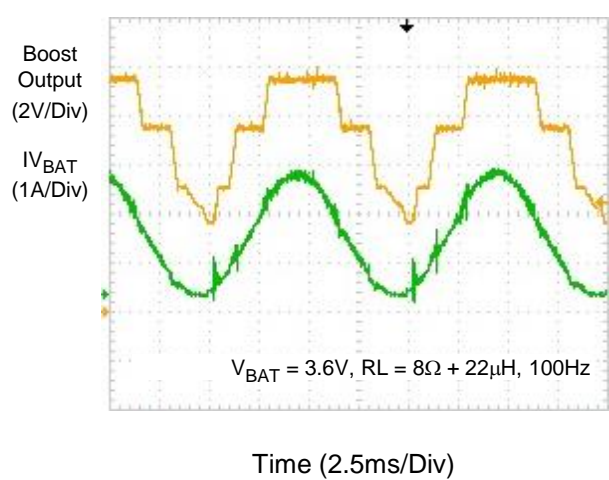
**Output Power vs. Battery Supply Voltage**



**PSRR**



**Boost Change Mode Behavior**



## I<sup>2</sup>C Interface

### Device Addressing

The RT5509 support I<sup>2</sup>C control interface. The default device address is accessed via Pin ADS1 and ADS2. (see Table 1.) Four separate address are supported for stereo mode application. The levels on pins ADS1 and

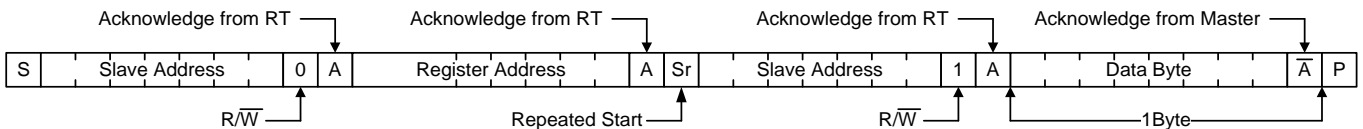
ADS2 determine the values of bits 1 and 2, respectively. The generic address is independent of pins ADS1 and ADS2.

**Table 1. Address Selection Via Pins ADS1 and ADS2**

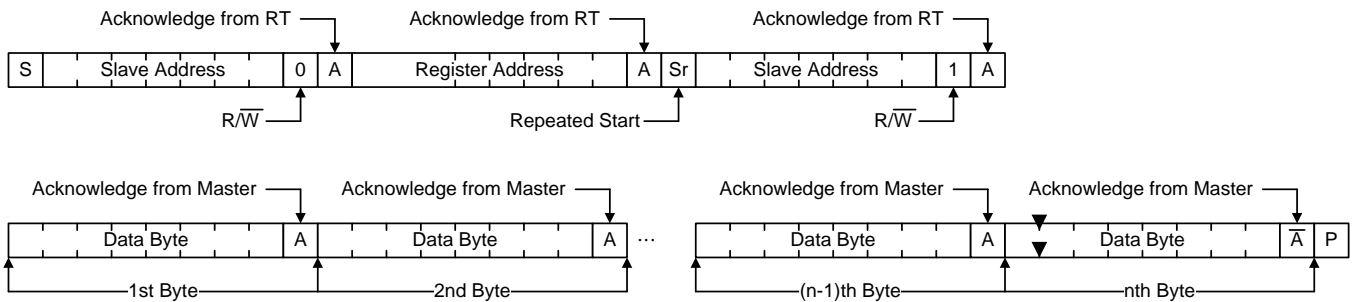
| ADS2 Pin (V) | ADS1 Pin (V) | Address  | Function (bit 0)   |
|--------------|--------------|----------|--------------------|
| 0            | 0            | 0110100x | 0 : write 1 : read |
| 0            | DVDD         | 0110101x | 0 : write 1 : read |
| DVDD         | 0            | 0110110x | 0 : write 1 : read |
| DVDD         | DVDD         | 0110111x | 0 : write 1 : read |

### Read Function

Reading One Indexed Byte of Data from RT (With 1-Byte)

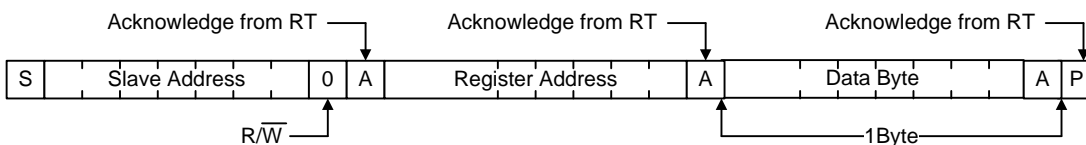


Reading n Indexed Words of Data from RT (With N-Byte)

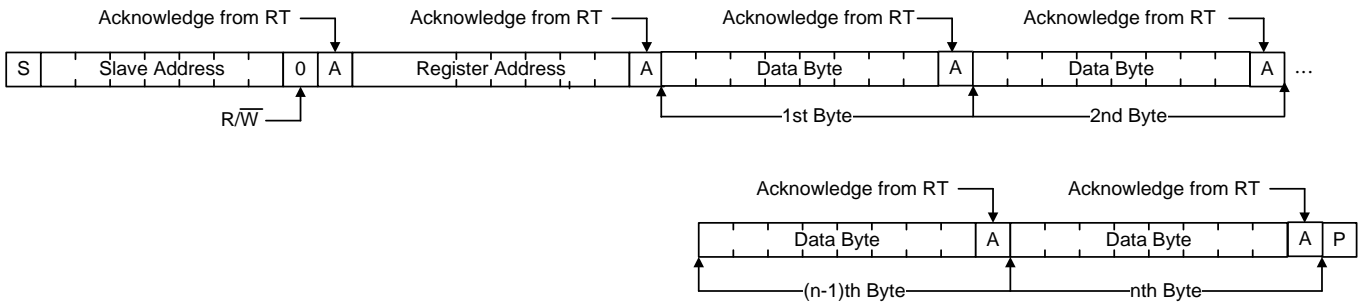


### Write Function

Writing One Byte of Data to RT (With 1-Byte)



Writing n Byte of Data to RT (With N-Byte)



## Operation Mode

The RT5509 can operate in six different modes which are power-down / suspend / operating / mute / off / fault.

Internal functional block operational status in different mode is depicted in Figure 5.

| Mode<br>Bik      | PWDN | SUSP | OP | MUTE | OFF | FAULT |
|------------------|------|------|----|------|-----|-------|
| PLL              | ×    | ○    | ○  | ○    | ○   | ○     |
| I <sup>2</sup> C | ○    | ○    | ○  | ○    | ○   | ○     |
| I <sup>2</sup> S | ×    | ×    | ○  | ○    | ○   | ○     |
| SPK              | ×    | ×    | ○  | ○    | ○   | ○     |
| AMP              | ×    | ×    | ○  | △    | ⊠   | ⊠     |

- : Normal operation
- △ : Operational with zero input
- ⊠ : Output floating
- ×

Figure 5. Operation Mode

### Power-Down Mode (PWDN = 1)

When PWDN is set to 1, chip will enter power-down mode.

In power-down mode, power consumption is minimum and PWM outputs are floating.

I<sup>2</sup>C remains awake in power-down mode.

If PWDN is set to 1, I<sup>2</sup>S is also disabled.

### Suspend Mode (BCK/LRCK Invalid)

When BCK/LRCK is invalid, chip will enter suspend mode.

In suspend mode, most of the data path are off, and PWM outputs are floating.

I<sup>2</sup>C remains awake in power-down mode.

PLL keeps awake used to monitor BCK/LRCK on I<sup>2</sup>S bus to see if they are correct.

### Operating Mode (PWDN = 0, SPKE = 1, SPKM = 0, AMPE = 1)

Operating mode is selected via PWDN/SPKE/SPKM/AMPE at register 0xXX. One of I<sup>2</sup>S interface (DATA1/DATA2) is selected as the audio source. In

operating mode, the frequency of LRCK should be the same as I<sup>2</sup>SFS.

### Mute Mode (PWDN = 0, SPKE = 1, SPKM = 1, AMPE = 1)

Soft muting is used to prevent pop noise and is implemented in the speaker protection block when SPKE set to logic 1. Ramp up/down in exponential scale are implemented when switching between muted and unmuted mode.

### Off Mode (PWDN = 0, SPKE = 1, AMPE = 0)

The outputs of class-D are floating and chip is biased in off mode.

Soft mute can be executed if AMPDS at register 0xXX equals to 1 before chip enters off mode.

### Fault Mode

Chip enters fault mode when an error event of physical protection mechanisms occurs (OCP/OVP/UVP/OTP).

The outputs of class-D are floating in Fault mode. The system exits from Fault mode after the protection event released for a checking cycle of about 200ms.

**Mode Transition**

The state machine of mode transition is shown in Figure 6. “Mute” mode is not shown in this figure since it can be considered as the sub-mode of the normal Operating mode, only with zero input signal.

The “Off” mode is usually used only in the power down sequence, and is depicted in the next sub-clause.

After power on, the control bit will always be reset to PWDN mode.

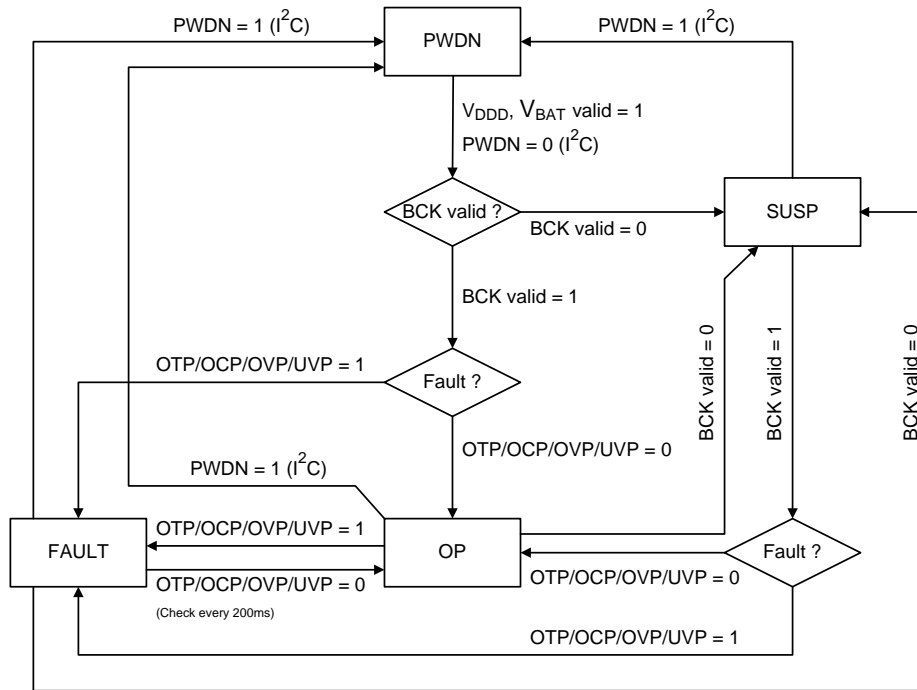


Figure 6. Mode Transition

**Power ON Sequence**

The power on sequence is shown in Figure 7. After power is valid, two groups of control signals should be set, without specific order requirement between these two groups :

1. I<sup>2</sup>C : PWDN, AMPE, SPKE should be programmed. These three bits can be programmed by single command since they are at the same byte address.
  2. I<sup>2</sup>C : I<sup>2</sup>SDIS, I<sup>2</sup>SDF, I<sup>2</sup>SFS set for reference clock selection for PLL.
- I<sup>2</sup>S : BCK should be valid on the specified interface.

If the PWDN is set to 0 before the BCK valid, it will go to SUSP mode automatically. The output of amplifier will be valid after entering OP mode, signal ramp up will always be implemented when the mode transits from PWDN or SUSP mode to OP mode.

**Power OFF Sequence**

The power off sequence is shown in Figure 8. PWDN mode should be set before the power supplies disconnected. To avoid pop or click, the amplifier should be turned off by setting AMPE = 0 before power down. Soft muting will also be enabled automatically if AMPDS bit is set to 1, which further ensures a pop-free procedure.

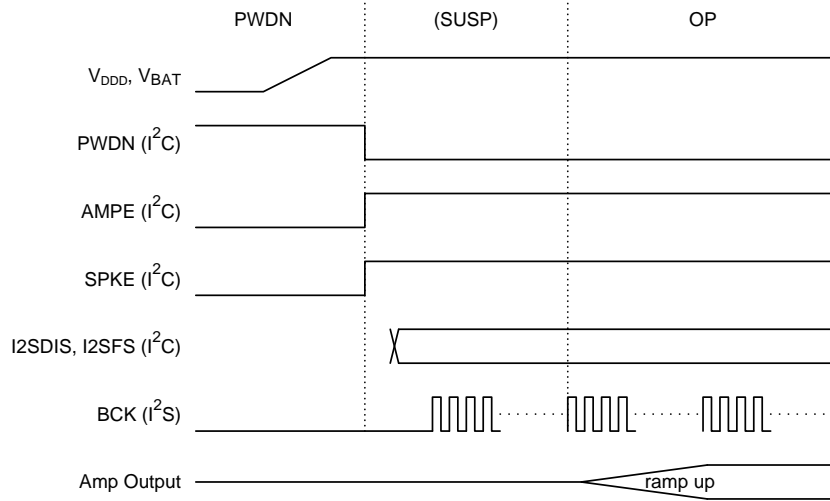


Figure 7. Power ON Sequence

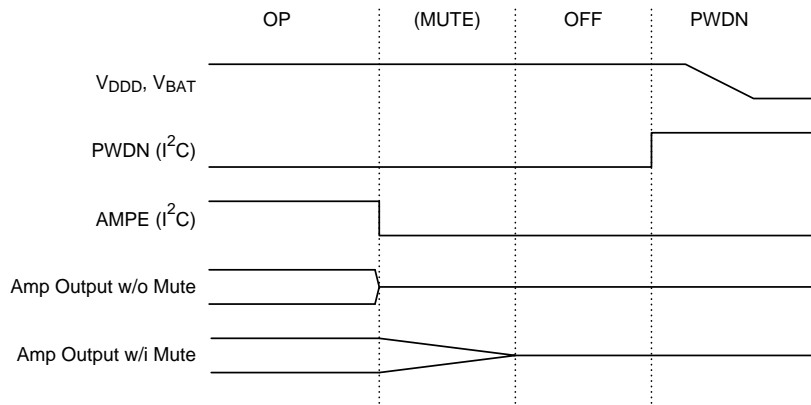


Figure 8. Power OFF Sequence

**I<sup>2</sup>S Mode Change without PWDN**

Suspend mode is detected if the clock source from I<sup>2</sup>S is not valid according to the value of I<sup>2</sup>SDF/I<sup>2</sup>SFS. In this case, soft muting is implemented before entering suspend mode. In the opposite situation, if the clock

source from I<sup>2</sup>S is detected valid again, signal ramp up is implemented at the start after it enters the operating mode.

The above procedure is shown in Figure 9.

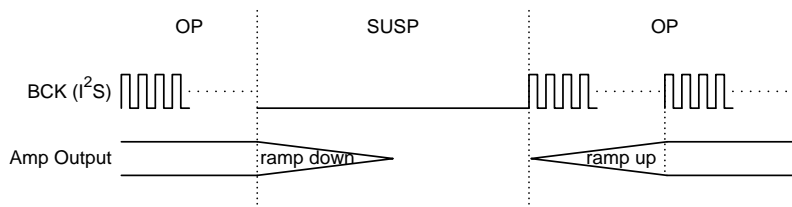


Figure 9. I<sup>2</sup>S Mode Change without PWDN



## Data (I<sup>2</sup>S) Interface

### Data Format

The I<sup>2</sup>S formats supported by the RT5509 are listed below :

| Interface                 | Data Format  | BCK Frequency |
|---------------------------|--------------|---------------|
| I <sup>2</sup> S Standard | up to 16-bit | 32fs          |
| I <sup>2</sup> S Standard | up to 24-bit | 48fs          |
| I <sup>2</sup> S Standard | up to 24-bit | 64fs          |
| MSB-justified             | up to 16-bit | 32fs          |
| MSB-justified             | up to 24-bit | 48fs          |
| MSB-justified             | up to 24-bit | 64fs          |
| LSB-justified (16-bit)    | 16-bit       | 32fs          |
| LSB-justified (16-bit)    | 16-bit       | 48fs          |
| LSB-justified (16-bit)    | 16-bit       | 64fs          |
| LSB-justified (18-bit)    | 18-bit       | 48fs          |
| LSB-justified (18-bit)    | 18-bit       | 64fs          |
| LSB-justified (20-bit)    | 20-bit       | 48fs          |
| LSB-justified (20-bit)    | 20-bit       | 64fs          |
| LSB-justified (24-bit)    | 24-bit       | 48fs          |
| LSB-justified (24-bit)    | 24-bit       | 64fs          |

fs : 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

### I<sup>2</sup>S Sampling Rate

I<sup>2</sup>S can support sampling rate of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz. As shown in Figure 10, the

sampling rate conversion block is applied to convert the data to internal working sampling rate, that is 44.1kHz or 48kHz. In stereo mode, the gain between two paths can be passed through each other.

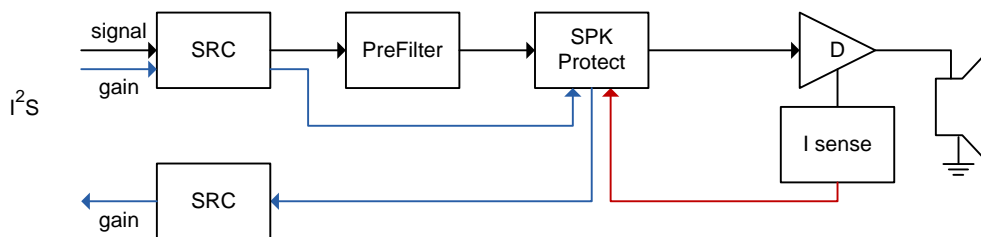


Figure 10. Sampling Rate

### Setting I<sup>2</sup>S Format / Sampling Rate

I<sup>2</sup>S data format and fs can be set by I<sup>2</sup>SFOMAT and I<sup>2</sup>SRATE at register 0x04 to 0x05.

The RT5509 should be configured to power down or suspend mode before changing I<sup>2</sup>SFORMAT/I<sup>2</sup>SRATE.

### Input Path

I<sup>2</sup>S input interface is shown in Figure 11. An internal mux select for two audio sources are supported. DATA1 is used to provide stereo or pass-through application and uses BCK1/2, LRCK1/2 as its clock and word select signal. The active I<sup>2</sup>S input is selected by I<sup>2</sup>SDIS

and I<sup>2</sup>SCHS at register 0x06. After selecting I<sup>2</sup>S input source, I<sup>2</sup>SLRS can be used to decide which channel (left, right or mixed) is sent to bi-quads.

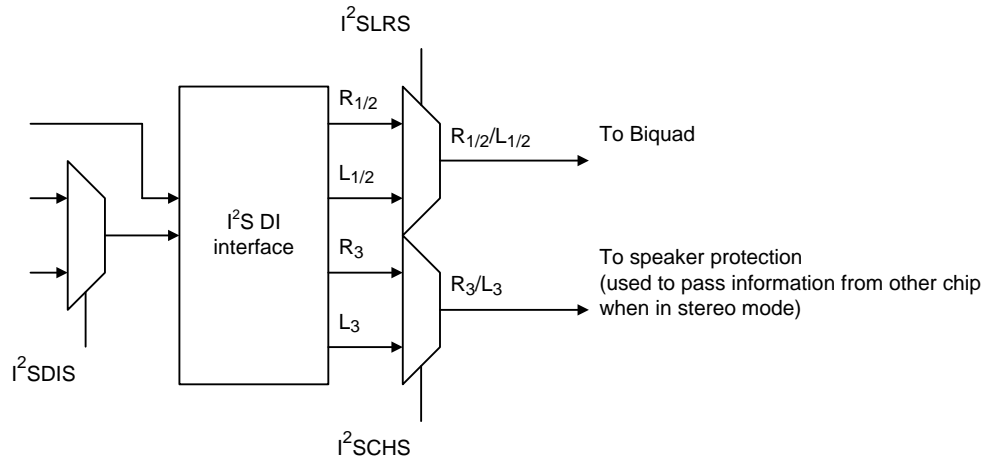


Figure 11. I<sup>2</sup>S Input Mux

**Output Path**

DATAO can output different data via I<sup>2</sup>SDOS/I<sup>2</sup>SDOR /I<sup>2</sup>SDOL at register 0x07 to 0x08. It can also be disabled via I<sup>2</sup>SDOE at register 0x08. DATAO uses

BCK1/2 as its reference clock to transmit desired data. LRCK1/2 is referred when I<sup>2</sup>SDOS/I<sup>2</sup>SDOE is switched to output I<sup>2</sup>SDOR/I<sup>2</sup>SDOL.

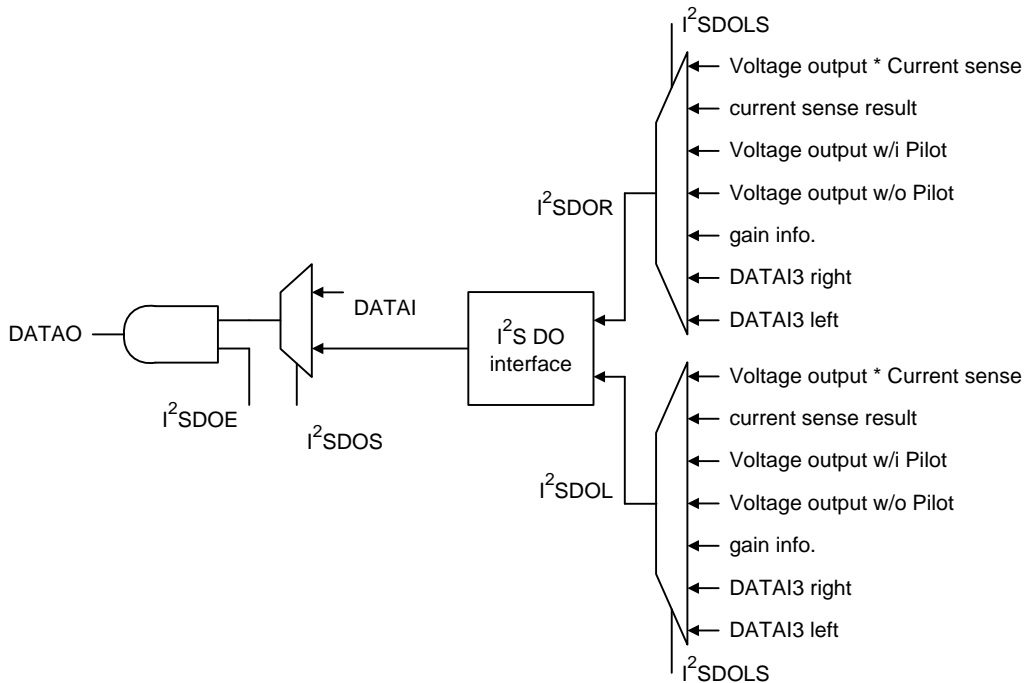


Figure 12. I<sup>2</sup>S Output Mux

**Sampling Rate Delay**

The SRC introduces delay with respect to different I<sup>2</sup>S sampling rates, which is shown in Table 2.

**Table 2. Sampling Rate Conversion Delay**

| I <sup>2</sup> S sampling rate | Delay | Absolute Delay |
|--------------------------------|-------|----------------|
| fs = 8k                        | 29/fs | 3.6ms          |
| fs = 11.025k                   | 28/fs | 2.5ms          |
| fs = 12k                       | 28/fs | 2.3ms          |
| fs = 16k                       | 29/fs | 1.8ms          |
| fs = 22.05k                    | 26/fs | 1.2ms          |
| fs = 24k                       | 26/fs | 1.1ms          |
| fs = 32k                       | 29/fs | 0.9ms          |
| fs = 44.1k                     | 0/fs  | 0ms            |
| fs = 48k                       | 0/fs  | 0ms            |

The I<sup>2</sup>S signals at different sampling rate are all up-sampled to 48ksps or 44.1ksps before DSP processing or pass-through to PWM + class D amplifier. The data path delay is dominated by the group delay of SRC, the look-ahead delay of gain limiter, and some minor delay in SPK protection algorithm (< 0.5ms).

For example : the worst case loopback delay of I<sup>2</sup>S may be about 16ms (3.6 \* 2 + 8 + 0.5) if fs = 8k and look-ahead delay = 8ms.

**Signal Processing Path**

After sampling rate conversion, the signal is processed by two sub-functions as shown in Figure 13. The pre-filters are some audio effect related functions, and the SPK protection block is the core function for speaker protection.

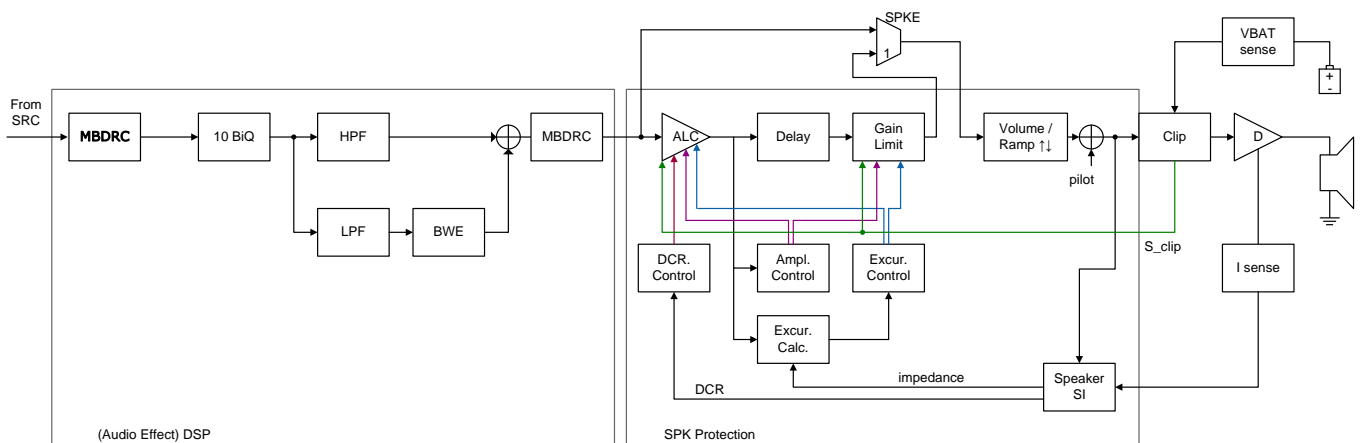


Figure 13. Signal Processing Path

## Pass-Through Mode

There is pass-through mode for debug or application use.

SPKE = 0 viewed as DSP through mode, where the signal is processed by DSP then passed through volume and amplifier.

Set SPKE = 1 to the normal mode, all functions are turned on regardless of the setting of DSPE.

Pilot is always disabled if SPKE = 0.

## Audio Effect DSP Functions

### 10-BiQuad

After channel selection, there are 10 fully programmable bi-quad filters implemented for user-specified frequency response. The coefficients are 24-bit 2's complement numbers, which are set by I<sup>2</sup>C interface.

### Band-Split & BWE

Dedicated HPF/LPF with programmable corner frequency are equipped after 10-Biquad filters, both are implemented by selectable 1<sup>st</sup> or 2<sup>nd</sup> order Butterworth filter.

LPF is only needed when optional BWE is enabled. The BWE block generate harmonic terms to recover the suppressed of low-frequency signal that is not efficiently conveyed on small loudspeaker.

All the HPF/LPF/BWE functions can be bypassed.

### Dynamic Range Control (DRC)

DRC is a specific feature to automatically adjust the volume gain corresponds to different input signal. With DRC function, the output dynamic range is under controlled from input amplitude is unknown or varies over a wide range. The RT5509 provide three thresholds as dynamic range compression (DRC\_TH0), extension (DRC\_TH1) and Noise Gate. For the application of compression and extension, the slope ratio can be programmed as R0 and R1, respectively.

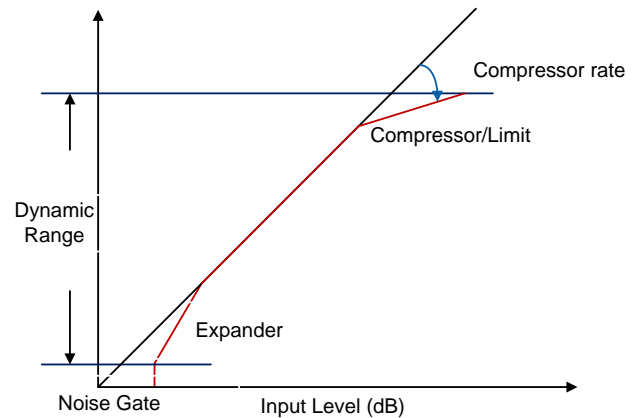


Figure 14. Dynamic Range Control

DRC function is composed of several parts as following Figure. The input signal passes through the programmable Energy Filter (DRC\_AE). The Filter structure is shown in Figure 15. The time constant of each filter can be determined by below equation :

$$t_{\text{window}} = \frac{-1}{f_s \ln(1 - ae)}$$

Then, the filtered signal is compared with the given compression threshold. After the comparison between Input signal amplitude and threshold, the Attack Rate (DRC\_AA) determines how quickly the DRC gain decreases when the signal amplitude is high. The Decay Rate (DRC\_AD) determines how quickly the DRC gain increases when the signal amplitude is low.

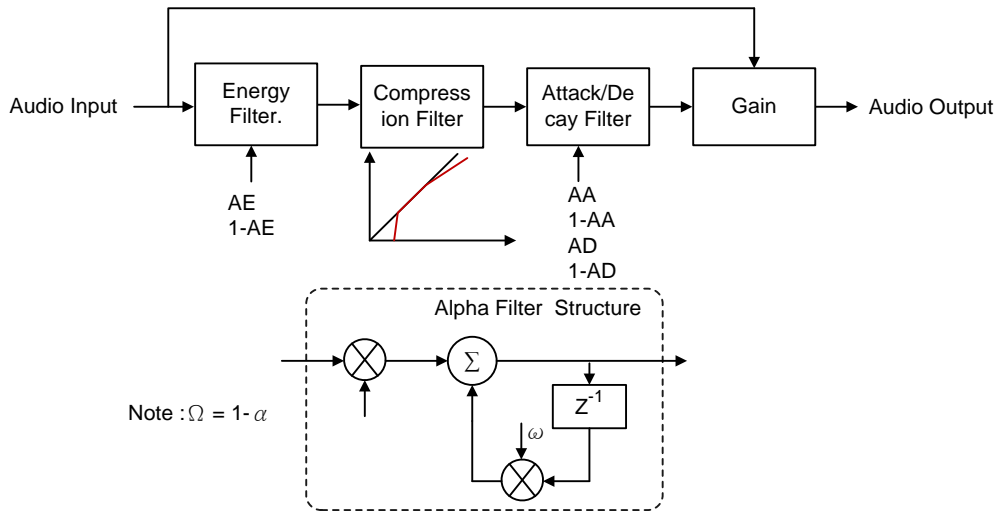


Figure 15. DRC Structure and Signal Processing Path

**Speaker Protection Functions**

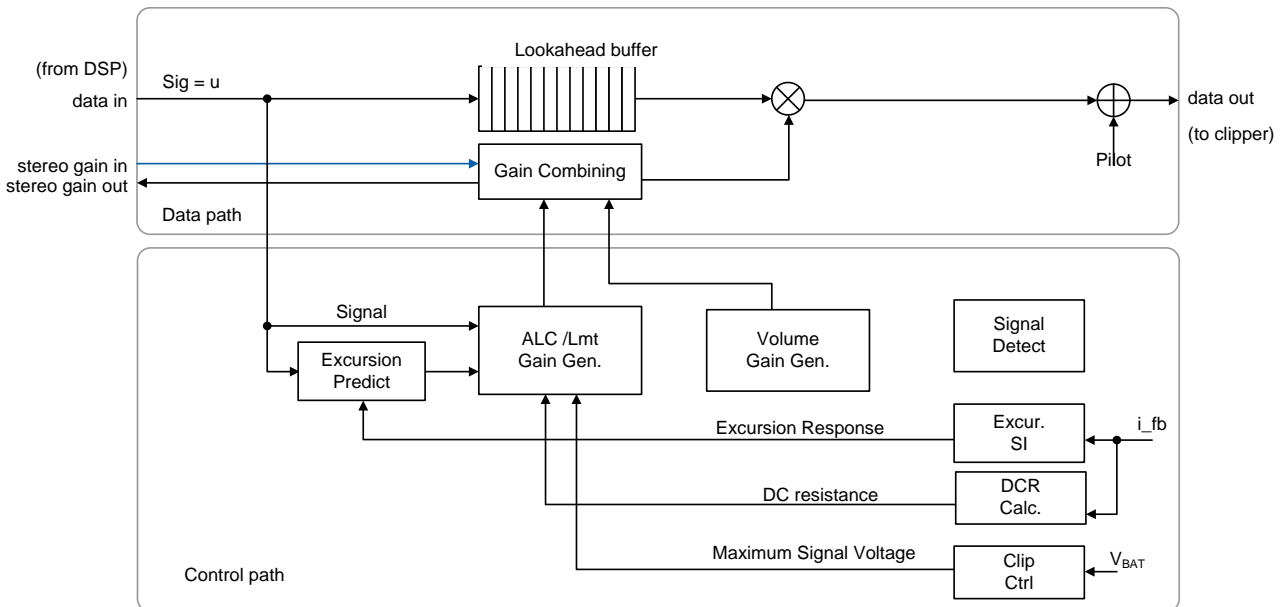


Figure 16. Block Diagram of SPK Protection Function

The following sub-clauses explain the function of each sub-block.

**Look-Ahead Delay Buffer**

Look-ahead delay can be programmed from 0 up to 480 samples, which is up to 10ms at 48k sampling rate. This delay should contain stereo gain synchronization delay.

**Gain Processing on the Data Path**

The level control, limiting for protection, and the volume control are implemented by multiplying the signal on the data path, with the gain generated from the control path.

**Pilot**

The pilot signal, with constant magnitude (30mV) is added at the last stage of data path. The frequency of pilot is fixed  $f_p = 50\text{Hz}$ . The pilot is disabled at

PWDN/SUSPD/Off/Fault/Mute mode. A register control bit can be configured to set if the pilot is also turned off in Silence mode. If yes, then the pilot should be turned off after signal power below threshold for SilenceResetTime. This bit also defines if the DC resistance is monitored or not in Silence mode.

Except for Fault mode, the pilot always turned on or turned off at zero cross level. In worst case the pilot turn-off latency will be 11.6ms.

## Signal Detector

The signal activity is detected when the input signal level is above a user defined threshold. The detection window can be specified to be 5ms/10ms/20ms.

Another long time constant: SilenceRestTime is used to ensure the silence happen and set the ALC to its initial gain.

### Parameters :

sThresAct : silence or active threshold (0 to -90dBFS, -6dB step)

SilenceResetTime : the time to reset ALC gain to initial value (0 to 15 seconds)

## Peak Detector

The peak detector monitors the peak of the signal magnitude and the estimated excursion. The algorithm is described as following equation, with attack time can be specified as 0ms/1ms/2ms/4ms and release time can be specified by (1-RT) represented in 16-bit 2's complement format.

$$\begin{aligned}
 xPeak(n) &= (1-AT) \times xPeak(n-1) + AT \times |x(n)| \\
 xPeak(n) &= (1-RT) \times xPeak(n-1)
 \end{aligned}$$

for

$$\begin{aligned}
 |x(n)| &> xPeak(n-1) \\
 |x(n)| &\leq xPeak(n-1)
 \end{aligned}$$

## Automatic Level Control (ALC)

The core of ALC gain control is depicted in Figure 15. The gain is checked and adjusted every ALC\_period, which is specified by UpDoubleTime and DnHalfTime registers. These two register bit fields have physical meaning which mapped to approximately ±6dB per second. They can be specified from 1/16 to 15.9375 seconds with resolution of 1/16s.

The internal logic implements ALC\_period by a counter expired every 16 \* UpDoubleTime or 16 \* DnHalfTime when the gain is going up/dn respectively. Depend on the clock base of I<sup>2</sup>S, the nominal of ±6dB per second for double/half the gain is actually approximately by :

$$\begin{aligned}
 44.1k &: 20 \times \log_{10}((4097/4096)^{(48000/16)}) = 6.36dB; \\
 &20 \times \log_{10}((4095/4096)^{(48000/16)}) = -6.36dB \\
 48k &: 20 \times \log_{10}((4097/4096)^{(44100/16)}) = 5.84dB; \\
 &20 \times \log_{10}((4095/4096)^{(44100/16)}) = -5.84dB
 \end{aligned}$$

### The Parameters for ALC Control :

sThresALC[7:0] : Threshold of signal, specified by 0 to 1. 1 corresponds to the maximum allowable signal specified by clipper module.

xThresALC[7:0] : Threshold of excursion, specified by 0 to 1. 1 corresponds to the maximum allowable excursion.

sThresALC and xThresALC are 8-bit unsigned number representing the value 1/128 to 1, 0x80 is normalized to 1.

UpDoubleTime[7:0] : gain double time = UpDoubleTime /16 (seconds)

DnHalfTime[7:0] : gain half time = DnHalfTime /16 (seconds)

InitUpDoubleTime[7:0] : gain double time used for signal just detected from silence mode.

UpDoubleTime, DnHalfTime, InitUpDoubleTime and InitDnHalfTime are unsigned 8-bit number representing the value 1/16 to 15.9375, 0x10 is normalized to 1.

ALCInitGain[2:0] : ALC initial gain when signal is detected from silence mode. 0 to 21dB, 3dB step.

ALCMaxGain[2:0] : ALC maximum allowable gain. 0 to 21dB, 3dB step.

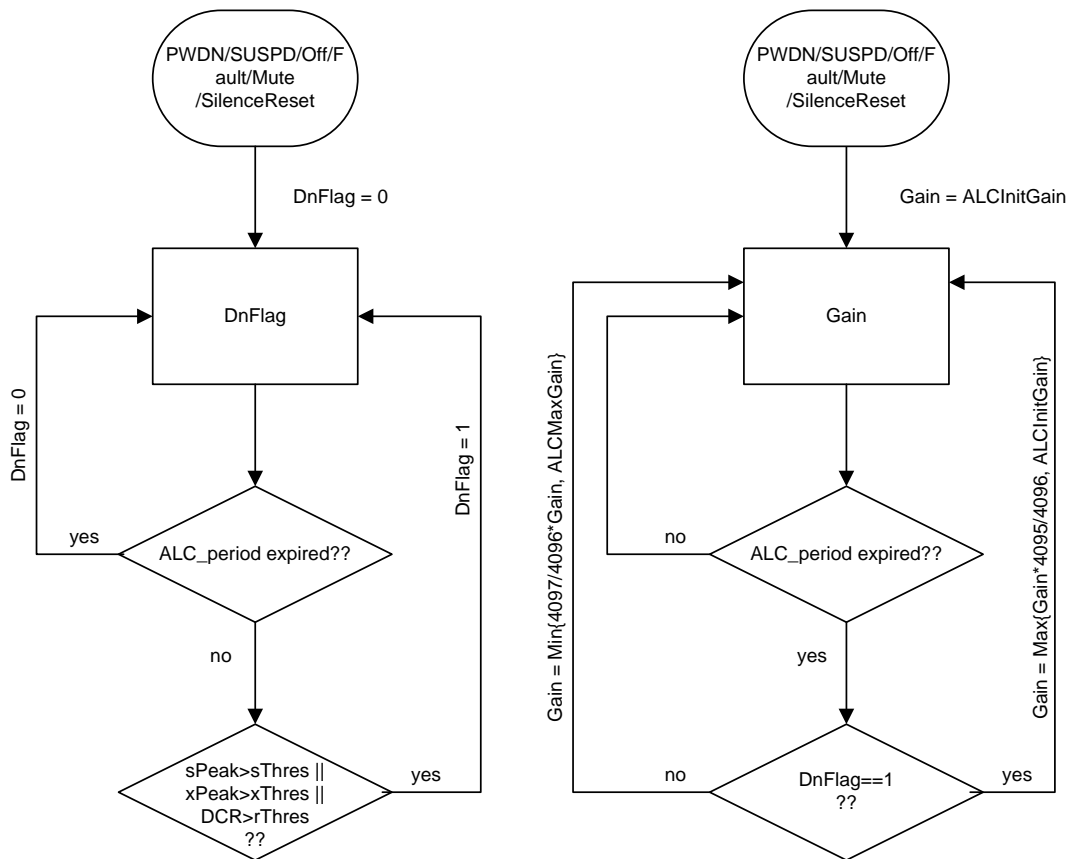


Figure 17. Gain Generation for ALC

**Gain Limiter**

The signal and excursion is limited to ensure the signal is not clipped, and the excursion never growth over the maximum allowable value.

The gain required to limit the signal and excursion are calculated by :

$$G_{Lmt} = \min \left\{ \frac{sThres}{sPeak}, \frac{xThres}{xPeak}, 1 \right\}$$

The parameters for Limiter control :

sThresLmt : Threshold of signal, specified by 0 to 1. 1 corresponds to the maximum allowable signal specified by clipper module.

xThresLmt : Threshold of excursion, specified by 0 to 1. 1 corresponds to the maximum allowable excursion.

xThresLmtDamage : Threshold of excursion when either resistance or excursion damage is detected.

**DC Resistance Control Loop**

**DC Resistance Measurement**

Metal coil resistance is highly linear dependent on the temperature, for example the scale factor is +0.393%/C for copper. The coil resistance is online monitored by the speaker protection algorithm. The update is disabled at PWDN/SUSPD/Off/Fault/Mute mode. A register bit can be set to define if the DC resistance is monitored or not in Silence mode.

The parameters for Coil Resistance :

- ▶ RNML : Nominal resistance of coil ( $\Omega$ )
- ▶ rApp : The application resistance between amplifier and the loudspeaker, normalized to RNML. The application resistance is assumed to be constant through all time.

PI Control Loop :

The parameters for PI-control loop :

- ▶ rMaxExcess : The maximum tolerable resistance growth ratio. 8-bit unsigned number representing the value 1/256 to 255/256
- ▶ PdictWeight : The weighting of prediction
- ▶ Kp : proportional gain of PI-controller
- ▶ KiKpRatio : ratio of Ki/Kp

This value of rMaxExcess should be set correctly considering the material dependent scale factor and the ambient temperature when the resistance calibration procedure is activated.

### Excursion Control Loop

#### Speaker (Impedance) Identification

IIR with 2<sup>nd</sup> to 5<sup>th</sup> order can be chosen in this implementation. 3<sup>rd</sup> order is generally sufficient for the mobile devices, and 5<sup>th</sup> order is reserved for the case when vented-box is implemented. The impedance coefficients update is disabled at PWDN/SUSPD/Off /Fault/Mute mode or when the input signal power is below the threshold of the signal detector (Silence mode).

The parameters for impedance identification

- ▶ SglEn : enable the adaptation in single-tone case
- ▶ SIBlocks : block size to average coefficient update vector
- ▶ SIOrd : order of IIR filter
- ▶ InitImpIDMu : step size to update coefficient in initial stage
- ▶ ImpIDMU : step size in normal stage

#### Excursion Prediction

The excursion is predicted by integrating the back emf, which is induced by the coil movement and direct proportional to its velocity scaled by the BI factor.

#### Resistance Calibration :

A measurement of resistance is activated by register control, after this procedure, the initial value of DCR is saved to One-Time-Program (OTP) memory.

The command/status for DC Resistance Calibration :

- ▶ DCRCalEn : Trigger the automatic DCR calibration procedure once
- ▶ InitDCR : Calibrated DC resistance value

#### BI Calibration

BI factor  $\phi(0)$  can be calibrated to check if the preset coefficient is adequate.

The command/status for BI Calibration :

- ▶ BICalEn : Trigger the automatic BI calibration procedure once
- ▶ InitBIFactor : Calibrated BI factor

#### Speaker Damage Detection

In two cases the loudspeaker is considered as damaged :

1. The DCR deviates for a scale above predefined value.
2. The Resonant deviates for a scale above or below predefined value.

The parameters for Damage detection :

- ▶ rMaxDamage : Threshold of resistor growth, specified by 0 to 1, represents the ratio with respect to the value of initial calibrated resistor. "0" is a special setting that disables this function.
- ▶ fScaleDamage : The boundary for resonant frequency drift vs. the preset resonant frequency. 0 to 1.
- ▶ fRes x fScaleDamage > fRes0 or fRes < fRes0 x fScaleDamage will trigger the damage event.
- ▶ DamgeRecoveryTime : The time (seconds) to recovery from damaged situations. "0" is a special setting that disables this function.

This value of rMaxDamage should be set correctly considering the material dependent scale factor and the ambient temperature when the resistance calibration procedure is activated.



**Volume Control**

The volume control can be set from -127.5dB to 0dB, with step = 0.5dB. The control timing is illustrated as in Figure 18. When a new gain is set by I<sup>2</sup>C, the hardware will change from the original setting in step of 0.5dB/ΔT, where ΔT is the step size with the following options :  
 ΔT = 4, 8, 16, 32, 64 samples, or ΔT = 0 stands for no

ramping up / down is applied.

When mute mode is set by I<sup>2</sup>C or detected by hardware, the volume setting is overruled, but the original gain setting is kept in hardware, allows to be recovered to the original state.

Volume control can be bypassed by register.

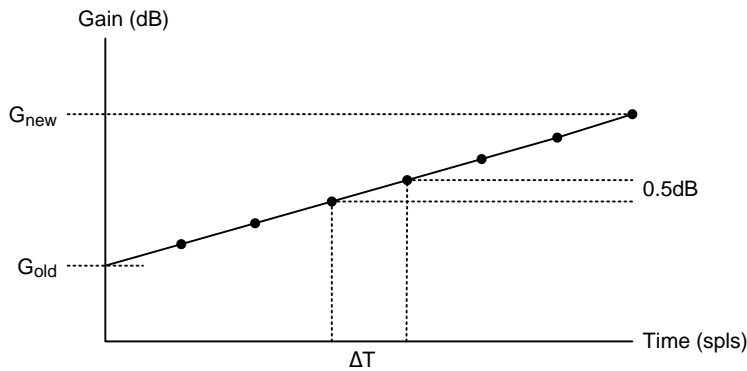


Figure 18. Volume Control Timing Graph

The threshold is normalized to 1 is passed to speaker protection which equals to :

$$\text{ClipThres (normalized)} = \frac{5 - (VBCPS - V_{BAT}) \times CPSLP}{5}$$

ClipThres (normalized) equals to 1 if signal is small and never reaches to the threshold. When signal is large and is clipped by this threshold, ClipThres (normalized) will be sent to speaker protection block.

If battery voltage returns to a hysteresis level, ClipThres will increase by a rate of CLIPRR to a certain level which is defined by VBCPS, CPSLP and VBAT. As ClipThres increases, speaker protection will also increase its gain to let the signal return to its original level. The battery voltage hysteresis can bet set via BVHYS at register 0x0B.

Boost Converter

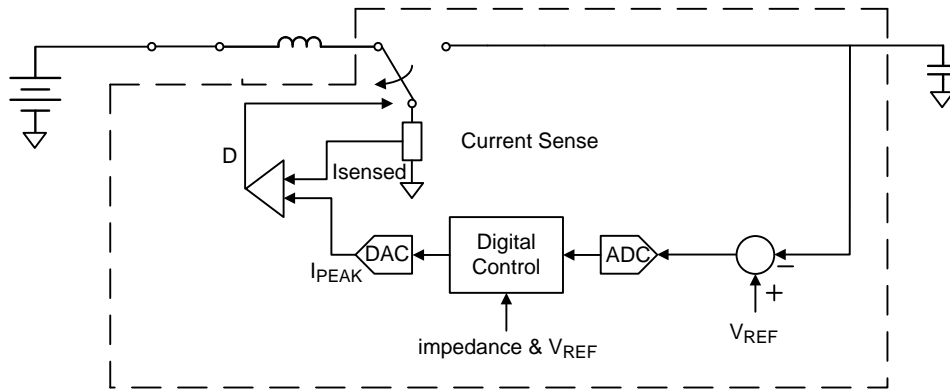


Figure 19. Boost Converter Schematic

A built-in boost converter is used to adjust class-D supply voltage. This converter could be operated in 4 different modes which are :

**Disable Mode**, in this case class-D is powered externally, boost converter is off.

**Battery Mode**,  $V_{BST} = V_{BAT}$ , boost converter is powered, but MOS is switched to OFF state at all times.

**Fixed Mode**,  $V_{BST} = V_{BSTPG}$ ,  $V_{BAT}$  is boosted to a certain value.

**Adaptive Mode**,  $V_{BST}$  depends on the level of signal  
The boost mode can be selected via  $BBMODE$  at register 0x14.

When boost converter is powered and in Boost/Adaptive mode, it tries to regulate the output voltage  $V_{BST}$  to a desired value. The switching frequency  $f_{sw}$  is 2.048MHz (for  $f_s = 8/12/16/24/32$  kHz)/1.8816MHz (for  $f_s = 11.025/22.05/44.1$ kHz).

The digital control logic inside this converter collects  $V_{REF}/load/V_o$  information and then output a  $I_{PEAK}$  value to general a proper D value which makes  $V_o$  equals  $V_{REF}$ . When in adaptive mode, boost converter can be used to generate required class-D power supply according to  $V_{BAT}$ ,  $TH1/TH2/TH3$ ,  $THT1/THT2/THT3$  and  $TOT$  where  $TH1/2/3$ ,  $THT1/2/3$  and  $TOT$  is at register 0x10 to 0x13. The detail function is shown below :

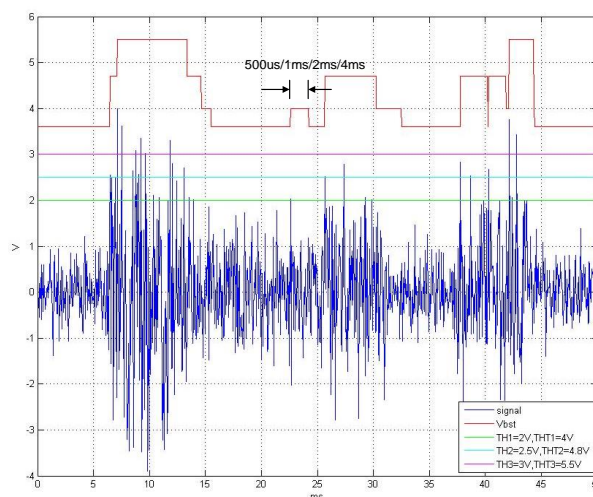


Figure 20. Illustration for Adaptive Boost Mode

TOT can be set to 500us/1ms/2ms/4ms :

```
if ( signal >= THx )
tot_cntx = 1;
elseif ( tot_cntx == TOT )
tot_cntx = 0;
elseif ( tot_cntx ~= 0 )
tot_cntx = tot_cntx+1;
else
tot_cntx = tot_cntx;           (x:1/2/3)
if ( tot_cnt3 > 0 )
vbst = THT3;
elseif ( tot_cnt2 > 0 )
vbst = THT2;
elseif ( tot_cnt1 > 0 )
vbst = THT1;
else
vbst = VBAT;
```

Register Definition

Address Mapping

Registers Description

| ADDR | Byte | Bits | R/W | Name             | Description  | Default   |
|------|------|------|-----|------------------|--|-----------|
| 0x00 | 1    | 7:0  | R   | CHIP_ID[7:0]     | Chip Revision ID   |           |
| 0x01 | 1    | 7    | R   | BCK_CLOCK_STABLE | BCK rate stable  | 1         |
|      |      | 6    | R   | PLL_LOCK         | PLL is locked to BCK or LRCK<br>0 : unlocked<br>1 : locked                                 | 0         |
|      |      | 5    | R   | BAT_UV           | Battery voltage under threshold<br>0 : normal<br>1 : under threshold                       | 0         |
|      |      | 4    | R   | AMP_OV           | Class-D amplifier supply voltage (VDDP) over threshold<br>0 : normal<br>1 : over threshold | 0         |
|      |      | 3    | R   | AMP_OC           | Class-D amplifier output current over threshold<br>0 : normal<br>1 : over threshold        | 0         |
|      |      | 2    | R   | AMP_OT           | Class-D amplifier temperature over threshold<br>0 : normal<br>1 : over threshold           | 0         |
|      |      | 1    | R   | BST_OC           | Boost converter current over threshold<br>0 : normal<br>1 : over threshold                 | 0         |
|      |      | 0    | R   | BST_OT           | Boost converter temperature over threshold<br>0 : normal<br>1 : over threshold             | 1         |
| 0x02 |      | 7:2  | R/W | AUD_WL           | Audio interface word length. Valid range : 16 bit – 32bit                                  | 6'b100100 |
|      |      | 1    | WC  | flagResDmg       | resistance exceeds the predefined value  | 1'b0      |
|      |      | 0    | WC  | flagFreqDmg      | resonant frequency out of range  | 1'b0      |

| ADDR | Byte | Bits | R/W | Name            | Description  | Default |
|------|------|------|-----|-----------------|--|---------|
| 0x03 | 1    | 7:6  |     | Reserved        |  |         |
|      |      | 5    | R/W | D_EN_TRIWAVE    | Enable triangle wave generator   | 0       |
|      |      | 4    | R/W | AMPDS           | Soft off mode enable<br>0 : Enter soft mode before off mode<br>1 : enter off mode directly   | 0       |
|      |      | 3    | R/W | AMPE            | Class D Enable<br>0 : disable Class D<br>1 : enable Class D  | 0       |
|      |      | 2    | R/W | SPKM            | Speaker protection mute<br>0 : disable speaker protection mute<br>1 : enable speaker protection mute   | 0       |
|      |      | 1    | R/W | SPKE            | Speaker protection block enable<br>0 : disable speaker protection<br>1 : enable speaker protection   | 0       |
|      |      | 0    | R/W | PWDN            | Chip power down control<br>0 : chip enable<br>1 : chip power down  | 1       |
| 0x04 | 1    | 7:6  |     | Reserved        |  |         |
|      |      | 4    | R/W | DSP_MODE_SEL    | 0 : DSP_MODE_A<br>1 : DSP_MODE_B   | 0       |
|      |      | 3:2  | R/W | AUD_FMT[1:0]    | 00 : I <sup>2</sup> S<br>01 : Left Justify<br>10 : Right Justify   | 2'b00   |
|      |      | 1:0  | R/W | AUD_BITS[1:0]   | 00 : 24 Bits<br>01 : 20 Bits<br>10 : 18 Bits<br>11 : 16 Bits   | 2'b00   |
| 0x05 | 1    | 7    | R   | BCK_VALID       | BCK stable and match with BCK_MODE setting   | 0       |
|      |      | 6    | R/W | BCK_MODE_DET_EN | Check BCK_VALID to enable audio path<br>0 : without check BCK_VALID<br>1 : check BCK_VALID   | 0       |
|      |      | 4:3  | R/W | BCK_MODE[1:0]   | BCK Mode Select<br>00 : 32fs<br>01 : 48fs<br>Others : 64fs   | 2'b10   |
|      |      | 2:0  | R/W | SR_MODE[1:0]    | Sampling Rate Select<br>000 : 8K<br>001 : 12K/11.025K<br>010 : 16K<br>011 : 24K/22.05K<br>100 : 32K<br>101 : 48K/44.1K<br>110 : 96K/88.2K<br>111 : 192K/176.4K | 3'b101  |

| ADDR | Byte | Bits | R/W | Name                 | Description  | Default |
|------|------|------|-----|----------------------|--|---------|
| 0x06 | 1    | 7:4  |     | Reserved             |  |         |
|      |      | 3:2  | R/W | I <sup>2</sup> SLRS  | Biquad input selection<br>00 : left channel<br>01 : (left+right) / 2<br>10 : right channel<br>11 : reversed  | 2'b01   |
|      |      | 1    | R/W | I <sup>2</sup> SCHS  | I <sup>2</sup> S interface DATAI3 channel selection<br>0 : from DATAI3 left channel<br>1 : from DATAI3 right channel   | 0       |
|      |      | 0    | R/W | I <sup>2</sup> SDIS  | I <sup>2</sup> S interface 1/2 selection<br>0 : from I <sup>2</sup> S interface 1<br>1 : from I <sup>2</sup> S interface 2   | 0       |
| 0x07 | 1    | 7:4  | R/W | I <sup>2</sup> SDORS | DATAO right channel output selection(DATA.R format: Q0.23)<br>0x0 : DATAI3 left = DATAO.R<br>0x1 : DATAI3 right = DATAO.R<br>0x2 : gain information = DATAO.R<br>0x3 : voltage output w/o pilot = DATAO.R*16<br>0x4 : voltage output w/l pilot = DATAO.R<br>0x5 : current sense result = DATAO.R<br>0x6 : (voltage output w/l pilot) * current sense = DATAO.R * 16<br>0x7 : FDRC_DATA_OUT = DATAO.R<br>0x8 : SPK_DATA_OUT = DATAO>R<br>0x9 : est. current (for excursion est.) = DATAO.R<br>0xa : estimated current error = DATAO.R<br>0xb : rx_pilot = DATAO.R<br>0xc : estimated excursion = DATAO.R * 16<br>0xd : estimated Resistor = DATAO.R * 16<br>0xe : input signal behind notch filters = DATAO.R<br>0xf : excursion peak = DATAO.R | 4'h5    |

| ADDR | Byte | Bits | R/W | Name                 | Description  | Default |
|------|------|------|-----|----------------------|--|---------|
| 0x07 | 1    | 3:0  | R/W | I <sup>2</sup> SDOLS | DATAO left channel output selection(DATA.L format: Q0.23)<br>0x0 : DATAI3 left = DATAO.L<br>0x1 : DATAI3 right = DATAO.L<br>0x2 : gain information = DATAO.L<br>0x3 : voltage output w/o pilot = DATAO.L*16<br>0x4 : voltage output w/l pilot = DATAO.L<br>0x5 : current sense result = DATAO.L<br>0x6 : (voltage output w/l pilot) * current sense = DATAO.L * 16<br>0x7 : EQ_DATA_OUT = DATAO.L<br>0x8 : DAC_DATA_IN = DATAO.L<br>0x9 : voltage input for excursion estimation = DATAO.L<br>0xa : est. current (for sys. identification) = DATAO.L<br>0xb : estimated velocity = DATAO.L * 16<br>0xc : digital maximum allowable absolute data = DATAO.L<br>0xd : side channel gain = DATAO.L<br>0xe : voltage from spkfb = DATAO.L<br>0xf : speaker protection input data = DATAO.L | 4'h4    |
| 0x08 | 1    | 7:3  |     | Reserved             |  |         |
|      |      | 2:1  | R/W | I <sup>2</sup> SDOS  | DATAO pass through selection<br>11 : DATAO is from DATAI1<br>10 : DATAO is from DATAI2<br>01 : DATAO is from DATAI3<br>00 : DATAO is from I <sup>2</sup> SDOR/L  | 2'b00   |
|      |      | 0    | R/W | I <sup>2</sup> SDOE  | DATAO output enable<br>0 : disable<br>1 : enable   | 0       |

| ADDR | Byte | Bits | R/W | Name      | Description  | Default |
|------|------|------|-----|-----------|--|---------|
| 0x09 | 1    | 7    | R/W | ORDER_DSP | 0 : EQ → BWE → DRC<br>1 : DRC → EQ → BWE   | 1       |
|      |      | 6    | R/W | STRSYNC   | Gain Synchronize in stereo mode<br>0 : Don't sync<br>1 : Sync to use minimum gain from two channels                                      | 0       |
|      |      | 5    | R/W | LMTEN     | Limiter Enable<br>0 : Disable<br>1 : Enable  | 0       |
|      |      | 4    | R/W | ALCEN     | ALC gain Control enable<br>0 : disable<br>1 : enable   | 0       |
|      |      | 3    | R/W | MBDRcen   | Multi-Band DRC Enable<br>0 : Disable<br>1 : Enable   | 0       |
|      |      | 2    | R/W | BWEEN     | LPF + BWE enable<br>0 : disable, output zero at lower branch<br>1 : enable   | 0       |
|      |      | 1    | R/W | HPFEN     | HPF enable<br>0 : Bypass at upper branch<br>1 : enable   | 0       |
|      |      | 0    | R/W | BQEN      | 10 Band BQ Enable<br>0 : Bypass 10 band BQ<br>1 : Enable 10 band BQ  | 0       |
| 0x10 | 1    | 7:3  |     | Reserved  |  | 0       |
|      |      | 2:0  | R/W | VBCPS     | Clip threshold setting<br>000 : 4.0V<br>001 : 3.75V<br>010 : 3.6V<br>011 : 3.45V<br>100 : 3.3V<br>101 : 3.15V<br>110 : 3V<br>111 : 2.85V | 0       |



| ADDR | Byte | Bits  | R/W | Name            | Description   | Default  |
|------|------|-------|-----|-----------------|---|----------|
| 0x11 | 1    | 7     | R/W | CLPE            | Clip enable   | 0        |
|      |      | 6     | R/W | Reserved        |   |          |
|      |      | 5:4   | R/W | BVHYS           | Battery voltage recovery hysteresis<br>00 : battery voltage + 0.05<br>01 : battery voltage + 0.1<br>10 : battery voltage + 0.15<br>11 : battery voltage + 0.2   | 2'b00    |
|      |      | 3:2   | R/W | CLIPRR          | Rate of V <sub>O</sub> threshold recover when VBAT return<br>00 : increase by 1/8 of original V <sub>O</sub> per 1s<br>01 : increase by 1/8 of original V <sub>O</sub> per 1.5s<br>10 : increase by 1/8 of original V <sub>O</sub> per 2s<br>11 : increase by 1/8 of original V <sub>O</sub> per 2.5s | 2'b00    |
|      |      | 1:0   | R/W | CLIPDR          | Rate of V <sub>O</sub> threshold drop when VBAT is low<br>00 : 1/16 of original per sample<br>01 : 1/8 of original V <sub>O</sub><br>10 : 1/4 of original V <sub>O</sub><br>11 : 1 step to target   | 2'b00    |
| 0x12 | 2    | 15:10 | R/W | Reserved        |   |          |
|      |      | 9:0   | R/W | CPSLP           | Clip slope setting :<br>For example 3V <sub>O</sub> / VBAT<br>CPSLP = 3 / DtoA GAIN (DAC + CLASS-D)   | 10'h000  |
| 0x13 | 2    | 15:0  | R/W | VOMIN           | Minimum Clip threshold converted from (V)<br>For example, minimum clip threshold is 2.5V, then<br>V <sub>O_MIN</sub> = 2.5V / DtoA GAIN (DAC + CLASS-D)<br>16'b0 : no minimum   | 16'h0000 |
| 0x14 | 2    | 15:0  | R/W | SIGMAX          | Digital maximum allowable absolute data:<br>SIG_MAX = max absolute voltage (V) / DtoA GAIN (DAC+CLASS-D)<br>This value should be less than 1  | 16'h4000 |
| 0x15 | 1    | 7     | R/W | D_ADC_BUF_EN    | IMADC VREF BUF enable   | 0        |
|      |      | 6     | R/W | D_BYPASS_OCP_EN | Boost bypass mode OCP enable  | 0        |
|      |      | 5     | R/W | D_PREDRV_EN     | Boost predriver enable  | 0        |
|      |      | 4     | R/W | D_ISENSE_EN     | Boost current sense enable  | 0        |
|      |      | 3     | R/W | D_CMPPWM_EN     | Boost comparator enable   | 0        |

| ADDR | Byte | Bits | R/W | Name             | Description  | Default   |
|------|------|------|-----|------------------|--|-----------|
| 0x1B | 1    | 7:0  | R/W | VBAT_GAIN        | Mapping VBAT 1LSB to real value (1LSB = 1/1024V) :<br>Ex. VBAT 1LSB = 5mV<br>VBAT_GAIN = 0.005/(1/1024) * 32 =                       | (MTP)     |
| 0x1E | 1    | 1:0  | R/W | BST_MODE         | Boost mode :<br>00 : disable<br>01 : battery<br>10 : fixed<br>11 : adaptive  | 2'b00     |
| 0x1F | 1    | 11:6 | R/W | BST_THT1         | 000000 : disabled<br>000001 to 100001 : 2.9 +<br>BST_THT1 * 0.2V<br>e.g. 000001 : 3.1V, 100001 = 9.5V<br>100010 to 111111 : Reserved | 6'b000000 |
|      |      | 5:0  | R/W | BST_TH1          | 000000 : disabled<br>000001 to 100001 : 1.3 +<br>BST_THT1 * 0.2V<br>e.g. 000001 : 1.5V, 100001 = 7.9V<br>100010 to 111111 : Reserved | 6'b000000 |
| 0x20 | 1    | 11:6 | R/W | BST_THT2         | same defination as BST_THT1  | 6'b000000 |
|      |      | 5:0  | R/W | BST_TH2          | same defination as BST_TH1   | 6'b000000 |
| 0x21 | 1    | 11:6 | R/W | BST_THT3         | same defination as BST_THT1  | 6'b000000 |
|      |      | 5:0  | R/W | BST_TH3          | same defination as BST_TH1   | 6'b000000 |
| 0x22 | 1    | 7    | R/W | EN_AMP_OCP_LATCH | 1: enable amplifier OCP latch  | 0         |
|      |      | 3:2  | R/W | SLEW_RATE        | VBST slew rate when using<br>adaptive mode :<br>00 : 2.5mV/μs<br>01 : 5mV/μs<br>10 : 10mV/μs<br>11 : 20mV/μs                         | 2'b01     |
|      |      | 1:0  | R/W | BST_TOT          | Level timeout time :<br>00 : 500μs<br>01 : 1ms<br>10 : 2ms<br>11 : 4ms   | 2'b01     |
| 0x23 | 1    | 7:0  | R/W | SIG_GAIN         | Signal path gain :<br>SIG_GAIN = DA gain * other analog<br>gain * 10   | 8'h69     |
| 0x24 | 1    | 5    | R/W | DCM_EN           | DCM enable :<br>0 : disable<br>1 : enable  | 1         |
|      |      | 4    | R/W | PSM_EN           | PSM enable :<br>0 : disable<br>1 : enable  | 1         |

| ADDR | Byte | Bits  | R/W | Name            | Description   | Default   |
|------|------|-------|-----|-----------------|---|-----------|
| 0x25 | 1    | 7:6   | R/W | Reserved        |   |           |
|      |      | 5:0   | R/W | PSM_THR1        | PSM IPEAK value setting :<br>When 6-bit IDAC1 < PSM_THR1,<br>PSM mode is enabled if PSM_EN<br>and DCM_EN is on. The actual<br>IPEAK is calculated as following:<br>IPEAK to (IDAC1(6-bit) * 0.625e-3<br>*12.2 * 50 /6.1) – (slope_comp *<br>(1-VBAT * effi / VBST)) | 6'b000000 |
| 0x26 | 1    | 7:4   | R/W |                 |   |           |
|      |      | 3     | R   | OC_EV           | OC event happens  |           |
|      |      | 2     | R   | OT_EV           | OT event happens  |           |
|      |      | 1     | R/W | OCP_EN          | Over-current protection enable :<br>0 : disable<br>1 : enable   | 1         |
| 0x2B | 1    | 7     | R/W | Reserved        |   |           |
|      |      | 6:0   | R/W | CC_MAX          | IDAC1 peak value  | 6'b000000 |
| 0x2C | 1    | 7     | R/W | Reserved        |   |           |
|      |      | 6:0   | R/W | OCP_CURR        | IDAC1 6-bit ocp enable level  | 6'b0      |
| 0x2D | 2    | 15:12 |     | Reversed        |   |           |
|      |      | 11    | RC  | INT_LEAK_SPK    | Speaker air leak interrupt  | 0         |
|      |      | 10    | R   | INT_flagResDmg  | Similar as 0x02 flagResDmg, but<br>this bit CAN'T be cleared by read,<br>and only can be clear by write 0 to<br>corresponding bit in register 0x02  | 0         |
|      |      | 9     | R   | INT_flagFreqDmg | Similar as 0x02 flagFreqDmg, but<br>this bit CAN'T be cleared by read,<br>and only can be clear by write 0 to<br>corresponding bit in register 0x02h  | 0         |
|      |      | 8     | RC  | INT_STB_BCK     | BCK stable interrupt  | 0         |
|      |      | 7     | RC  | INT_LCK_PLL     | PLL lock interrupt  | 0         |
|      |      | 6     | RC  | INT_OC_BST_P    | Predicted boost converter<br>over-current interrupt   | 0         |
|      |      | 5     | RC  | INT_UV_VBAT     | VBAT under-voltage interrupt  | 0         |
|      |      | 4     | RC  | INT_OV_PVDD     | PVDD over-voltage interrupt   | 0         |
|      |      | 3     | RC  | INT_OC_AMP_P    | Amplifier PMOS over-current<br>interrupt  | 0         |
|      |      | 2     | RC  | INT_OC_AMP_N    | Amplifier NMOS over-current<br>interrupt  | 0         |
|      |      | 1     | RC  | INT_OC_BST      | Boost converter over-current<br>interrupt   | 0         |
|      |      | 0     | RC  | INT_OT          | Boost temperature interrupt   | 0         |

| ADDR | Byte | Bits  | R/W | Name             | Description  | Default |
|------|------|-------|-----|------------------|--|---------|
| 0x2E | 2    | 15:12 |     | Reserved         |  |         |
|      |      | 11    | R/W | MSK_INT_LEAK_SPK | Speaker air leak interrupt                               | 0       |
|      |      | 10    | R/W | MSK_flagResDmg   | Speaker's resistance out of range interrupt mask         | 0       |
|      |      | 9     | R/W | MSK_flagFreqDmg  | Speaker's resonant frequency out of range interrupt mask | 0       |
|      |      | 8     | R/W | MSK_INT_STB_BCK  | BCK stable interrupt mask                                | 0       |
|      |      | 7     | R/W | MSK_INT_LCK_PLL  | PLL lock interrupt mask                                  | 0       |
|      |      | 6     | R/W | MSK_INT_OC_BST_P | Predicted boost converter over-current interrupt mask    | 1       |
|      |      | 5     | R/W | MSK_INT_UV_VBAT  | VBAT under-voltage interrupt mask                        | 1       |
|      |      | 4     | R/W | MSK_INT_OC_PVDD  | PVDD over-voltage interrupt mask                         | 1       |
|      |      | 3     | R/W | MSK_INT_OC_AMP_P | Amplifier PMOS over-current interrupt mask               | 1       |
|      |      | 2     | R/W | MSK_INT_OC_AMP_N | Amplifier NMOS over-current interrupt mask               | 1       |
|      |      | 1     | R/W | MSK_INT_OC_BST   | Boost converter over-current interrupt mask              | 1       |
|      |      | 0     | R/W | MSK_INT_OT       | Over-temperature interrupt mask                          | 1       |

| ADDR | Byte | Bits  | R/W | Name              | Description   | Default  |
|------|------|-------|-----|-------------------|---|----------|
| 0X2F | 2    | 15:12 |     | Reserved          |   |          |
|      |      | 11:10 | R/W | T_DG_INT_UV_VBAT  | INT_UV_VBAT deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch  | 2'b01    |
|      |      | 9:8   | R/W | T_DG_INT_OV_PVDD  | INT_OV_PVDD deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch  | 2'b01    |
|      |      | 7:6   | R/W | T_DG_INT_OC_AMP_P | INT_OC_AMP_N deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch | 2'b00    |
|      |      | 5:4   | R/W | T_DG_INT_OC_AMP_N | INT_OC_AMP_N deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch | 2'b00    |
|      |      | 3:2   | R/W | T_DG_INT_OC_BST   | INT_OC_BST deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch   | 2'b00    |
|      |      | 1:0   | R/W | T_DG_INT_OT       | INT_OT deglitch time<br>00 : no deglitch<br>01 : 40ns deglitch<br>10 : 81ns deglitch<br>11 : 122ns deglitch       | 2'b00    |
| 0x30 | 1    | 7:4   | R/W | SilenceRestTime   | Silence reset time :<br>0 to 15 seconds   | 4'b0001  |
|      |      | 3:0   | R/W | sThresAct         | Signal Active threshold :<br>0 to -90dB (sThresAct * -6dB)  | 4'b1010  |
| 0x32 | 2    | 15:14 |     | Reserved          |   |          |
|      |      | 13:9  | R/W | delayGain[4:0]    | The gain delay which is used to synchronize left channel and right channel  | 5'h00    |
|      |      | 8:0   | R/W | tDelay            | Look-ahead delay samples<br>The behavior is undefined if tDelay = 0   | 9'h64    |
| 0x33 | 1    | 7:2   |     | Reserved          |   |          |
|      |      | 1:0   | R/W | tAttackSel        | Attack Time Selection :<br>00 : 0ms<br>01 : 0.1ms<br>10 : 0.2ms<br>11 : 0.3ms                                     | 2'b10    |
| 0x34 | 2    | 15:0  | R/W | tRelease          | Release Time constant (1-RT)  | 16'h7fce |

| ADDR | Byte | Bits | R/W | Name             | Description   | Default  |
|------|------|------|-----|------------------|---|----------|
| 0x35 | 2    | 15:0 | R/W | tHoldRelease     | Hold Release Time constant<br>(1-RT) <sup>t</sup> Delay   | 16'h6dd3 |
| 0x38 | 1    | 7:0  | R/W | sThresLmt        | Signal threshold for gain limiter<br>1/128 to 1, 0x80 normalized to 1                                       | 8'h80    |
| 0x39 | 1    | 7:0  | R/W | xThresLmt        | Excursion threshold for gain limiter<br>1/128 to 1, 0x80 normalized to 1                                    | 8'h80    |
| 0x3A | 1    | 7:0  | R/W | sThresALC        | Signal threshold for automatic gain<br>controller<br>1/128 to 1, 0x80 normalized to 1                       | 8'h40    |
| 0x3B | 1    | 7:0  | R/W | xThresALC        | Excursion threshold for automatic<br>gain controller<br>1/128 to 1, 0x80 normalized to 1                    | 8'h40    |
| 0x3C | 1    | 7:0  | R/W | InitUpDoubleTime | Gain up double time for initial active<br>1/16 to 15.9375, 0x10 normalized to<br>1                          | 8'h04    |
| 0x3D | 1    | 7:0  | R/W | UpDoubleTime     | Gain up double time<br>1/16 to 15.9375, 0x10 normalized to<br>1   | 8'h10    |
| 0x3E | 1    | 7:0  | R/W | DnHalfTime       | Gain down half time<br>1/16 to 15.9375, 0x10 normalized to<br>1   | 8'h40    |
| 0x3F | 1    | 7:4  | R/W | ALCMaxGain       | ALC maximum gain<br>-24 to 21dB (ALCMaxGain * 3dB)  | 4'b0111  |
|      |      | 3:0  | R/W | ALCInitGain      | ALC initial gain<br>-24 to 21dB (ALCInitGain * 3dB)   | 4'b0000  |
| 0x41 | 1    | 7:0  | R/W | InitImpIDMu      | Initial adaptation step size<br>1/128 to 255/128  | 8'h04    |
| 0x42 | 1    | 7:0  | R/W | ImpIDMu          | Normal adaptation step size<br>1/2048 to 255/2048   | 8'h02    |
| 0x43 | 1    | 7:0  | R/W | gPilot           | Gain of pilot (in digital domain)<br>1/4096 to 255/4096 (gPilot*1/16);<br>gPilot = 1/256 to 255/256         | 8'h11    |
| 0x44 | 1    | 7:2  | R/W | TRXdelay[5:0]    |   | 0        |
|      |      | 1    | R/W | sIPilotEN        | Pilot enable in silence mode  | 0        |
|      |      | 0    | R/W | PilotEN          | Pilot enable  | 0        |
| 0x45 | 1    | 7    | R/W | Reserved         |   |          |
|      |      | 6:4  | R/W | PilotScale       | Scale-up factor = 2 <sup>PilotScale</sup><br>to scale up the output of HPF to<br>extract the pilot          | 0        |
|      |      | 3    | R/W | iSenseInv        | inverse the sign of the current<br>sensing data   | 0        |
|      |      | 2:0  | R/W | iSenseScale      | Scale-up factor = 2 <sup>iSenseScale</sup><br>to let CRx/CTx in the range of [1, 2)<br>at calibration phase | 0        |

| ADDR | Byte | Bits  | R/W | Name            | Description   | Default  |
|------|------|-------|-----|-----------------|---|----------|
| 0x46 | 3    | 23:0  | R/W | iSenseGain      | Gain of current sense loop, normalized to 32Ω<br>Read/Write to OTP if SenseGPGMEN = 1<br>Read/Write to local register if SenseGPGMEN = 0    | (MTP)    |
| 0x47 | 3    | 23:0  | R/W | Rapp            | Application resistance, normalized to 32Ω   | 0        |
| 0x48 | 1    | 7:0   | R/W | rMaxExcess      | Maximum allowable DCR growth ratio<br>1/256 to 255/256  | 0        |
| 0x49 | 2    | 15:11 | R/W | Reserved        |   |          |
|      |      | 10:8  | R/W | PdictWeightExp  | PdictWeight = PdictWeightMant * 2^PdictWeightExp<br>PdictWeightExp = 0 to 7   | 3'h7     |
|      |      | 7:0   | R/W | PdictWeightMant | 1/128 to 255/128, 0x80 normalized to 1  | 8'h80    |
| 0x4A | 2    | 15:10 | R/W | Reserved        |   |          |
|      |      | 9:8   | R/W | KpExp           | Kp = KpMant * 2^KpExp<br>KpExp = 0 to 3   | 2'h3     |
|      |      | 7:0   | R/W | KpMant          | 1/128 to 255/128, 0x80 normalized to 1  | 8'h80    |
| 0x4B | 1    | 7:0   | R/W | KiKpRatio       | The ratio of Ki/Kp<br>1/256 to 255/256  | 8'h3     |
| 0x4C | 1    | 7:0   | R/W | InitDCRIDMu     | Initial adaptation step size<br>1/256 to 255/256  | 8'h40    |
| 0x4D | 1    | 7:0   | R/W | DCRIDMu         | Normal adaptation step size<br>1/1024 to 255/1024   | 8'h04    |
| 0x4E | 3    | 23:0  | R/W | CalibDCR        | Factory calibrated DC resistor<br>Read/Write to OTP if DCRPGEN = 1<br>Read/Write to local register if DCRPGEN = 0                           | (MTP)    |
| 0x4F | 2    | 15:0  | R/W | CalibBL         | Factory calibrated BL factor<br>Read/Write to OTP if BLPGEN = 1<br>Read/Write to local register if BLPGEN = 0<br>CalibBL = reg[0x4f] / 2^15 | (MTP)    |
| 0x50 | 1    | 7     | R/W | CalibEn         | Trigger the calibration to start; self-cleared  | 0        |
|      |      | 0     | R   | CalibRDY        | The calibration output is ready for software reading  | 0        |
| 0x51 | 2    | 15:0  | R/W | CalibReq        | Calibration frequency = round (2 * f_Hz / fs * 65536); fs = 48000   | 16'h0000 |
| 0x52 | 2    | 15:0  | R/W | GalibGain       | Gain of the signal, ranged in [0,1), bit[15] is sign-bit and should be 0 for positive value   | 16'h0000 |

| ADDR | Byte | Bits | R/W | Name            | Description  | Default |
|------|------|------|-----|-----------------|--|---------|
| 0x53 | 4    | 31:0 | R   | CalibOut0       | Output #1 of calibration data  |         |
| 0x54 | 4    | 31:0 | R   | CalibOut1       | Output #2 of calibration data  |         |
| 0x55 | 1    | 7:0  | R/W | xThresLmtDamage | Excursion threshold for gain limiter when damage mode is detected<br>1/128 to 1, 0x80 normalized to 1  | 8'h1a   |
| 0x56 | 1    | 7:0  | R/W | rMaxDamage      | Maximum allowable DCR growth ratio to regard coil as damaged<br>1/256 to 255/256   | 8'hcd   |
| 0x57 | 1    | 7:0  | R/W | fScaleDamage    | If the value of SetResFreq/GetResFreq or GetResFreq/SetResFreq is less than this factor, then the diaphragm is regarded as damaged<br>fScaleDamage represents : 1/256 to 255/256   | 8'h80   |
| 0x58 | 1    | 7:4  | R/W | Reserved        |  |         |
|      |      | 3:0  | R/W | RecoveryTime    | The time to exit the damage mode after the RMAXDMGE or FSCALDMGE criteria is no longer violated.<br>Range for 0 to 15s   | 0       |
| 0x59 | 2    | 15:0 | R/W | SetResFreq      | Preset resonant frequency for damage detection<br>SetResFreq = round (2 * fres / fs * 65536); fs = 48000   | 16'h889 |
| 0x5A | 2    | 15:0 | R   | GetResFreq      | Estimated resonant frequency<br>fres (Hz) = GetResFreq / 65536 * fs / 2  |         |
| 0x5B | 1    | 2:0  | R/W | VOLCTRL         | Ramp control when new volume setting is different from old setting :<br>000 : no ramp up/down<br>001 : 0.5dB per 4 samples<br>010 : 0.5dB per 8 samples<br>011 : 0.5dB per 16 samples<br>100 : 0.5dB per 32 samples<br>101 : 0.5dB per 64 samples<br>others : reserved | 0       |
| 0x5C | 1    | 7:0  | R/W | VOLUME          | Volume, downward<br>0 to -127.5dB in -0.5dB step   | 0       |
| 0x5D | 4    | 31:0 | R   | CalibOutX       | Output #2 of calibration X data  |         |
| 0x5E | 4    | 31:0 | R   | CalibOutY       | Output #2 of calibration Y data  |         |



| ADDR | Byte | Bits    | R/W | Name          | Description  | Default      |
|------|------|---------|-----|---------------|--|--------------|
| 0x5F | 4    | 6:5     | R/W | DRC_CUT_LEAKY | 00 : 0dB<br>01 : -3dB<br>10 : -6dB<br>11 : -9dB                              | 2'b00        |
|      |      | 4       | R/W | EN_LMT_LEAK   | 0 : disable<br>1 : let xThresLmtDamage to take effect                        | 0            |
|      |      | 3:0     | R/W | REG_LEAK_THR  | Threshold to set the flag of leaky speaker<br>Threshold = REG_LEAK_THR / 128 | 4'b0000      |
| 0x60 | 20   | 159:128 | R/W | bq_1_b0       | u[31:26], b0[25:0]   | 32'h00000000 |
|      |      | 127:96  | R/W | bq_1_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_1_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_1_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_1_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0x61 | 20   | 159:128 | R/W | bq_2_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_2_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_2_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_2_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_2_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0x62 | 20   | 159:128 | R/W | bq_3_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_3_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_3_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_3_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_3_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0x63 | 20   | 159:128 | R/W | bq_4_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_4_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_4_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_4_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_4_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0x64 | 20   | 159:128 | R/W | bq_5_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_5_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_5_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_5_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_5_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0x65 | 20   | 159:128 | R/W | bq_6_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_6_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_6_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_6_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_6_a2       | u[31:26], a2[25:0]   | 32'h00000000 |

| ADDR | Byte | Bits    | R/W | Name       | Description        | Default      |
|------|------|---------|-----|------------|--------------------|--------------|
| 0x66 | 20   | 159:128 | R/W | bq_7_b0    | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_7_b1    | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_7_b2    | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_7_a1    | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_7_a2    | u[31:26], a2[25:0] | 32'h00000000 |
| 0x67 | 20   | 159:128 | R/W | bq_8_b0    | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_8_b1    | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_8_b2    | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_8_a1    | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_8_a2    | u[31:26], a2[25:0] | 32'h00000000 |
| 0x68 | 20   | 159:128 | R/W | bq_9_b0    | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_9_b1    | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_9_b2    | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_9_a1    | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_9_a2    | u[31:26], a2[25:0] | 32'h00000000 |
| 0x69 | 20   | 159:128 | R/W | bq_10_b0   | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_10_b1   | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_10_b2   | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_10_a1   | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_10_a2   | u[31:26], a2[25:0] | 32'h00000000 |
| 0x6A | 20   | 159:128 | R/W | VB_bq_1_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_1_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_1_b1 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_1_b1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_1_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0x6B | 20   | 159:128 | R/W | VB_bq_2_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_2_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_2_b1 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_2_b1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_2_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0x6C | 20   | 159:128 | R/W | VB_bq_3_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_3_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_3_b1 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_3_b1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_3_a2 | u[31:26], a2[25:0] | 32'h00000000 |

| ADDR | Byte | Bits    | R/W | Name            | Description           | Default      |
|------|------|---------|-----|-----------------|-----------------------|--------------|
| 0x6D | 20   | 159:128 | R/W | VB_bq_4_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_4_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_4_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_4_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_4_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x6E | 20   | 159:128 | R/W | VB_bq_5_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_5_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_5_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_5_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_5_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x6F | 20   | 159:128 | R/W | VB_bq_6_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_6_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_6_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_6_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_6_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x70 | 20   | 159:128 | R/W | VB_bq_7_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_7_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_7_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_7_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_7_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x71 | 20   | 159:128 | R/W | VB_bq_8_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_8_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_8_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_8_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_8_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x72 | 20   | 159:128 | R/W | VB_bq_9_b0      | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 127:96  | R/W | VB_bq_9_b1      | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_bq_9_b1      | u[31:26], b2[25:0]    | 32'h00000000 |
|      |      | 63:32   | R/W | VB_bq_9_b1      | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_bq_9_a2      | u[31:26], a2[25:0]    | 32'h00000000 |
| 0x73 | 24   | 191:160 | R/W | VB_fcn_a0       | u[31:26], a0[25:0]    | 32'h00800000 |
|      |      | 159:128 | R/W | VB_fcn_a1       | u[31:26], a1[25:0]    | 32'h00000000 |
|      |      | 127:96  | R/W | VB_fcn_a2       | u[31:26], a2[25:0]    | 32'h00000000 |
|      |      | 95:64   | R/W | VB_fcn_b0       | u[31:26], b0[25:0]    | 32'h00800000 |
|      |      | 63:32   | R/W | VB_fcn_b1       | u[31:26], b1[25:0]    | 32'h00000000 |
|      |      | 31:0    | R/W | VB_fcn_b2       | u[31:26], b2[25:0]    | 32'h00000000 |
| 0x75 | 4    | 31:0    | R/W | VB_GAIN_2[25:0] | u[31:26], gain1[25:0] | 32'h00800000 |
| 0x76 | 4    | 31:0    | R/W | VB_GAIN_3[25:0] | u[31:26], gain1[25:0] | 32'h00800000 |

| ADDR | Byte | Bits | R/W | Name                   | Description  | Default      |
|------|------|------|-----|------------------------|--|--------------|
| 0x77 | 4    | 31:0 | R/W | VB_GAIN_4[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x78 | 4    | 31:0 | R/W | VB_GAIN_5[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x79 | 4    | 31:0 | R/W | VB_GAIN_6[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x7A | 4    | 31:0 | R/W | VB_GAIN_7[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x7B | 4    | 31:0 | R/W | VB_GAIN_8[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x7C | 4    | 31:0 | R/W | VB_GAIN_9[25:0]        | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x7D | 4    | 31:0 | R/W | VB_GAIN_10[25:0]       | u[31:26], gain1[25:0]  | 32'h00800000 |
| 0x7E | 1    | 7    | R/W | PALPF4EN               | 2 <sup>nd</sup> Biquad enable  | 0            |
|      |      | 6    |     | Reversed               |  |              |
|      |      | 5:4  | R/W | CONSTANT [1:0]         |  | 2'b00        |
|      |      | 3:0  | R/W | SLOP [3:0]             |  | 4'b0000      |
| 0x7F | 1    | 7:0  | R/W | BW_COEFF[7:0]          | Default : 0dB, 0.5dB per steps<br>Increase setting will decrease output gain<br>Decrease setting will increase                               | 8'h30        |
| 0x80 | 1    | 7    | R/W | SW_RESET               | 1 : Software Reset   | 0            |
|      |      | 0    |     | Reserved               |  | 0            |
| 0x81 | 1    | 7:5  |     | D_SPK_BOOST[2:0]       | Class D gain control [000:110] = 0 to 15db/3db   | 3'b100       |
|      |      | 4:0  |     | D_SPKLPF_VOL[4:0]      | PGA Feedback Gain control RF [0000 to 1111] = -31db to 0db/1db   | 4'b10111     |
| 0x82 | 1    | 1:0  | R/W | D_PGA_SPKPGA_VOL [1:0] | PGA Input Gain control 00 = -6dB<br>01 = -3dB 10 = 0dB 11 = 3dB  | 2'b10        |
| 0x86 | 1    | 7    | R/W | D_VMID_EN              | VMID enable (AVDD/2)   | 0            |
|      |      | 6    | R/W | D_VMID_FAST            | VMID quick charge  | 0            |
| 0x88 | 1    | 7    | R/W | D_CS_EN                | Current sense enable   | 0            |
| 0x8B | 2    | 15:0 | R/W | vbat_data[15:0]        | Read mode : read vbat_data value from vbt_sens<br>Write mode : when 0xC8 vbat_data_tst_en is set to 1, vbat_data is from this register       | 16'h0000     |
| 0x8C | 2    | 15:0 | R/W | vtherm_data[15:0]      | read mode : read vtherm_data value from vbt_sens<br>write mode : when 0xC8 vtherm_data_tst_en is set to 1, vtherm_data is from this register | 16'h0000     |

| ADDR | Byte | Bits | R/W | Name                    | Description   | Default |
|------|------|------|-----|-------------------------|---|---------|
| 0x8D | 1    | 5    | R/W | vbt_sense_auto_en       | Battery/Temperature auto sense enable :<br>1 : enable battery/temperature auto sense<br>0 : disable   | 0       |
|      |      | 4:2  | R/W | vbt_sense_time_sel[2:0] | Battery/Temperature sense period :<br>000 : sense every 16ms<br>001 : sense every 32ms<br>010 : sense every 64ms<br>011 : sense every 128ms<br>100 : sense every 256ms<br>101 : sense every 512ms<br>110 : sense every 1024ms<br>111 : sense every 2048ms | 3'b000  |
|      |      | 1:0  | R/W | vbt_sense_clk_sel[1:0]  | Battery/Temperature sense ADC clock frequency selection :<br>00 : 384KHz<br>01 : 192KHz<br>10 : 96KHz<br>11 : 48KHz   | 2'b00   |
| 0x96 | 1    | 7    | R/W | ovp_prot_en             | OVP protection enable :<br>1 : enable ovp protection<br>0 : disable   | 0       |
|      |      | 6    | R/W | uvp_prot_en             | UVP protection enable :<br>1 : enable uvp protection<br>0 : disable   | 0       |
|      |      | 5    | R/W | cd_ocp_prot_en          | Class-D OCP protection enable :<br>1 : enable Class-D OCP protection<br>0 : disable   | 0       |
| 0x97 | 1    | 0    | R/W | PLL_FREERUN             | 1 : PLL free run mode   | 1       |
| 0x99 | 1    | 3:2  | R/W | PLL_CKSEL[1:0]          | Select the output to PLL_CKOUT pin(debug & meas.)<br>2'b00 -> CKOUT (24.576M, 22.5792M)<br>2'b01 -> CKOUT/2 (24.576M/2, 22.5792M/2)<br>2'b10 -> PLL_CKOUT = FREF<br>2'b11 -> PLL_CKOUT = FREF (reserved)  | 0       |
|      |      | 1:0  | R/W | PLL_RDYSEL[1:0]         | PLL/FLL output ready<br>2'b00 -> PLL_RDY = CLK_RDY<br>2'b01 -> PLL_RDY = (preserved)<br>2'b10 -> PLL_RDY = SHIFTGAIN_RDY<br>2'b11 -> PLL_RDY = SHIFTGAIN_RDY (preserved)  | 0       |

| ADDR | Byte | Bits  | R/W | Name                          | Description   | Default  |
|------|------|-------|-----|-------------------------------|---|----------|
| 0x9A | 1    | 5:4   | R/W | PLL_BW_RATIO                  | Kp / Ki ratio :<br>2'b00 -> Kp = 1; Ki = 1/8<br>2'b01 -> Kp = 1; Ki = 1/16<br>2'b10 -> Kp = 1; Ki = 1/32<br>2'b11 -> Kp = 1; Ki = 1/64  | 2'b01    |
|      |      | 3     | R/W | PLL_DZONE_MODE                | dead-zone mode :<br>1 : accumlate Kp path, larger BW.<br>0 : skip Ki path, smaller BW.  | 1        |
|      |      | 2     | R/W | PLL_NDSM_MODE                 | DSM order for fractional-N mode<br>0 : 1 <sup>st</sup> order<br>1 : 2 <sup>nd</sup> order   | 1        |
|      |      | 1:0   | R/W | PLL_REF_DIV[1:0]              | Input reference frequency divided ratio<br>2'b00 -> FREF<br>2'b01 -> FREF/2<br>2'b10 -> FREF/4<br>2'b11 -> FREF/8   | 2'b00    |
| 0x9B | 1    | 5     | R   | CK_CMPOUT_IDAC2               | Boost voltage loop comparator output  |          |
|      |      | 4     | R   | CK_ISENSE_FLAG                | Boost current loop comparator output  |          |
|      |      | 3:1   | R   | LOCK_DET[2:0]                 | The value of phase error (log scale)  |          |
|      |      | 0     | R   | PLL_RDY                       | PLL is ready.<br>Its source is based on PLL_RDYSEL[1:0]   |          |
| 0x9C | 4    | 31:29 |     | Reserved                      |   |          |
|      |      | 28:16 | R/W | PLL_N_I                       | PLL frequency disivor, integer part. {PLL_N_I, PLL_N_F} is a unsigned number in u13.16 format, which specifies the ratio of nominal system clock ( ~ 24MHz) over reference clock frequency. | 13'h0008 |
|      |      | 15:0  | R/W | PLL_N_F                       | PLL frequency disivor, fractional part.   | 16'h0000 |
| 0x9F | 1    | 6     | R/W | I <sup>2</sup> S_LOSS_DET_EN  | 1 : Enable LRCK/BCK loss check  | 0        |
|      |      | 5     | R/W | I <sup>2</sup> C_TIME_OUT_SEL | 1 : Reset Chip if I <sup>2</sup> C timeout and check function enable  | 0        |
|      |      | 4     | R/W | I <sup>2</sup> C_TIME_OUT     | 1 : Enable I <sup>2</sup> C time out check  | 0        |
|      |      | 3     | R   | BCK_LOSS                      | 1 : BCK loss  | 0        |
|      |      | 2     | R   | LRCK_LOSS                     | 1 : LRCK loss   | 0        |

| ADDR | Byte | Bits | R/W | Name             | Description  | Default |
|------|------|------|-----|------------------|--|---------|
|      |      | 7:6  |     | Reserved         |  |         |
| 0xA2 | 1    | 4:0  | R/W | spk_rpt_sel[4:0] | 0x00 : limiter gain = spk_rpt * 16<br>0x01 : ALC gain = spk_rpt * 16<br>0x02 : gain information = spk_rpt<br>0x03 : voltage output w/o pilot = spk_rpt * 16<br>0x04 : voltage output w/l pilot = spk_rpt<br>0x05 : corrent sense result = spk_rpt<br>0x06 : (voltage output w/l pilot)*current sense = spk_rpt * 16<br>0x07 : ATC gain = spk_rpt * 16<br>0x08 : voltage delay = spk_rpt * 16<br>0x09: Estimated current = spk_rpt * 16<br>0x0a : Estimated current error = spk_rpt * 16<br>0x0b : Estimated velocity = spk_rpt * 16<br>0x0c : Estimated excursion = spk_rpt * 16<br>0x0d : Estimated Resistor = spk_rpt * 16<br>0x0e : input signal peak = spk_rpt * 16<br>0x0f : excursion peak = spk_rpt * 16<br>0x10 : phi1 = spk_rpt * 16π<br>0x11 : phi2 = spk_rpt * 16π<br>0x12 : phi3 = spk_rpt * 16π<br>0x13 : phi4 = spk_rpt * 16π<br>0x14 : phi5 = spk_rpt * 16π<br>0x15 : adaptive b0 = spk_rpt * 16<br>0x16 : adaptive b1 = spk_rpt * 16<br>0x17 : adaptive b2 = spk_rpt * 16<br>0x18 : adaptive b3 = spk_rpt * 16<br>0x19 : adaptive b4 = spk_rpt * 16<br>0x1a : adaptive b5 = spk_rpt * 16<br>0x1b : tx_data = spk_rpt<br>0x1c : rx_pilot = spk_rpt<br>0x1d : tx_pilot = spk_rpt<br>0x1e : digital maximum allowable absolute data = spk_rpt * 16<br>0x1f :<br>single_tone = spk_rpt[23]<br>active = spk_rpt[22]<br>silence = spk_rpt[21]<br>dmgRes = spk_rpt[20]<br>dmgFreq = spk_rpt[19]<br>damage = spk_rpt[18]<br>acq = spk_rpt[17]<br>spkE = spk_rpt[16]<br>cntr10ms = spk_rpt[8:0] | 5'h02   |

| ADDR | Byte | Bits | R/W | Name                | Description   | Default  |
|------|------|------|-----|---------------------|---|--|
| 0xA3 | 3    | 23:0 | R   | spk_rpt[23:0]       | Format : Q0.23, please refer to spk_rpt_sel   |  |
| 0xA4 | 3    | 23:0 | R/W | nDelay[23:0]        | The delay added to the output voltage of SPKFB for synchronization.<br>nDelay = reg[0xa4] / 2 <sup>21</sup><br>The range is [-2, 3) with 21 fractional bits.  | 0  |
| 0xA5 | 3    | 23:0 | R/W | res[23:0]           | The initial value of the parameter which is proportional to the resistance.<br>Resistance = reg[0xa5] / 2 <sup>23</sup><br>The range is [0, 2) with 23 fractional bits.                                 | 24'h800000   |
| 0xA6 | 3    | 23:0 | R/W | phi1[23:0]          | The initial value of the radians for the adaptive filter.<br>The radians $\pi/2$ is normalized to 1/2, and the range is [-0.5, 0.5] with 23 fractional bits.<br>Phi1 c = reg[a6] / 2 <sup>23</sup> * pi | 24'hC4266F   |
| 0xA7 | 3    | 23:0 | R/W | phi2[23:0]          |   | 24'h345F58   |
| 0xA8 | 3    | 23:0 | R/W | phi3[23:0]          |   | 24'hFE21CB   |
| 0xA9 | 3    | 23:0 | R/W | phi4[23:0]          |   | 24'h000000   |
| 0xAA | 3    | 23:0 | R/W | phi5[23:0]          |   | 24'h000000   |
| 0xAB | 3    | 23:0 | R/W | Adptive_b0[23:0]    |   | The initial value of the expansion coefficient for the adaptive filter.<br>The range is [-2, 2) with 22 fractional bits.<br>B0 = reg[ab] / 2 <sup>22</sup> |
| 0xAC | 3    | 23:0 | R/W | Adptive_b1[23:0]    | 24'hF1EBC8  |  |
| 0xAD | 3    | 23:0 | R/W | Adptive_b2[23:0]    | 24'h33BD58  |  |
| 0xAE | 3    | 23:0 | R/W | Adptive_b3[23:0]    | 24'h309E9   |  |
| 0xAF | 3    | 23:0 | R/W | Adptive_b4[23:0]    | 24'h000000  |  |
| 0xB0 | 3    | 23:0 | R/W | Adptive_b5[23:0]    | 24'h000000  |  |
| 0xB4 | 1    | 7    | R/W | OTP_PLL_LOCK_IGNORE | Access MTP memory without PLL lock  | 0  |
|      |      | 5:4  | R/W | D_IB_IDAC2          | Boost block Bias current option<br>00 = 1.25 $\mu$<br>01 = 2.5 $\mu$<br>10 = 3.75 $\mu$<br>11 = 5 $\mu$   | 2'b01  |
|      |      | 3    | R/W | TDM_EN              | I <sup>2</sup> S TDM enable bit   | 0  |
|      |      | 2    | R/W | TDM_ADC_SEL         | I <sup>2</sup> S ADC TDM slot selection   | 0  |
|      |      | 1    | R/W | TDM_DAC_SEL         | I <sup>2</sup> S DAC TDM slot selection   | 0  |
|      |      | 0    | R/W | dcrEstInSiilMod     | Do DCR estimation when act signal is not logic 0  | 0  |
| 0xCF | 1    | 7:0  | R/W | DRC_MIN_GAIN        |   | 8'hFF  |
| 0xD0 | 1    | 7:4  | R/W | Reserved            |   | 2'b00  |
|      |      | 3:0  | R/W | DRC_SET_SEL[3:0]    | 0000 : DRC1<br>0001 : DRC2<br>0010 : DRC3<br>0011 : DRC4<br>0100 : DRC5<br>other : no define  | 4'h0   |



| ADDR | Byte | Bits    | R/W | Name          | Description  | Default      |
|------|------|---------|-----|---------------|--|--------------|
| 0xD1 | 16   | 127:122 |     | Reserved      |  |              |
|      |      | 121:96  | R/W | DRC_AE        | DRC_AE[25:0]   | 26'h0800000  |
|      |      | 95:90   |     | Reserved      |  |              |
|      |      | 89:64   | R/W | DRC_1_AE      | DRC_1_AE[25:0]   | 26'h0000000  |
|      |      | 63:58   |     | Reserved      |  |              |
|      |      | 57:32   | R/W | DRC_AA        | DRC_AA[25:0]   | 26'h0800000  |
|      |      | 31:26   |     | Reserved      |  |              |
|      |      | 25:0    | R/W | DRC_AD        | DRC_AD[25:0]   | 26'h0800000  |
| 0xD2 | 7    | 55      | R/W | DRC_RMS       | 0 : RMS<br>1 : Peak  | 0            |
|      |      | 54:52   | R/W | DRC_KNEE[2:0] |  | 3'b000       |
|      |      | 51:50   |     | Reserved      |  |              |
|      |      | 49:40   | R/W | DRC_TH0[9:0]  | 1. 0 to -127dB, 0.125dB per step<br>2. 10'h000 is 0dB<br>3. value definiton is 7.3     | 10'h000      |
|      |      | 39:34   |     | Reserved      |  |              |
|      |      | 33:24   | R/W | DRC_TH1[9:0]  | 1. 0 to -127dB, 0.125dB per step<br>2. 10'h000 is 0dB                                  | 10'h000      |
|      |      | 23:16   | R/W | DRC_OFF[7:0]  | 1. +24dB to -24dB<br>2. 0.25dB per step<br>3. value definiton is 6.2, MSB is sign bit. | 8'h00        |
|      |      | 15:13   |     | Reserved      |  |              |
|      |      | 12:8    | R/W | DRC_R0[4:0]   | 1. 0 to 1<br>2. 5'h10 is 1   | 5'h10        |
|      |      | 7       |     | Reserved      |  |              |
|      |      | 6:0     | R/W | DRC_R1[6:0]   | 1. 1 to 8<br>2. 7'h10 is 1   | 7'h10        |
| 0xD3 | 20   | 159:128 | R/W | bq_1_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_1_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_1_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_1_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_1_a2       | u[31:26], a2[25:0]   | 32'h00000000 |
| 0xD4 | 20   | 159:128 | R/W | bq_2_b0       | u[31:26], b0[25:0]   | 32'h00800000 |
|      |      | 127:96  | R/W | bq_2_b1       | u[31:26], b1[25:0]   | 32'h00000000 |
|      |      | 95:64   | R/W | bq_2_b2       | u[31:26], b2[25:0]   | 32'h00000000 |
|      |      | 63:32   | R/W | bq_2_a1       | u[31:26], a1[25:0]   | 32'h00000000 |
|      |      | 31:0    | R/W | bq_2_a2       | u[31:26], a2[25:0]   | 32'h00000000 |

| ADDR | Byte | Bits    | R/W | Name    | Description        | Default      |
|------|------|---------|-----|---------|--------------------|--------------|
| 0xD5 | 20   | 159:128 | R/W | bq_3_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_3_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_3_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_3_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_3_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xD6 | 20   | 159:128 | R/W | bq_4_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_4_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_4_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_4_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_4_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xD7 | 20   | 159:128 | R/W | bq_5_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_5_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_5_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_5_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_5_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xD8 | 20   | 159:128 | R/W | bq_6_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_6_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_6_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_6_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_6_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xD9 | 20   | 159:128 | R/W | bq_7_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_7_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_7_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_7_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_7_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xDA | 20   | 159:128 | R/W | bq_8_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_8_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_8_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_8_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_8_a2 | u[31:26], a2[25:0] | 32'h00000000 |
| 0xDB | 20   | 159:128 | R/W | bq_9_b0 | u[31:26], b0[25:0] | 32'h00800000 |
|      |      | 127:96  | R/W | bq_9_b1 | u[31:26], b1[25:0] | 32'h00000000 |
|      |      | 95:64   | R/W | bq_9_b2 | u[31:26], b2[25:0] | 32'h00000000 |
|      |      | 63:32   | R/W | bq_9_a1 | u[31:26], a1[25:0] | 32'h00000000 |
|      |      | 31:0    | R/W | bq_9_a2 | u[31:26], a2[25:0] | 32'h00000000 |

| ADDR | Byte | Bits    | R/W | Name              | Description                             | Default      |
|------|------|---------|-----|-------------------|---|--------------|
| 0xDC | 20   | 159:128 | R/W | bq_10_b0          | u[31:26], b0[25:0]                      | 32'h00800000 |
|      |      | 127:96  | R/W | bq_10_b1          | u[31:26], b1[25:0]                      | 32'h00000000 |
|      |      | 95:64   | R/W | bq_10_b2          | u[31:26], b2[25:0]                      | 32'h00000000 |
|      |      | 63:32   | R/W | bq_10_a1          | u[31:26], a1[25:0]                      | 32'h00000000 |
|      |      | 31:0    | R/W | bq_10_a2          | u[31:26], a2[25:0]                      | 32'h00000000 |
| 0xDD | 20   | 159:128 | R/W | bq_11_b0          | u[31:26], b0[25:0]                      | 32'h00800000 |
|      |      | 127:96  | R/W | bq_11_b1          | u[31:26], b1[25:0]                      | 32'h00000000 |
|      |      | 95:64   | R/W | bq_11_b2          | u[31:26], b2[25:0]                      | 32'h00000000 |
|      |      | 63:32   | R/W | bq_11_a1          | u[31:26], a1[25:0]                      | 32'h00000000 |
|      |      | 31:0    | R/W | bq_11_a2          | u[31:26], a2[25:0]                      | 32'h00000000 |
| 0xDE | 20   | 159:128 | R/W | bq_12_b0          | u[31:26], b0[25:0]                      | 32'h00800000 |
|      |      | 127:96  | R/W | bq_12_b1          | u[31:26], b1[25:0]                      | 32'h00000000 |
|      |      | 95:64   | R/W | bq_12_b2          | u[31:26], b2[25:0]                      | 32'h00000000 |
|      |      | 63:32   | R/W | bq_12_a1          | u[31:26], a1[25:0]                      | 32'h00000000 |
|      |      | 31:0    | R/W | bq_12_a2          | u[31:26], a2[25:0]                      | 32'h00000000 |
| 0xDF | 2    | 15      | R/W | DC_CUT_FILTER_DIS | 1 : Disable DC-Cut filter               | 0            |
|      |      | 14      | R/W | H_BAND_BYPASS     | 1 : Bypass High band DRC                | 0            |
|      |      | 13      | R/W | M_BAND_BYPASS     | 1 : Bypass Middle band DRC              | 0            |
|      |      | 12      | R/W | L_BAND_BYPASS     | 1 : Bypass Low band DRC                 | 0            |
|      |      | 11:10   |     | Reserved          |   |              |
|      |      | 9       | R/W | SideChain_2_ON    | 1 : Enable sidchain for low band DRC    | 0            |
|      |      | 8       | R/W | SideChain_1_ON    | 1 : Enable sidchain for Middle band DRC | 0            |
|      |      | 7:5     |     | Reserved          |   | 0            |
|      |      | 4       | R/W | DRC5_EN           | 1 : DRC5 enable                         | 0            |
|      |      | 3       | R/W | DRC4_EN           | 1 : DRC4 enable                         | 0            |
|      |      | 2       | R/W | DRC3_EN           | 1 : DRC3 enable                         | 0            |
|      |      | 1       | R/W | DRC2_EN           | 1 : DRC2 enable                         | 0            |
|      |      | 0       | R/W | DRC1_EN           | 1 : DRC1 enable                         | 0            |
| 0xF4 | 1    | 7       | R/W | FDRC_CK_EN        | 1 : enable FDRC block clock             | 1            |
|      |      | 6       | R/W | BOOST_CK_EN       | 1 : enable BOOST block clock            | 1            |
|      |      | 5       | R/W | ADC_CK_EN         | 1 : enable ADC block clock              | 1            |
|      |      | 4       | R/W | DAC_CK_EN         | 1 : enable DAC block clock              | 1            |
|      |      | 3       | R/W | SSRC_CK_EN        | 1 : enable SSRC block clock             | 1            |
|      |      | 2       | R/W | DSP_CK_EN         | 1 : enable DSP block clock              | 1            |
|      |      | 1       | R/W | SPK_CK_EN         | 1 : enable SPK Protection block clock   | 1            |
|      |      | 0       | R/W | ANA_CK_EN         | 1 : enable analog block clock           | 1            |

| ADDR | Byte | Bits | R/W | Name             | Description                       | Default |
|------|------|------|-----|------------------|-----------------------------------|---------|
| 0xF5 | 1    | 7:2  | R/W | Reserved         |                                   | 6'h00   |
|      |      | 1    | R/W | SAFE_GUARD_CK_EN | 1 : enable SAFE Guard block clock | 1       |
|      |      | 0    | R/W | CAL_CK_EN        | 1 : enable Cal block clock        | 1       |

**Application Information**

**Inductor Selection**

The recommended value of inductor for DC-to-DC boost converter applications is 1μH. Small size and better efficiency are the major concerns for portable devices, such as the RT5509 used for mobile phone. The inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency.

The maximum current of inductor is highly depends on the speaker impedance which determines the output current of the boost converter. The inductor saturation

current rating should be considered to cover the inductor peak current which can be approximated by the following equation :

$$I_{L\_max} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}$$

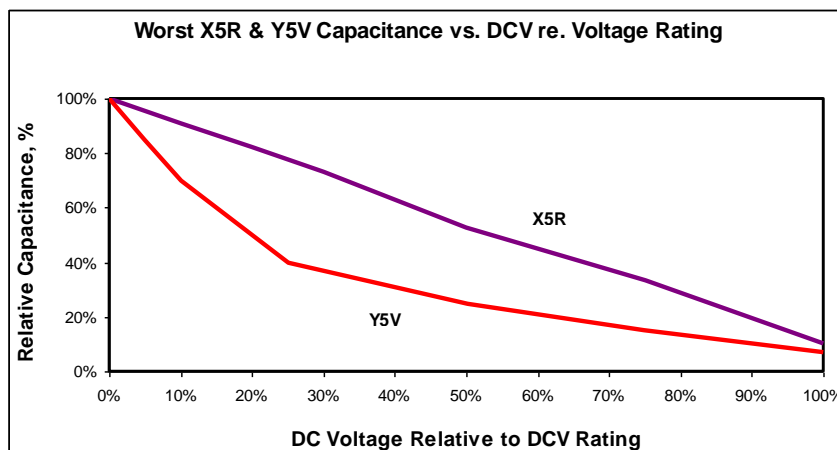
Following is the inductor selection reference for typical speaker impedances with 10% tolerance and 95% efficient.

| R <sub>L</sub> (Ω) | I <sub>OUT</sub> (A) | I <sub>L_MAX</sub> (A) | Manufacturer | Part Number    |
|--------------------|----------------------|------------------------|--------------|----------------|
| 8                  | 1.14                 | 1.43                   | Murata       | MDT2520-CN1ROM |
| 6                  | 1.52                 | 1.81                   | Coilcraft    | PFL2512-102MEB |
| 4                  | 2.28                 | 2.57                   | Coilcraft    | LPS4012-102NLB |

**Capacitor Selection**

For low ripple voltage, ceramic capacitors with low ESR are recommended. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. X5R and X7R types are suitable because

of their wide voltage range and good operating temperature characteristics. The capacitance value decreases over the DC-biasing voltage range (30% to 70% decrease) as following figure. Consequently, the nominal value of the capacitor should be close to twice the minimum value specified



The output ripple can be determined as following equation :

$$\Delta V_{OUT} = \frac{D \times I_{OUT} \times T_S}{\eta \times C_{OUT}} + \left( \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}} \right) \times r_{C\_esr}$$

For the application of the RT5509 to boost VBAT to 9.5V, a 10μF for input capacitor, an 22μF for boost capacitor and a 100nF for DVDD decoupling capacitor are recommended.

Boost capacitor connect to BST is important for stability. The C<sub>PVDD</sub> capacitance is changed by DC bias. When select capacitor, please notice the DC bias characteristics. The RT5509 minimum recommended C<sub>PVDD</sub> capacitance is 6μF for output power 3.6W, C<sub>PVDD</sub> capacitance is 8μF for output power 4.3W.

### Filter Free Operation and Ferrite Bead Filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. Typically, impedance rises over 150Ω before 30MHz to provide at least -20dB decade is minimum requirement (such as TDK : MPZ1608S221A) Figure 21. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

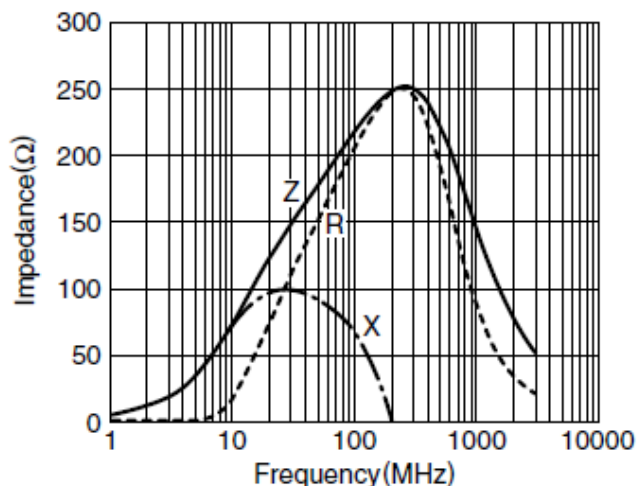


Figure 21. Impedance of MPZ1608S221A

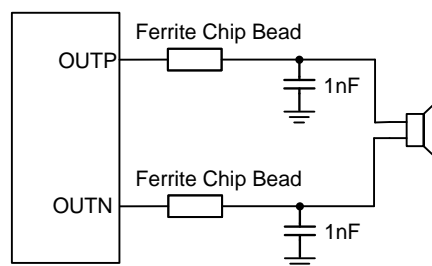


Figure 22. Typical Ferrite Chip Bead Filter

### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature  $T_{J(MAX)}$ , listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance,  $\theta_{JA}$ , is highly package dependent. For WL-CSP-48B 3.04x2.99 (BSC)

package, the thermal resistance,  $\theta_{JA}$ , is  $27^{\circ}\text{C/W}$  on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at  $T_A = 25^{\circ}\text{C}$  can be calculated as below :

$$P_{D(\text{MAX})} = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / (27^{\circ}\text{C/W}) = 3.7\text{W for a WL-CSP-48B } 3.04 \times 2.99 \text{ (BSC) package}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed  $T_{J(\text{MAX})}$  and the thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 23 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

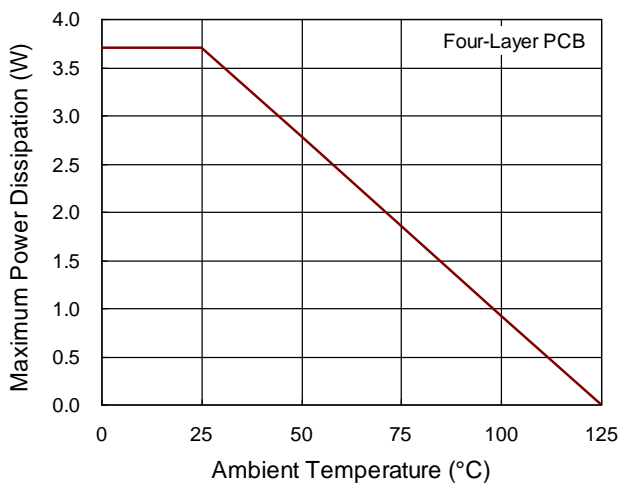


Figure 23. Derating Curve of Maximum Power Dissipation

**Layout Consideration**

For best performance of the RT5509, the below PCB Layout guidelines must be strictly followed.

For achieving good quality, the traces of VSPOUTP and VSPOUTN should be kept equal width and length respectively. The Bead + C should be placed close to chip for better EMI performance. The power trace of boost inductor is suggested to place on the external layers for higher current capability. Please place the inductor as close as possible to the chip.

For achieving good audio quality, must place the decoupling capacitors as close as possible to the DVDD pins and ground connection link to DGND and AGND first before going to GND plane, the trace width of DVDD is 6mil at least. 1.8V source provide other device power in the system. If power trace layout was not well, that can adversely affect their own.

To prevent this problem, Star connection used from DVDD power source to DVDD directly.

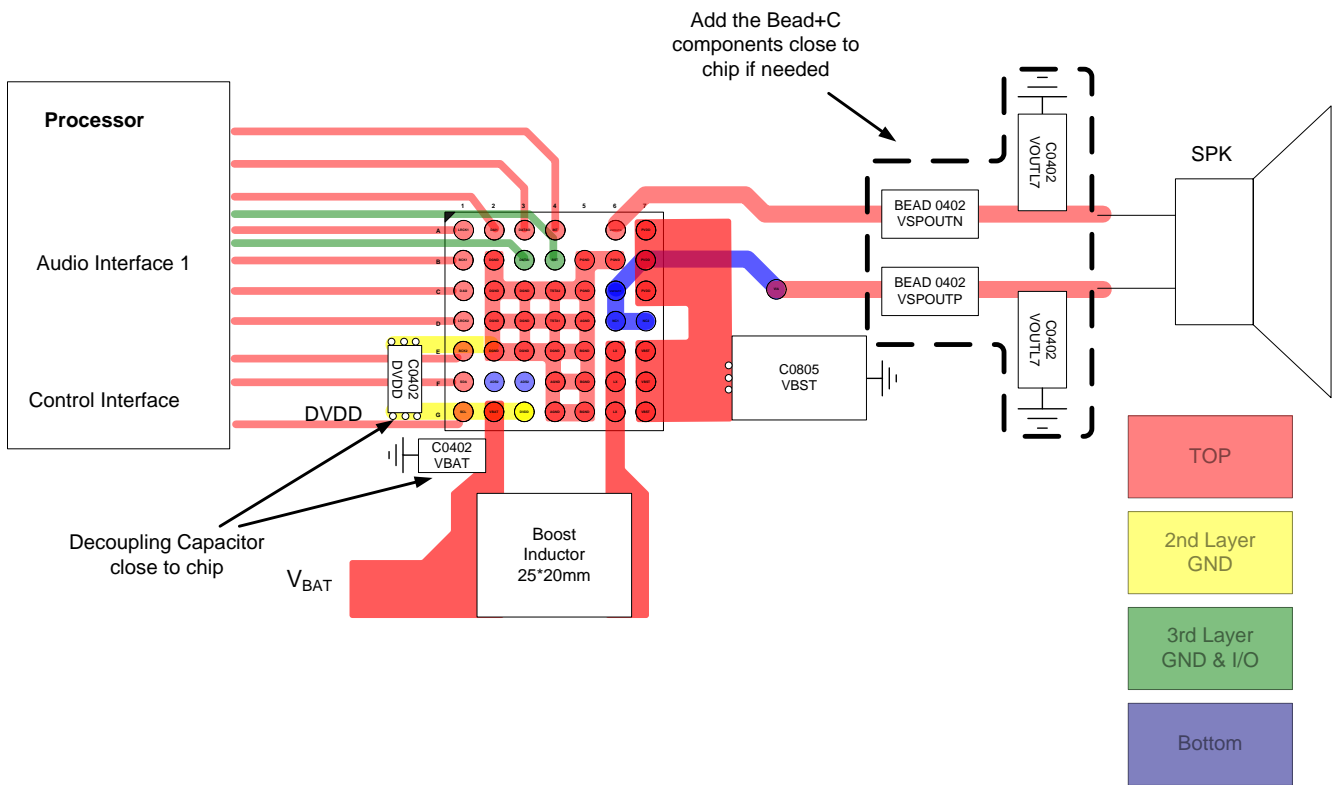


Figure 24. PCB Layout Guide

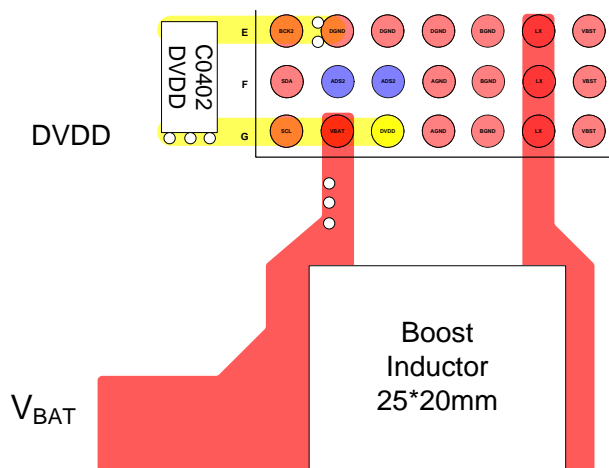
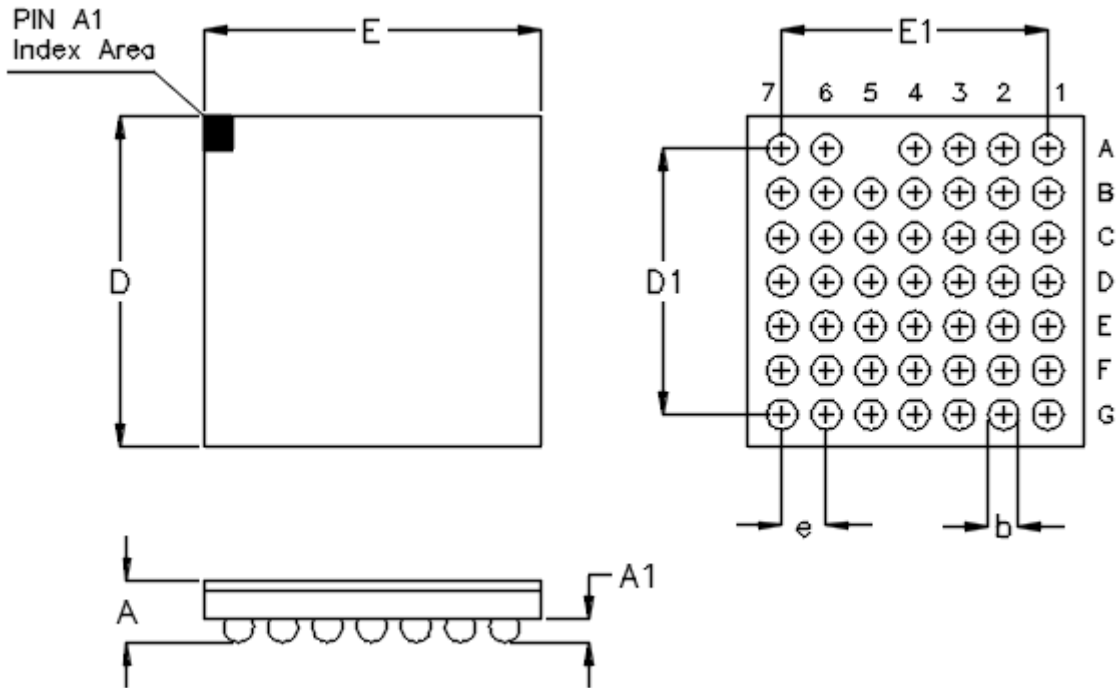


Figure 25. DVDD Layout Suggestion



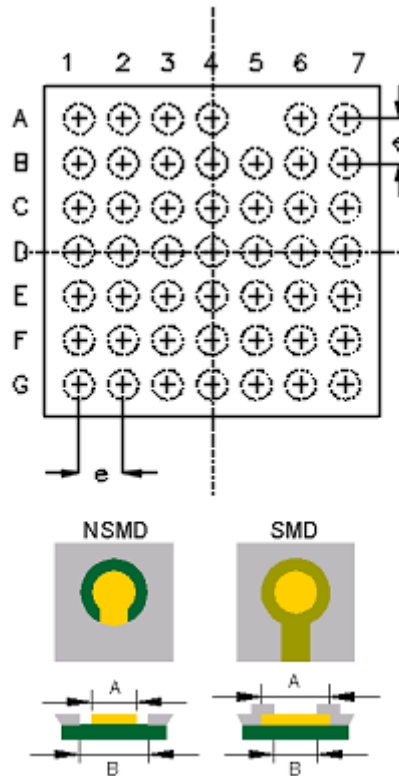
**Outline Dimension**



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | 0.500                     | 0.600 | 0.020                | 0.024 |
| A1     | 0.170                     | 0.230 | 0.007                | 0.009 |
| b      | 0.240                     | 0.300 | 0.009                | 0.012 |
| D      | 2.950                     | 3.030 | 0.116                | 0.119 |
| D1     | 2.400                     |       | 0.094                |       |
| E      | 3.000                     | 3.080 | 0.118                | 0.121 |
| E1     | 2.400                     |       | 0.094                |       |
| e      | 0.400                     |       | 0.016                |       |

**48B WL-CSP 3.04x2.99 Package (BSC)**

Footprint Information



| Package                 | Number of Pin | Type | Footprint Dimension (mm) |       |       | Tolerance |
|-------------------------|---------------|------|--------------------------|-------|-------|-----------|
|                         |               |      | e                        | A     | B     |           |
| WL-CSP3.04x2.99-48(BSC) | 48            | NSMD | 0.400                    | 0.240 | 0.340 | ±0.025    |
|                         |               | SMD  |                          | 0.270 | 0.240 |           |

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