

600nA I_Q, 1A Output HCOT Buck Converter

General Description

The RT5705 is a high efficiency synchronous step-down converter featuring typ. 600nA quiescent current. It provides high efficiency at light load down to few. Its input voltage range is from 2.2V to 5.5V and provides an adjustable regulated output voltage from 1.8V to 3.3V in 100mV steps while delivering output currents up to 1A. The integrated slew rate controlled load switch provides typ. 0.6Ω on-resistance and can distribute the selected output voltage to a sub-system.

The Hysteretic Constant-On-Time (HCOT) operation with internal compensation allow the transient response to be optimized over a wide range of loads and output capacitors.

The RT5705 is a available in WDFN-12AL 3x2 package.

Ordering Information

RT5705 □ □

- Package Type
QW : WDFN-12AL 3x2 (W-Type)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

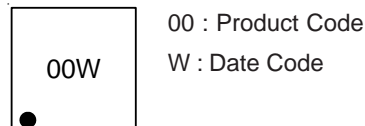
Features

- Operates from a Single Li-ion Cell : 2.2V to 5.5V
- Adjustable Output Voltage : 1.8V to 3.3V
- Typ. 600nA Quiescent Current
- PFM Operation
- Automatic Transition to 100% Duty Cycle Operation Available
- Up to 94% Efficiency
- Internal Compensation
- Output Discharge
- Output Short Protection
- Thermal shutdown Protection
- Power Good Output
- Up to 1A Output Current

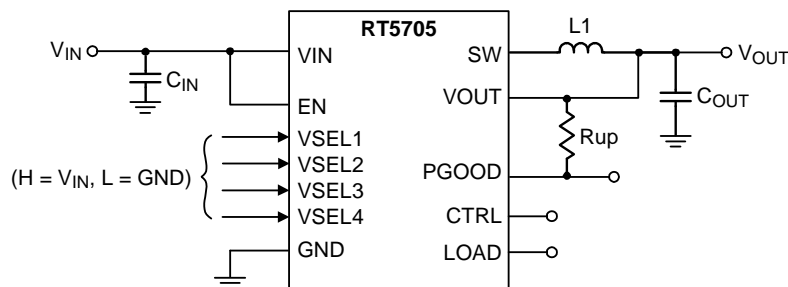
Applications

- Hand-Held Devices Application
- Portable Information Application
- Battery Powered Equipment
- Wearable Devices Application

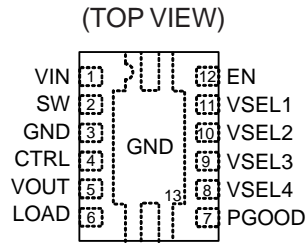
Marking Information



Simplified Application Circuit



Pin Configuration

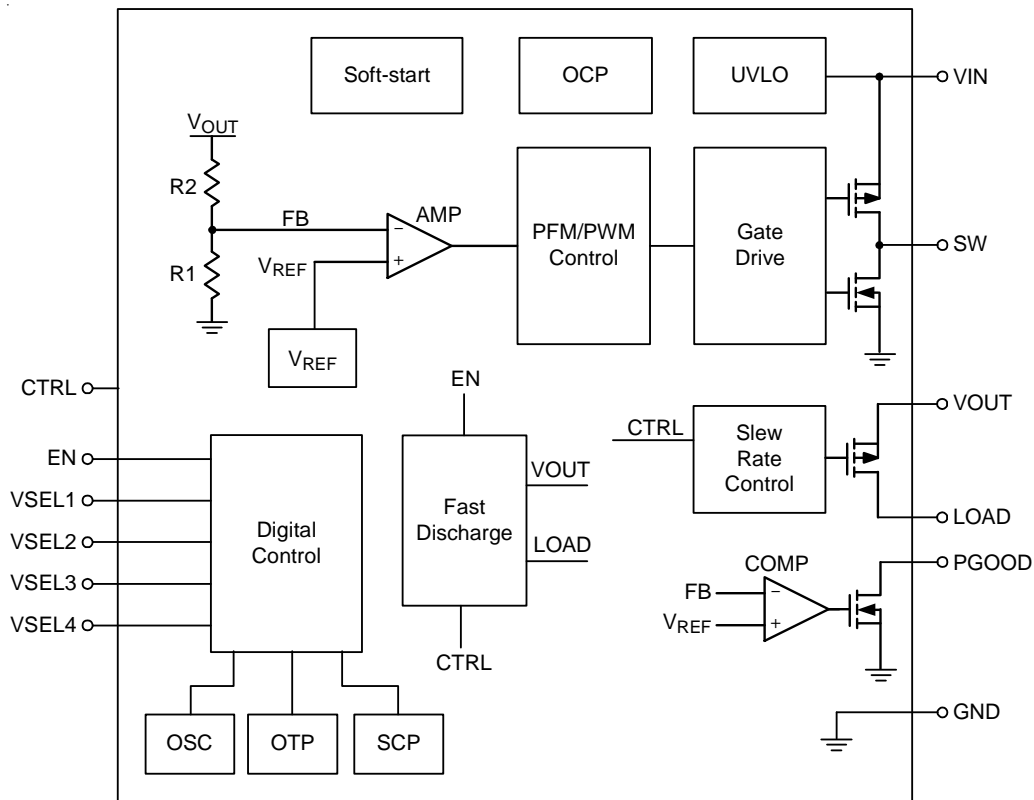


WDFN-12AL 3x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply input voltage.
2	SW	Switch node. Connect this pin to output inductor.
3	GND	Ground.
4	CTRL	CTRL = H, open sub-system, CTRL = L, close sub-system. Don't floating.
5	VOUT	Output voltage.
6	LOAD	Supply rail to sub-system and controlled CTRL pin.
7	PGOOD	Power good pin. (Open drain)
8	VSEL4	Output voltage selection pin. See Table.1 for VOUT selection. (H = VIN, L = GND)
9	VSEL3	Output voltage selection pin. See Table.1 for VOUT selection. (H = VIN, L = GND)
10	VSEL2	Output voltage selection pin. See Table.1 for VOUT selection. (H = VIN, L = GND)
11	VSEL1	Output voltage selection pin. See Table.1 for VOUT selection. (H = VIN, L = GND)
12	EN	Chip enable input.
13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT5705 is a hysteretic constant on time (HCOT) switching buck converter, designed to an adjustable output voltage from an input supply voltage. The inductor current is regulated by a fast current regulator which is controlled by a voltage control loop. The voltage error amplifier gets its feedback input from the VOUT pin. The output voltage of the RT5705 is adjustable via SEL1 to SEL4 pins. When V_{IN} is closed to V_{OUT}, the device entering 100% duty cycle operation with seamless technique and keep a minimum current ripple in the inductor.

Current Protection

The inductor current is monitored via the internal switches cycle-by-cycle.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of V_{IN} is lower than the UVLO falling threshold voltage, the device will be lockout.

Thermal Shutdown

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will autocratically resume switching.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ----- 0.3V to 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 WDFN-12AL 3x2 ----- 3.17W
- Package Thermal Resistance (Note 2)
 WDFN-12AL 3x2, θ_{JA} ----- 31.5°C/W
 WDFN-12AL 3x2, θ_{JC} ----- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature Range ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ----- 2.2V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 3.6\text{V}$, $C_{IN} = 10\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}	$V_{IN} = V_{OUT} + 1\text{V}$	2.2	--	5.5	V
Under-Voltage Lockout Rising Threshold	V_{UVLOR}		2	--	2.2	V
Under-Voltage Lockout Falling Threshold	V_{UVLOF}		1.8	--	2	V
VOUT Voltage Accuracy	V_{OUT_acc}	$V_{IN} = 3.6\text{V}$, $I_{OUT} = 100\text{mA}$, $V_{OUT} = 1.8\text{V}$	-2	0	2	%
Input Quiescent Current	I_{QVIN}	Non-switching	--	600	--	nA
Switching Quiescent Current	I_{QSW}	$V_{IN} = 3.6\text{V}$, $V_{OUT} = 3.3\text{V}$	--	1	--	μA
Shutdown Current	I_{SHDN}	$V_{IN} = 3.6\text{V}$, $EN = 0\text{V}$	--	0.2	1	μA
UGATE Current Limit	I_{CLUG}	$2.2\text{V} \leq V_{IN} \leq 5.5\text{V}$	--	1.5	--	A
LGATE Current Limit	I_{CLLG}	$2.2\text{V} \leq V_{IN} \leq 5.5\text{V}$	--	1.5	--	A
High Side Switch R_{ON}		$V_{IN} = 3.6\text{V}$	--	350	--	$\text{m}\Omega$
Low Side Switch R_{ON}		$V_{IN} = 3.6\text{V}$	--	250	--	$\text{m}\Omega$
VOUT Pin Input Leakage	I_{VOUT}	$V_{OUT} = 3.3\text{V}$	--	100	--	nA
SW Pin Leakage Current	I_{SW}		--	--	5	μA
Operation Quiescent Current_Laod Switch (OPEN)	I_Q	CTRL = H, non-switching,	--	6	10	μA
VOUT Minimum Off Time	t_{MIN_OFF}	$V_{IN} = 3.6\text{V}$, $V_{OUT} = 1.8\text{V}$	--	80	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Minimum On Time	t _{MIN_ON}	V _{IN} = 3.6V, V _{OUT} = 1.8V	--	385	--	ns
Load Switch						
Load Switch R _{ON}	R _{ON_LOAD}	V _{OUT} = 1.8V, I _{OUT} = 50mA, CTRL = V _{IN} , V _{IN} = 2.2V to 5.5V	--	0.6	--	Ω
Load Switch Discharge R _{ON}	R _{ON_LOADDis}	V _{OUT} = 1.8V, I _{OUT} = 50mA, CTRL = GND, V _{IN} = 2.2V to 5.5V	--	10	--	Ω
Timing						
Regulator Start Up Delay Time	t _{SS_EN}	EN to V _{OUT} rising	--	0.1	--	ms
Regulator Soft Start Time	t _{SS}	V _{IN} = 2.2 to 5.5V, EN = V _{IN}	--	2	--	ms
Load Switch Rise Time	t _{Rise_LOAD}	I _{OUT} = 0mA, I _{LOAD} = 20mA, CTRL = GND to V _{IN} , V _{IN} = 2.2V to 5.5V	--	200	--	μs
Logic Input						
Input High Threshold	V _{IH}	V _{IN} = 2.2V to 5.5V	1.2	--	--	V
Input Low Threshold	V _{IL}	V _{IN} = 2.2V to 5.5V	--	--	0.4	V
Input Pin Bias Current	I _{IN}		--	10	--	nA
Power Good OUTPUT						
Power Good Threshold Voltage	V _{TH_PG+}	Rising output voltage on V _{OUT} pin, referred to V _{OUT}	--	97.5	--	%
Low Level Output Voltage	V _{OUT_L}	2.2V ≤ V _{IN} ≤ 5.5V, EN = GND, current into PG pin I _{PG} = 4mA	--	--	0.3	V
Bias Current into PG Pin	I _{IN_PG}	PG pin is high impedance, V _{OUT} = 2V, EN = V _{IN} , CTRL = GND, I _{OUT} = 0mA	--	--	25	nA

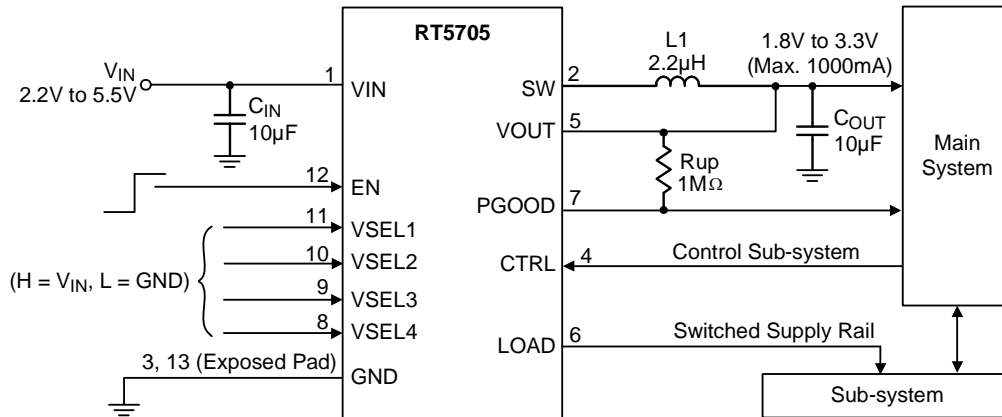
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



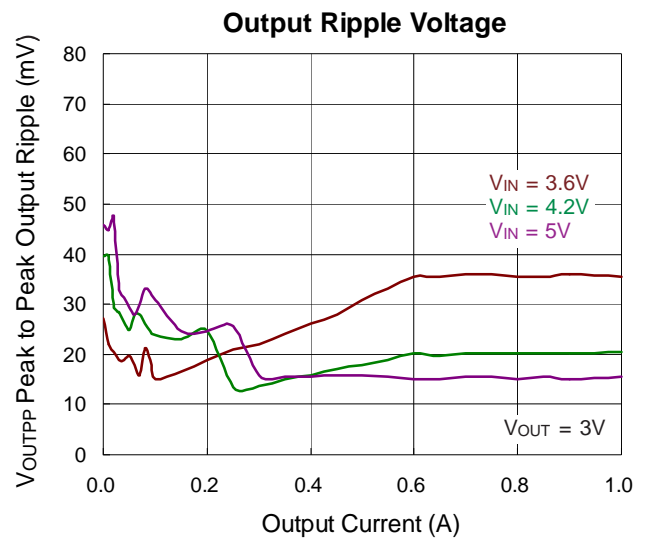
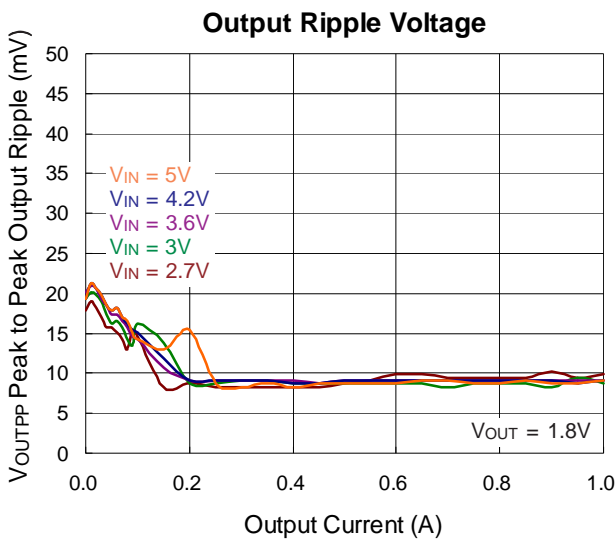
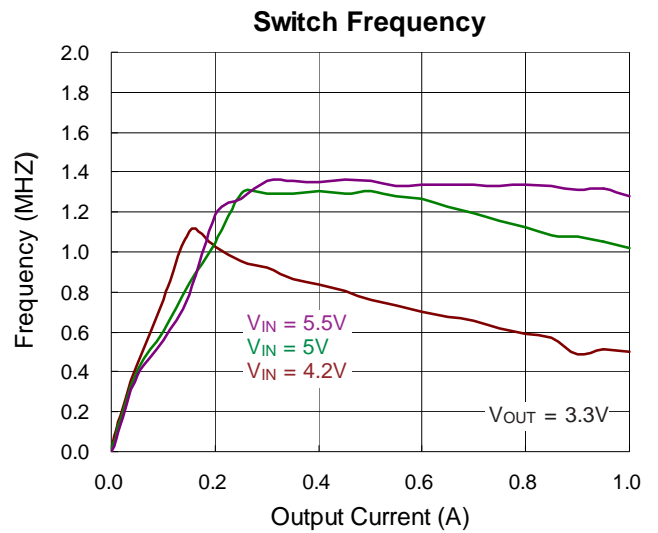
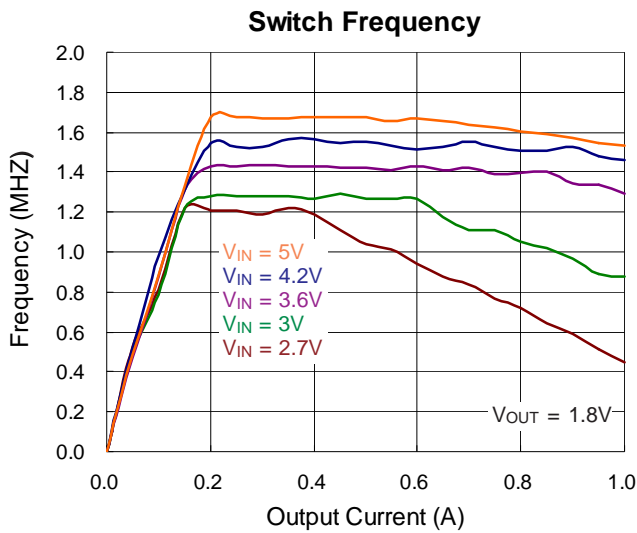
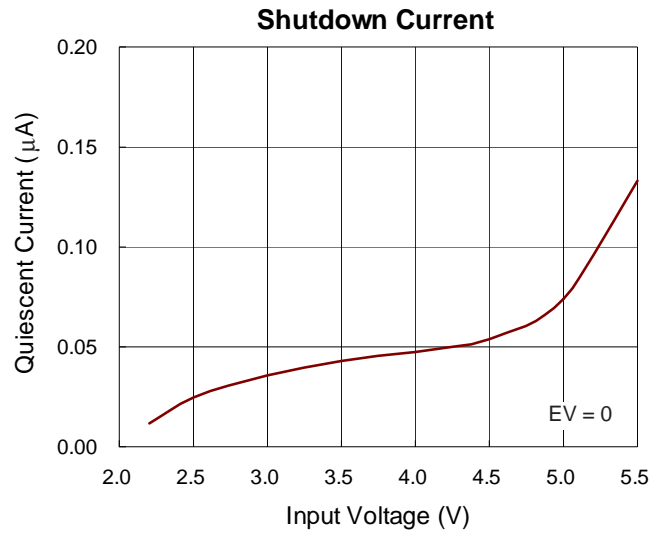
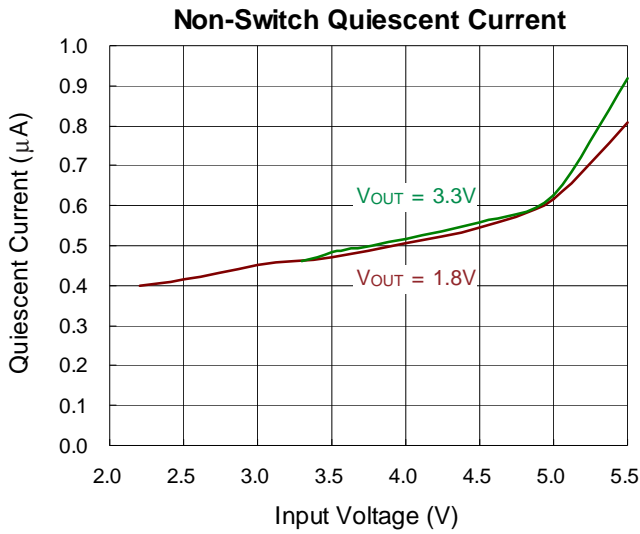
BOM List

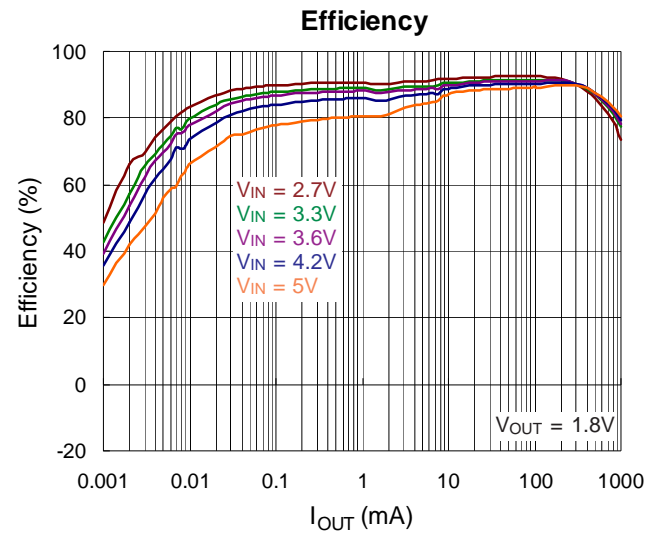
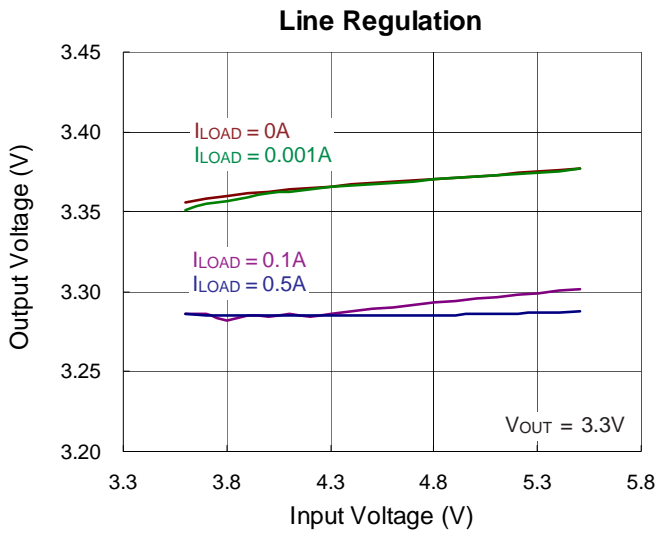
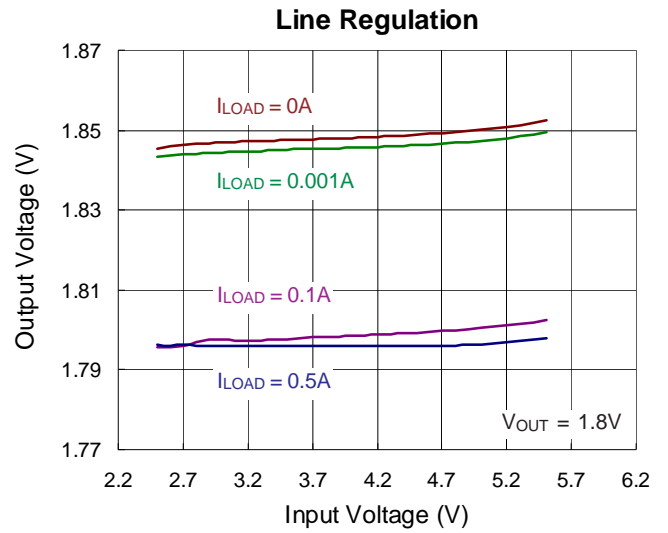
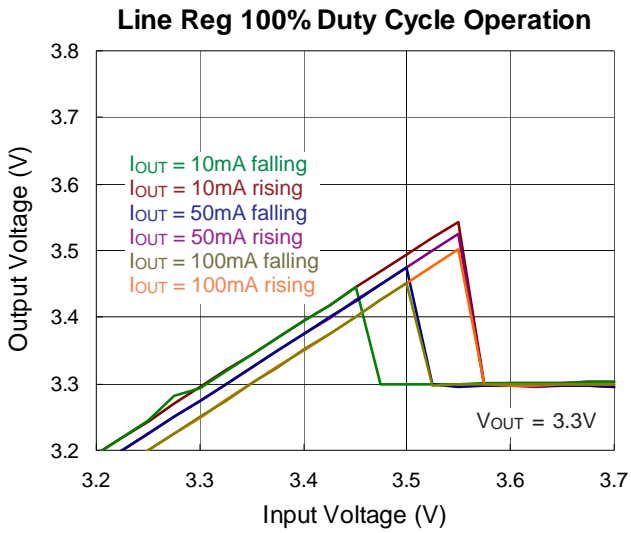
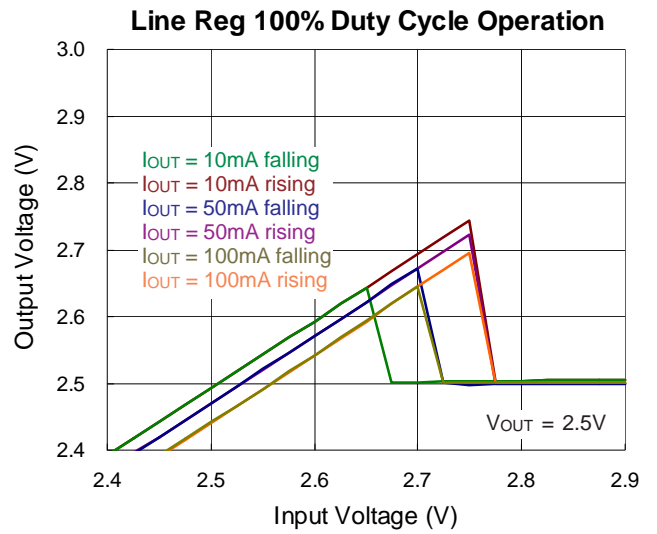
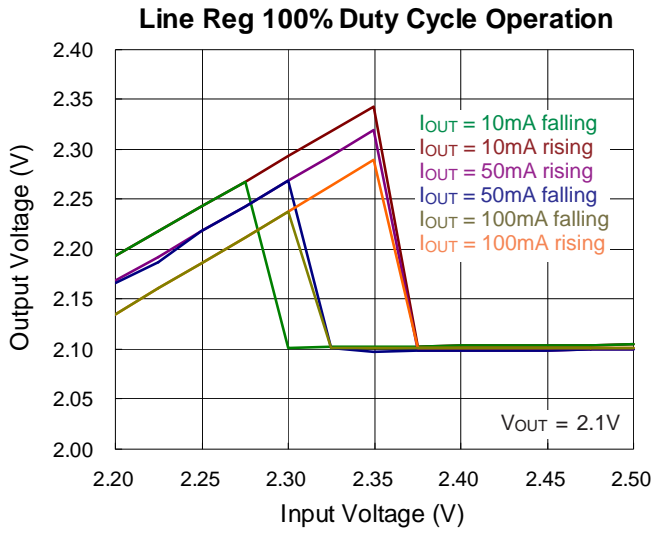
Reference	Part Number	Manufacturer	Package	Value
C _{IN} , C _{OUT}	GRM188R60J106M	Murata	0603/X5R	10µF
L1	1239AS-H-2R2M	Murata	252012	2.2µH

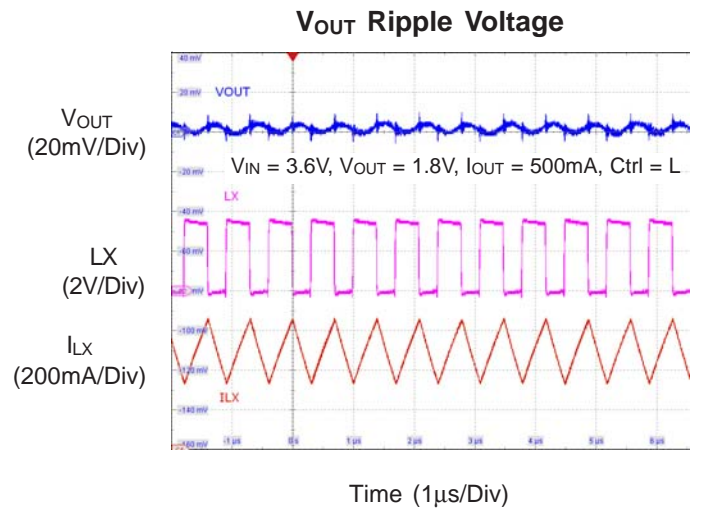
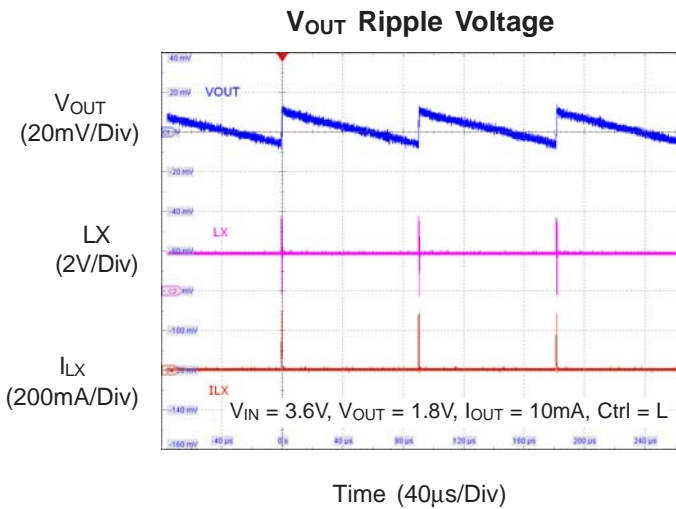
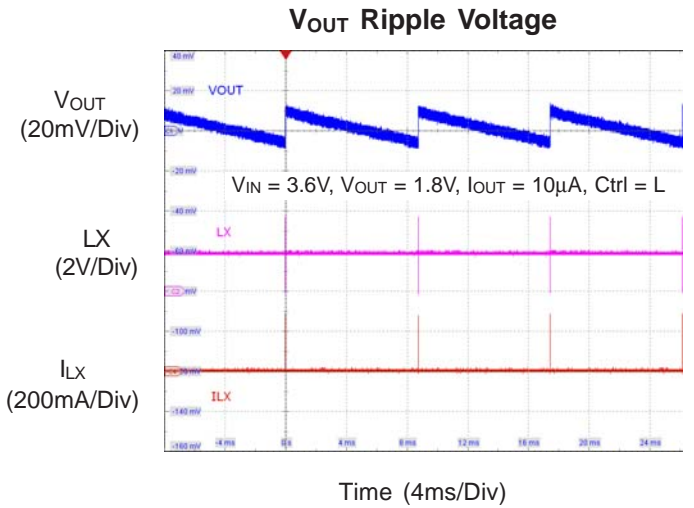
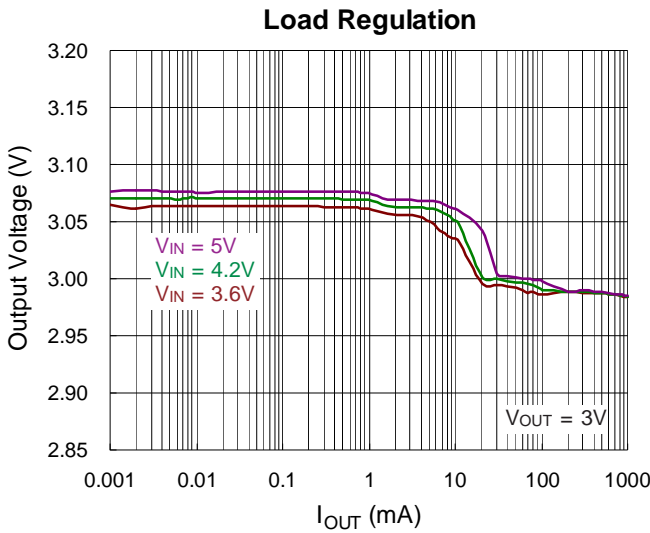
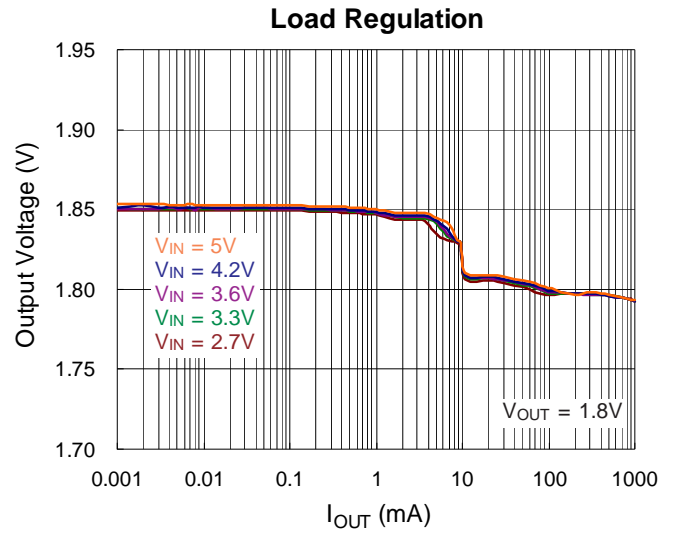
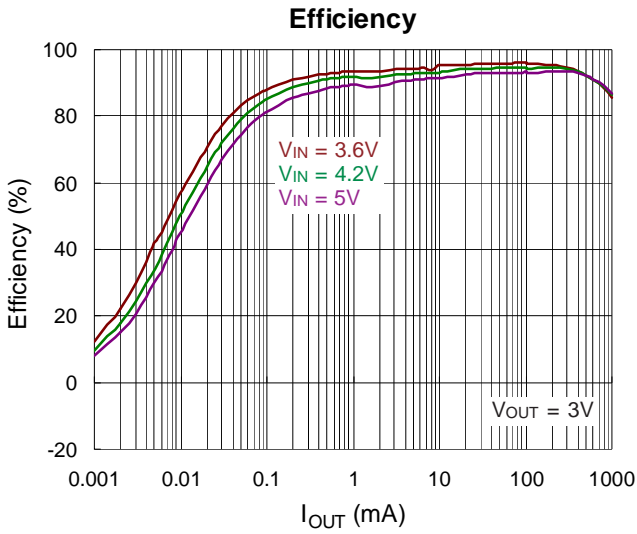
Table 1. Output Voltage Setting

V _{OUT} (V)	VSEL4	VSEL3	VSEL2	VSEL1
1.8	0	0	0	0
1.9	0	0	0	1
2	0	0	1	0
2.1	0	0	1	1
2.2	0	1	0	0
2.3	0	1	0	1
2.4	0	1	1	0
2.5	0	1	1	1
2.6	1	0	0	0
2.7	1	0	0	1
2.8	1	0	1	0
2.9	1	0	1	1
3	1	1	0	0
3.1	1	1	0	1
3.2	1	1	1	0
3.3	1	1	1	1

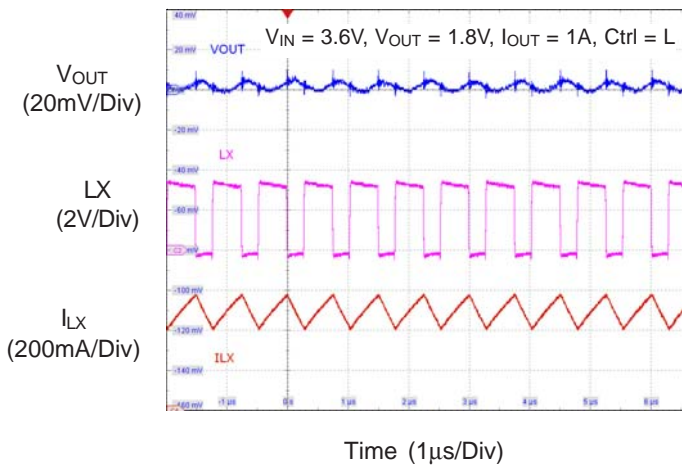
Typical Operating Characteristics



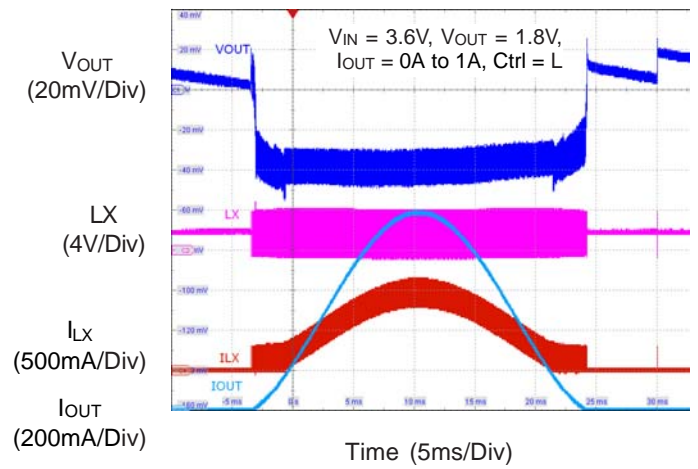




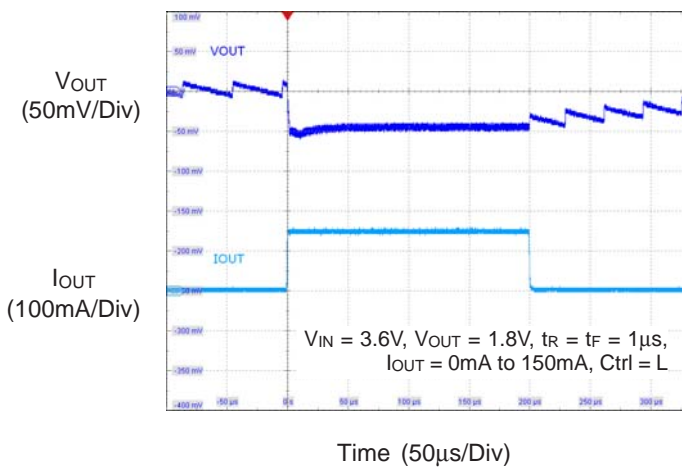
V_{OUT} Ripple Voltage



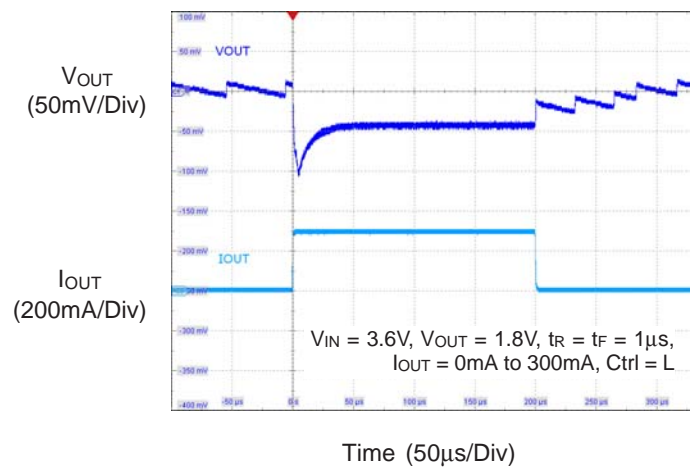
Load Sweep V_{OUT}



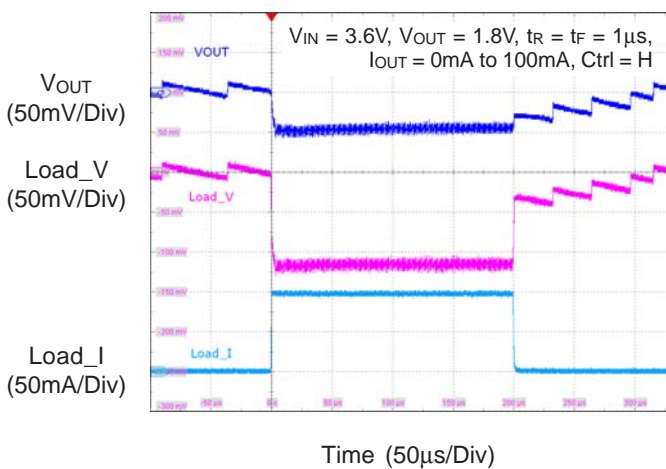
Load Transient



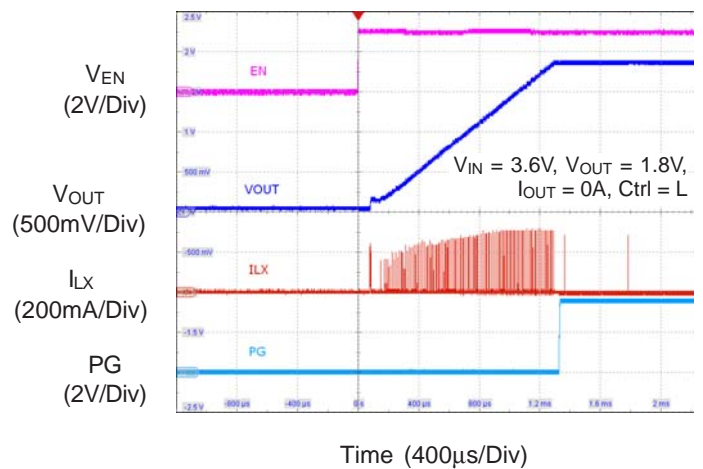
Load Transient



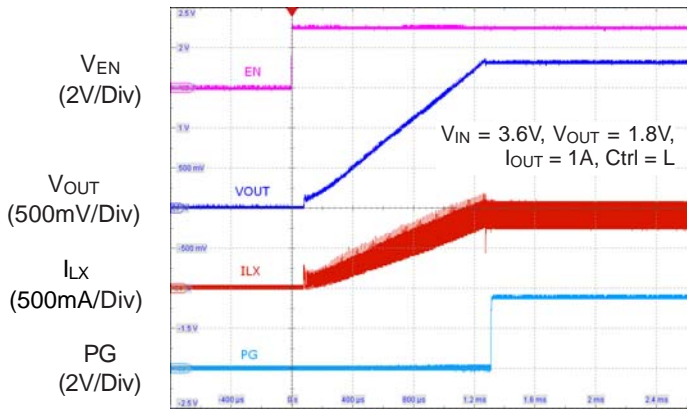
Load Transient at LSW



Power On EN

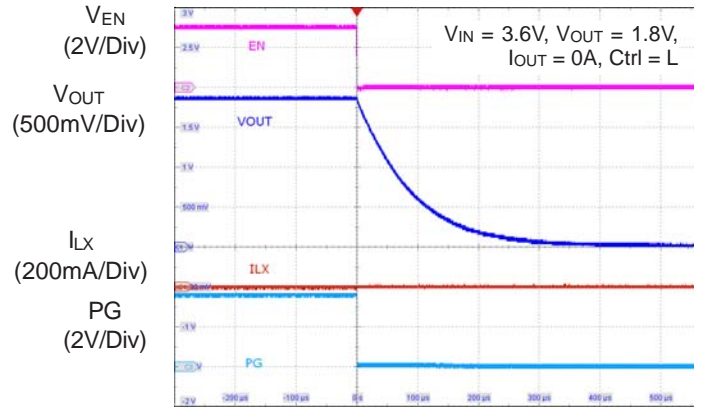


Power On EN



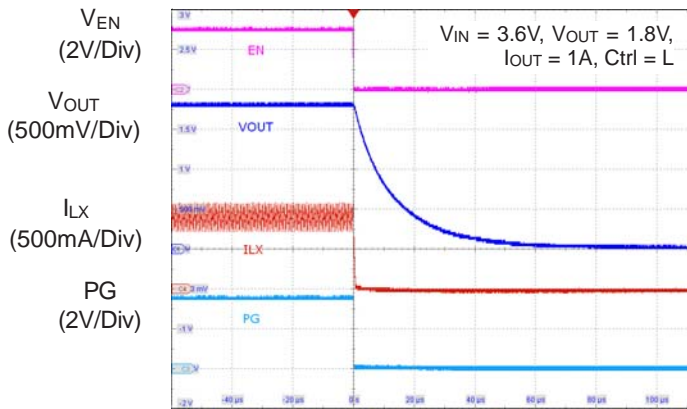
Time (400µs/Div)

Power Off EN



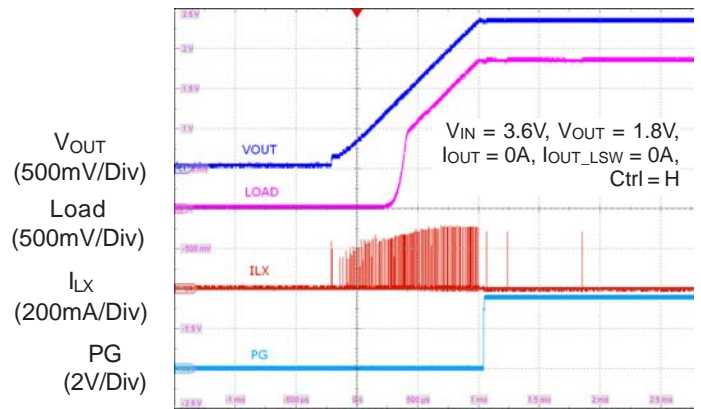
Time (100µs/Div)

Power Off EN



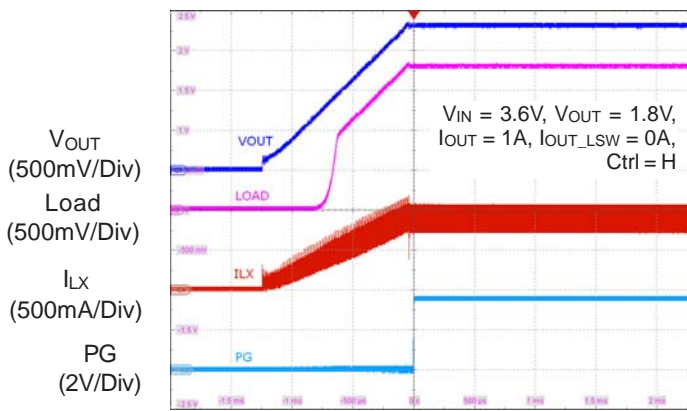
Time (20µs/Div)

Power On LSW



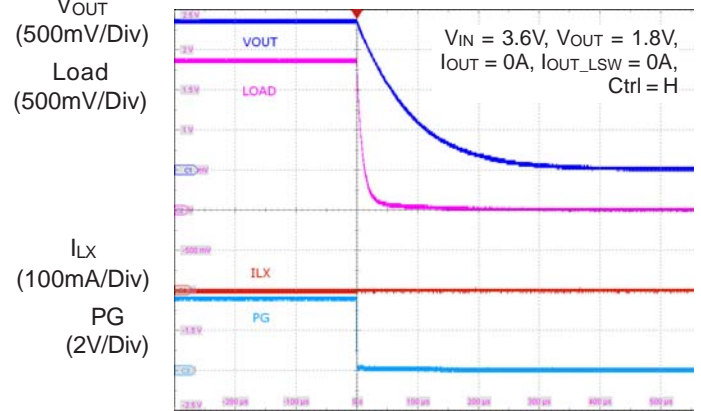
Time (500µs/Div)

Power On LSW



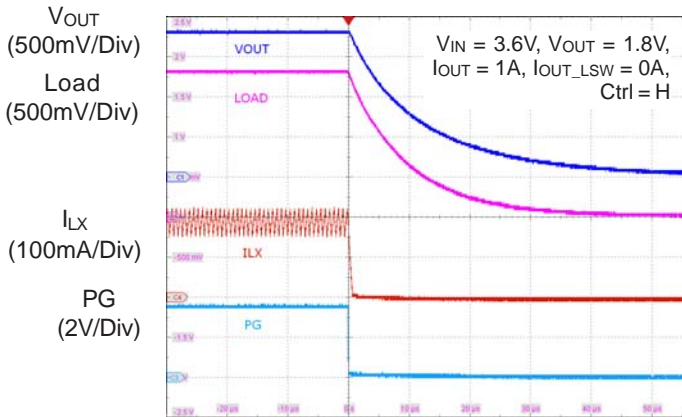
Time (500µs/Div)

Power Off LSW



Time (100µs/Div)

Power Off LSW



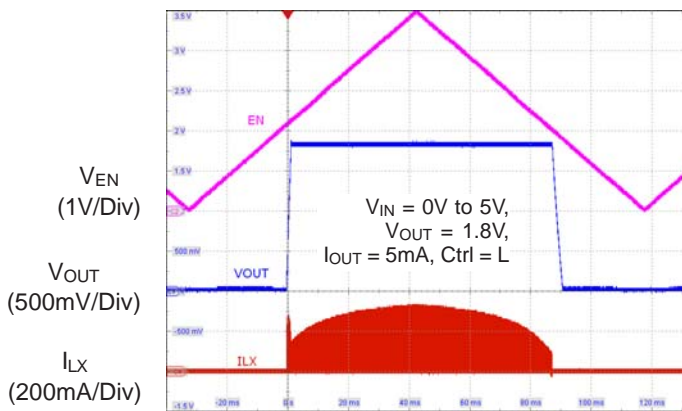
Time (10µs/Div)

Dynamic VSEL



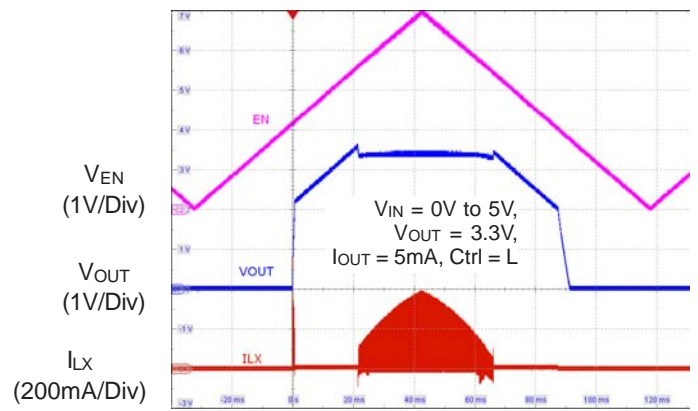
Time (600µs/Div)

Input Voltage Ramp Up/Down



Time (20ms/Div)

Input Voltage Ramp Up/Down



Time (20ms/Div)

Application Information

The RT5705 is a synchronous low voltage step-down converter that can support the input voltage range from 2.2V to 5.5V and the output current can be up to 1A. Internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection, over temperature protection, and short circuit protection.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be lockout.

Short Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly rate during a single switching cycle. A current runaway detector is used to monitor inductor current. After 3ms, the RT5705 restart operation and inductor current limit to current limit level.

Over-Temperature Protection

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds a threshold, the device stops operating. As soon as the IC temperature decreases below the threshold with a hysteresis, it starts operating again.

Protection Type	Threshold Refer to Electrical spec.	Protection Method	Shut Down Delay Time	Reset Method
OCP	$I_L > 1.5A$	Turn off high/low-side MOSFET	CL will trigger right away.	$I_L < 1.5A$
UVP	$V_{IN} < 2.1V$	Shutdown	100 μ s	$V_{IN} > 2.2V$
OTP	TEMP > 160°C	Shutdown	No delay	OTP Hysteresis = 20°C
SCP	$V_{OUT} < 0.7V$	Shutdown	No delay	After 3ms, restart and limit to I _{CL} level.

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic high, the device starts operation with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Output Voltage Setting

The RT5705 doesn't require an external resistor divider to program the output voltage. The device by the pins VSEL 1-4. The RT5705 supports an output voltage range of 1.8V to 3.3V in 100mV steps. The output voltage can be changed during operation and supports a simple dynamic output voltage scaling, shown .The output voltage is programmed according to Table 1.

100% Duty Cycle Operation

As the supply input voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-MOSFET and the inductor.

Power Good

The power good output is an open-drain output and needs to be connected to a voltage source with a pull-up 1M Ω resistor to avoid PGOOD floating.

The power good output can be used an indicator for system monitor IC status.

CTRL with Load Switch

The CTRL pin set to high, the LOAD pin is connected to the VOUT pin via an load switch and can power up an additional, provide sub-system used .

If CTRL pin is pulled to GND, the LOAD pin is disconnected from the VOUT pin and internally connected to GND by an internal discharge switch.

Inductor Selection

The recommended power inductor is 2.2μH with over 1.6A saturation current rating. In applications, need to select an inductor with the low DCR to provide good performance and efficiency.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f \times C_{OUT}} \right]$$

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature T_{J(MAX)}, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where T_{J(MAX)} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-12AL 3x2 package, the thermal resistance, θ_{JA}, is 31.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (31.5^\circ\text{C/W}) = 3.17\text{W for a WDFN-12AL 3x2 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed T_{J(MAX)} and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

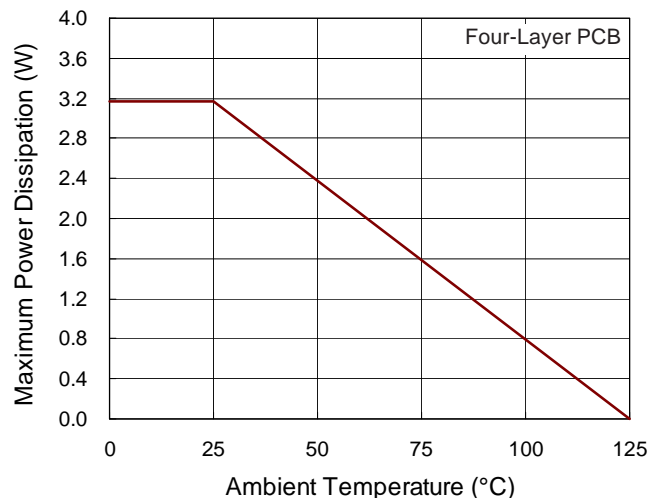


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

Some PCB layout guidelines for optimal performance of the RT5705 list as following.

Following figure shows the real PCB layout considerations and it is based on the real component size whose unit is millimeter (mm).

- ▶ The input capacitor should be placed as closed as possible to PVIN pin for good filtering.

- ▶ The high current path should be made as short and wide as possible.
- ▶ The inductor should be placed as close to LX1 and LX2 pin for reducing EMI.
- ▶ The output capacitor should be placed as closed as possible to PGND pin to ground plane to reduce noise coupling.

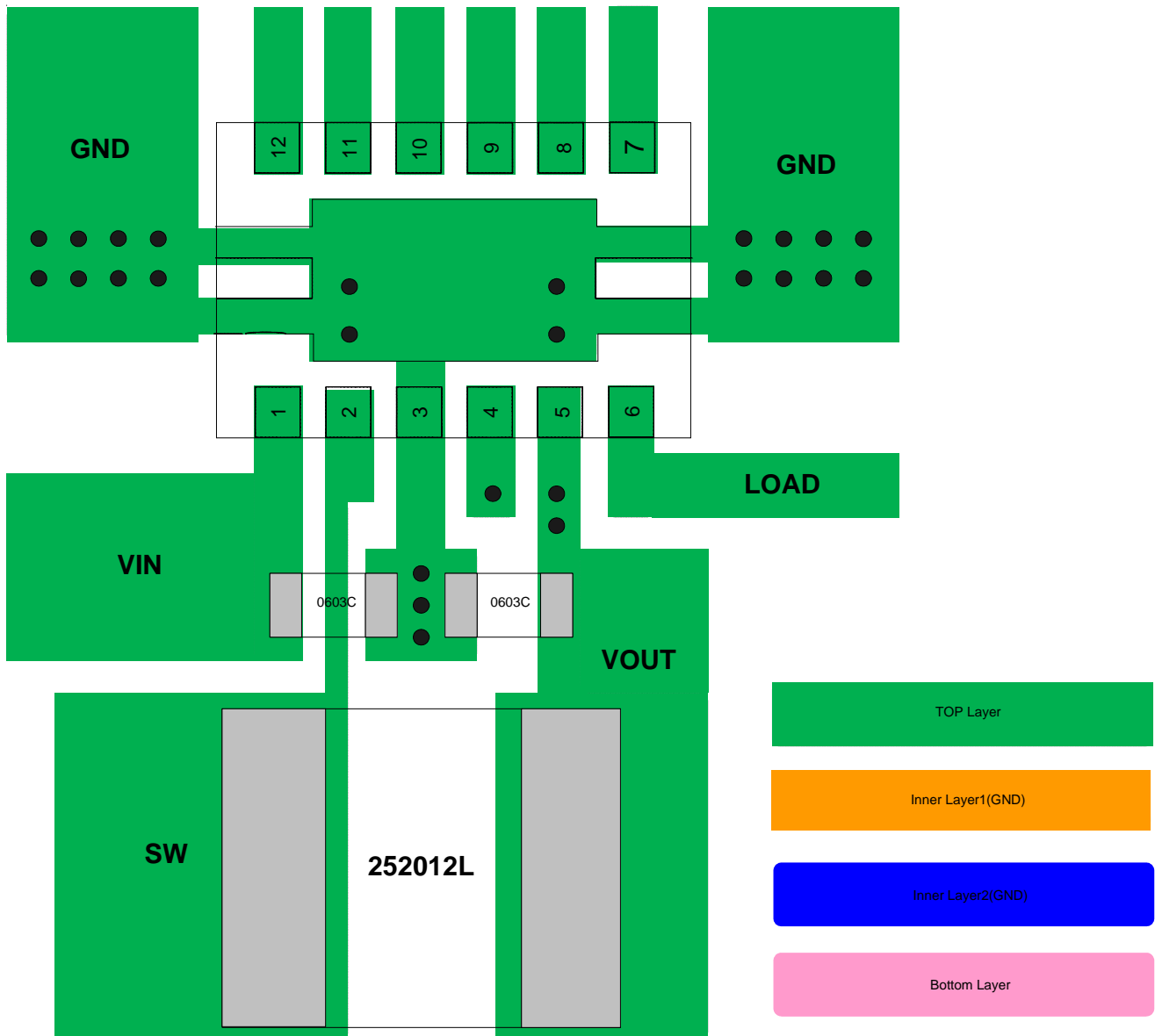
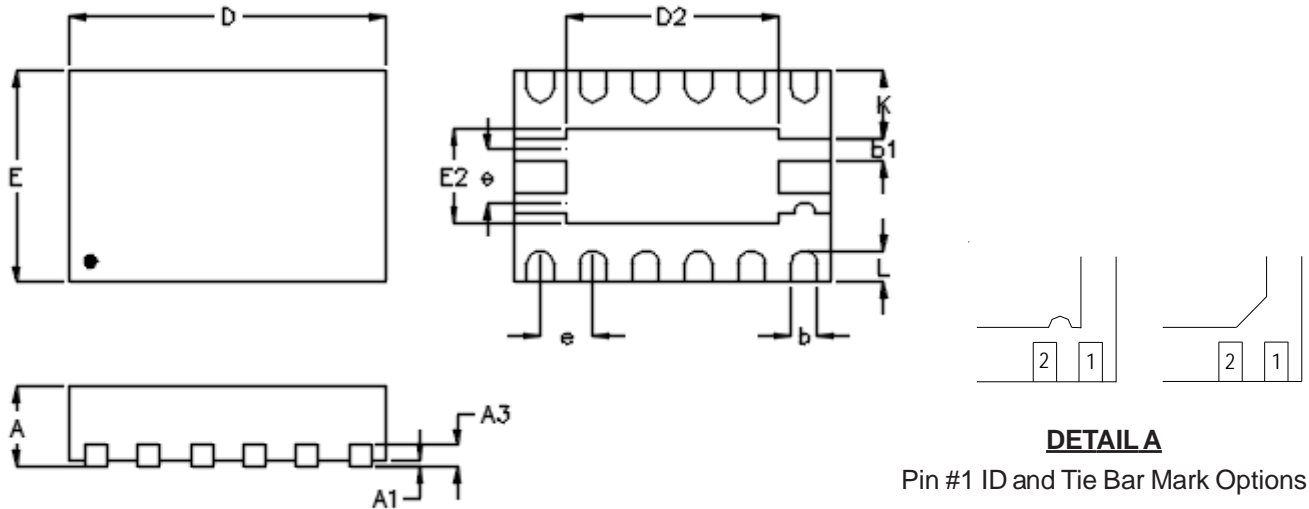


Figure 2. PCB Layout Guide

Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
b1	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	1.950	2.050	0.077	0.081
E	1.950	2.050	0.077	0.081
E2	0.850	0.950	0.033	0.037
e	0.500		0.020	
L	0.250	0.350	0.010	0.014
K	0.650		0.026	

W-Type 12AL DFN 3x2 Package

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