RICHTEK® **RT6160A**

Low Quiescent, High Efficiency 3A Buck-Boost Converter with I²C Interface

1 General Description

The RT6160A is a high-efficiency, single inductor and Advanced Constant On-Time (ACOT®) monolithic synchronous Buck-Boost converter that can deliver up to 3A of output current from 2.2V to 5.5V. It can well regulate the digitally programmable output voltage from 2.025V to 5.2V, making it suitable for a wide range of input supply applications, regardless of whether the input voltage is lower, higher than, or even equal to the output voltage. The ACOT® control architecture features outstanding line/load transient response, seamless transition between buck and boost modes, and provides stable operation with small ceramic output capacitors without the need for complicated external compensation.

The RT6160A features an I²C interface, which allows for programmable output voltage, ultra-sonic mode control, soft-start slew-rate adjustment and device status monitoring. The target output voltage can also be switched through the external VSEL pin to perform dynamic voltage scaling (DVS), and the ramp-up slew-rate and ramp mode of DVS can also be set by configuring the related registers.

The RT6160A operates with automatic PFM and has a low quiescent current design of typically 2μA, maintaining high efficiency during light load operation.

At higher loads, the device automatically switches to a 2.2MHz fixed frequency control, which easily smooths out the switching ripple voltage with small package filtering elements. And the integrated low $R_{DS(ON)}$ power MOSFETs features excellent efficiency under heavy load conditions. In shutdown mode, the supply current is typically 0.1μA, excellent in reducing power consumption. PFM mode can be disabled if fixed frequency is desired. The RT6160A is available in a small WL-CSP-15B 1.4x2.3 (BSC) package.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

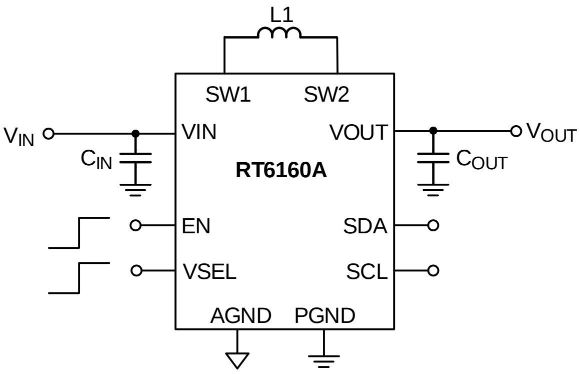
2 Features

- **Automatic Seamless Mode Transition with Real Buck, Buck-Boost and Boost Operation**
- **Input Voltage Range: 2.2V to 5.5V**
- **Output Voltage Range: 2.025V to 5.2V with Digitally Programmable (25mV/steps)**
- **Default Output Voltage Setting:**
  - **V_{OUT} = 3.3V at VSEL = L**
  - **V_{OUT} = 3.45V at VSEL = H**
- **Maximum Continuous Output Current:**
  - **Up to 2.5A for V_{IN} ≥ 2.5V, V_{OUT} = 3.3V**
  - **Up to 3A for V_{IN} ≥ 3V, V_{OUT} = 3.3V**
  - **Up to 2A for V_{IN} ≥ 3V, V_{OUT} = 5V**
- **Up to 95% Efficiency (V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{LOAD} = 1A)**
- **1μA Non-Switching Low Quiescent Current**
- **I²C Interface (Up to 1MHz)**
- **Allows Dynamically-Voltage-Scaling Control**
- **Automatic PFM Mode and Forced PWM Mode Selection**
- **Ultra-Sonic Mode Operation**
- **OCP, UVLO, OTP, OVP, UVP Protected Function for Robustness**
- **15-Ball WL-CSP Package**

3 Applications

- Smartphones and Tablets
- Portable Devices
- Wearable Devices
- System Pre-Regulators
- Point-of-Load Regulators
- Wifi Module
- USB VCONN Supplies
- TWS Earbud Chargers

4 Simplified Application Circuit



5 Ordering Information

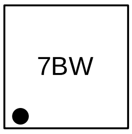
RT6160A □

Package Type
WSC: WL-CSP-15B 1.4x2.3 (BSC)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information



7B: Product Code
W: Date Code

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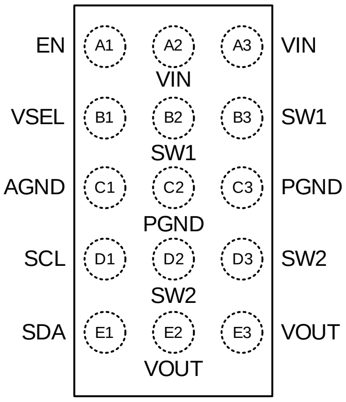
7 Pin Configuration

(TOP VIEW)

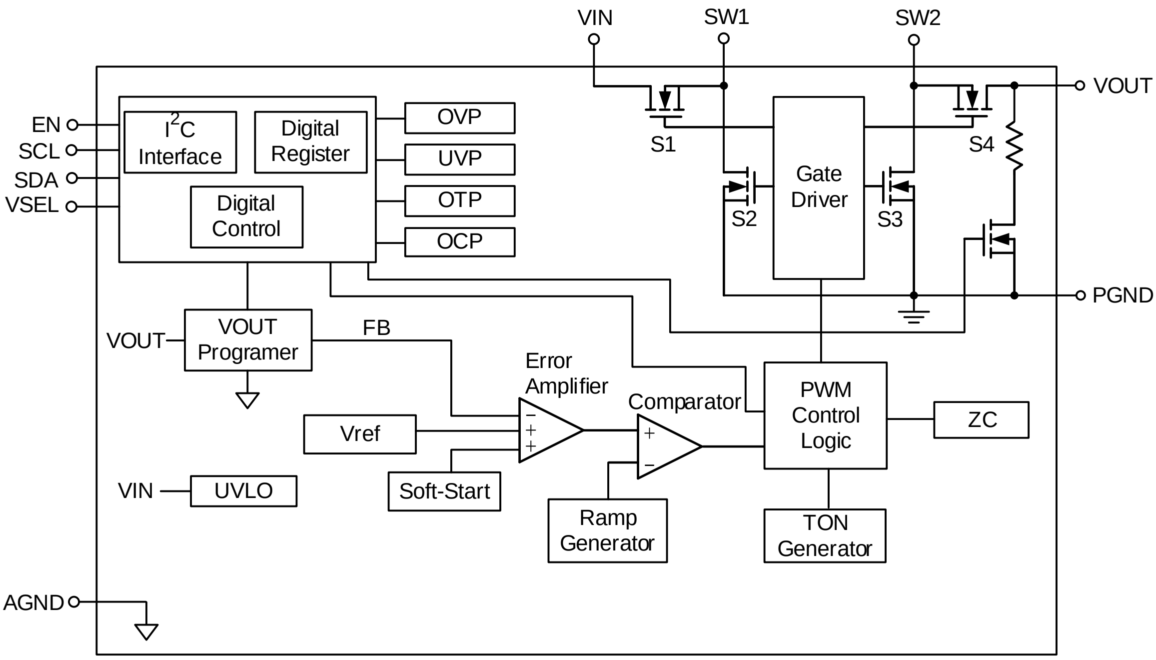


WL-CSP-15B 1.4x2.3 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
A2, A3	VIN	Power input. The input voltage range is from 2.2V to 5.5V after soft-start is finished. Connect input capacitors between this pin and PGND with minimal path. It is recommended to use a 10μF/6.3V/X5R/0402 and a 0.1μF/6.3V/X5R/0201 ceramic capacitors.
B1	VSEL	Voltage select pin. When this pin is tie to ground, V_{OUT} is set by the VOUT1 register; tie to logic-high, V_{OUT} is set by the VOUT2 register.
B2, B3	SW1	Switching node 1. Connect to the inductor.
C1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
C2, C3	PGND	Power ground. The low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
D1	SCL	I^2C serial interface clock. This pin requires a pull-up resistor to I^2C power supply.
D2, D3	SW2	Switching node 2. Connect to the inductor.
E1	SDA	I^2C serial interface data. This pin requires a pull-up resistor to I^2C power supply.
E2, E3	VOUT	Output voltage sense through this pin. Connect to output capacitor. It is recommended to use two 22μF/10V/X5R/0603 ceramic capacitors.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- Input Voltage, VIN ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to 6.2V
- Switch Node Voltage, SW1, SW2
  - DC ---------- –0.3V to 6V
  - AC (<50ns) ---------- –5V to 8.5V
- Other I/O Pins Voltages (EN, VSEL, SCL, SDA) ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WL-CSP-15B 1.4x2.3 (BSC) ---------- 1.88W
- Package Thermal Resistance (Note 2)
  - WL-CSP-15B 1.4x2.3 (BSC), θ_{JA} ---------- 53°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Input Voltage, V_{IN} ---------- 2.2V to 5.5V
- Output Voltage, V_{OUT} ---------- 2.025V to 5.2V
- Output Current, I_{OUT} ---------- 0A to 3A
- Input Capacitance, C_{IN} (Note 5) ---------- 5μF (Min.)
- Output Capacitance, C_{OUT} (Note 5) ---------- 16μF (Min.)
- Inductance, L ---------- 0.39μH to 0.56μH
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Effective capacitance after DC bias effects have been considered.

12 Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 3.3V, T_A = T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		2.2	--	5.5	V
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	2.11	2.14	2.19	V
Undervoltage Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	2.02	2.05	2.08	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}		--	90	--	mV
Quiescent Current (Switching Current)	I_{Q_SW}	V_{EN} = V_{IN} = 3.6V, I_{OUT} = 0A	--	3	6	μA
Quiescent Current (Non-Switching Current)	I_{Q_NSW}	V_{EN} = V_{IN} = 3.6V, I_{OUT} = 0A, not switching	--	2	4	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 3.6V	--	0.1	1	μA
High-Level Input Current	I_{IH}	VSCL = VSDA = VSEL = 1.8V, no pull-up resistor	--	--	0.1	μA
Low-Level Input Current	I_{IL}	VSCL = VSDA = VSEL = 0V, no pull-up resistor	--	--	0.1	μA
Input Bias Current	I_{BIAS}	V_{EN} = 0 to 5.5V	--	--	0.1	μA
High-Side MOSFET Leakage Current	I_{HS_LK}	V_{EN} = 0V, V_{SW} = 0V	--	1	--	μA
On-Resistance of High-side MOSFET	R_{DSON_H}		--	25	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}		--	38	--	mΩ
Output Discharge Resistor	R_{DISCHG}	V_{EN} = 0V	--	5	--	Ω
EN Input Voltage Rising threshold	V_{EN_R}	V_{IN} = 2.2V to 5.5V	1.2	--	--	V
EN Input Voltage Falling threshold	V_{EN_F}	V_{IN} = 2.2V to 5.5V	--	--	0.4	V
Input Voltage Logic-High (SCL, SDA, VSEL)	V_{IH}		1.2	--	--	V
Input Voltage Logic-Low (SCL, SDA, VSEL)	V_{IL}		--	--	0.4	V
Output Voltage Range	V_{OUT_RANGE}		2.025	--	5.2	V
Default Output Voltage (VSEL = L)	$V_{OUT\_SEL\_L}$	V_{SEL} = low	--	3.3	--	V
Default Output Voltage (VSEL = H)	$V_{OUT\_SEL\_L}$	V_{SEL} = high	--	3.45	--	V
Output Voltage Accuracy (FPWM)	$V_{OUT\_ACC\_FPWM}$	Forced PWM operation	−1	--	1	%
Output Voltage Accuracy (AUTO)	$V_{OUT\_ACC\_AUTO}$	Auto PFM operation	−1	--	3	%
Output Voltage Accuracy (USC)	$V_{OUT\_ACC\_USC}$	Ultra-Sonic operation	−1	--	3	%
Line Regulation	V_{LINE_REG}	(Note 6)	--	0.5	--	%
Load Regulation	V_{LOAD_REG}	(Note 6)	--	0.5	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Continuous Output Current	I_{MAX}	$V_{IN} \geq 2.5V$, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF (Note 7)	2.5	--	--	A
		$V_{IN} \geq 3V$, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF (Note 7)	3	--	--	
High-Side Switch (Peak) Current Limit	I_{LIM_H}	V_{IN} = 3.6V, V_{OUT} = 3.3V	4.5	5	5.5	A
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	V_{IN} = 3.6V, V_{OUT} = 3.3V	4	4.5	5	A
PFM to PWM Threshold Inductor Current	$I_{L\_T\_PFM}$	V_{IN} = 3.6V, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	0.3	--	A
Efficiency	η	V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Auto PFM operation	--	95	--	%
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Forced PWM operation	--	94	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Auto PFM operation	--	94	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Forced PWM operation	--	95	--	
Output Ripple Voltage	V_{OUT_RIPPLE}	V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Auto PFM operation (Note 6)	--	50	--	mV
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Forced PWM operation (Note 6)	--	20	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Auto PFM operation (Note 6)	--	25	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, Forced PWM operation (Note 6)	--	10	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Transient Response	V_{LOAD_TR}	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.05A to 1A, t_R = t_F = 1μs (Note 6)	–100	--	100	mV
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.05A to 0.5A, t_R = t_F = 1μs (Note 6)	–50	--	50	
Line Transient Response	V_{LINE_TR}	I_{OUT} = 1A, V_{IN} = 3V to 3.6V to 3V, t_R = t_F = 10μs (Note 6)	–50	--	50	mV
Switching Frequency	f_{SW}	Boost or Buck operation	--	2.2	--	MHz
Switching Frequency Range	f_{SW_RANGE}	Forced PWM operation, I_{OUT} = 100mA	0.5	--	3	MHz
Switching Frequency at Ultra-Sonic Mode	f_{SW_USC}	I_{OUT} = 1mA	30	--	--	kHz
Minimum On-Time	t_{ON_MIN}		20	--	60	ns
Minimum Off-Time	t_{OFF_MIN}		20	--	60	ns
Output Voltage Rising Time Turn-On Rise Time	t_R	Output voltage ramp to output voltage 95%, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	300	1000	μs
Enable Delay Time	t_{DLY_EN}	Enable pin logic-high to output voltage ramp, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	220	300	μs
VSEL Delay Time	t_{DLY_VSEL}	Delay between rising edge of V_{SEL} and start of DVS ramp	--	30	--	μs
Output Undervoltage Rising Threshold	V_{UVP_R}		--	95	--	%
Output Undervoltage Falling Threshold	V_{UVP_F}		--	90	--	%
Output Voltage Dynamic Voltage Scaling Slew Rate	DVS_{SR}	0x01, bit[1:0] = 00b	0.8	1	1.2	V/ms
		0x01, bit[1:0] = 01b	2	2.5	3	
		0x01, bit[1:0] = 10b	4	5	6	
		0x01, bit[1:0] = 11b	8	10	12	
Over-Temperature Protection Threshold	T_{OTP}	(Note 6)	140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	(Note 6)	--	20	--	°C

Note 6. Guaranteed by design.

Note 7. The device can sustain the maximum recommended output current, Users must verify that the thermal performance of the end application can support the maximum output current.

12.1 I²C Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Output Threshold Voltage (SCL, SDA, VSEL) SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
I²C Work Voltage SCL, SDA Low-Level Input Threshold Voltage	V_{IH_I2C}		--	1.8	--	V
Input Current Each IO Pin	I_{IN_I2C}		–10	--	10	μA
SDA Setup Time	$t_{SU;DAT}$		70	--	--	ns
SCL Clock Frequency	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	
		Fast mode plus	--	--	1000	
Bus Free Time between Stop and Start	t_{BUF}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard mode	0.1	--	--	ns
		Fast mode	0.1	--	--	
		Fast mode plus	0.1	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard mode	--	--	3.45	μs
		Fast mode	--	--	0.9	
		Fast mode plus	--	--	0.45	
SDA Setup Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
		Fast mode plus	50	--	--	
SCL Clock Low Period	t_{LOW}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock High Period	t_{HIGH}	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	

13 Typical Application Circuit

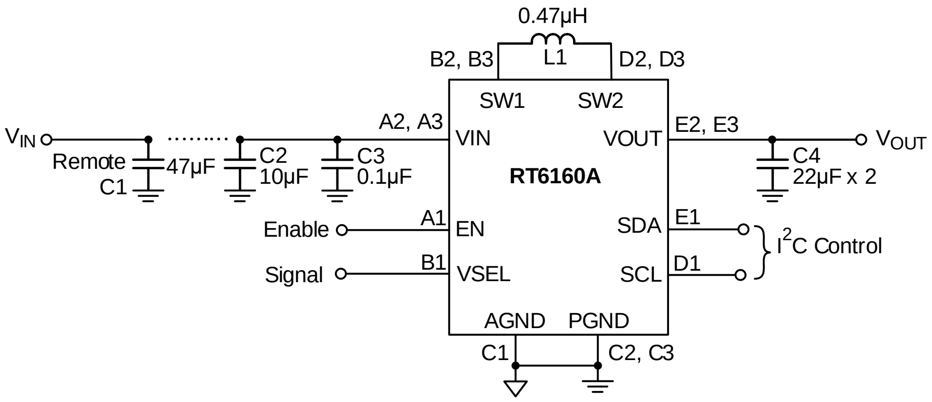


Table 1. Recommended Components Information (Note 8)

Reference	Part Number	Description	Package	Manufacturer
C1 (Note 9)	GRM32ER61C476KE15	47μF/16V/X5R	1210	Murata
C2	GRM155R60J106ME15	10μF/6.3V/X5R	0402	Murata
C3 (Note 10)	GRM033R60J104KE19	0.1μF/6.3V/X5R	0201	Murata
C4	GRM188R61A226ME15	22μF/10V/X5R	0603	Murata
L1	XFL4015-471MEC	0.47μH	4x4x1.5mm	Coilcraft

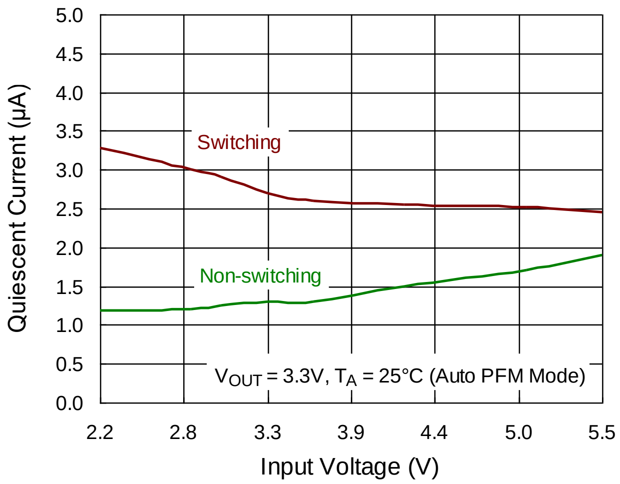
Note 8. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Note 9. The decoupling capacitor C1 is Remote C_{OUT} capacitor. C1 is optional. The device is designed to operate with a DC supply voltage in the range 2.2V to 5.5V. If the input supply is more than a few centimeters from the device, we recommend you add some bulk capacitance to the ceramic bypass capacitors. A 47μF electrolytic capacitor is a typical selection for the bulk capacitance.

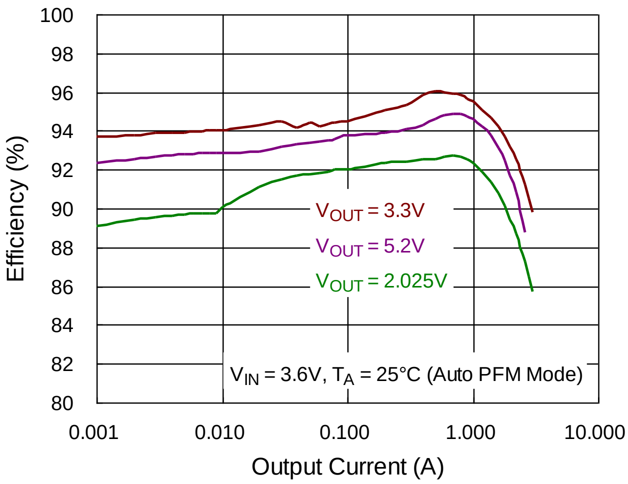
Note 10. The decoupling capacitor C3 is recommended to reduce any high frequency component on VIN bus. C3 is optional and used to filter any high frequency component on VIN bus.

14 Typical Operating Characteristics

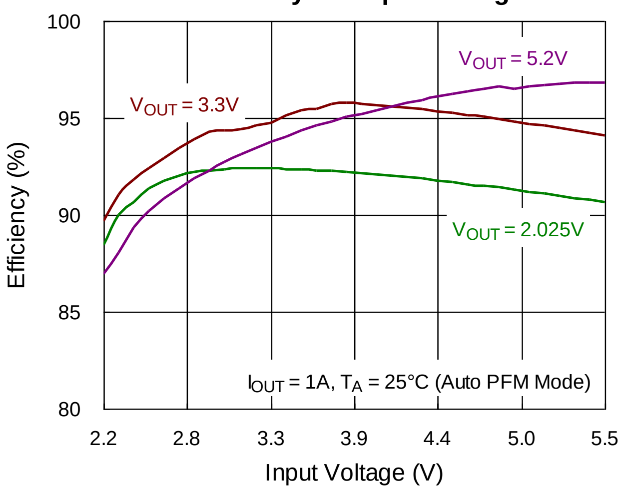
Quiescent Current vs. Input Voltage



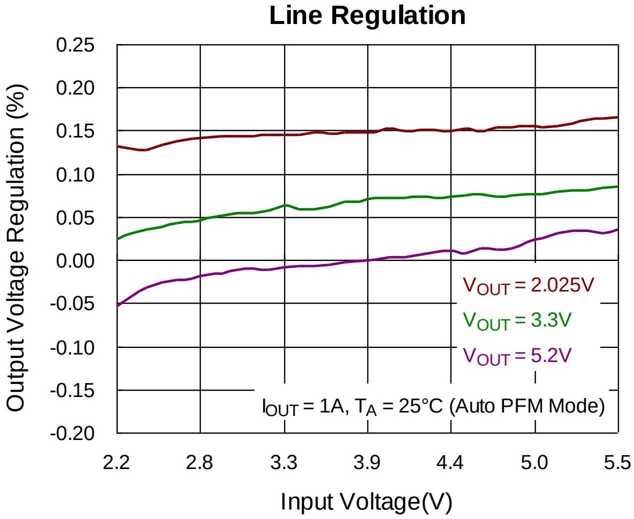
Efficiency vs. Output Current



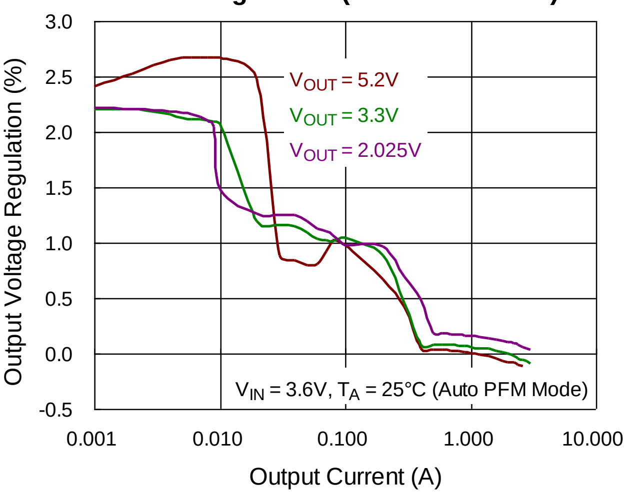
Efficiency vs. Input Voltage



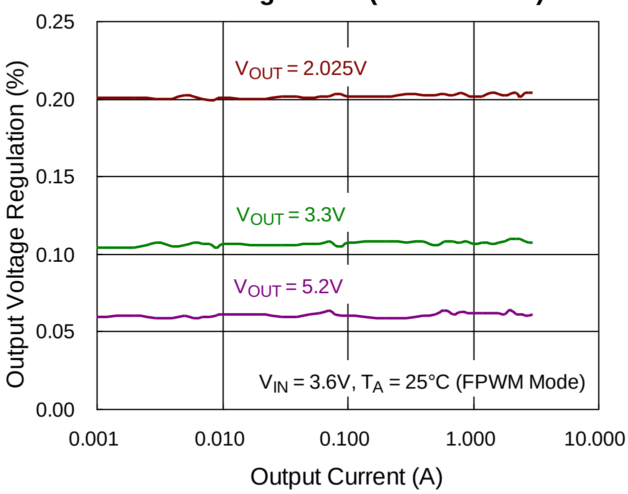
Line Regulation



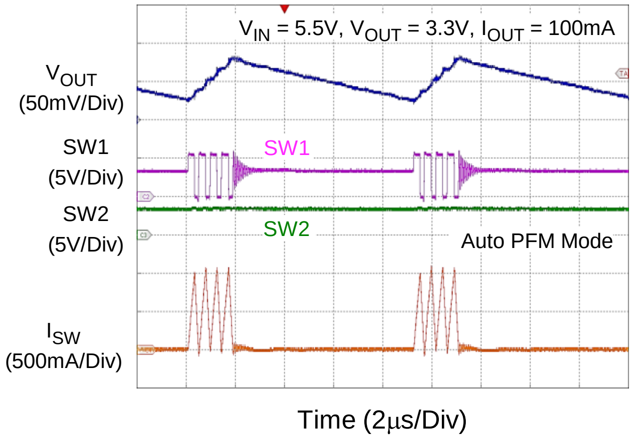
Load Regulation (Auto PFM Mode)



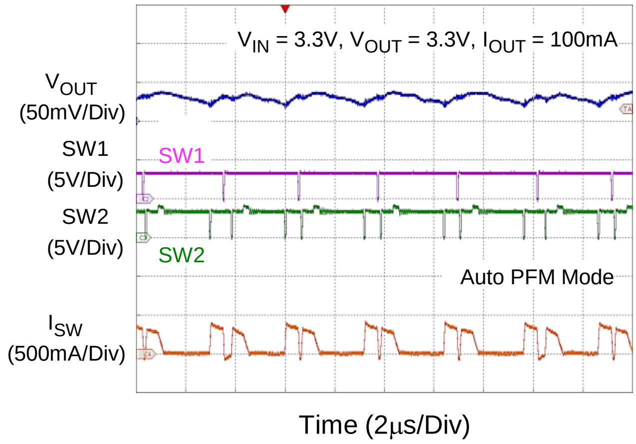
Load Regulation (FPWM Mode)



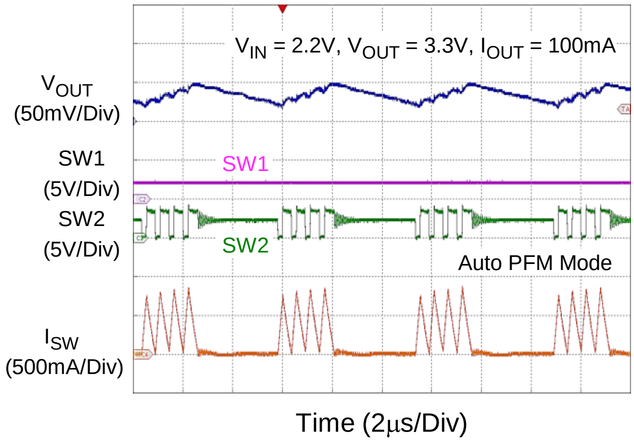
PFM Switching Waveforms (Buck Operation)



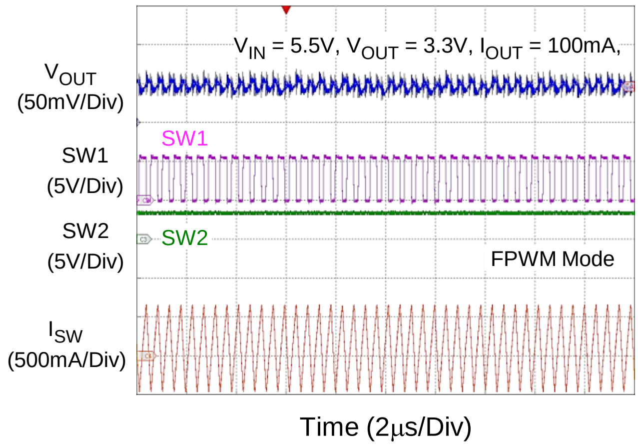
PFM Switching Waveforms (Buck-Boost Operation)



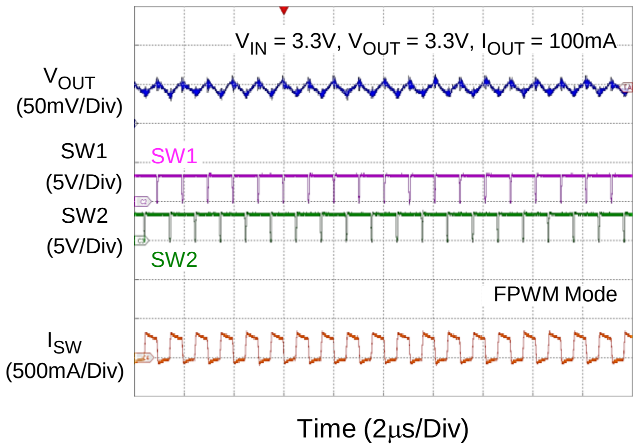
PFM Switching Waveforms (Boost Operation)



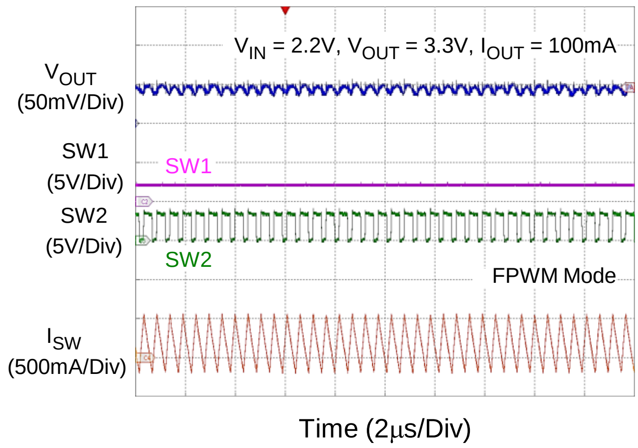
PWM Switching Waveforms (Buck Operation)



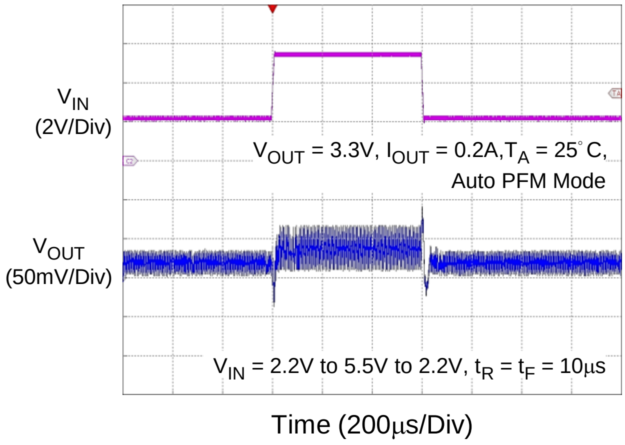
PWM Switching Waveforms (Buck-Boost Operation)



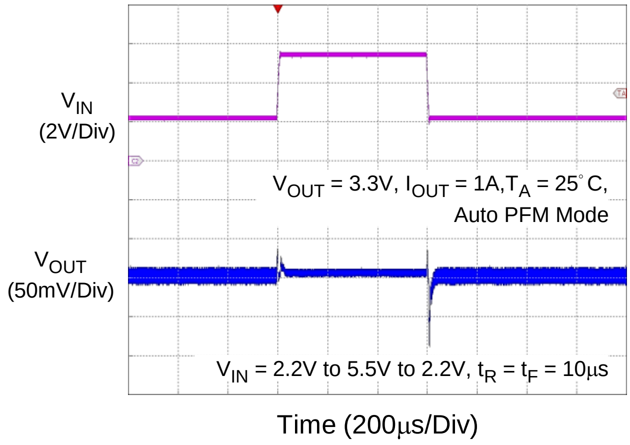
PWM Switching Waveforms (Boost Operation)



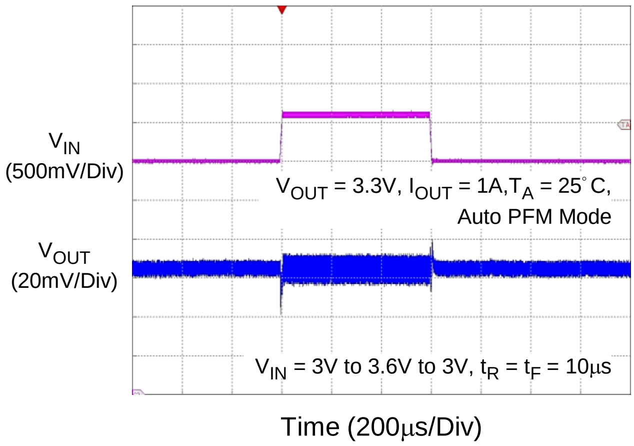
Line Transient Response (Light Load)



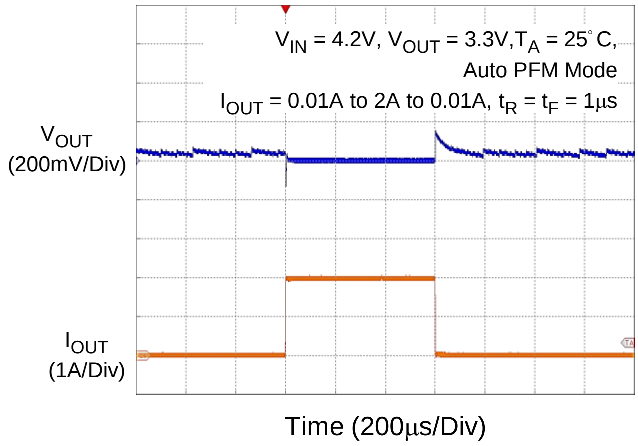
Line Transient Response (Heavy Load)



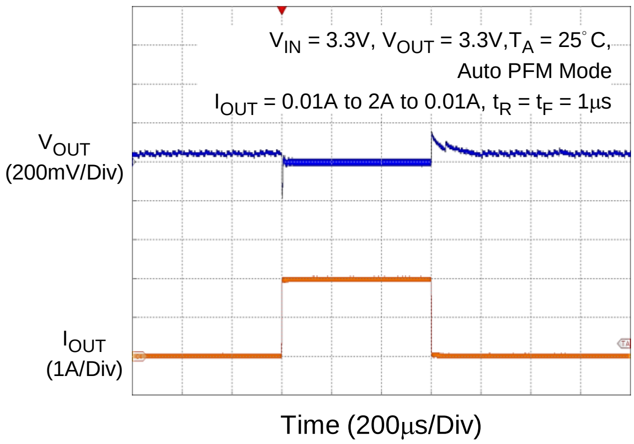
Line Transient Response (SPEC Condition)



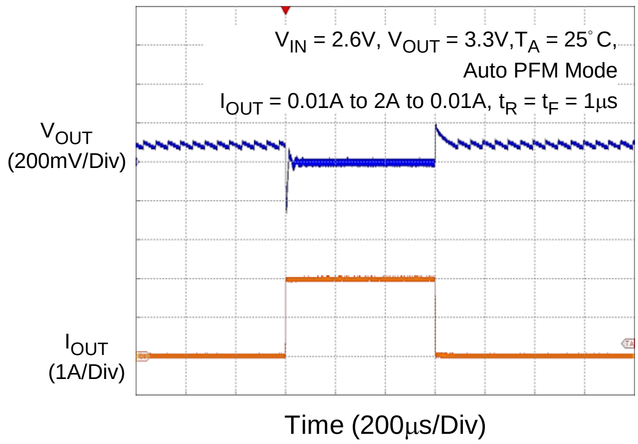
Load Transient Response (Buck)



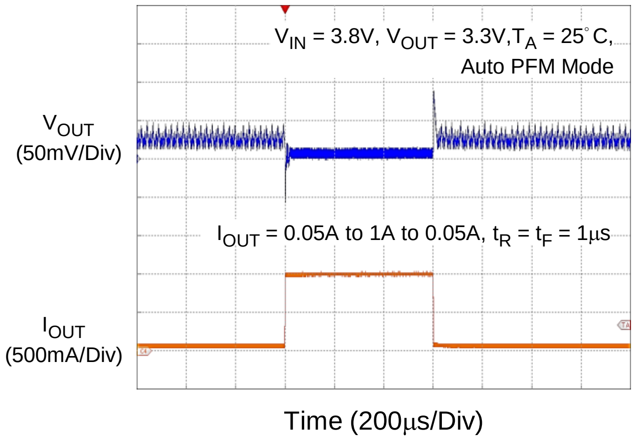
Load Transient Response (Buck-Boost)



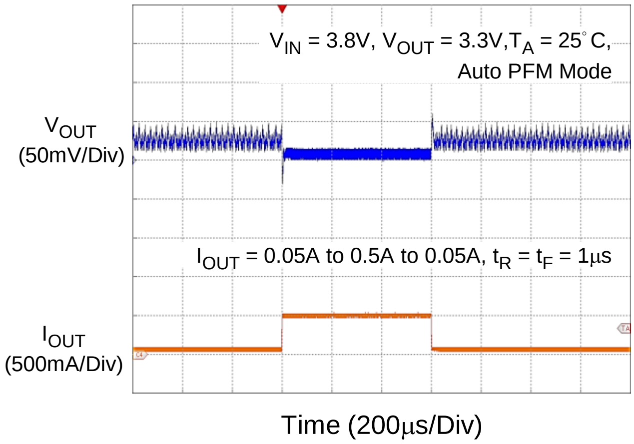
Load Transient Response (Boost)



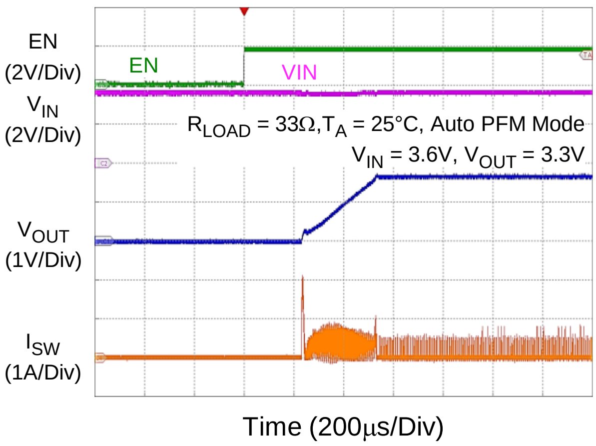
Load Transient Response (SPEC Condition1)



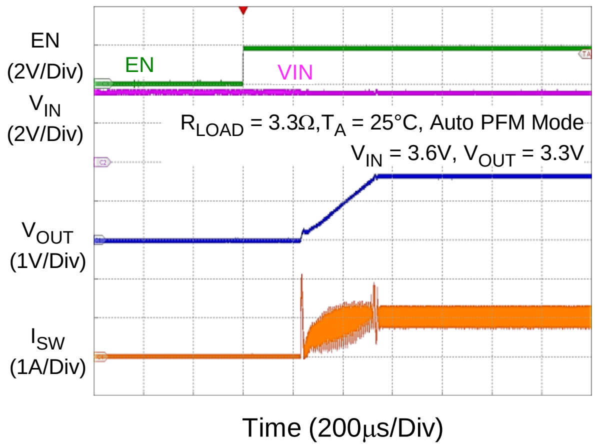
Load Transient Response (SPEC Condition2)



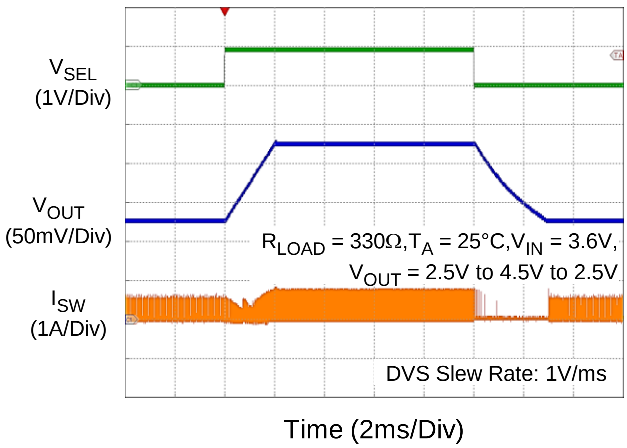
Start-Up Waveforms (Light Load)



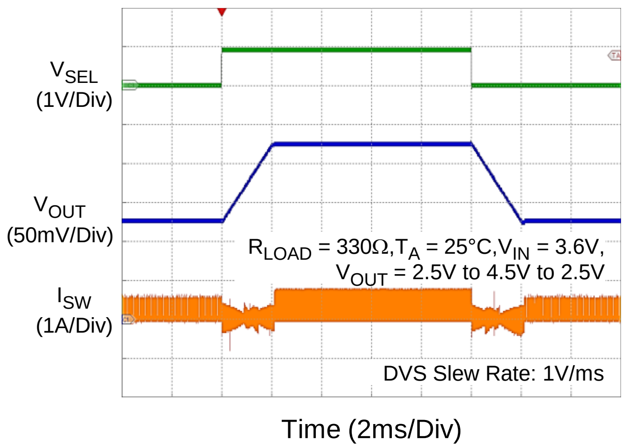
Start-Up Waveforms (Heavy Load)



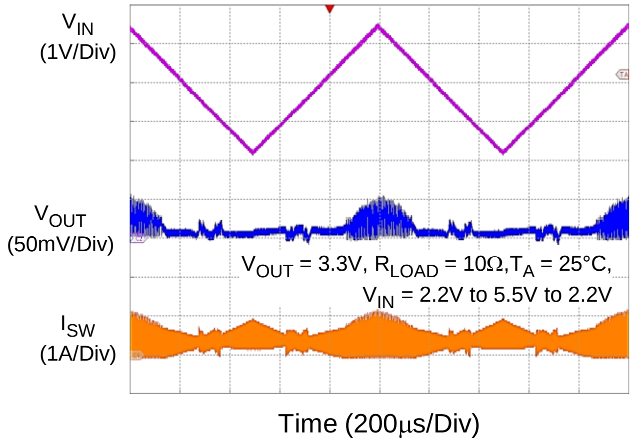
Dynamic Voltage Scaling (RPWM Function Disable)



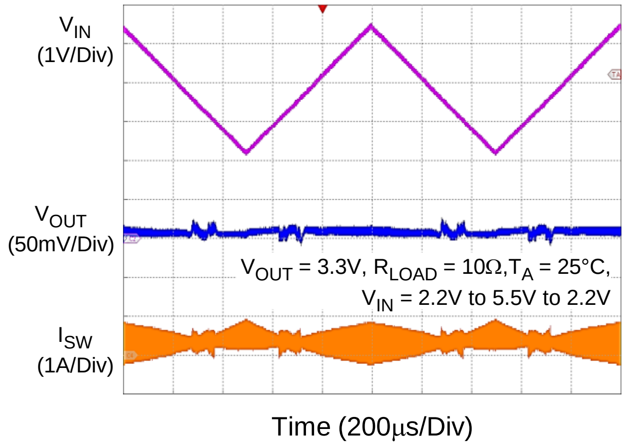
Dynamic Voltage Scaling (RPWM Function Enable)



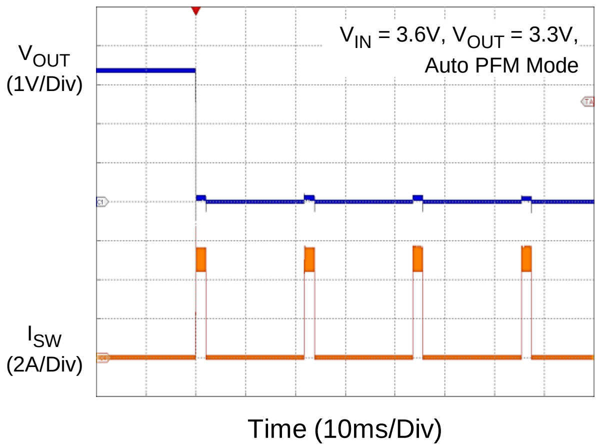
Line Sweep (Auto PFM Mode)



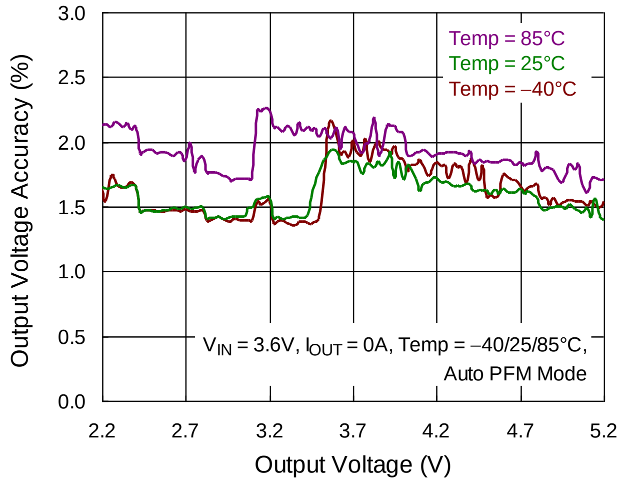
Line Sweep (FPWM Mode)



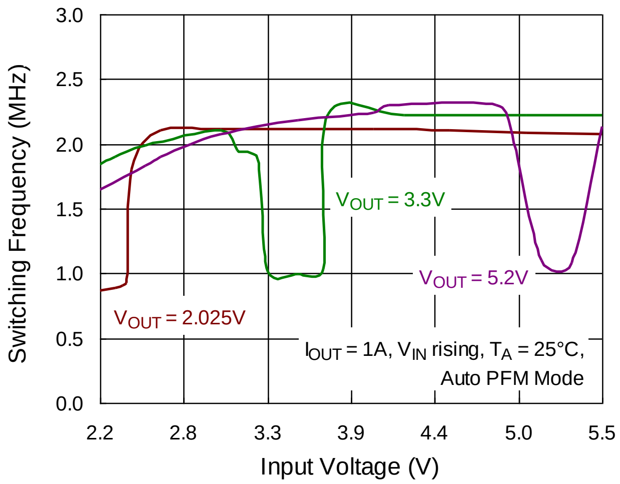
Output Short-Circuit Behavior



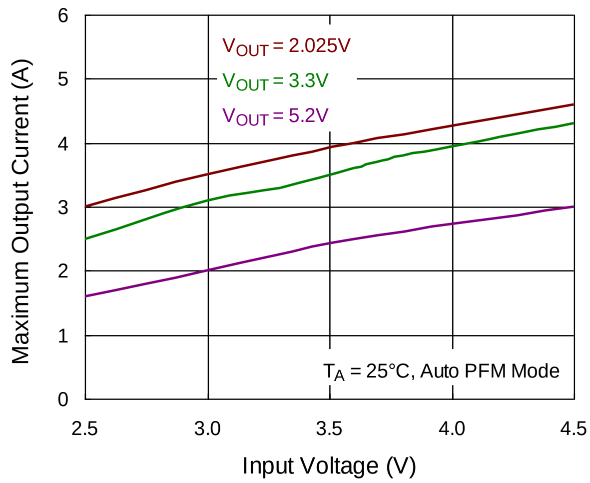
Output Voltage Accuracy



Switching Frequency vs. Input Voltage



Maximum Output Current vs. Input Voltage



15 Operation

The RT6160A utilizes a high-efficiency, single-inductor, Advanced Constant On-Time (ACOT®) mode control mechanism designed to achieve a fast transient response and good stability with low-ESR ceramic capacitors.

The ACOT® control scheme uses a virtual inductor current ramp generated inside the IC to replace the ramp normally provided by the output capacitor's ESR. The internal ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

15.1 Buck Operation

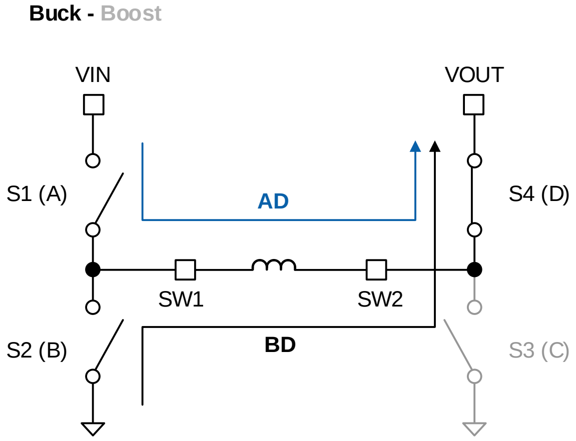


Figure 1. Buck Operation

When $V_{IN} > V_{OUT}$, the device operates like a buck converter. In steady-state buck-mode operation, the on-time pulse turns on the high-side switch S1, while S4 remains on, and the inductor current ramps up linearly. After the on-time period, the high-side switch S1 is turned off, and the synchronous rectifier switch S2 is turned on, while S4 remains on, and the inductor current ramps down linearly.

15.2 Boost Operation

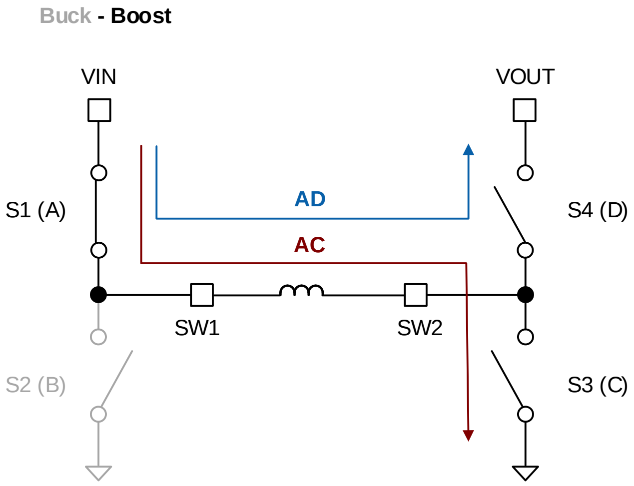


Figure 2. Boost Operation

When $V_{IN} < V_{OUT}$, the device operates like a boost converter. In boost mode at light load condition, the on-time pulse turns on the S3 switch for a constant on-time, while S1 remains on, and the inductor current ramps up linearly. After the on-time period, the S3 switch is turned off, and the synchronous rectifier switch S4 is turned on for a certain time, while S1 remains on, and the inductor current ramps down linearly. The S4 will turn off when inductor current drops to zero. As the loading current increases and the device operates in continuous-conduction mode (CCM), the switches are modulated to maintain the desired output voltage. When the feedback signal is less than the reference, the device turns switch S3 on, while S1 remains on, after the off-time one-shot is cleared and the inductor current ramps up linearly. Then the off-time one-shot turns S4 on, while S1 remains on, and the inductor current ramps down linearly.

15.3 Buck-Boost Operation

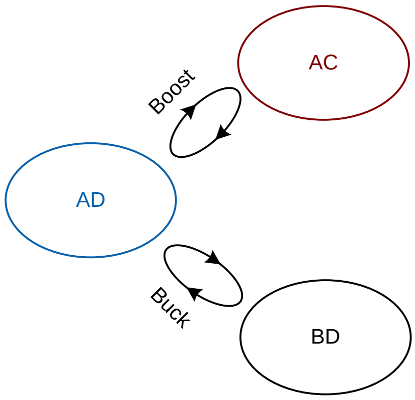


Figure 3. Buck-Boost Operation

When $V_{IN} \approx V_{OUT}$, all four transistors switch continuously, and the device operates in buck-boost mode. In buck-boost mode at light-load condition, the device turns switches S1 and S3 on, allowing the inductor current to increase linearly before reaching target peak-current level. When the inductor current reaches peak-current level, switches S1 and S4 are turned on for a constant time, allowing the inductor current to decrease linearly. Afterward, switches S2 and S4 are turned on to ensure the inductor will decrease to zero level. At light-load condition, the frequency increases as the loading increases. After the loading current is large enough, the converter will escape boundary-conduction mode and enter continuous-conduction mode. Furthermore, when V_{IN} is close to V_{OUT} in CCM, the switching frequency will decrease to half of the nominal switching frequency and the device will keep output voltage well-tracking as the target V_{OUT}.

16 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The basic RT6160A application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

16.1 Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. During the soft-start period, device sets $\overline{PG}$ to "1" until VOUT reach 99% of its setting voltage.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if

- The load current is large
- The output capacitance is large

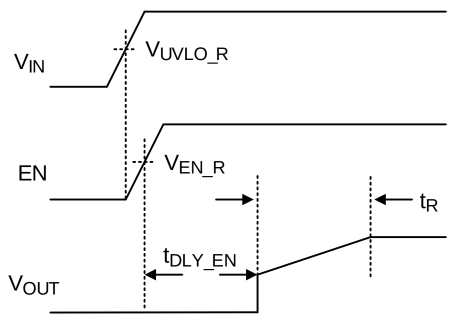


Figure 4. Soft-Start Sequence

16.2 Enable

The RT6160A provides an EN pin, as an external chip enable control, to enable or disable the device. If EN voltage is held below the logic-high threshold (V_{EN_R}), switching is inhibited, even if the VIN voltage is above UVLO rising threshold voltage (V_{UVLO_R}). If EN voltage is held below 0.4V, the converter will enter shutdown mode; in this state, the converter is disabled and all registers are reset to default value. During shutdown mode, the supply current can be reduced to I_{SHDN} (1μA or below). It's recommended that the VIN voltage should be higher than VIN rising threshold voltage (V_{UVLO_R}) first. Then, when the EN voltage rises above the logic-high threshold (V_{EN_R}), the device will turn on, enabling switching and initiating the soft-start sequence.

Note that there is a 100μs delay time to allow I^2C read/write operations when the EN pin goes above the logic-high threshold.

16.3 VSEL

- When VSEL = L, the default output voltage is 3.3V, which can be programmed via Address 0x04[6:0] in the VOUT1 register.
- When VSEL = H, the default output voltage is 3.45V, which can be programmed via Address 0x05[6:0] in the VOUT2 register.

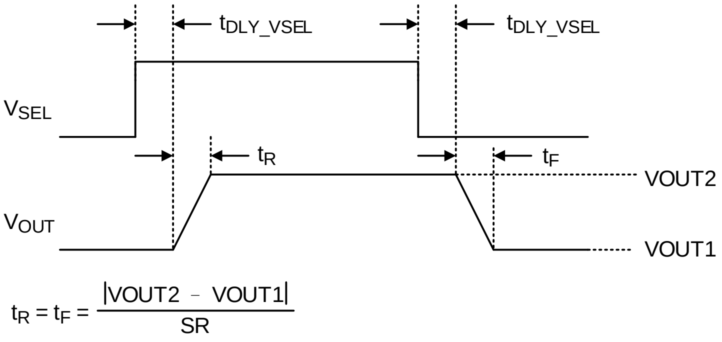


Figure 5. DVS Control the VSEL Pin

SR is the slew rate set by the (DVS Slew Rate) bits in the CONTROL register.

16.4 Auto PFM (Pulse Frequency Modulation) Mode

To save power and improve efficiency at low loads, the Buck/Boost operate in PFM (Pulse Frequency Modulation) mode as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When load increases and inductor current becomes continuous again, the Buck/Boost automatically goes back to PWM fixed frequency mode. Additionally, the RT6160A will enter DSLP (Deep Sleep) to achieve low input quiescent current at no load. Auto PFM Mode is the default mode.

16.5 FPWM (Forced Pulse Width Modulation) Mode

The switching frequency is forced into PWM mode operation. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM.

To enable Forced-PWM operation, set the FPWM bit in the Control register to 1.

16.6 Ultra-Sonic Mode

To avoid acoustic noise problem when operation, the switching frequency is designed to be always higher than 30kHz even there is no load at output.

To enable Ultra-Sonic Mode operation, set the Ultra-Sonic Mode bit in the Control register to 1.

16.7 Ramp-PWM Function

If Ramp-PWM function is enabled, the device operates in forced-PWM when it ramps from one output voltage to another during dynamic voltage scaling. This function is useful if you want the device to operate in Auto PFM Mode, but you want to make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in Auto PFM Mode and Ramp-PWM is disabled, the devices cannot always control the ramp from a higher output voltage to a lower output voltage, because in Automatic PFM/PWM Mode the devices cannot sink current.

To enable Ramp-PWM function, set the RAMP bit in the control register to 1.

To disable Ramp-PWM function, clear the RAMP bit in the control register to 0.

16.8 Dynamically Voltage Scaling Control

The RT6160A supports programmable slew-rate control feature for increasing and decreasing the output voltage, also known as Dynamically Voltage Scaling (DVS). The ramp slew-rate can be set to 1V/ms, 2.5V/ms, 5V/ms or 10V/ms through bit1 and bit0 of the control register. Moreover, the operation mode during DVS region can be adjusted through control register bit2. When the device operates in Auto PFM/PWM mode, if the bit2 is set to 1, the device will change to Forced PWM mode operation during DVS region and back to auto PFM/PWM mode after reaching target output voltage. And the device will keep auto PFM/PWM mode during DVS region if the bit2 of control register is set to 0.

16.9 Output Discharge

The device actively discharges the output when the EN pin is low.

16.10 V_{OUT} Selection

The RT6160A has programmable V_{OUT} from 2.025V to 5.2V with 25mV resolution.

The output voltage can be set by VOUTX register bit and the output voltage is given by the following equation:

V_{OUT} = 2.025V + VOUTX [6:0] x 25mV

For example:

if VOUTX [6:0] = 110011 (51 decimal), then

V_{OUT} = 2.025V + 51 x 25mV = 2.025V + 1.275V = 3.3V.

The RT6160A also has external VSEL pin to select VOUT1(0X04) or VOUT2(0X05). Pulling VSEL to high is for VOUT2 and pulling VSEL to low is for VOUT1.

Upon POR, VOUT1, and VOUT2 are reset to their default voltages.

16.11 Power-Good Comparator

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 if you read the Status register when a power-good condition exists.

16.12 Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW1 and SW2 waveform to adjust the zero current threshold voltage. When the current of low side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to achieve better efficiency.

16.13 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

16.14 PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominal 2.2MHz.

16.15 Inductor Selection

Choosing an inductor value will affect transient response, ripple, and other performance aspects. The RT6160A recommends a nominal inductance value of 0.47μH to achieve optimal performance.

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L which is I_{MAX} multiplied by 0.3 will be a reasonable starting point.

The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

16.16 Input Capacitor Selection

Steady state and transient response operation performance also depend on input voltage stability or not. The RT6160A at least a 10μF input capacitor is recommended to prevent input voltage instability with application operation.

It is recommended that the capacitor be placed as close as possible to the VIN and GND pins of the IC. If the input supply is located more than a few centimeters from the device, adding some bulk capacitance to the ceramic bypass capacitors is recommended.

A 47μF electrolytic capacitor is a typical selection for the bulk capacitance.

16.17 Output Capacitor Selection

The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor.

The output capacitor is selected based on the output ripple, which is calculated using the equation below:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT_{CAP}}$$

$$\Delta V_{ESR} = I_{C_{RMS}} \times R_{C_{ESR}}$$

$$\Delta V_{OUT_{CAP}} = \frac{I_{OUT} \times Duty}{f_{SW} \times C_{MIN}}$$

User can choose a capacitor using the equation to meet the system's ripple specifications. It is recommended to use at least two 22μF capacitors to match the application's requirements for VOUT ripple and stability performance.

Table 2. Protection Trigger Condition and Behavior

The RT6160A features some protections, such as OCP, OVP, UVLO, OTP and UVP. As the table shown, it is described the protection actions.

Protection Type	Threshold Refer to Electrical Spec.	Deglitch Time	Protection Method	Reset Method
OCP (Note 11)	I_L > 5A	0	Turn off Boost LG or Turn off Buck UG	I_L < 4.5A
UVLO	V_{IN} < 2.08V (max.)	0	Turn off all	V_{IN} > 2.17V (max.)
OTP	TEMP > 150°C	0	Turn off all	OTP Hysteresis = 20°C
OVP	V_{OUT} > 6V	0	Turn off all	V_{OUT} < 5.6V
UVP	V_{OUT} < 0.9 x V_{OUT_Target}	2ms	Turn off all	V_{OUT} > 0.95 x V_{OUT_Target}

Note 11. Turn off all switches when OCP event occurs and is continuing for 2ms.

16.18 Overcurrent Protection

The OCP function is implemented by UGATE and LGATE. When the inductor current reaches the UGATE current limit threshold, the high-side MOSFET will be turned-off. The low-side MOSFET turns on to discharge the inductor current until the inductor current trips below the LGATE current limit threshold. After UGATE current limit triggered, the max inductor current is decided by the inductor current rising rate and the response delay time of the internal network.

16.19 Input UVLO Protection

In addition to the EN pin, the RT6160A also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the V_{IN} voltage rises above V_{UVLO_R}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the V_{IN} voltage goes below the UVLO falling threshold voltage (V_{UVLO_F}), this switching will be inhibited; if V_{IN} voltage rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume switching.

16.20 Over-Temperature Protection

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will automatically resume switching. When the device detects an over-temperature condition, it sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 if you read the Status register when the junction temperature of the device is less than 130°C.

16.21 Overvoltage Protection

When the VOUT pin is floating, the device will trigger overvoltage protection to prevent the output voltage from exceeding critical values. If the output reaches the OVP threshold, the device will regulate the voltage to maintain it at this threshold value.

16.22 Undervoltage Protection

The RT6160A provides Hiccup Mode for Undervoltage Protection (UVP). When the V_{OUT} voltage drops below 90% of Target V_{OUT}, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT6160A will retry to build up output voltage automatically. When the UVP condition is removed, the converter will soft-start to target voltage and resume normal operation.

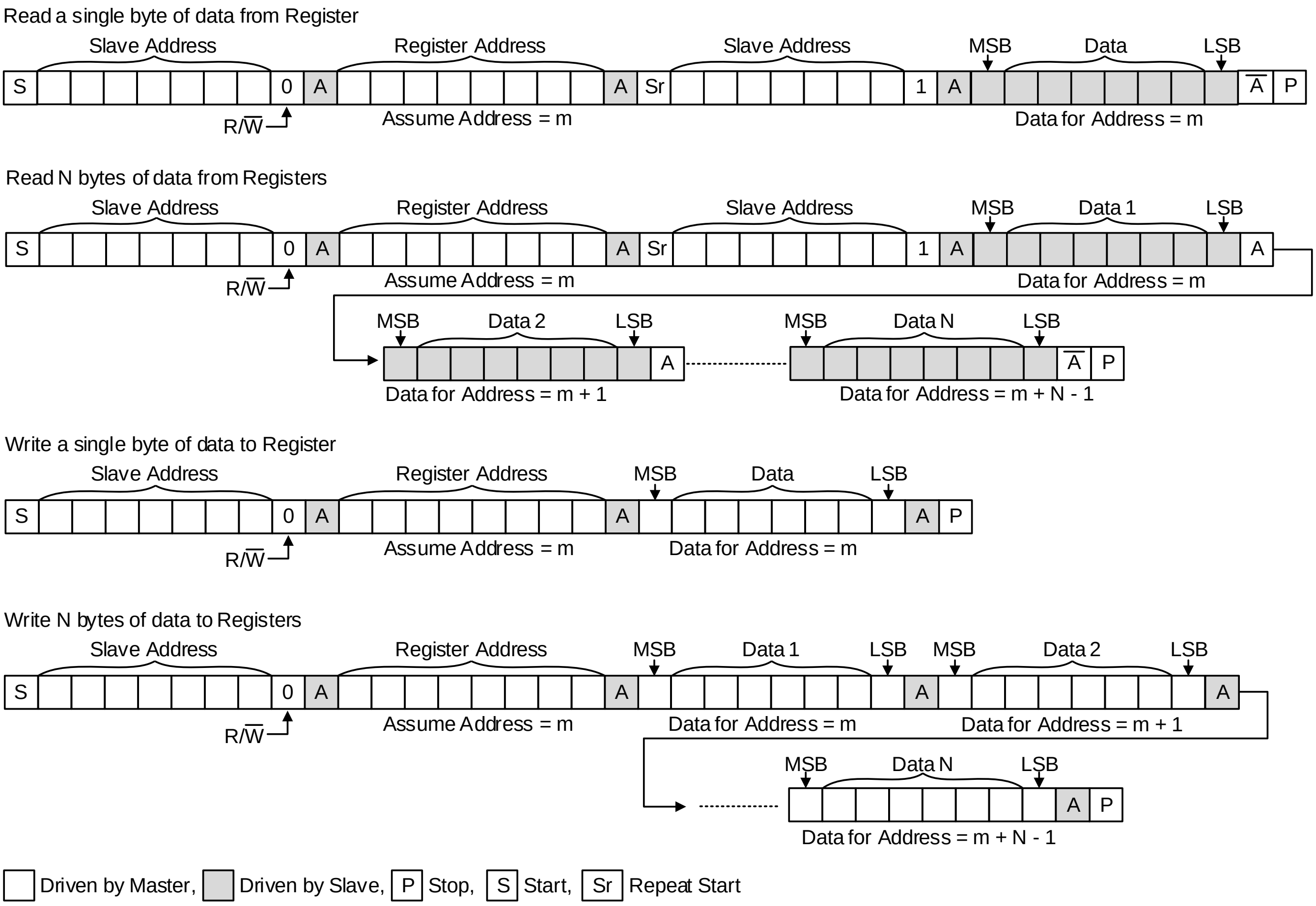
16.23 I²C Interface

The following table shows the RT6160A slave address 0x75(7bit).

RT6160A I²C Slave Address (75H)			
MSB	LSB	R/W bit	R/W
111010	1	1/0	EB/EA

The I²C interface bus must be connect a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.

16.23.1 Read and Write Function



16.23.2 I²C Waveform Information

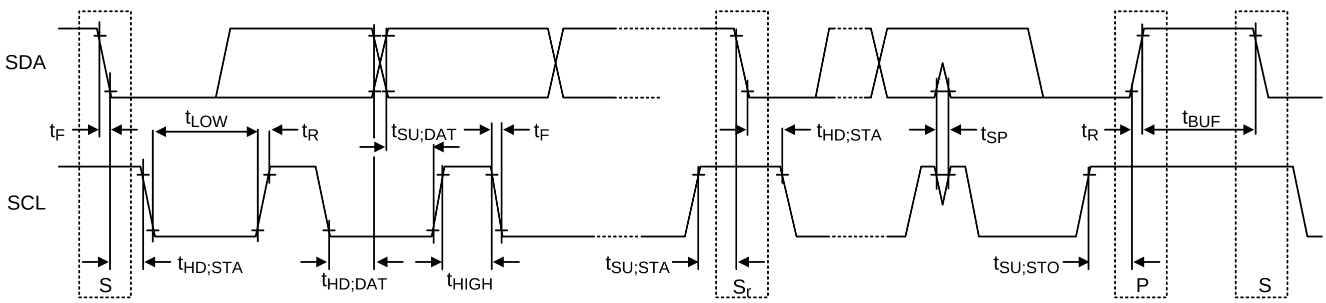


Figure 6. I²C Read and Write Stream and Timing Diagram

16.24 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-15B 1.4x2.3 (BSC) package, the thermal

resistance, θ_{JA}, is 53°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (53°C/W) = 1.88W for a WL-CSP-15B 1.4x2.3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

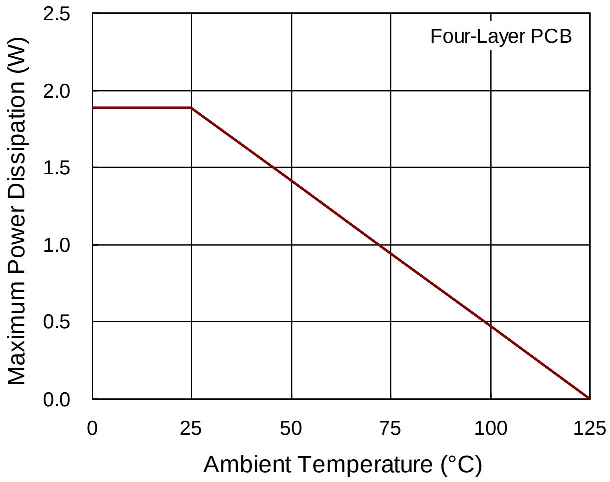


Figure 7. Derating Curve of Maximum Power Dissipation

16.25 Layout Considerations

For the best performance of the RT6160A, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to IC to minimize the power loop area. A typical 0.1μF decoupling capacitor is recommended to reduce power loop area and any high frequency component on VIN.
- Switching node (SW1 and SW2) are with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW1 and SW2 node to prevent stray capacitive noise pickup.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2^{nd} GND plate through top to 2^{nd} via.

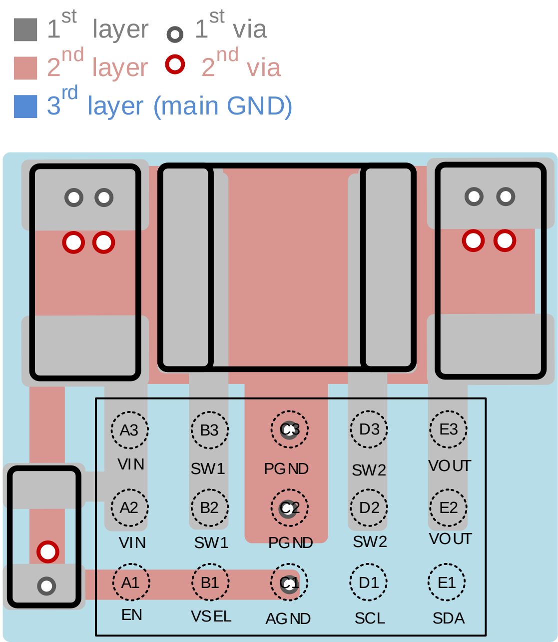


Figure 8. Layout Guide

1. The loop from VIN to CIN to PGND should be as short as possible to reduce the switching noise of Buck mode.
2. The loop from VOUT to COUT to PGND should be as short as possible to reduce the switching noise of Boost mode.
3. The loop from VIN to AGND should separate with PGND loop for noise reducing.
4. Connect AGND to C3 or C2 directly to reduce the noise.

17 Functional Register Description

17.1 Register Table Lists

Name	Address	Description
CONTROL	0x01	Output pull-down slew rate control MODE function control DVS slew rate function control
STATUS	0x02	Read IC status
DEVID	0x03	Device Identity
VOUT1	0x04	Output Voltage 1 when the VSEL pin is low
VOUT2	0x05	Output Voltage 2 when the VSEL pin is High

17.2 Register Description

I^2C Slave address = 1110101 (75H)

I^2C Register Map

R: Read Only

RW: Read and Write

Address 0x01	CONTROL							
Bits	7	6	5	4	3	2	1	0
Name	Reserved	I^2C_SDA_SLEW		Ultra-Sonic Mode	Forced PWM	Ramp PWM	DVS Slew Rate	
Reset	0	0	0	0	0	0	0	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address 0x02	STATUS							
Bits	7	6	5	4	3	2	1	0
Name	Reserved			HD	UV	OC	TSD	$\overline{PG}$
Reset	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R
Address 0x03	DEVID							
Bits	7	6	5	4	3	2	1	0
Name	Manufacturer				Major		Minor	
Reset	1	0	1	0	1	0	0	0
Type	R	R	R	R	R	R	R	R
Address 0x04	VOUT1							
Bits	7	6	5	4	3	2	1	0
Name	Reserved	VOUT1						
Reset	0	0	1	1	0	0	1	1
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address 0x05	VOUT2							
Bits	7	6	5	4	3	2	1	0
Name	Reserved	VOUT2						
Reset	0	0	1	1	1	0	0	1
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address	Register Name	Bit	Bit Name	Default	Type	Description
0x01	CONTROL	7	Reserved	0	R	Reserved
		6:5	I^2C_SDA_SLEW	00	R/W	SDA pin output pull-down slew rate 00: High (default) 01: Medium 10: Low 11: Very low
		4	Ultra-Sonic Mode	0	R/W	This bit controls the ultra-sonic mode function. 0: Ultra-Sonic mode disabled (default) 1: Ultra-Sonic mode enabled
		3	Forced PWM	0	R/W	This bit controls the forced-PWM mode function. 0: Forced PWM operation disabled (default) 1: Forced PWM operation enabled
		2	Ramp PWM	0	R/W	This bit controls the ramp-PWM function. 0: Ramp-PWM operation disabled (default) 1: Ramp-PWM operation enabled
		1:0	DVS Slew Rate	00	R/W	These bits control the slew rate of the DVS function. 00: 1.0V/ms (default) 01: 2.5V/ms 10: 5.0V/ms 11: 10.0V/ms

Address	Register Name	Bit	Bit Name	Default	Type	Description
0x02	STATUS	7:5	Reserved	000	R	Reserved
		4	HD	0	R	This bit shows the status of the hot-die function. 0: Normal operation (default) 1: An hot-die event was detected
		3	UV	0	R	This bit shows the status of the undervoltage function. 0: Normal operation (default) 1: An undervoltage event was detected
		2	OC	0	R	This bit shows the status of the overcurrent function. 0: Normal operation (default) 1: An overcurrent event was detected
		1	TSD	0	R	This bit shows the status of the thermal shutdown function. 0: Temperature good (default) 1: An over-temperature event was detected
		0	$\overline{PG}$	0	R	This bit shows the status of the power-good comparator. 0: Power-good (default) 1: A power-not-good was detected

Address	Register Name	Bit	Bit Name	Default	Type	Description
0x03	DEVID	7:4	Manufacturer	1010	R	These bits identify the device manufacturer. 1010: Richtek (default)
		3:2	Major	10	R	These bits identify the major silicon revision. 00: A (initial silicon) 01: B (first major revision) 10: C (second major revision) (default) 11: D (third major revision)
		1:0	Minor	00	R	These bits identify the minor silicon revision. 00: 0 (initial silicon) (default) 01: 1 (first minor revision) 10: 2 (second minor revision) 11: 3 (third minor revision)
Address	**Register Name**	**Bit**	**Bit Name**	**Default**	**Type**	**Description**
0x04	VOUT1	7	Reserved	0	R	Reserved
		6:0	VOUT1	0110011	R/W	These bits set the output voltage when the VSEL pin is low. 0000000: V_{OUT} = 2.025V 0000001: V_{OUT} = 2.05V 0000010: V_{OUT} = 2.075V … 0110011: V_{OUT} = 3.3V (default) … 1111101: V_{OUT} = 5.15V 1111110: V_{OUT} = 5.175V 1111111: V_{OUT} = 5.2V
Address	**Register Name**	**Bit**	**Bit Name**	**Default**	**Type**	**Description**
0x05	VOUT2	7	Reserved	0	R	Reserved
		6:0	VOUT2	0111001	R/W	These bits set the output voltage when the VSEL pin is High. 0000000: V_{OUT} = 2.025V 0000001: V_{OUT} = 2.05V 0000010: V_{OUT} = 2.075V … 0111001: V_{OUT} = 3.45V (default) … 1111101: V_{OUT} = 5.15V 1111110: V_{OUT} = 5.175V 1111111: V_{OUT} = 5.2V

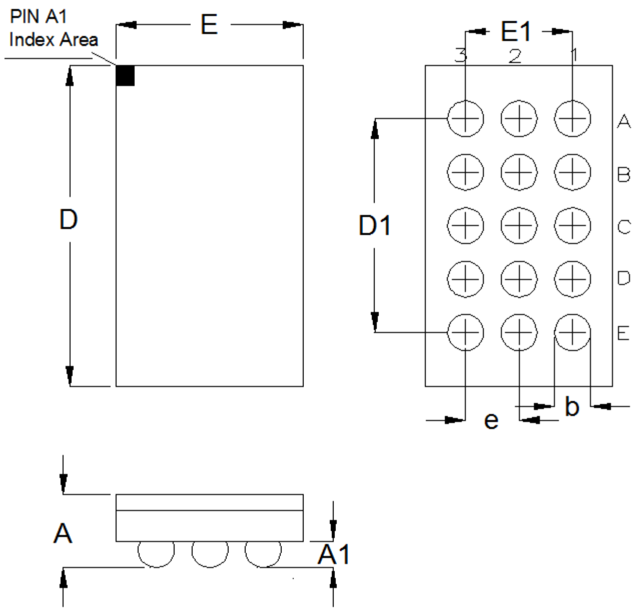
Table 3. Register VOUT1/VOUT2[6:0] vs. Output Voltage

VOUT1 Address = 0x04, Output Voltage 1 when the VSEL pin is low.

VOUT2 Address = 0x05, Output Voltage 2 when the VSEL pin is high.

Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)
0000000	2.025	0100000	2.825	1000000	3.625	1100000	4.425
0000001	2.05	0100001	2.85	1000001	3.65	1100001	4.45
0000010	2.075	0100010	2.875	1000010	3.675	1100010	4.475
0000011	2.1	0100011	2.9	1000011	3.7	1100011	4.5
0000100	2.125	0100100	2.925	1000100	3.725	1100100	4.525
0000101	2.15	0100101	2.95	1000101	3.75	1100101	4.55
0000110	2.175	0100110	2.975	1000110	3.775	1100110	4.575
0000111	2.2	0100111	3	1000111	3.8	1100111	4.6
0001000	2.225	0101000	3.025	1001000	3.825	1101000	4.625
0001001	2.25	0101001	3.05	1001001	3.85	1101001	4.65
0001010	2.275	0101010	3.075	1001010	3.875	1101010	4.675
0001011	2.3	0101011	3.1	1001011	3.9	1101011	4.7
0001100	2.325	0101100	3.125	1001100	3.925	1101100	4.725
0001101	2.35	0101101	3.15	1001101	3.95	1101101	4.75
0001110	2.375	0101110	3.175	1001110	3.975	1101110	4.775
0001111	2.4	0101111	3.2	1001111	4	1101111	4.8
0010000	2.425	0110000	3.225	1010000	4.025	1110000	4.825
0010001	2.45	0110001	3.25	1010001	4.05	1110001	4.85
0010010	2.475	0110010	3.275	1010010	4.075	1110010	4.875
0010011	2.5	0110011	3.3	1010011	4.1	1110011	4.9
0010100	2.525	0110100	3.325	1010100	4.125	1110100	4.925
0010101	2.55	0110101	3.35	1010101	4.15	1110101	4.95
0010110	2.575	0110110	3.375	1010110	4.175	1110110	4.975
0010111	2.6	0110111	3.4	1010111	4.2	1110111	5
0011000	2.625	0111000	3.425	1011000	4.225	1111000	5.025
0011001	2.65	0111001	3.45	1011001	4.25	1111001	5.05
0011010	2.675	0111010	3.475	1011010	4.275	1111010	5.075
0011011	2.7	0111011	3.5	1011011	4.3	1111011	5.1
0011100	2.725	0111100	3.525	1011100	4.325	1111100	5.125
0011101	2.75	0111101	3.55	1011101	4.35	1111101	5.15
0011110	2.775	0111110	3.575	1011110	4.375	1111110	5.175
0011111	2.8	0111111	3.6	1011111	4.4	1111111	5.2

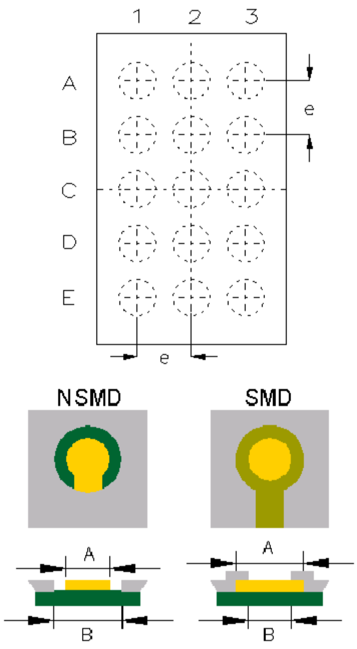
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.260	2.340	0.089	0.092
D1	1.600		0.063	
E	1.360	1.440	0.054	0.057
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.4x2.3 Package (BSC)

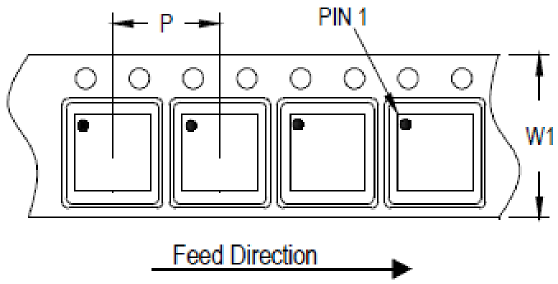
19 Footprint Information

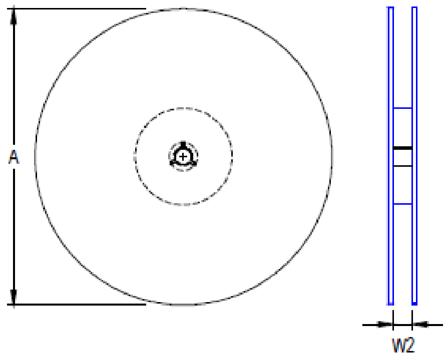


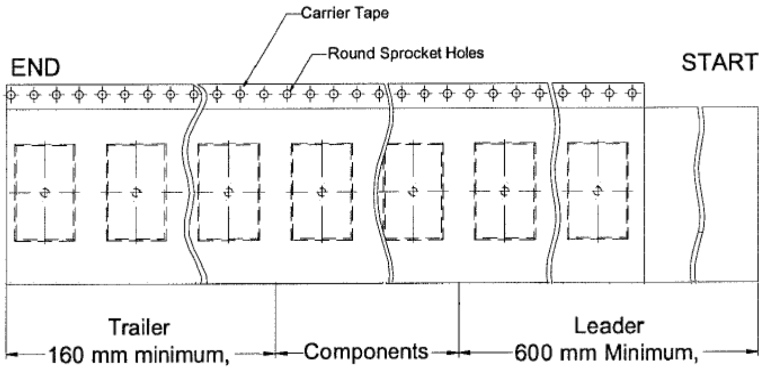
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.4x2.3-15(BSC)	15	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

20 Packing Information

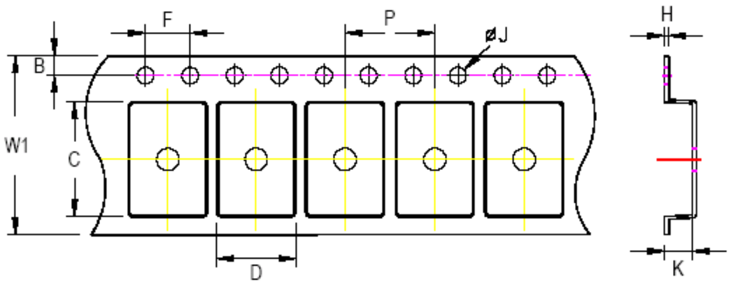
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.4x2.3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.4x2.3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
02	2023/7/7	Modify	Ordering Information on P2 Electrical Characteristics on P5 Note 3 on P9 Application Information on P16 Packing Information on P29, 30, 31
03	2024/4/10	Modify	General Description on P1 Simplified Application Circuit on P2 Pin Configuration on P4 Functional Pin Description on P4 Functional Block Diagram on P5 Absolute Maximum Ratings on P6 Electrical Characteristics on P7 to 11 Typical Application Circuit on P12 Typical Operating Characteristics on P14, 16, 17 Operation on P18, 19 Application Information on P20, 21, 22, 23, 24, 26, 27 Packing Information on P35