5V/12V Synchronous Buck PWM DC/DC Controller

General Description

The RT8105A is a synchronous buck PWM controller with embedded MOSFET gate drivers. This part operates with 5V/12V supply voltage, has fixed 300kHz switching frequency, and utilizes voltage mode control. The feedback control loop is compensated internally to simplify the converter design.

The RT8105A provides enable/disable function to support power sequence control. This device also provides full fault protection functions to protect the load. This part uses lossless low side MOSFET $R_{DS(ON)}$ current sense technique for over current protection with adjustable threshold. Other features include internal soft-start and V_{IN} detection function.

Ordering Information

RT8105A □ □

- Package Type
  S : SOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

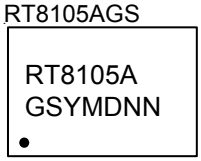
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

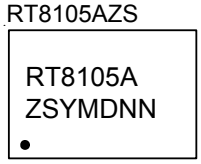
Marking Information

RT8105AGS



RT8105AGS : Product Number
YMDNN : Date Code

RT8105AZS



RT8105AZS : Product Number
YMDNN : Date Code

Features

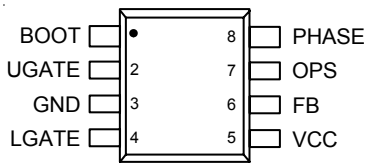
- **5V or 12V Supply Voltage**
- **Embedded Non-Overlapping N-MOSFET Driver**
- **300kHz Fixed Switching Frequency**
- **Internal Control Loop Compensation**
- **Enable/Disable Control**
- **Full 0 to 100% Duty Ratio**
- **Low Side MOSFET $R_{DS(ON)}$ Current Sense**
- **Adjustable Over Current Protection with Improved Noise Immunity**
- **Full-Time Over Voltage Protection**
- **Fast Transient Response**
- **Internal Soft-Start**
- **RoHS Compliant and Halogen Free**

Applications

- Graphic Card
- Motherboard
- IA Equipment
- Telecomm Equipment
- Mid-Power DC/DC Regulator

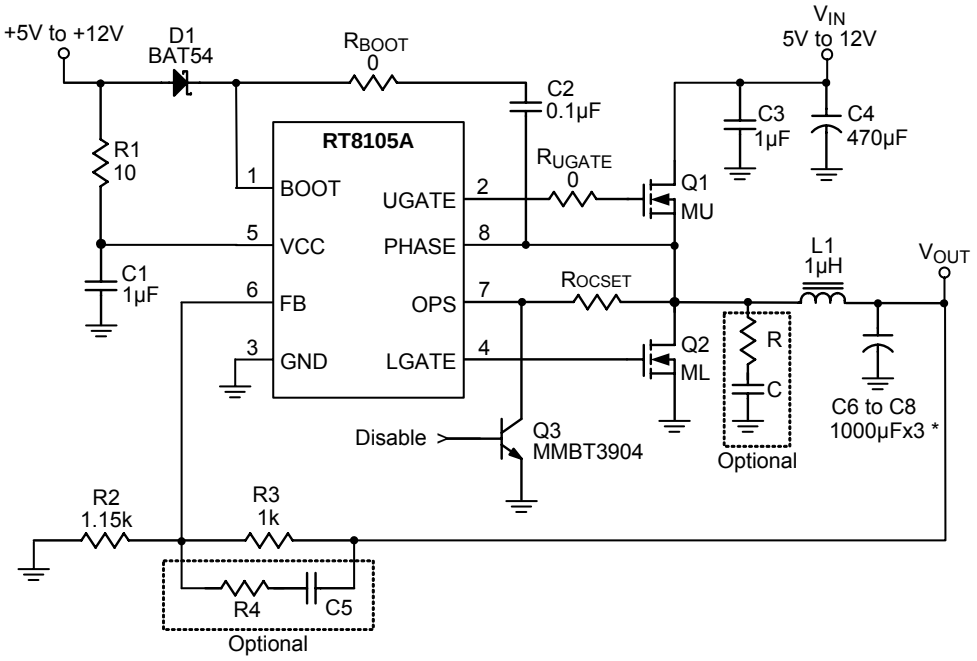
Pin Configurations

(TOP VIEW)



SOP-8

Typical Application Circuit



$$V_{OUT} = V_{REF} \times (1 + \frac{R3}{R2})$$

V_{REF}: Internal reference voltage (0.8V ±2%)

* : Each has $ESR_{(MAX)}$ = 28mΩ

Functional Pin Description

BOOT (Pin 1)

Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

UGATE (Pin 2)

Upper gate driver output. Connect to the gate of high side power N-MOSFET. This pin is monitored by the adaptive shoot through protection circuitry to determine when the upper MOSFET has turned off.

GND (Pin 3)

Both signal and power ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance.

LGATE (Pin 4)

Lower gate drive output. Connect to the gate of low-side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

VCC (Pin 5)

Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.

FB (Pin 6)

Switcher feedback voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.

OPS (OCSET, POR and Shutdown) (Pin 7)

This pin provides multi-function of the over current setting, UGATE turn-on POR sensing, and shut-down features. Connecting a resistor (R_{OCSET}) between OPS and PHASE pins sets the over-current trip point.

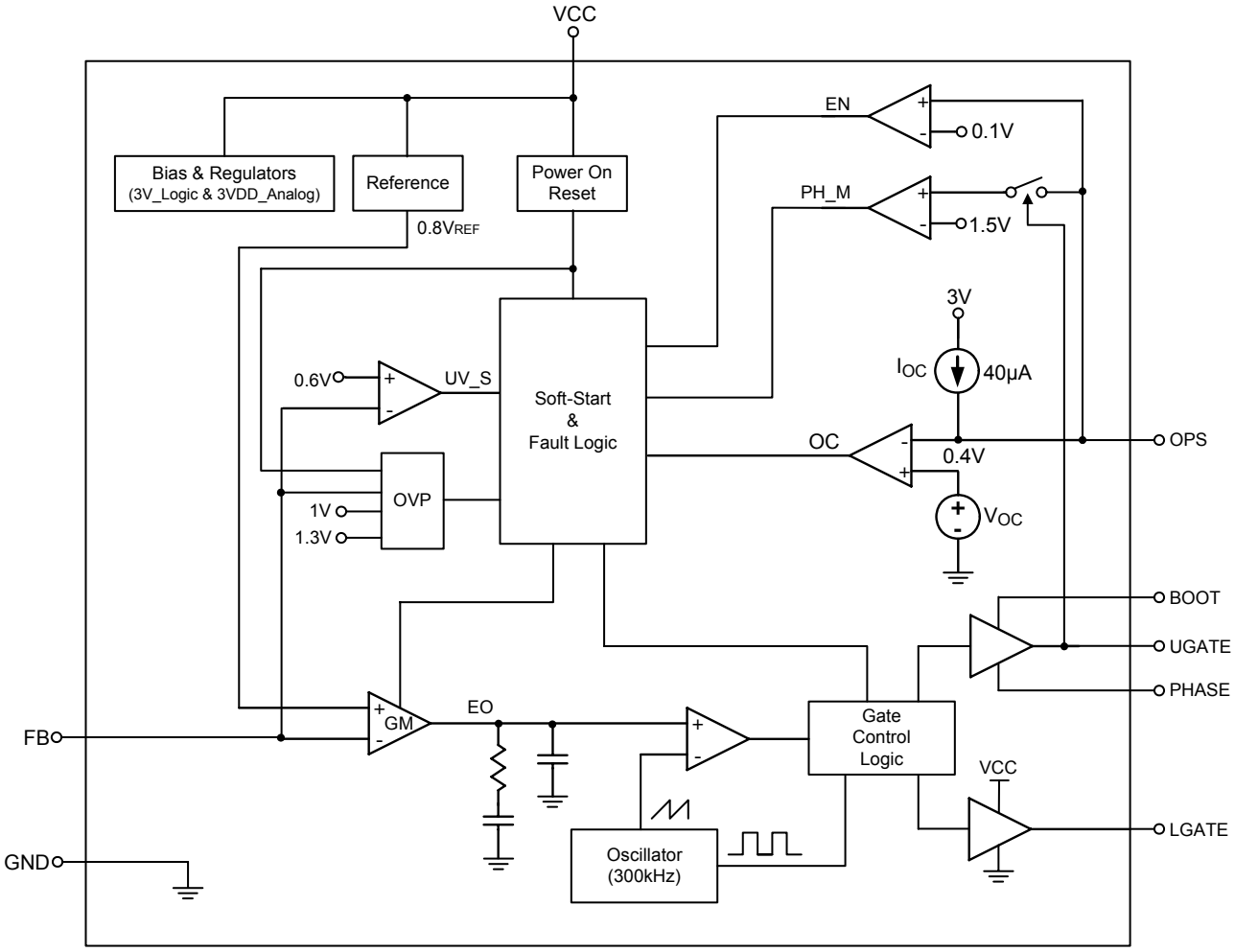
Pulling the pin to ground resets the device and all external MOSFETs are turned off allowing the output voltage power rails to float.

This pin is also used to detect V_{IN} in power on stage and issues an internal POR signal.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 16V
- BOOT to PHASE ---------- 15V
- UGATE to PHASE
  - DC ---------- –0.3V to ($V_{BOOT-PHASE}$ + 0.3V)
  - < 20ns ---------- –5V to ($V_{BOOT-PHASE}$ + 5V)
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - < 20ns ---------- –5V to 25V
- LGATE to GND
  - DC ---------- –0.3V to (V_{CC} + 0.3V)
  - < 20ns ---------- –5V to (V_{CC} + 5V)
- Input, Output or I/O Voltage ---------- GND – 0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C (Note 2)
  - SOP-8 ---------- 0.625W
- Package Thermal Resistance
  - SOP-8, θ_{JA} ---------- 160°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.75V to 13.2V
- Junction Temperature Range ---------- –20°C to 125°C
- Ambient Temperature Range ---------- –20°C to 85°C

Electrical Characteristics

(V_{CC} = 5V/12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Nominal Supply Current	I_{CC}	UGATE and LGATE Open, V_{CC} = 12V	--	4	15	mA
Power-On Reset						
POR Threshold	V_{CCRTH}	V_{CC} Rising	3.8	4.1	4.35	V
Hysteresis	V_{CCHYS}		0.35	0.55	--	V
Switcher Reference						
Feedback Reference Voltage	V_{REF}	V_{CC} = 12V	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC} = 12V	250	300	350	kHz
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	1.5	--	V_{P-P}

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier (GM)						
E/A Transconductance	gm	(Note 5)	--	0.2	--	ms
Open Loop DC Gain	A_O	(Note 5)	--	90	--	dB
PWM Controller Gate Drivers (V_{CC} = 12V)						
Upper Gate Source	I_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{UGATE} - V_{PHASE}$ = 6V	0.6	1	--	A
Upper Gate Sink	R_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{UGATE} - V_{PHASE}$ = 1V	--	4	8	Ω
Lower Gate Source	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	0.6	1	--	A
Lower Gate Sink	R_{LGATE}	V_{CC} = 12V, V_{LGATE} = 1V	--	3	5	Ω
Protection						
FB Under-Voltage Trip	Δ_{FBUVT}	FB Falling	70	75	80	%
OC Current Source	I_{OC}	V_{PHASE} = 0V	35	40	45	μA
Pre-OVP Threshold (Before POR)	V_{OVP1}	V_{CC} = 3V, Sweep V_{FB}	--	0.7	1.3	V
OVP Threshold (After POR)	V_{OVP2}	V_{CC} = 5V, Sweep V_{FB}	1	1.3	1.5	V
Soft-Start Interval	T_{SS}		--	4.5	--	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a low-effective thermal conductivity single-layer test board of JEDEC 51-3 thermal measurement standard. The measurement case position of θ_{JC} is on the lead of the package.

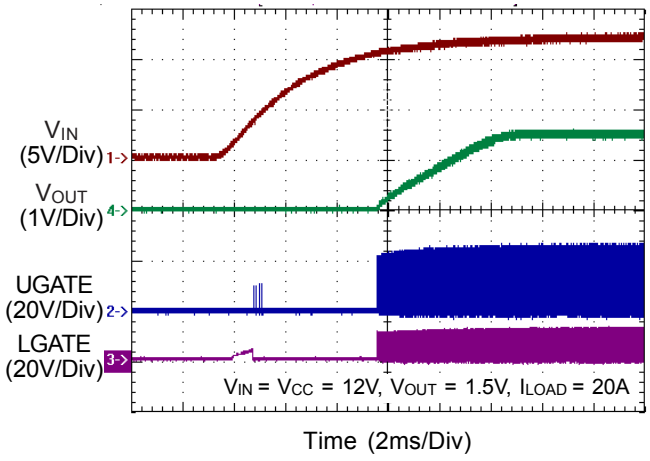
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

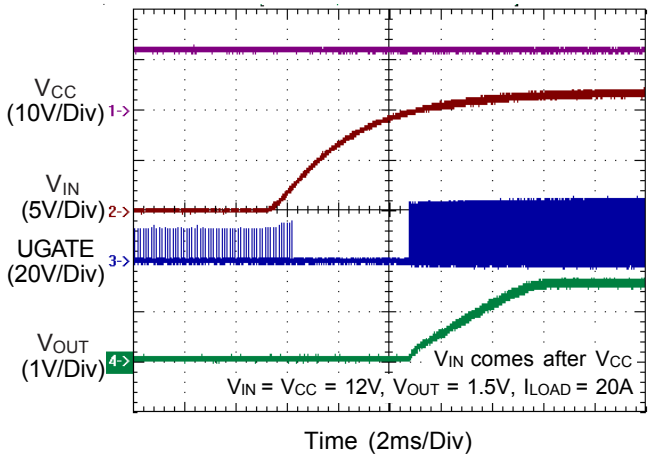
Note 5. Guarantee by design.

Typical Operating Characteristics

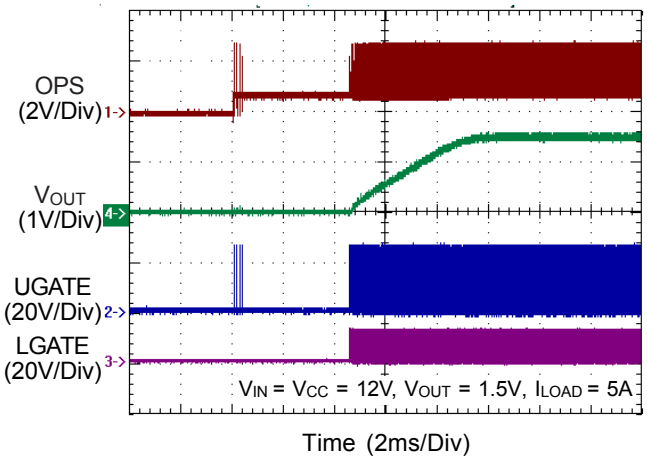
Power On from V_{IN}



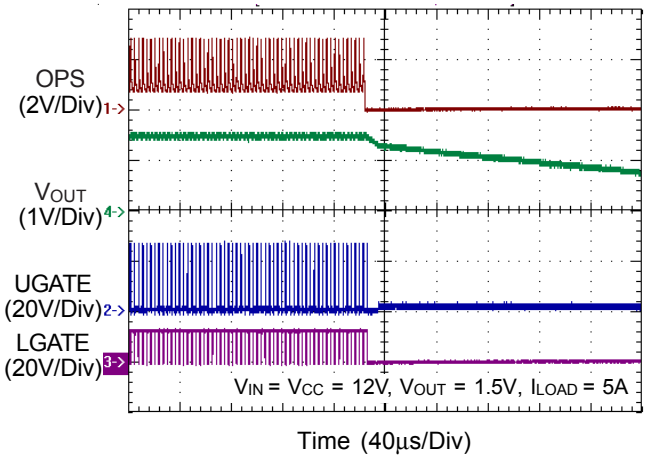
V_{IN} and V_{CC} Power Sequence



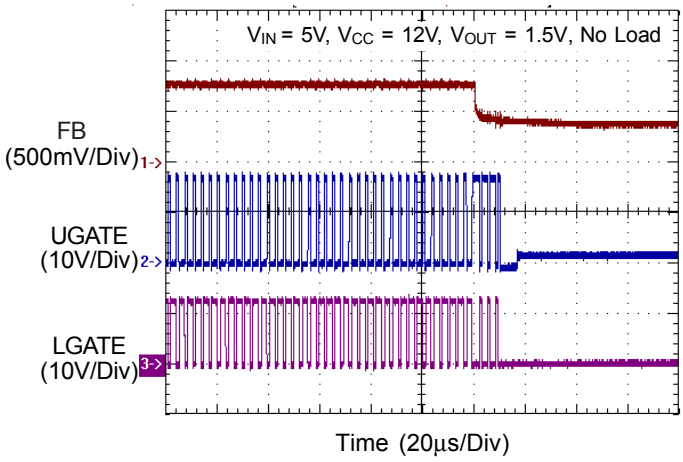
Enable from OPS



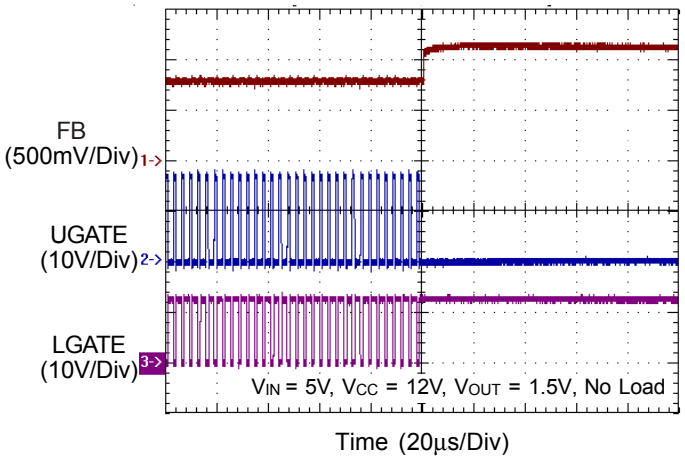
Disable from OPS



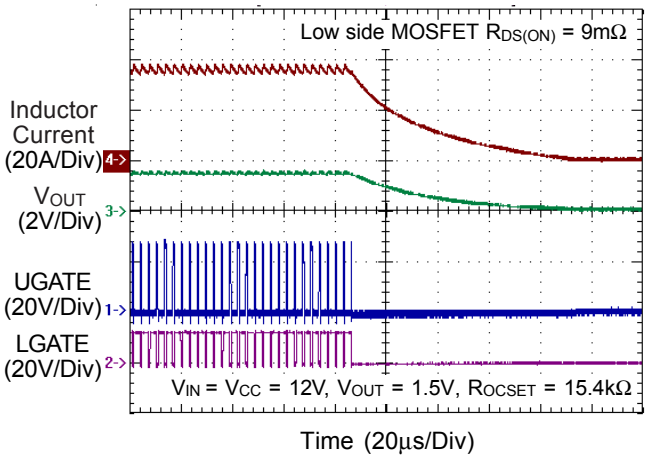
Under Voltage Protection



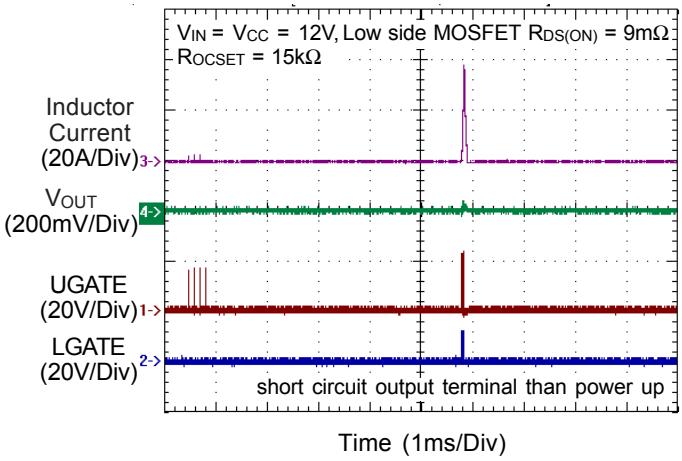
Over Voltage Protection



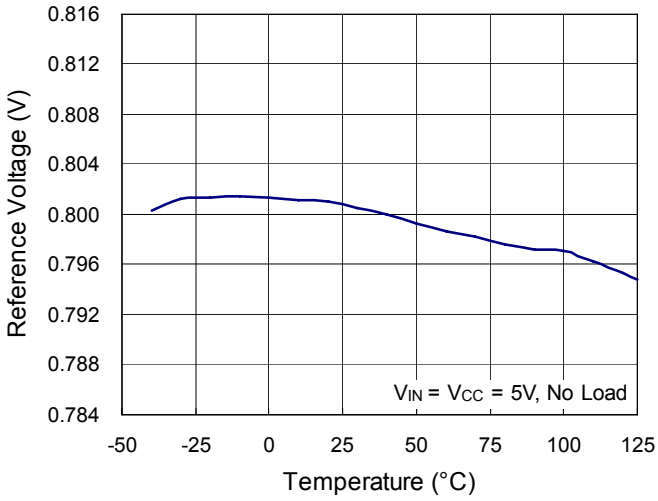
Over Current Protection



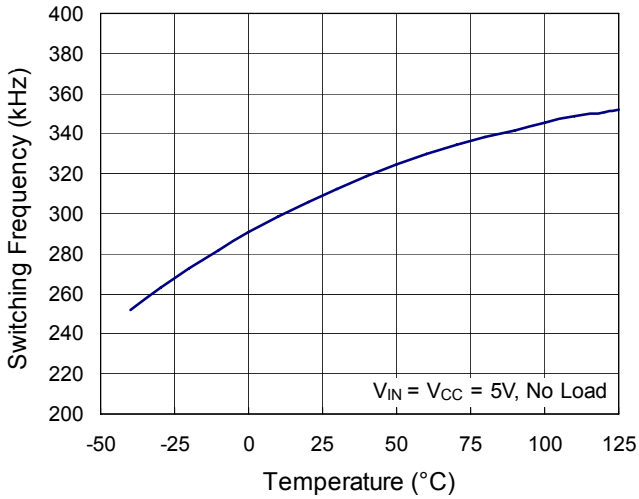
Short Circuit Over Current Protection



Reference Voltage vs. Temperature



Switching Frequency vs. Temperature

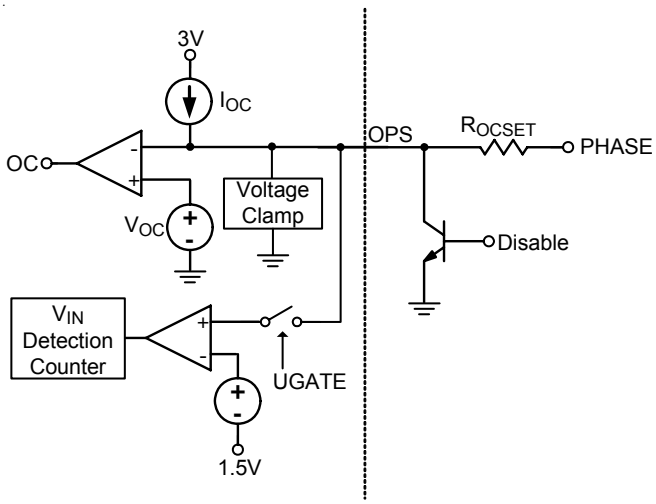


Application Information

The RT8105A is a fixed-frequency, single phase synchronous buck controller with embedded MOSFET gate drivers. This part provides precise output voltage regulation, supports enable/disable control, and has complete fault protection functions. The RT8105A utilizes lossless $R_{DS(ON)}$ current sense technique, and provides adjustable over current protection. This IC uses voltage mode control and the control loop is internally compensated to eliminate external component count.

VCC Power on Reset and V_{IN} Detection

At start up, when VCC initially rises above the power on reset (POR) rising threshold V_{CCRTH}, UGATE pin will output continuous pulses (about 10kHz, 1% duty cycle) for converter input voltage V_{IN} detection. The RT8105A detects the voltage pulses at OPS pin to recognize that V_{IN} is ready. Figure 1 shows the operation of input voltage V_{IN} detection. If the OPS voltage exceeds 1.5V for four times, making internal counter = 4 (both rising edge + falling edge for counter increment = 1), V_{IN} is recognized ready. Once V_{IN} is recognized ready, controller will initiates soft start operation. Because an internal current source (for over current protection) will continuously flow out of OPS pin, R_{OCSET} is highly recommended to be less than 30kΩ to ensure correct operation.



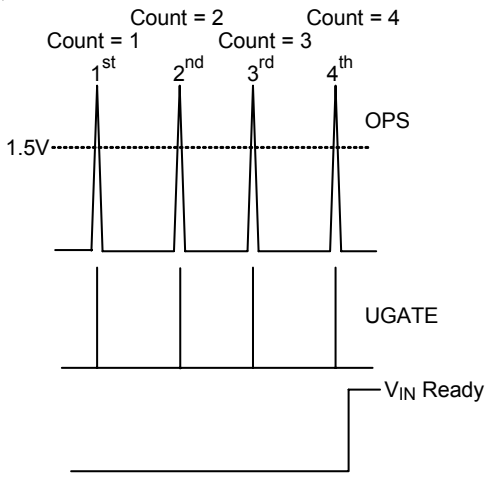


Figure 1. V_{IN} Detection Function

Soft-Start

Once V_{IN} is recognized ready, LGATE will go high for a short period of time to discharge the pre-biased voltage at the output capacitor. After that, controller will initiate soft start operation. RT8105A provides soft start function internally. The soft start function is used to prevent the large inrush current while converter is powered up. The FB signal will track the internal soft start signal, which is controlled by an internal digital counter and ramps up from zero in a monotone during soft start period. Therefore the duty cycle of UGATE signal will increase gradually and so does the input current. The typical soft start time duration is 3ms.

Over Current Protection (OCP)

The RT8105A utilizes $R_{DS(ON)}$ current sense technique to detect the inductor valley current for over current protection. Figure 2 shows the Over Current Protection (OCP) scheme of RT8105A. A resistor R_{OCSET} connected from PHASE pin to OPS pin sets the threshold. An internal current source I_{OC} flows out of OPS pin through R_{OCSET} determines the OCP trip point I_{OCSET}, which can be calculated using the following equation :

$$I_{OCSET} \approx \frac{40\mu A \times R_{OCSET} - 0.4}{R_{DS(ON)} \text{ of the low side MOSFET}}$$

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

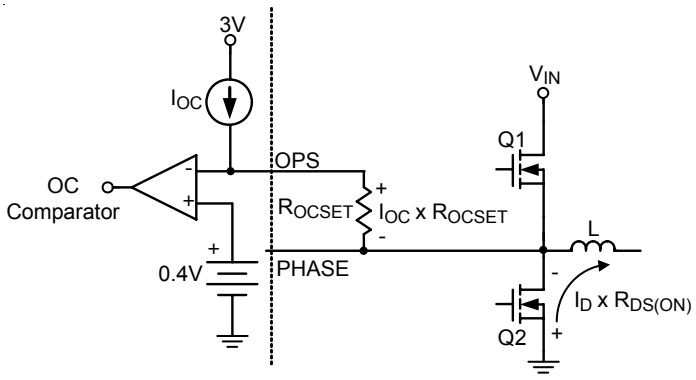


Figure 2. Over Current Protection Scheme

Inductor valley current exceeds OCP trip point I_{OCSET} in one switching cycle is regarded as an over current event. The controller has an internal counter to monitor the over current event. To avoid OCP false tripping, only four consecutive over current events will trip OCP. When OCP is tripped, the controller shuts down, both UGATE and LGATE will go low to stop the energy transfer to the load. The OCP is a latched protection, it can only be reset by toggling VCC POR.

Over Voltage Protection (OVP)

The feedback voltage at FB pin is continuously monitored for over voltage protection. When OVP is tripped, UGATE will go low and LGATE will go high to discharge the output capacitor. RT8105A provides full-time over voltage protection whenever soft start completes or not. Over voltage protection has two operating conditions: before soft start completes and after soft start completes. Each condition is described as follows.

Before soft start completes, the typical OVP threshold is 125% of the internal reference voltage V_{REF}. RT8105A provides non-latched OVP before soft start completes. The controller will return to normal operation if over voltage condition is removed.

After soft start completes, however, the OVP threshold is typically raised to 162.5% of V_{REF}. RT8105A provides latched OVP, which means controller will shut down. Under this condition, the controller can only be reset if VCC POR is toggled.

Under Voltage Protection (UVP)

The feedback voltage at FB pin is also monitored for under voltage protection. The under voltage protection has a 10μs triggered time delay. When UVP is triggered, both UGATE and LGATE will go low. The UVP is not a latched protection, controller will always try to restart in a hiccupped way.

Enable/Disable Control

The RT8105A supports enable/disable control function to provide the flexibility in power sequence control. The controller is disabled by pulling OPS pin to ground. It is recommended to use bipolar junction transistor (BJT) to implement the enable/disable function. Note that the OCP point is very sensitive to the parasitic capacitance at OPS pin. Parasitic capacitance at OPS pin will have influence on the OCP point. To minimize PCB trace parasitic component, it is recommended to place the BJT and R_{OCSET} close to IC, and use short copper trace.

Input Capacitor Selection

The selection of input capacitor depends on the converter input ripple current. The buck converter draws current from the input capacitor when high side MOSFET is on, this input current is pulsating. The RMS value of the ripple current flowing through the input capacitor can be expressed as follows :

$$Irms = I_{OUT}\sqrt{D(1-D)} \quad (A)$$

The input capacitor must be able to handle this RMS current. It is recommended to add ceramic capacitors and place them physically close to the drain of the high side MOSFET. This can effectively reduce the input ripple voltage of the converter.

Output Inductor Selection

The selection of output inductor depends on the output current and operating frequency. Low inductance value provides fast transient response, but the associated large current ripple will cause large output voltage ripple and decrease efficiency.

The first step is to determine the inductor current ripple according to the rated load current I_{OUT}, which is given by the converter specification. In general, a 20% to 40% of

inductor ripple current percentage ($\Delta I_L/I_{OUT}$) is preferred in practical application. Therefore the inductor current ripple ΔI_L can be obtained. The minimum inductance can then be determined as follows :

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_S \times \Delta I_L}$$

Where :

V_{IN} = Input voltage

V_{OUT} = Output voltage

ΔI_L = Inductor current ripple

f_S = Switching frequency

Output Capacitor Selection

The selection of output capacitor depends on the inductor ripple current, the output ripple voltage and the amount of voltage undershoot during load transient. The output ripple voltage is a function of both the capacitance and the equivalent series resistance (ESR). The output ripple voltage can be expressed as follows :

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC}$$

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{C_{OUT}} \int_{t1}^{t2} i_{C_{OUT}} dt$$

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \frac{V_{OUT}}{C_{OUT}} (1-D) T_S^2$$

where ΔV_{OR} is caused by ESR, and ΔV_{OC} is related to the capacitance value.

For electrolytic capacitor application, major of the output voltage ripple is typically contributed by the ESR. Therefore, the output voltage ripple can be simplified as follows :

$\Delta V_{OUT} = \Delta I_L$ x ESR

Therefore the ESR can be determined for a given output voltage ripple requirement as the reference of capacitor selection. The output capacitor must be able to handle the inductor ripple current that is determined in the first step. Refer to the capacitor datasheet and choose capacitor with sufficient ripple current rating, the ESR can also be obtained from the datasheet. Once the L, C and ESR are known, the next step is to check the close loop stability.

Control Loop Stability

The RT8105A utilizes operational transconductance amplifier (OTA) as the error amplifier and implements the control loop compensation network internally. Figure 3 shows the internal Type II compensator, which provides two poles and one zero to the control loop.

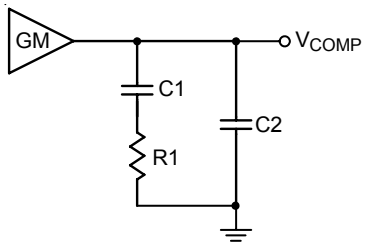


Figure 3. Internal Type II Compensator

One of the poles is located at low frequency to increase the low frequency gain to improve the DC regulation accuracy, the location of the other pole and the zero can be calculated as follows :

$$F_Z = \frac{1}{2\pi \times R1 \times C1}; \quad F_P = \frac{1}{2\pi \times R1 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

The transconductance and the internal compensation values are : gm = 0.2mA/V, R1 ≈ 75kΩ, C1 ≈ 2.5nF, C2 ≈ 10pF.

The gain of the internal compensator at middle frequency can be calculated as follows :

$G_{mid\text{-}freq.}$ = gm x R1

Figure 4 shows the system Bode plot. The close loop gain is the sum of the modulation gain and the compensation gain. The goal is to obtain the required crossover frequency with sufficient phase margin. The general guideline is to design the crossover frequency as between 1/10 to 1/5 of the switching frequency. The phase margin is preferred to be greater than 45° to ensure stability.

Because RT8105A utilizes internal compensation for the control loop, the location of F_Z, F_P and the gain at mid-frequency provided by the internal compensator are fixed. Therefore the inductance, output capacitance and the ESR of the output capacitor should be carefully selected to avoid instability.

The location of the double pole F_{LC} and the ESR zero F_{ESR} can be calculated as follows :

$$F_{LC} = \frac{1}{2\pi \times L \times C};\ F_{ESR} = \frac{1}{2\pi \times ESR \times C}$$

For an given L and C, if the ESR is too small, the location of the zero contributed by ESR is far away from that of the LC double pole, the system will not have sufficient phase margin. If the ESR is too large, the location of the ESR zero moves towards low-frequency, the crossover frequency may go beyond 1/5 switching frequency, resulting in higher jitter and unstable operation.

Manipulate the Bode plot according to the chosen L, C and ESR value to check the stability before circuit implementation. If the phase margin is insufficient or the bandwidth is far beyond the general guideline, the inductor, output capacitor and ESR values should be reselected, and the stability should be checked again. To meet the stability criteria, two or more capacitors in parallel is a common practice.

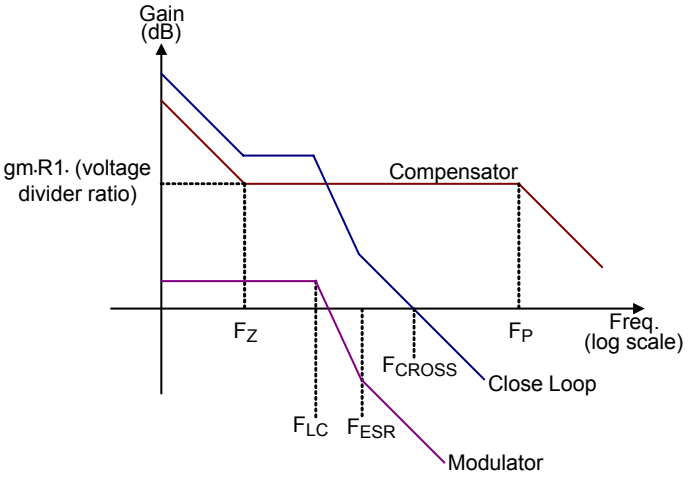


Figure 4. System Bode Plot

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8105A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 packages, the thermal resistance, θ_{JA}, is 160°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (160°C/W) = 0.625W for SOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8105A package, the derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

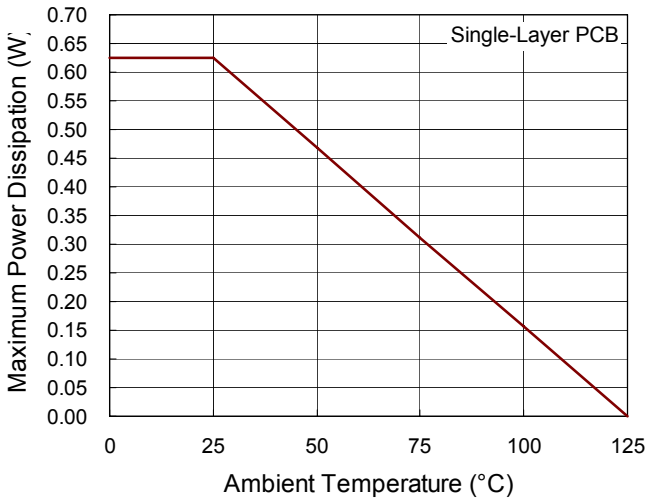


Figure 5. Derating Curve for RT8105A Package

Layout Considerations

PCB layout is critical to high current high frequency switching converter design. A good layout can help the controller to function properly and obtain better performance. In reverse, the circuit may have more power loss, pool performance and even malfunction without a carefully layout. The general guidelines of PCB layout are listed as follows for reference.

- Power stage components should be placed first. Place the input bulk capacitors close to the high-side power MOSFETs, and then locate the output inductor. Finally, place the output capacitors.
- Place the ceramic capacitors physically close to the drain of the high-side MOSFET. This can reduce the input voltage drop when high side MOSFET is turned on.
- Keep the high current loops as short as possible. The current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components of PCB trace and component lead. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and also reduce EMI.
- Make MOSFET gate driver path as short as possible. Since the gate driver uses high current pulses to switch on/off power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low side MOSFET, because this can reduce the possibility of shoot-through. Make the width of gate driving path (include the trace to the bootstrap capacitor and diode) as wide as possible to reduce the trace resistance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- Voltage feedback path must be kept away from switching nodes. The switching nodes, such as the interconnection between high-side MOSFET, low side MOSFET and inductor, are extremely noisy. Feedback path must be kept away from this kind of noisy node to avoid noise pick-up.
- The feedback voltage divider resistor must be placed close to FB pin because it is noise-sensitive.
- OCP threshold setting resistor, R_{OCSET}, should be placed close to the controller.
- The BJT used for enable/disable control should be placed close to the controller to minimize the trace parasitic components.
- A multi-layer PCB design is recommended. Use one single layer as the solid ground plane.

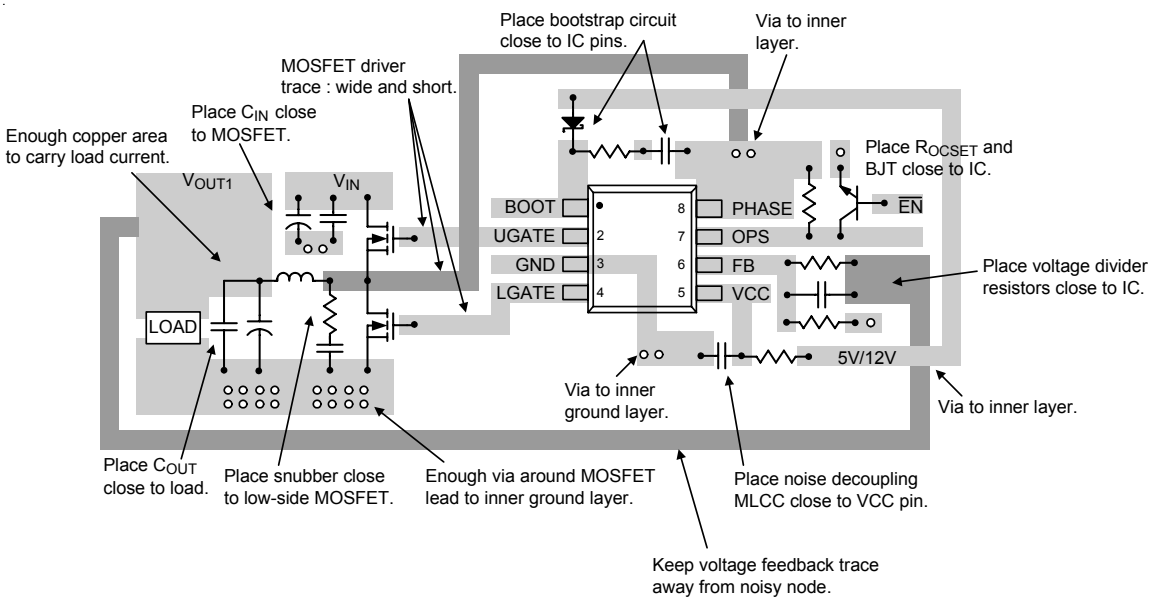
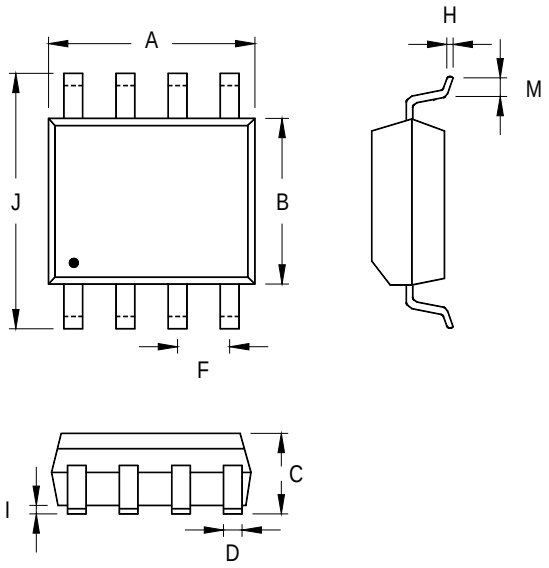


Figure 6. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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