

Easy to Use Power Bank Solution (EZPBS™) Integrated Chip with Switch Charger, ADC, and Load Switch

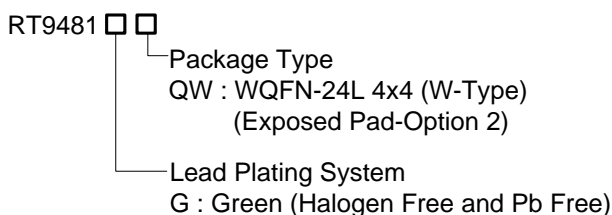
General Description

The RT9481 is a high integration and easy to use power solution for Li-ion power bank and other powered handheld applications. We call it EZPBS™ (Easy to Use Power Bank Solution). This single chip includes a Switching Charger with Boost function, Analog to Digital Converter (ADC), USBOUT Load Switch, Adapter Detection with BC1.2, DCP controller and LDO.

Applications

- Power Bank

Ordering Information

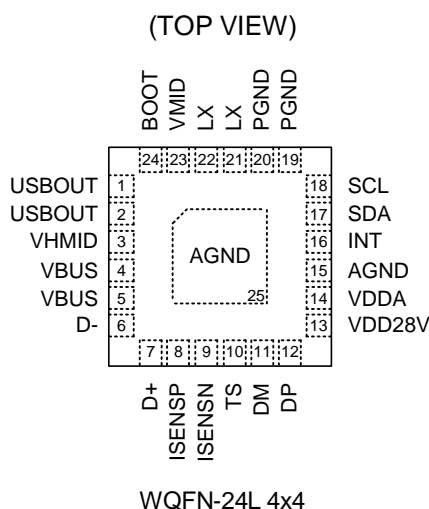


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations



Features

System

- High Accuracy Voltage/Current Regulation
 - ▶ $\pm 1\%$ Charge Voltage Regulation
 - ▶ $\pm 0.1A$ Charge Current Regulation
 - ▶ $\pm 3\%$ Boost USBOUT Voltage Regulation
- Thermal Shutdown Protection
- Reverse Leakage Protection to Prevent Battery Drainage.
- Built-In USBOUT DCP Controller
- Built-In USBOUT Attach/Detach Detection
- Built-In USBOUT Light Load Detection
- Built-In Load Switch with Current Regulation Thermal Regulation and Output Short Current Protection
- Built-In Adapter Detection with BC1.2
- Built-In Accurate ADC to Measure VBAT, VBUS, TS, IBAT, USBOUT and IUSBOUT
- Built-In LDO
- Interrupt Output for Event Notification
- I²C Interface with 400kHz

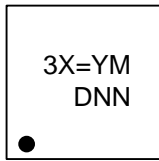
Charge Mode

- Charge Voltage Regulation : 3.65V to 4.6V
- Charge Current Regulation : 0.7A to 2.7A
- Minimum Input Voltage Regulation (MIVR) : 4.2V to 4.8V
- Average Input Current Regulation (AICR) : 0.1A to 2A
- Charge Termination Current : 0.15A to 0.6A
- Pre-charge Threshold : 2.3V to 3.8V
- Pre-charge Current : 0.2A to 0.5A
- Thermal Regulation
- VMID Under Voltage Protection
- VBUS Over Voltage Protection
- Battery Over Voltage Protection
- Bad Adapter Detection

Boost Mode

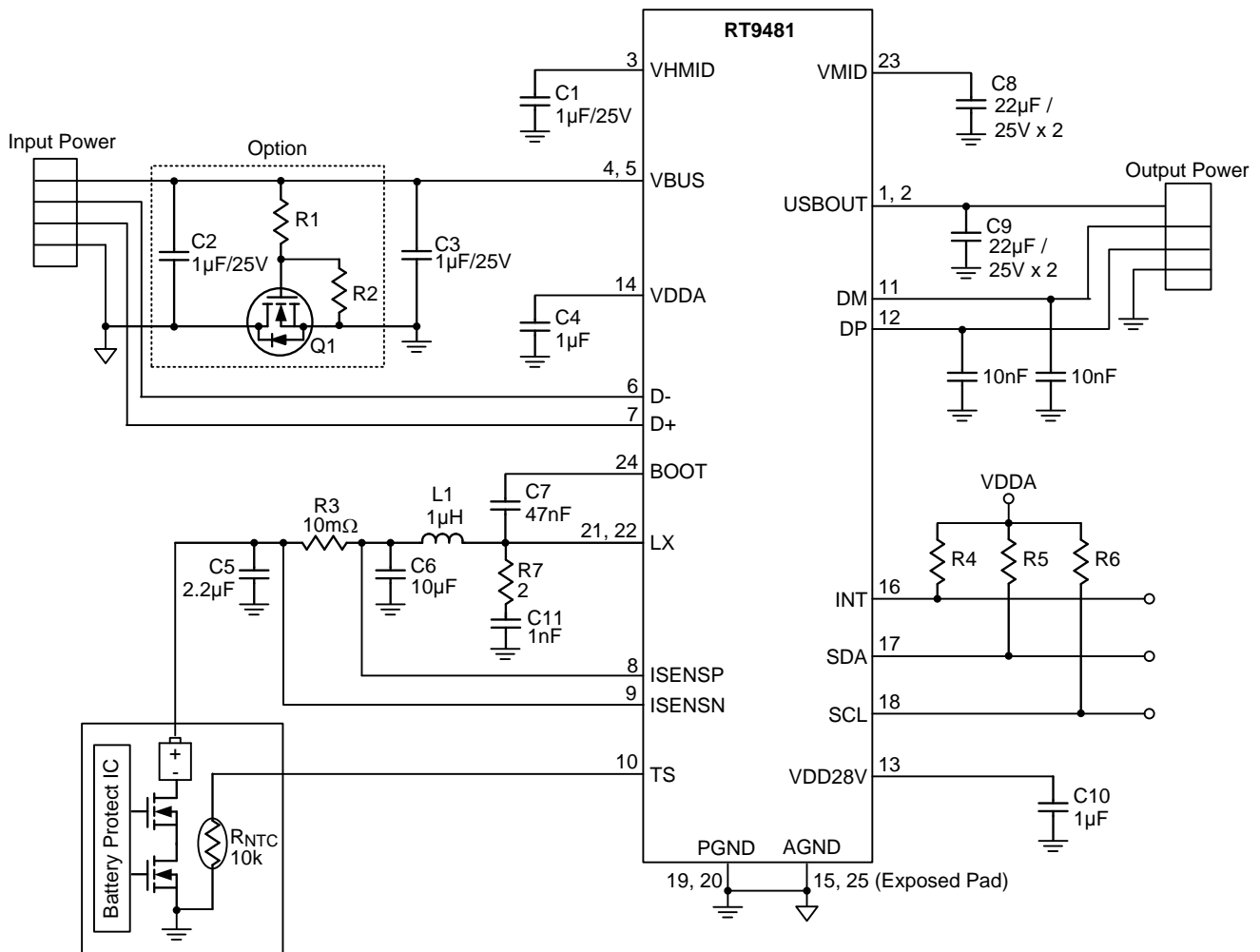
- Boost Output Current Up to 3A
- Boost Output Voltage : 3.65V to 5.2V
- Battery Under Voltage Protection : 2.5V to 3.2V
- VMID Over Voltage Protection

Marking Information



3X= : Product Code
YMDNN : Date Code

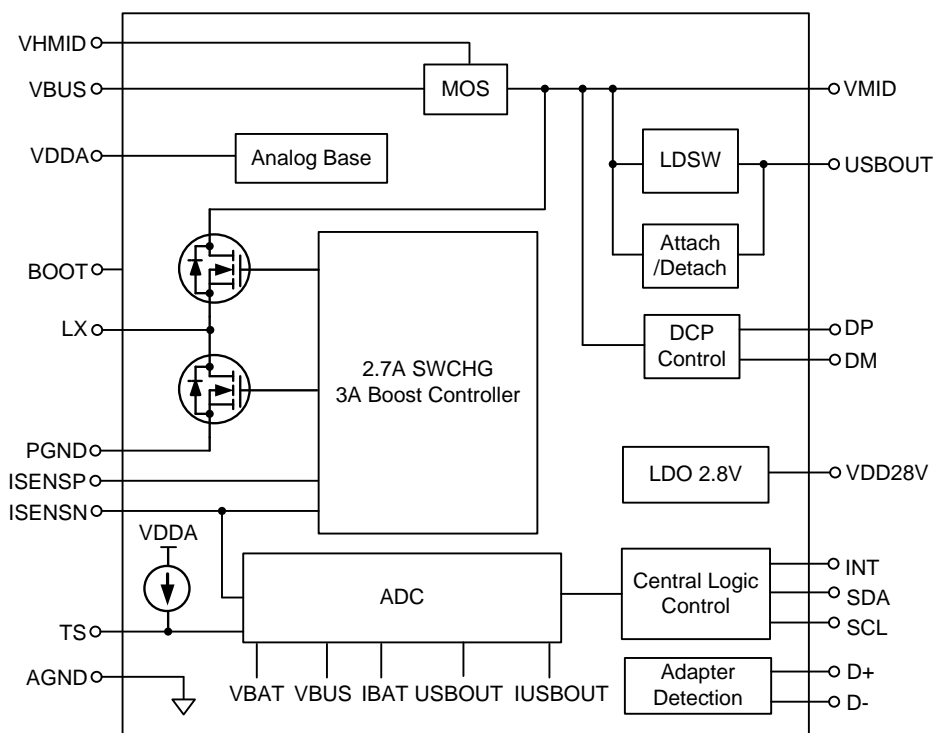
Typical Application Circuit



Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|-------------------------|----------|--|
| 1, 2 | USBOUT | USB Power Output. |
| 3 | VHMID | Internal Use Only. |
| 4, 5 | VBUS | VBUS Power Supply. |
| 6 | D- | D- Input for Adapter Detection. |
| 7 | D+ | D+ Input for Adapter Detection. |
| 8 | ISENSP | Charging Current Sensing Positive Node. |
| 9 | ISENSN | Charging Current Sensing Negative Node and Connect to Battery Plus Terminal. |
| 10 | TS | Battery Temperature Detection Pin. |
| 11 | DM | DCP Controller DM Output. |
| 12 | DP | DCP Controller DP Output. |
| 13 | VDD28V | Internal Use LDO Output. |
| 14 | VDDA | Internal Power for Analog Blocks, Put 1 μ F to GND. |
| 15, 25 (Exposed Pad) | AGND | Analog Ground Node. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation. |
| 16 | INT | Interrupter Signal. Connect an external pull-up resistor. |
| 17 | SDA | Data Input and Output for I ² C Serial Port. Connect an external pull-up resistor. |
| 18 | SCL | Clock Input for I ² C Serial Port. Connect an external pull-up resistor. |
| 19, 20 | PGND | Power Ground for Switching Charger. |
| 21, 22 | LX | Internal Switch Node to Output Inductor Connection. |
| 23 | VMID | Connection Point Between Reverse Blocking and High-Side. |
| 24 | BOOT | Bootstrap Power Node for Switching Charger. |

Functional Blocks Diagram



Operation

The RT9481 is a high integrated IC for Li-Ion battery power bank. It includes a Switch charger 2.7A, a synchronous Boost 5V.

Charge Current

Base on thermal regulation function, the charging current can support up to 2.7A.

VBUS Over Voltage Protection

If the input voltage (VBUS) is higher than the threshold voltage V_{OVP} , the internal OVP signal will go high and the charger will stop charging until V_{IN} is below $V_{OVP} - \text{hysteresis}$.

VMID Over Voltage Protection

If the internal voltage (VMID) is higher than the threshold voltage V_{OVP} , the internal OVP signal will go high and the charger will stop charging until VMID is below $V_{OVP} - \text{hysteresis}$.

VMID Under Voltage Protection

If the internal voltage (VMID) is lower than the threshold voltage V_{UVP} , the internal VMID_UVP signal will go high and the system will disable LDSW

function in order to protect system from short-to-ground current damages.

USBOUT SCP

The USBOUT short circuit protection (SCP) function will prevent system from burning out by monitoring the voltage drop between LDSW. If the USBOUT is short to ground, the inrush current will make the VDS voltage too large to damage chip. The SCP function also reports this condition to protect chip in time.

Boost OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, The OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

OTP

The converter has an over-temperature protection.

When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be

regulated until the junction temperature drops under the falling threshold.

CC/CV/TR Multi Loop Controller

There are constant current loop, constant voltage loop and thermal regulation loop to control the charging current.

Base Circuits

Base circuits provide the internal power, VDDA and reference voltage and bias current.

Buck Regulator for Charging and Boost Regulator as BOOST

The multi-loop controller controls the operation of charging process and current supply to the system. It also controls the circuits as a Boost converter for BOOST applications.

USB Charger Detection

The RT9481 detects USB Charger (Standard Charger Port, Charging Downstream Port and Dedicated Charger Port) via D+ and D- pins.

USBOUT Attach/Detach Detection

RT9481 includes an auto attach detection for the power bank product. The attach detection has a current threshold which represent an attach condition. When the attach detection is enable, the USBOUT will generate a 1.6V to monitor the load current. Once load current is greater than 5 μ A, the attach flag will be reported until the load current is removed.

I²C Controller

The key parameters of charging and BOOST are programmable through I²C commands.

Absolute Maximum Ratings (Note 1)

- VBUS, VHMID Supply Input Voltage ----- -0.3V to 18V
- VMID----- -0.3V to 6.7V
- LX, BOOT ----- -0.3V to 6V
- VMID – VBUS, BOOT– LX----- -0.3V to 6V
- Others ----- -0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
 - WQFN-24L 4x4 ----- 3.57W
- Package Thermal Resistance (Note 2)
 - WQFN-24L 4x4, θ_{JA} ----- 28°C/W
 - WQFN-24L 4x4, θ_{JC} ----- 7.1°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Model) ----- 2kV
 - MM (Machine Model) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage----- 4.3V to 5.65V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range----- -40°C to 85°C

Electrical Characteristics(V_{BUS} = 5V, V_{BATS} = 4.2V, T_A = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|--------------------------|---|-----|------|------|------|
| Input Power Source | | | | | | |
| VBUS Operation Range | | | 4 | -- | 5.65 | V |
| VBUS Supply Current | I _Q | PWM switching, I _{CHG} = I _{BAT} = 0mA | -- | 10 | -- | mA |
| | | High Impedence Mode | -- | -- | 200 | μA |
| Leakage Current from Battery | I _{BAT_LEAK} | V _{BAT} = 4.2V, V _{BUS} = 0V, Charger off. 1/80 ADC execution time duty | -- | 40 | 60 | μA |
| Protection | | | | | | |
| VBUS OVP Threshold Voltage | V _{BUS_OVP} | VBUS Rising | 5.7 | 6 | 6.3 | V |
| VBUS OVP Hysteresis | V _{BUS_OVP_HYS} | VBUS Falling | -- | 200 | -- | mV |
| VBUS UVLO | V _{BUS_UVLO} | VBUS Rising | 3 | 3.25 | 3.5 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|---------------------------|--|-----|---------|------|------|
| VBUS UVLO Hysteresis | V _{BUS_UVLO_HYS} | VBUS Falling | -- | 150 | -- | mV |
| ISENSN OVP | V _{BAT_OVP} | VISENSN Rising | 103 | 107 | 114 | % |
| ISENSN OVP Hysteresis | V _{BAT_OVP_HYS} | VISENSN Falling | -- | 5 | -- | % |
| Over Temperature Protection | T _{OTP} | (Note 5) | -- | 160 | -- | °C |
| OTP Hysteresis | T _{OTP_HYS} | | -- | 20 | -- | °C |
| Thermal Regulation Threshold | T _{REG} | Optional 100/120/135°C by I ² C (Default value is 120°C) | -- | 120 | -- | °C |
| Input Power Source Detection | | | | | | |
| Poor Source Detect Threshold | V _{BUS_pr} | Bad Voltage Source Detection | 3.6 | 3.8 | 4 | V |
| Poor Source Detect Deglitch | t _{BUS_pr_dg} | | -- | 30 | -- | ms |
| Poor Source Detect Hysteresis | V _{BUS_pr_hys} | VBUS Rising | 100 | -- | 200 | mV |
| Current Sink to GND | I _{BUS_pr} | During Poor Source Detection | -- | 50 | -- | mA |
| Detection Interval Time | t _{BUS_pr_int} | | -- | 2 | -- | s |
| Sleep Mode Comparator | | | | | | |
| Sleep-Mode Entry Threshold VBUS – ISENSN | V _{SLP} | 3V < VISENSN < V _{BATREG} , VBUS Falling | -- | 40 | 100 | mV |
| Sleep-Mode Exit Hysteresis VBUS Symbol ISENSN | V _{SLPEXIT} | 3V < VISENSN < V _{BATREG} , VBUS Rising | 40 | 120 | 200 | mV |
| Sleep-Mode Deglitch Time | t _{SLP} | VBUS Rising Above V _{SLP} + V _{SLPEXIT} | -- | 30 | -- | ms |
| Minimum Input Voltage Regulation (MIVR) | | | | | | |
| Minimum Input Voltage Regulation | V _{MIVR} | Optional 4.2V to 4.8V by I ² C per 0.1V (Default value is 4.7V) | 4.2 | -- | 4.8 | V |
| V _{MIVR} Accuracy | | | –5 | -- | 5 | % |
| Average Input Current Regulation (AICR) Accuracy | I _{AICR_100mA} | I _{AICR} = 100mA | 80 | 90 | 100 | mA |
| | I _{AICR_500mA} | I _{AICR} = 500mA | 400 | 450 | 500 | |
| | I _{AICR_700mA} | I _{AICR} = 700mA | 560 | 630 | 700 | |
| | I _{AICR_1000mA} | I _{AICR} = 1000mA | 800 | 900 | 1000 | |
| AICR Range | I _{AICR} | Optional 100mA to 2000mA by I ² C (Default value is 0.5A) | 100 | -- | 2000 | mA |
| VDDA Regulator | | | | | | |
| VDDA Voltage | V _{DDA} | V _{BUS} > 4.5V | -- | 4.5 | -- | V |
| | | V _{BUS} < VISENSN | -- | VISENSN | -- | |
| VDDA UVLO | V _{DDA_UV} | VDDA Rising | 2.4 | 2.5 | 2.6 | V |
| VDDA UVLO Hysteresis | V _{DDA_UV_hys} | VDDA Falling | -- | 150 | -- | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---------------------------------|--|------|-----|-----|------|
| Battery Voltage Regulation | | | | | | |
| Battery Voltage Regulation | V _{BATREG} | Optional 3.65V to 4.6V by I ² C per 25mV (Default value is 4.2V) | 3.65 | -- | 4.6 | V |
| V _{BATREG} Accuracy | | | -1 | -- | 1 | % |
| Re-Charge Threshold | ΔV _{REG} | V _{ISENSN} Falling, ΔV _{REG} = (V _{BATREG} - V _{REC}) | 50 | 125 | 200 | mV |
| Re-Charge Deglitch Time | t _{REC} | | -- | 128 | -- | ms |
| Charging Current Regulation | | | | | | |
| Output Charging Current | I _{CHG} | R _{SENSE} = 10mΩ, Optional 0.7A to 2.7A by I ² C per 0.25A (Default value is 0.7A) | 0.7 | -- | 2.7 | A |
| I _{CHG} Accuracy | I _{CHG_ACC} | R _{SENSE} = 10mΩ | -100 | -- | 100 | mA |
| Pre-Charge Threshold | V _{PREC} | Rising, Optional 2.3V to 3.8V by I ² C per 0.1V (Default value is 3V) | 2.3 | -- | 3.8 | V |
| V _{PREC} Accuracy | | | -5 | -- | 5 | % |
| Pre-Charge Current | I _{PREC} | Optional 200mA to 500mA by I ² C per 100mA (Default value is 300mA) | 200 | -- | 500 | mA |
| I _{PREC} Accuracy | | | -20 | -- | 20 | % |
| Charge Termination Detection | | | | | | |
| End of Charge Current | I _{EOC} | R _{SENSE} = 10mΩ, Optional 150mA to 600mA by I ² C (Default value is 200mA) | 150 | -- | 600 | mA |
| I _{EOC} Accuracy | | R _{SENSE} = 10mΩ | -100 | -- | 100 | mA |
| Deglitch Time for EOC | t _{EOC} | I _{CHG} < I _{EOC} , V _{ISENSN} > (V _{BATREG} - ΔV _{REG}) Optional 4ms to 32ms by I ² C (Default value is 32ms) | 4 | -- | 32 | ms |
| Charger Timer Protection | | | | | | |
| Fast-Charge Time-Out | | Optional 6Hrs to 20Hrs by I ² C per 2Hrs (Default value is 20Hrs) | 6 | -- | 20 | Hrs |
| Pre-Charge Time-Out | | Optional 30Mins to 60Mins by I ² C per 15Mins (Default value is 60Mins) | 30 | -- | 60 | Mins |
| PWM Switching Charger | | | | | | |
| VBUS to LX Resistance | R _{DS(ON)_VBUS_LX} | From VBUS to LX, as I _{AICR} disable or I _{AICR} = 2A | -- | 97 | -- | mΩ |
| VBUS to USBOUT Resistance | R _{DS(ON)_VBUS_USBOUT} | From VBUS to USBOUT | -- | 98 | -- | mΩ |
| Low-Side On-Resistance | R _{DS(ON)_LS} | From LX to PGND | -- | 35 | -- | mΩ |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|--------------------------|---|-------|------|-----|------|
| Efficiency for Charge | EFF_CHG | $V_{BUS} = 5V$, $V_{ISENSN} = 4V$, and $I_{CHG} = 2A$ | -- | 90 | -- | % |
| Oscillator Frequency | fOSC | | -- | 0.75 | -- | MHz |
| Frequency Accuracy | | | -10 | -- | 10 | % |
| Maximum Duty Cycle | D _{MAX} | At Minimum Voltage Input | -- | 95 | -- | % |
| Minimum Duty Cycle | D _(MIN) | | 0 | -- | -- | % |
| Peak OCP as Charger Mode | | | -- | 4.5 | -- | A |
| Boost Mode Operation | | | | | | |
| Output Voltage Level | V _{BOOST} | To VMID Optional 3.625V to 5.2V by I ² C per 25mV (Default value is 5.1V) | 3.625 | -- | 5.2 | V |
| Output Voltage Accuracy | | | -3 | -- | 3 | % |
| Output Current On VMID | I _{BST} | $V_{BAT} > 3V$ | 3 | -- | -- | A |
| Efficiency for Boost | EFF_BST | $V_{MID} = 5V$, $V_{ISENSN} = 4V$, and Loading = 2A | -- | 92 | -- | % |
| Peak OCP as Boost Mode | I _{OCP_BST} | | -- | 6 | -- | A |
| VMID OVP as Reverse Boost | V _{OVP_BST} | VMID Rising | -- | 6 | -- | V |
| VMID OVP Hysteresis | V _{OVP_BST_HYS} | VMID Falling | -- | 200 | -- | mV |
| Battery UVP for Boost | V _{BATMIN} | Falling, I ² C Programmable Per 0.1V Optional 2.5V to 3.2V by I ² C per 0.1V (Default value is 3V) | 2.5 | -- | 3.2 | V |
| NTC Function | | | | | | |
| Current Source for NTC 10kΩ | ITS_10k | | 33 | 35 | 37 | μA |
| Load Switch for USBOUT | | | | | | |
| Supply Voltage | V _{SW} | | 2.5 | 5 | 5.5 | V |
| Load Switch On Resistance of MOSFET | R _{DS(ON)_SW} | $V_{MID} = 5V$, $I_O = 1000mA$ | -- | 35 | -- | mΩ |
| Load Switch UVP Delta | V _{SW_UVP_D} | VMID – VUSBOUT | -- | 1.4 | -- | V |
| Light Load Detection Current | I _{DET_10mA} | Detection current | -- | 10 | -- | mA |
| Thermal Regulation Threshold of the Load Switch | T _{REG_LSW} | Optional 100°C to 135°C by I ² C (Default value is 100°C) | -- | 100 | -- | °C |
| Adapter Detection | | | | | | |
| D+ Voltage Source | V _{D+_SRC} | | 0.5 | -- | 0.7 | V |
| V _{DAT_REF} Voltage | V _{DAT_REF} | | 0.25 | -- | 0.4 | V |
| VLGC Voltage | V _{LGC} | | 0.8 | -- | 2 | V |
| D- Sink Current | I _{DN_SINK} | | 50 | -- | 150 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|------------------------------|---|------|-----|------|------|
| USBOUT Attach/Detach Detection | | | | | | |
| USBOUT Attach Voltage | | I _{USBOUT} = 1.5μA | 1.4 | 1.6 | 1.8 | V |
| USBOUT Attach/Detach Threshold | | C _{USBOUT} = 40μF, Note 6 | 1 | 5 | 10 | μA |
| Detect Time 1 | | V _{BAT} = 3V, C _{OUT} = 30μF, 0X24[4:2] = 010 | -- | 375 | -- | ms |
| Detect Time 2 | | V _{BAT} = 3V, C _{OUT} = 50μF, 0X24[4:2] = 100 | -- | 600 | -- | ms |
| LDO 2.8V | | | | | | |
| Output Voltage | V _{OUT_2.8V} | C _{OUT} = 1μF | 2.66 | 2.8 | 2.94 | V |
| Output Current | I _{OUT_2.8V} | V _{DDA} > 3V | 10 | -- | -- | mA |
| The Time for VOUT Ready | t _{RDY_2.8V} | C _{OUT} = 1μF | 1 | -- | -- | ms |
| ADC Characteristics | | | | | | |
| Resolution | | | -- | 12 | -- | Bit |
| Measurement Error | V _{GERR} | V _{BAT} , TS | -10 | -- | 10 | mV |
| | | V _{BUS} , USBOUT | -50 | -- | 50 | mV |
| | | I _{BAT} < 1A | -100 | -- | 100 | mA |
| | | I _{BAT} > 1A | -10 | -- | 20 | % |
| | | I _{USBOUT} < 1A | -100 | -- | 100 | mA |
| | | I _{USBOUT} > 1A | -10 | -- | 10 | % |
| Conversion Time | T _{CONV} | | -- | -- | 25 | ms |
| Logic Inputs (SDA SCL) | | | | | | |
| SDA, SCL Input Threshold Voltage | High-Level | | 1.5 | -- | -- | V |
| | Low-Level | | -- | -- | 0.4 | |
| Open Drain Low Voltage | V _{ODL} | I _{SINK} = 1mA | -- | -- | 0.4 | V |
| I²C Timing Characteristics | | | | | | |
| SCL Clock Rate | f _{SCL} | V _{DDA} = 3.3V | -- | -- | 400 | kHz |
| Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated | t _{HD;STA} | | 0.6 | -- | -- | ms |
| Input Power | | | | | | |
| DCP Controller Power UVLO Threshold Voltage from VMID | V _{UVLO_R_DCP_CTRL} | Rising | 3.9 | 4.1 | 4.3 | V |
| UVLO Hysteresis | V _{UVLO_F_CP_CTRL} | Falling | 100 | 200 | 300 | mV |
| DCP Controller Supply Current | I _{DCP_CTRL} | 4.5V < V _{UID} < 5V | -- | 150 | 200 | μA |
| BC1.2 DCP Mode | | | | | | |
| DP and DM Shorting Resistance | R _{DPM_SHORT} | V _{DP} = 0.8V, I _{DM} = 1mA | -- | 157 | 200 | Ω |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------------|------------------------|------|-----|------|------|
| Resistance Between DP/DM and GND | R _{DCHG_SHORT} | DP = 0.8V | 350 | 656 | 1150 | kΩ |
| Voltage Threshold on DP1 under which the Device Goes Back to Divider Mode | V _{DPL_TH_DET} | Falling | 310 | 330 | 350 | mV |
| Hysteresis | V _{DPL_TH_DET_HYS} | Rising | -- | 50 | -- | mV |
| DIVIDER Mode | | | | | | |
| DP Output Voltage for DIVIDER Mode | V _{DP_2.7V} | V _{UID} = 5V | 2.57 | 2.7 | 2.84 | V |
| DM Output Voltage for DIVIDER Mode | V _{DM_2.7V} | V _{UID} = 5V | 2.57 | 2.7 | 2.84 | V |
| DP Output Impedance for DIVIDER Mode | R _{DP_PAD1} | I _{DP} = -5μA | 24 | 30 | 36 | kΩ |
| DM Output Impedance for DIVIDER Mode | R _{DM_PAD1} | I _{DM} = -5μA | 24 | 30 | 36 | kΩ |
| DP and DM Shorting Resistance | R _{PM_short} | | -- | 150 | 200 | Ω |
| 1.2V / 1.2V Mode | | | | | | |
| DP Output Voltage for 1.2V Mode | V _{DP_1.2V} | | 1.12 | 1.2 | 1.28 | V |
| DP Output Impedance for 1.2V Mode | R _{DP_PAD} | | 80 | 102 | 130 | kΩ |

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

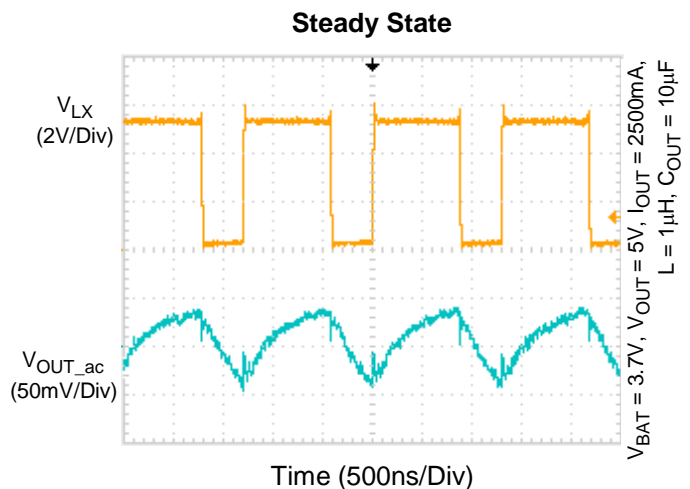
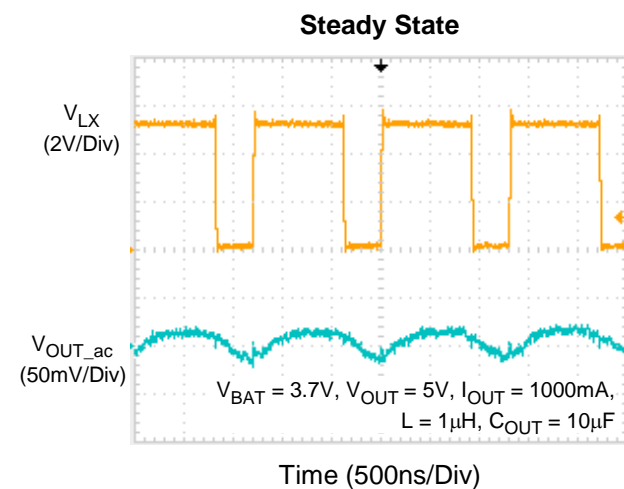
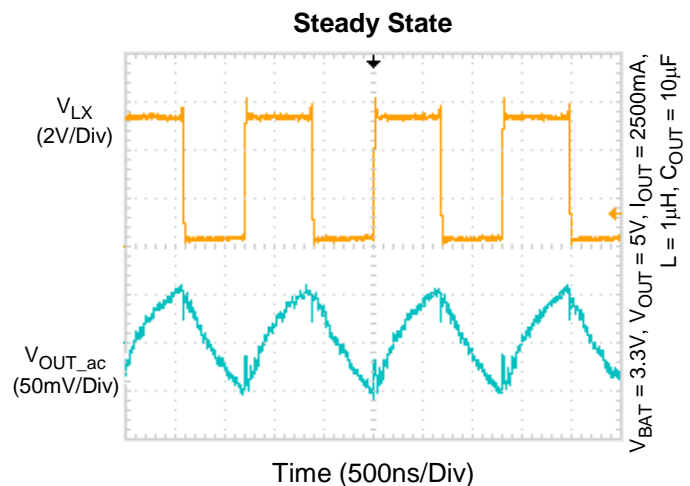
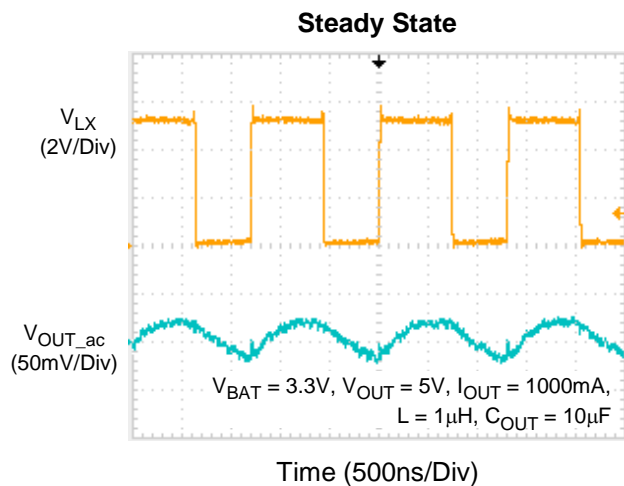
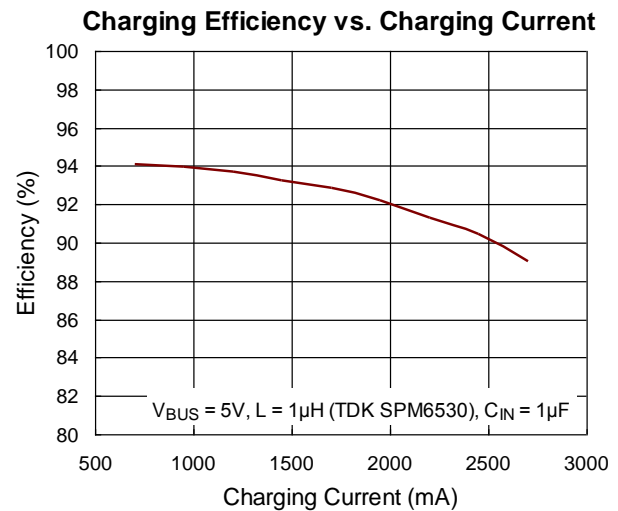
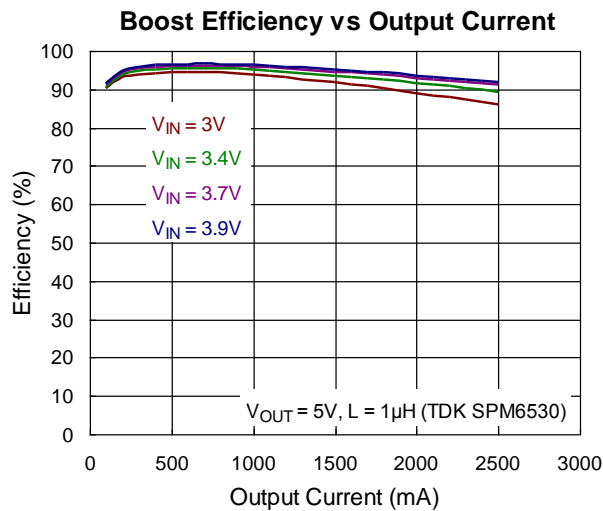
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Note 6. It will attach when only plug-in APPLE charging line.

Typical Operating Characteristics



Application Information

Switching Charger

The switching charger integrates a synchronous PWM controller with power MOSFETs to provide Minimum Input Voltage Regulation (MIVR), Average Input Current Regulation (AICR), high accuracy current and voltage regulation, and charge termination.

In charge mode, the switching charger supports a precision charging system for single cell. In boost mode, the switching charger works as the boost converter. And in high impedance mode, the switching charger stops charging or boosting and operates in a mode with low current from battery to reduce the power consumption when the portable device is in standby mode.

Notice that the switching charger does not integrate input power source (AC adapter or USB input) charging detection. Thus, the switching charger does not set the charge current automatically. The charge current needs to be set via I²C interface by the host. The switching charger application mechanism and I²C compatible interface are introduced in later sections.

Charge Mode Operation

Minimum Input Voltage Regulation (MIVR)

The switching charger features Minimum Input Voltage Regulation function to prevent input voltage drop due to insufficient current provided by the adaptor or USB input. If MIVR function is enabled, the input voltage decreases when the over current of the input power source occurs. VBUS is regulated at a predetermined voltage level which can be set as 4.2V to 4.8V per 0.1V by I²C interface. At this time, the current drawn by the switching charger equals to the maximum current value that the input power can provide at the predetermined voltage level, instead of the set value.

Table 1. MIVR Register Setting Table

| MIVR[2:0] | V _{MIVR} |
|-----------|-------------------|
| 000 | Disable |
| 001 | 4.2V |
| 010 | 4.3V |
| 011 | 4.4V |
| 100 | 4.5V |
| 101 | 4.6V |
| 110 | 4.7V (default) |
| 111 | 4.8V |

Charge Profile

The switching charger provides a precision Li-ion or Li-polymer charging solution for single-cell applications. Input current limit, charge current, termination current, charge voltage and input voltage MIVR are all programmable via the I²C interface. In charge mode, the switching charger has five control loops to regulate input current, charge current, charge voltage, input voltage MIVR and device junction temperature. During the charging process, all five loops (if MIVR is enabled) are enabled and the dominant one will take over the control.

For normal charging process, the Li-ion or Li-polymer battery is charged in three charging modes depending on the battery voltage. At the beginning of the charging process, the switching charger is in pre-charge mode. When the battery voltage rises above pre-charge threshold voltage (V_{PREC}), the switching charger enters fast-charge mode. Once the battery voltage is close to the regulation voltage (V_{BATREG}), the switching charger enters constant voltage mode.

Pre-Charge Mode

For life-cycle consideration, the battery cannot be charged with large current under low battery condition. When the I_{SENSEN} pin voltage is below pre-charge threshold voltage (V_{PREC}), the charger is in pre-charge mode with a weak charge current which equals to the pre-charge current (I_{PREC}). In pre-charge mode, the charger basically works as a Linear Charger. The pre-charge current also acts as the current limit when the I_{SENSEN} pin is shorted.

The Pre-Charge current levels are 200mA to 500mA programmed by I²C per 100mA.

Table 2. VPREC Register Setting Table

| VPREC[2:0] | Pre-Charge Threshold |
|------------|----------------------|
| 0000 | 2.3V |
| 0001 | 2.4V |
| 0010 | 2.5V |
| 0011 | 2.6V |
| 0100 | 2.7V |
| 0101 | 2.8V |
| 0110 | 2.9V |
| 0111 | 3V (default) |
| 1000 | 3.1V |
| 1001 | 3.2V |
| 1010 | 3.3V |
| 1011 | 3.4V |
| 1100 | 3.5V |
| 1101 | 3.6V |
| 1110 | 3.7V |
| 1111 | 3.8V |

Table 3. IPREC Register Setting Table

| IPREC[1:0] | Pre-Charge Current |
|------------|--------------------|
| 00 | 200mA |
| 01 | 300mA (default) |
| 10 | 400mA |
| 11 | 500mA |

Fast-Charge Mode and Settings

As the ISENSN pin rises above VPREC, the charger enters fast-charge mode and starts switching. Notice that the switching charger does not integrate input power source (AC adapter or USB input) detection. Thus, the switching charger does not set the charge current automatically. Unlike the linear charger (LDO), the switching charger (Buck converter) is a current amplifier. The current drawn by the switching charger is different from the current into the battery. The user can set the Average Input Current Regulation (AICR) and output charge current (ICHRG) respectively.

Cycle-by-Cycle Current Limit

The charger of the switching charger has an embedded cycle-by-cycle current limit for inductor. Once the inductor current touches the threshold, the charger stops charging immediately to prevent over

current from damaging the device. Notice that, the mechanism cannot be disabled by any way.

Adapter Detection

RT9481 includes the VBUS detection function. When VBUS plugs in, CHGGOODADP_STAT will reset to 0 once VBUS not rising exceeds 3.8V after 16ms. Besides, if VBUS falling below 3.8V during the charging interval, CHGBADADP_STAT is set as 1 to inform customer the poor adapter situation.

Average Input Current Regulation (AICR)

The AICR levels are 100mA to 2A programmed by I²C per 50mA.

Charge Current (ICHRG)

The charge current into the battery is determined by the sense resistor (RSENSE) and ICC setting by I²C. The voltage between the ISENSP and ISENSN pins is regulated to the voltage control by ICC setting.

As the RSENSE is 10mΩ, the Fast-Charge currents are 700mA to 2.7A programmed by I²C per 250mA.

Table 4. ICHG Register Setting Table

| ICHG[3:0] | VCC | ICHG RSENSE is 10mΩ |
|-----------|--------|---------------------|
| 0000 | 7mV | 0.7A (default) |
| 0001 | 9.5mV | 0.95A |
| 0010 | 12mV | 1.2A |
| 0011 | 14.5mV | 1.45A |
| 0100 | 17mV | 1.7A |
| 0101 | 1.95mV | 1.95A |
| 0110 | 2.2mV | 2.2A |
| 0111 | 2.45mV | 2.45A |
| 1000 | 2.7mV | 2.7A |

Constant Voltage Mode and Settings

The switching charger enters constant voltage mode when the VBAT voltage is close to the output-charge voltage (VBATREG). Once in this mode, the charge current begins to decrease. For default settings (charge current termination is disabled), the switching charger does not turn off and always regulates the battery voltage at VBATREG. However, once the charge current termination is enabled, the charger terminates if the charge current is below termination current (IEOC) in constant-voltage mode. The charge current termination function is controlled by the I²C interface.

After termination, a new charge cycle restarts when one of the following conditions is detected :

- ▶ The ISEN pin voltage falls below the V_{BATREG} as V_{REC} threshold.
- ▶ VBUS Power On Reset (POR).
- ▶ Enable bit toggle or Charger reset (via I²C interface)

Battery Charge Voltage (V_{BATREG})

The output-charge voltage is set by the I²C interface. Its range is from 3.65V to 4.6V per 25mV.

Termination Current (I_{EOC})

If the charger current termination is enabled (TE bit = "1"), the end-of-charge current is determined by both the termination current sense voltage (V_{EOC}) and sense resistor (R_{SENSE}). As R_{SENSE} is 10m Ω , I_{EOC} is set by the I²C interface from 150mA to 600mA.

Table 5. EOC Register Setting Table

| EOC[2:0] | VEOC | IEOC R_{SENSE} is 10m Ω |
|----------|---------|----------------------------------|
| 000 | Disable | Disable |
| 001 | 1.5mV | 150mA |
| 010 | 2mV | 200mA (default) |
| 011 | 2.5mV | 250mA |
| 100 | 3mV | 300mA |
| 101 | 4mV | 400mA |
| 110 | 5mV | 500mA |
| 111 | 6mV | 600mA |

VBUS Voltage Protection in Charge Mode

During charge mode, there are two protection mechanisms against if input power source capability is less than the charging current setting. One is AICR and the other is minimum input voltage regulation. A suitable level of AICR can prevent VBUS drop by the insufficient capability. As the AICR setting is not suitable, MIVR will regulate the VBUS in the setting level and sink the maximum current of power source.

Sleep Mode ($V_{VBUS} - V_{VBAT} < V_{SLP}$)

The switching charger enters sleep mode if the voltage drop between the VBUS and ISEN pin falls below V_{SLP} . In sleep mode, the reverse blocking switch and PWM are all turned off. This function prevents battery drain during poor or no input power source.

VBUS Over Voltage Protection

When VBUS rises above the input over voltage threshold, the switching charger stops charging and then sets fault status bits. The condition is released when VBUS falls below OVP threshold. The switching charger then resumes charging operation.

Reverse Boost Mode Operation Trigger and Operation

The switching charger features Boost support. When BOOST function is enabled, the synchronous boost control loop takes over the power MOSFETs. In boost mode, the VMID pin is regulated to 5V (typ.) to support other BOOST devices connected to the USB connector.

USBOUT Over-Voltage Protection

In boost mode, the output over voltage protection is triggered when the VMID voltage is above the output OVP threshold. When OVP occurs, the boost converter stops switching and turns off immediately.

Battery Protection

Battery Over-Voltage Protection in Charge Mode

The switching charger monitors the VBAT voltage for output over voltage protection. In charge mode, if the VBAT voltage rises above $V_{OVP_BAT} \times V_{BATREG}$, such as when the battery is suddenly removed, the switching charger stops charging and then sets fault status bits and sends out fault pulse at the INT pin. The condition is released when the VBAT voltage falls below $(V_{OVP_BAT} - \Delta V_{OVP_BAT}) \times V_{OVP_BAT}$. The switching charger then resumes charging process with default settings and the fault is cleared.

Low Battery Voltage Protection (LBP)

When the Battery voltage is lower than a specified value, the converter will stop switching. Until the battery voltage rises above the low battery voltage protection threshold plus hysteresis voltage value, the converter resumes switching. The low battery voltage protection can be programmed with 8 different levels (2.5V to 3.2V).

Table 6. LBP Register Setting Table

| LBP[2:0] | Low Battery Protection Level |
|----------|------------------------------|
| 000 | 2.5V |
| 001 | 2.6V |
| 010 | 2.7V |
| 011 | 2.8V |
| 100 | 2.9V |
| 101 | 3V (default) |
| 110 | 3.1V |
| 111 | 3.2V |

USB Battery Charging Specification

The RT9481 supports adapter detection for dedicated charging port, Charging downstream port and Standard downstream port by D- and D+.

USB Dedicated Charging Port Controller

The RT9481 supports an USB dedicated charging port (DCP) controller. The DCP controller detects USB data line voltage, and automatically provides the correct electrical signatures on the data lines (DM and DP) to charge compliant devices. D+ =2.7V and D- =2.0V. BC1.2 DCP, required to short the D+ Line to the D- Line and 1.2 V on both D+ and D- Lines.

IRQ and STA Operation

RT9481 summarize all IRQ items in the register table. All IRQ_status registers are implemented as reset after read. If IRQ_enable bit is Low, the IRQ_status bit will

not update status. IRQ_enable will mask IRQ_status to trigger IRQ Low, so the system can decide which interrupt is necessary.

When STA low to high or high to low IRQ will be trigger but STA will keep situation and cannot be masked only mask IRQ.

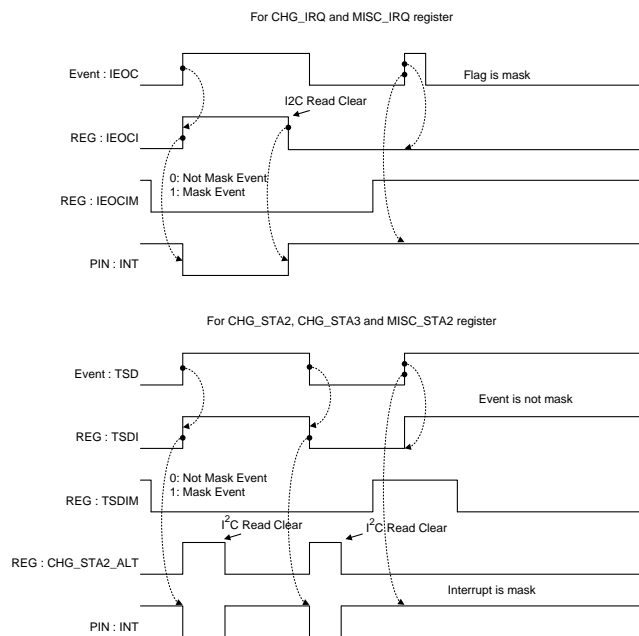


Figure 1. IRQ and STA Operation

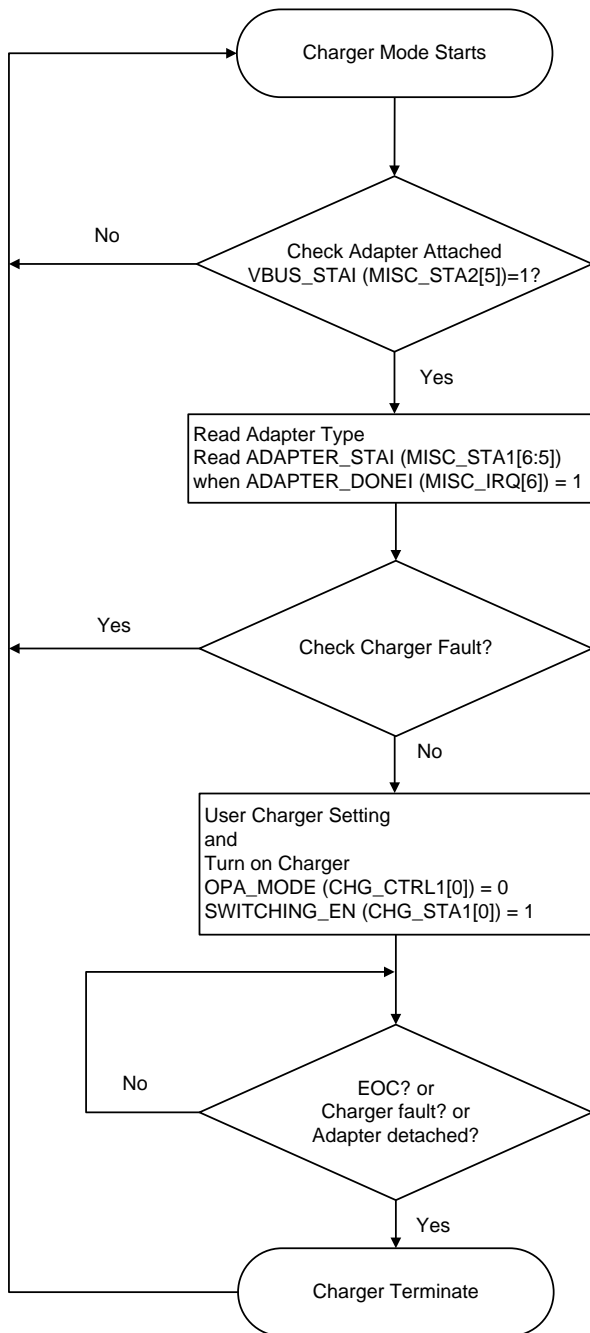


Figure 2. Charger Mode Flow

Charger Mode Flow

The Charger mode is start from adapter attached, the flag of VBUS_STAI (MISC_STA2[5]) will be set to high and the host can read this bit to check adapter attached or not. Then adapter type detection will auto start to detect the type of adapter with BC1.2 standard. Its detection result is

show in the flag ADAPTER_STAI (MISC_STA1[6:5]) when ADAPTER_DONE (MISC_IRQ[6]) is set.

The host could decide the user Charger setting by adapter type, like AICR or ICHG etc... For example, set IAICR to 0.5A, if the adapter type is SDP. Set IAICR to 1.5A, if the adapter type is CDP or DCP.

If there is no Charger fault event triggered in registers CHG_STAT1 or CHG_STAT2, the host can decide to turn on Charger or not. Set user Charger setting from registers CHG_CTRL1 to CHG_CTRL6 before turn on Charger. Please refer to I2C register map for detailed functional setting. To enable Charger by setting OPA_MODE (CHG_CTRL1[0]) to low and setting SWITCHING_EN (CHG_STA1[0]) to high.

When charging is start the host can check CHG_STAT (CHG_STA1[5]) to make sure the charging is in progress.

If system want to implement the charge and bypass feature, the host can set EN_LDSW (USBOUT_CTL[6]) to high to turn on Load Switch and set EN_DCP (USBOUT_CTL[7]) to high to turn on DCP Controller, then the power of adapter could bypass to device when battery is under charging.

Charger Terminate

There are three conditions to terminate Charger and the host could set SWITCHING_EN (CHG_STA1[0]) to low to turn off Charger.

End of Charge (EOC)

Set TE (CHG_CTRL1[1]) to high to enable Termination function, then the Charger will terminate automatically and CHTERMI (CHG_IRQ[7]) is set to high when the charging current is below IEOC (CHG_CTRL5[2:0]) and charging voltage is above re-charge threshold. The host could turn on Charger again when CHRCHGI (CHG_IRQ[5]) is set.

Charger Fault

The Charger automatically terminates when Charger fault event be triggered in Table 7.

Table 7. Charger Fault Event

| Charger Fault Event | Flag | Register |
|------------------------|---------------------|-------------|
| Power Status | PWR_Rdy = 0 | CHG_STA1[2] |
| Thermal Shutdown | TSD_STAT = 1 | CHG_STA2[7] |
| VBUS OVP | VBUSOVP_STAT = 1 | CHG_STA2[6] |
| Reverse Protection | CHRV_P_STAT = 1 | CHG_STA2[5] |
| Battery OVP | CHBATOV_STAT = 1 | CHG_STA2[4] |
| Good Adaptor Detection | CHGGOODADP_STAT = 0 | CHG_STA2[1] |
| Bad Adaptor Detection | CHGBADADP_STAT = 1 | CHG_STA2[0] |

Adapter Detach

The flag of VBUS_STAI will be set to low when adapter detached and it will terminate Charger directly.

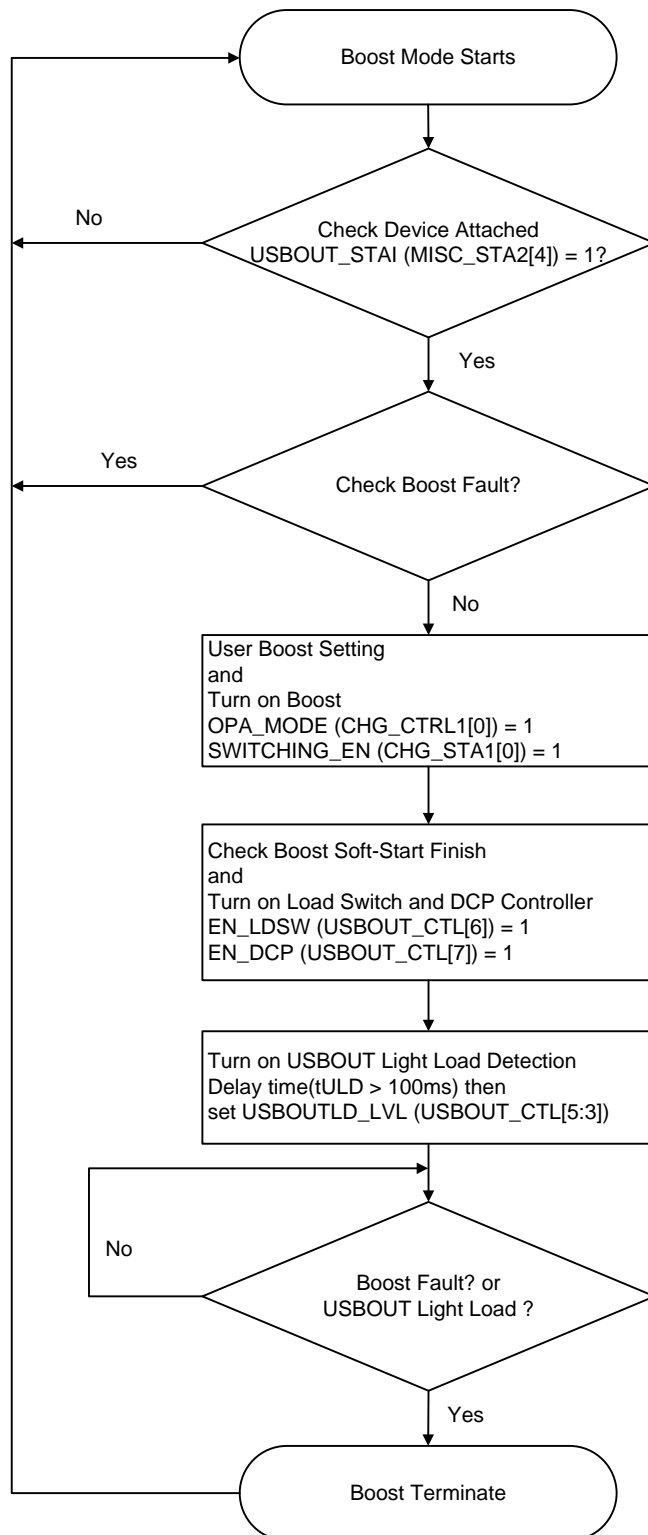


Figure 3. Boost Mode Flow

Boost Mode Flow

The Boost mode could start from device attached, and the flag of USBOUT_STAI (MISC_STA2[4]) will be set to high for indicate the device attached. The USBOUT attach detection is control by register ATTACH_CTL[5].

If there is no any Boost fault triggered in registers CHG_STAT2 or BST_IRQ or MISC_IRQ, the host can decide to turn on Boost or not. The host can set user Boost setting before turn on the Boost from registers CHG_CTRL1 to CHG_CTRL6 and please refer to I2C register map for detailed functional setting.

The Boost could be enable by set OPA_MODE (CHG_CTRL1[0]) to high and setting SWITCHING_EN (CHG_STA1[0]) to high.

Before enable the Load Switch suggest to wait Boost soft start (CHG_IRQ[3]) finish, it can guarantee the Boost ready for output.

Then the host could set EN_LDSW (USBOUT_CTL[6]) to high to turn on Load Switch and the Boost would start output current to device. For let device identify the power bank is a powerful adapter, to set EN_DCP (USBOUT_CTL[7]) to high to turn on DCP controller at the same time.

USBOUT light load detection (USBOUTLD_CTL[5:3]) can help the host to check the device charging full or device detached by the condition of USBOUT current is under the threshold or not. But according to USB standard, the device will start charging after it connect to adapter 100 millisecond. We suggest to add delay time t_{ULD} over 100 millisecond before enable USBOUT light load detection after Load Switch turn on. It could avoid USBOUT light load detection trigger early.

The host could read BOOST_STAT (CHG_STA1) to make sure the Boost is in progress.

Discharging Terminate

There are two conditions to terminate discharging.

Boost Fault

The Boost automatically terminates when Boost fault event be triggered in Table 8.

Table 8. Boost Fault Event

| Boost Fault Event | Flag | Register |
|-----------------------------------|------------|-------------|
| Thermal Shutdown | TSD_STAT | CHG_STA2[2] |
| Boost Thermal Shutdown | BSTTSDI | BST_IRQ[7] |
| VMID Over Voltage Protect | BSTVMIDVPI | BST_IRQ[6] |
| Battery Voltage is too Low | BSTLOWVI | BST_IRQ[5] |
| Load Switch Short Current Protect | LDSW_SCPI | MISC_IRQ[5] |
| VMID Short Current Protect | VMIDSCPI | MISC_IRQ[1] |
| VMID Under Voltage Protect | VMIDUVPI | MISC_IRQ[0] |

USBOUT Light Load

It means device charging full or device detached when USBOUTLD_STAT (MISC_STA2) set to high. According to USBOUTLD_STAT, the host could decide to turn off Boost or not.

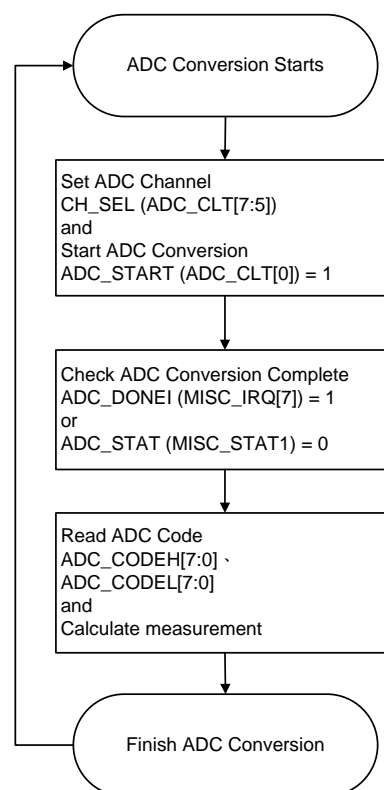


Figure 4. ADC Conversion Operation Flow

ADC Conversion Operation Flow

Figure 4 shows ADC conversion operation flow. ADC conversion starts from set ADC channel CH_SEL (ADC_CLT[7:5]) and set ADC_START (ADC_CLT[0]) to high. ADC conversion time is 25ms and ADC_DONEI (MISC_IRQ[7]) will set to high and ADC_STAT (MISC_STAT1) will set to low also, the host could read them to make sure ADC conversion completes.

The host could read ADC code high byte (ADC_CODEH[7:0]) and low byte (ADC_CODEL[7:0]) to calculate the voltage or current measurement relative to ADC channel.

Table 9 shows the every measurement equation of ADC channel. Please pay attention to the calculation of IBAT, it need to consider the setting of ICHG (CHG_CTRL6[7:4]).

ADC code format is unsigned. If operation is Charger mode, IBAT means battery charging current. If operation is boost mode, IBAT means battery discharging current.

The code of IBAT is invalid if SWITCHING_EN (CHG_STA1[0]) is set to low. And the code of IUSBOUT is invalid if EN_LDSW (USBOUT_CTL[6]) is set to low.

The TS pin will automatic output 35uA during ADC TS channel under conversion. It will cause the IR drop on NTC thermistor and then ADC measure the voltage on TS pin. The host could get the temperature by mapping the voltage. We suggest to use 10kΩ NTC which the beta (B25/85) is 3435k, like SEMITEC 103AT.

Table 9. Calculate Voltage or Current Measurement

| ADC Channel | Measurement Equation | Measurement Range |
|-------------|--|-------------------|
| VBAT | $VBAT = ((ADC_CODEH \times 256) + ADC_CODEL) \times 1.25 \text{ mV}$ | 0V to VDDA |
| VBUS | $VBUS = ((ADC_CODEH \times 256) + ADC_CODEL) \times 6.25 \text{ mV}$ | 1V to 18V |
| USBOUT | $USBOUT = ((ADC_CODEH \times 256) + ADC_CODEL) \times 6.25 \text{ mV}$ | 1V to 6V |
| TS | $TS = ((ADC_CODEH \times 256) + ADC_CODEL) \times 1.25 \text{ mV}$ | 0V to VDDA |
| IBAT | $IBAT = ((ADC_CODEH \times 256) + ADC_CODEL) \times ICHG \times 1.25 \text{ mA}$ | 0A to 6A |
| IUSBOUT | $IUSBOUT = ((ADC_CODEH \times 256) + ADC_CODEL) \times 2.5 \text{ mA}$ | 0A to 6A |

Table 10. Protection Items

| | Protection Type | Threshold (typical) Refer to Electrical Spec. | Protection Methods | IC Shutdown Delay Time | Reset Method |
|--------|------------------|--|--|------------------------|--|
| VBAT | LBP | VBAT < LPB setting | Exist boost mode | None | VDDA power reset |
| | OVP | VBAT > 1.07 x CHG_CV | Stop charging | None | VDDA power reset or VBAT falling to 1.02 x CHG_CV |
| VDDA | UVP | VDDA < 2.35V | analog circuit disable | None | VDDA > 2.5V |
| VBUS | OVP | VBUS > 6V | Stop charging, UUG disable | None | VDDA power reset or VBUS falling to VBUS_OVP-hysteresis |
| | Bad adapter | VBUS < 3.8V | None | None | VDDA power reset or VBUS rising to VBUS_BAD + hysteresis |
| | Good adapter | None | None | None | None |
| | RVP | VBUS < VBAT | Stop charging, UUG disable | None | VDDA power reset or VBUS rising above VBAT |
| | TREG | Temp. \approx Thermal regulation setting | None | None | VDDA power reset or thermal loop release |
| | MIVR | VBUS \approx MIVR setting | None | None | VDDA power reset or MIVR loop release |
| | AICR | IBUS \approx AICR setting | None | None | VDDA power reset or AICR loop release |
| VMID | OVP | N/A | N/A | | N/A |
| | UVP | 3.5V | Absolute voltage below threshold | | sEn_VMIDUVP |
| | SCP | 3.5V | Absolute voltage below threshold | | sEn_VMIDUVP |
| USBOUT | LDSWREG | 1.5A/2A/2.5A/3A | Load current is above current limit | | sEn_LDSW |
| | LDSWSCP | VDS~1.4V | VDS voltage is too high | | sEn_LDSW |
| | Current limit | 1.5A/2A/2.5A/3A | Load current reach to limit-point | | sEn_LDSW |
| Boost | Current limit | Inductor current > 6A | cycle by cycle, inductor current limit | None | Inductor current < 6A |
| OTP | Thermal Shutdown | Temp > 160°C | Stop charging, UUG disable | None | Temp < 160°C |

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For WQFN-24L 4x4 package, the thermal resistance, θ_{JA} , is 28°C /W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (28^\circ\text{C} / \text{W}) = 3.57\text{W for WQFN-24L 4x4 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

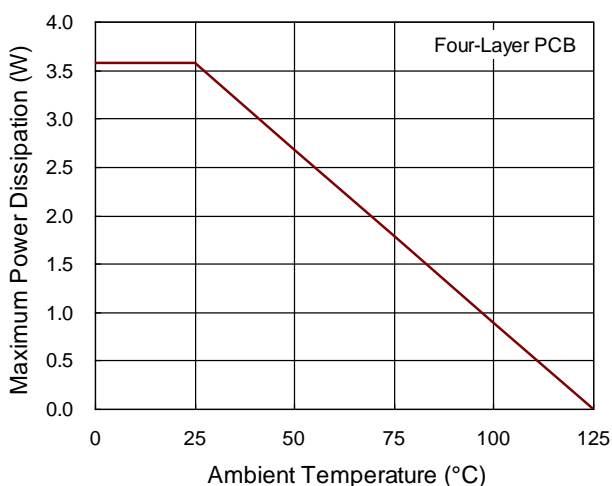


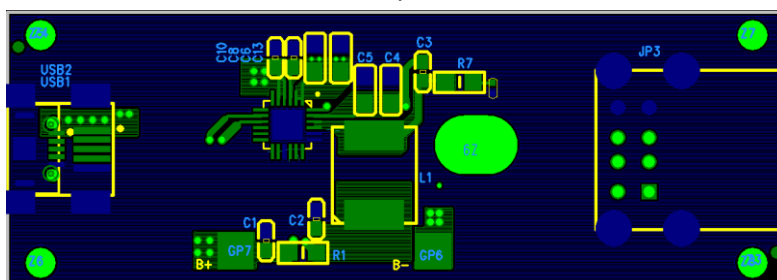
Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

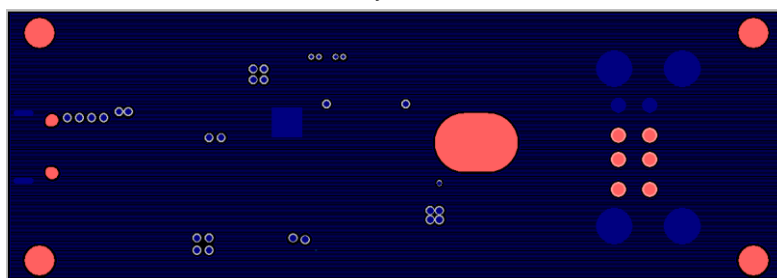
Some PCB layout guidelines for optimal performance of RT9481 list as following. Following figure shows the real PCB layout considerations and it is based on the real component size whose unit is millimeter (mm).

- ▶ Place the input and output capacitors as close to the input and output pins as possible.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ The output inductor and boot capacitor should be placed close to the chip and LX pins.
- ▶ The battery voltage sensing point should be placed after the output capacitor.
- ▶ To optimize current sense accuracy, connect the traces to RSENSE with Kelvin sense connection by ISENSEN and ISENSP.
- ▶ LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- ▶ Add Snubber in LX: 2Ω resistor 0805 package and 1nF capacitor.

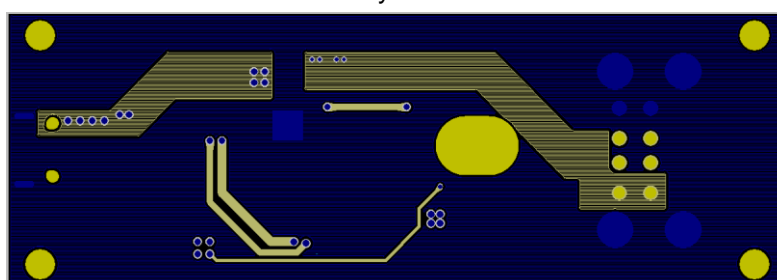
Top :



layer2 :



Layer3 :



Bottom :

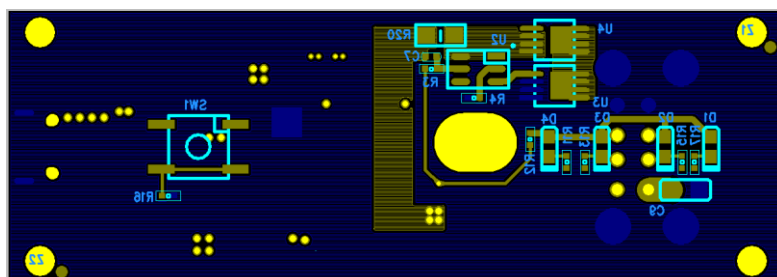


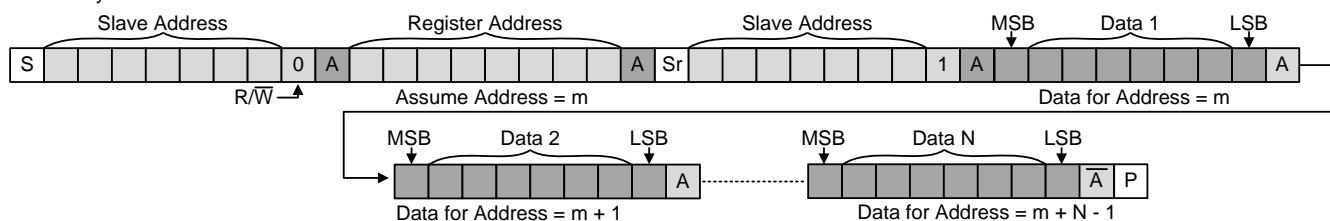
Figure 6. PCB Layout Guide

I²C Interface

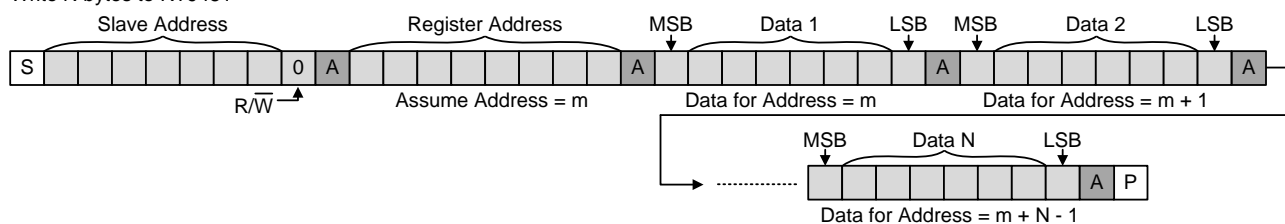
RT9481 I²C slave address = 7'b1101100.

I²C interface support fast mode (bit rate up to 400kb/s). The write or read bit stream ($N \geq 1$) is shown below :

Read N bytes from RT9481



Write N bytes to RT9481



I²C Register Map

Register of the SWCHG

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|--------------|------------------|-------------|---|-------------|-------------|---------|------------|-----------------|------|---------------|
| Low BAT CTRL | 0X00 | Meaning | Fix_ Freq | Sel_ SWFreq | Higher_ OCP | HZ | LBP Enable | LBP[2:0] | | |
| | | Default | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Fix_Freq | | | Control the switching frequency to be dynamic or fix 0 : Auto-change frequency 1 : Fixed frequency (default) | | | | | | | |
| Sel_ SWFreq | | | The switching frequency selection bit (Charger/ Boost) 0 : The switching frequency is 1.5MHz 1 : The switching frequency is 0.75MHz (default) | | | | | | | |
| Higher_ OCP | | | Higher_OCP enable 0 : Disable (default) 1 : Higher IL OCP level selection of buck mode and boost mode | | | | | | | |
| HZ | | | 0 : Not high impedance mode (default) 1 : High impedance | | | | | | | |
| LBP Enable | | | Low Battery Protection Enable 0 : Disable 1 : Enable (default) | | | | | | | |
| LBP[2:0] | | | Define Low Battery Protection Level. The default voltage is 3V. | | | | | | | |
| | | | Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
| | | | 000 | 2.5V | 010 | 2.7V | 100 | 2.9V | 110 | 3.1V |
| | | | 001 | 2.6V | 011 | 2.8V | 101 | 3V (default) | 111 | 3.2V |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|-------------|---|----------------|--------|---------|--------|---------|--------|------------|
| Charger Control 1 | 0X01 | Meaning | IAICR[5:0] | | | | | | TE | OPA_ MODE |
| | | Default | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| IAICR[5:0] | | | Define AICR current. The default current is 0.5A. | | | | | | | |
| | | | Code | Current | Code | Current | Code | Current | Code | Current |
| | | | 000000 | Disable | 010000 | 0.8A | 100000 | 1.6A | 110000 | 2A |
| | | | 000001 | 0.1A | 010001 | 0.85A | 100001 | 1.65A | 110001 | 2A |
| | | | 000010 | 0.1A | 010010 | 0.9A | 100010 | 1.7A | 110010 | 2A |
| | | | 000011 | 0.15A | 010011 | 0.95A | 100011 | 1.75A | 110011 | 2A |
| | | | 000100 | 0.2A | 010100 | 1A | 100100 | 1.8A | 110100 | 2A |
| | | | 000101 | 0.25A | 010101 | 1.05A | 100101 | 1.85A | 110101 | 2A |
| | | | 000110 | 0.3A | 010110 | 1.1A | 100110 | 1.9A | 110110 | 2A |
| | | | 000111 | 0.35A | 010111 | 1.15A | 100111 | 1.95A | 110111 | 2A |
| | | | 001000 | 0.4A | 011000 | 1.2A | 101000 | 2A | 111000 | 2A |
| | | | 001001 | 0.45A | 011001 | 1.25A | 101001 | 2A | 111001 | 2A |
| | | | 001010 | 0.5A (default) | 011010 | 1.3A | 101010 | 2A | 111010 | 2A |
| | | | 001011 | 0.55A | 011011 | 1.35A | 101011 | 2A | 111011 | 2A |
| | | | 001100 | 0.6A | 011100 | 1.4A | 101100 | 2A | 111100 | 2A |
| | | | 001101 | 0.65A | 011101 | 1.45A | 101101 | 2A | 111101 | 2A |
| | | | 001110 | 0.7A | 011110 | 1.5A | 101110 | 2A | 111110 | 2A |
| | | | 001111 | 0.75A | 011111 | 1.55A | 101111 | 2A | 111111 | 2A |
| TE | | | Termination enable 0 : Disable charge current termination (default) 1 : Enable charge current termination | | | | | | | |
| OPA_MODE | | | 0 : Charger mode (default) 1 : Boost mode | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|------------|--|---------|--------|----------------|--------|---------|----------|------------|
| Charger Control 2 | 0X02 | Meaning | CHG_CV[5:0] | | | | | | Reserved | Reserved |
| | | Default | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| CHG_CV[5:0] | | | Define battery regulation voltage. The delta-V of the Battery regulation voltage is 25mV. The default voltage is 4.2V. | | | | | | | |
| | | | Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
| | | | 000000 | 3.65V | 010000 | 4.05V | 100000 | 4.45V | 110000 | 4.6V |
| | | | 000001 | 3.675V | 010001 | 4.075V | 100001 | 4.475V | 110001 | 4.6V |
| | | | 000010 | 3.7V | 010010 | 4.1V | 100010 | 4.5V | 110010 | 4.6V |
| | | | 000011 | 3.725V | 010011 | 4.125V | 100011 | 4.525V | 110011 | 4.6V |
| | | | 000100 | 3.75V | 010100 | 4.15V | 100100 | 4.55V | 110100 | 4.6V |
| | | | 000101 | 3.775V | 010101 | 4.175V | 100101 | 4.575V | 110101 | 4.6V |
| | | | 000110 | 3.8V | 010110 | 4.2V (default) | 100110 | 4.6V | 110110 | 4.6V |
| | | | 000111 | 3.825V | 010111 | 4.225V | 100111 | 4.6V | 110111 | 4.6V |
| | | | 001000 | 3.85V | 011000 | 4.25V | 101000 | 4.6V | 111000 | 4.6V |
| | | | 001001 | 3.875V | 011001 | 4.275V | 101001 | 4.6V | 111001 | 4.6V |
| | | | 001010 | 3.9V | 011010 | 4.3V | 101010 | 4.6V | 111010 | 4.6V |
| | | | 001011 | 3.925V | 011011 | 4.325V | 101011 | 4.6V | 111011 | 4.6V |
| | | | 001100 | 3.95V | 011100 | 4.35V | 101100 | 4.6V | 111100 | 4.6V |
| | | | 001101 | 3.975V | 011101 | 4.375V | 101101 | 4.6V | 111101 | 4.6V |
| | | | 001110 | 4V | 011110 | 4.4V | 101110 | 4.6V | 111110 | 4.6V |
| | | | 001111 | 4.025V | 011111 | 4.425V | 101111 | 4.6V | 111111 | 4.6V |
| | | | CHG : 3.65V + CHG_CV x 0.025V, max. : 4.6V | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) | | | |
|----------------------|------------------|------------|--|---------|--------|--|--------|---------|---------------|----------------|--|--|--|
| Charger Control 3 | 0X03 | Meaning | Boost _CV[5:0] | | | | | | TREG_SEL[1:0] | | | | |
| | | Default | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | | | |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | | |
| Boost _CV[5:0] | | | Define Boost regulation voltage. The delta-V of the Boost voltage is 25mV. The default voltage is 5.1V. | | | | | | | | | | |
| | | | Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage | | | |
| | | | 000000 | 3.625V | 010000 | 4.025V | 100000 | 4.425V | 110000 | 4.825V | | | |
| | | | 000001 | 3.65V | 010001 | 4.05V | 100001 | 4.45V | 110001 | 4.85V | | | |
| | | | 000010 | 3.675V | 010010 | 4.075V | 100010 | 4.475V | 110010 | 4.875V | | | |
| | | | 000011 | 3.7V | 010011 | 4.1V | 100011 | 4.5V | 110011 | 4.9V | | | |
| | | | 000100 | 3.725V | 010100 | 4.125V | 100100 | 4.525V | 110100 | 4.925V | | | |
| | | | 000101 | 3.75V | 010101 | 4.15V | 100101 | 4.55V | 110101 | 4.95V | | | |
| | | | 000110 | 3.775V | 010110 | 4.175V | 100110 | 4.575V | 110110 | 4.975V | | | |
| | | | 000111 | 3.8V | 010111 | 4.2V | 100111 | 4.6V | 110111 | 5V | | | |
| | | | 001000 | 3.825V | 011000 | 4.225V | 101000 | 4.625V | 111000 | 5.025V | | | |
| | | | 001001 | 3.85V | 011001 | 4.25V | 101001 | 4.65V | 111001 | 5.05V | | | |
| | | | 001010 | 3.875V | 011010 | 4.275V | 101010 | 4.675V | 111010 | 5.075V | | | |
| | | | 001011 | 3.9V | 011011 | 4.3V | 101011 | 4.7V | 111011 | 5.1V (default) | | | |
| | | | 001100 | 3.925V | 011100 | 4.325V | 101100 | 4.725V | 111100 | 5.125V | | | |
| | | | 001101 | 3.95V | 011101 | 4.35V | 101101 | 4.75V | 111101 | 5.15V | | | |
| | | | 001110 | 3.975V | 011110 | 4.375V | 101110 | 4.775V | 111110 | 5.175V | | | |
| | | | 001111 | 4V | 011111 | 4.4V | 101111 | 4.8V | 111111 | 5.2V | | | |
| | | | | | | Boost : 3.625 + Boost _CV x 0.025V, Boost max.: 5.2V | | | | | | | |
| | | | TREG_SEL[1:0] | | | Define thermal regulation level | | | | | | | |
| 00 : 100°C | | | | | | | | | | | | | |
| 01 : 120°C (default) | | | | | | | | | | | | | |
| 10 : 135°C | | | | | | | | | | | | | |
| 11 : 135°C | | | | | | | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|------------|--|---------|-------|----------|------|----------|------|--------------------|
| Charger Control 4 | 0X04 | Meaning | TMR2X_EN | JEITA | WT_FC | | | WT_PRC | | EN_TMR |
| | | Default | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| TMR2X_EN | | | Run charge timer in half clock rate during MIVR, AICR and thermal regulation. 0 : Disable 2X extended charger timer 1 : Enable 2X extended charger timer (default) | | | | | | | |
| JEITA | | | JEITA function 0 : Charging regulation current is ICHG (default) 1 : Charging regulation current is ICHG/2 | | | | | | | |
| WT_FC | | | Define Fast charge Timer. The default time is 20 hours. | | | | | | | |
| | | | Code | Hours | Code | Hours | Code | Hours | Code | Hours |
| | | | 000 | 6 hours | 010 | 10 hours | 100 | 14 hours | 110 | 18 hours |
| | | | 001 | 8 hours | 011 | 12 hours | 101 | 16 hours | 111 | 20 hours (default) |
| WT_PRC | | | Define Pre-charge charge Timer 00 : 30mins 01 : 45mins 10 : 60mins (default) 11 : 60mins | | | | | | | |
| EN_TMR | | | 0 : Disable internal timer function (default) 1 : Enable internal timer function | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|------------|---|---------|------|-----------------|------|----------|------|----------------|
| Charger Control 5 | 0X05 | Meaning | MIVR[2:0] | | | IPREC[1:0] | | EOC[2:0] | | |
| | | Default | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| MIVR[2:0] | | | Define VMIVR voltage. The default voltage is 4.7V. | | | | | | | |
| | | | Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
| | | | 000 | Disable | 010 | 4.3V | 100 | 4.5V | 110 | 4.7V (default) |
| | | | 001 | 4.2V | 011 | 4.4V | 101 | 4.6V | 111 | 4.8V |
| IPREC[1:0] | | | Define Pre-Charge Current 00 : 200mA 01 : 300mA (default) 10 : 400mA 11 : 500mA | | | | | | | |
| EOC[2:0] | | | Define Termination Current (IEOC RSENSE is 10mΩ). The default current is 200mA. | | | | | | | |
| | | | Code | Current | Code | Current | Code | Current | Code | Current |
| | | | 000 | Disable | 010 | 200mA (default) | 100 | 300mA | 110 | 500mA |
| | | | 001 | 150mA | 011 | 250mA | 101 | 400mA | 111 | 600mA |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|------------|--|----------------------|------|----------------|------------|-------------|------|-------------|
| Charger Control 6 | 0X06 | Meaning | ICHG[3:0] | | | | VPREC[3:0] | | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ICHG[3:0] | | | Define charging regulation current. The default current is 7mV (0.7A). | | | | | | | |
| | | | Code | Current | Code | Current | Code | Current | Code | Current |
| | | | 0000 | 7mV (0.7A) (default) | 0100 | 17mV (1.7A) | 1000 | 27mV (2.7A) | 1100 | 27mV (2.7A) |
| | | | 0001 | 9.5mV (0.95A) | 0101 | 19.5mV (1.95A) | 1001 | 27mV (2.7A) | 1101 | 27mV (2.7A) |
| | | | 0010 | 12mV (1.2A) | 0110 | 22mV (2.2A) | 1010 | 27mV (2.7A) | 1110 | 27mV (2.7A) |
| | | | 0011 | 14.5mV (1.45A) | 0111 | 24.5mV (2.45A) | 1011 | 27mV (2.7A) | 1111 | 27mV (2.7A) |
| | | | External Sensing R : Charge current sense voltage (current equivalent for 10mΩ sense resistor) | | | | | | | |
| VPREC[3:0] | | | Define Pre-Charge Threshold. The default voltage is 3V. | | | | | | | |
| | | | Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
| | | | 0000 | 2.3V | 0100 | 2.7V | 1000 | 3.1V | 1100 | 3.5V |
| | | | 0001 | 2.4V | 0101 | 2.8V | 1001 | 3.2V | 1101 | 3.6V |
| | | | 0010 | 2.5V | 0110 | 2.9V | 1010 | 3.3V | 1110 | 3.7V |
| | | | 0011 | 2.6V | 0111 | 3V (default) | 1011 | 3.4V | 1111 | 3.8V |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|----------------|--------------------|----------|----------|----------|----------|----------|------|-------------------|
| Charger Control 7 | 0X07 | Meaning | Reserved | Reserved | Reserved | Reserved | Reserved | TDEG_EOC | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| TDEG_EOC[2:0] | | | EOC de-glitch time | | | | | | | |
| | | | Code | Time | Code | Time | Code | Time | Code | Time |
| | | | 000 | 32μs | 010 | 128μs | 100 | 4ms | 110 | 16ms |
| | | | 001 | 64μs | 011 | 256μs | 101 | 8ms | 111 | 32ms (default) |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-----------------|------------------|------------|---|----------|----------|----------|------------|---------|-----------|--------------|
| Charger Status1 | 0X08 | Meaning | UUGPUMP_STAT | VBAT_LVL | CHG_STAT | CHG_Done | BOOST_STAT | PWR_Rdy | SWBASE_EN | SWITCHING_EN |
| | | Default | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | Read/Write | R | R | R | R | R | R | R/W | R/W |
| UUGPUMP_STAT | | | UUG pump enable status 0 : UUG pump is disable 1 : UUG pump is enable | | | | | | | |
| VBAT_LVL | | | Battery voltage level detect under charging 0 : Battert voltage is lower than pre-charge level 1 : Battery voltage is higher than fast-charge level | | | | | | | |
| CHG_STAT | | | Charging Status 0 : Charging is not in progress 1 : Charging is in progress | | | | | | | |
| CHG_Done | | | Charger Done indication bit 0 : Charging is not done 1 : Charging is done | | | | | | | |
| BOOST_STAT | | | 0 : Not in Boost mode 1 : Boost mode | | | | | | | |
| PWR_Rdy | | | Power status bit 0 : VBUS > VBUS_OVP or VBUS < VBUS_UVLO or VBUS < ISENSEN + VSLP (Power Fault) 1 : VBUS_UVLO < VBUS < VBUS_OVP & VBUS > ISENSEN + VSLP (Power Ready) | | | | | | | |
| SWBASE_EN | | | Switching charger base circuit enable 0 : Disabled 1 : Enabled | | | | | | | |
| SWITCHING_EN | | | Charger/ Boost enable 0 : Charger/ Boost is disabled 1 : Charger/ Boost is enabled | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|------------------|------------------|------------|--|--------------|------------|--------------|----------|----------|-----------------|----------------|
| Charger Status 2 | 0X09 | Meaning | TSD_STAT | VBUSOVP_STAT | CHRVP_STAT | CHBATOV_STAT | Reserved | Reserved | CHGGOODADP_STAT | CHGBADADP_STAT |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | Read/Write | R | R | R | R | R | R | R | R |
| TSD_STAT | | | Thermal shutdown fault. Set when the die temperature exceeds thermal shutdown threshold. 0 : Thermal shutdown is not on going 1 : Thermal shutdown is on going | | | | | | | |
| VBUSOVP_STAT | | | VBUS over voltage protection. Set when VBUS > VIN_OVP is detected. 0 : VBUS is not over voltage 1 : VBUS is over voltage | | | | | | | |
| CHRVP_STAT | | | Charger fault. Reverse protection fault (VBUS < ISENSEN + VSLP) 0 : Reverse protection is not occur 1 : Reverse protection is occur | | | | | | | |
| CHBATOV_STAT | | | Charger fault. Battery OVP. 0 : Battery is not OVP 1 : Battery is OVP | | | | | | | |
| CHGGOODADP_STAT | | | Good adaptor detection. It is only enabled in the VBUS plug-in. Once it pass the detection, it will always high and enable charging. 0 : Adaptor is not good adaptor 1 : Adaptor is good adaptor | | | | | | | |
| CHGBADADP_STAT | | | Bad adaptor detection. It is used to indicate the adaptor input voltage is lower than 3.8V during the charging 0 : Adaptor is not bad adaptor 1 : Adaptor is bad adaptor | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|------------------|------------------|------------|--|-------------|-------------|-------------|----------|----------|----------|---------------|
| Charger Status 3 | 0X0A | Meaning | CHTREG_STAT | CHMIVR_STAT | CHAICR_STAT | CHRCHG_STAT | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| CHTREG_STAT | | | Charger warning. Thermal regulation loop active. 0 : Thermal regulation loop is not active 1 : Thermal regulation loop is active | | | | | | | |
| CHMIVR_STAT | | | Charger warning. Input voltage MIVR loop active. 0 : MIVR loop is not active 1 : MIVR loop is active | | | | | | | |
| CHAICR_STAT | | | Charger warning. Input current AICR loop active. 0 : AICR loop is not active 1 : AICR loop is active | | | | | | | |
| CHRCHG_STAT | | | Indicate battery voltage is below re-charge level under charging 0: Battery voltage higher re-charge level 1 : Battery voltage lower re-charge level | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|---------------|------------------|-------------|--|------|----------|----------|-------------|----------|----------------|----------------|
| CHG_ IRQ | 0X0B | Meaning | CHTER MI | IEOC | CHRC HGI | CHTM RFI | SOFTSTA RTI | Reserved | CHG_ STAT2_ALT | CHG_ STAT3_ALT |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/ Write | R/C | R/C | R/C | R/C | R/C | R/W | R/C | R/C |
| CHTERMI | | | Charge terminated. | | | | | | | |
| IEOC | | | Charge current is lower than EOC current. | | | | | | | |
| CHRCHGI | | | Re-Charge request. | | | | | | | |
| CHTMRFI | | | Charger fault. time-out (fault). | | | | | | | |
| SOFTSTARTI | | | Charger or Boost soft-start finish | | | | | | | |
| CHG_STAT2_ALT | | | The status of CHG_STAT2 register is change | | | | | | | |
| CHG_STAT3_ALT | | | The status of CHG_STAT3 register is change | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------|------------------|------------|---|--------------|----------|----------|----------|----------|----------|------------|
| BST_IRQ | 0X0C | Meaning | BSTTSDI | BSTVMID OVPI | CHRC HGI | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/C | R/C | R/C | R/W | R/W | R/W | R/W | R/W |
| BSTTSDI | | | Boost fault. Thermal shutdown; auto set OPA_MODE and SWITCHING_EN to low. | | | | | | | |
| BSTVMIDOVPI | | | Boost fault. VMID OVP; auto set OPA_MODE and SWITCHING_EN to low. | | | | | | | |
| BSTLOWVI | | | Boost fault. Battery voltage is too low; auto set OPA_MODE and SWITCHING_EN to low. | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|--------------------------|------------------|------------|--|----------------|----------------|---------------|----------|----------|-------------------|-----------------|
| Charger Status 2 Control | 0X0D | Meaning | TSDI_STATM | VBUSOV_P_STATM | CHRV_P_STATM | CHBATOV_STATM | Reserved | Reserved | CHGGOODA_DP_STATM | CHGBADADP_STATM |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| TSDI_STATM | | | Thermal shutdown interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VBUSOV_P_STATM | | | VBUS over voltage protection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHRV_P_STATM | | | Reverse protection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHBATOV_STATM | | | Battery OVP interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHGGOODADP_STATM | | | Good adaptor detection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHGBADADP_STATM | | | Bad adaptor detection interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
| Charger Status 3 Control | 0X0E | Meaning | CHTREG_STATM | CHMIVR_STATM | CHAI_C_R_STATM | CHGRCHG_STATM | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| CHTREG_STATM | | | Thermal regulation loop active interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHMIVR_STATM | | | Input voltage MIVR loop active interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHAI_C_R_STATM | | | Input current AICR loop active interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHGRCHG_STATM | | | Battery voltage re-charge level interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|---------------------|------------------|------------|---|-------------|-----------|----------|-------------|----------|---------------|---------------|
| Charger IRQ Control | 0X0F | Meaning | CHTERMIM | IEOCM | CHRGIM | CHTMRFIM | SOFTSTARTIM | Reserved | CHG_STAT2_ALT | CHG_STAT3_ALT |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| CHTERMIM | | | Charge terminated interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| IEOCM | | | Charge current is lower than EOC current interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHRGIM | | | Charger Re-Charge request interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHTMRFIM | | | CHTMRFI interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| SOFTSTARTIM | | | SOFTSTARTI interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHG_STAT2_ALT | | | CHG_STAT2_ALT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| CHG_STAT3_ALT | | | CHG_STAT3_ALT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
| Boost IRQ Control | 0X10 | Meaning | BSTTSDIM | BSTVMIDOVPI | BSTLOWVIM | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| BSTTSDIM | | | Boost fault. Thermal shutdown interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| BSTVMIDOVPI | | | Boost fault. VMID OVP interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| BSTLOWVIM | | | Boost fault. Battery voltage is too low interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

Register of the ADC & LDSW & DCP Control & Adapter Detection & Attach Control & Reset

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-----------|------------------|-------------|--|----------------|------|----------|----------|----------|----------|------------|
| ADC_ CTL | 0X20 | Meaning | CH_SEL | | | Reserved | Reserved | Reserved | Reserved | ADC_ START |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| CH_SEL | | | ADC channel selection. | | | | | | | |
| | | | Code | Chanel | Code | Chanel | Code | Chanel | Code | Chanel |
| | | | 000 | VBAT (default) | 010 | USBOUT | 100 | IBAT | 110 | Reserved |
| | | | 001 | VBUS | 011 | TS | 101 | IUSBOUT | 111 | Reserved |
| ADC_START | | | ADC start control 0 : ADC conversion not active (default) 1 : Start ADC conversion (auto clear when conversion done) | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|--------------|------------------|--------------------|---------------|------|------|------|------|------|------|---------------|
| ADC CODEH | 0X21 | Meaning | ADC_CODEH | | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/ Write | R | R | R | R | R | R | R | R |
| ADC_CODEH | | ADC code high byte | | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-----------|------------------|-------------------|------------|------|------|------|------|------|------|------------|
| ADC CODEL | 0X22 | Meaning | ADC_CODEL | | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R | R | R | R | R | R | R | R |
| ADC_CODEL | | ADC code low byte | | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------------|------------------|-------------|--|----------|---------------|------|------|----------|-----------------|------------|
| USBOUT Control | 0X23 | Meaning | EN_ DCP | EN_ LDSW | USBOUTLDI_LVL | | | Reserved | LDSW_ TREG[1:0] | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| EN_DCP | | | DCP controller Enable 0 : DCP controller disable (default) 1 : DCP controller enable | | | | | | | |
| EN_LDSW | | | Load Switch Enable 0 : Load switch disable (default) 1 : Load switch enable | | | | | | | |
| USBOUTLDI_LVL | | | USBOUTLDI_LVL | | | | | | | |
| | | | Code | Current | | | Code | Current | | |
| | | | 000 | Disable | | | 100 | 50mA | | |
| | | | 001 | NA | | | 101 | 100mA | | |
| | | | 010 | 10mA | | | 110 | 150mA | | |
| | | | 011 | 30mA | | | 111 | 150mA | | |
| LDSW_TREG[1:0] | | | Thermal regulation level 00 : Disable 01 : 100°C (default) 10 : 120°C 11 : 135°C | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------------|------------------|------------|---|----------------------|-------------|---------------|------|-----------------------|---------------|---------------|
| ATTACH Control | 0X24 | Meaning | EN_ADAPTERDET | EN_VBUSAT | EN_USBOUTAT | USBOUTAT_TIME | | | USBOUTAT_Mode | Reserved |
| | | Default | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| EN_ADAPTERDET | | | Adapter type detect enable 0 : Adapter detect disable 1 : Adapter detect enable (default) | | | | | | | |
| EN_VBUSAT | | | VBUS attach/detach detect enable 0 : VBUS attach/detach detect disable 1 : VBUS attach/detach detect enable (default) | | | | | | | |
| EN_USBOUTAT | | | USBOUT attach/detach detect enable 0 : USBOUT attach/detach detect disable 1 : USBOUT attach/detach detect enable (default) | | | | | | | |
| USBOUTAT_TIME | | | USBOUT attach/detach detection time. | | | | | | | |
| | | | Code | Time | | Code | | Time | | |
| | | | 000 | Detection time 150ms | | 100 | | Detection time 600ms | | |
| | | | 001 | Detection time 250ms | | 101 | | Detection time 700ms | | |
| | | | 010 | Detection time 375ms | | 110 | | Detection time 925ms | | |
| | | | 011 | Detection time 475ms | | 111 | | Detection time 1125ms | | |
| USBOUTAT_Mode | | | USBOUT attach detect mode 0 : Normal Mode 1 : Power Saving Mode, power save 50% and detection time increase 100% | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------|------------------|------------|---|-------------|------|----------|----------|----------|----------|------------|
| MISC_STA1 | 0X25 | Meaning | ADC_STA | ADAPTER_STA | | Reserved | Reserved | Reserved | Reserved | Reserved |
| | | Default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| ADC_STA | | | ADC status 0 : ADC is idle 1 : ADC conversion is on going | | | | | | | |
| ADAPTER_STA | | | VBUS adapter type 00 : SDP with D+ / D- floating 01 : SDP 10 : CDP 11 : DCP | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|---------------|------------------|------------|---|---------------|-----------|-------------|--------------|-----------|----------|------------|
| MISC_STA2 | 0X26 | Meaning | LDSWREG_STAT | USBOUTLD_STAT | VBUS_STAT | USBOUT_STAT | VDDAUVP_STAT | LDSW_STAT | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R | R | R | R | R | R | R/W | R/W |
| LDSWREG_STAT | | | Load switch warning. LDSW output current regulation loop active 0 : LDSW output current regulation loop is not active 1 : LDSW output current regulation loop is active | | | | | | | |
| USBOUTLD_STAT | | | USBOUT light load indicator 0 : USBOUT loading > USBOUTLC_LVL or disable 1 : USBOUT loading < USBOUTLC_LVL | | | | | | | |
| VBUS_STAT | | | VBUS connection status 0 : VBUS has no adapter connect (VBUS < VBUS_POR) 1 : VBUS has adapter connect (VBUS > UVLO & VBUS > ISENSEN + VSLP) | | | | | | | |
| USBOUT_STAT | | | USBOUT device connection status 0 : USBOUT has no device connect 1 : USBOUT has device connect | | | | | | | |
| VDDAUVP_STAT | | | VDDA under voltage protect, disable SWCHG, LDSW, DCP Control, Adapter Detection, ADC and TS driver when VDDAUVP is occur. 0 : VDDA UVP is not trigger 1 : VDDA UVP is trigger | | | | | | | |
| LDSW_STAT | | | Load switch status 0 : Load switch is turn off 1 : Load switch is turn on | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|---------------|------------------|------------|---|---------------|-----------|----------|---------------|------|----------|------------|
| MISC_IRQ | 0X27 | Meaning | ADC_DONEI | ADAPTER_DONEI | LDSW_SCPI | LDSWRDYI | MISC_STA2_ALT | WDTI | VMIDSCPI | VMIDUV PI |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/C | R/C | R/C | R/C | R/C | R/C | R/C | R/W |
| ADC_DONEI | | | ADC conversion done interrupt | | | | | | | |
| ADAPTER_DONEI | | | Adapter detection done interrupt | | | | | | | |
| LDSW_SCPI | | | Load switch short current protect interrupt | | | | | | | |
| LDSWRDYI | | | Load switch turn on ready | | | | | | | |
| MISC_STA2_ALT | | | The status of MISC_STA2_ALT register is change | | | | | | | |
| WDTI | | | WDT interrupt | | | | | | | |
| VMIDSCPI | | | VMID short current protect interrupt, auto set EN_LDSW to 0 | | | | | | | |
| VMIDUV PI | | | VMID under voltage protect interrupt, auto set EN_LDSW to 0 | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------------|------------------|-------------|--|-----------------|-------------|---------------|---------------|-------------|----------|------------|
| MISC_STA2 Control | 0X28 | Meaning | LDSWREG_S TATM | USBOUTLD _STATM | VBUS_ STATM | USBOUT_ STATM | VDDAUV_ STATM | LDSW_ STATM | Reserved | Reserved |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/ Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| LDSWREG_STATM | | | LDSWREG_STAT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| USBOUTLD_STATM | | | USBOUTLD_STAT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VBUS_STATM | | | VBUS_STATI interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| USBOUT_STATM | | | USBOUT_STAT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VDDAUVP_STATM | | | VDDAUVP_STAT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| LDSW_STATM | | | LDSWM_STAT interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------------|------------------|------------|--|----------------|------------|----------|---------------|----------|------------|------------|
| MISC_IRQ_CTRL | 0X29 | Meaning | ADC_DONEIM | ADAPTER_DONEIM | LDSW_SCPIM | LDSWRDYM | MISC_STA2_ALT | Reserved | VMIDSC PIM | VMIDUV PIM |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADC_DONEIM | | | ADC_DONEI interrupt mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| ADAPTER_DONEIM | | | ADAPTER_DONEI mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| LDSW_SCPIM | | | LDSW_SCPIM mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| LDSWRDYM | | | LDSWRDYM mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| MISC_STA2_ALT | | | MISC_STA2_ALT mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VMIDSC PIM | | | VMIDSC PIM mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |
| VMIDUV PIM | | | VMIDUV PIM mask 0 : Interrupt is not masked 1 : Interrupt is masked | | | | | | | |

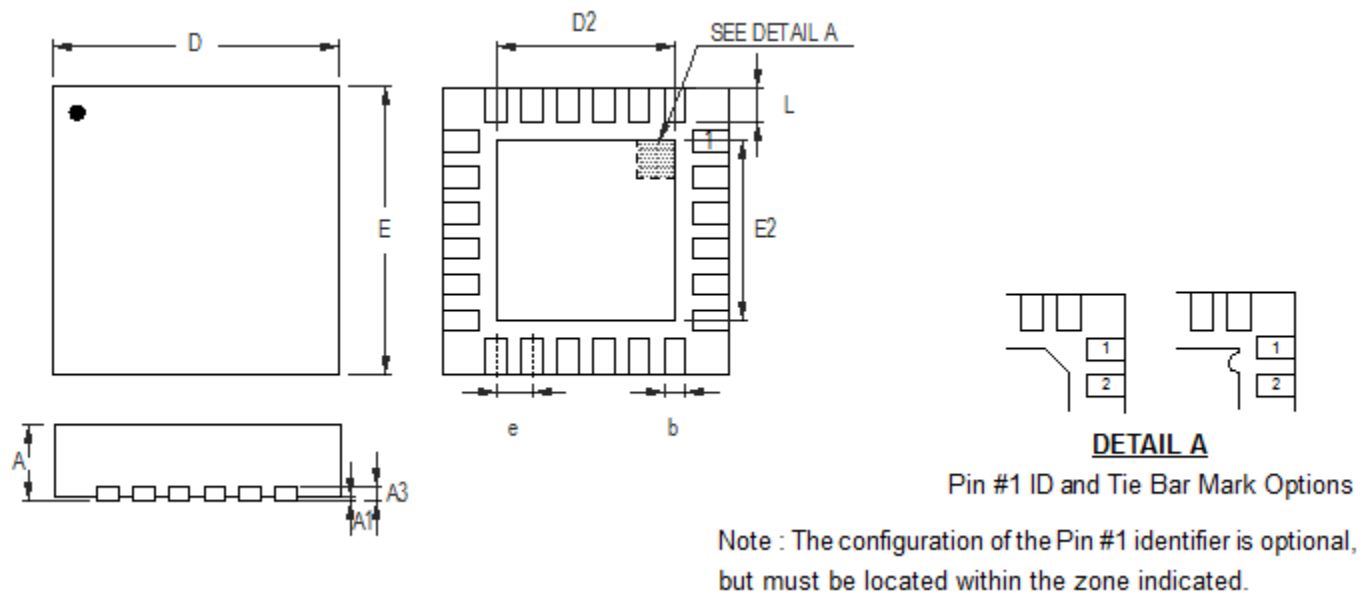
| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------|------------------|------------|---|------|------|------|------|------|------|------------|
| RESET | 0X2A | Meaning | RESET | | | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | W | W | W | W | W | W | W | W |
| RESET | | | Reset control register 0X96 : RESET, reset whole chip include register and circuit 0X3C : REG_RST, reset whole register setting to default only | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|-------------|------------------|------------|--|----------|------|------|----------|----------|----------|--------------|
| WDT_CTRL | 0X2B | Meaning | WDT_EN | Reserved | WDT | | Reserved | Reserved | Reserved | WDT_REFR ESH |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | W |
| WDT_EN | | | WDT enable control 0 : WDT disable (default) 1 : WDT enable | | | | | | | |
| WDT | | | Watch Dog Timer, it will reset whole chip when time out 00 : 8 second (default) 01 : 16 second 10 : 32 second 11 : 64 second | | | | | | | |
| WDT_REFRESH | | | Watch Dog Timer refresh 0 : No action 1 : Refresh watch dog timer | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------------|------------------|---------|--|----------|----------------|------|------|------|------|------------|
| LDSW_ILIM_FUSE | 0X2C | Meaning | Reserved | Reserved | LDSW_ILIM_FUSE | | | | | |
| | | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Read | R | R | R | R | R | R | R | R |
| LDSW_ILIM_FUSE | | | Report the fuse setting of LDSW current regulation | | | | | | | |

| Function | Register Address | | b[7] (MSB) | b[6] | b[5] | b[4] | b[3] | b[2] | b[1] | b[0] (LSB) |
|----------------|------------------|------------|--|------|----------------|------|------|------|------|------------|
| LDSW_ILIM_CTRL | 0X2D | Meaning | LDSW_ILIM_LVL | | LDSW_ILIM_CTRL | | | | | |
| | | Default | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| LDSW_ILIM_LVL | | | LDSW current regulation 00 : Min = 1.0A, TYP = 2.0A, MAX = 3.0A 01 : Min = 1.5A, TYP = 2.5A, MAX = 3.5A 10 : Min = 2.0A, TYP = 3.0A, MAX = 4.0A | | | | | | | |
| LDSW_ILIM_CTRL | | | LDSW_ILIM_CTRL = LDSW_ILIM_FUSE-[2500-TARGET+(LDSW_ILIM_LVL-1)x567]/35 Target = the target USBOUT current regulation setting, the unit is mA. | | | | | | | |

Outline Dimension



| Symbol | | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|----------|---------------------------|-------|----------------------|-------|
| | | Min | Max | Min | Max |
| A | | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | | 0.175 | 0.250 | 0.007 | 0.010 |
| b | | 0.180 | 0.300 | 0.007 | 0.012 |
| D | | 3.950 | 4.050 | 0.156 | 0.159 |
| D2 | Option 1 | 2.400 | 2.500 | 0.094 | 0.098 |
| | Option 2 | 2.650 | 2.750 | 0.104 | 0.108 |
| E | | 3.950 | 4.050 | 0.156 | 0.159 |
| E2 | Option 1 | 2.400 | 2.500 | 0.094 | 0.098 |
| | Option 2 | 2.650 | 2.750 | 0.104 | 0.108 |
| e | | 0.500 | | 0.020 | |
| L | | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 24L QFN 4x4 Package

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