RICHTEK®

# RT7084C2M

# Three-Phase PMSM/BLDC Motor Controller with Pre-Driver

## 1 General Description

The RT7084C2M is an application-specific IC designed for PMSM/BLDC motor applications. This two-in-one ASIC integrates several functional circuits, including a 3-phase motor controller, a 3-phase gate driver, three bootstrap diodes, a 5V LDO, and a buck converter.

The RT7084C2M embeds the ARM 32-bit Cortex-M0 core with peripheral circuits to perform sensorless Field Oriented Control (FOC). In addition, this ASIC provides several system-level peripheral functions, including filters at the ADC input, a communication interface, a thermal sensor, short circuit protection (SCP) and locked-rotor protection, to reduce component count, PCB size and system cost.

Moreover, the RT7084C2M drives external N-Channel MOSFETs in a three half-bridge configuration with built-in bootstrap circuitry.

The RT7084C2M is available in a VQFN-32L 4x4 package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

## 2 Ordering Information

RT7084C2M□-□

- Packing
  A: Standard
- Package Type(1)
  N: VQFN-32L 4x4 (V-Type)

**Note 1**.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

## 3 Marking Information


JY=: Product Code
YMDAN: Date Code

## 4 Features

- **Integrate 3-Phase PMSM/BLDC Controller, Gate Driver, Bootstrap Diodes, 5V LDO, and Buck Converter**
- **Input Voltage Range: 16V to 80V**
- **Sensorless, Sine-Wave Field Oriented Control (FOC)**
- **Integrate Filters at ADC Input**
- **Protections: SCP, UVLO, Locked-Rotor, and Thermal Detection**
- **PMSM/BLDC Motor Controller**
  - **ARM 32-bit Cortex-M0 CPU, Frequency up to 60MHz**
  - **Memories Size: 16kB MTP, Internal ROM with Embedded Motor Control Library and 4kB SRAM**
  - **Power Management: Deep Sleep**
  - **Communication Interface: $I^2C$ and UART**
  - **Configurable ADC Gain: x1, x4, and x8**
  - **5-Channel 12-Bit ADC**
    - **AD0 to AD3 for Differential Mode Current Sense**
    - **AD6 to AD8 for System Application**
  - **1-Channel Voltage Type 8-bit DAC**
- **Gate Driver**
  - **Floating Channel Designed for Bootstrap Operation**
  - **Sourcing/Sinking Current: 100mA/200mA**
  - **Built-In UVLO Functions for All Channels**
  - **Matched Propagation Delays for All Channels**
- **VQFN-32L 4x4 Package**

## 5 Applications

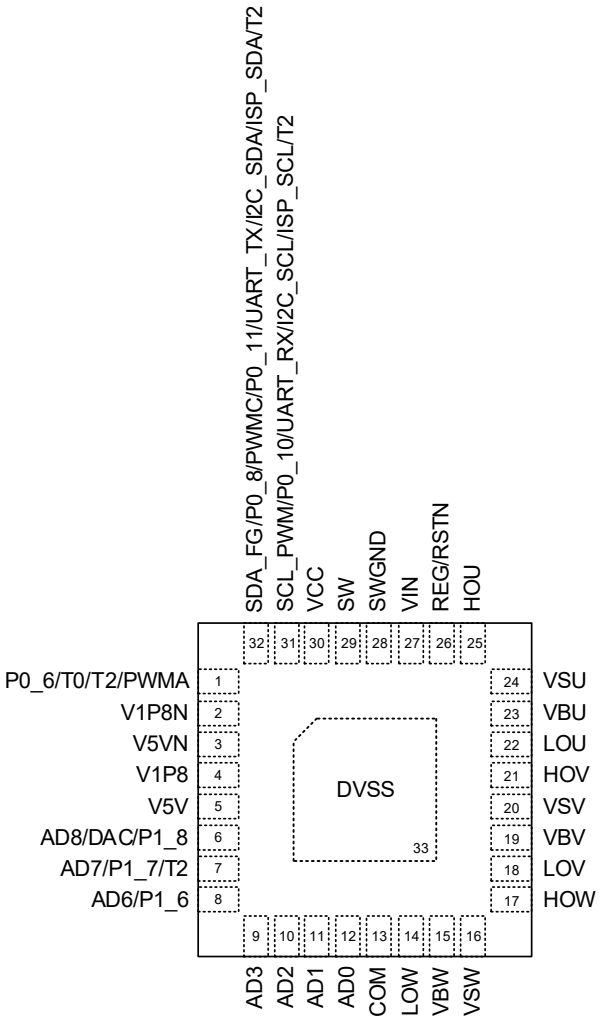
- Server Fans
- Telecom Fans
- Liquid Pumps

# Table of Contents


**1 General Description ..... 1**
**2 Ordering Information ..... 1**
**3 Marking Information ..... 1**
**4 Features ..... 1**
**5 Applications ..... 1**
**6 Pin Configuration ..... 3**
**7 Functional Pin Description ..... 3**
7.1 IO Type Definition ..... 5
**8 Functional Block Diagram ..... 6**
**9 Absolute Maximum Ratings ..... 7**
**10 Recommended Operating Conditions ..... 7**
**11 Electrical Characteristics ..... 8**
**12 Typical Application Circuit ..... 12**
12.1 Typical Application Circuit 1 ($V_M$ > 60V) ..... 12
12.2 Typical Application Circuit 2 ($V_M$ < 60V) ..... 13
**13 Typical Operating Characteristics ..... 14**
**14 Application Information ..... 16**
14.1 Negative Voltage of $V_{phase}$ ..... 16
14.2 Buck Converter ..... 17
14.3 Regulator with Voltage Clamp Zener ..... 17
14.4 Thermal Considerations ..... 18
**15 Outline Dimension ..... 20**
**16 Footprint Information ..... 21**
**17 Packing Information ..... 22**
17.1 Tape and Reel Data ..... 22
17.2 Tape and Reel Packing ..... 23
17.3 Packing Material Anti-ESD Property ..... 24
**18 Datasheet Revision History ..... 25**

# 6 Pin Configuration

(TOP VIEW)




VQFN-32L 4x4

# 7 Functional Pin Description

| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 1 | P0_6 | DI/DO | Pin 6 of GPIO port 0. |
| | T0 | DI | T0 external enable or external clock input pin. |
| | T2 | DI | T2 external enable or external clock input pin. |
| | PWMA | DO | Programmable PWMA output pin. |
| 2 | V1P8N | GND | Digital ground. |
| 3 | V5VN | GND | Analog ground. |
| 4 | V1P8 | P | 1.8V power pin. |
| 5 | V5V | P | 5V power pin. |

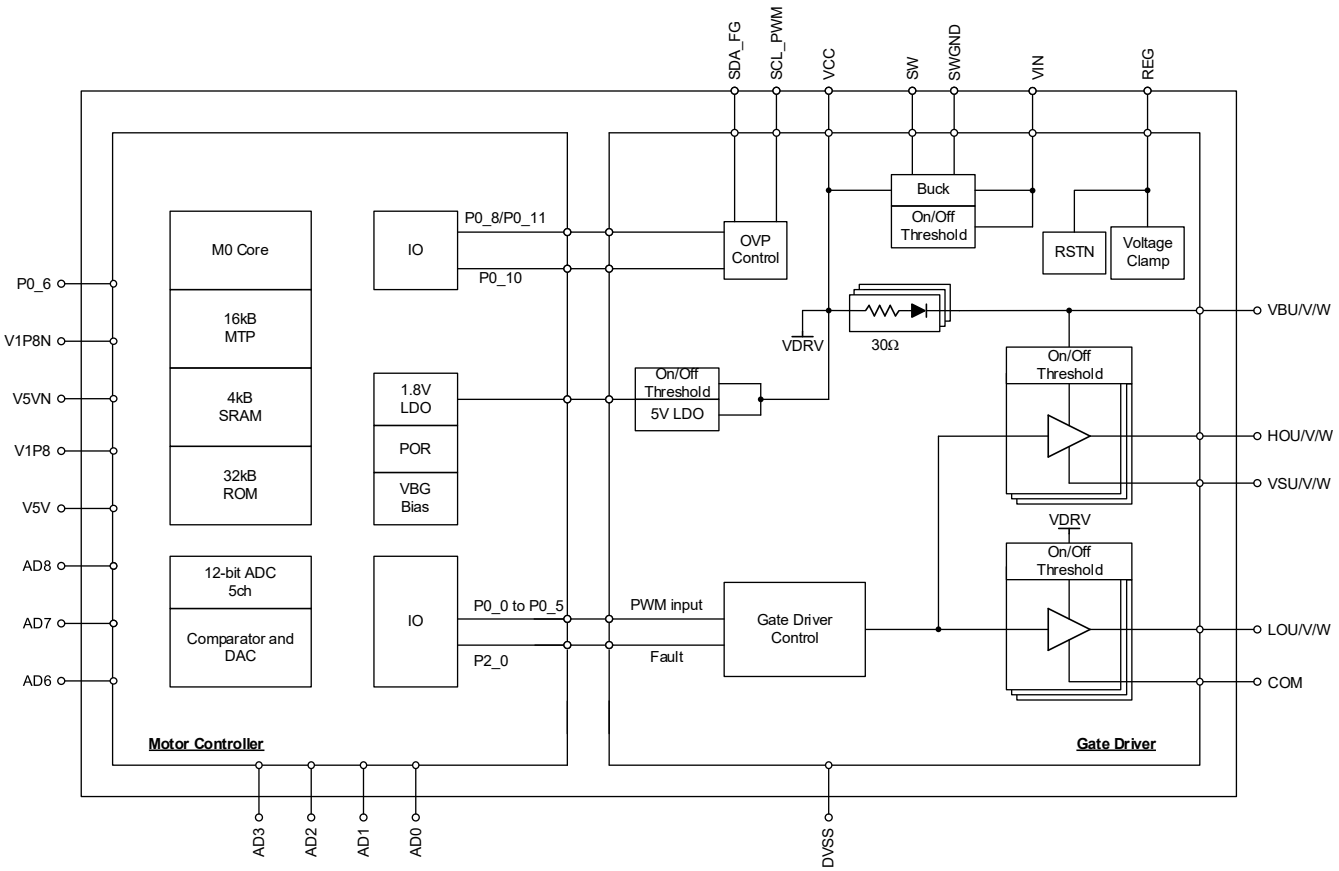
| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 6 | AD8 | AI | ADC channel 8 input pin. |
| | DAC | AO | Voltage type DAC output pin. |
| | P1_8 | DI/DO | Pin 8 of GPIO port 1. |
| 7 | AD7 | AI | ADC channel 7 input pin. |
| | P1_7 | DI/DO | Pin 7 of GPIO port 1. |
| | T2 | DI | T2 external enable or external clock input pin. |
| 8 | AD6 | AI | ADC channel 6 input pin. |
| | P1_6 | DI/DO | Pin 6 of GPIO port 1. |
| 9 | AD3 | AI | ADC channel 3 for differential negative input pin only. |
| 10 | AD2 | AI | ADC channel 2 for differential positive input pin only. |
| 11 | AD1 | AI | ADC channel 1 for differential negative input pin only. |
| 12 | AD0 | AI | ADC channel 0 for differential positive input pin only. |
| 13 | COM | GND | Gate driver ground. |
| 14 | LOW | VO | Low-side gate output of Phase W. |
| 15 | VBW | VI | High-side floating supply voltage of Phase W. |
| 16 | VSW | VI | High-side floating supply offset voltage of Phase W. |
| 17 | HOW | VO | High-side gate output of Phase W. |
| 18 | LOV | VO | Low-side gate output of Phase V. |
| 19 | VBV | VI | High-side floating supply voltage of Phase V. |
| 20 | VSV | VI | High-side floating supply offset voltage of Phase V. |
| 21 | HOV | VO | High-side gate output of Phase V. |
| 22 | LOU | VO | Low-side gate output of Phase U. |
| 23 | VBU | VI | High-side floating supply voltage of Phase U. |
| 24 | VSU | VI | High-side floating supply offset voltage of Phase U. |
| 25 | HOU | VO | High-side gate output of Phase U. |
| 26 | REG | VO | Voltage clamper for regulator with NMOS. |
| | RSTN | DI | Low active reset pin. |
| 27 | VIN | VI | Buck input voltage. |
| 28 | SWGND | GND | Buck ground. |
| 29 | SW | VO | Switch node of buck converter. |
| 30 | VCC | VI | Controller and gate driver supply voltage. |
| 31 | SCL_PWM | DI/DO | Clock pin with overvoltage protection. |
| | P0_10 | DI/DO | Pin 10 of GPIO port 0. |
| | UART_RX | DI | UART receiving pin. |
| | I2C_SCL | DI/DO | $I^2C$ clock pin. |
| | ISP_SCL | DI | In system programming clock pin. |
| | T2 | DI | T2 external enable or external clock input pin. |

| Pin No. | Pin Name | Type | Pin Function |
|---|---|---|---|
| 32 | SDA_FG | DI/DO | Data pin with overvoltage protection. |
| | P0_8 | DI/DO | Pin 8 of GPIO port 0. |
| | PWMC | DO | Programmable PWMC output pin. |
| | P0_11 | DI/DO | Pin 11 of GPIO port 0. |
| | UART_TX | DO | UART transmitting pin. |
| | I2C_SDA | DI/DO | $I^2C$ data pin. |
| | ISP_SDA | DI/DO | In system programming data pin. |
| | T2 | DI | T2 external enable or external clock input pin. |
| 33 (Exposed Pad) | DVSS | GND | Digital ground. |

### 7.1 IO Type Definition

- DI: Digital Input Pin
- DO: Digital Output Pin
- AI: Analog Input Pin
- AO: Analog Output Pin
- P: Power Pin
- VI: Voltage Input Pin
- VO: Voltage Output Pin

# 8 Functional Block Diagram



## 9 Absolute Maximum Ratings

(Note 2)

- Controller and Driver Supply Voltage, VCC ---------- –0.3V to 15V
- Controller Supply Voltage, V5V ---------- –0.3V to 6.5V
- Controller Supply Voltage, V1P8 ---------- –0.3V to 2.5V
- Buck Supply Voltage, VIN ---------- –0.3V to 66V
- Buck Switch Voltage, SW ---------- –0.3V to 66V
- Clamping Voltage, REG ---------- –0.3V to 50V
- VSU, VSV, VSW to COM ---------- –2V to 100V
- VSU, VSV, VSW to COM (Transient, 2μs) ---------- –5V to 100V
- VBU, VBV, VBW to COM ---------- –0.3V to 100V
- HOU, HOV, HOW to COM ---------- –0.3V to 100V
- LOU, LOV, LOW to COM ---------- –0.3V to 15V
- VSU, VSV, VSW dv/dt ---------- ±5V/ns
- SDA_FG, SCL_PWM to DVSS ---------- –0.3V to 90V
- Voltage of I/O Pin, P0_6 ---------- –0.3V to 6.5V
- Analog Input Voltage (AD0 to AD3) ---------- –5V to 11V
- Analog Input Voltage (AD6 to AD8) ---------- –0.3V to 6.5V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  VQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 3)
  VQFN-32L 4x4, $\theta_{JA}$ ---------- 27.8°C/W
  VQFN-32L 4x4, $\theta_{JC}$ ---------- 4.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

**Note 2**. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 3**. $\theta_{JA}$ is simulated under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is simulated at the bottom of the package.

**Note 4**. Devices are ESD sensitive. Handling precautions are recommended.

## 10 Recommended Operating Conditions

(Note 5)

- Controller and Driver Supply Voltage, VCC ---------- 9.5V to 10.5V
- Controller Supply Voltage, V5V ---------- 4.5V to 5.5V
- Buck Supply Voltage, VIN ---------- 16V to 60V
- Buck Switch Voltage, SW ---------- –0.3V to 60V
- Clamping Voltage, REG ---------- 0V to 45V

- VSU, VSV, VSW to COM ---------- –2V to 80V
- VSU, VSV, VSW to COM (Transient, 2μs) ---------- –5V to 80V
- VBU, VBV, VBW to COM ---------- 0V to 90V
- SDA_FG, SCL_PWM to DVSS ---------- 0V to 20V
- Voltage of I/O Pin, P0_6 ---------- 0V to 5V
- Analog Input Voltage (AD0 to AD3 and AD6 to AD8) ---------- 0V to 5V
- Buck Input Capacitor on VIN ---------- 0.1μF
- Controller and Driver Supply Voltage Capacitor on VCC ---------- 4.7μF
- LDO Capacitor on V5V ---------- 1μF
- LDO Capacitor on V1P8 ---------- 1μF
- Minimum Time Period of RSTN, $t_{RSTN}$ ---------- 100μs
- Ambient Temperature Range ---------- –40°C to 105°C
- Junction Temperature Range ---------- –40°C to 125°C

**Note 5**. The device is not guaranteed to function outside its operating conditions.

## 11 Electrical Characteristics

($V_{V5V}$ = 5V, $V_{VIN}$ = 48V, $V_{VCC}$ = 10V, $T_A$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Clock Section** | | | | | | |
| System Frequency | $f_{SCLK}$ | | 58.8 | 60 | 61.2 | MHz |
| Slow Clock for Sleep Mode | $f_{LCLK}$ | | 77.6 | 80 | 82.4 | kHz |
| **LDO Section** | | | | | | |
| V5V LDO Turn-On Threshold | $V_{V5V\_LDO\_THON}$ | | 6.9 | 7.5 | 8.1 | V |
| V5V LDO Turn-Off Threshold | $V_{V5V\_LDO\_THOFF}$ | | 5.9 | 6.5 | 7.1 | V |
| V5V LDO Threshold Hysteresis | $V_{V5V\_HYS}$ | | -- | 1 | -- | V |
| V5V LDO Output Voltage | $V_{V5V}$ | | 4.85 | 5 | 5.15 | V |
| V5V Current at Operation Mode | $I_{V5V\_OPER}$ | | -- | 20 | -- | mA |
| V5V Current at Deep Sleep Mode | $I_{V5V\_DSLP}$ | | -- | 1.3 | -- | mA |
| V5V LDO Current Limit | $I_{V5V\_OC}$ | $V_{V5V}$ < 3.3V | -- | 15 | -- | mA |
| | | $V_{V5V}$ > 3.3V | 70 | -- | 130 | |
| V1P8 LDO Turn-On Threshold | $V_{V1P8\_LDO\_THON}$ | | 3.9 | 4.1 | 4.3 | V |
| V1P8 LDO Turn-Off Threshold | $V_{V1P8\_LDO\_THOFF}$ | | 3.4 | 3.6 | 3.8 | V |
| V1P8 LDO Threshold Hysteresis | $V_{V1P8\_HYS}$ | | -- | 0.5 | -- | V |
| V1P8 LDO Output Voltage | $V_{V1P8}$ | $C_{V1P8}$ = 1μF, $I_{LOAD}$ = 40mA | 1.62 | 1.8 | 1.98 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| V5V Undervoltage for Interrupt Flag | $V_{V5V\_UV}$ | | 4.1 | 4.3 | 4.5 | V |
| V1P8 Undervoltage for Interrupt Flag | $V_{V1P8\_UV}$ | | -- | 1.5 | -- | V |
| **ADC Section (0V to 3V, 12-bit, Single End Mode, Gain = 1)** (Note 6) | | | | | | |
| Minimum Conversion Voltage | $V_{I\_MIN}$ | Code 000h | -- | 0 | -- | V |
| Maximum Conversion Voltage | $V_{I\_MAX}$ | Code FFFh | -- | 3 | -- | V |
| ADC Offset | $V_{OFFSET}$ | | –20 | -- | 20 | LSB |
| **SCDAC Section (0V to 1.2V, 8-bit for Short Current)** (Note 6) | | | | | | |
| Minimum Conversion Voltage | $V_{O\_MIN}$ | Code 00h | -- | 0 | -- | V |
| Maximum Conversion Voltage | $V_{O\_MIN}$ | Code FFh | -- | 1.2 | -- | V |
| DAC Offset | $V_{OFFSET}$ | | –4 | -- | 4 | LSB |
| **VDAC Section (0V to 3V, 8-bit for General Purposed Comparator)** (Note 6) | | | | | | |
| Minimum Conversion Voltage | $V_{O\_MIN}$ | Code 00h | -- | 0 | -- | V |
| Maximum Conversion Voltage | $V_{O\_MIN}$ | Code FFh | -- | 3 | -- | V |
| DAC Offset | $V_{OFFSET}$ | | –4 | -- | 4 | LSB |
| Output Resistance of DAC | $R_O$ | | -- | 5 | -- | kΩ |
| **Current Limit Comparator (Short Circuit)** | | | | | | |
| Input Voltage Range of Comparator | $V_{I\_COMP}$ | | 0 | -- | 1.2 | V |
| Comparator Offset | $V_{OFFSET}$ | | –15 | -- | 15 | mV |
| **General Purposed Comparator (Level Comparator)** | | | | | | |
| Input Voltage Range of Comparator | $V_{I\_COMP}$ | | 0.5 | -- | 3 | V |
| Comparator Offset | $V_{OFFSET}$ | | –20 | -- | 20 | mV |
| **IO of P0_6 Section** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.2 | 2.6 | 3 | V |
| Input Low Voltage | $V_{IL}$ | | 1.1 | 1.6 | 2 | V |
| Hysteresis | $V_H$ | | -- | 1 | -- | V |
| Pull-Up Resistor | $R_{UP}$ | | -- | 80 | -- | kΩ |
| Pull-Down Resistor | $R_{DOWN}$ | | -- | 40 | -- | kΩ |
| High Level Output Current | $I_{OH}$ | @ 0.8 x V5V | -- | 5 | -- | mA |
| Low Level Output Current | $I_{OL}$ | @ 0.2 x V5V | -- | 10 | -- | mA |

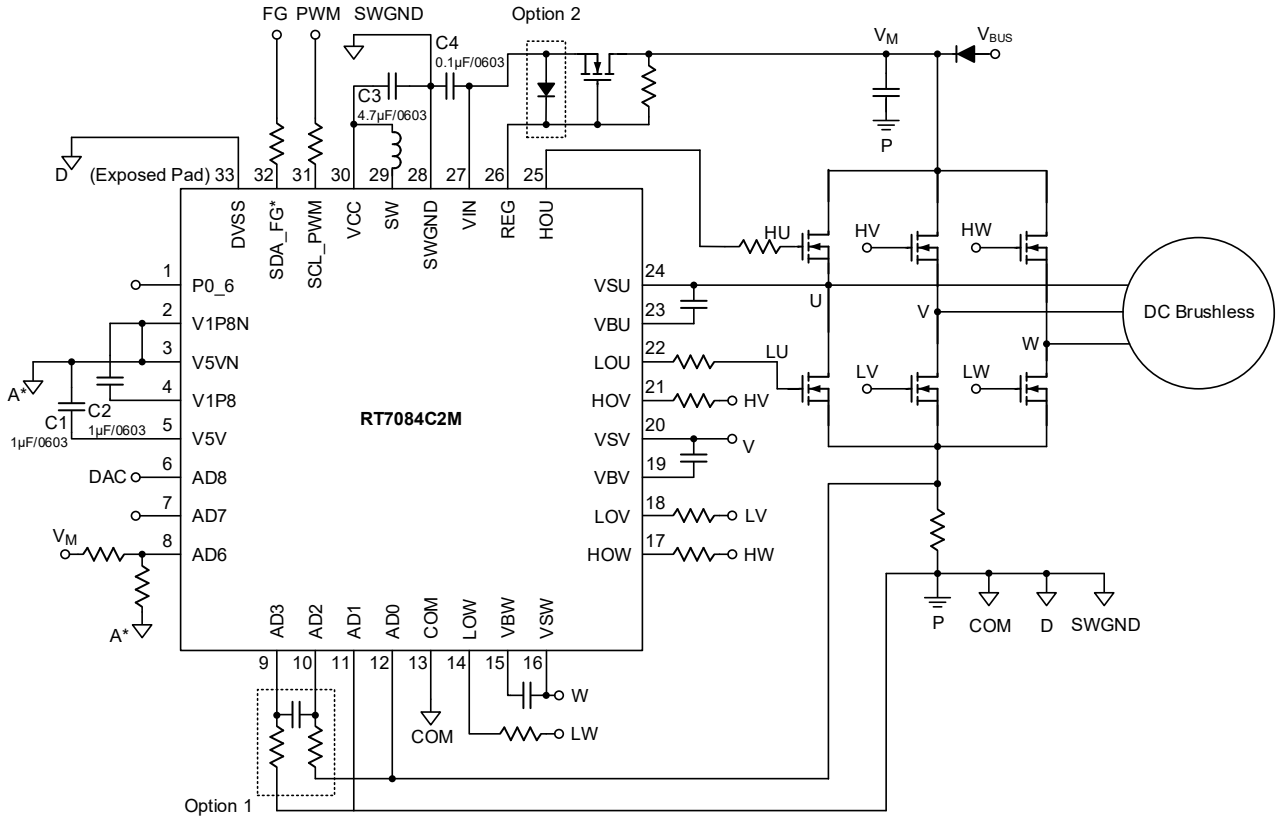
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **IO of P1_6 to P1_8 Section** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.2 | 2.6 | 3 | V |
| Input Low Voltage | $V_{IL}$ | | 1.1 | 1.6 | 2 | V |
| Hysteresis | $V_H$ | | -- | 1 | -- | V |
| Pull-Up Resistor | $R_{UP}$ | Only P1_6/P1_7 | -- | 80 | -- | kΩ |
| High Level Output Current | $I_{OH}$ | @ 0.8 x V5V | -- | 5 | -- | mA |
| Low Level Output Current | $I_{OL}$ | @ 0.2 x V5V | -- | 10 | -- | mA |
| **IO of AD6 to AD8** | | | | | | |
| Time Constant of Input RC Filter at AD_FLT = 1 | $t_{AD6-8FLT=1}$ | Set register AD_FLT = 1, AD_FLT_ORD = 0 | -- | 6 | -- | μs |
| Time Constant of Input RC Filter at AD_FLT = 0 | $t_{AD6-8FLT=0}$ | Set register AD_FLT = 0, AD_FLT_ORD = 0 | -- | 1 | -- | μs |
| Bias Current at AD8 | $I_{AD8\_BIAS}$ | | 95 | 100 | 105 | μA |
| **$I^2C$ Interface ($t_{SYS}$ = 1/ $f_{SCLK}$)** | | | | | | |
| $I^2C$ Clock Cycle Time | $t_{SCL}$ | | $t_{SYS}$ x 80 | -- | -- | ns |
| $I^2C$ Start Bit Setup Time | $t_{START}$ | | -- | $t_{SCL}$ / 2 | -- | ns |
| $I^2C$ Stop Bit Setup Time | $t_{STOP}$ | | -- | $t_{SCL}$ / 2 | -- | ns |
| $I^2C$ Data Setup Time | $t_{SETUP}$ | | -- | $t_{SYS}$ | -- | ns |
| $I^2C$ Data Hold Time | $t_{HOLD}$ | | -- | $t_{SYS}$ | -- | ns |
| **SDA/FG and SCL/PWM Section** | | | | | | |
| OVP Level | $V_{OVP}$ | | 24 | -- | 34 | V |
| Input High Voltage | $V_{IH}$ | | 2.2 | 2.6 | 3 | V |
| Input Low Voltage | $V_{IL}$ | | 1.1 | 1.45 | 2 | V |
| Hysteresis | $V_H$ | | -- | 1.15 | -- | V |
| **REG Section** | | | | | | |
| Zener Clamp Voltage | $V_{CLAMP}$ | $I_{CLAMP}$ = 100μA | 33.4 | 39.2 | 45 | V |
| Operation Current | $I_Z$ | | -- | -- | 180 | μA |
| **Buck Converter Section** | | | | | | |
| VIN Turn-On Threshold | $V_{VIN\_THON}$ | | 13 | 14 | 15 | V |
| VIN Turn-Off Threshold | $V_{VIN\_THOFF}$ | | 12 | 13 | 14 | V |
| VIN Threshold Hysteresis | $V_{VIN\_HYS}$ | | -- | 1 | -- | V |
| VIN Operation Current | $I_{VIN\_OPER}$ | | -- | 1.2 | -- | mA |
| Buck High-Side $R_{DS(ON)}$ | $R_{DS(ON)\_H}$ | | -- | 4.35 | -- | Ω |
| Buck Low-Side $R_{DS(ON)}$ | $R_{DS(ON)\_L}$ | | -- | 4.6 | -- | Ω |
| Buck Minimum On-Time | $t_{ON\_MIN}$ | VIN - VCC = 45V | 62.3 | 65.2 | 68.1 | ns |
| Buck High-Side Turn-On Threshold | $V_{ZCD}$ | | -- | −20 | -- | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blanking Time for VZCD | tZCD | | -- | 130 | -- | ns |
| Buck Output Voltage | VVCC | | 9.45 | -- | 10.53 | V |
| **High-Side and Low-Side Driver Section** | | | | | | |
| High-Side Driver Turn-On Threshold | VHS_THON | | 4.5 | 5 | 5.5 | V |
| High-Side Driver Turn-Off Threshold | VHS_THOFF | | 4 | 4.5 | 5 | V |
| High-Side Threshold Hysteresis | VHS_HYS | | -- | 0.5 | -- | V |
| Low-Side Driver Turn-On Threshold | VLS_THON | | 6.9 | 7.5 | 8.1 | V |
| Low-Side Driver Turn-Off Threshold | VLS_THOFF | | 6.4 | 7 | 7.6 | V |
| Low-Side Threshold Hysteresis | VLS_HYS | | -- | 0.5 | -- | V |
| Driver Operating Current | IVCC_OP | PWM = 20kHz (COUT = 1nF), VV5V = 5.5V | -- | -- | 1.7 | mA |
| Driver Quiescent Current | IVCC_Q | LOU/V/W and HOU/V/W output low, VV5V = 5.5V | -- | -- | 1500 | μA |
| VBS Quiescent Current for One Channel | IBSX_Q | HOU/V/W output low | -- | -- | 450 | μA |
| Bootstrap Diode Forward Voltage | VD_BOOT | Id = 5mA | -- | 0.8 | -- | V |
| | | Id = 0.1A | -- | 3.3 | -- | |
| Bootstrap Diode Resistance for Current Limitation | RLMT | (Note 6) | -- | 30 | -- | Ω |
| The Difference between Input Voltage and Output Voltage | VOH | IO = 5mA, VVBU/V/W - VHOU/V/W, VVCC - VLOU/V/W | -- | 100 | -- | mV |
| | VOL | IO = –5mA, VHOU/V/W - VVSU/V/W, VLOU/V/W - VCOM | -- | 40 | -- | |
| HOU/V/W and LOU/V/W Sourcing Current | IO+ | PWM input is high, VVBSU/V/W = VVCC = 10V, VHOU/V/W = VLOU/V/W = 7V (Note 6) | -- | 100 | -- | mA |
| HOU/V/W and LOU/V/W Sinking Current | IO- | PWM input is low, VHOU/V/W = VLOU/V/W = 3V (Note 6) | -- | 200 | -- | mA |
| Turn-On Rise Time | tR | VVCC = 10V, CLOAD = 1nF (Note 6) | -- | 100 | -- | ns |
| Turn-Off Fall Time | tF | VVCC = 10V, CLOAD = 1nF (Note 6) | -- | 50 | -- | ns |
| Turn-On Propagation Delay | tON | VVCC = 10V | 30 | -- | 110 | ns |
| Turn-Off Propagation Delay | tOFF | VVCC = 10V | 30 | -- | 110 | ns |
| Delay Matching | MT | VVCC = 10V, VVSU/V/W = 16V | -- | -- | 60 | ns |
| | | VVCC = 10V, VVSU/V/W = 80V | -- | -- | 60 | |

**Note 6**. This parameter is guaranteed by design.

# 12 Typical Application Circuit

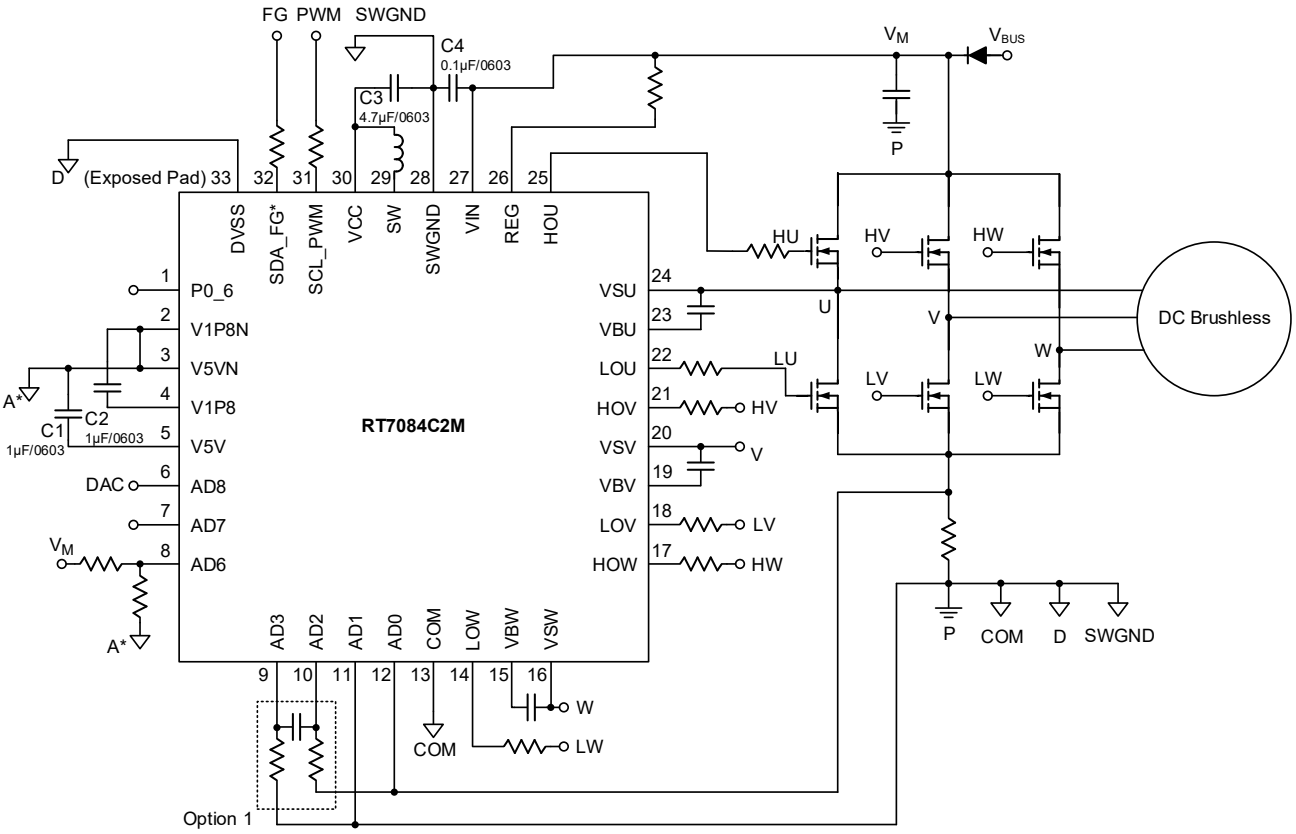
## 12.1 Typical Application Circuit 1 ($V_M$ > 60V)




**Note 7.**

1. If C1 and C2 cannot be placed close to the IC, an additional 0.1µF capacitor should be placed close to the IC.
2. C3 and C4 should be placed as close as possible to the IC and SWGND.
3. A* is a separate loop, do not connect it to DVSS (D) and PGND (P).
4. SDA_FG* is a multi-function pin including P0_8 and P0_10.
5. Option 1 is for power control demand.
6. Option 2 is used to avoid damaging the MOSFET of voltage clamp during programming period.

## 12.2 Typical Application Circuit 2 ($V_M$ < 60V)

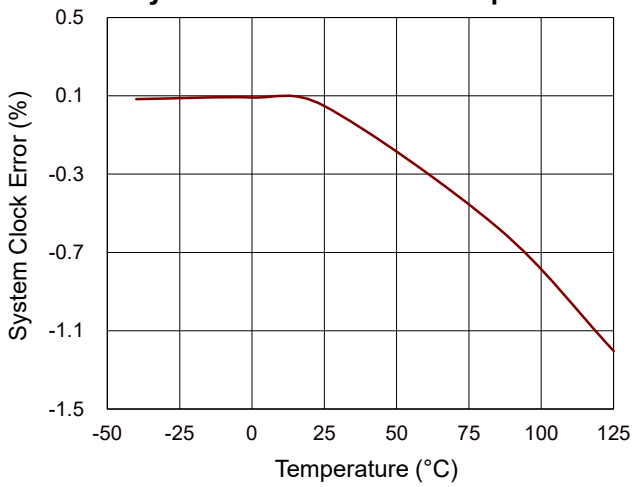



**Note 8.**

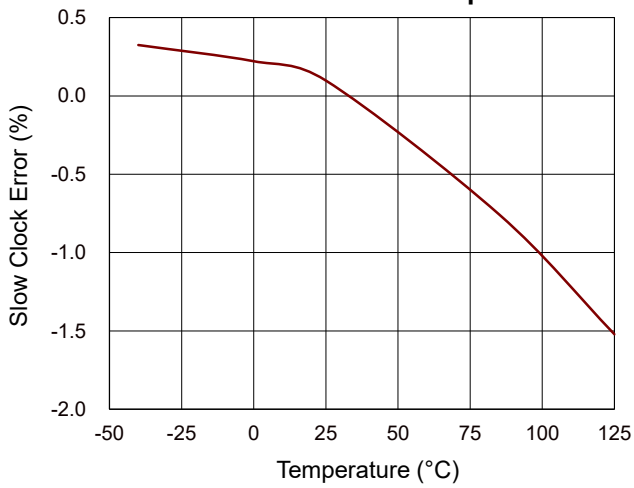
1. If C1 and C2 cannot be placed close to the IC, an additional 0.1µF capacitor should be placed close to the IC.
2. C3 and C4 should be placed as close as possible to the IC and SWGND.
3. A* is a separate loop, do not connect it to DVSS (D) and PGND (P).
4. SDA_FG* is a multi-function pin including P0_8 and P0_10.
5. Option 1 is for power control demand.

## 13 Typical Operating Characteristics

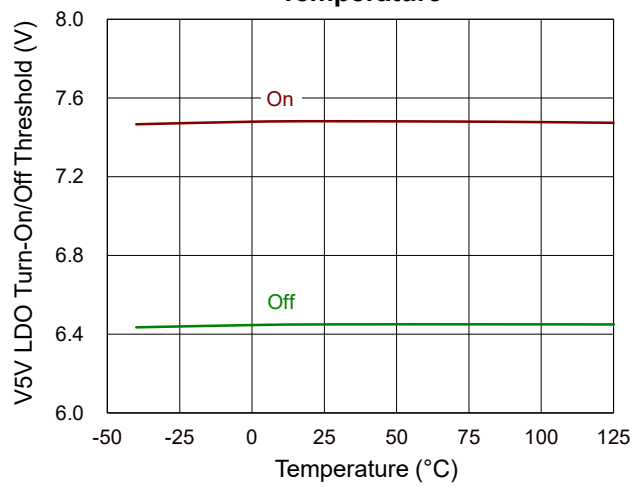
System Clock Error vs. Temperature



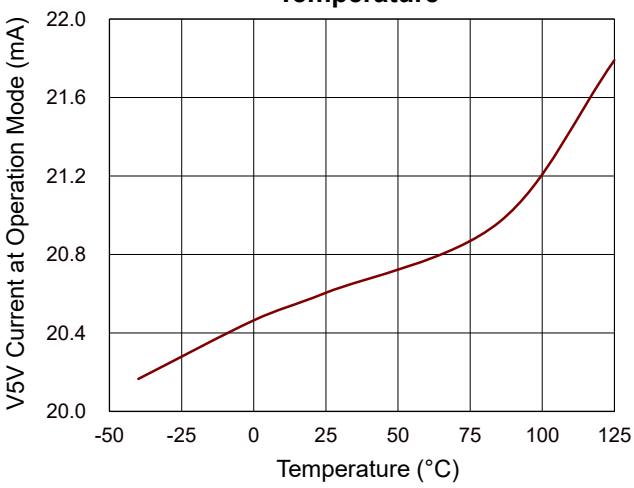

Slow Clock Error vs. Temperature



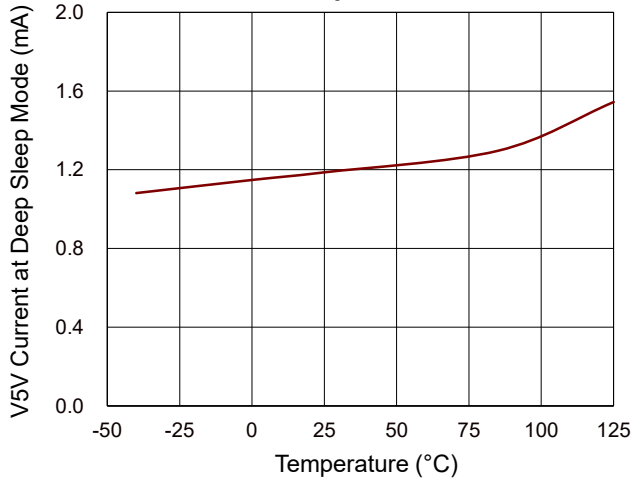

V5V LDO Turn-On/Off Threshold vs. Temperature



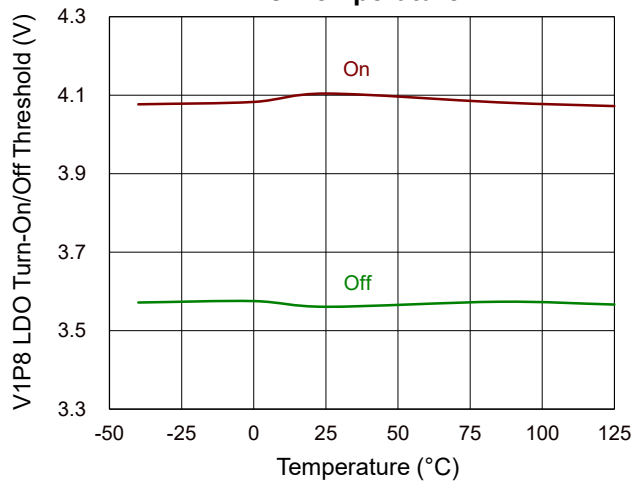

V5V Current at Operation Mode vs. Temperature

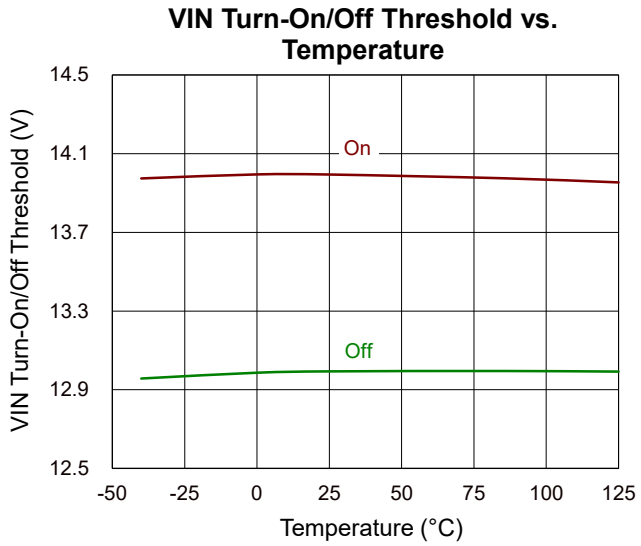


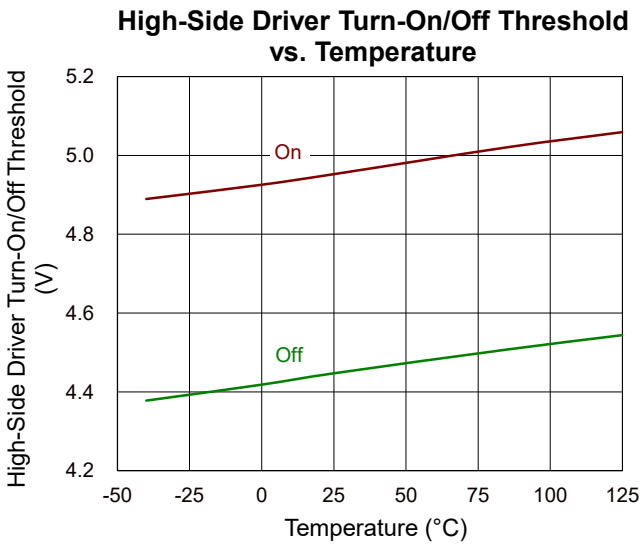

V5V Current at Deep Sleep Mode vs. Temperature

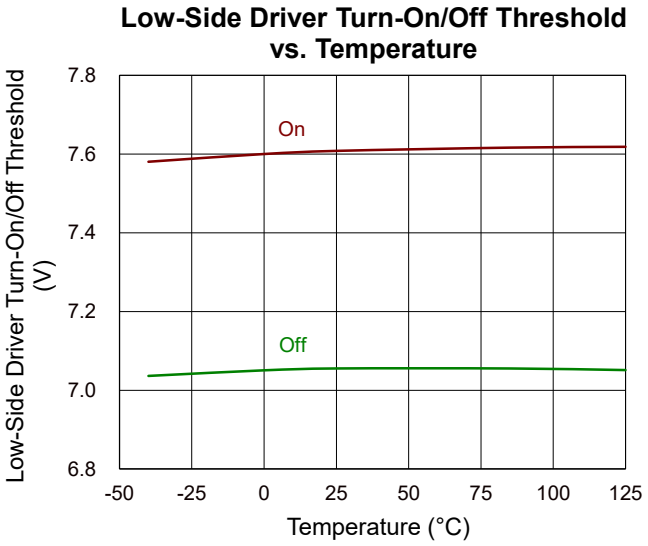


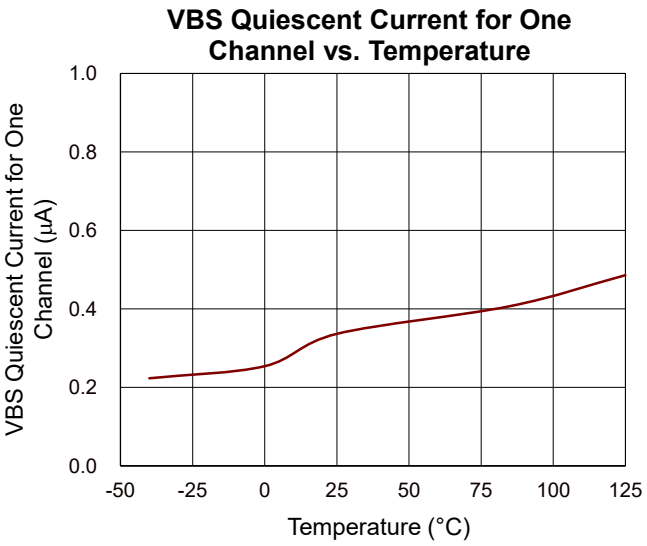

V1P8 LDO Turn-On/Off Threshold vs. Temperature





# 14 Application Information

(Note 9)

## 14.1 Negative Voltage of $V_{phase}$

When the high-side MOSFET turns off, a high di/dt current commutation is generated from the low-side MOSFET to the load during the switching transient. The fast transition slew rate with parasitic inductance induces a negative voltage spike that can be estimated with the equation $V_L$ = L x di/dt. The inductance L = L1 + L2 represents the parasitic inductance of the PCB trace and the wire bonding of the MOSFET.

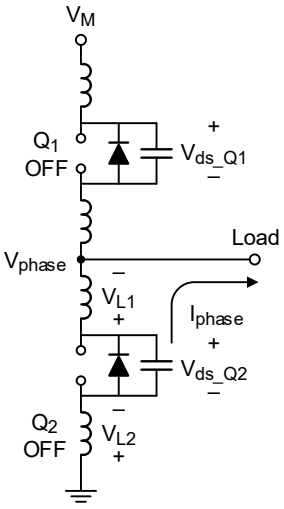



Figure 1. Negative $V_{phase}$ Voltage Spike during Low-Side MOSFET Conducts Transition

According to the equation, higher parasitic inductance can contribute to a larger negative voltage at the $V_{phase}$ point. To reduce the negative $V_{phase}$ voltage, it is recommended to minimize the trace of the power loop and the distance between components. However, if the negative $V_{phase}$ spike remains excessive, a further step can be taken as shown in Figure 2. A resistance between 3.3Ω and 10Ω is recommended for $R_{ext}$ which is placed between the VS pin and the switching node $V_{phase}$.

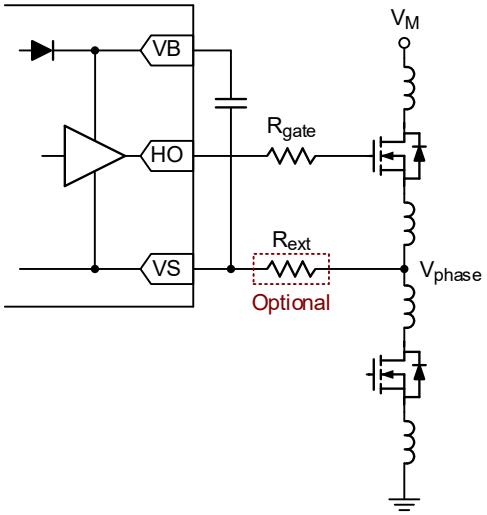



Figure 2. External Resistor between VS and $V_{phase}$

### 14.2 Buck Converter

The RT7084C2M contains a high-efficiency synchronous step-down (Buck) DC-DC converter with an input range from 16V to 60V. This Buck converter implements Constant On-Time (COT) control, adopting Boundary Conduction Mode (BCM). The values of peripheral circuit components L1, $C_{IN}$, and $C_{OUT}$ are listed in Table 1 and Table 2.

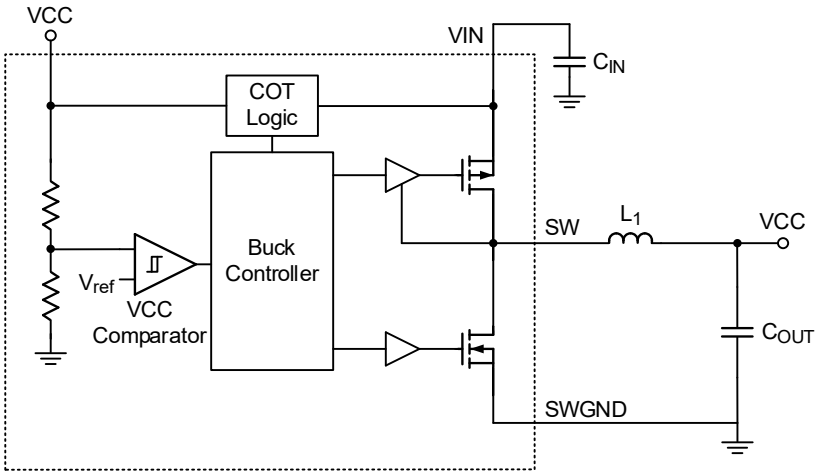



Figure 3. Buck Converter

**Table 1. Recommended Value for Buck Converter with Regulator MOSFET or $V_{IN}$ < 45V**

| | | | |
|---|---|---|---|
| **$L_1$ (μH)** | 10 | 15 | 22 |
| **$L_1$ Saturation Current (mA)** | >450 | >300 | >200 |
| **$C_{OUT}$ (μF)** | 4.7 | | |
| **$C_{IN}$ (μF)** | 0.1 | | |

**Table 2. Recommended Value for Buck Converter without Regulator MOSFET and 45V < $V_{IN}$ < 60V**

| | | | |
|---|---|---|---|
| **$L_1$ (μH)** | 10 | 15 | 22 |
| **$L_1$ Saturation Current (mA)** | >550 | >400 | >300 |
| **$C_{OUT}$ (μF)** | 4.7 | | |
| **$C_{IN}$ (μF)** | 0.1 | | |

### 14.3 Regulator with Voltage Clamp Zener

When the input voltage $V_M$ is higher than 45V, the regulator circuit (as shown in Figure 4) clamps the input voltage VIN at 45V. Due to the high voltage drop across the regulator, it is important to pay attention to the power loss of the N-MOSFET and ensure proper heat dissipation. The values of peripheral circuit components C1 and R1 are listed in Table 3.

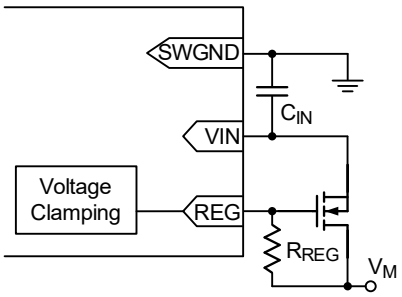



Figure 4. Regulator Circuit

**Table 3. The Recommended Value for Component $R_{REG}$ and $C_{IN}$**

| | |
|---|---|
| **$R_{REG}$ (Ω)** | 270k |
| **$C_{IN}$ (μF)** | 0.1 |

### 14.4 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; $T_A$ is the ambient temperature; and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to -ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a VQFN-32L 4x4 package, the thermal resistance, $\theta_{JA}$, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (27.8°C/W) = 3.59W for a VQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curve in Figure 5 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

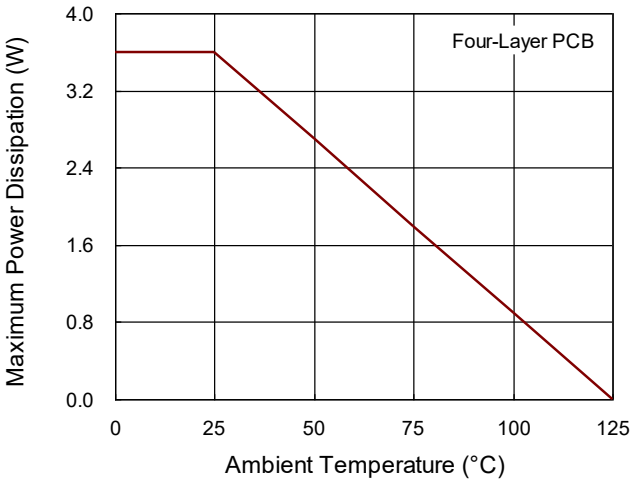
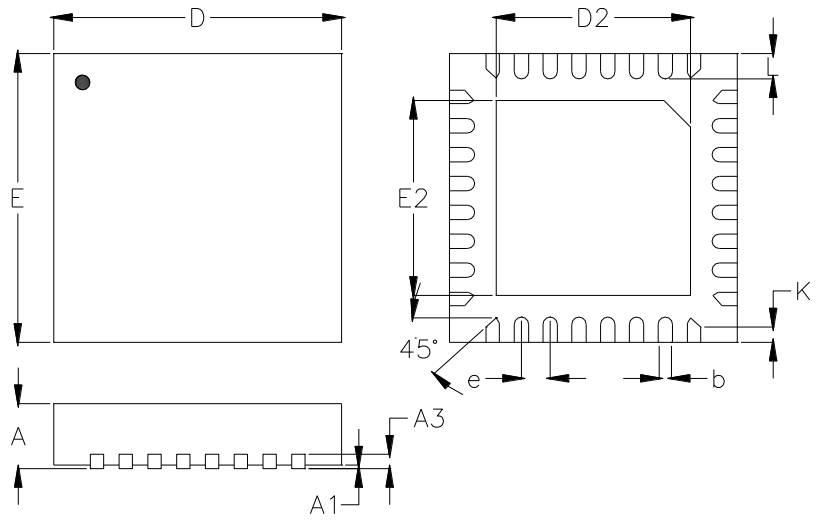
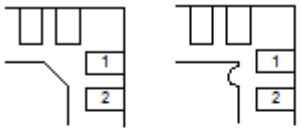



Figure 5. Derating Curve of Maximum Power Dissipation

**Note 9**. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

## 15 Outline Dimension




**DETAIL A**

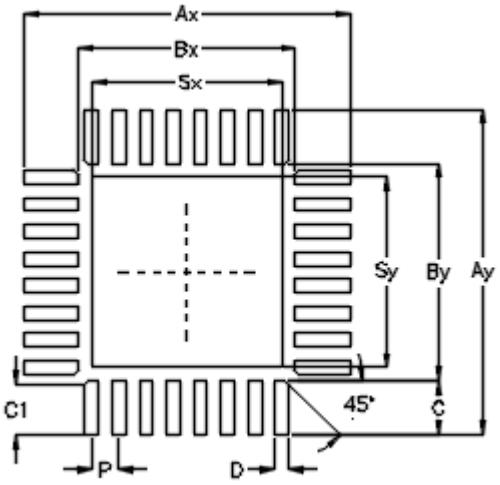
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 3.950 | 4.050 | 0.156 | 0.159 |
| D2 | 2.650 | 2.750 | 0.104 | 0.108 |
| E | 3.950 | 4.050 | 0.156 | 0.159 |
| E2 | 2.650 | 2.750 | 0.104 | 0.108 |
| e | 0.400 | | 0.016 | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |
| K | 0.200 | | 0.008 | |

**V-Type 32L QFN 4x4 Package**

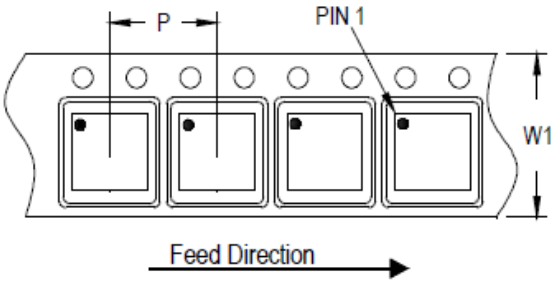
## 16 Footprint Information

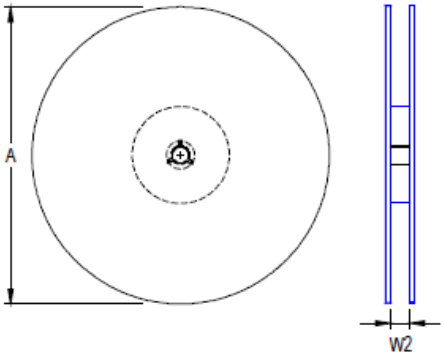


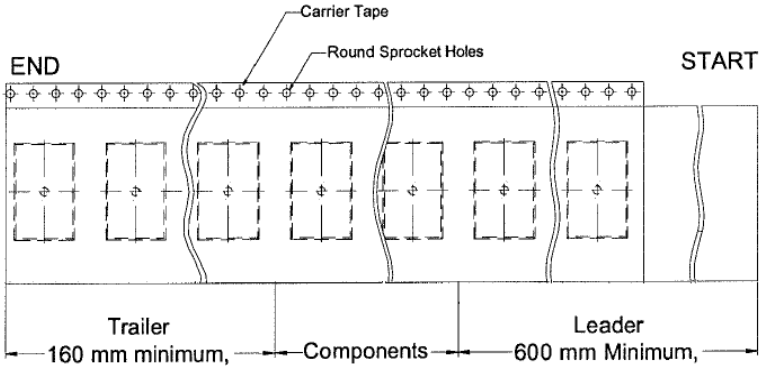

| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P | Ax | Ay | Bx | By | C*32 | C1*8 | D | Sx | Sy | |
| V/W/U/XQFN4*4-32 | 32 | 0.40 | 4.80 | 4.80 | 3.20 | 3.20 | 0.80 | 0.75 | 0.20 | 2.80 | 2.80 | ±0.05 |

# 17 Packing Information

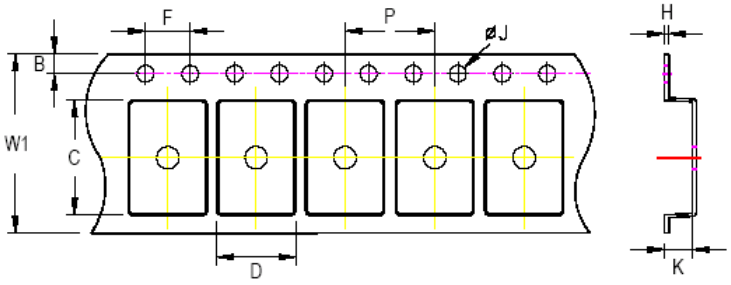
## 17.1 Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| (V, W) QFN/DFN 4x4 | 12 | 8 | 180 | 7 | 1,500 | 160 | 600 | 12.4/14.4 |




**C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 12mm carrier tape: 0.5mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | K | | H |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 12mm | 12.3mm | 7.9mm | 8.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 1.0mm | 1.3mm | 0.6mm |

### 17.2 Tape and Reel Packing

| Step | Photo/ Description | Step | Photo/ Description |
|---|---|---|---|
| 1 |  Reel 7” | 4 |  3 reels per inner box **Box A** |
| 2 |  HIC & Desiccant (1 Unit) inside | 5 |  12 inner boxes per outer box |
| 3 |  Caution label is on backside of Al bag | 6 |  Outer box **Carton A** |

| Container / Package | Reel | | Box | | | | Carton | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Size(cm) | Reels | Units | Item | Size(cm) | Boxes | Unit |
| (V, W) QFN & DFN 4x4 | 7” | 1,500 | Box A | 18.3*18.3*8.0 | 3 | 4,500 | Carton A | 38.3*27.2*40.0 | 12 | 54,000 |
| | | | Box E | 18.6*18.6*3.5 | 1 | 1,500 | For Combined or Partial Reel. | | | |

### 17.3 Packing Material Anti-ESD Property

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

**Richtek Technology Corporation**
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

## 18 Datasheet Revision History

| Version | Date | Description |
|---|---|---|
| 00 | 2024/6/7 | First Edition |
| 01 | 2026/6/8 | Absolute Maximum Ratings<br>Packing Information |