1A, 1MHz, 6V CMCOT Synchronous Step-Down Converter

General Description

The RT5710F is a high efficiency synchronous step-down DC-DC converter. Its input voltage range is from 2.5V to 6V and provides an adjustable regulated output voltage from 0.6V to 3.8V while delivering up to 1A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The Current Mode Constant-On-time (CMCOT) operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

Applications

- STB, Cable Modem, & xDSL Platforms
- LCD TV Power Supply & Metering Platforms
- General Purpose Point of Load (POL)

Ordering Information

RT5710F□□□

- Package Type
  QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup

Note :

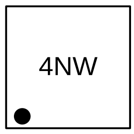
Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Efficiency Up to 95%**
- **$R_{DS(ON)}$ 160mΩ HS / 110mΩ LS**
- **V_{IN} Range 2.5V to 6V**
- **V_{REF} 0.6V with ±1% Accuracy**
- **CMCOT Control Loop Design for Best Transient Response, Robust Loop Stability with Low-ESR (MLCC) C_{OUT}**
- **Fixed Soft-Start 1.2ms**
- **Cycle-by-Cycle Over-Current Protection**
- **Input Under-Voltage Lockout**
- **Output Under-Voltage Protection (UVP Hiccup)**
- **Thermal Shutdown Protection**
- **Power Saving at Light Load**

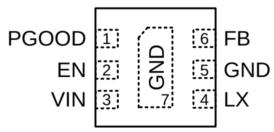
Marking Information



4N : Product Code
W : Date Code

Pin Configuration

(TOP VIEW)

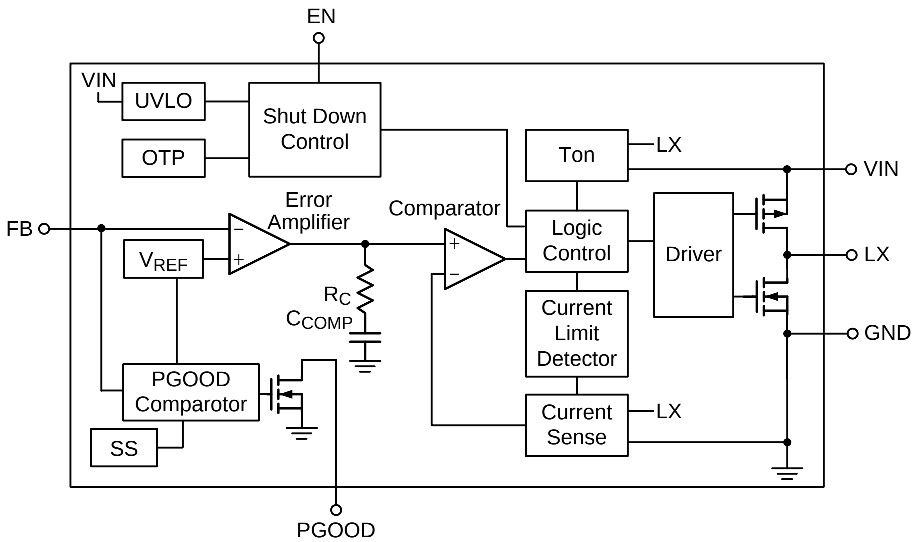


WDFN-6L 2x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGOOD	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. PGOOD is pulled up when the FB voltage is within 90%, otherwise it is LOW.
2	EN	Enable control input.
3	VIN	Supply voltage input. The RT5710F operates from a 2.5V to 6V input.
4	LX	Switch node.
5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	FB	Feedback.

Functional Block Diagram



Operation

The RT5710F is a synchronous low voltage step-down converter that can support the input voltage range from 2.5V to 6V and the output current can be up to 1A. The RT5710F uses a constant on-time, current mode architecture. In normal operation, the high-side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low-side MOSFET peak current is measured by internal RSENSE. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

UV Comparator

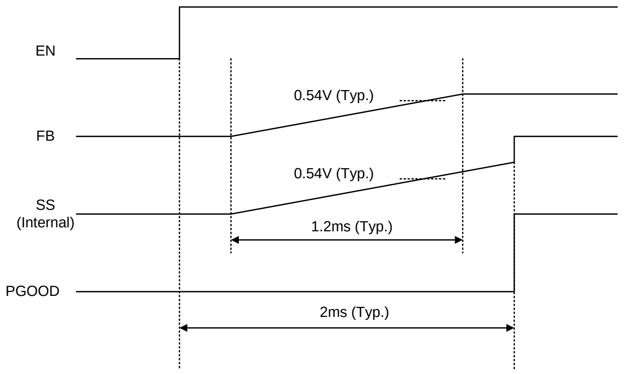
If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V, the UV comparator's output will go high and the switch controller will turn off the high-side MOSFET. The output under-voltage protection is designed to operate in Hiccup mode.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 1.2ms.

PGOOD Comparator

When the feedback voltage (V_{FB}) is higher than threshold voltage 0.54V and the internal soft-start function has been finished, the PGOOD open drain output will be high impedance. The internal PGOOD MOSFET is typical 100Ω. The PGOOD signal delay time is defined from EN high to the internal soft-start function end which is about 2ms (Typ.).



Enable Comparator

A logic-high enables the converter; a logic-low forces the IC into shutdown mode.

Over-Current Protection (OCP)

The RT5710F provides over-current protection by detecting low-side MOSFET valley inductor current. If the sensed valley inductor current is over the current limit threshold (1.5A typ.), the OCP will be triggered. When OCP is tripped, the RT5710F will keep the over current threshold level until the over current condition is removed.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C, the device reinstates the power up sequence.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6.5V
- LX Pin Switch Voltage---------- –0.3V to (V_{IN} + 0.3V)
  <20ns---------- –4.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 2.1W
- Package Thermal Resistance (Note 2)
  WDFN-6L 2x2, θ_{JA} ---------- 47.5°C/W
  WDFN-6L 2x2, θ_{JC} ---------- 11.5°C/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 6V
- Ambient Temperature Range---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.5	--	6	V
Feedback Reference Voltage		V_{REF}		0.594	0.6	0.606	V
Feedback Leakage Current		I_{FB}	V_{FB} = 0.6V	--	--	0.1	μA
DC Bias Current			Active, V_{FB} = 0.63V, not switching	--	22	--	μA
			Shutdown	--	--	1	
Switching Leakage Current				--	--	1	μA
Switching Frequency				--	1	--	MHz
Switch On Resistance, High		R_{PMOS}	I_{LX} = 0.3A	--	160	--	mΩ
Switch On Resistance, Low		R_{NMOS}	I_{LX} = 0.3A	--	110	--	mΩ
Valley Current Limit		I_{LIM}		1.1	1.5	2	A
Under-Voltage Lockout Threshold		V_{UVLO}	V_{DD} rising	--	2.25	2.5	V
			V_{DD} falling	--	2	--	
Over-Temperature Threshold				--	150	--	°C
EN Threshold Voltage	H-Level	V_{ENH}	EN rising	0.7	0.85	1.05	V
	L-Level	V_{ENL}	EN falling	0.5	0.75	0.95	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD Pin Threshold (relative to V_{OUT})		FB rising	--	90	--	%
		FB falling	--	85	--	
PGOOD Open-Drain Impedance (PGOOD = low)			--	--	100	Ω
Soft-Start Time	t_{SS}		--	1.2	--	ms
Minimum Off-Time	t_{OFF_MIN}		--	120	--	ns
Output Discharge Switch On Resistance			--	1.8	--	kΩ

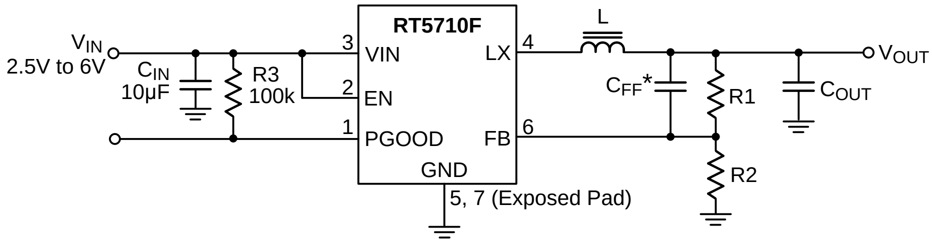
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

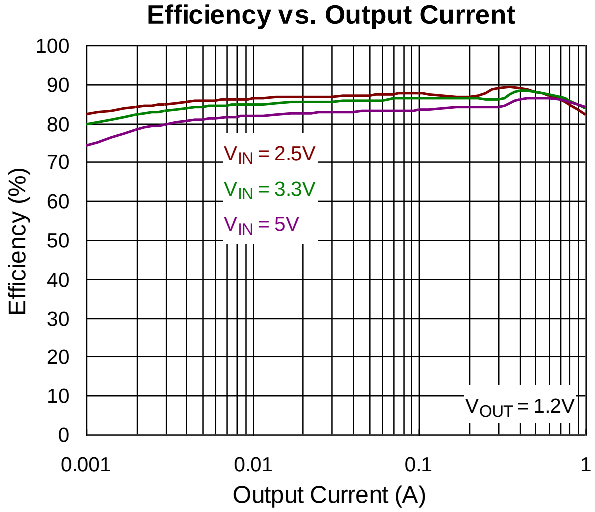


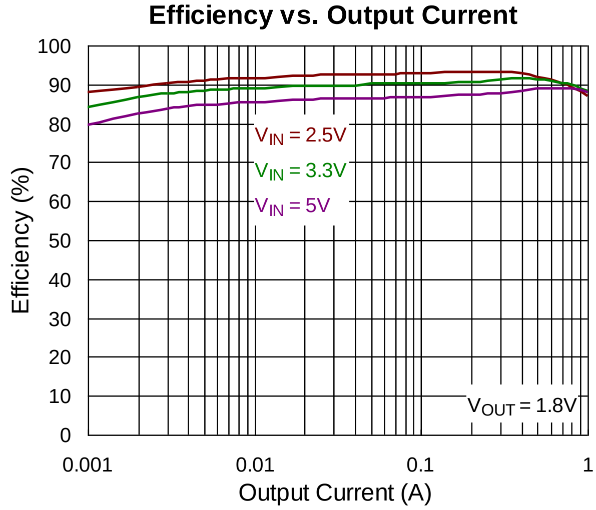
*C_{FF} : Optional, 6.8pF if it is needed

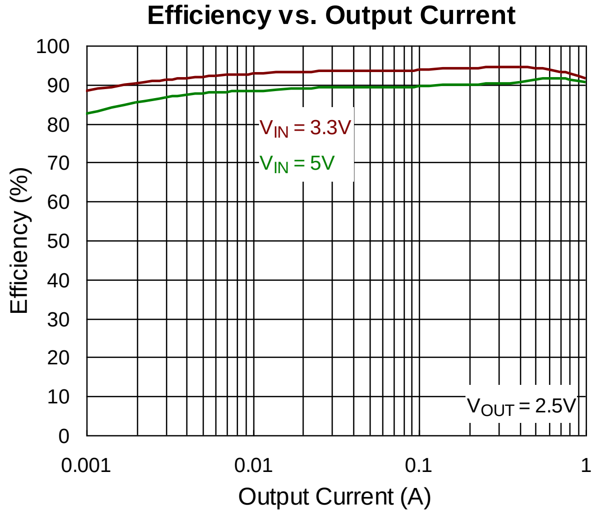
Table 1. Suggested Component Values

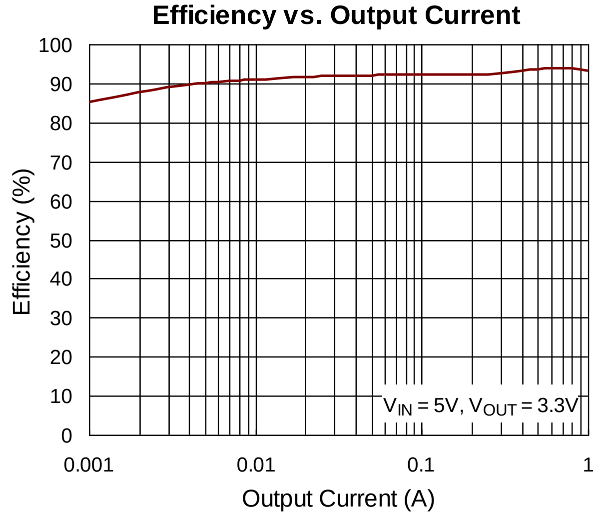
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
3.3	90	20	1.5	10
1.8	100	50	1.5	10
1.5	100	66.6	1.5	10
1.2	100	100	1.5	10
1.05	100	133	1.5	10
1	100	148	1.5	10

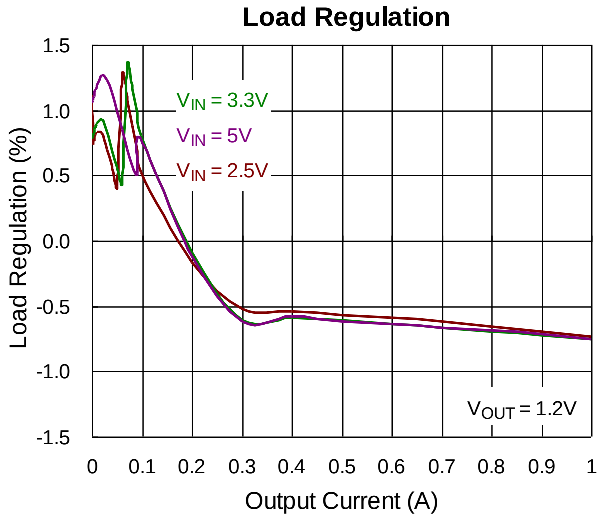
Typical Operating Characteristics

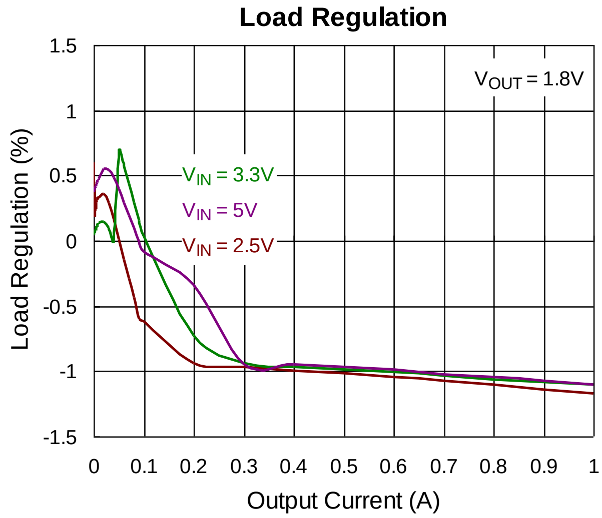


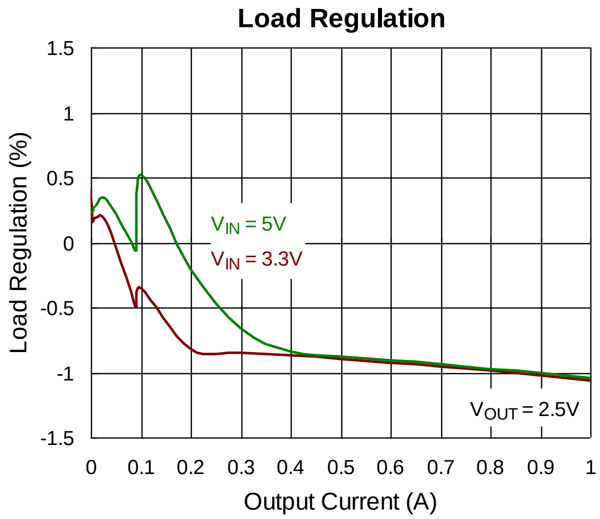


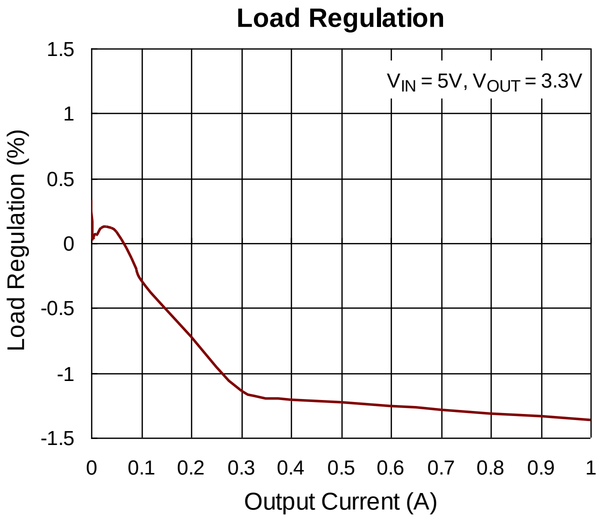


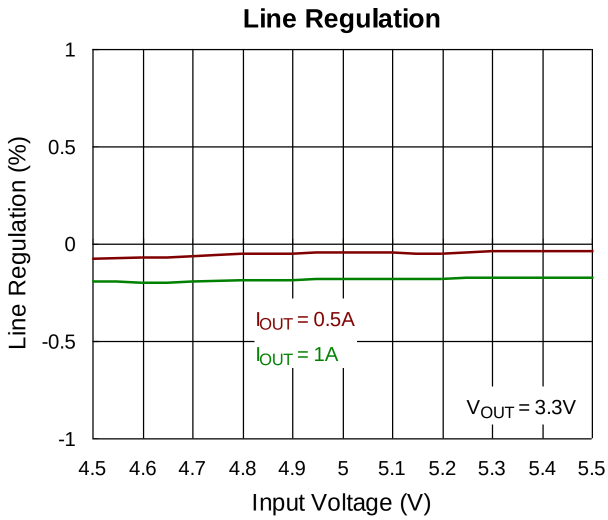


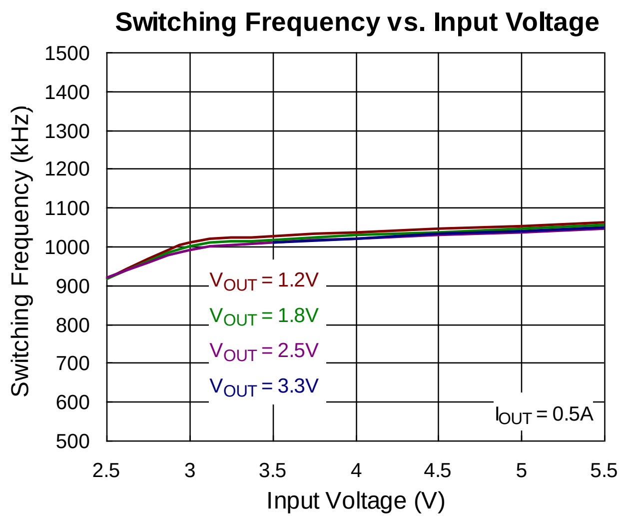


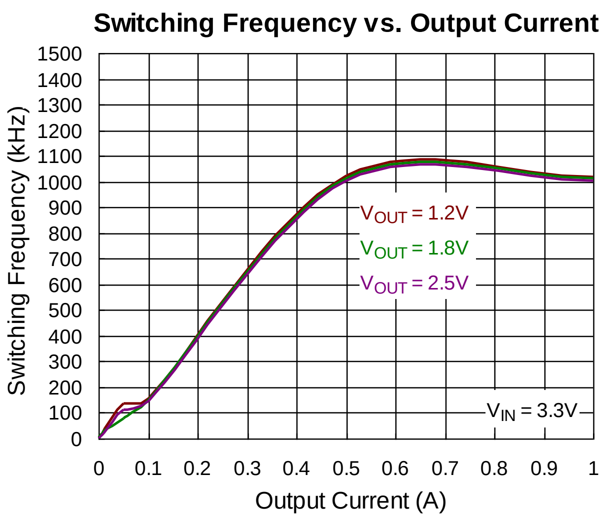


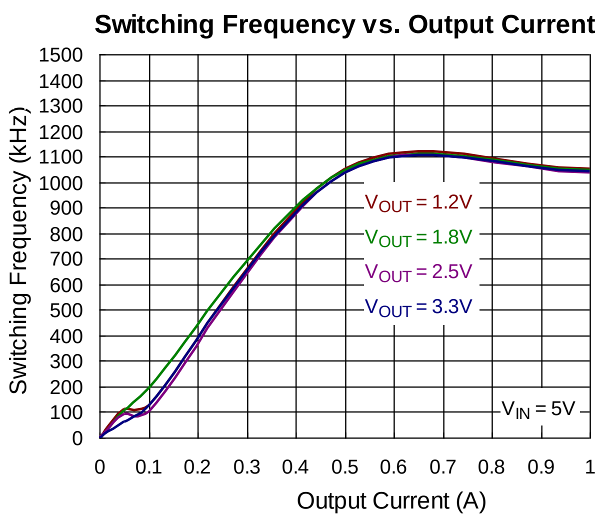

Load Regulation
Load Regulation (%)
Output Current (A)
VIN = 5V
VIN = 3.3V
VOUT = 2.5V


Load Regulation
VIN = 5V, VOUT = 3.3V
Load Regulation (%)
Output Current (A)

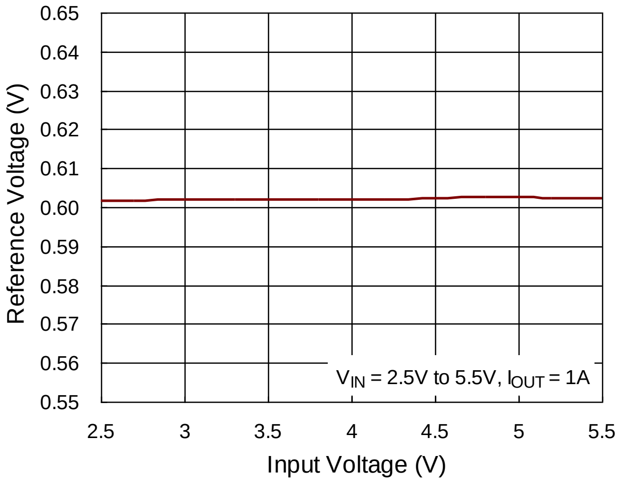

Line Regulation
Line Regulation (%)
Input Voltage (V)
IOUT = 0.5A
IOUT = 1A
VOUT = 3.3V


Switching Frequency vs. Input Voltage
Switching Frequency (kHz)
Input Voltage (V)
VOUT = 1.2V
VOUT = 1.8V
VOUT = 2.5V
VOUT = 3.3V
IOUT = 0.5A

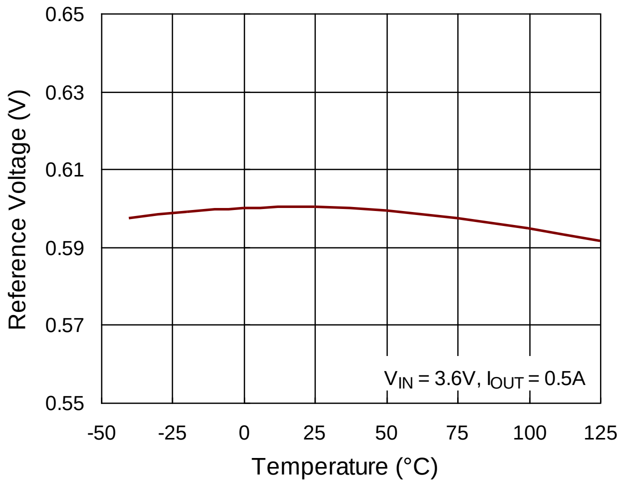

Switching Frequency vs. Output Current
Switching Frequency (kHz)
Output Current (A)
VOUT = 1.2V
VOUT = 1.8V
VOUT = 2.5V
VIN = 3.3V


Switching Frequency vs. Output Current
Switching Frequency (kHz)
Output Current (A)
VOUT = 1.2V
VOUT = 1.8V
VOUT = 2.5V
VOUT = 3.3V
VIN = 5V

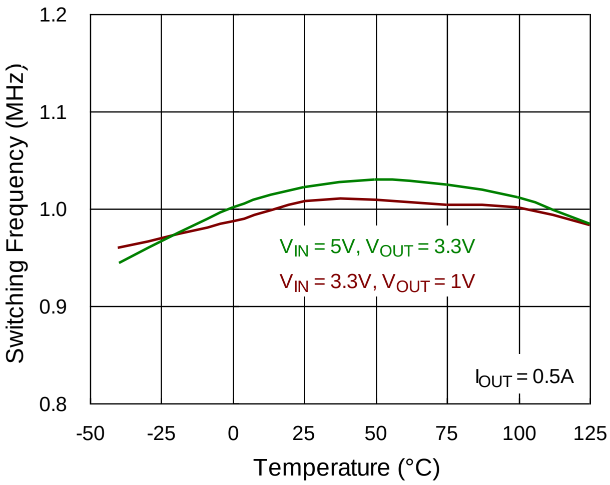
Reference Voltage vs. Input Voltage



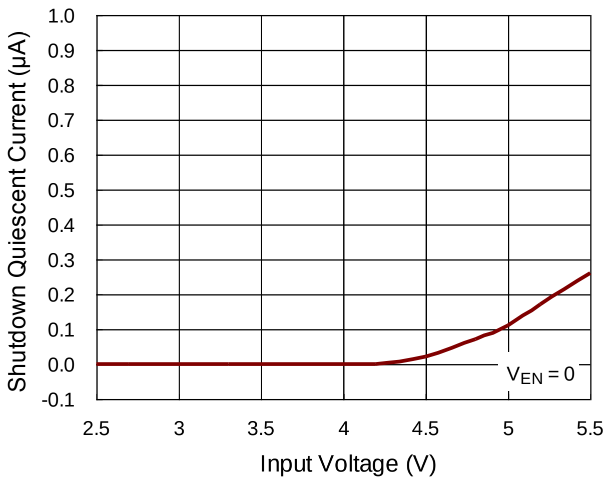
Reference Voltage vs. Temperature



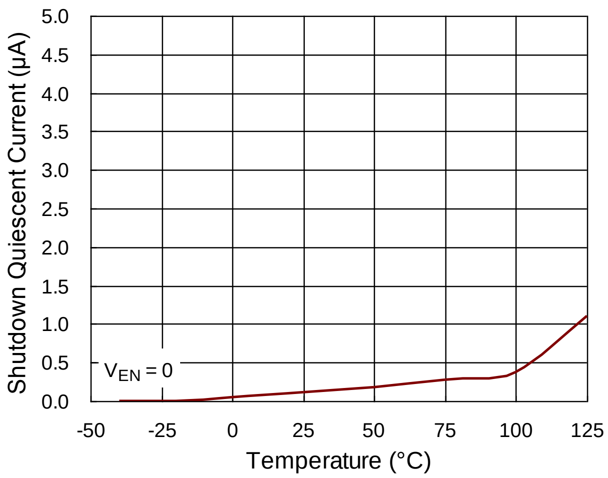
Switching Frequency vs.Temperature



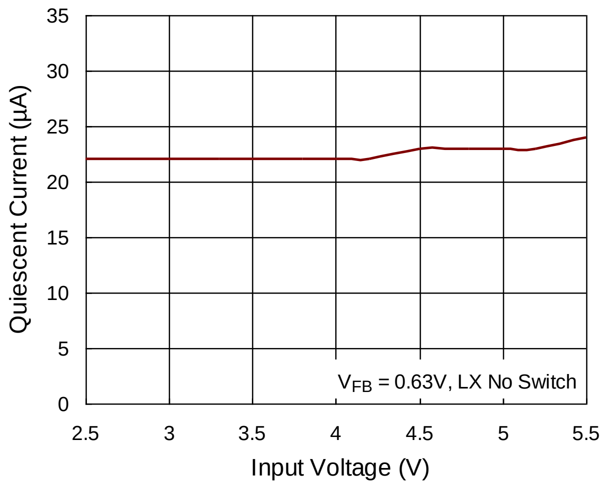
Shutdown Quiescent Current vs. Input Voltage

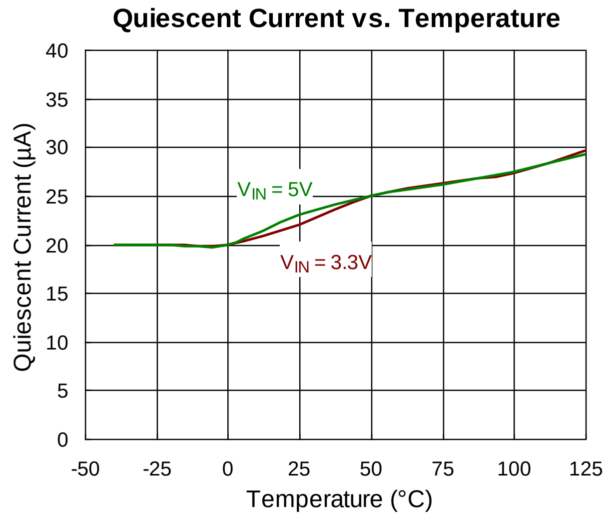


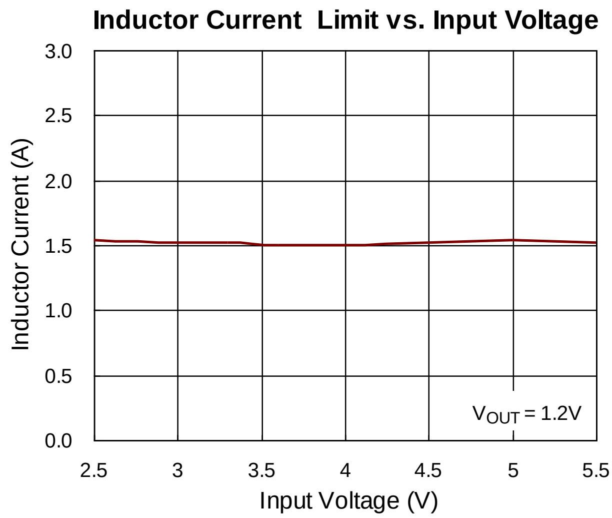
Shutdown Quiescent Current vs. Temperature

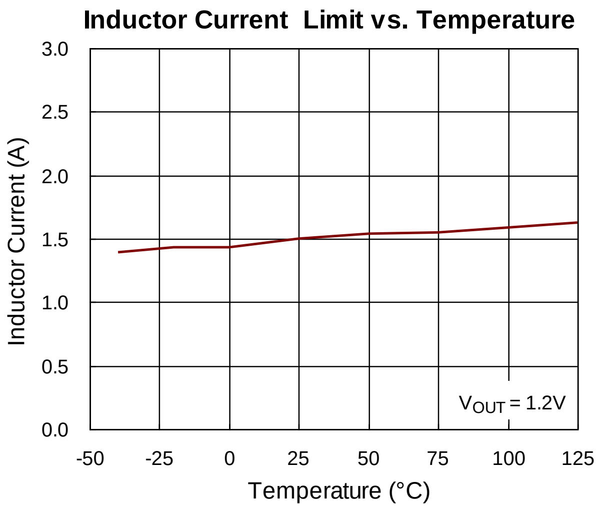


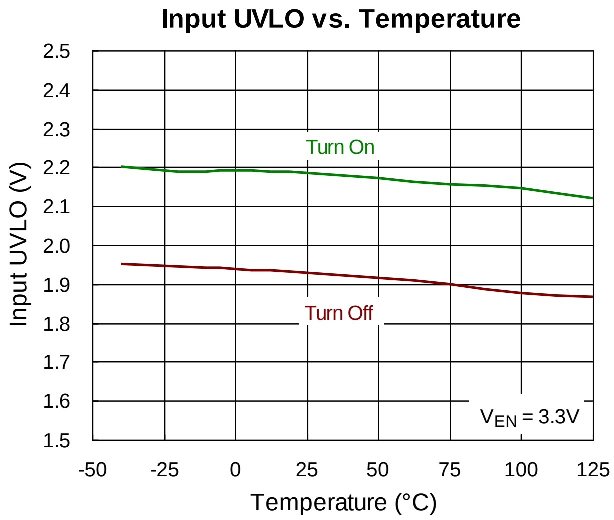
Quiescent Current vs. Input Voltage

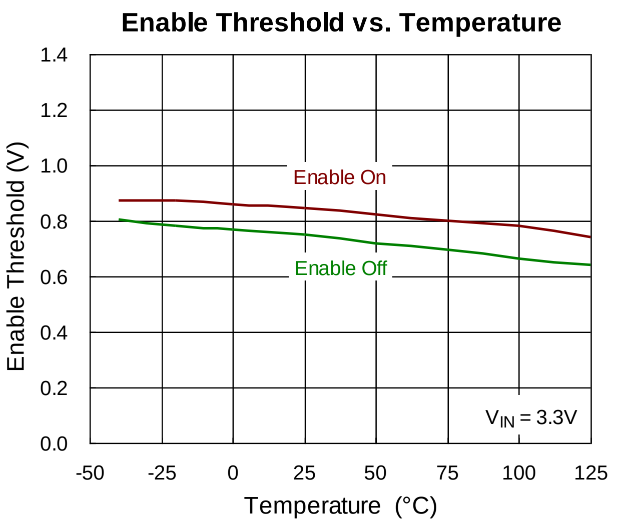


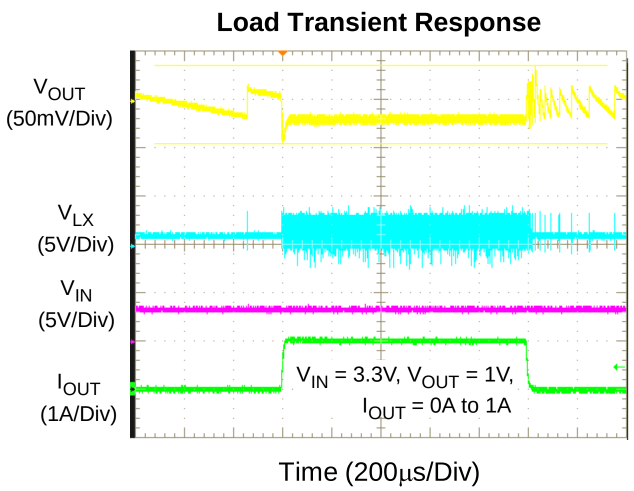

Quiescent Current vs. Temperature
Quiescent Current (μA)
40
35
30
25
20
15
10
5
0
-50
-25
0
25
50
75
100
125
Temperature (°C)
VIN = 5V
VIN = 3.3V


Inductor Current Limit vs. Input Voltage
Inductor Current (A)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
2.5
3
3.5
4
4.5
5
5.5
Input Voltage (V)
VOUT = 1.2V

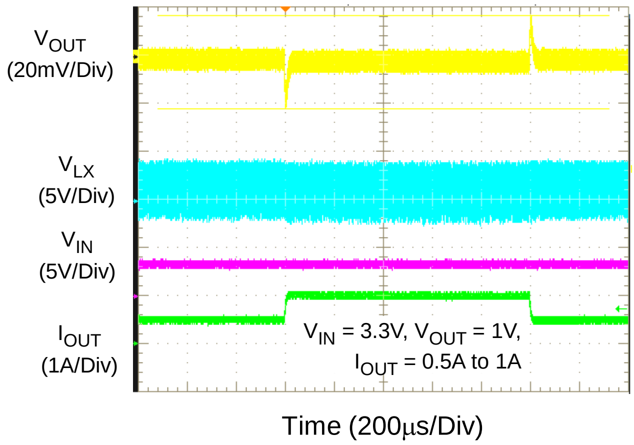

Inductor Current Limit vs. Temperature
Inductor Current (A)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
VOUT = 1.2V


Input UVLO vs. Temperature
Input UVLO (V)
2.5
2.4
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
-50
-25
0
25
50
75
100
125
Temperature (°C)
Turn On
Turn Off
VEN = 3.3V

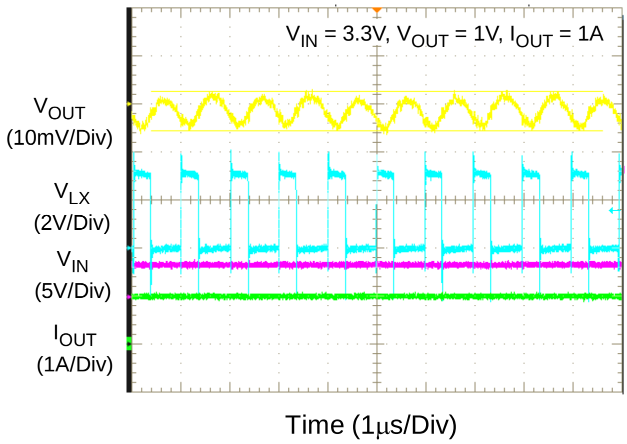

Enable Threshold vs. Temperature
Enable Threshold (V)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
Enable On
Enable Off
VIN = 3.3V


Load Transient Response
VOUT (50mV/Div)
VLX (5V/Div)
VIN (5V/Div)
IOUT (1A/Div)
VIN = 3.3V, VOUT = 1V,
IOUT = 0A to 1A
Time (200μs/Div)

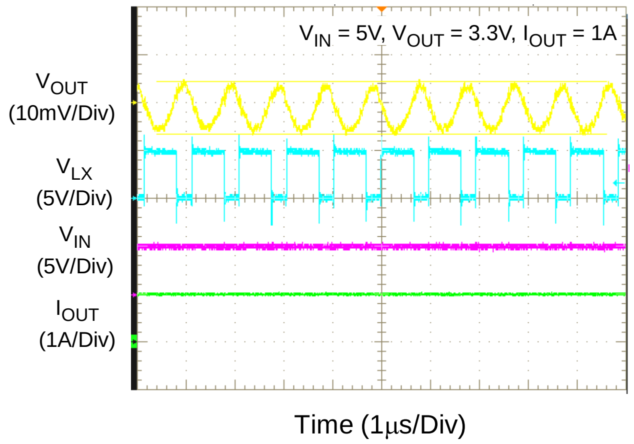
Load Transient Response



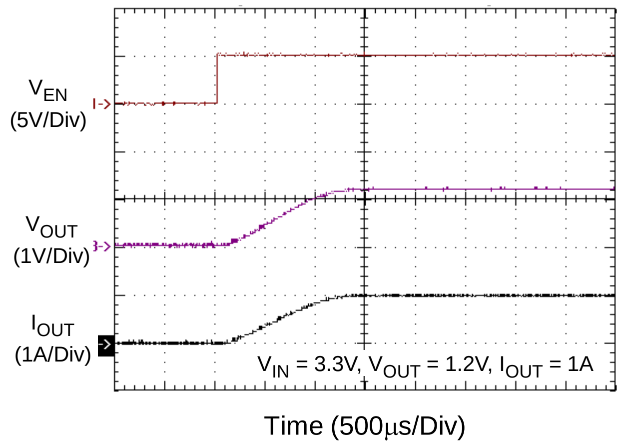
Voltage Ripple



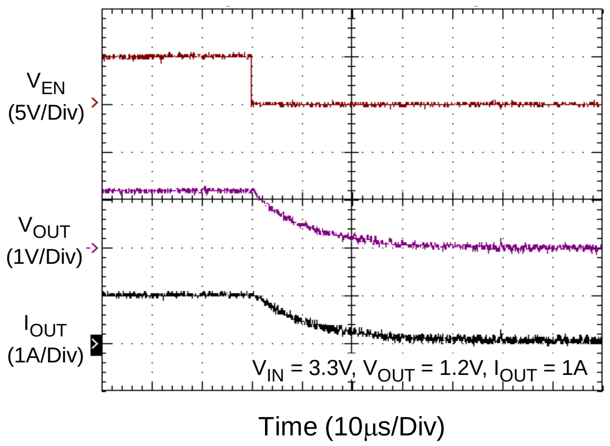
Voltage Ripple



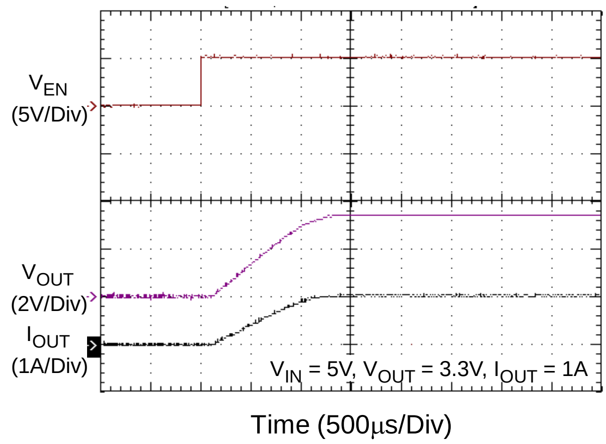
Power On from EN



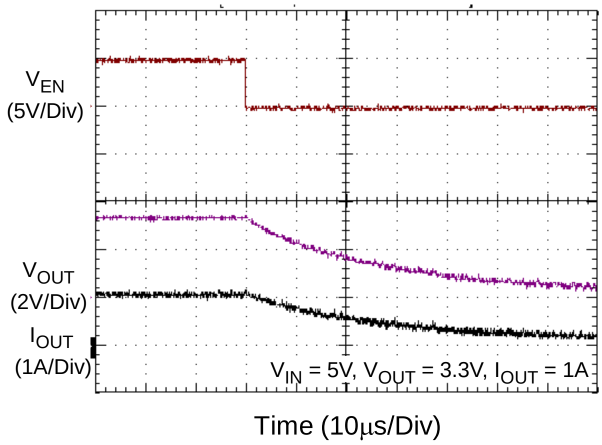
Power Off from EN



Power On from EN



Power Off from EN



Application Information

The RT5710F is a single-phase step-down converter. It provides single feedback loop, constant on-time current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over-current protection, under-voltage protection and over-temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typ.).

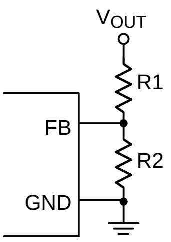


Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT5710F remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT5710F begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT5710F provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

UVLO Protection

The RT5710F has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.25V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Inductor saturation current should be chosen over IC's current limit.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10μF are recommended for the input capacitor. The X5R and

X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-6L 2x2 package, the thermal resistance, θ_{JA}, is 47.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (47.5°C/W) = 2.1W for a WDFN-6L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

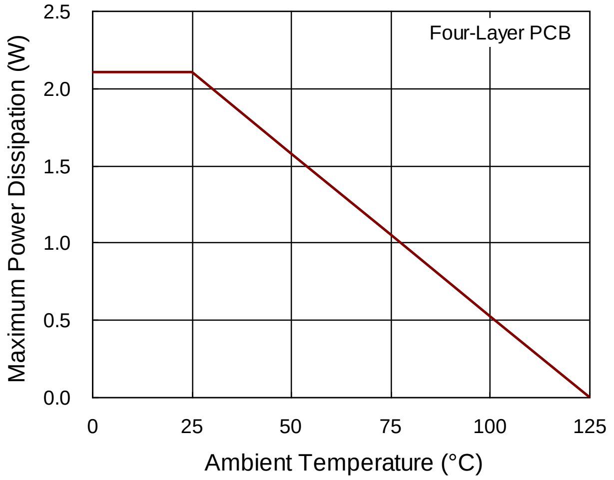


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT5710F, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close to the IC as possible.
- LX should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- Keep every trace connected to pin as wide as possible for improving thermal dissipation.
- The feedback components must be connected as close to the device as possible. Keep sensitive component away.
- Via can help to reduce power trace and improve thermal dissipation.

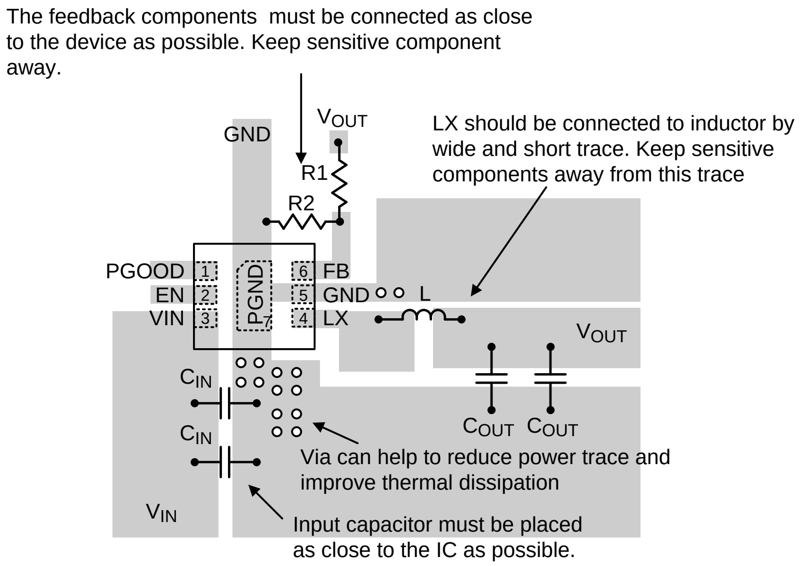
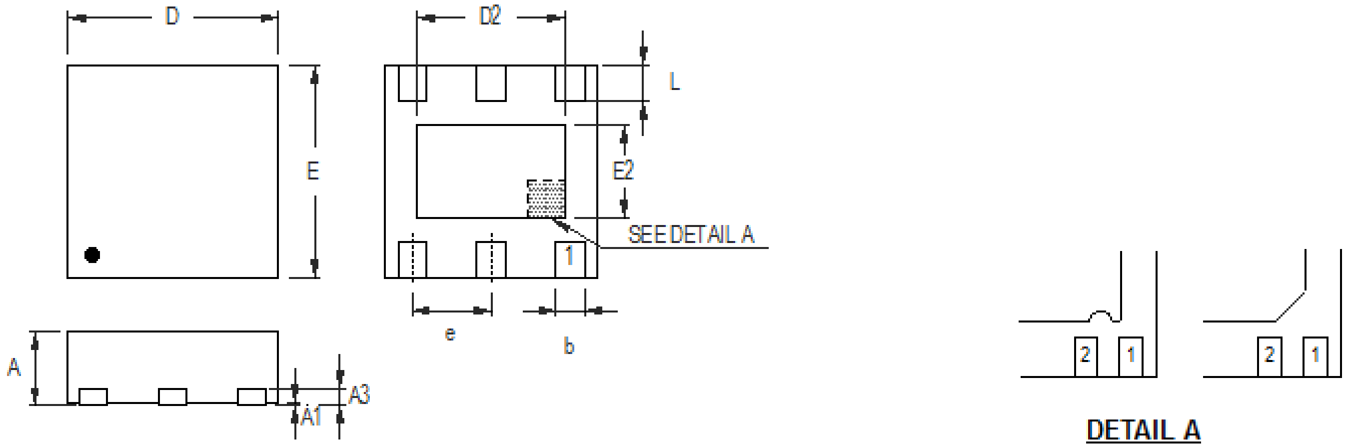


Figure 3. PCB Layout Guide

Outline Dimension



DETAIL A

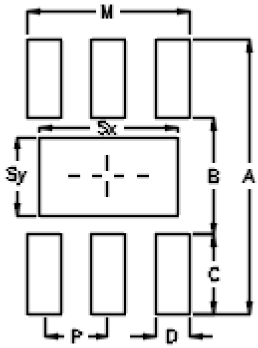
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-6	6	0.65	2.80	1.20	0.80	0.35	1.40	0.80	1.65	±0.05

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