2A, 18V, 800kHz, ACOT™ Step-Down Converter

General Description

The RT6212C/D is a high-efficiency, monolithic synchronous step-down DC-DC converter that can deliver up to 2A output current from a 4.5V to 18V input supply. The RT6212C/D adopts ACOT architecture to allow the transient response to be improved and keep in constant frequency. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault conditions also include output under-voltage protection, output over-current protection, and thermal shutdown.

Ordering Information

RT6212C/D □□□

- Package Type
  J6F : TSOT-23-6 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup
- PSM/PWM
  C : PSM/PWM
  D : Force-PWM

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

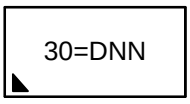
- **Integrated 163mΩ/86mΩ MOSFETs**
- **4.5V to 18V Supply Voltage Range**
- **800kHz Switching Frequency**
- **ACOT Control**
- **Feedback Reference Voltage 0.8V ± 1.5%**
- **Internal Start-Up into Pre-Biased Outputs**
- **Compact Package : TSOT-23-6 Pin**
- **Input Under-Voltage Lockout**
- **Over-Current Protection and Hiccup**

Applications

- Set-Top Boxes
- Portable TVs
- Access Point Routers
- DSL Modems
- LCD TVs

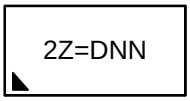
Marking Information

RT6212CHGJ6F



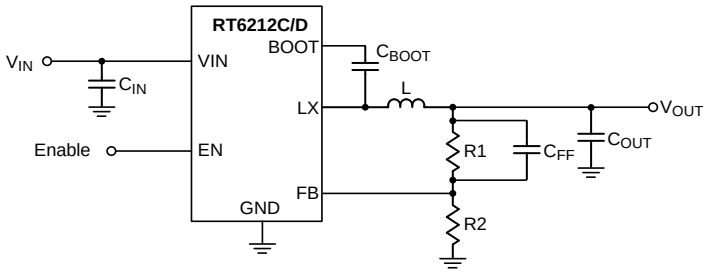
30= : Product Code
DNN : Date Code

RT6212DHGJ6F



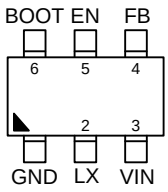
2Z= : Product Code
DNN : Date Code

Simplified Application Circuit



Pin Configuration

(TOP VIEW)

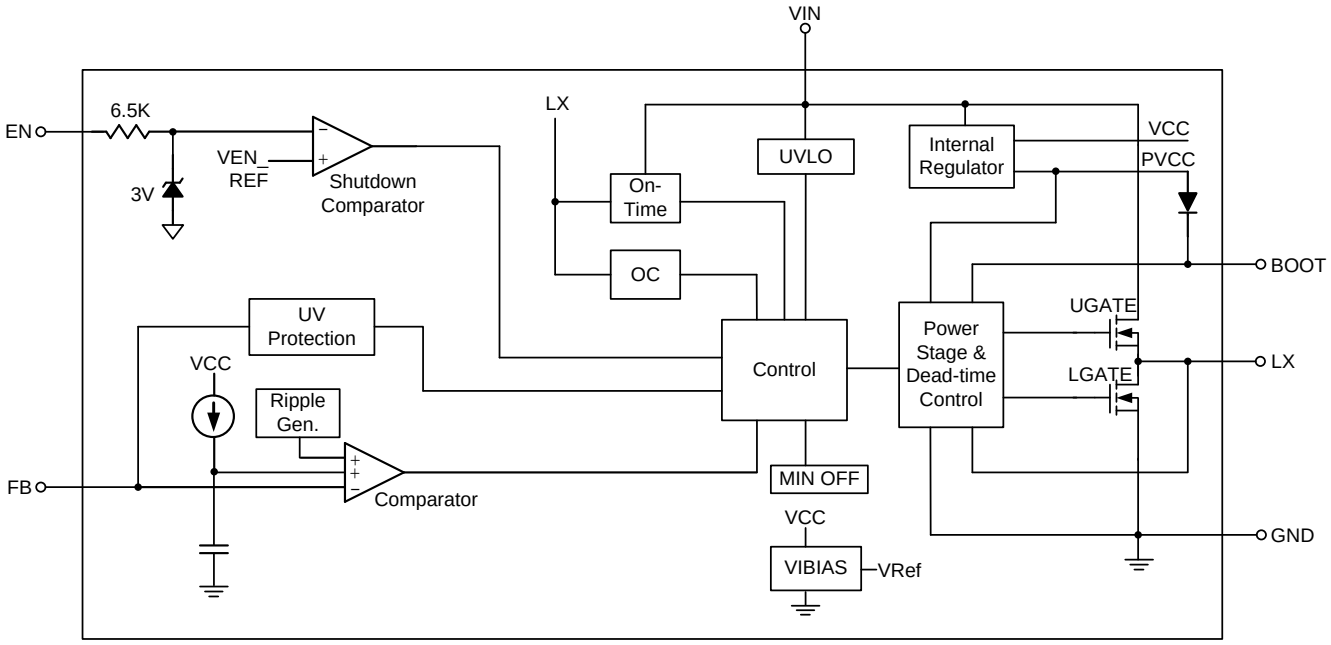


TSOT-23-6 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	System ground. Provides the ground return path for the control circuitry and low-side power MOSFET.
2	LX	Switch node. LX is the switching node that supplies power to the output and connect the output LC filter from LX to the output load.
3	VIN	Power input. Supplies the power switches of the device.
4	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback voltage is 0.8V typically.
5	EN	Enable control input. Floating this pin or connecting this pin to GND can disable the device and connecting this pin to logic high can enable the device.
6	BOOT	Bootstrap supply for high-side gate driver. Connect a 100nF or greater capacitor from LX to BOOT to power the high-side switch.

Functional Block Diagram

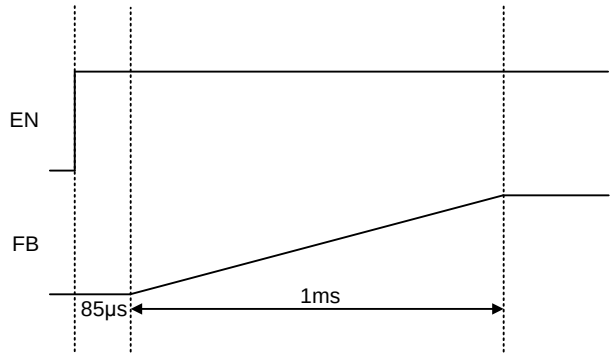


Operation

The RT6212C/D is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT™ control mode can reduce the output capacitance and provide fast transient response. It can minimize the component size without additional external compensation network.

Soft-Start (SS)

The RT6212C/D provides an internal soft-start feature for inrush control. At power up, the internal capacitor is charged by an internal current source I_{SS} to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up. The output voltage starts to rise in 85μs from EN rising, and the soft-start ramp-up time (V_{FB} from 0V to 0.8V) is 1ms.



UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be lockout.

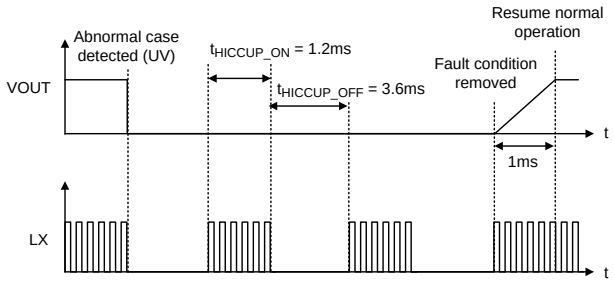
Thermal Shutdown

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will autocratically resume switching.

Output Under-Voltage Protection and Hiccup Mode

The RT6212C/D includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period of time, the RT6212C/D will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (3.6ms), and then attempt to recover automatically for t_{HICCUP_ON} (1.2ms). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –0.3V to (V_{IN} + 0.3V)
  < 50ns ---------- –6V to 25V
- BOOT Pin Voltage ---------- (V_{LX} – 0.3V) to (V_{IN} + 6.3V)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-6 (FC) ---------- 1.667W
- Package Thermal Resistance (Note 2)
  TSOT-23-6 (FC), θ_{JA} ---------- 60°C/W
  TSOT-23-6 (FC), θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	18	V
Under-Voltage Lockout Threshold	V_{UVLO}		3.6	3.9	4.2	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	340	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.85V	--	0.5	--	mA
Soft-Start						
Soft-Start Time	t_{SS}		--	1000	--	μs
Enable Voltage						
Enable Voltage Threshold	V_{EN_R}	V_{EN} rising	1.4	1.5	1.6	V
	V_{EN_F}	V_{EN} falling	1.18	1.28	1.38	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Voltage						
Feedback Reference Voltage	V_{REF}	4.5V ≤ V_{IN} ≤ 18V	0.788	0.8	0.812	V
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$	V_{BOOT} − V_{LX} = 4.8V	--	163	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	86	--	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}		--	5.8	--	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		2.6	3.3	--	
Switching Frequency						
Switching Frequency	f_{SW}		600	800	1000	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		35	60	85	ns
Minimum Off-Time	t_{OFF_MIN}		185	240	315	
Output Under-Voltage and Over-Voltage Protections						
OVP Trip Threshold		OVP detect	--	125	--	%
OVP Propagation Delay			--	10	--	µs
UVP Trip Threshold		UVP detect	45	50	55	%
		Hysteresis	--	10	--	
UVP Propagation Delay			--	5	--	µs
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JA} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

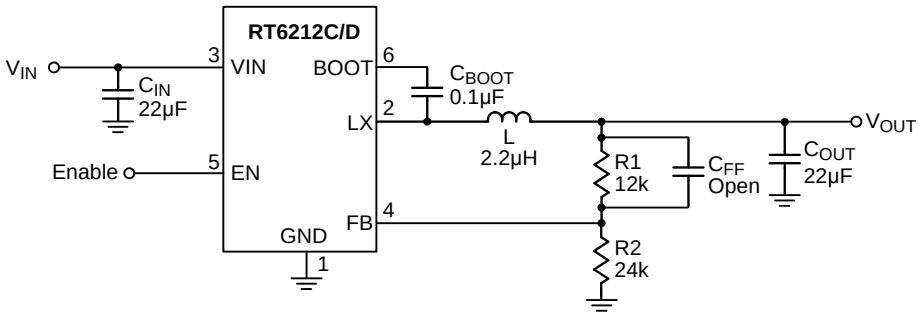


Table 1. Recommended Components Selection (RT6212C/DHGJ6F)

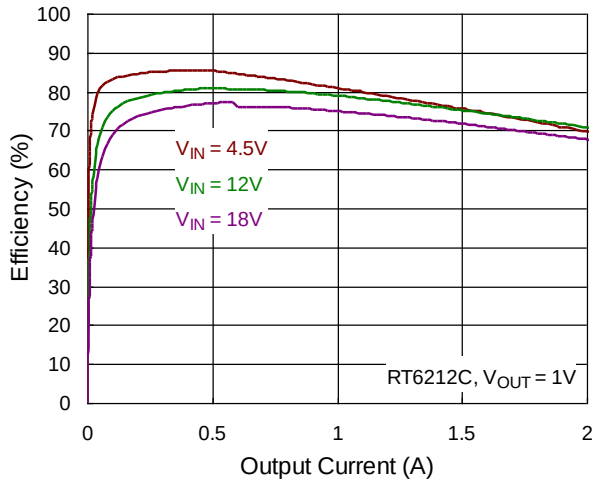
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF)
1	6	24	--	1.2	22
1.2	12	24	--	1.2	22
1.5	21	24	--	2.2	22
1.8	30	24	10 to 100	2.2	22
2.5	51	24	10 to 68	2.2	22
3.3	75	24	10 to 68	2.2	22
5	126	24	10 to 68	3.3	22

Note : (1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

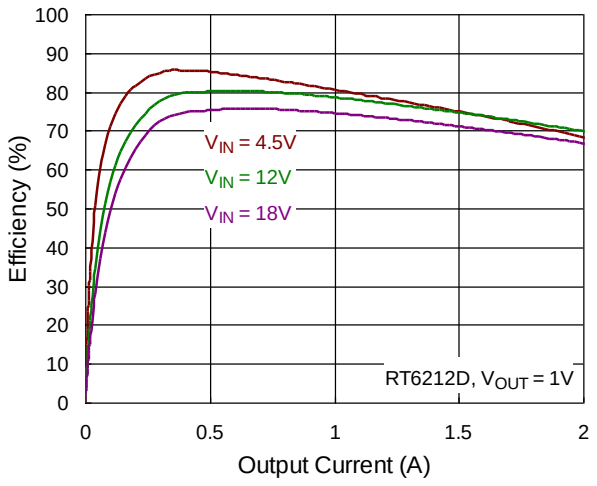
(2) For low output voltage application, it can optimize the load transient response of the device by adding feedforward capacitor (C_{FF}).

Typical Operating Characteristics

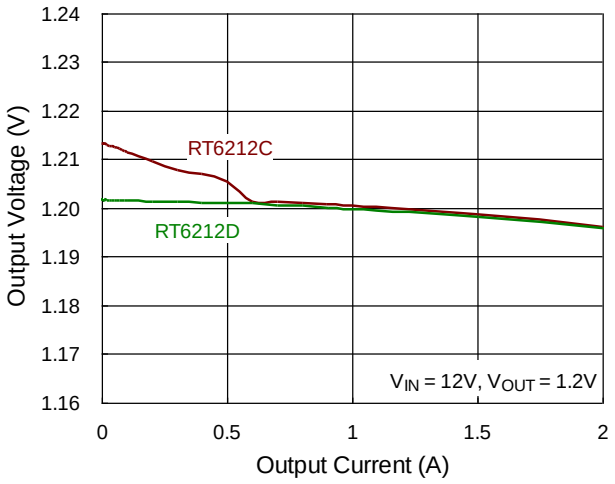
Efficiency vs. Output Current



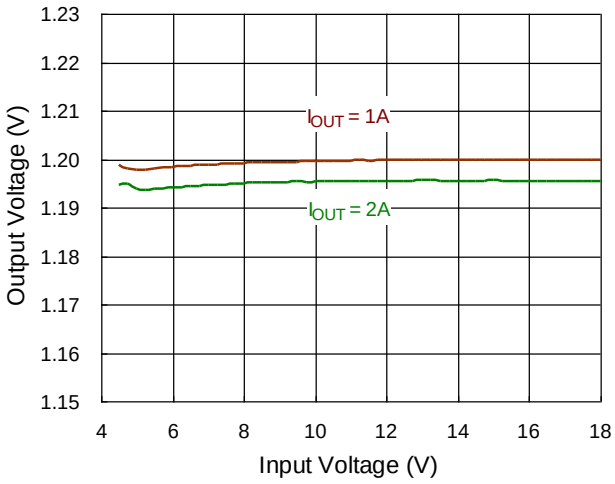
Efficiency vs. Output Current



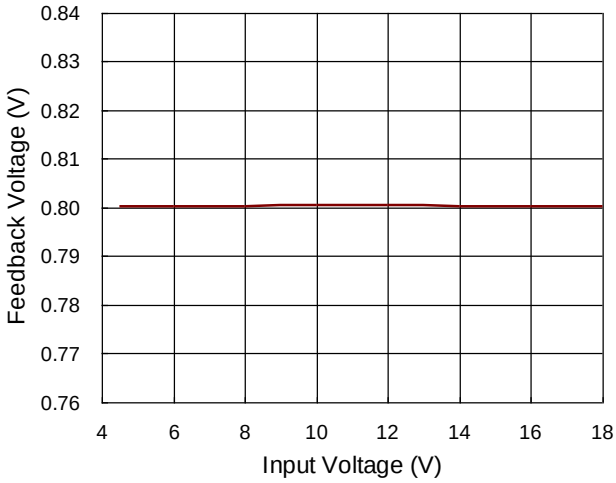
Output Voltage vs. Output Current



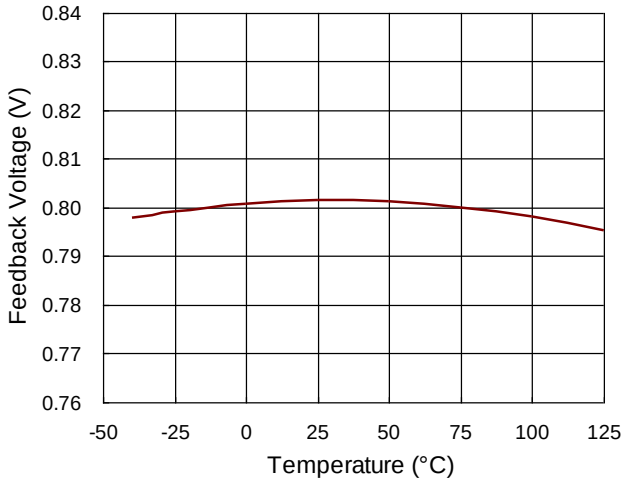
Output Voltage vs. Input Voltage



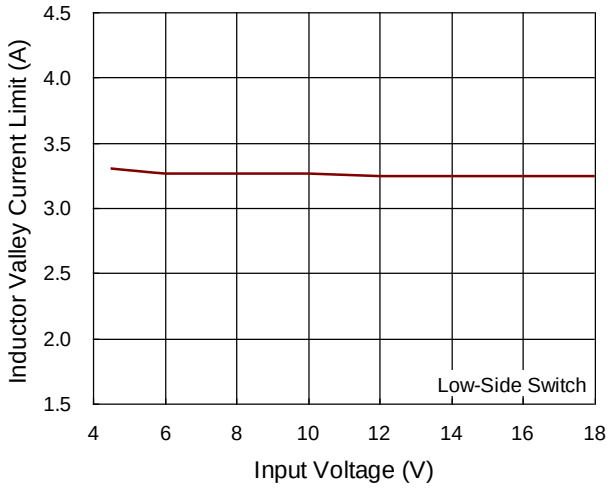
Feedback Voltage vs. Input Voltage



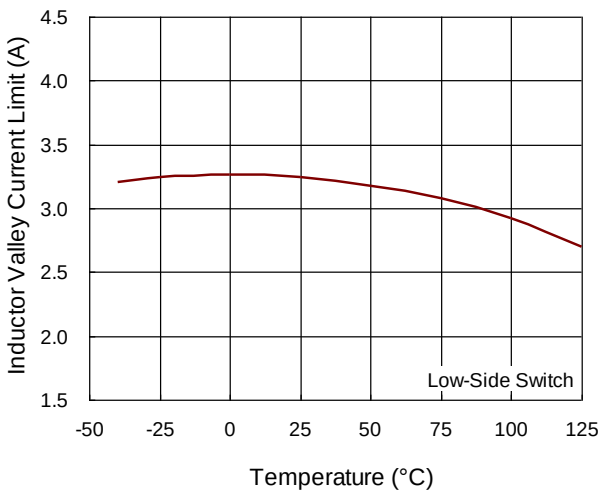
Feedback Voltage vs. Temperature



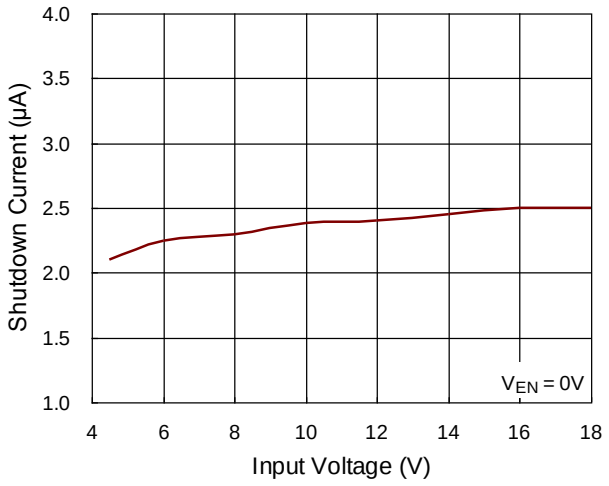
Inductor Valley Current Limit vs. Input Voltage



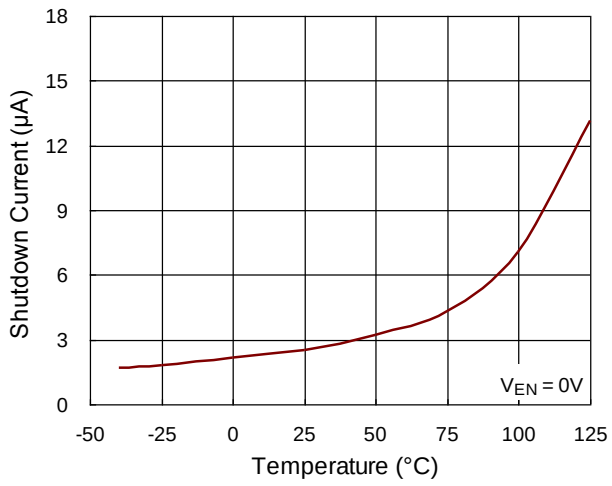
Inductor Valley Current Limit vs. Temperature



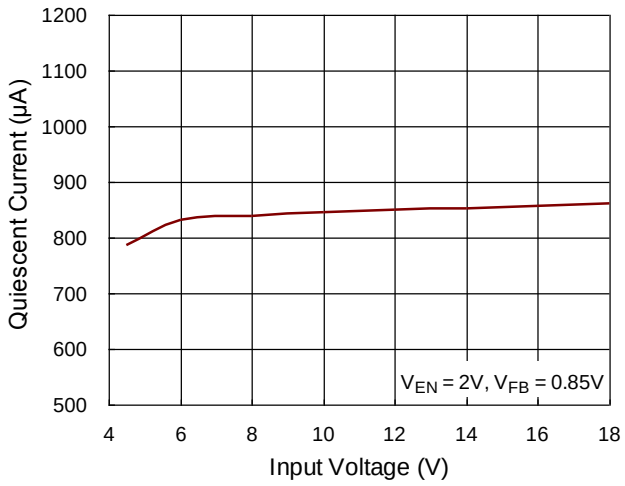
Shutdown Current vs. Input Voltage



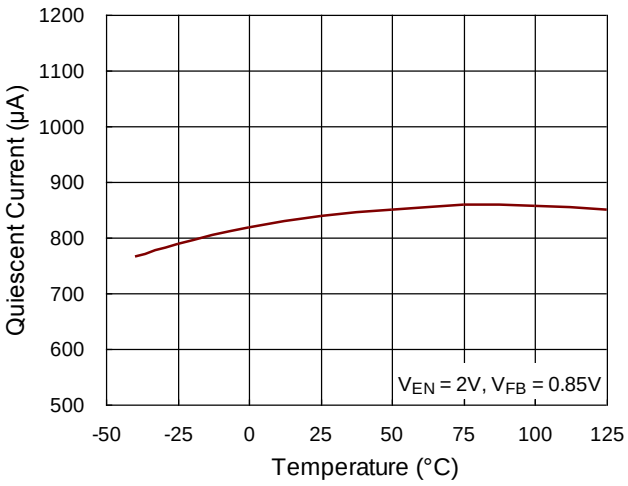
Shutdown Current vs. Temperature



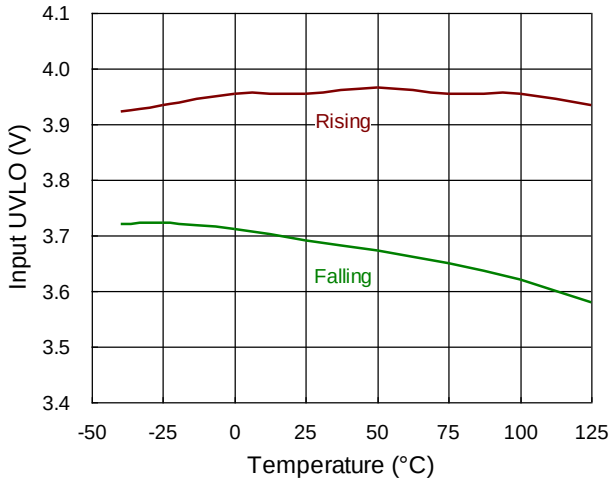
Quiescent Current vs. Input Voltage



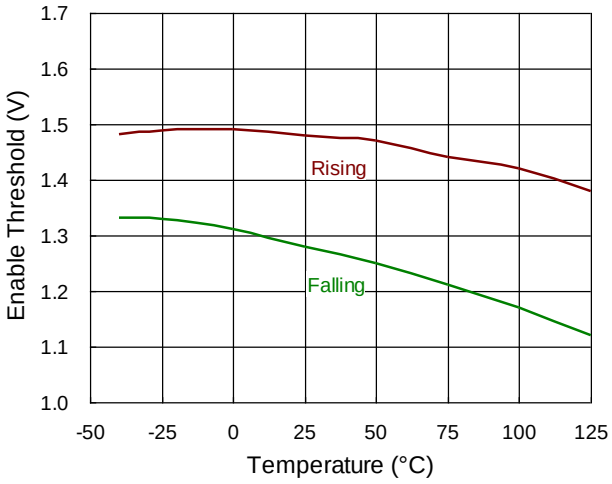
Quiescent Current vs. Temperature



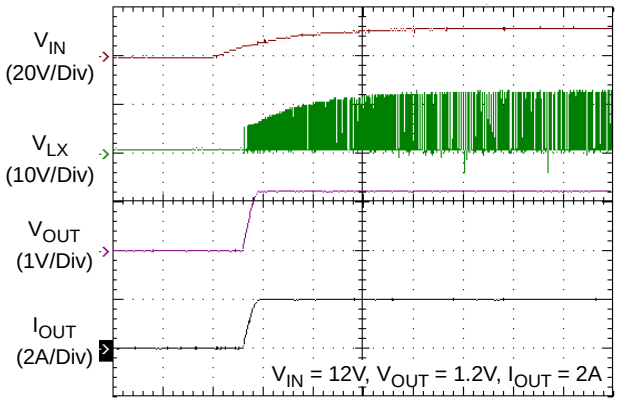
Input UVLO vs. Temperature



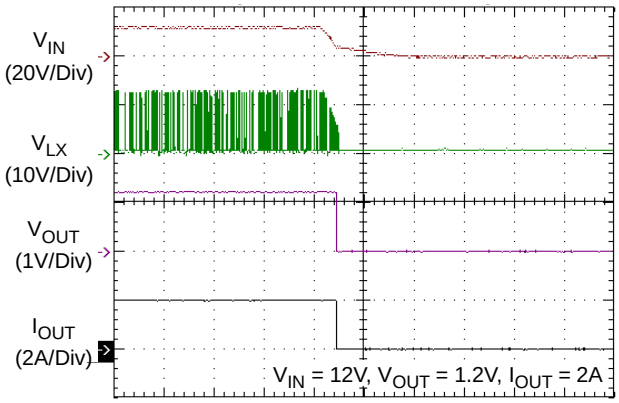
Enable Threshold vs. Temperature



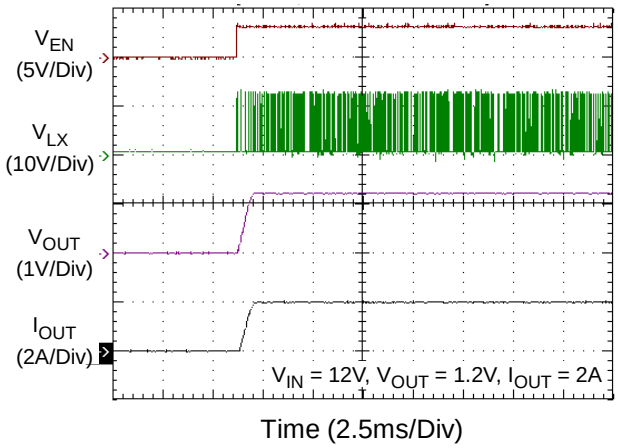
Power On from Input Voltage



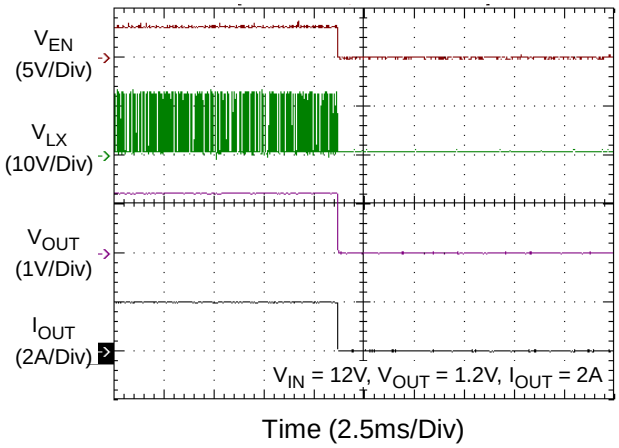
Power Off from Input Voltage



Power On from Enable



Power Off from Enable



Application Information

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) typically 40% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level or the IC may not be able to meet the desired output current. If needed, reduce the inductor ripple current (ΔI_L) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Considering the Typical Operating Circuit for 1.8V output at 2A and an input voltage of 12V, using an inductor ripple of 0.8A (40%), the calculated inductance value is :

$$L = \frac{1.8 \times (12 - 1.8)}{12 \times 800kHz \times 0.8A} = 2.4\mu H$$

The ripple current was selected at 0.8A and, as long as we use the calculated 2.4μH inductance, that should be the actual ripple current amount. The ripple current and required peak current as below :

$$\Delta I_L = \frac{1.8 \times (12 - 1.8)}{12 \times 800kHz \times 2.4\mu H} = 0.8A$$

$$\text{and } I_{L(PEAK)} = 2A + \frac{0.8A}{2} = 2.4A$$

For the 2.4μH value, the inductor's saturation and thermal rating should exceed at least 2.4A. For more conservative, the rating for inductor saturation current must be equal to or greater than switch current limit of the device rather than the inductor peak current.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current (I_{RMS}) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT6212C/D input which could potentially cause large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT6212C/D are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.8V output and an inductor ripple of 0.8A, with 1 x 22μF output capacitance each with about 5mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 0.8A \times 5m\Omega = 4mV$$

$$V_{RIPPLE(C)} = \frac{0.8A}{8 \times 22\mu F \times 800kHz} = 5.68mV$$

$$V_{RIPPLE} = 4mV + 5.68mV = 9.68mV$$

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small.

However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 800kHz switching frequency.

But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

For the Typical Operating Circuit for 1.8V output, the circuit has an inductor 2.4μH and 1 x 22μF output capacitance with 5mΩ ESR each. The ESR step is 2A x 5mΩ = 10mV which is small, as expected. The output voltage sag and soar in response to full 0A-2A-0A instantaneous transients are :

$$t_{ON} = \frac{1.8V}{12V \times 800kHz} = 187ns$$

$$\text{and } D_{MAX} = \frac{187ns}{187ns + 240ns} = 0.44$$

where 240ns is the minimum off time.

$$V_{SAG} = \frac{2.4\mu H \times (2A)^2}{2 \times 22\mu F \times (12V \times 0.44 - 1.8V)} = 63mV$$

$$V_{SOAR} = \frac{2.4\mu H \times (2A)^2}{2 \times 22\mu F \times 1.8V} = 121mV$$

The sag is about 3.5% of the output voltage and the soar is a full 6.7% of the output voltage. The ESR step is negligible here but it does partially add to the soar, so keep that in mind whenever using higher-ESR output capacitors.

The soar is typically much worse than the sag in high input, low-output step-down converters because the high input voltage demands a large inductor value which stores lots of energy that is all transferred into the output if the load stops drawing current. Also, for a given inductor, the soar for a low output voltage is a greater voltage change and an even greater percentage of the output voltage.

Any sag is always short-lived, since the circuit quickly sources current to regain regulation in only a few switching cycles. With the RT6212D, any overshoot transient is typically also short-lived since the converter will sink current, reversing the inductor current sharply until the output reaches regulation again. The RT6212C discontinuous operation at light loads prevents sinking current so, for that IC, the output voltage will soar until load current or leakage brings the voltage down to normal.

Most applications never experience instantaneous full load steps and the RT6212C/D high switching frequency and fast transient response can easily control voltage regulation at all times. Also, since the sag and soar both are proportional to the square of the load change, if load steps were reduced to 1A (from the 2A examples preceding) the voltage changes would be reduced by a factor of almost ten. For these reasons sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, always calculate soar to make sure that over-voltage protection will not be triggered. Under-voltage is not likely since the threshold is very low (50%), that function has a long delay (5μs), and the IC will quickly

return the output to regulation. Over-voltage protection has a minimum threshold of 125% and short delay of 10μs and can actually be triggered by incorrect component choices, particularly for the RT6212C which does not sink current.

Feed-Forward Capacitor (C_{FF})

The RT6212C/D are optimized for ceramic output capacitors and for low duty cycle applications. However for high-output voltages, with high feedback attenuation, the circuit's response becomes over-damped and transient response can be slowed. In high-output voltage circuits (V_{OUT} > 1.8V) transient response is improved by adding a small "feed-forward" capacitor (C_{FF}) across the upper FB divider resistor (Figure 1), to increase the circuit's Q and reduce damping to speed up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value that following below step.

- Get the BW the quickest method to do transient response form no load to full load. Confirm the damping frequency. The damping frequency is BW.

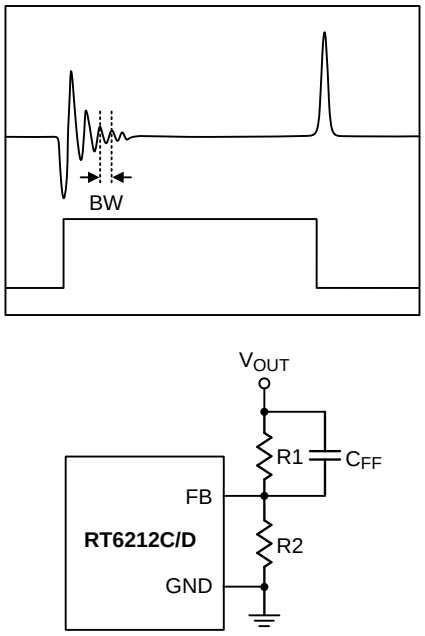


Figure 1. C_{FF} Capacitor Setting

- C_{FF} can be calculated base on below equation :

$$C_{FF} = \frac{1}{2 \times 3.1412 \times R1 \times BW \times 0.8}$$

Enable Operation (EN)

For automatic start-up the low-voltage EN pin can be connected to VIN through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to VIN by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins (1.5V, typical).

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 3). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 4).

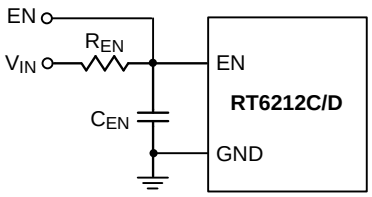


Figure 2. External Timing Control

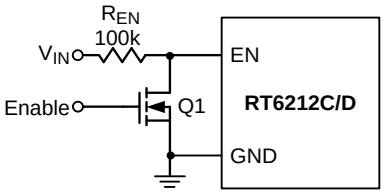


Figure 3. Digital Enable Control Circuit

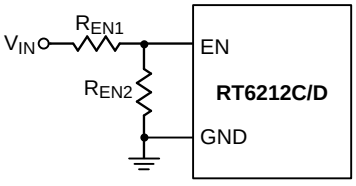


Figure 4. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected

to FB. The output voltage is set according to the following equation :

V_{OUT} = 0.8V x (1 + R1 / R2)

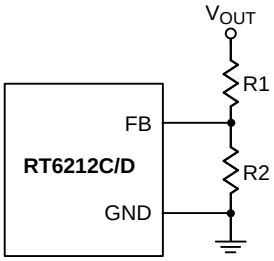


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{LX} rises rapidly. During switch turn-off, LX is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{LX}'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in Figure 6 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

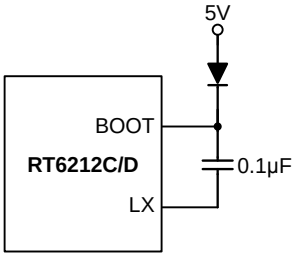


Figure 6. External Bootstrap Diode

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For TSOT-23-6 (FC) package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for a TSOT-23-6 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

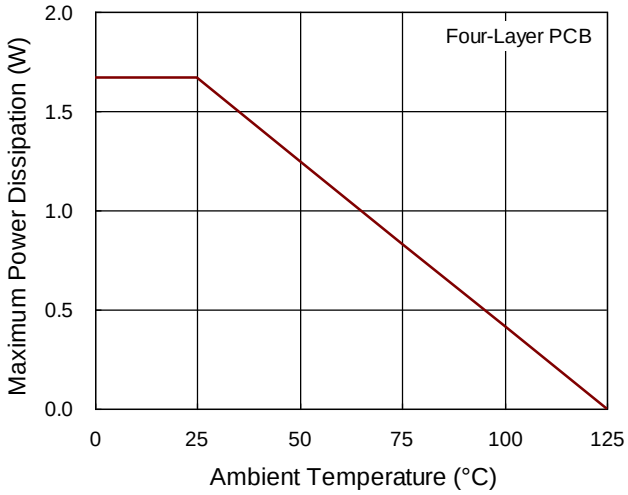


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT6212C/D.
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

An example of PCB layout guide is shown from Figure 8.

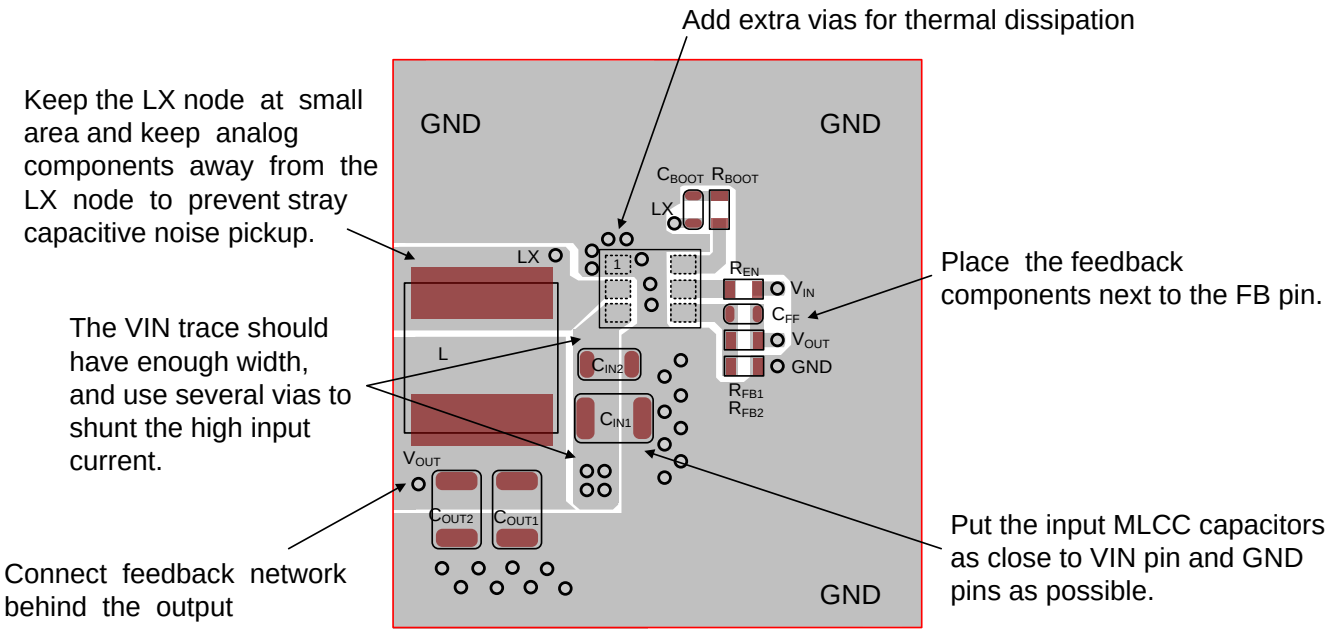
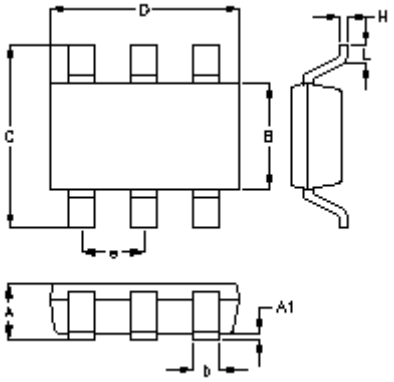


Figure 8. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.950		0.037	
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-6 (FC) Surface Mount Package

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