USB-C Protection Solutions for Signal Path, CC OVP Switch, VCONN Switch, SBU OVP 1:2 Switch and USB2.0 Switch with BC12 and Charging Port Configuration

General Description

The RT1737 is a highly integrated USB-C Protection IC which includes IEC-61000-4-2 ESD protection cell for SBU/DP/DM. The RT1737 integrates high voltage protection switches for DP/DM/SBU1/SBU2/CC1/CC2 to prevent high voltage VBUS from touching the adjacent pins. The AMR of DPDM/SBU/CC OVP switches is 28V. High Voltage USB 2.0 Switches also support SDP/DCP/CDP configuration.

The RT1737 also integrates SBU 1:2 OVP Mux for specific application like debugging mode, factory mode, etc.

VCONN Switch with OVP/OCP/RVP/RCP/UVP protection is also integrated. The RPD_CC1/CC2 pins function as the Rd pin in dead-battery mode and are independent of CC1/CC2, which provides each customer system with flexibility.

The RT1737 is available in a WQFN-32L 5x5 package.

Ordering Information

RT1737□□

- Package Type
  QW: WQFN-32L 5x5 (W-Type)
- Lead Plating System
  G: Green (Halogen Free and Pb Free)

Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

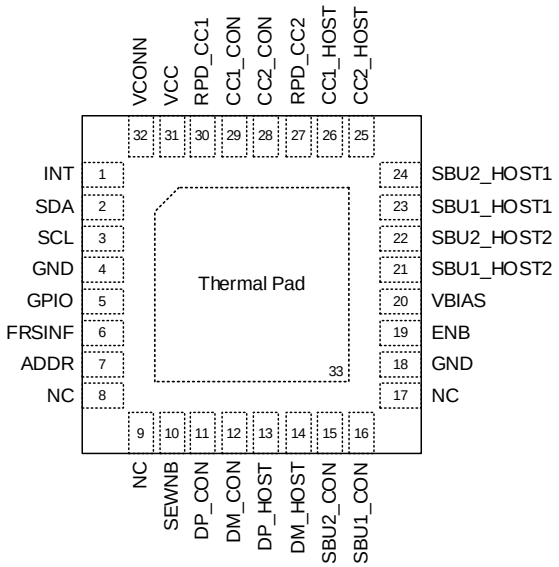
- **6-Channel of short to VBUS Overvoltage Protection (CC1_CON, CC2_CON, SBU1_CON, SBU2_CON, DP_CON and DM_CON)**
- **60ns Ultra-Fast OVP Response Time of DP/DM/CC/SBU**
- **High Absolute Maximum Ratings = 28V of CC1_CON, CC2_CON, SBU1_CON, SBU2_CON, DP_CON, DM_CON**
- **DP/DM USB2.0 Switch with 3dB BW of 800MHz, High Voltage of 21V Protection and Supports Charging Port Controller for SINK and SRC Port (BC1.2)**
- **SBU OVP with 1:2 Mux Selectable**
- **4-State ADDR pin for Multiport Application**
- **Dead Battery Mode Support**
- **VCONN Switch Integrated with OVP/OCP/RCP/UVP/RVP Protection**
- **IEC61000-4-2 Contact Discharge Protection**
  - **DP_CON/DM_CON: ±8kV**
  - **SBU1_CON/SBU2_CON: ±8kV**

Applications

- Desktop, Notebook, PC
- USB Hub/Dongle
- TV/Monitor
- Server/Data Center

Pin Configuration

(TOP VIEW)

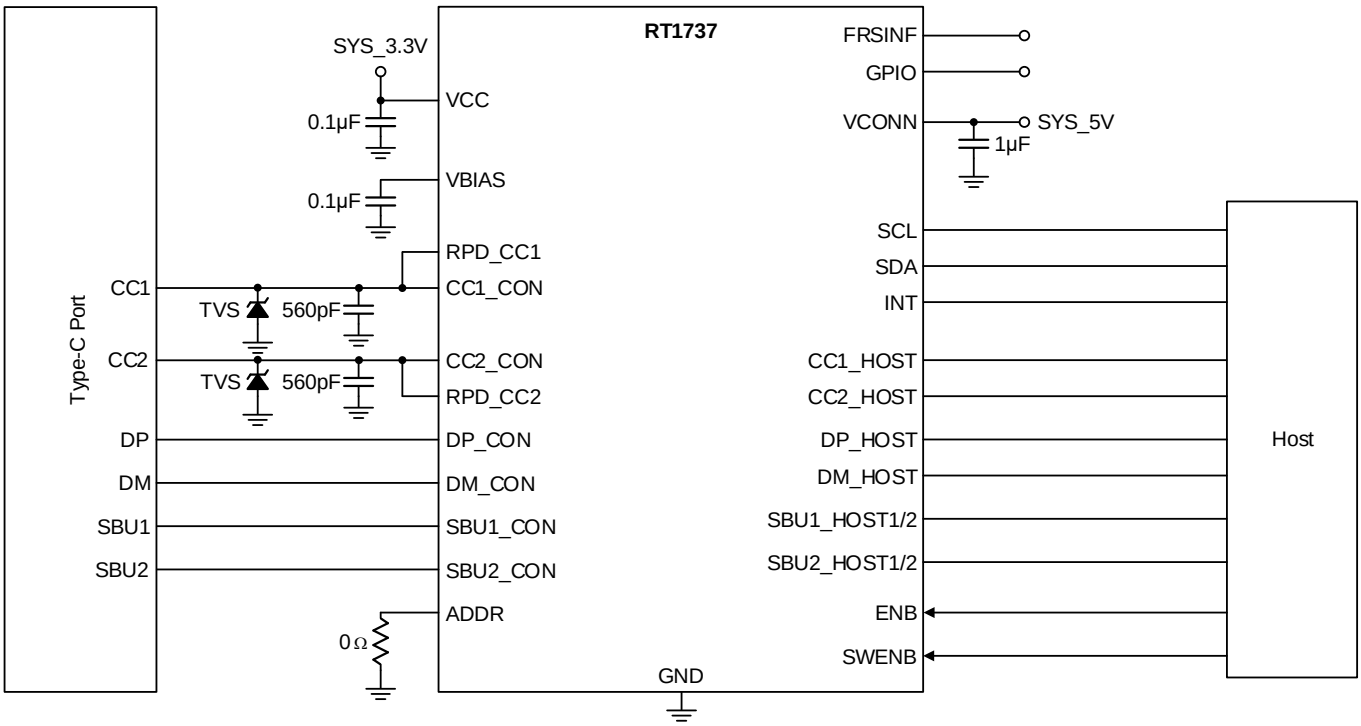


WQFN-32L 5x5

Marking Information

RT1737GQW: Product Code
YMDNN: Date Code

Simplified Application Circuit

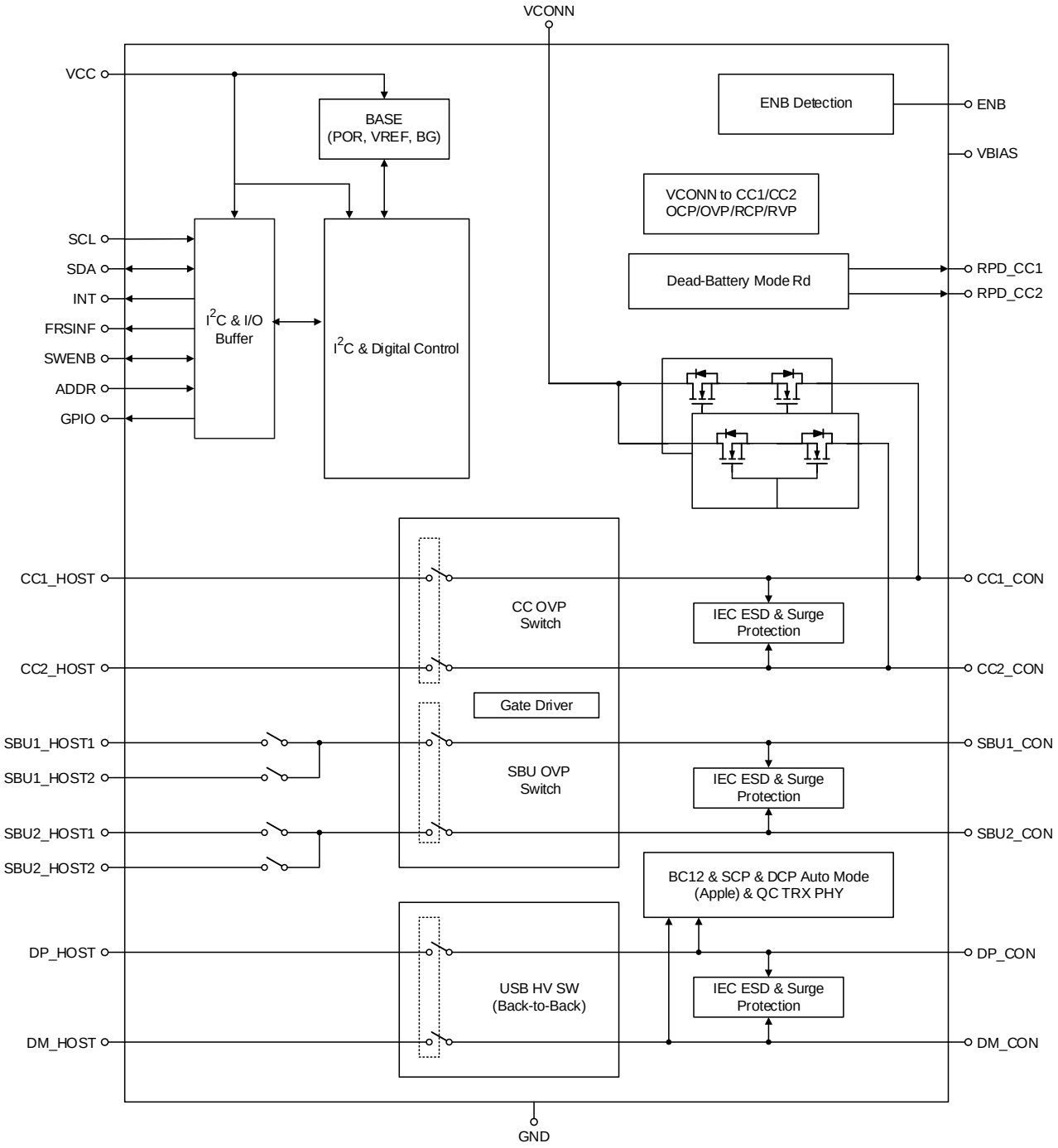


Functional Pin Description

Pin No.	Pin Name	Pin Function
1	INT	Open drain output; I^2C interrupt and chip alert.
2	SDA	I^2C serial data input/output. Open-drain. An external pull-up resistor is required.
3	SCL	I^2C interface serial clock input. Open-drain. An external pull-up resistor is required.
4, 18	GND	Ground. The exposed pad must be connected and well soldered to a large GND.
5	GPIO	Configurable GPIO with open-drain or push-pull type, used as power switch control for FRS setting.
6	FRSINF	GPIO output pin for informing buck-boost chip to supply 5V for FRS event.
7	ADDR	Address selection node when used with multiple Type-C ports.
8, 9, 17	NC	No internal connection. Connect to ground.
10	SWENB	GPIO input pin for turning on the force CC and SBU switches. The pin is initially floating, and when it is pulled low, the switch turns on. Pulling the pin high has no effect on the switch.
11	DP_CON	Type-C connector side DP switch. Connect DP pin of the USB Type-C connector.
12	DM_CON	Type-C connector side DM switch. Connect DM pin of the USB Type-C connector.
13	DP_HOST	System side of the DP switch. Connect to DP pin of the USB connector.
14	DM_HOST	System side of the DM switch. Connect to DM pin of the USB connector.
15	SBU2_CON	Type-C connector side SBU2 switch. Connect SBU2 pin of the USB Type-C connector.
16	SBU1_CON	Type-C connector side SBU1 switch. Connect SBU1 pin of the USB Type-C connector.
19	ENB	GPIO input pin for the force chip in shipping mode for the lowest quiescent. Initial pull low, high active.
20	VBIAS	VBIAS pin connecting capacitor for ESD protection. Put a 0.1μF capacitor on this pin to ground.
21	SBU1_HOST2	System side of the SBU1 switch. Connect to SBU pin of the SBU MUX2.
22	SBU2_HOST2	System side of the SBU2 switch. Connect to SBU pin of the SBU MUX2.
23	SBU1_HOST1	System side of the SBU1 switch. Connect to SBU pin of the SBU MUX1.
24	SBU2_HOST1	System side of the SBU2 switch. Connect to SBU pin of the SBU MUX1.
25	CC2_HOST	System side of the CC2 switch. Connect to CC pin of the CC/PD controller.
26	CC1_HOST	System side of the CC1 switch. Connect to CC pin of the CC/PD controller.
27	RPD_CC2	If dead battery resistors are required, short pin to CC2_CON. If dead battery resistors are not required, short pin to GND.
28	CC2_CON	Type-C connector side CC2 switch. Connect CC2 pin of the USB Type-C connector.
29	CC1_CON	Type-C connector side CC1 switch. Connect CC1 pin of the USB Type-C connector.
30	RPD_CC1	If dead battery resistors are required, short pin to CC1_CON. If dead battery resistors are not required, short pin to GND.
31	VCC	Main power input for the RT1737.

Pin No.	Pin Name	Pin Function
32	VCONN	Regulated power input pin to output VCONN through CC pin for Type-C full-featured cables and other accessories. If the type c port does not support VCONN power, connect this pin to GND with 10kΩ resister.
33	Thermal Pad	Used as a heatsink. Thermal pad connect to PCB ground plane.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- CC1_CON, CC2_CON, SBU1_CON, SBU2_CON, DP_CON, DM_CON ---------- –0.3V to 28V
- RPD_CC1, RPD_CC2, VBIAS ---------- –0.3V to 28V
- CC1_HOST, CC2_HOST, SBU1_HOST1, SBU2_HOST1, SBU1_HOST2, SBU2_HOST2, DP_HOST, DM_HOST ---------- –0.3V to 6V
- VCC, VCONN, SDA, SCL, INT, ADDR, FRSINF, ENB, SWENB, GPIO ---------- –0.3V to 6V
- Output Current (VCONN to CC1_CON/CC2_CON) ---------- 0A to 0.8A
- Output Current (CC1_CON/CC2_CON/CC1_HOST/CC2_HOST) ---------- –100mA to 100mA
- Output Current (SBU1_CON/SBU2_CON/SBU1_HOST1/ SBU2_HOST1/SBU1_HOST2/SBU2_HOST2) ---------- –100mA to 100mA
- Output Current (DP_CON/DM_CON/DP_HOST/DM_HOST) ---------- –100mA to 100mA
- Power Dissipation, P_D @ T_A = 25°C
- WQFN-32L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)
- WQFN-32L 5x5, θ_{JA} ---------- 27.5°C/W
- WQFN-32L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- ±2kV
  DP_CON, DM_CON, SBU1_CON, SBU2_CON,
  (IEC 61000-4-2 Contact Discharge) ---------- ±8kV
  DP_CON, DM_CON, SBU1_CON, SBU2_CON,
  (IEC 61000-4-2 Air Discharge) ---------- ±15kV
  DP_CON, DM_CON, CC1_CON, CC2_CON, SBU1_CON, SBU2_CON
  (IEC 61000-4-5 Surge) ---------- ±28V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VCC ---------- 3V to 5.5V
- VCONN Supply Voltage ---------- 3V to 5.5V
- VCONN Supply Current ---------- 200mA to 700mA
- I/O Voltage CC1_CON/CC2_CON/RPD_CC1/RPD_CC2 ---------- 0V to 5.5V
- I/O Voltage CC1_HOST/CC2_HOST ---------- 0V to 4.2V
- I/O Voltage DP_CON/DM_CON/DP_HOST/DM_HOST ---------- 0V to 4.2V
- I/O Voltage SBU1_CON/SBU2_CON/SBU1_HOST/SBU2_HOST ---------- 0V to 4.2V
- I/O Voltage SDA, SCL, INT, ADDR, FRSINF, ENB, SWENB, GPIO ---------- 0V to 3.6V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(VCC = 3V to 5.5V, V_{CC} (Typ.) = 3.3V, T_A = –40°C to 85°C and T_A (Typ.) = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Current						
Quiescent Current - Shutdown Mode	Ishutdown_VCC	Shutdown current for VCC = 3.3V, ENB = High, SWENB = High	--	1.8	4	μA
Quiescent Current - Shipping Mode	I_Shipping mode_ VCC_DataSwitchOn	VCC = 3V to 5.5V, ENB = Low, SWENB = Low, CC/SBU CON-HOST switch on, DPDM switch off	100	175	240	μA
Quiescent Current - Shipping Mode	I_Shipping mode_ VCC_DataSwitchOff	VCC = 3V to 5.5V, ENB = Low, SWENB = High, CC/SBU/DPDM switch all off	12	26	42	μA
Quiescent Current - Normal Mode	I_Normalmode_VCC _DataSwitchOn_Vco nnOn	VCC = 3V to 5.5V, ENB = Low, SWENB = High, CCx_CON-HOST switch on, CCx_CON-VCONN switch on, SBUx_CON-HOST switch on, DPDM_CON-HOST switch on	250	350	435	μA
Quiescent Current - CC Toggle Mode	I_CCtoggleMode VCC	VCC = 3V to 5.5V, ENB = Low, SWENB = High, CCx_CON-HOST Switch On, SBUx_CON-HOST switch off, DPDM_CON-HOST switch off	40	70	90	μA
UVLO						
UVLO for VCC	VCC_{UVLO}	VCC falling	-	-	1.8	V
VCONN Switch						
VCONN OVP	V_{CONN_OVP}		5.6	5.8	6	V
Hysteresis on VCONN OVP	$V_{CONN\_OVP\_HYS}$		--	60	--	mV
VCONN Undervoltage Threshold	V_{CONN_UVT}		2.4	2.7	3	V
Hysteresis on VCONN UV	$V_{CONN\_UVT\_HYS}$		50	100	150	mV
VCONN RVP1	V_{CONN_RVP1}		0.15	0.3	0.55	V
VCONN RVP2	V_{CONN_RVP2}		0.25	0.5	0.75	V
VCONN OCP Range (Shutdown)	$V_{CONN\_OCP\_range}$		200	--	700	mA
VCONN OCP Range_200mA	$I_{OCP\_Range\_200mA}$	OCP setting = 200mA	125	200	285	mA
VCONN OCP Range_300mA	$I_{OCP\_Range\_300mA}$	OCP setting = 300mA	240	300	360	mA
VCONN OCP Range_400mA	$I_{OCP\_Range\_400mA}$	OCP setting = 400mA	320	400	530	mA
VCONN OCP Range_500mA	$I_{OCP\_Range\_500mA}$	OCP setting = 500mA	400	500	600	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCONN OCP Range_600mA	$I_{OCP\_Range\_600mA}$	OCP setting = 600mA	480	600	720	mA
VCONN OCP Range_700mA	$I_{OCP\_Range\_700mA}$	OCP setting = 700mA	560	700	840	mA
Ron for VCONN Switch	V_{CONN_Ron}	VCC = 3V to 5.5V, I_{SW} = 100 to 700mA	--	0.3	0.4	Ω
VCONN RCP Range	$V_{CONN\_RCP\_range}$		50	--	300	mA
CC Switch						
On Leakage Current of CC Switch	$I_{ON\_CCx\_CON\_3.6V}$	VCC = 3 to 5.5V, CCx_CON = 0V to 3.6V, CCx_HOST is floating, RPD_CC1 & RPD_CC2 connect to CC1_CON & CC2_CON	–5	--	5	μA
Off Leakage Current of CCx_CON	$I_{ON\_CCx\_CON\_3.6V}$	VCC = 3 to 5.5V, CCx_CON = 3.6V, RPD_CC1 & RPD_CC2 not connect to CC1_CON & CC2_CON	–5	--	5	μA
Off Leakage Current of CCx_CON	$I_{OZ\_CCx\_CON\_24V}$	VCC = 3 to 5.5V, CCx_CON = 24V, RPD_CC1 & RPD_CC2 connect to CC1_CON & CC2_CON	--	9	12	mA
Power−Off Leakage Current CCx_CON	$I_{OFF\_CCx\_CON\_3.6V}$	VCC = 0V, CCx_CON = 3.6V, RPD_CC1 & RPD_CC2 not connect to CC1_CON & CC2_CON	–5	--	5	μA
On Leakage Current of CCx_HOST	$I_{ON\_CCx\_HOST\_3.6V}$	VCC = 3 to 5.5V = 3.3V, CCx_HOST = 0V to 3.6V, RPD_CC1 & RPD_CC2 connect to CC1_CON & CC2_CON	–5	--	5	μA
Off Leakage of CCx_HOST	$I_{OZ\_CCx\_HOST\_3.6V}$	VCC = 3 to 5.5V, CCx_HOST = 0V to 3.6V, RPD_CC1 & RPD_CC2 not connect to CC1_CON & CC2_CON	–5	--	5	μA
Power−Off Leakage Current CCx_HOST	$I_{OFF\_CCx\_HOST\_3.6V}$	VCC = 0V, CCx_HOST = 0V to 3.6V, RPD_CC1 & RPD_CC2 not connect to CC1_CON & CC2_CON	–1	--	1	μA
Off Leakage Current of CCx_CON to CC_HOST	$I_{OFF\_CCx\_CON\_24V}$ to CCx_HOST	VCC = 0V or 3 to 5.5V CCx_CON = 24V CCx_HOST pins are set to 0V, measure leakage out of CCx_HOST pins	–1	--	1	μA
CC Input OVP Lockout 5.8V	$V_{OV\_SBU\_TRIP\_5V8}$	Rising edge	5.6	5.8	6	V
CC Input OVP Lockout 3.8V	$V_{OV\_SBU\_TRIP\_3V8}$	Rising edge	3.7	3.8	3.9	V
CC Input OVP Lockout 3.6V	$V_{OV\_SBU\_TRIP\_3V6}$	Rising edge	3.5	3.6	3.7	V
CC Input OVP Hysteresis	$V_{OV\_CC\_HYS}$		--	60	--	mV
CCx_HOST Switch On Resistance	R_{ON_CC}	VCC = 3V to 5.5V, V_{SW} = 0V to 3.6V, I_{SW} = 30mA	--	6	9	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CC On Resistance Flatness	$R_{ON(FLAT)\_CC}$	Sweep CCx_CON voltage between 0V and 1.2V. I_{SW} = 30 mA. –40°C ≤ T_J ≤ 85°C	--	--	0.2	Ω
CCx_HOST Switch Turn-On Time	t_{ON_CC}	CCx_CON = 2.5V, RL = 1kΩ	150	250	400	μs
CCx_HOST Switch Turn-Off Time	t_{OFF_CC}	CCx_CON = 2.5V, RL = 1kΩ	--	--	1	μs
Threshold Voltage of the Pull-Down Switch in Series with Rd during Dead Battery	V_{TH_DB}	External 80μA	0.25	--	1.5	V
		External 180μA	0.45	--	1.5	V
		External 330μA	0.85	--	2.45	V
–3dB Bandwidth	BW_CC	Test power 0dBm, single ended, 50Ω terminal	--	50	--	MHz
CC Pins OVP Response Time	$t_{OVP\_CC\_1}$	Hot-Plug CCx_CON with a 1 meter USB Type-C cable. Hot-Plug voltage CCx_CON = 0V to 24V. VCC = 3.3V. Put a 30Ω resistor to GND on CCx_HOST, time OVP Thre to CCx_HOST 0V, CC_OVP_SEL set 3.6V or 3.8V	--	60	120	ns
CC Pins OVP Response Time	$t_{OVP\_CC\_2}$	Hot-Plug CCx_CON with a 1 meter USB Type-C cable. Hot-Plug voltage CCx_CON = 0V to 24V. VCC = 3.3V. Put a 30Ω resistor to GND on CCx_HOST, time OVP Thre to CCx_HOST 0V, CC_OVP_SEL set 5.8V	--	80	120	ns
Short-to-VBUS System-Side Clamping Voltage on the CCx_HOST Pins	$V_{STBUS\_CCx\_HOST\_CLAMP}$	Hot-Plug CCx_CON with a 1 meter USB Type-C cable. Hot-Plug voltage CCx_CON = 0 to 24V. VCC = 3 to 5.5V. Put a 30Ω resistor to GND on CCx_HOST	--	7	8.5	V
SBU Switch						
On Leakage Current of SBU Switch	$I_{ON\_SBUx\_CON\_3.6V}$	VCC = 3 to 5.5V, SBUx_CON = 0V to 3.6V, SBUx_HOST is floating	–3	--	3	μA
Off Leakage Current of SBUx_CON	$I_{OZ\_SBUx\_CON\_3.6V}$	VCC = 3 to 5.5V, SBUx_CON = 3.6V	–3	--	3	μA
Off Leakage Current of SBUx_CON	$I_{OZ\_SBUx\_CON\_24V}$	VCC = 3 to 5.5V, SBUx_CON = 24V	--	--	800	μA
Power−Off Leakage Current SBUx_CON	$I_{OFF\_SBUx\_CON\_3.6V}$	VCC = 0V, SBUx_CON = 3.6V	–3	--	3	μA
On Leakage Current of SBUx_HOST	$I_{ON\_SBUx\_HOST\_3.6V}$	VCC = 3 to 5.5V, SBUx_HOST = 0V to 3.6V	–3	--	3	μA
Off Leakage of SBUx_HOST	$I_{OZ\_SBUx\_HOST\_3.6V}$	VCC = 3 to 5.5V, SBUx_HOST = 0V to 3.6V	–3	--	3	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Leakage Current of SBUx_CON to SBUx_HOST	$I_{OFF\_SBUx\_CON\_24V\ to\ SBUx\_HOST}$	VCC = 0V or 3 to 5.5V SBUx_CON = 24V SBUx_HOST pins are set to 0V, measure leakage out of SBUx_HOST pins	–1	--	1	μA
SBU Input OVP Lockout 4.5V	$V_{OV\_SBU\_TRIP\_4V5}$	Rising edge	--	4.5	--	V
SBU Input OVP Lockout 3.8V	$V_{OV\_SBU\_TRIP\_3V8}$	Rising edge	--	3.8	--	V
SBU Input OVP Lockout 3.7V	$V_{OV\_SBU\_TRIP\_3V7}$	Rising edge	--	3.7	--	V
SBU Input OVP Lockout 3.6V	$V_{OV\_SBU\_TRIP\_3V6}$	Rising edge	--	3.6	--	V
SBU Input OVP Hysteresis	$V_{OV\_SBU\_HYS}$		--	60	--	mV
SBUx_HOST Switch On Resistance	R_{ON_SBU}	V_{SW} = 0V to 3.6V, I_{SW} = 30mA	--	6	9	Ω
SBU On Resistance Flatness	$R_{ON(FLAT)\_SBU}$	Sweep SBUx voltage between 0V and 3.6V. I_{SW} = 30 mA. –40°C ≤ T_J ≤ 85°C	--	--	0.15	Ω
SBUx_HOST Switch Turn-On Time	t_{ON_SBU}	SBUx_CON = 2.5V, RL = 1kΩ	50	100	200	μs
SBUx_HOST Switch Turn-Off Time	t_{OFF_SBU}	SBUx_CON = 2.5V, RL = 1kΩ	--	--	1	μs
–3dB Bandwidth	BW_{SBU}	Test power 0dBm, Single ended, 50Ω terminal	200	--	--	MHz
Crosstalk for SBU	X_{talk_SBU}	Measure crosstalk at f = 1 MHz from SBU1_HOST to SBU2_CON or SBU2_HOST to SBU1_CON. Vcm1 = 3.6V, Vcm2 = 0.3V. Be sure to terminate open sides to 50Ω	--	–80	--	dB
Off Isolation between SBU1_HOST, SBU2_HOST to SBU1_CON/SBU2_CON	OIRR_SBU	Test power 0dBm at 1kHz, measure the SBU1_CON to SBU1_HOST or SBU2_CON to SBU2_HOST with 50Ω terminal	--	–100	–90	dB
SBU Pins OVP Response Time	t_{OVP_SBU}	Hot-Plug SBUx_CON with a 1 meter USB Type-C cable. Hot-Plug voltage SBUx_CON = 0 to 24V. VCC = 3 to 5.5V. Put a 100nF capacitor in series with a 40Ω resistor to GND on SBUx_HOST, time OVP Thre to SBUx_HOST 0V	--	60	120	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Short-to-VBUS System-Side Clamping Voltage on the SBUx_HOST Pins	$V_{STBUS\_SBUHOST\_CLAMP}$	Hot-Plug SBUx_CON with a 1 meter USB Type-C cable. Hot-Plug voltage SBUx_CON = 0V to 24V. VCC = 3 to 5.5V. Put a 100nF capacitor in series with a 40Ω resistor to GND on SBUx_HOST	--	7	8.5	V
DP/DM Switch						
On Leakage Current of USB Switch	$I_{ON\_CON\_USB\_3.6V}$	VCC = 3 to 5.5V, DM_CON, DP_CON = 0V to 3.6V, DP_HOST and DM_HOST = float	–3	--	3	µA
Off Leakage Current of DP_CON and DM_CON	$I_{OZ\_CON\_USB\_3.6V}$	VCC = 3 to 5.5V, DM_CON and DP_CON = 3.6V	–3	--	3	µA
Off Leakage Current of DP_CON and DM_CON	$I_{OZ\_CON\_USB\_24V}$	VCC = 3 to 5.5V, DM_CON and DP_CON = 24V	--	--	800	µA
Power−Off Leakage Current of DP_CON and DM_CON	$I_{OFF\_CON\_USB\_3.6V}$	VCC = 0V, DM_CON and DP_CON = 3.6V	–3	--	3	µA
On Leakage Current of DP_HOST and DM_HOST	$I_{ON\_USB\_HOST\_3.6V}$	VCC = 3 to 5.5V, DP_HOST and DM_HOST = 0V to 3.6V	–3	--	3	µA
Off Leakage Current of DP_HOST and DM_HOST	$I_{OZ\_USB\_HOST\_3.6V}$	VCC = 3 to 5.5V, DM_HOST and DP_HOST = 0V to 3.6V	–3	--	3	µA
Off Leakage Current of CON_USB to USB_HOST	$I_{OFF\_CON\_USB\_24V\ to\ USB\_HOST}$	VCC = 0V or 3 to 5.5V, DP_CON & DM_CON = 24V DP_HOST and DM_HOST pins are set to 0V, measure leakage out of DP_HOST & DM_HOST pins	–1	--	1	µA
USB Input OVP Lockout	$V_{OV\_USB\_TRIP}$	Rising edge	--	4.5	--	V
USB Input OVP Hysteresis	$V_{OV\_USB\_HYS}$		--	60	--	mV
USB Switch On Resistance	R_{ON_USB}	VCC =3V to 5.5V, V_{SW} = 0V to 3.6V, I_{SW} = 8mA	--	6	9	Ω
USB On Resistance Flatness	$R_{ON(FLAT)\_USB}$	Sweep USB voltage between 0V and 3.6V. I_{SW} = 8mA. –40°C ≤ T_J ≤ 85°C	--	--	0.15	Ω
USB Switch Turn−On Time	t_{ON_USB}	DP_CON = DM_CON = 1.5V, RL = 1kΩ	50	100	200	µs
USB Switch Turn−Off Time	t_{OFF_USB}	DP_CON = DM_CON = 1.5V, RL = 1kΩ	--	--	1	µs
−3dB Bandwidth for USB	BW_{USB}	Test power 0dBm, Single ended, 50Ω terminal	700	800	--	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Crosstalk for USB	X_{talk_USB}	Swing 1VPP at 1MHz, measure the DP_HOST to DM_CON or DM_HOST to DP_CON with 50Ω terminal	--	−80	--	dB
Off Isolation between DP_HOST, DM_HOST and Com-mon Node Pins	OIRR_USB	Test power 0dBm at 1kHz, measure the DP_CON to DP_HOST or DM_CON to DM_HOST with 50Ω terminal	--	−100	--	dB
DP and DM Pins OVP Response Time	t_{OVP_USB}	Hot-Plug DP/DM_CON with a 1 meter USB Type-C cable. Hot-Plug voltage DP/DM_CON = 0V to 24V. VCC = 3 to 5.5V. Put a 100nF capacitor in series with a 40Ω resistor to GND on DP/DM_HOST, time OVP Thre to DP/DM_HOST 0V	--	60	120	ns
Short-to-VBUS System-Side Clamping VSB_HOST Pins	$V_{STBUS\_USB\_HOST\_CLAMP}$	Hot-Plug DP/DM_CON with a 1 meter USB Type-C cable. Hot-Plug voltage DP/DM_CON = 0 to 24 V. VCC = 3 to 5.5V. Put a 100nF capacitor in series with a 40Ω resistor to GND or High-Z to GND on DP/DM_HOST	--	7	8.5	V
DP/DM Detection						
DP Source Voltage	V_{DP_SRC}		0.5	0.6	0.7	V
DM Source Voltage	V_{DM_SRC}		0.5	0.6	0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
Logic Threshold Voltage	V_{LGC_CHG}		0.8	--	2	V
DP Sink Current	I_{DP_SINK}		50	100	150	μA
DM Sink Current	I_{DM_SINK}		50	100	150	μA
Data Contract Detect Current Source	I_{DP_SRC}		7	10	13	μA
Dedicated Charging Port Resistance Across DP/DM	R_{DCP_DAT}		--	--	200	Ω
DP Pull-Down Resistance	R_{DP_DWN}		14.25	20	24.8	kΩ
DM Pull-Down Resistance	R_{DM_DWN}		14.25	20	24.8	kΩ
DP Source On Time	$t_{DP\_SRC\_ON}$		40	64	80	ms
DM Source On Time	$t_{DM\_SRC\_ON}$		40	64	80	ms
DCD Timeout	$t_{DCD\_TIMEOUT}$		300	600	900	ms
Over-Temperature Protection						
Over-Temperature Protection Shutdown Threshold Rising	T_{OPT}	VCC = 3.3V	140	150	160	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Protection Shutdown Threshold Falling	$T_{OPT\_RECOVER}$	VCC = 3.3V	95	110	125	°C
INT						
INT Low-Level Output Voltage	V_{INT_OL}	I_{INT_OL} = 4mA	--	--	0.4	V
ENB						
ENB High-Level Input Voltage	V_{IH_ENB}		1.4	--	--	V
ENB Low-Level Input Voltage	V_{IL_ENB}		--	--	0.4	V
SWENB						
SWENB High-Level Input Voltage	V_{IH_SWEN}		1.3	--	--	V
SWENB Low-Level Input Voltage	V_{IL_SWEN}		--	--	0.45	V
FRSINF						
FRSINF High-Level Output Voltage	V_{OH_FRSINF}		1.5	--	--	V
FRSINF Low-Level Output Voltage	V_{OL_FRSINF}		--	--	0.3	V
FRSINF High-Level Leakage Current	I_{OH_FRSINF}		--	--	1	μA
I^2C						
Low-Level Input Voltage	V_{IL}	VCC = 3V to 5.5V	--	--	0.4	V
High-Level Input Voltage	V_{IH}	VCC = 3V to 5.5V	1.2	--	--	V
Low-Level Output Voltage	V_{OL}	VCC = 3V to 5.5V, open-drain	--	--	0.4	V
Input Current each IO Pin	I_I	VCC = 3V to 5.5V 0.1 VCC < V_I < 0.9 VCC_{MAX}	−10	--	10	μA
SCL Clock Frequency	f_{SCL}	VCC = 3V to 5.5V	100	--	3400	kHz
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	VCC = 3V to 5.5V	--	--	50	ns
Data Hold Time	$t_{HD:DAT}$	VCC = 3V to 5.5V	30	--	--	ns
Data Set-Up Time	$t_{SU:DAT}$	VCC = 3V to 5.5V	70	--	--	ns
Address1	address1(7bit)0x70		--	0	--	kΩ
Address2	address2(7bit)0x71		--	310	--	kΩ
Address3	address3(7bit)0x72		--	620	--	kΩ
Address4	address4(7bit)0x73		--	Open	--	kΩ

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

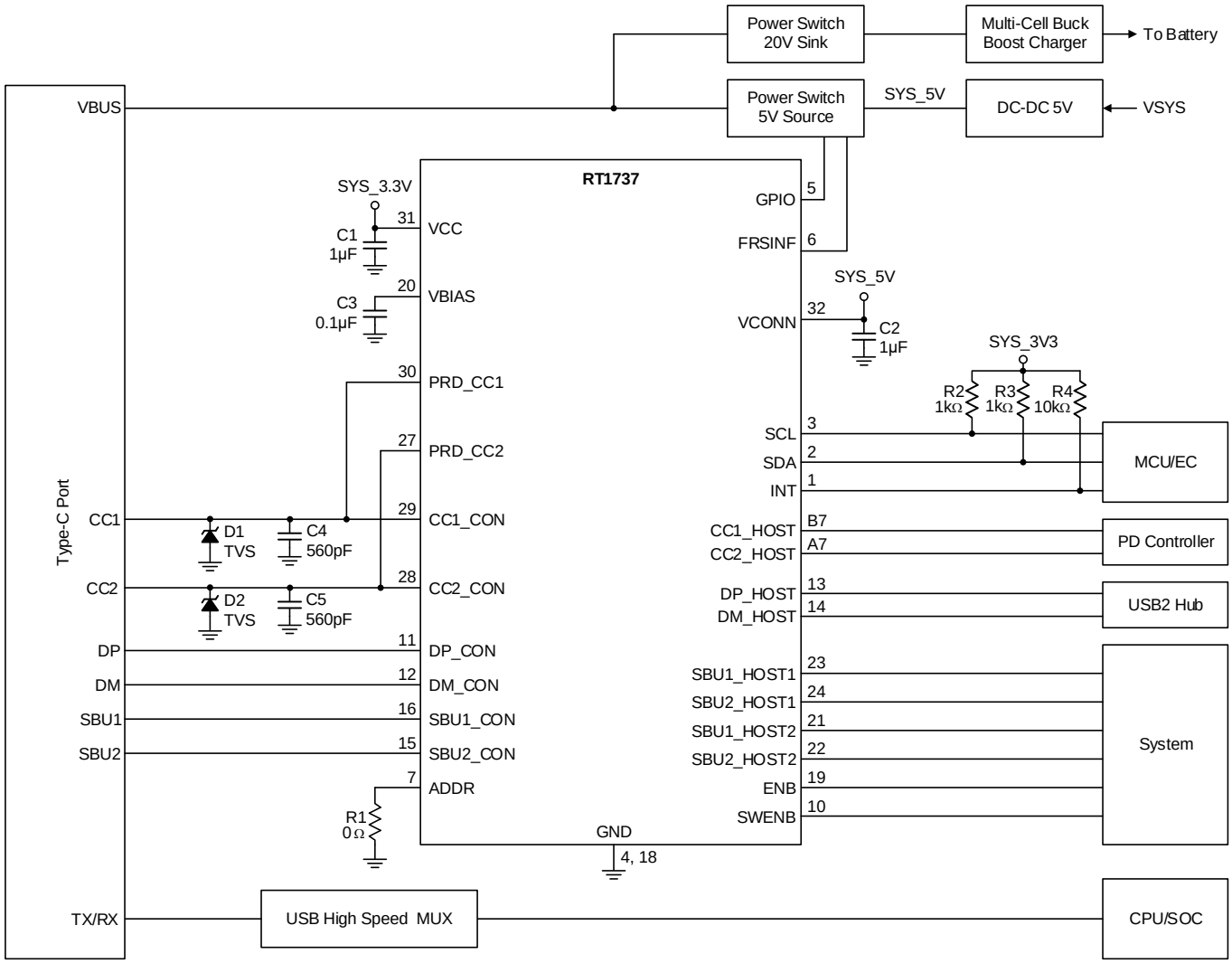
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

The RT1737 in DRP Application (DRP port, Source 5V, Sink 20V)



The followings are the recommended component information.

Pin	Part Number	Description	Package	Manufacturer
VCC (C1)	GRM155R61E105KA12	1µF/25V/X5R	0402	muRata
VCONN (C2)	GRM155R61E105KA12	1µF/25V/X5R	0402	muRata
VBIAS (C3)	0402B104K500CT	0.1µF/50V/X7R	0402	Walsin
CC1_CON (C4), CC2_CON (C5)	C0603C561J5RACAUTO	560pF/50V/X7R	0603	KEMET
CC1_CON (D1), CC2_CON (D2)	PESD12VV1BL	TVS Diodes	DFN-1006-2	Nexperia

Note: CC1_CON/CC2_CON is recommended to be put with TVS and Cap, that CC1_CON/CC2_CON will pass IEC61000-4-2 Contact Discharge ±8kV and Air Discharge ±15kV.

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

4-Channel IEC 61000-4-2 ESD Protection (SBU1_CON, SBU2_CON, DP_CON and DM_CON)

The RT1737 provides 4-Channel IEC 61000-4-2 system level ESD protection for the SBU1, SBU2, DP and DM pin. To ensure proper protection against electrostatic discharge (ESD) events that may affect end users, the USB Type-C interface requires IEC system level ESD protection. The RT1737's CC1_CON/CC2_CON is recommended to be put with TVS and Cap, that CC1_CON/CC2_CON will pass IEC61000-4-2 Contact Discharge ±8kV and Air Discharge ±15kV.

Input Overvoltage Protection

The RT1737 has 6-channel Short to VBUS overvoltage protection for the CC1, CC2, SBU1, SBU2, DP and DM pins of the USB Type-C receptacle via internal OVP level. When the input voltage exceeds the OVP level, the RT1737 will ultra-fast turn off internal switches around 60ns/80ns to prevent the high input voltage from damaging the end system. When the CC/SBU/DPDM input voltage returns to normal operation voltage range with hysteresis 60mV, the switch will turn on again.

All switches for CC1_CON/CC2_CON, SBU1_CON/SBU2_CON and DP_CON/DM_CON own OVP comparator and are controlled by their comparator independently. If any one of channel voltage exceeds OVP threshold, the channel switch will turn off.

Over-Temperature Protection (OTP)

The RT1737 monitors its internal temperature to prevent thermal failures. The chip turns off the switches when the junction temperature reaches 150°C. The IC will resume after the junction temperature is cool down by 40°C.

Chip Enable/Quiescent States

The active or quiescent states of the RT1737 are set by GPIO ENB, the states are shown below:

Chip State	Power-On	
ENB High/Low	High	Low
Chip state	Quiescent	Enable
All switch state	Off	By I^2C setting

Chip Data Switch Control States

The RT1737 Data Switch can be set by GPIO SWENB and I^2C, the states as shown below:

Chip State	Power-On Initial		After I^2C setting	
SWENB	High	Low	High	Low
SBUx_CON to SBUx_HOST1	On	On	by setting	On
SBUx_CON to SBUx_HOST2	Off	Off	by setting	Off
CCx_CON to CCx_HOST	On	On	by setting	On
DPDM_CON to DPDM_HOST	Off	Off	by setting	by setting

I²C Interface

The RT1737 can be configured to four slave addresses by setting the resistance between ADDR (pin 7) and GND.

I²C Address in 7-bit	Resistance between ADDR and GND (Unit: kΩ)
0x70	0
0x71	309
0x72	649
0x73	open

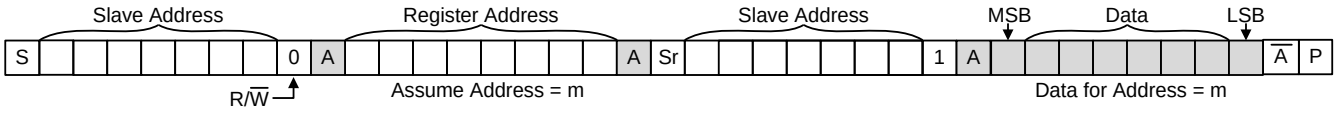
Taking the 0x73 in 7-bit for example.

RT1737 I²C Slave Address			
MSB	**LSB**	**R/W bit**	**R/W**
111001	1	1/0	87/86

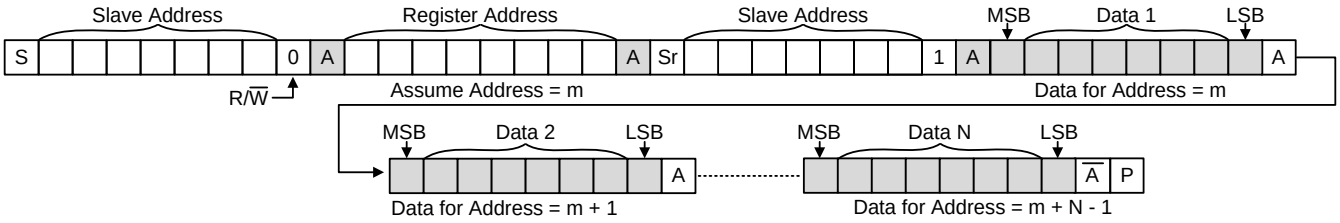
The I²C interface bus must be connected to a resistor of 1kΩ to power node and independently connected to processor, individually. The I²C timing diagrams are listed below.

- **Read and Write Function**

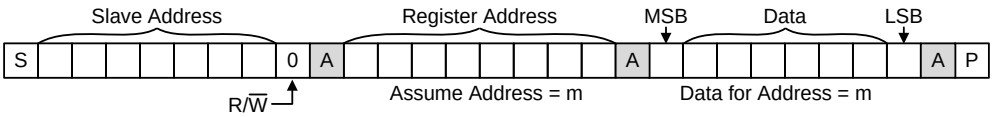
Read single byte of data from Register



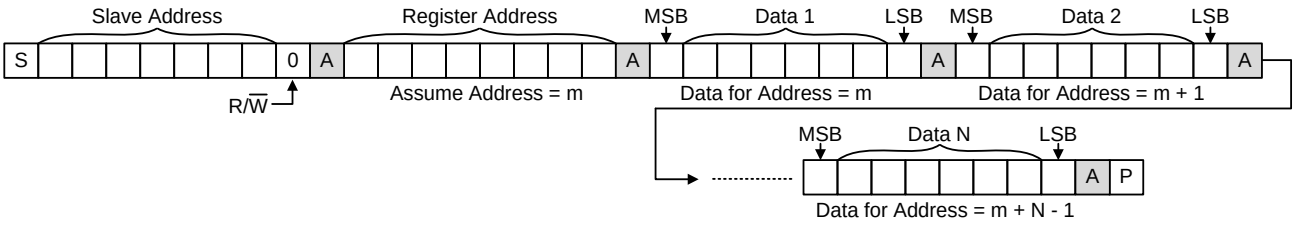
Read N bytes of data from Registers



Write single byte of data to Register

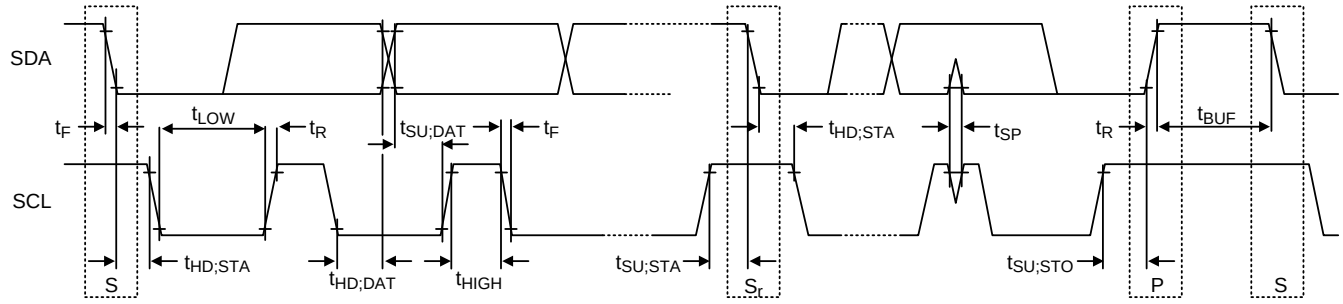


Write N bytes of data to Registers



Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

- **I²C Waveform Information**



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (27.5°C/W) = 3.63W for a WQFN-32L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

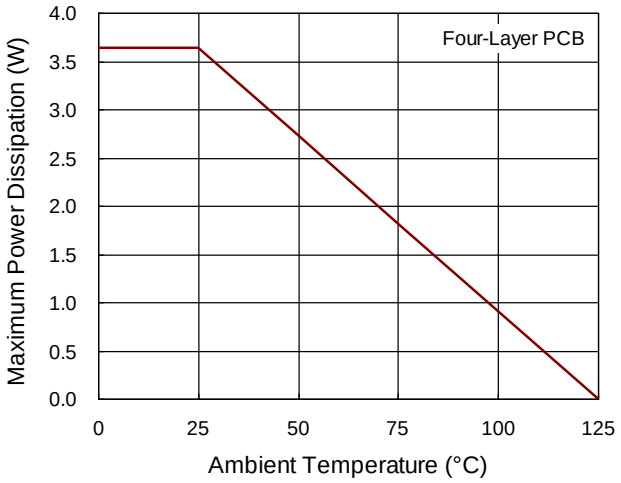


Figure 1. Derating Curve of Maximum Power Dissipation

Register Description

R: Read only

R/W: Read and write

RWS: Read and write, also automatically set by particular conditions

RWC: Read and write, also automatically cleared by particular conditions

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x00	1	PRODUCT_ID0	7:0	PRODUCT_ID	00110111	R	
0x01	1	PRODUCT_ID1	7:0	PRODUCT_ID	00010111	R	
0x02	1	DEVICE_ID0	7:0	DEVICE_ID	00000001	R	
0x03	1	DEVICE_ID1	7:0	DEVICE_ID	01001001	R	
0x04	1	SW_RESET	7:1	Reserved	0000000	R	Reserved
			0	SW_RESET	0	W	When writing 1'b1 to this bit, it will trigger soft-reset event, and all register setting will reset to default value. A delay of 1ms is recommended after soft-reset.
0x08	1	INT_MASK0	7	OT_FLAG_MASK	0	RW	OT flag change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			6	Reserved	0	R	Reserved
			5	POR_RESET_MASK	0	RW	POR reset INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			4:0	Reserved	00000	R	Reserved
0x09	1	INT_MASK1	7	CC_SW_MASK	0	RW	CC1/CC2 switch status change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			6	DPDM_SW_MASK	0	RW	DP/DM switch status change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			5	SBU12_SW_MASK	0	RW	SBU1/SBU2 switch status change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			4:0	Reserved	00000	R	Reserved
0x0A	1	INT_MASK2	7:0	Reserved	00000000	R	Reserved
0x0B	1	INT_MASK3	7:0	Reserved	00000000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x0C	1	INT_MASK4	7	FRS_TX_DONE_MASK	0	RW	FRS TX done INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			6:5	Reserved	00	R	Reserved
			4	FRS_RX_MASK	0	RW	FRS signal receive INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			3:0	Reserved	0000	R	Reserved
0x0D	1	INT_MASK5	7	VCON_SAFE0V_MASK	0	RW	VCON < 0.8V INT Mask 0: Interrupt masked (default) 1: Interrupt unmasked
			6	VCON_PRESENT_MASK	0	RW	VCON > 2.4V INT Mask 0: Interrupt masked (default) 1: Interrupt unmasked
			5:4	Reserved	00	R	Reserved
			3	BGOK_CHG_MASK	0	RW	Bandgap status change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			2	BC12_SRC_CHG_MASK	0	RW	BC12 source mode status change INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			1	HVDCP_CHK_DONE_MASK	0	RW	HVDCP check done INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			0	BC12_SNK_DONE_MASK	0	RW	BC12 sink mode flow done INT mask 0: Interrupt masked (default) 1: Interrupt unmasked

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x0E	1	INT_MASK6	7	VCON_SHT_GND_MASK	0	RW	VCON short to GND INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			6	VCON_UVP_MASK	0	RW	VCON UVP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			5	VCON_RCP_MASK	0	RW	VCON RCP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			4	VCON_RVP_MASK	0	RW	VCON RVP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			3	Reserved	0	R	Reserved
			2	VCON_OCP_MASK	0	RW	VCON OCP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			1	CC2_OV_MASK	0	RW	CC2 OVP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
			0	CC1_OV_MASK	0	RW	CC1 OVP INT mask 0: Interrupt masked (default) 1: Interrupt unmasked
0x10	1	INT_EVENT0	7	OT_FLAG_INT	0	RWC	0: Cleared (default) 1: OTP INT triggered
			6	Reserved	0	R	Reserved
			5	POR_RESET_INT	0	RWC	0: Cleared (default) 1: POR reset INT triggered
			4:0	Reserved	00000	R	Reserved
0x11	1	INT_EVENT1	7	CC12_SW_INT	0	RWC	0: Cleared (default) 1: CC1/CC2 switch OVP INT triggered
			6	DPDM_SW_INT	0	RWC	0: Cleared (default) 1: DP/DM switch OVP INT triggered
			5	SBU12_SW_INT	0	RWC	0: Cleared (default) 1: SBU1/SBU2 switch OVP INT triggered
			4:0	Reserved	00000	R	Reserved
0x12	1	INT_EVENT2	7:0	Reserved	00000000	R	Reserved
0x13	1	INT_EVENT3	7:0	Reserved	00000000	R	Reserved
0x14	1	INT_EVENT4	7	FRS_TX_DONE_INT	0	RWC	0: Cleared (default) 1: FRS TX done INT triggered
			6:5	Reserved	00	R	Reserved
			4	FRS_RX_INT	0	RWC	0: Cleared (default) 1: Receive CC FRS signal INT triggered
			3:0	Reserved	0000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x15	1	INT_EVENT5	7	VCON_SAFE0V_INT	0	RWC	0: Cleared (default) 1: VCON < 0.8V INT triggered
			6	VCON_PRESENT_INT	0	RWC	0: Cleared (default) 1: VCON > 2.4V INT triggered
			5:4	Reserved	00	R	Reserved
			3	BGOK_CHG_INT	0	RWC	0: Cleared (default) 1: Bandgap Status change INT triggered
			2	BC12_SRC_CHG_INT	0	RWC	0: Cleared (default) 1: BC12 source mode status change INT triggered
			1	HVDCP_CHK_DONE_INT	0	RWC	0: Cleared (default) 1: HVDCP check done INT triggered
			0	BC12_SNK_DONE_INT	0	RW	0: Cleared (default) 1: BC12 sink mode flow done INT triggered
0x16	1	INT_EVENT6	7	VCON_SHT_GND_INT	0	RW	0: Cleared (default) 1: VCON short to GND INT triggered
			6	VCON_UVP_INT	0	RW	0: Cleared (default) 1: VCON UVP INT triggered
			5	VCON_RCP_INT	0	RW	0: Cleared (default) 1: VCON RCP INT triggered
			4	VCON_RVP_INT	0	RW	0: Cleared (default) 1: VCON RVP INT triggered
			3	Reserved	0	R	Reserved
			2	VCON_OCP_INT	0	RW	0: Cleared (default) 1: VCON OCP INT triggered
			1	CC2_OV_INT	0	RW	0: Cleared (default) 1: CC2 OVP INT triggered
			0	CC1_OV_INT	0	RW	0: Cleared (default) 1: CC1 OVP INT triggered
0x18	1	INT_STS0	7	OT_FLAG	0	R	OT Flag
			6:0	Reserved	0000000	R	Reserved
0x19	1	INT_STS1	7:0	Reserved	00000000	R	Reserved
0x1A	1	INT_STS2	7:0	Reserved	00000000	R	Reserved
0x1B	1	INT_STS3	7:0	Reserved	00000000	R	Reserved
0x1C	1	INT_STS4	7:0	Reserved	00000000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x1D	1	INT_STS5	7	VCON_SAFE0V	0	R	0: VCON > 0.8V (default) 1: VCON < 0.8V
			6	VCON_ PRESENT	0	R	0: VCON < 2.4V (default) 1: VCON > 2.4V
			5:4	Reserved	00	R	Reserved
			3	BGOK_STS	0	R	Bandgap status 0: Bandgap ready (default) 1: Bandgap not ready
			2	BC12_SRC_ CHG	0	R	BC12 source mode status change
			1	HVDCP_CHK_ DONE	0	R	HVDCP check done
			0	BC12_SNK_ DONE	0	R	BC12 sink mode flow done
0x1E	1	INT_EVENT6	7	VCON_SHT_ GND	0	R	VCON OCP INT
			6	VCON_UVP	0	R	VCON OCP INT
			5	VCON_RCP	0	R	VCON OCP INT
			4	VCON_RVP	0	R	VCON OCP INT
			3	Reserved	0	R	Reserved
			2	VCON_OCP	0	R	VCON OCP INT
			1	CC2_OV	0	R	CC2 OVP INT
			0	CC1_OV	0	R	CC1 OVP INT
0x1F	1	SYS_ STATUS	7:6	Reserved	00	R	Reserved
			5	PIN_SWENB	0	R	Pin SWENB
			4:2	Reserved	000	R	Reserved
			1	PD_DBRD_ OPEN	0	R	Dead battery RD OPEN status 0: Dead battery RD connects to CC pin (default) 1: Dead battery RD is open from CC pin.
			0	Reserved	0	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x20	1	SYS_CTRL	7:5	Reserved	000	R	Reserved
			4	OT_EN	1	RW	Over-temperature protection enable 0: Disable 1: Enable (default)
			3:2	Reserved	00	R	Reserved
			1	DEAD_ BATTERY	0	RW	Dead battery mode When this bit is 1'b1, it will force the device to enter dead battery mode. In dead battery mode, HV/LV switch will be closed. This bit will auto-set to 1'b1 when VIN_LV < 2.9V. And this bit can only clear to 0 by I^2C when VIN_LV > 2.9V. 0: Exit dead battery mode (default) 1: In dead battery mode
			0	Reserved	1	R	Reserved
0x21	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x22	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x23	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x24	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x25	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x26	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x27	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x28	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x29	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x2A	1	Reserved	7:0	Reserved	00000000	R	Reserved
0x2B	1	Reserved	7:0	Reserved	00000000	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x2C	1	I2C_RESET	7	I2C_TO_RST_EN	0	RW	Set this bit to 1'b1 to enable I^2C reset timer. When I^2C reset timer is enabled, it will monitor SCL and SDA. When SCL and SDA both keep low, I^2C reset timer will start to count, and I^2C reset timer will be cleared to 0 when SCL or SDA become high. When I^2C reset timer timeout, it will trigger soft reset event, and all register will reset to default value. 0: Disable I^2C reset timer (default) 1: Enable I^2C reset timer
			6:4	Reserved	000	R	Reserved
			3:0	I2C_TO_RST_SEL	1000	RW	Timeout time for I^2C reset timer (timeout time = (I2C_TO_RST_SEL+1) * 16ms) 0000: 16ms 0001: 32ms … 1000: 144ms (default) ... 1111: 256ms
0x2D	1	CC_FRS_CTRL1	7:5	Reserved	000	R	Reserved
			4	FRSINF_CLEAR	0	RW	Set FRSINF to low Write this bit to 1'b1 will set FRSINF to low. After FRSINF set to low, this bit will clear to 1'b0. 0: No action (default) 1: Set FRSINF to Low
			3:2	Reserved	00	R	Reserved
			1	FRS_RX_EN	0	RW	Detect CC FRS signal enable 0: Disable (default) 1: Enable
			0	FRS_TX_EN	0	RW	Send CC FRS signal (drive CC low) This bit will auto clear to 1'b0 after 100μs 0: Disable (default) 1: Enable

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x2E	1	CC_FRS_CTRL2	7	FRS_CMPEN_HYS	1	RW	CC detection hysteresis enable control 0: Disable 1: Enable (default)
			6:4	Reserved	000	R	Reserved
			3:2	FRSINF_DRV	00	RW	FRSINF output driving ability 00: 20mV/s (default) 01: 40mV/s 10: 60mV/s 11: 80mV/s
			1	FRSINF_TYPE	0	RW	FRSINF output type 0: Open drain (default) 1: Push-pull
			0	FRSINF_EN	0	RW	FRSINF enable 0: Disable (Enable LV SRC path when FRS) (default) 1: Enable (Enable HV SRC path when FRS)
0x2F	1	CC_FRS_CTRL3	7:4	FRS_RX_TIME	1001	RW	Fast role swap detection time 0000: 4μs 0001: 8μs …. 1001: 40μs (default) …. 1111: 64μs
			3	FRS_RX_TYPE	0	RW	CC FRS signal detect type 0: Over FRS_RX_TIME (default) 1: Over FRS_RX_TIME and less than 128μs
			2	FRS_TIMEOUT_DIS	1	RW	Wait VIN_LV > VBUS after FRS timeout (200μs) 0: Keep wait VIN_LV > VBUS 1: Disable to wait VIN_LV > VBUS (default)
			1:0	VREF_RX_FRS	10	RW	Fast role swap detection threshold on CC pin 00: 0.48V 01: 0.50V 10: 0.52V (default) 11: 0.54V

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x30	1	CC_SW_CTRL	7	CC2_OVP_FLAG	0	R	CC2 OVP status 0: No OVP occurs (default) 1: OVP occurs
			6	CC1_OVP_FLAG	0	R	CC1 OVP status 0: No OVP occurs (default) 1: OVP occurs
			5	STS_CC2_SW	0	R	CC2 CON to HOST switch status 0: Disable (default) 1: Enable
			4	STS_CC1_SW	0	R	CC1 CON to HOST switch status 0: Disable (default) 1: Enable
			3:2	Reserved	00	R	Reserved
			1	CC_SWEN	0	RW	CC1/CC2 SW enable in normal mode 0: Disable CC1/CC2 switch (default) 1: Enable CC1/CC2 switch
			0	CC_TOGGLE_MODE	0	RW	CC Toggle mode When this bit set to 1'b1, CC1/CC2 switch will be enabled, and VCONN will be disabled. 0: CC1/CC2 in normal mode (default) 1: CC1/CC2 in toggle mode
0x31	1	VCONN_CTRL1	7:5	Reserved	000	R	Reserved
			4	VCONN_DISCHG_EN	0	RW	VCONN discharge enable 0: Disable VCONN discharge (default) 1: Enable VCONN discharge
			3:2	Reserved	00	R	Reserved
			1	VCONN_ORIENT	0	RW	VCONN orientation 0: When VCONN is enabled, apply it to the CC2 pin. (default) 1: When VCONN is enabled, apply it to the CC1 pin.
			0	VCONN_EN	0	RW	VCONN to CC1/CC2 enable VCONN can only be enable when STS_CC1_SW = 1'b1 0: Disable VCONN (default) 1: Enable VCONN to CC1/CC2

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x32	1	VCONN_CTRL2	7	VCONN_DET_EN	0	RW	CC pin (VCONN) detection enable control (sPD_VCONN_PRESENT_FLAG, sPD_VCONN_SAFE0V_FLAG, sPD_VCONN_INVALID_FLAG) 0: Disable (default) 1: Enable
			6:5	Reserved	00	R	Reserved
			4	VCONN_AUTO_DISCHG_EN	0	RW	VCON auto discharge enable. Set this bit to enable VCONN auto discharge when VCONN fault occur. 0: Not auto discharge (default) 1: Auto discharge
			3	VCONN_RCP_EN	0	RW	VCONN RCP enable control 0: Disable (default) 1: Enable
			2	VCONN_RVP_EN	0	RW	Set this bit to 1'b1 to enable PD_VCONN Reverse Voltage Protection. PD_VCONN Reverse Voltage Protection will check if CC (selected for VCONN) voltage is greater than PD_VCONN (internal VCONN voltage) or not. If this event occurred (CC voltage greater than PD_VCONN), VCONN_RVP(0x99[2]) will set to 1'b1, and PD_VCONN will be disabled. 0: Disable (default) 1: Enable
			1	CC2_OVP_EN_CC2	0	RW	Enable CC2 OVP, to detect whether CC2 voltage is greater than 5.75V 0: Disable (default) 1: Enable
			0	CC1_OVP_EN_CC1	0	RW	Enable CC1 OVP, to detect whether CC1 voltage is greater than 5.75V 0: Disable (default) 1: Enable

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x33	1	VCONN_CTRL3	7	VCONN_UVP_CP_EN	1	R	VCONN_INVALID_FLAG action selection: 0: After VCONN INVALID, wait digital turn-off VCONN_EN 1: After VCONN INVALID, VCONN_INVALID_FLAG directly turn-off VCONN_EN (default)
			6	VCONN_OCP_CP_EN	1	R	VCONN_OCP_FLAG action selection: 0: After VCONN OCP, wait digital turn-off VCONN_EN 1: After VCONN OCP, VCONN_OCP_FLAG directly turn-off VCONN_EN (default)
			5	VCONN_RCP_CP_EN	1	RW	VCONN_RCP_FLAG action selection: 0: After VCONN RCP, wait digital turn-off VCONN_EN 1: After VCONN RCP, VCONN_RCP_FLAG directly turn-off VCONN_EN (default)
			4	VCONN_RVP_CP_EN	1	RW	VCONN_RVP_FLAG action selection: 0: After VCONN RVP, wait digital turn-off VCONN_EN 1: After VCONN RVP, VCONN_RVP_FLAG directly turn-off VCONN_EN (default)
			3	VCONN_OVP_DEG	0	RW	VCONN OVP deglitch 0: Deglitch disable (default) 1: Deglitch enable
			2	VCONN_RVP_SEL	0	RW	Threshold for PD_VCONN reverse voltage protection 0: PD_VCONN + 0.3V (default) 1: PD_VCONN + 0.5V
			1	VCONN_UVP_SEL	0	RW	VCONN undervoltage protect selection: 0: From VCONN_INVALID (2.7V) (default) 1: From VCONN_PRESENT (2.4V)
			0	Reserved	0	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x34	1	VCONN_CTRL4	7:5	VCONN_RCP_SEL	000	RW	VCONN RCP level selection (typical) 000: 50mA (default) 001:100mA 010: 200mA 011: 300mA 100: Reserved 101: Reserved 110: Reserved 111: Reserved
			4:2	VCONN_OCP_SEL	010	RW	PD_VCONN OCP level selection 000: Reserved 001: 200mA 010: 300mA (default) 011: 400mA 100: 500mA 101: 600mA 110: 700mA 111: Reserved
			1:0	CC_OVP_SEL	01	RW	CC1/CC2 OVP threshold selection 00: 3.6V 01: 3.8V (default) 10: 5.8V 11: 5.8V
0x35	1	VCONN_CTRL5	7:5	Reserved	000	R	Reserved
			4:3	VCONN_GATDIS_SEL	00	RW	Discharge resistor of VCONN SW gate 00: NMOS (default) 01: NMOS + 1kΩ 10: NMOS + 10kΩ 11: NMOS + 100kΩ
			2:1	VCONN_SHT_GND_TIMER	10	RW	PD_VCONN shot to GND check timer. When VCONN_EN = 1, if VCONN_PRESENT = 0 & After VCONN_SHT_GND_TIMER, VCONN_SHT_GND will go 1 00: 0.5ms 01: 0.75ms 10: 1ms (default) 11: 3ms
			0	VCONN_SOFTEND_TIMER	0	RW	Soft-start time after PD_VCONN enabled. 0: 3ms (default) 1: 5ms
0x36	1	Reserved	7:0	Reserved	00001111	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x38	1	SBU_CTRL_01	7:6	Reserved	00	R	Reserved
			5	SWEN_OVP_DLY	0	RW	OVP flag delay time after OV_EN enable 0: 8μs (default) 1: 1μs
			4	SBUSW_MUX_SEL	1	RW	SBU to Host Mux select 0: SBU1_CON to SBU1_HOST2, SBU2_CON to SBU2_HOST2 1: SBU1_CON to SBU1_HOST1, SBU2_CON to SBU2_HOST1 (default)
			3	SBU2_SWEN	1	RW	SBU2 switch enable 0: Disable 1: Enable (default)
			2	SBU1_SWEN	1	RW	SBU1 switch enable 0: Disable 1: Enable (default)
			1	DM_SWEN	0	RW	DM switch enable 0: Disable (default) 1: Enable
			0	DP_SWEN	0	RW	DP switch enable 0: Disable (default) 1: Enable
0x39	1	SBU_CTRL_02	7:2	Reserved	000000	R	Reserved
			1:0	SBU_OV_SEL	11	RW	SBU1/SBU2 OVP level select 00: 3.6V 01: 3.7V 10: 3.8V 11: 4.5V (default)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x3A	1	SBU_CTRL_03	7	DPDM_OV_DEG	0	RW	DPDM OVP deglitch 0: Deglitch disable (default) 1: Deglitch enable
			6	SBU_OV_DEG	0	RW	SBU OVP deglitch 0: Deglitch disable (default) 1: Deglitch enable
			5:4	SBUDPDM_REC_TIME	00	RW	DPDM OVP recovery time 00: 200μs (default) 01: 400μs 10: 600μs 11: 800μs Note: ±8μs
			3	SBUDPDM_REC_TYPE	1	RW	SBU OVP recovery type select 0: Recovery time compute after OV rising 1: Recovery time compute after OV falling (default)
			2	CC_OV_OFF_ALL	0	RW	Switch off when CC OV 0: Turn off CC/VCONN (default) 1: Turn off SBU1/SBU2/DP/DM/CC1/CC2/VCONN
			1	DPDM_OV_OFF_ALL	0	RW	Switch off when DPDM OV 0: Turn off DP/DM (default) 1: Turn off SBU1/SBU2/DP/DM/CC1/CC2/VCONN
			0	SBU_OV_OFF_ALL	0	RW	Switch off when SBU OV 0: Turn off SBU1/SBU2 (default) 1: Turn off SBU1/SBU2/DP/DM/CC1/CC2/VCONN

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x3B	1	SBUDPDM_OV_STS	7	SBU2_OV_FLAG	0	R	SBU2 OVP status 0: No OVP occurs (default) 1: OVP occurs
			6	SBU1_OV_FLAG	0	R	SBU1 OVP status 0: No OVP occurs (default) 1: OVP occurs
			5	DM_OV_FLAG	0	R	DM OVP status 0: No OVP occurs (default) 1: OVP occurs
			4	DP_OV_FLAG	0	R	DP OVP status 0: No OVP occur (default) 1: OVP occur
			3	STS_SBU2_SWEN	1	R	SBU2 switch status 0: Switch off 1: Switch on (default)
			2	STS_SBU1_SWEN	1	R	SBU1 switch status 0: Switch off 1: Switch on (default)
			1	STS_DM_SWEN	0	R	DM switch status 0: Switch off (default) 1: Switch on
			0	STS_DP_SWEN	0	R	DP switch status 0: Switch off (default) 1: Switch on
0x40	1	BC12_SNK_FUNC	7	BC12_SNK_EN	0	RW	Enable BC12 Sink side function 0: Disable (default) 1: Enable
			6	Reserved	1	R	Reserved
			5:4	DCDT_SEL	10	RW	DCD timeout function select 00: Disable DCD timeout function 01: Enable 300ms DCD timeout function 10: Enable 600ms DCD timeout function (default) 11: Wait data contact
			3	VLGC_OPT	0	RW	Enable primary detection high reference voltage option 0: Disable (default) 1: Enable
			2	VPORT_SEL	1	RW	Voltage select for primary detection, secondary detection and HVDCP detection 0: 0.6V 1: Depends on DPDM_VSRC_SEL (default)
			1:0	Reserved	00	R	Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x41	1	BC12_STAT	7:6	Reserved	00	R	Address is reserved and register is physically designed
			5	HVDCP	0	R	1: TA is HVDCP
			4	DCDT	0	R	1: DCD time out
			3:0	PORT_STAT	0000	R	0000: No information (default) 0001 to 0111: Reserved 1000: VBUS = device 1 (2.7V & 2V mode) 1001: VBUS = device 2 (1.2V & 1.2V mode) 1010: VBUS = device 3 (2V & 2.7V mode) 1011: VBUS = device 4 (2.7V & 2.7V mode) 1100: VBUS = device 5 (2V & 2V mode)/unknown TA (500mA) 1101: VBUS = SDP (500mA) 1110: VBUS = CDP (1500mA) 1111: VBUS = DCP (2400mA)
0x43	1	DPDM_CTR1 DPDM_SET	7	MANUAL_ MODE	0	RW	Enable DPDM control by SW manual mode
			6	DPDM_DET_EN	0	RW	Enable DPDM_DET BASE
			5	DPDM_SW_ VCP_EN	0	RW	Enable DPDM HVSW and charge-pump, pull gate voltage to VCP
			4	DPDM_SW_EN	0	RW	When DPDM_SW_VCP_EN = 0, enable DPDM HVSW, pull gate voltage to VDDA (Reg direct out)
			3	DPDM_SHORT _EN	0	RW	DPDM short enable 0: Not short (default) 1: Short
			2	Reserved	0	R	Reserved
			1:0	DPDM_VSRC _SEL	10	RW	VDP_SRC/VDM_SRC voltage selection 11: 0.70V 10: 0.65V (default) 01: 0.60V 00: 0.55V

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x44	1	DPDM_CTR2 LDO_VSET	7	DP_LDO_EN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_LDO_VSEL	000	RW	DP LDO output voltage selection 000: 0.6V (DPDM_VSRC_SEL MUST = 2'b00) (default) 001: 1.8V (DPDM_VSRC_SEL MUST = 2'b01) 010: 2.8V (DPDM_VSRC_SEL MUST = 2'b01) 011: 3.3V (DPDM_VSRC_SEL MUST = 2'b01) 100: 1.2V 101: 2.7V 110: Reserved 111: Reserved
			3	DM_LDO_EN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			2:0	DM_LDO_VSEL	000	RW	DM LDO output voltage selection 000: 0.6V (DPDM_VSRC_SEL MUST = 2'b00) (default) 001: 1.8V (DPDM_VSRC_SEL MUST = 2'b01) 010: 2.8V (DPDM_VSRC_SEL MUST = 2'b01) 011: 3.3V (DPDM_VSRC_SEL MUST = 2'b01) 100: 1.2V 101: 2.7V 110: Reserved 111: Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x45	1	DPDM_CTR3 DISCHG_ SET	7	DP_DISCHG_ EN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_DISCHG_ RSEL	000	RW	DP discharge resistor selection 000: 6.0kΩ (default) 001: 20kΩ 010: 0.7μA 011: 100μA 1xx: 900kΩ
			3	DM_DISCHG_ EN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			2:0	DM_DISCHG_ RSEL	000	RW	DM discharge resistor selection 000: 6.0kΩ (default) 001: 20kΩ 010: 0.7μA 011: 100μA 1xx: 900kΩ
0x46	1	DPDM_CTR4 DP_PULL_ SET	7	DP_PULL_REN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DP_PULL_ RSEL	011	RW	DP pull-up resistor selection 000: 1.2kΩ 001: 10kΩ 010: 15kΩ 011: Bypass (~120Ω) (default) 100: 30kΩ 101: 102kΩ
			3	Reserved	0	R	Reserved
			2	DP_PULL_IEN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			1:0	DP_PULL_ISEL	01	RW	DP pull-up current selection 01: 10μA (default) Others: Reserved

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x47	1	DPDM_CTR5 DM_PULL_ SET	7	DM_PULL_REN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			6:4	DM_PULL_ RSEL	011	RW	DM pull-up resistor selection 000: 1.2kΩ 001: 10kΩ 010: 15kΩ 011: Bypass (~120Ω) (default) 100: 30kΩ 101: 102kΩ
			3	reserved	0	R	Reserved
			2	DM_PULL_IEN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			1:0	DM_PULL_ISEL	01	RW	DM pull-up current selection 01: 10μA (default) Others: Reserved
0x48	1	DPDM_CTR6 DPDM_VREF _HIDET	7:5	Reserved	000	R	Reserved
			4:0	VREF_HIDET	00000	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI)

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x49	1	DPDM_CTR7 DPDM_VREF_LODET	7:5	Reserved	000	R	Reserved
			4:0	VREF_LODET	00000	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V (default) … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI)
0x4A	1	DPDM_CTR8 DPDM_CMP	7	Reserved	0	R	Reserved
			6	DPDM_HIDET_CMPEN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			5	DPDM_LODET_CMPEN	0	RW	While manual mode == '1', change to manual mode 0: Disable (default) 1: Enable
			4	DPDM_CMP_HYS_EN	0	RW	DPDM detection hysteresis enable control 0: Disable (default) 1: Enable
			3:0	Reserved	0000	R	Reserved
0x4B	1	DPDM_CTR9 DPDM_STATUS	7:4	DPDM_STATUS	0000	R	DPDM CMP Status
			3	DP_HIDET_OUT	0	R	DP 0: V_{IN} > VREF_HI (default) 1: V_{IN} < VREF_HI
			2	DP_LODET_OUT	0	R	DP 0: V_{IN} < VREF_LO (default) 1: V_{IN} > VREF_LO
			1	DM_HIDET_OUT	0	R	DM 0: V_{IN} > VREF_HI (default) 1: V_{IN} < VREF_HI
			0	DM_LODET_OUT	0	R	DM 0: V_{IN} < VREF_LO (default) 1: V_{IN} > VREF_LO
0x4C	1	AUTO_TA_CTRL	7:6	Reserved	00	R	Reserved
			5	AUTO_TA_DP_RSEL	0	RW	DP pulldown resistor in auto TA mode 0: 20k (default) 1: 900k

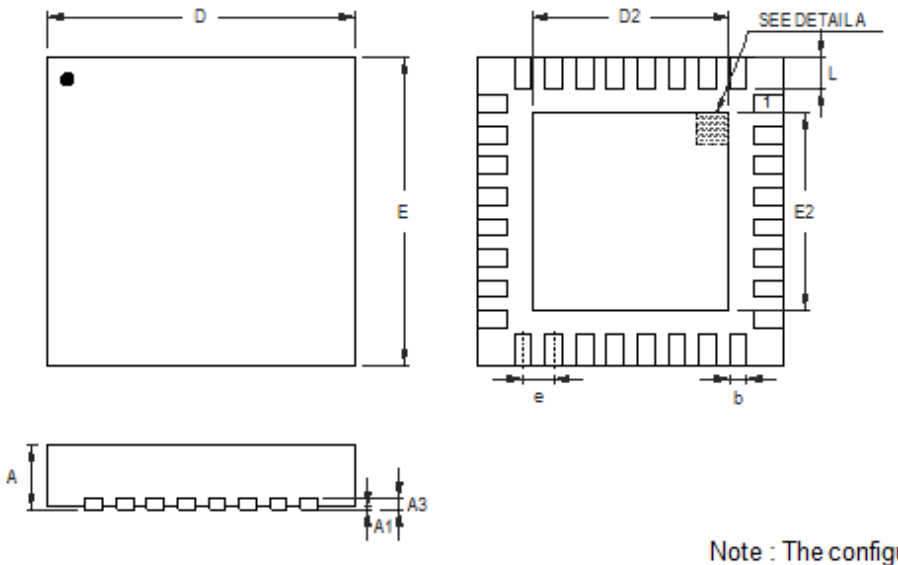
Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
			4:0	Reserved	11101	R	Reserved
0x4D	1	BC12_SRC_FUNC	7	BC12_SRC_EN	0	RW	BC12/TA function enable 0: Disable (default) 1: Enable
			6:4	SRC_MODE_SEL	000	RW	Mode selection 000: BC12 SDP (default) 001: BC12 CDP 010: BC12 DCP 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Auto TA
			3:0	Reserved	0000	R	Reserved
0x4E	1	SRC_STS_01	7	HVDCP_IN_ATTACH	0	R	HVDCP device attach 0: No HVDCP device attach (default) 1: HVDCP device attach Note: This bit preset the current state of HVDCP device. This bit can be checked any time.
			6:5	Reserved	00	R	Reserved
			4	STS_HVDCP_CHG	0	R	HVDCP DPDM level change 0: No DPDM level change (default) 1: DPDM level change (keep stable over HVDCP_GLITCH_CHG time) Note: This bit is updated after INT_BC12_TA_CHG is set to 1'b1. It will remain unchanged until next time INT_BC12_TA_CHG is set to 1'b1. Check this bit only after INT_BC12_TA_CHG is set to 1'b1.
			3:2	Reserved	00	R	Reserved
			1	STS_CDP_ERR	0	R	CDP flow error 0: No CDP flow error (default) 1: CDP flow error Note: This bit is updated after INT_BC12_TA_CHG is set to 1'b1. It will remain unchanged until next time INT_BC12_TA_CHG is set to 1'b1. Check this bit only after INT_BC12_TA_CHG is set to 1'b1.
			0	STS_CDP_DONE	0	R	CDP flow done 0: No CDP flow (default) 1: CDP flow done Note: This bit is updated after INT_BC12_TA_CHG is set to 1'b1. It will remain unchanged until next time INT_BC12_TA_CHG is set to 1'b1. Check this bit only after INT_BC12_TA_CHG is set to 1'b1.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x4F	1	SRC_STS_02	7:4	DECR_CNT	0000	R	Decreasing count Note: This register will be updated after writing any value to this byte.
			3:0	INCR_CNT	0000	R	Increasing count Note: This register will be updated after writing any value to this byte.
0x50	1	SRC_CTRL_01	7:6	DPDM_GLITCH	00	RW	DP/DM deglitch 00: 100μs (default) 01: 132μs 10: 168μs 11: 200μs
			5:4	USBDET_TIMEOUT_SEL	10	RW	USB device detect timeout 00: 1.024s 01: 2.048s 10: 4.096s (default) 11: 8.192s
			3:2	PRIMARY_TIMEOUT_SEL	00	RW	Primary detection timeout 00: 1.0s (default) 01: 1.3s 10: 1.6s 11: 2.0s
			1:0	CDP_VSRC_ON_SEL	10	RW	V_{SRC_ON} time detect 00: 16ms 01: 24ms 10: 32ms (default) 11: 40ms

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x51	1	SRC_CTRL_02	7	Reserved	0	R	Reserved
			6	SCP_VREF_SEL	0	RW	SCP V_{REF} select (for SCP 0.4V & 2.5V) 0: 0.325V (default) 1: 2.425V
			5	SCP_CMP_HYS_EN	0	RW	DPDM detection hysteresis enable control for 0.4V & 2.5V (SCP) 0: Disable (default) 1: Enable
			4:0	DPDM_VOL_H2	10011	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: In CDP mode, this register is used to check USB attach level. In Auto TA mode, this register is used to check DPDM high level after device attach.

Address	Length	Register Name	Bit	Bit Name	Default	Type	Description
0x52	1	SRC_CTRL_03	7:5	Reserved	010	RW	Reserved
			4:0	DPDM_VOL_H	01001	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP to check Vdp_src high level
0x53	1	SRC_CTRL_04	7:6	HVDCP_GLITCH_CHG	01	RW	HVCP DPDM change deglitch 00: 16ms 01: 25ms (default) 10: 40ms 11: 55ms
			5	Reserved	0	R	Reserved
			4:0	DPDM_VOL_L	11010	RW	DPDM voltage detection setting (HI/LO) Threshold: 0.1V to 2.6V (LSB = 0.1V) 00000: 0.1V … 11001: 2.6V ---------- 11010: 0.275V (BC1.2 VDAT_REF_MIN) (default) 11011: 0.375V (BC1.2 VDAT_REF_MAX) 11100: 0.9V (BC1.2 VLGC_MIN) 11101: 1.975V (BC1.2 VLGC_MAX) 11110: 1.5V (A_DET_LO) 11111: 2.3V (A_DET_HI) Note: This register is used for CDP to check Vdp_src high level

Outline Dimension

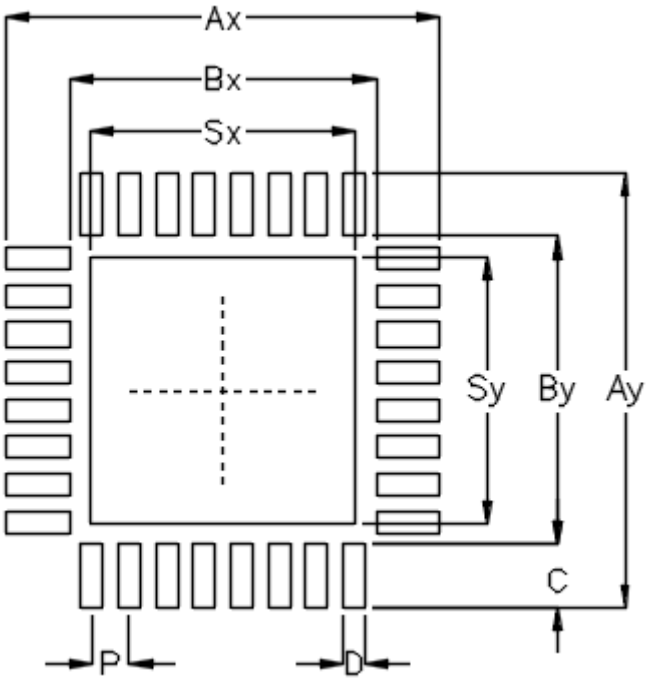


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

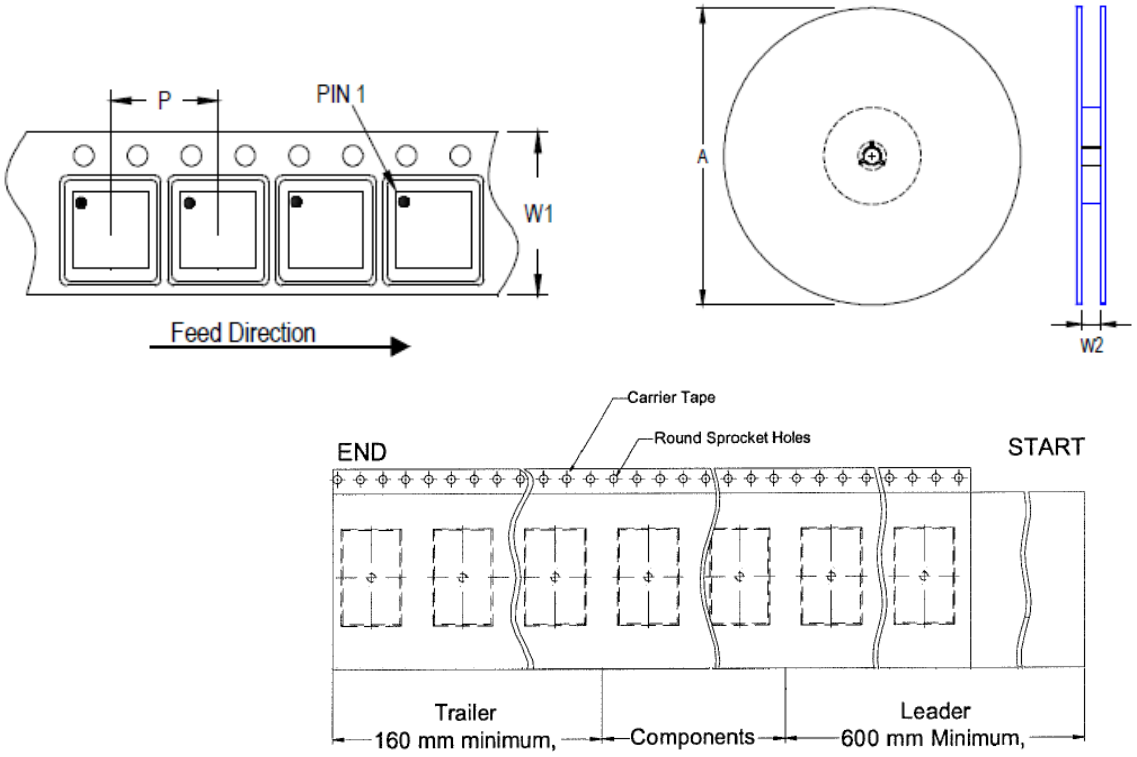
Footprint Information



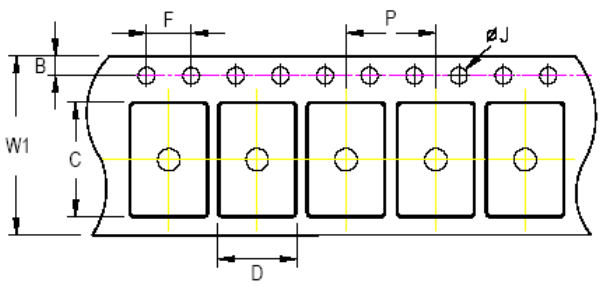
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-32	32	0.50	5.80	5.80	4.10	4.10	0.85	0.30	3.55	3.55	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/5/10	Final	Marking Information on P2