

## 1A, 6V, Ultra Low Dropout Linear Regulator

### General Description

The RT2517C is a high performance positive voltage regulator designed for applications requiring low input voltage and ultra low dropout voltage at up to 1A. The feature of ultra low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 2.2V and the output voltage is adjustable by an external resistive divider. The RT2517C provides an excellent output voltage regulation over variations in line, load and temperature. Current limit and thermal shutdown functions are provided. Additionally, an enable pin is designed to further reduce power consumption while shutdown and the shutdown current is as low as 0.1µA.

The RT2517C is available in the VDFN-8AL 3x3 package.

### Ordering Information

RT2517C	□□
	└─ Package Type
	QV : VDFN-8AL 3x3 (V-Type)
	└─ Lead Plating System
	G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

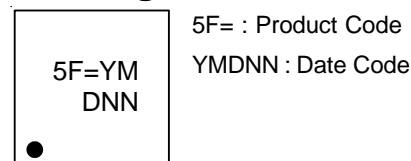
### Features

- Input Voltage Range : 2.2V to 6V
- V<sub>OUT</sub> Range from 1.2V to V<sub>IN</sub> - V<sub>DROP</sub>
- Reference Voltage : 1.2V ±2.5% over -40°C to 85°C
- Ultra Low Dropout Voltage : 150mV at 1A over -40°C to 85°C
- Low Quiescent 0.1µA in Shutdown Mode
- Soft-Discharge Function
- Thermal Shutdown and Current Limit
- RoHS Compliant and Halogen Free

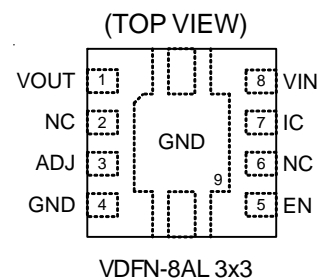
### Applications

- Automotive Audio, Navigation, & Info systems
- Industrial Grade General Purpose Point of Load
- Digital Set Top Boxes
- Vehicle Electronics

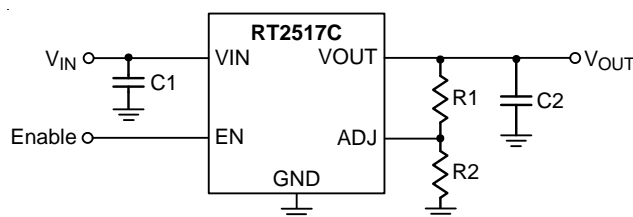
### Marking Information



### Pin Configuration



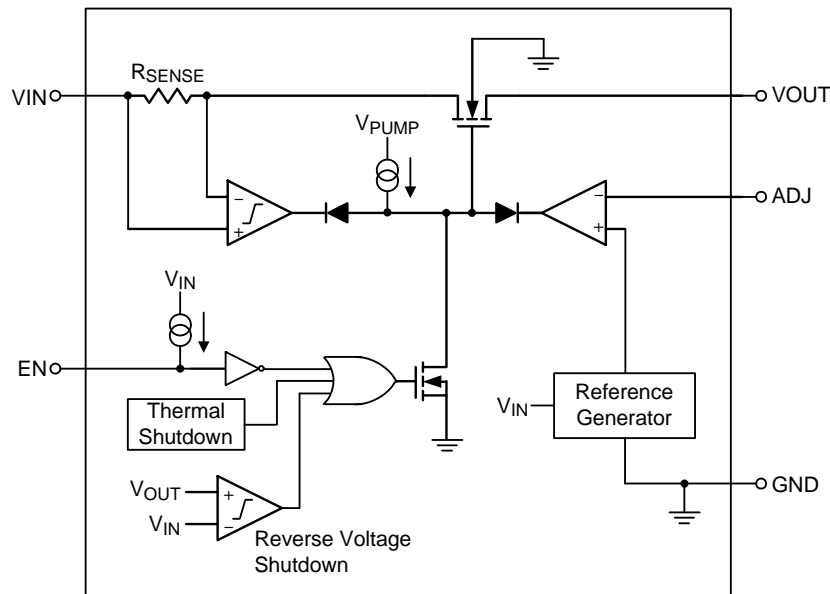
### Simplified Application Circuit



## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT	Output voltage. A minimum 10 $\mu$ F capacitor should be placed directly at this pin.
2, 6	NC	No internal connection.
3	ADJ	Feedback voltage input. Connect an external resistor divider to this pin for output voltage setting. If this pin is connected to the VOUT pin, the output voltage will be set at 1.2V.
4, 9 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum the power dissipation.
5	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to VIN if not used. (EN pin is not allowed to be left floating)
7	IC	Internal connection. Leave floating and do not make connection to this pin.
8	VIN	Supply voltage input. Connect a minimum 10 $\mu$ F ceramic capacitor at this pin.

## Functional Block Diagram



## Operation

The RT2517C is a low input voltage low dropout LDO that can support the input voltage range from 2.2V to 6V and the output current can be up to 1A. The RT2517C uses internal charge pump to achieve low input voltage operation and the internal compensation network is well designed to achieve fast transient response with good stability.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the on resistance of the power MOSFET is decreased to increase the output current through the power MOSFET, and the feedback voltage will be charge back to reference. If the feedback voltage is less than the reference, the power MOSFET current is decreased to make the output voltage discharge back to reference by the loading current.

### Reverse Current Protection

The reverse current protection is guarantee by the N-MOSFET with bulk capacitors connected to GND and the internal circuit. The reverse voltage detection circuit shuts the total loop down if the output voltage is higher than input voltage.

### Output Under-Voltage Protection (UVP) and Over-Current Fold-Back

When the feedback voltage is lower than 0.15V after internal soft-start end, the UVP is triggered. If the over-current condition is triggered during UVP state, the OC limit current will be decreased to limit the output power and change into re-soft start state at the same time.

### Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time is 150μs. During the soft-start state, the output current will be limited to prevent the inrush current.

### Over-Temperature Protection (OTP)

The RT2517C has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature back to normal and move to re-soft start state.

## Absolute Maximum Ratings (Note 1)

- Supply Voltage,  $V_{IN}$  ----- -0.3V to 7V
- Other Pins ----- -0.3V to 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$   
 VDFN-8AL 3x3 ----- 3.31W
- Package Thermal Resistance (Note 2)  
 VDFN-8AL 3x3,  $\theta_{JA}$  ----- 30.2°C/W  
 VDFN-8AL 3x3,  $\theta_{JC}$  ----- 5.5°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)  
 HBM (Human Body Model) ----- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage,  $V_{IN}$  ----- 2.2V to 6V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

( $V_{IN} = 2.2\text{V}$  to  $6\text{V}$ ,  $I_{OUT} = 10\mu\text{A}$  to  $1\text{A}$ ,  $V_{ADJ} = V_{OUT}$ ,  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	$V_{OUT}$	$V_{IN} = 3.3\text{V}$ , $T_A = 25^\circ\text{C}$	-1	--	1	%
		$2.2\text{V} \leq V_{IN} \leq 6\text{V}$ , $10\text{mA} \leq I_{OUT} \leq 1\text{A}$	-2.5	--	2.5	
Shutdown Current	$I_{SHDN}$	$V_{IN} = 3.3\text{V}$ , $V_{EN} = 0\text{V}$	--	0.1	--	$\mu\text{A}$
Quiescent Current	$I_Q$	$V_{IN} = 3.3\text{V}$ , $I_{OUT} = 0\text{A}$	--	0.4	--	mA
Line Regulation	$\Delta V_{LINE}$	$I_{OUT} = 10\text{mA}$	--	0.01	--	%/V
Load Regulation	$\Delta V_{LOAD}$	$I_{OUT} = 10\text{mA}$ to $1\text{A}$ , $V_{IN} = 3.3\text{V}$	--	0.5	--	%A
Current Limit	$I_{LIM}$	$V_{IN} = 3.3\text{V}$	1.05	1.6	--	A
Short-Circuit Current	$I_{SC}$	$V_{OUT} = 0\text{V}$	--	700	--	mA
Current Foldback Threshold	$V_{Fold}$	$V_{IN} = 3.3\text{V}$	--	0.4	--	V
Dropout Voltage	$V_{DROP}$	$I_{OUT} = 1\text{A}$	--	150	300	mV
ADJ Reference Voltage	$V_{ADJ}$	$V_{IN} = 3.3\text{V}$ , $V_{ADJ} = V_{OUT}$ , $I_{OUT} = 10\text{mA}$ $T_A = 25^\circ\text{C}$	1.192	1.2	1.216	V
ADJ Current	$I_{ADJ}$	$V_{IN} = 3.3\text{V}$	--	20	--	nA
Power Supply Rejection Ratio	PSRR	$f = 100\text{Hz}$ , $I_{OUT} = 1\text{A}$	--	58	--	dB
		$f = 10\text{kHz}$ , $I_{OUT} = 1\text{A}$	--	37	--	
Output Noise Voltage	$e_{NO}$	$C_{OUT} = 10\mu\text{F}$	--	$27 \times V_{OUT}$	--	$\mu\text{V}_{RMS}$
EN Input Voltage	Logic-High	$V_{IH}$	1.7	--	--	V
	Logic-Low	$V_{IL}$	--	--	0.5	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Current	$I_{EN}$	$V_{IN} = 6V, V_{EN} = 0V$	--	0.02	--	$\mu A$
Thermal Shutdown Threshold	$T_{SD}$		--	160	--	$^{\circ}C$
Thermal Shutdown Hysteresis	$\Delta T_{SD}$		--	30	--	$^{\circ}C$

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^{\circ}C$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

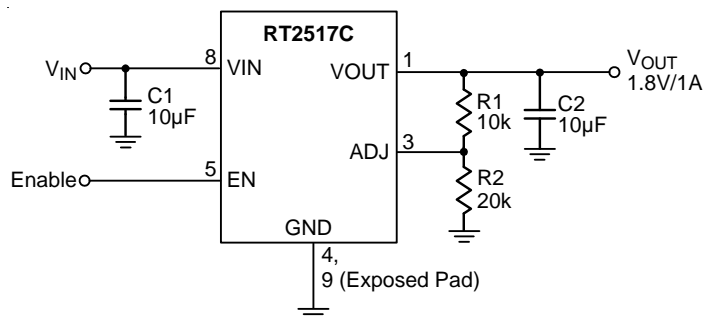
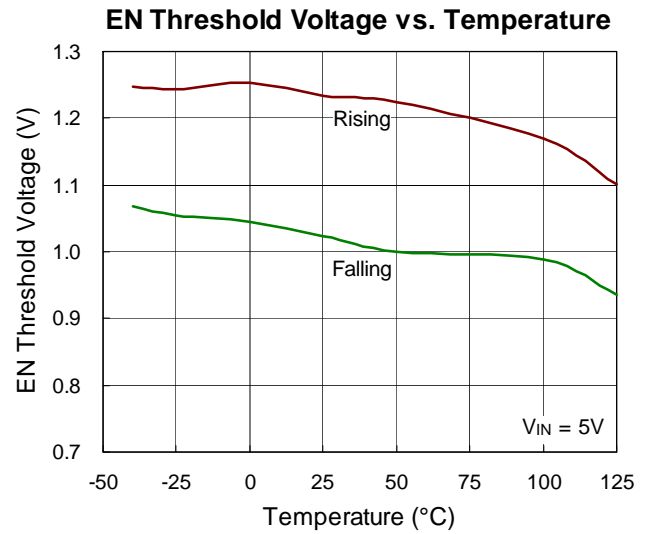
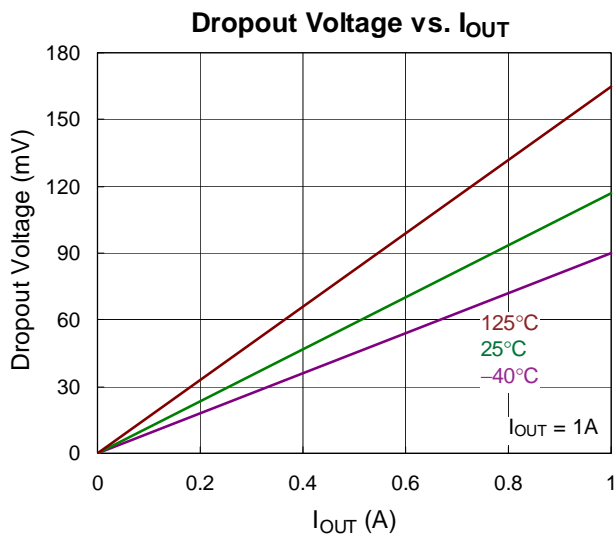
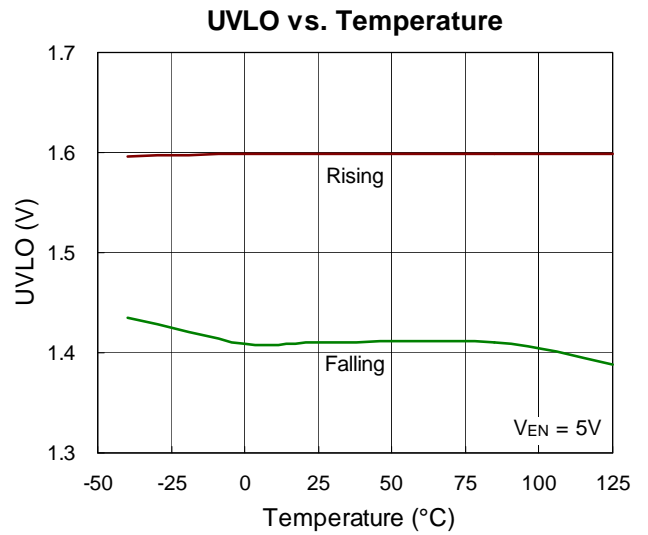
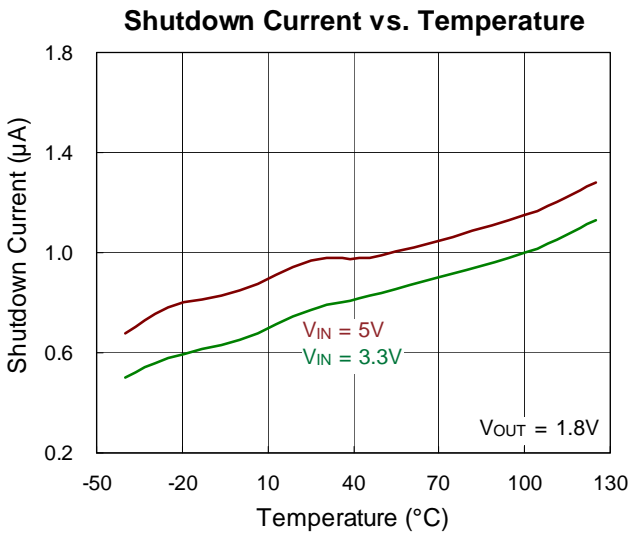
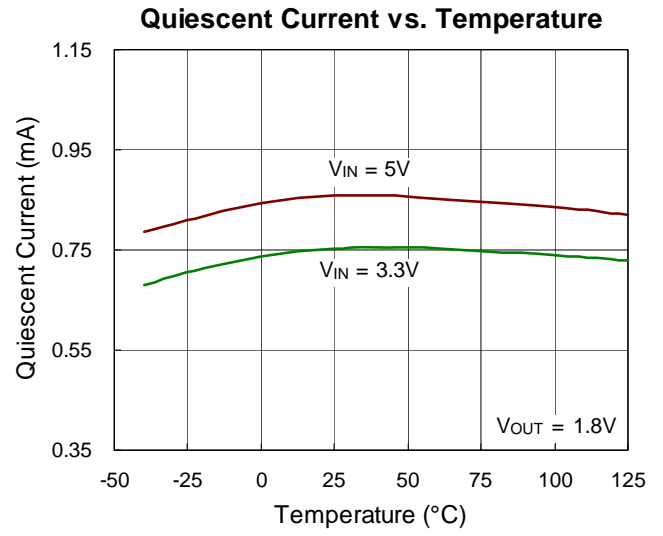
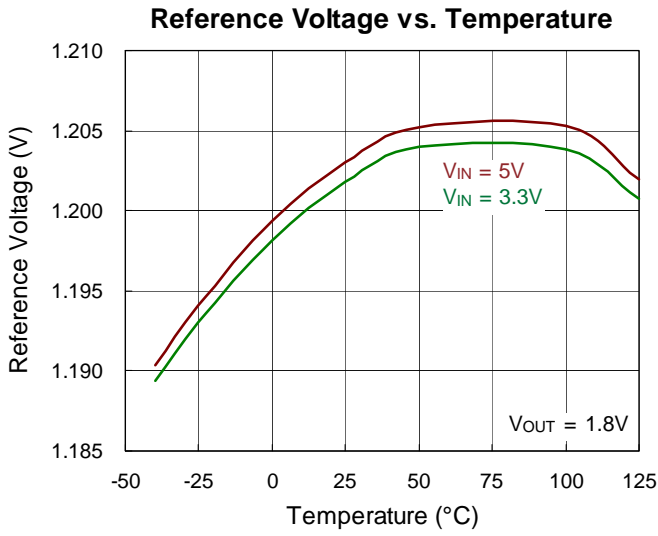
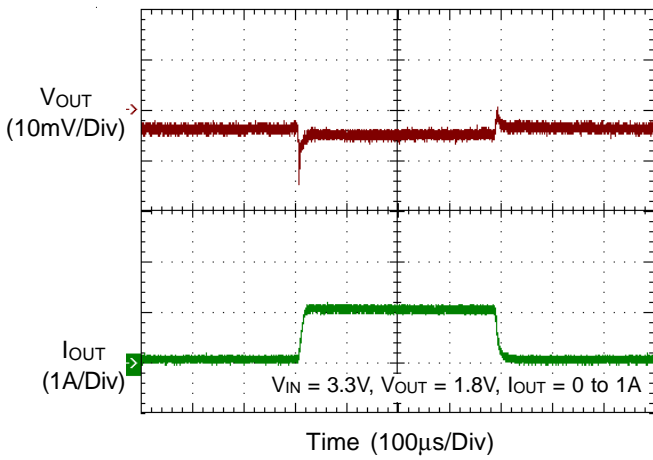


Figure 1. 1.8V Output Voltage Operation Circuit

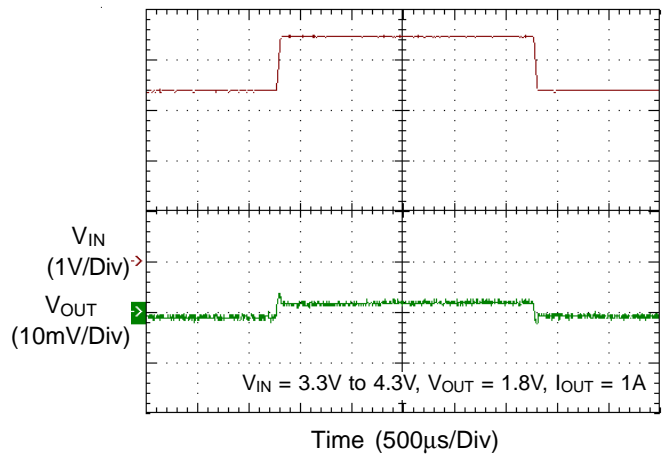
**Typical Operating Characteristics**



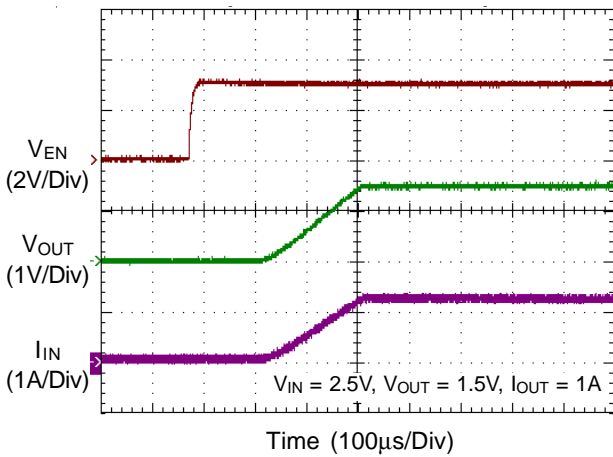
Load Transient Response



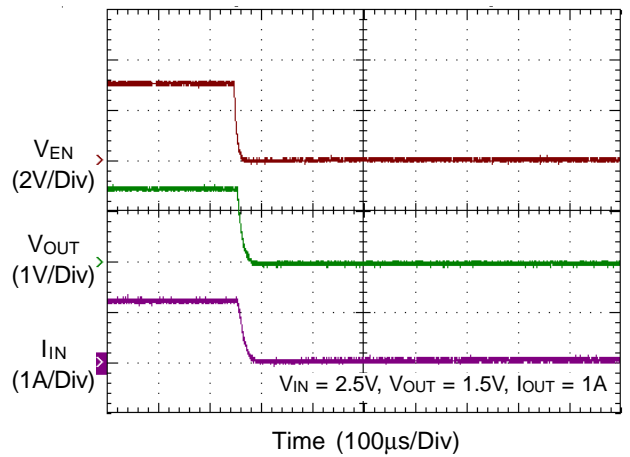
Line Transient Response



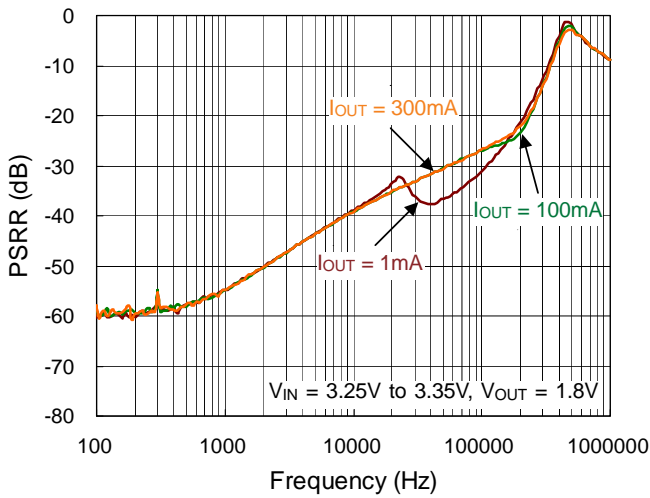
Power On from EN



Power Off from EN



PSRR vs. Frequency





## Application Information

The RT2517C is a low voltage, low dropout linear regulator with an external bias supply input capable of supporting an input voltage range from 2.2V to 6V and adjustable output voltage from 1.2V to  $(V_{IN} - V_{DROP})$ .

### Output Voltage Setting

The RT2517C output voltage is adjustable via the external resistive voltage divider. The output voltage is set according to the following equation :

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

For ADJ pin noise immunity, the resistive divider total value of R1 and R2 are suggested not over 100kΩ, where  $V_{ADJ}$  is the reference voltage with a typical value of 1.2V.

### Feed-Forward Capacitor ( $C_{FF}$ )

The RT2517C is designed to be stable without the external feed-forward capacitor ( $C_{FF}$ ). However, an external feedforward capacitor between VOUT and ADJ pin is often adopted to optimizes the transient, noise, and PSRR performance. Regarding to the resistance value of the voltage divider, the recommended  $C_{FF}$  values are as below :

$C_{FF} = 1\text{nF}$ , for both R1 and R2 are larger than 1kΩ

$C_{FF} = 10\text{nF}$ , for both R1 and R2 are smaller than 1kΩ

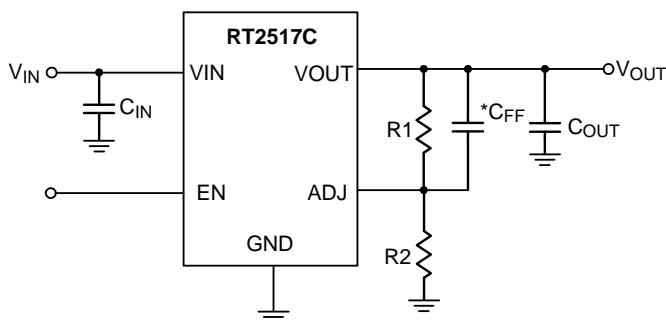


Figure 2. Application Circuit with  $C_{FF}$

### Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage  $V_{DROP}$  also can be expressed as the voltage drop on the pass-FET at specific output current ( $I_{RATED}$ ) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance  $R_{DS(ON)}$ . Thus the dropout voltage can be defined as  $(V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED})$ . For normal operation, the suggested LDO operating range is  $(V_{IN} > V_{OUT} + V_{DROP})$  for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade these performance severely.

### Chip Enable Operation

The RT2517C goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 10μA (max.). The EN pin can be directly tied to VIN to keep the part on.

### Current Limit

The RT2517C contains an independent current limit circuitry, which controls the pass transistor's gate voltage, limiting the output current to 1.6A (typ.).

### $C_{IN}$ and $C_{OUT}$ Selection

The RT2517C is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance range from 10μF to 47μF on the RT2517C output ensures stability.

Input capacitance is selected to minimize transient input droop during load current steps. For general application, the requirement of input capacitor with a 10μF is recommended to minimize input impedance and provide the desired effect and do not affect stability.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC

package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For VDFN-8AL 3x3 package, the thermal resistance,  $\theta_{JA}$ , is 30.2°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (30.2^\circ\text{C/W}) = 3.31\text{W for VDFN-8AL 3x3 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

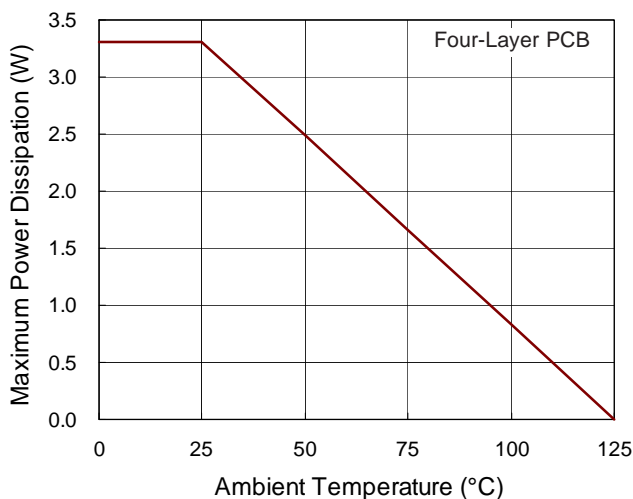
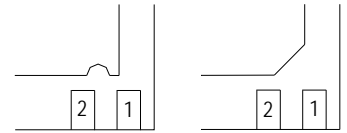
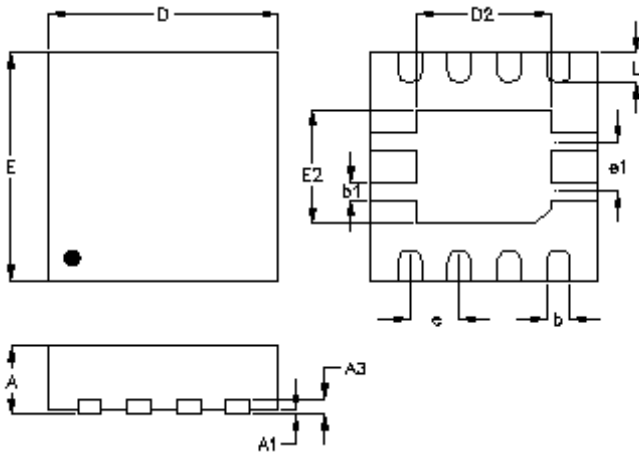


Figure 3. Derating Curve of Maximum Power Dissipation

**Outline Dimension**



**DETAILA**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.370	0.010	0.015
b1	0.230		0.009	
D	2.900	3.100	0.114	0.122
D2	1.700	1.800	0.067	0.071
E	2.900	3.100	0.114	0.122
E2	1.450	1.550	0.057	0.061
e	0.650		0.026	
e1	0.650		0.026	
L	0.350	0.450	0.014	0.018

**V-Type 8AL DFN 3x3 Package**

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