

3A Ultra-Low Dropout Linear Regulator with Power Good Indicator

1 General Description

The RT2534A/RT2534B is an ultra-low-dropout (LDO) linear regulator capable of operating with input voltages ranging from 0.8V to 5.5V and supplying up to 3A of output current. The output voltage of the RT2534A is adjustable from 0.8V to 3.6V, while that of the RT2534B ranges from 0.6V to 3.6V. The VBIAS supply voltage ranges from 2.7V to 5.5V, providing high-efficiency regulation in conditions where the output voltage is very close to the input voltage.

The RT2534A/RT2534B implements the EN and PG pins not only for system sequencing but also to indicate the status of the output voltage. This device features reverse-current protection to prevent chip damage during rapid input power-off events. It also integrates input undervoltage-lockout (UVLO), overcurrent protection (OCP), and over-temperature protection (OTP) to prevent fault conditions.

The RT2534A/RT2534B is available in the WDFN-10L 3x3 package that features high thermal conductivity. The device is fully specified for operation over the temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C .

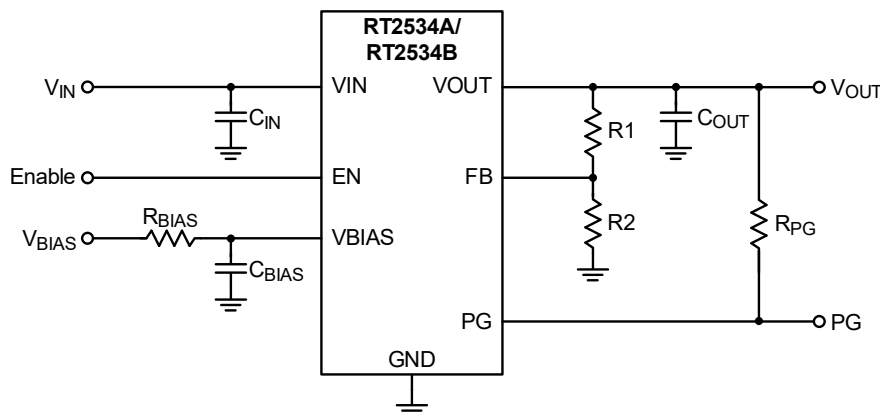
2 Features

- Ultra-Low V_{IN} Range: 0.8V to 5.5V
- VBIAS Voltage Range: 2.7V to 5.5V
- VOUT Voltage Range:
 - RT2534A: 0.8V to 3.6V
 - RT2534B: 0.6V to 3.6V
- Low Dropout: 180mV Typical at 3A, $V_{BIAS} = 5V$
- 1% Output Voltage Accuracy
- Power-Good Indicator for Easy Sequence Control
- Reverse-Current Protection
- Output Discharge
- Stable with Any Output Capacitor $\geq 2.2\mu\text{F}$
- Overcurrent and Over-Temperature Protections
- Available in WDFN-10L 3x3 Package

3 Applications

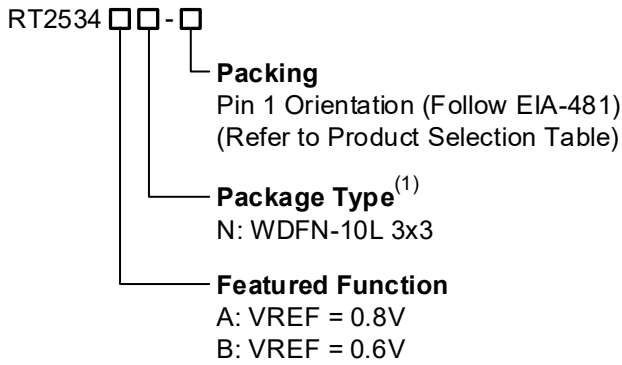
- Desktop & Notebook PCs
- Graphic Cards
- Network & Storage
- SMPS Post Regulators

4 Simplified Application Circuit



5 Ordering Information

5.1 Product Number Information



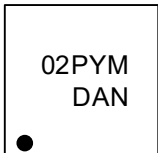
5.2 Product Selection Table

Orderable Product Number	Output Voltage	VREF	Package ⁽¹⁾	Pin 1 Quadrant
RT2534AN-A	0.8V to 3.6V (Adjustable)	0.8V	WDFN-10L 3x3	Q1
RT2534BN-A	0.6V to 3.6V (Adjustable)	0.6V		Q1

Note 1. Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

RT2534AN-A



02P: Product Code
 YMDAN: Date Code

RT2534BN-A

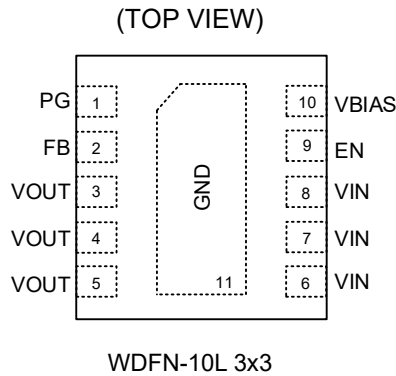


035: Product Code
 YMDAN: Date Code

Table of Contents

1	General Description	1	18	Application Information	18
2	Features	1	18.1	Dropout Voltage	18
3	Applications	1	18.2	Input, Output, and Bias Capacitor Selection	18
4	Simplified Application Circuit	1		18	
5	Ordering Information	2	18.3	Adjustable Output Voltage	18
	5.1 Product Number Information	2	18.4	Power-Up Sequence Requirement	18
	5.2 Product Selection Table.....	2	18.5	Thermal Considerations.....	18
6	Marking Information	2	18.6	Layout Considerations	19
7	Pin Configuration	4	19	Outline Dimension	21
8	Functional Pin Description	4	20	Footprint Information	22
9	Functional Block Diagram	5	21	Packing Information	23
10	Absolute Maximum Ratings	6	21.1	Tape and Reel Data	23
11	ESD Ratings	6	21.2	Tape and Reel Packing.....	24
12	Recommended Operating Conditions	6	21.3	Packing Material Anti-ESD Property	25
13	Thermal Information	7	22	Datasheet Revision History	26
14	Electrical Characteristics	7			
	14.1 System Characteristics	9			
15	Typical Application Circuit	10			
	15.1 Application Circuit	10			
	15.2 Recommended Components.....	11			
16	Typical Operating Characteristics	12			
17	Operation	15			
	17.1 VIN and VBIAS Supply.....	15			
	17.2 Undervoltage Lockout (UVLO)	15			
	17.3 Enable and Shutdown	16			
	17.4 Power-Good Indicator	16			
	17.5 Output Active Discharge.....	16			
	17.6 Reverse-Current Protection.....	16			
	17.7 Overcurrent Protection (OCP)				
	and Short-Circuit Protection (SCP)	17			
	17.8 Over-Temperature Protection (OTP)	17			

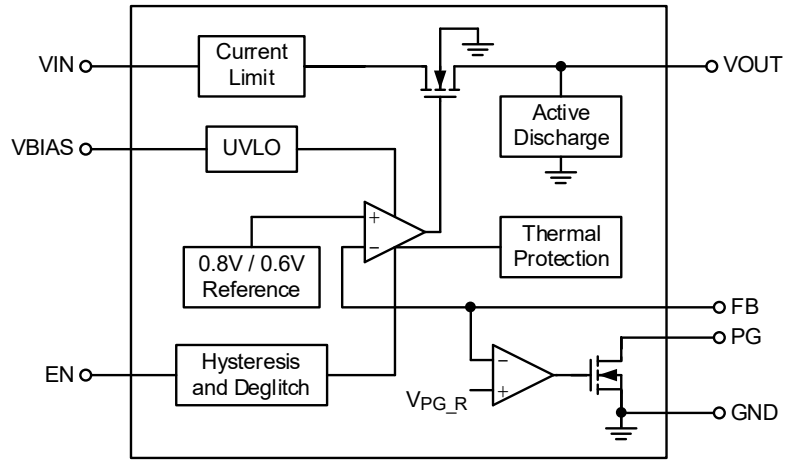
7 Pin Configuration



8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PG	Power-good indicator. This open-drain output pin is pulled high when the FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during soft-start period.
2	FB	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical) for the RT2534AN, and 0.6V for the RT2534BN. Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
3, 4, 5	VOUT	LDO output pin. Connect a ceramic capacitor with an effective capacitance of at least 2.2 μ F as close as possible to this pin and GND to minimize the output impedance.
6, 7, 8	VIN	Supply voltage input. The input voltage range is from 0.8V to 5.5V. Connect a ceramic capacitor with an effective capacitance of at least 1 μ F as close as possible from this pin to GND to minimize the input impedance
9	EN	Enable control input. A logic-high enables the regulator, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail and connect this pin to the external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
10	VBIAS	Bias supply voltage input. The input voltage range is from 2.7V to 5.5V. Connect a ceramic capacitor with an effective capacitance of at least 0.1 μ F as close as possible from this pin to GND if the external power rail can be used. For applications where an auxiliary bias voltage is not available or a low dropout voltage is not required, the VBIAS pin can be connected to the VIN pin with an effective capacitance of at least 4.7 μ F for optimal performance.
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB copper area for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN
 - DC----- -0.3V to 6.5V
 - < 200ns----- -0.3V to 7V
- BIAS Input Voltage, VBIAS
 - DC----- -0.3V to 6.5V
 - < 200ns----- -0.3V to 7V
- Other Pins ----- -0.3V to 6V
- Output Voltage, VOUT ----- -0.3V to 6.3V
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
 - HBM (Human Body Model)----- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ----- 0.8V to 5.5V
- BIAS Input Voltage, VBIAS----- 2.7V to 5.5V
- Output Voltage, VOUT (RT2534AN)----- 0.8V to 3.6V
- Output Voltage, VOUT (RT2534BN)----- 0.6V to 3.6V
- Junction Temperature Range----- -40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

([Note 5](#) and [Note 6](#))

Thermal Parameter		WDFN-10L 3x3	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	60.43	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	62.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	11.7	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	41.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board with dimensions of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

($V_{IN} = V_{OUT} + 0.3V$, $V_{BIAS} = 5V$, $V_{EN} = 1.1V$, $C_{BIAS} = 0.1\mu F$, $C_{IN} = C_{OUT} = 10\mu F$, $I_{OUT} = 50mA$, $T_A = 25^\circ C$.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range and Operating Current						
VIN Supply Input Voltage	V_{IN}		$V_{OUT} + V_{DROP}$	--	5.5	V
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	--	0.8	--	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	--	0.4	--	V
VBIAS Pin Voltage	V_{BIAS}		2.7	--	5.5	V
VBIAS Undervoltage Lockout Rising Threshold	$V_{UVLO_VBIAS_R}$	V_{BIAS} rising	2.5	2.7	2.9	V
VBIAS Undervoltage-Lockout Hysteresis	$V_{UVLO_VBIAS_HYS}$	Hysteresis	--	0.25	--	V
VBIAS Pin Quiescent Current	I_{BIAS_Q}		--	1	2	mA
VBIAS Pin Shutdown Current	I_{BIAS_SHDN}	$V_{EN} = 0.4V$	--	--	1	μA
EN Input Voltage Rising Threshold	V_{EN_R}	Logic-high	1.1	--	5.5	V
EN Input Voltage Falling Threshold	V_{EN_F}	Logic-low	0	--	0.7	
EN Threshold Hysteresis	V_{EN_HYS}		--	100	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Current	I _{EN}	V _{EN} = 5V	--	0.1	1	μA
EN Delay Time	t _{EN_DLY}	From EN high to V _{OUT} x 10%	--	250	--	μs
EN Deglitch Time	t _{EN_DG}		--	20	--	μs
Output Operation						
Output Voltage	V _{OUT}	V _{IN} = 5V, I _{OUT} = 3A	V _{REF}	--	3.6	V
Output Voltage Accuracy (Note 7)	V _{OUT_ACC}	2.97V ≤ V _{BIAS} ≤ 5.5V, 50mA ≤ I _{OUT} ≤ 3A	-1	--	1	%
Reference Voltage	V _{REF}	For RT2534A	--	0.8	--	V
		For RT2534B	--	0.6	--	
FB Pin Current	I _{FB}		-1	0.15	1	μA
Line Regulation	V _{LINE_REG}	V _{OUT(Normal)} + 0.3 ≤ V _{IN} ≤ 5.5V	--	0.03	--	%/V
Load Regulation	V _{LOAD_REG}	50mA ≤ I _{OUT} ≤ 3A	--	0.09	--	%/A
V _{IN} Dropout Voltage	V _{DROP_VIN}	I _{OUT} = 3A, V _{BIAS} = 5V, V _{IN} = V _{OUT(Normal)} - 100mV	--	180	270	mV
V _{BIAS} Dropout Voltage	V _{DROP_VBIAS}	I _{OUT} = 0.5A, V _{IN} = V _{BIAS}	--	--	1.2	V
		I _{OUT} = 1A, V _{IN} = V _{BIAS}	--	--	1.35	V
		I _{OUT} = 2A, V _{IN} = V _{BIAS}	--	--	1.55	V
		I _{OUT} = 3A, V _{IN} = V _{BIAS}	--	--	1.75	V
Current Limit (Note 8)	I _{LIM}	V _{OUT} decrease to 80% x V _{OUT}	2.9	3.45	4	A
Short-Circuit Current Limit	I _{SC}	Under foldback operation	--	0.65	--	A
Soft-Start Time	t _{SS}		--	1.7	--	ms
Discharge Resistor	R _{DISCHG}	V _{DIS} = 0.5V	--	90	--	Ω
Power-Good						
Power-Good Voltage Rising Threshold	V _{PG_R}	Threshold, V _{PG} from low to high	--	94	--	%V _{OUT}
Power-Good Voltage Hysteresis	V _{PG_HYS}	Hysteresis, V _{PG} from high to low	--	9.5	--	%V _{OUT}
Power-Good Rising Delay Time	t _{PG_R}	From V _{PG_R} to PG high	--	380	--	μs
PG Pin Low-Level Output Voltage	V _{PG_L}	I _{PG} = 1mA (Sinking), V _{OUT} < V _{PG}	--	--	0.3	V
PG Pin Leakage Current	I _{PG_LK}	V _{PG} = 5.25V, V _{OUT} > V _{PG}	--	0.1	--	μA

Note 7. The external resistor tolerance is not taken into account.

Note 8. OCP threshold level is not guaranteed to function outside its linear region.

14.1 System Characteristics

(The following specifications are guaranteed by design and are not performed in production testing. ($V_{IN} = V_{OUT} + 0.3V$, $V_{BIAS} = 5V$, $V_{EN} = 1.1V$, $C_{BIAS} = 0.1\mu F$, $C_{IN} = C_{OUT} = 10\mu F$, $I_{OUT} = 50mA$, $T_A = 25^\circ C$.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Power Supply Rejection Ratio (V_{IN} to V_{OUT})	PSRR	$f = 1kHz$, $V_{IN} = 1.8V$, $V_{OUT} = 1.5V$, $I_{OUT} = 1.5A$	--	50	--	dB	
		$f = 100kHz$, $V_{IN} = 1.8V$, $V_{OUT} = 1.5V$, $I_{OUT} = 1.5A$	--	20	--		
Power Supply Rejection Ratio (V_{BIAS} to V_{OUT})		$f = 1kHz$, $V_{IN} = 1.8V$, $V_{OUT} = 1.5V$, $I_{OUT} = 1.5A$	--	50	--	dB	
		$f = 100kHz$, $V_{IN} = 1.8V$, $V_{OUT} = 1.5V$, $I_{OUT} = 1.5A$	--	50	--		
Output Noise Voltage	V_n	$f = 100Hz$ to $100kHz$, $I_{OUT} = 1.5A$	RT2534A	--	25 x V_{OUT}	--	μV_{RMS}
			RT2534B	--	33.3 x V_{OUT}	--	
Over-Temperature Protection Threshold	T_{OTP}	Threshold	--	140	--	$^\circ C$	
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Hysteresis	--	20	--		

15 Typical Application Circuit

15.1 Application Circuit

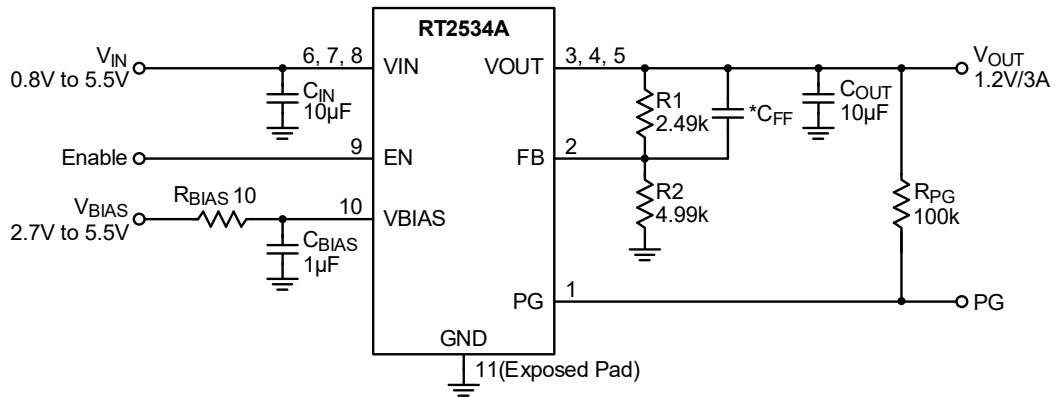


Figure 1. Configuration Circuit for VREF = 0.8V

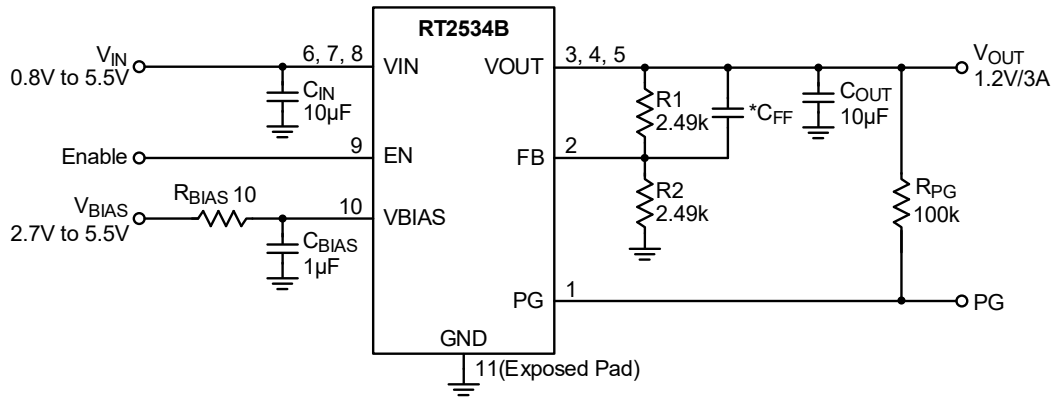


Figure 2. Configuration Circuit for VREF = 0.6V

*: The feedforward capacitor (C_{FF}) is optional for the transient response and circuit stability improvement.

15.2 Recommended Components

Table 1. Recommended Feedback-Resistor Values for VREF = 0.8V

Output Voltage (V)	External Resistor Divider Combination	
	R1 (Ω)	R2 (Ω)
0.8	Short	Open
0.9	0.619k	4.99k
1	1.13k	4.52k
1.05	1.37k	4.42k
1.1	1.87k	4.99k
1.2	2.49k	4.99k
1.5	4.12k	4.75k
1.8	3.57k	2.87k
2.5	3.57k	1.69k
3.3	3.57k	1.15k

Table 2. Recommended Feedback-Resistor Values for VREF = 0.6V

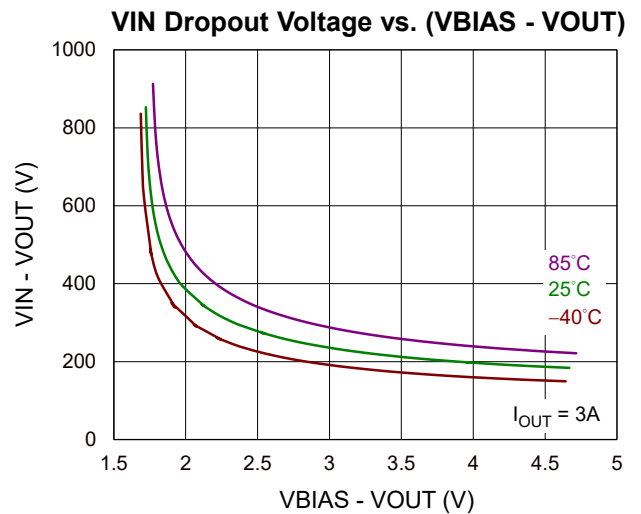
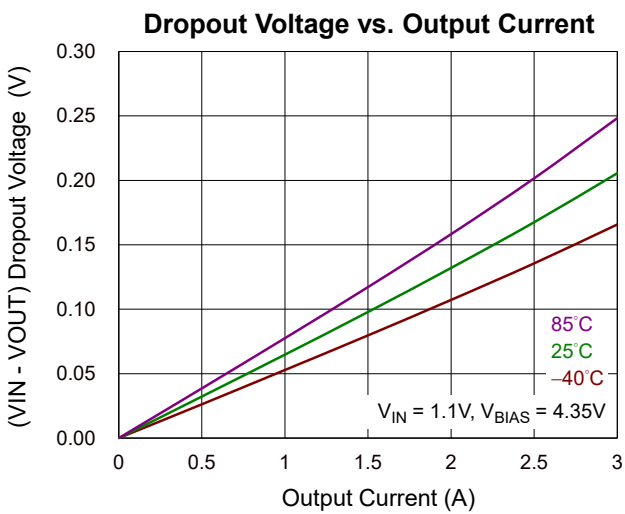
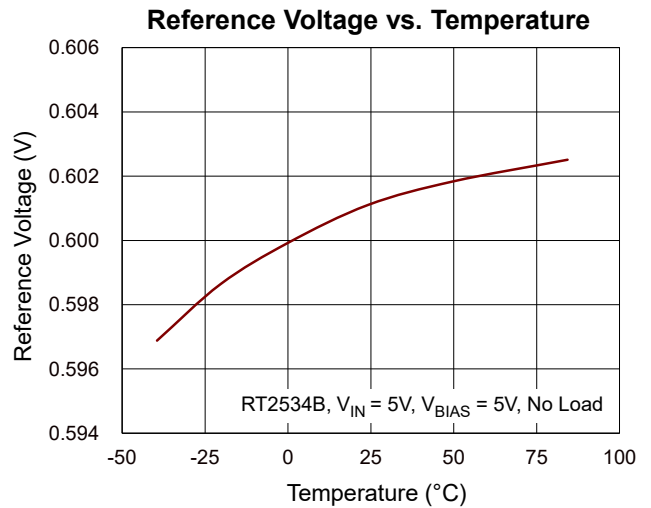
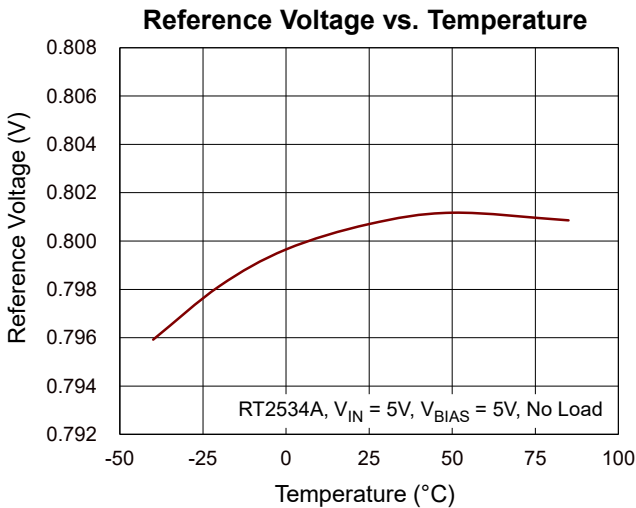
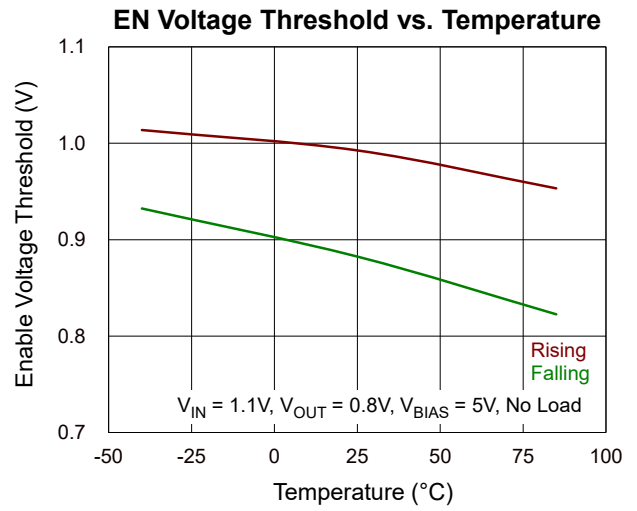
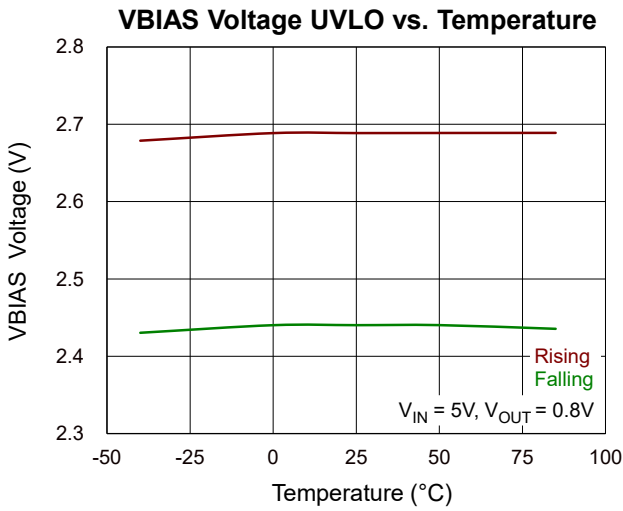
Output Voltage (V)	External Resistor Divider Combination	
	R1 (Ω)	R2 (Ω)
0.6	Short	Open
0.9	0.619k	1.24k
1	1.13k	1.69k
1.05	1.37k	1.82k
1.1	1.87k	2.26k
1.2	2.49k	2.49k
1.5	4.12k	2.74k
1.8	3.57k	1.78k
2.5	3.57k	1.13k
3.3	3.57k	0.787k

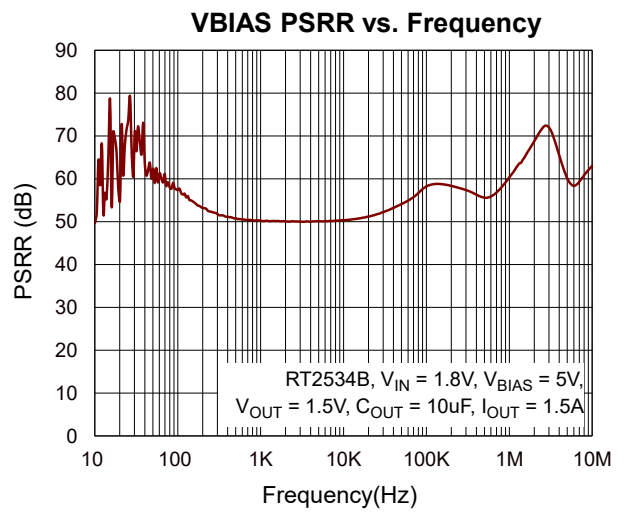
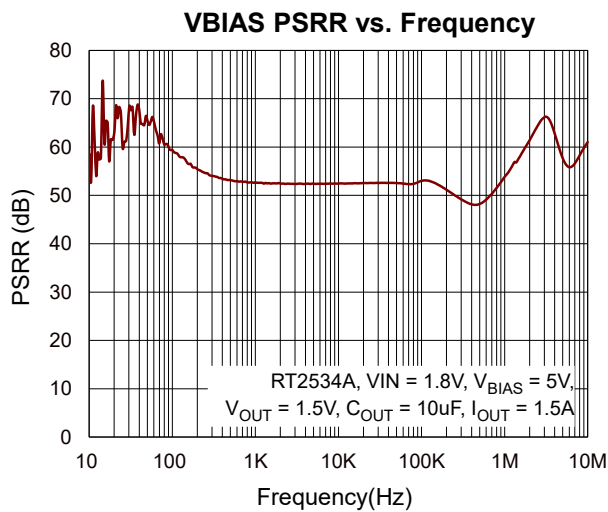
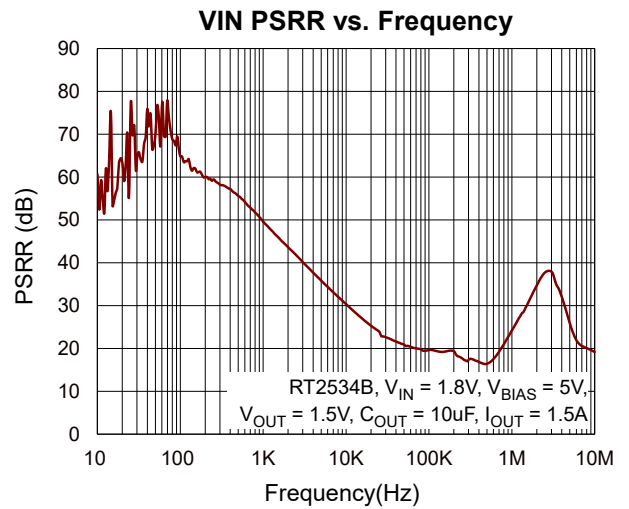
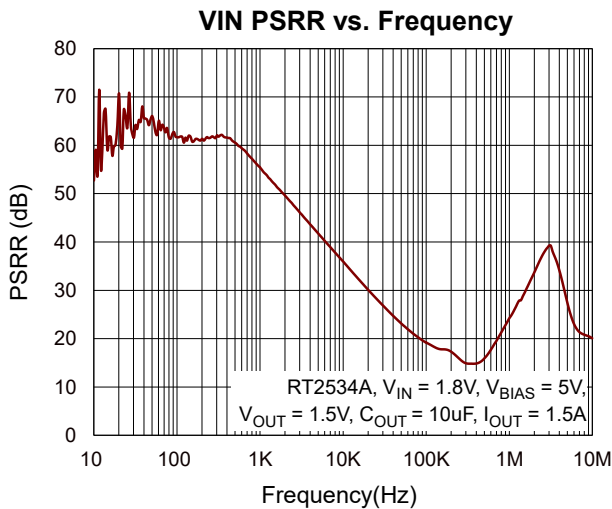
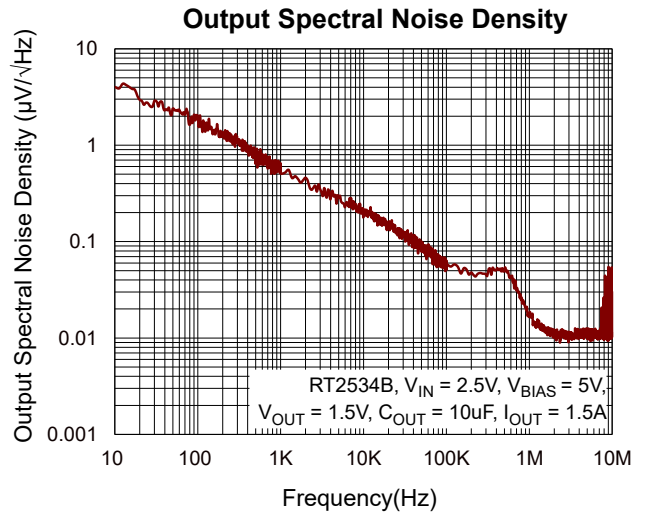
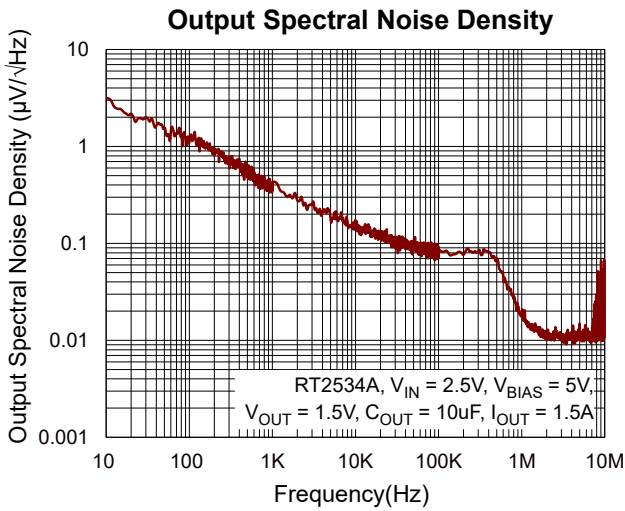
Table 3. Recommended External Components

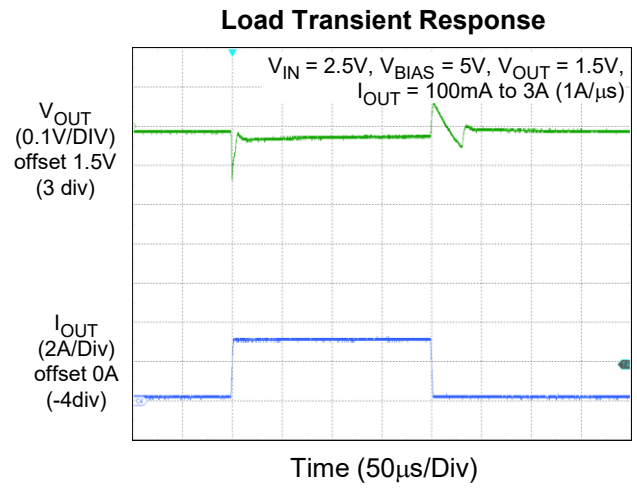
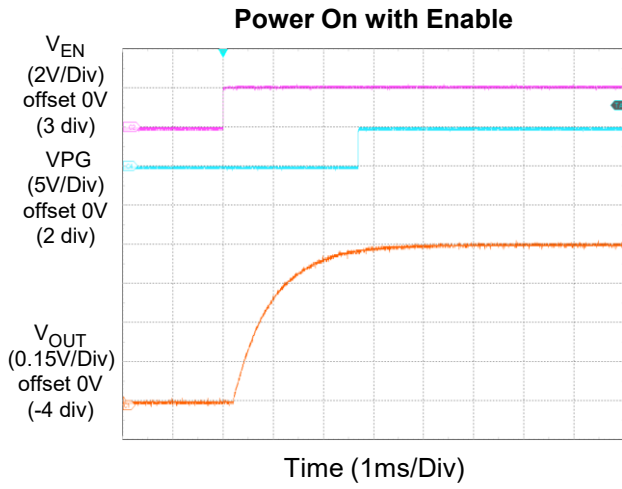
Reference	Qty	Part Number	Description	Package	Manufacture
IC	1	RT2534A/RT2534B	Linear Regulator	WDFN-10L 3x3	RICHTEK
C _{IN} , C _{OUT} (Note 9)	1	GRM21BR61C106ME15	10μF/16V/X5R	C-0805	MURATA
C _{BIAS}	1	GCJ188R71H104KA12	0.1μF/50V/X7R	C-0603	MURATA

Note 9. Considering the effective capacitance derated with biased voltage level, the C_{OUT} component needs satisfy the effective capacitance at least 2.2μF or above at targeted output level for stable and normal operation.

16 Typical Operating Characteristics







17 Operation

The RT2534A/RT2534B is a very low dropout linear regulator that operates from an input voltage as low as 0.8V. It provides a highly accurate output that is capable of supplying 3A of output current with a typical dropout voltage of only 180mV. The output voltage range of RT2534A is from 0.8V to 3.6V, and RT2534B is from 0.6V to 3.6V.

17.1 VIN and VBIAS Supply

The VBIAS input supplies the internal reference and LDO circuitry while all output current comes directly from the VIN input for high efficiency regulation. With an external VBIAS 3.25V above VOUT, the RT2534A/RT2534B offers very low dropout performance (180mV typical at 3A), which allows the device to be used in place of a DC-DC converter and still achieves good efficiency. This helps designers to achieve the smallest, simplest, and lowest-cost solution. In addition, the VBIAS pin must include a series R/C filter to prevent inductive noise from entering the internal IC circuitry.

For applications where an auxiliary bias voltage is not available or low dropout is not required. VBIAS is suggested to be 1.75V above VOUT and attention to power rating and thermal management is needed.

17.2 Undervoltage Lockout (UVLO)

The RT2534A/RT2534B implements undervoltage lockout (UVLO) circuitry on both the VIN and VBIAS pins to prevent operation under insufficient input voltage. The device constantly monitors these inputs, and will only enable normal operation when both voltages remain above their respective UVLO threshold levels. If either VIN or VBIAS drops below its falling UVLO threshold, the control loop is disabled and output regulation ceases, resulting in VOUT dropping. [Figure 3](#) illustrates the internal UVLO circuit's response to four different input voltage events (duration a, b, c and d), assuming the EN pin voltage remains above the logic-high threshold voltage (V_{EN_R}) at all times. During duration "a", VBIAS is above its UVLO threshold; however, VOUT remains disabled because VIN is below its UVLO threshold voltage. During duration "b", as VIN starts to rise, VOUT begins to ramp up after VIN exceeds the UVLO rising threshold voltage. Then VOUT reaches the target level with the internal fixed soft-start time and remains in regulation. During duration "c", there is a voltage drop in the power line, but it does not fall below the UVLO falling threshold. The device continues normal operation, and VOUT stays in regulation. In duration "d", VIN drops below the UVLO falling threshold, causing the control loop to be disabled and regulation to cease. Consequently, VOUT also drops.

In general applications, the instantaneous power line transients at the VIN pin will become worse due to longer power traces. As illustrated during duration "d", it leads to a collapse of VOUT. To effectively enhance input power stabilization, it is recommended to add additional input capacitance or to improve the input trace layout on the PCB.

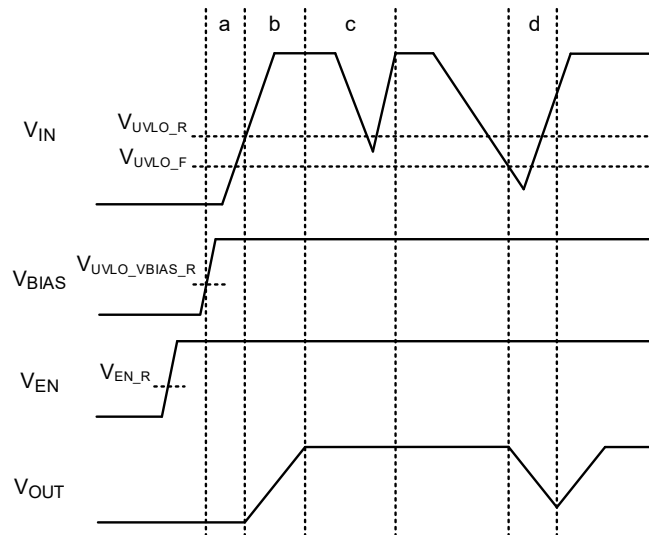


Figure 3. Undervoltage Lockout Trigger Conditions and Output Variation

17.3 Enable and Shutdown

The EN pin is active high. Applying a voltage above 1.1V ensures the LDO regulator turns on, while the regulator turns off if the VEN falls below 0.7V. The enable circuitry has a typical 50mV hysteresis and deglitching for use with relatively slow ramping analog signals. That helps to avoid on-off cycling resulting from small glitches in the VEN signal. A fast rise-time signal must be used to enable the RT2534A/RT2534B if precise turn-on timing is required. If not used, EN can be connected to either VIN or VBIAS. If EN is connected to VIN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

17.4 Power-Good Indicator

When the output voltage is greater than VPG_R, the output voltage is considered good, and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. If VOUT drops below VPG or if VBIAS drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled, or when OCP or OTP is triggered.

17.5 Output Active Discharge

The RT2534A/RT2534B implements an output discharge function that quickly discharges the output capacitor through an internal 90Ω (typical) discharge resistor connected from this pin to GND. This function is activated when the RT2534A/RT2534B is disabled.

17.6 Reverse-Current Protection

In general applications, reverse current may occur if the output is biased above the input supply voltage level or if the input supply experiences an instantaneous drop during light load operation, resulting in VIN being less than VOUT. In such situations, if VOUT exceeds VIN by more than the body diode's forward voltage in the internal pass element, reverse current may flow and may cause long-term device damage.

To address this, the RT2534A/RT2534B incorporates reverse-current protection to prevent the IC from unexpected damage without the need for an external Schottky diode.

17.7 Overcurrent Protection (OCP) and Short-Circuit Protection (SCP)

The RT2534A/RT2534B provides overcurrent protection (OCP) and short-circuit protection (SCP) to prevent the IC from catastrophic damage under conditions of output overcurrent or short-circuit. This is achieved by continuously monitoring the output current. While the internal current limit circuitry is designed to inhibit the operation beyond the rated current, persistent operation above this threshold may compromise the reliability of the RT2534A/RT2534B.

During current limiting, the output voltage drops as the load impedance decreases, eventually triggering thermal shutdown due to excessive power dissipation. Once the OCP or SCP conditions are removed, the RT2534A/RT2534B feedback or output voltage will return to the regulation setpoint, resuming normal operation.

17.8 Over-Temperature Protection (OTP)

The RT2534A/RT2534B includes over-temperature protection (OTP) circuitry to prevent overheating conditions. When the junction temperature exceeds the thermal shutdown threshold (T_{OTP}), the RT2534A/RT2534B is disabled and will resume normal operation automatically once the junction temperature cools down by thermal shutdown hysteresis (T_{OTP_HYS}). Additionally, continuous operation into thermal shutdown or at a junction temperature above 125°C may reduce the reliability of the RT2534A/RT2534B.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. This protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and should not be relied upon for normal operation. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or cause permanent damage to the device.

18 Application Information

([Note 10](#))

The RT2534A/RT2534B is a low dropout regulator that features soft-start capability. It provides EN and PG for easy system sequence control, and built-in overcurrent and over-temperature protection for safe operation.

18.1 Dropout Voltage

Because of two power supply inputs, VIN and VBIAS, and one VOUT regulator output, there are two specified dropout voltages. The first is the VIN dropout voltage, which is the voltage difference (VIN – VOUT) when VOUT starts to decrease by percentage specified in the [Electrical Characteristics](#) table.

The second, is the VBIAS dropout voltage, which is the voltage difference (VBIAS - VOUT) when the VIN and VBIAS pins are joined together and VOUT starts to decrease. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. In these applications, VBIAS is suggested to be 1.4V above VOUT and attention to power rating and thermal considerations is needed.

18.2 Input, Output, and Bias Capacitor Selection

The device is designed to be stable for all available types and values of output capacitors $\geq 2.2\mu\text{F}$. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the VIN and VBIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for VIN is $1\mu\text{F}$ and the minimum recommended capacitor for VBIAS is $0.1\mu\text{F}$. If VIN and VBIAS are connected to the same supply, the recommended minimum capacitor for VBIAS is $4.7\mu\text{F}$. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close to the pins as possible for optimum performance.

18.3 Adjustable Output Voltage

The output voltage of the RT2534A is adjustable from 0.8V to 3.6V, and RT2534B is adjustable from 0.6V to 3.6V. By using external voltage divider resistors as shown in [Typical Application Circuit](#), R1 and R2 can be calculated to set the desired output voltage. To achieve the maximum accuracy specifications, R2 should be $\leq 4.99\text{k}\Omega$.

18.4 Power-Up Sequence Requirement

The RT2534A/RT2534B supports powering on the input VIN, VBIAS, and EN pins in any order without damaging the device. Generally, connecting the EN and VIN pins for most applications is acceptable, as long as VIN and VEN are greater than the EN threshold (minimum 1.1V) and the input ramp rate of VIN and VBIAS is faster than the output settled soft-start ramp rate. If the VIN/VBIAS input source ramp rate is slower than the output settled soft-start time, the output will track the input supply ramp-up level minus the dropout voltage until it reaches the settled output voltage level. For the other case, if EN is connected with the VBIAS pin, and the provided VIN is present before VBIAS, the output soft-start will proceed as programmed. If VBIAS and VEN are present before VIN is applied and the settled soft-start time has expired, then VOUT tracks the VIN ramp-up. If the soft-start time has not expired, the output tracks the VIN ramp-up until the output reaches the value set by the charging soft-start capacitor.

18.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(\text{MAX})}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA(EVB)}$, is 41.5°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (41.5^\circ\text{C/W}) = 2.41\text{W for a WDFN-10L 3x3 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in [Figure 4](#) allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

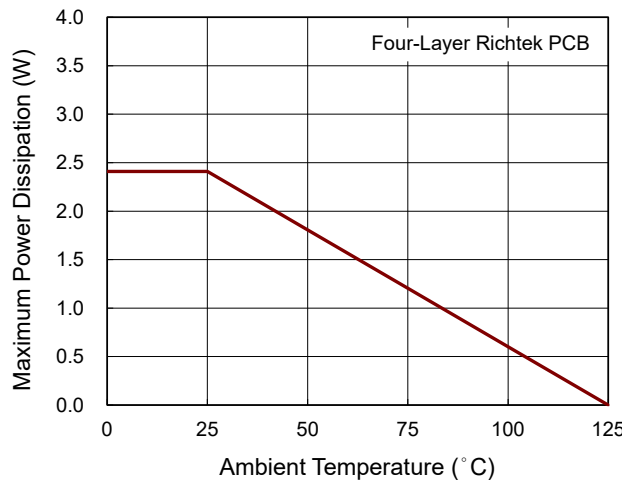


Figure 4. Derating Curves of Maximum Power Dissipation

18.6 Layout Considerations

For the best performance of the RT2534A/RT2534B, the following PCB layout suggestions are highly recommended:

- The input capacitor must be placed as close as possible to the IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connection.

[Figure 5](#) shows the examples for the layout references that help minimize inductive parasitic components, reduce load transients, and ensure good circuit stability.

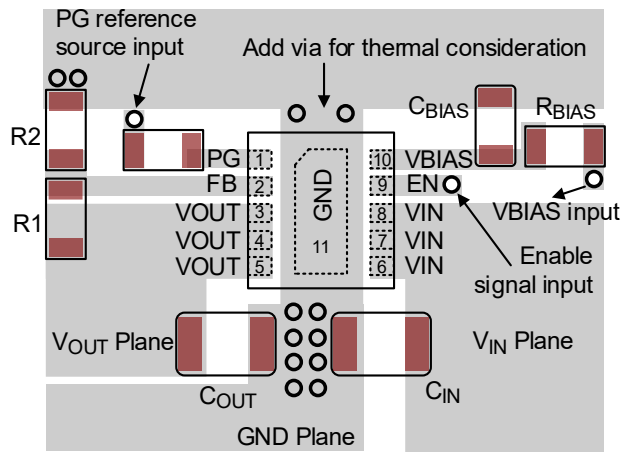
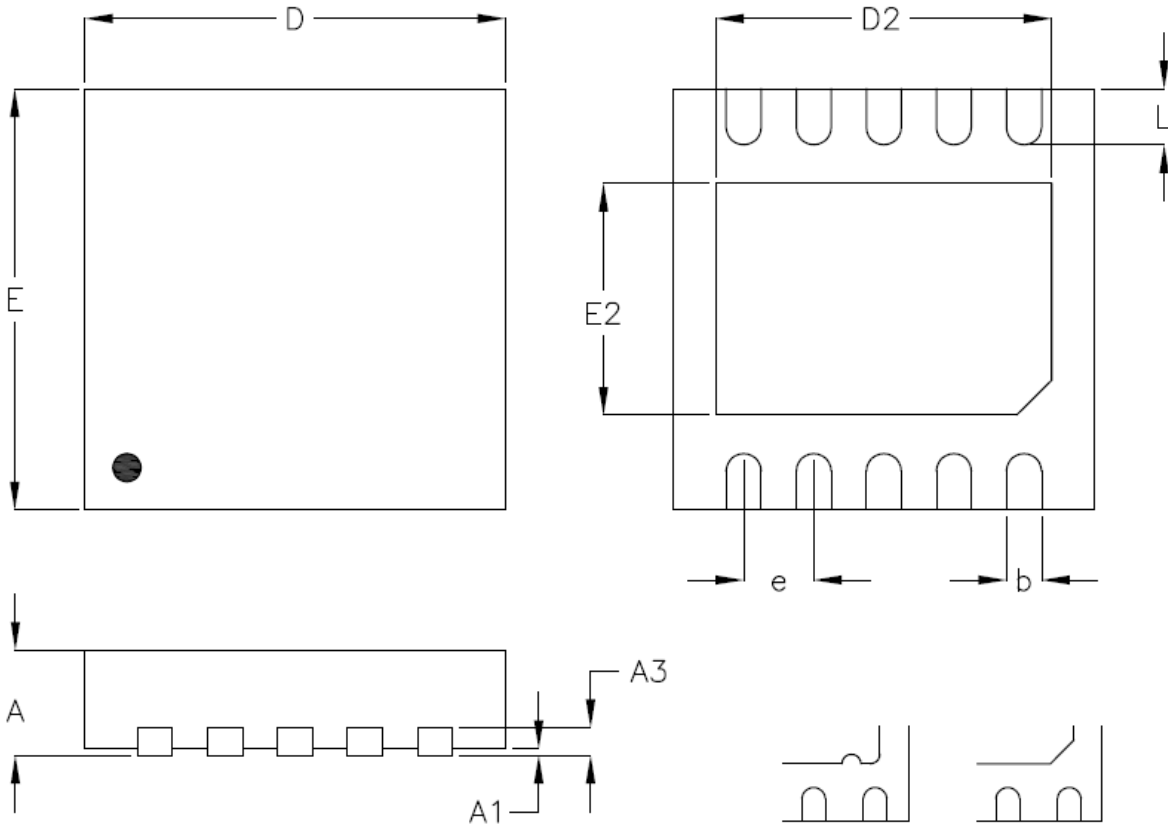


Figure 5. RT2534A/RT2534B PCB Layout Guide

Note 10. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension



DETAILA

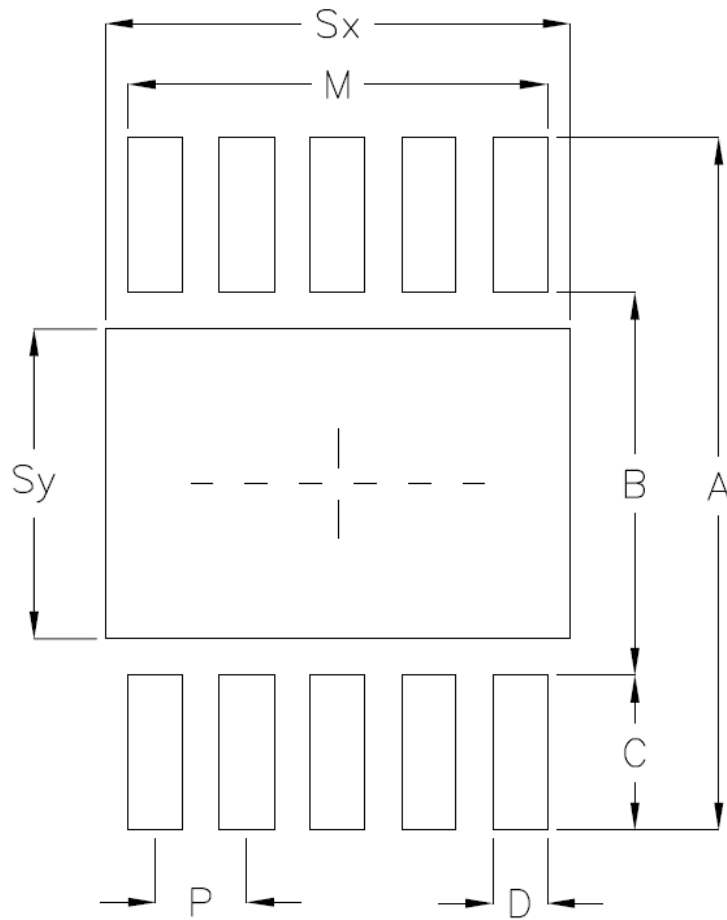
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

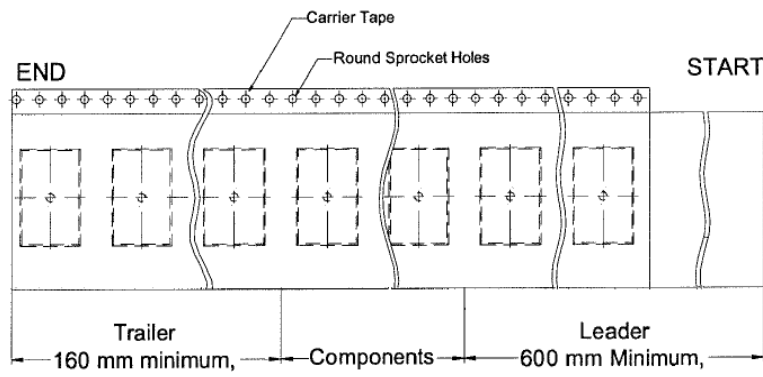
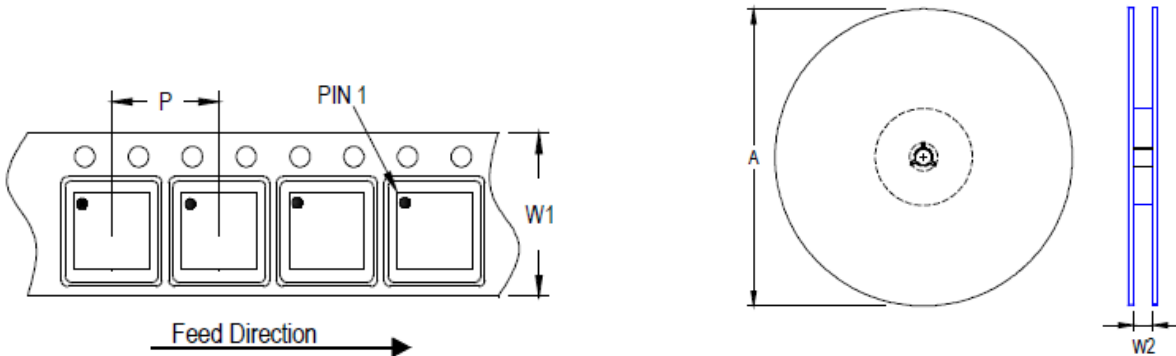
20 Footprint Information



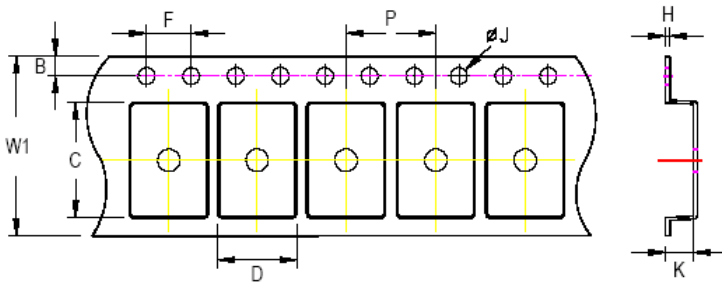
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

21 Packing Information

21.1 Tape and Reel Data









Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1		P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm	

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7"	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description
00	2026/3/13	First Edition