DDR Termination Regulator

General Description

RT2596 is a 1.5A continuous current sink/source tracking termination regulator, and its transient peak current is up to 3A. It is specifically designed for low-cost and low-external component count systems. The RT2596 possesses a high speed operating amplifier that provides fast load transient response. The RT2596 supports remote sensing functions and all features required to power the DDR SDRAM VTT bus termination according to the JEDEC specification. In addition, the RT2596 includes integrated sleep-state controls placing VTT in High-Z mode in $\overline{SD}$.

Features

- **Sink and Source Termination Regulator**
- **Remote Sensing**
- **PVIN, AVIN from 2.5V to 5.5V**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT2596□□

- Package Type
  - S : SOP-8
  - SP: SOP-8(Exposed Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

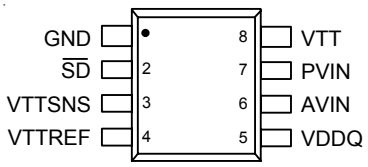
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

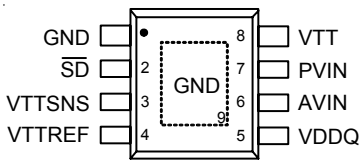
- Datacom & Enterprise Server
- Networking Communication
- Chipset/RAM Supply
- Generic DC/DC Power Regulator

Pin Configurations

(TOP VIEW)



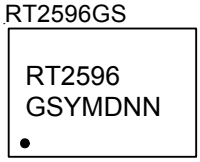
SOP-8



SOP-8 (Exposed Pad)

Marking Information

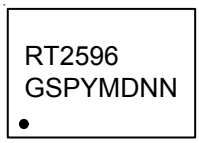
RT2596GS



RT2596GS : Product Number

YMDNN : Date Code

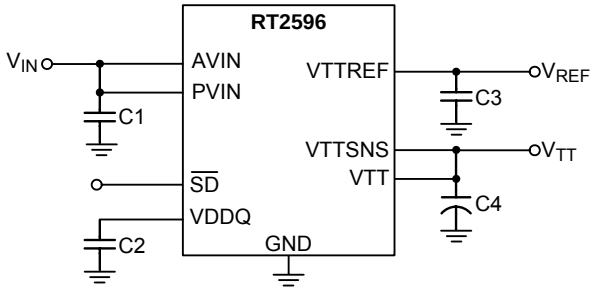
RT2596GSP



RT2596GSP : Product Number

YMDNN : Date Code

Simplified Application Circuit



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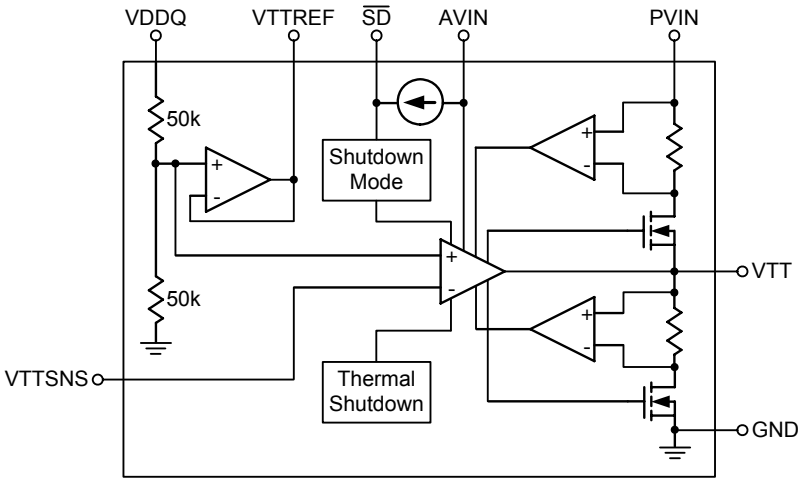
Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8	SOP-8 (Exposed Pad)		
1	1, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	2	$\overline{SD}$	Shutdown Control Input.
3	3	VTTSNS	Feedback Input for Regulating V_{TT}.
4	4	VTTREF	Buffered Internal Reference Voltage Equal to V_{DDQ} / 2.
5	5	VDDQ	Input for Internal Reference.
6	6	AVIN	Analog Input.
7	7	PVIN	Power Input.
8	8	VTT	Output of the Termination Regulator.

Function Block Diagram



Operation

Shutdown Mode

The shutdown mode can be controlled by the $\overline{SD}$ pin or thermal shutdown detector.

The shutdown mode will happen when the $\overline{SD}$ input voltage is under the logic threshold or junction temperature is over the thermal shutdown threshold.

The VTT pin will be high impedance and VREF will remain active under shutdown mode.

Thermal Shutdown

The regulator will enter shutdown mode when the junction temperature is over the thermal shutdown threshold.

VREF Buffer

The buffer senses the input voltage from VDDQ and provides an internal reference voltage of VDDQ / 2 for VTT regulator. The buffer remains active during shutdown mode.

VTT Regulator

The VTT output is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The output will be high impedance under shutdown mode.

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Absolute Maximum Ratings (Note 1)

- PVIN, AVIN, VDDQ, $\overline{SD}$ to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 ---------- 0.833W
  - SOP-8 (Exposed Pad) ---------- 2.13W
- Package Thermal Resistance (Note 2)
  - SOP-8, θ_{JA} ---------- 120°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- Junction Temperature ---------- 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- AVIN to GND ---------- 2.2V to 5.5V
- PVIN Supply Voltage ---------- 0V to AVIN
- $\overline{SD}$ Input Voltage ---------- 0V to AVIN
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 5), T_A = –40°C to 85°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VTTREF Output Voltage		V_{TTREF}	V_{IN} = V_{DDQ} = 2.3V	1.135	1.158	1.185	V
			V_{IN} = V_{DDQ} = 2.5V	1.235	1.258	1.285	
			V_{IN} = V_{DDQ} = 2.7V	1.335	1.358	1.385	
VREF Output Impedance		Z_{VREF}	I_{REF} = –30μA to 30μA	--	2.5	--	kΩ
VTT Output Voltage		V_{TT}	I_{OUT} = 0A, ±1.5A, V_{IN} = V_{DDQ} = 2.3V	1.125	1.159	1.19	V
			I_{OUT} = 0A, ±1.5A, V_{IN} = V_{DDQ} = 2.5V	1.225	1.259	1.29	
			I_{OUT} = 0A, ±1.5A, V_{IN} = V_{DDQ} = 2.7V	1.325	1.359	1.39	
VTTREF, VTT Output Offset		V_{TTTOL}	I_{OUT} = 0A	–20	0	20	mV
			I_{OUT} = –1.5A	–25	0	25	
			I_{OUT} = 1.5A	–25	0	25	
AVIN Quiescent Current		I_{Q_AVIN}	I_{OUT} = 0A	--	320	500	μA
VDDQ Input Impedance		Z_{VDDQ}	No Load	--	100	--	kΩ
AVIN Shutdown Current		I_{SHDN_AVIN}	$\overline{SD}$ = 0V	--	115	150	μA
$\overline{SD}$ Pin Leakage Current		I_{SHDNLK}	$\overline{SD}$ = 0V	--	2	5	μA
$\overline{SD}$ Input Voltage	Logic-High	V_{IH}		1.9	--	--	V
	Logic-Low	V_{IL}		--	--	0.8	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VTT Leakage Current	I_{ILK}	$\overline{SD}$ = 0V, V_{TT} = 1.25V	--	1	10	μA
VTTSNS Input Current	I_{VTTSNS}		--	13	--	nA
Thermal Shutdown Protection	T_{SD}	(Note 6)	--	165	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	(Note 6)	--	10	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection (air flow = 0 ft/min) at T_A = 25°C on a highly thermal conductive four-layer test board of JEDEC 51-7 thermal measurement standard. The test board size is 75.6mm x 114.3mm (3"x4.5") with 1.6mm thickness FR4 refer to JEDEC 51 standard. The test board exist four-layer copper, 2oz. (0.07mm) thickness. The case point of θ_{JC} is on the expose pad for SOP-8 (Exposed Pad) package.

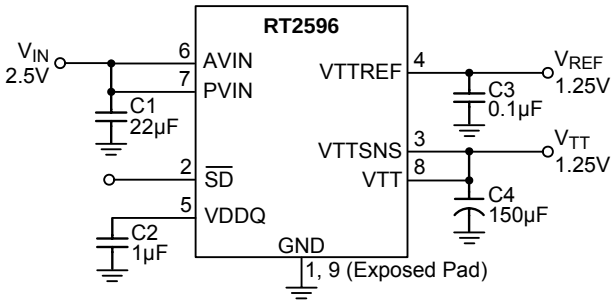
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. V_{IN} is defined as V_{IN} = AVIN = PVIN

Note 6. Guaranteed by design. No production test.

Typical Application Circuit



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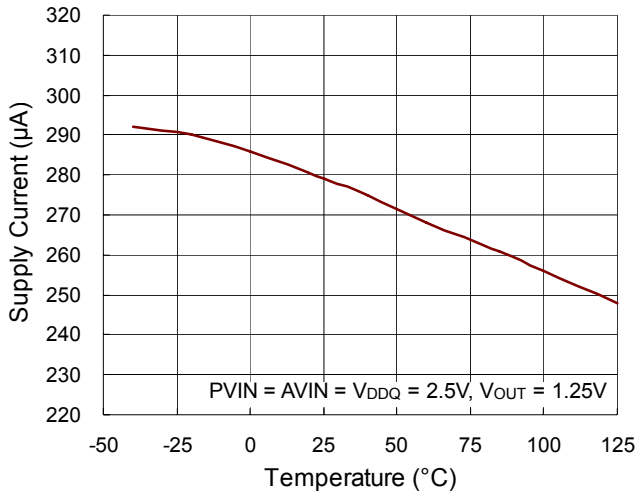
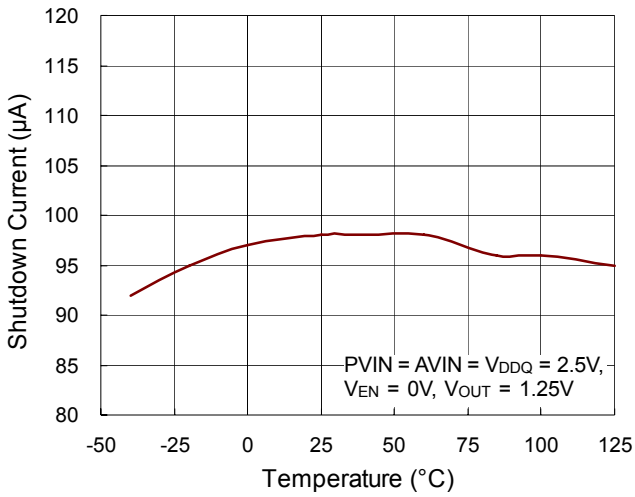
Typical Operating Characteristics

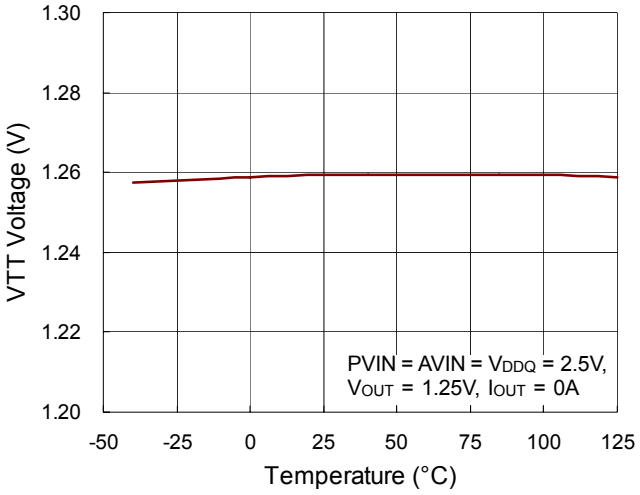
Supply Current vs. Temperature



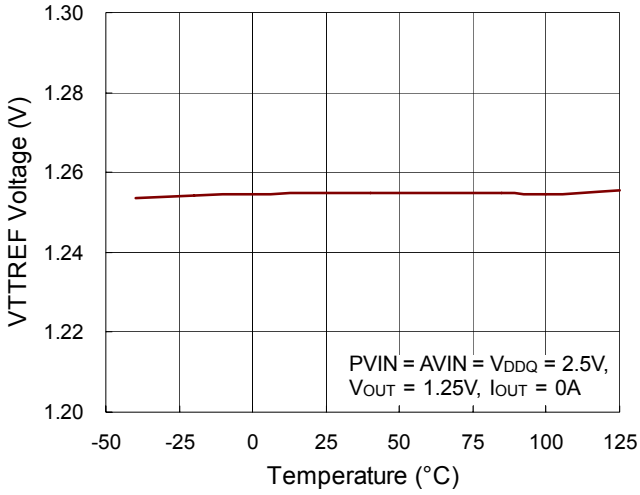
Shutdown Current vs. Temperature



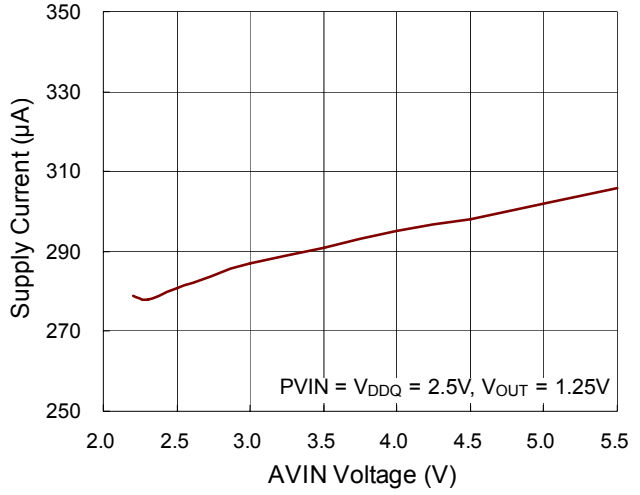
VTT Voltage vs. Temperature



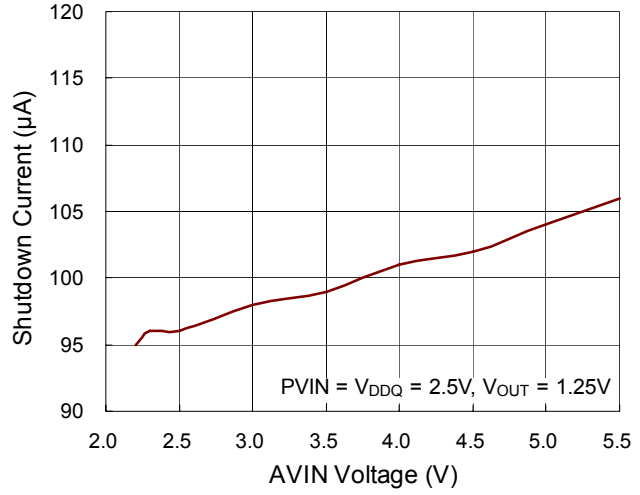
VTTREF Voltage vs. Temperature



Supply Current vs. AVIN Voltage



Shutdown Current vs. AVIN Voltage



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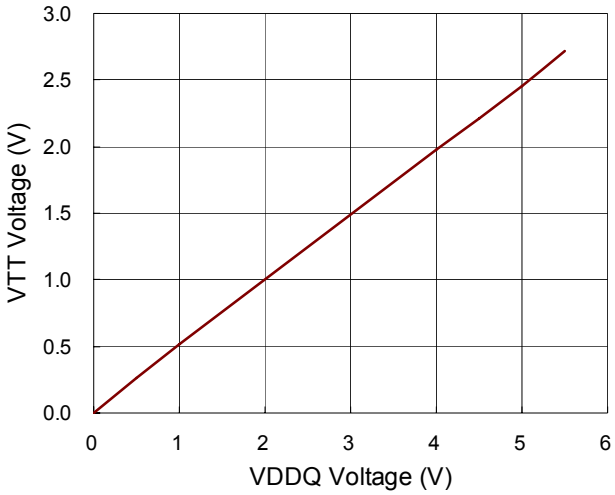
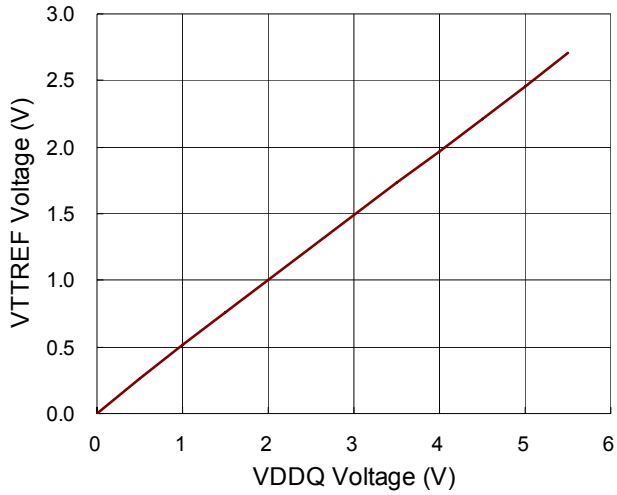
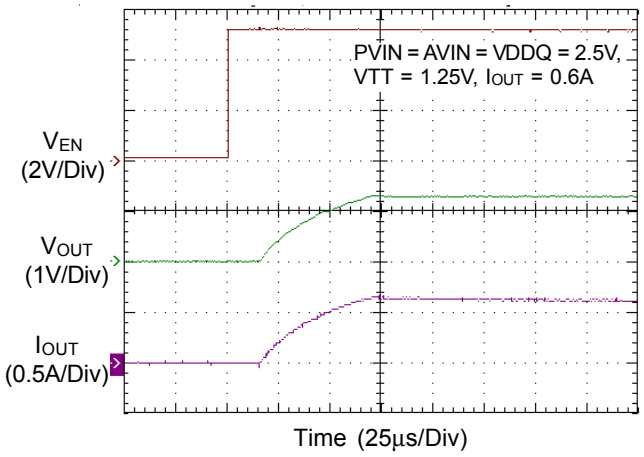
VTT Voltage vs. VDDQ Voltage



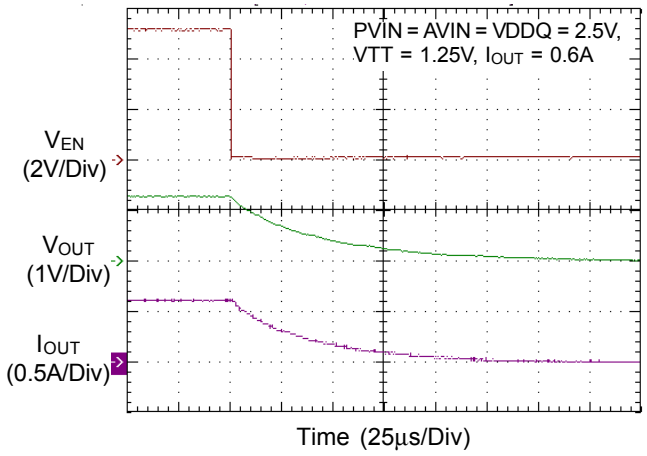
VTTREF Voltage vs. VDDQ Voltage



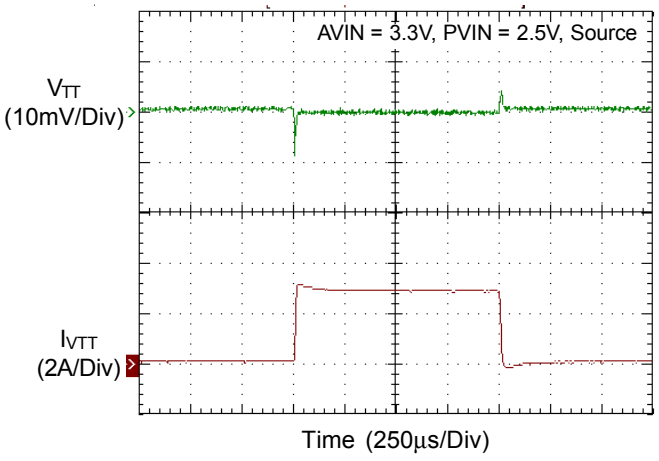
Power On from EN



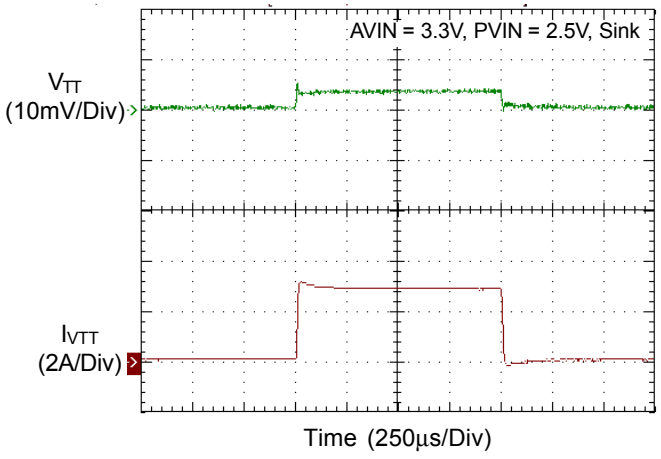
Power Off from EN



1.25VTT @ 3A Transient Response



1.25VTT @ 3A Transient Response



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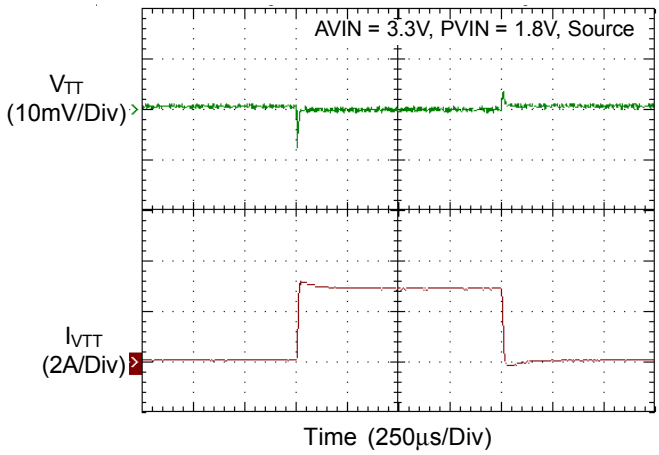
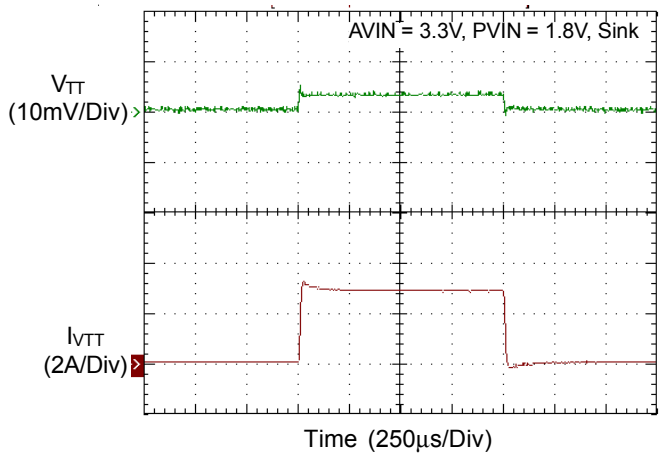
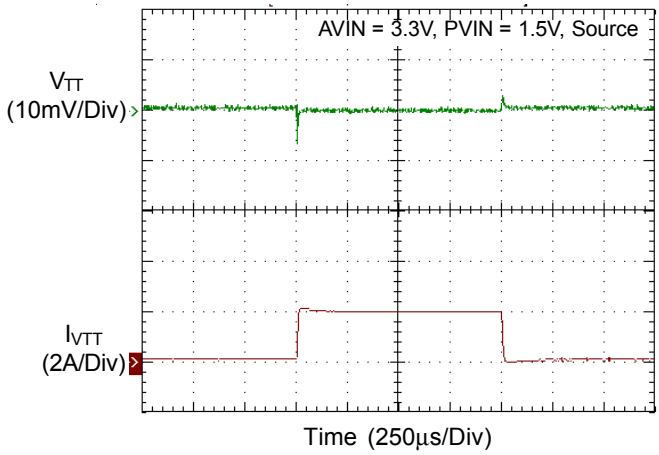
0.9VTT @ 3A Transient Response



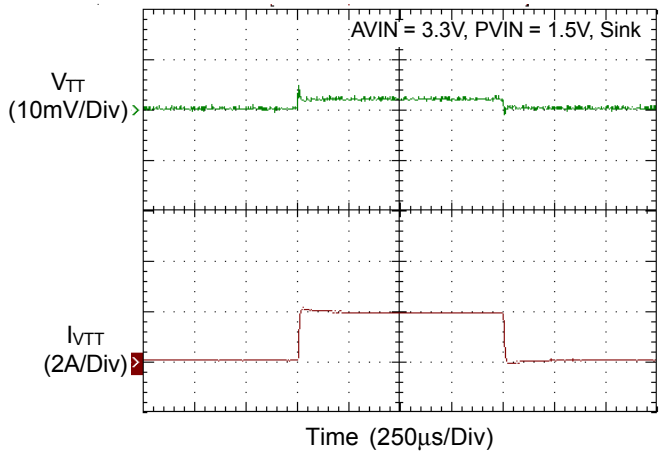
0.9VTT @ 3A Transient Response



0.75VTT @ 2A Transient Response



0.75VTT @ 2A Transient Response



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Application Information

RT2596 is a 1.5A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT2596 possesses a high speed operating amplifier that provides fast load transient response and only requires a 10μF ceramic input capacitor and two 10μF ceramic output capacitors.

VTTREF Regulator

VTTREF is a reference output voltage. To ensure stable operation, a 0.1μF ceramic capacitor between VTTREF and GND is recommended.

Capacitor Selection

Good bypassing is recommended from PVIN to GND to help improve AC performance. A 10μF or greater input capacitor located as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the PVIN pin of the IC. Adding a ceramic capacitor 1μF close to the AVIN pin can reduce the parasitic noises from the supply power. For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20μF. The RT2596 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VTT output terminal pin as close as possible.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 package, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for SOP-8 package

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.13W for SOP-8 (Exposed Pad) package

θ_{JA} is measured in the natural convection with no air flow on a highly thermal conductive four-layer test board of JEDEC 51-7 thermal measurement standard. The test board size is 75.6mm x 114.3mm (3"x4.5") with 1.6mm thickness FR4 refer to JEDEC 51 standard. Applied power dissipation is 0.5W for the thermal measurement. The test board exist four-layer copper, 2oz. (0.07mm) thickness. Force convection (air flow existed) also effects the thermal performance. Figure 1 shows the relation between thermal resistance θ_{JA} and the air flow factor.

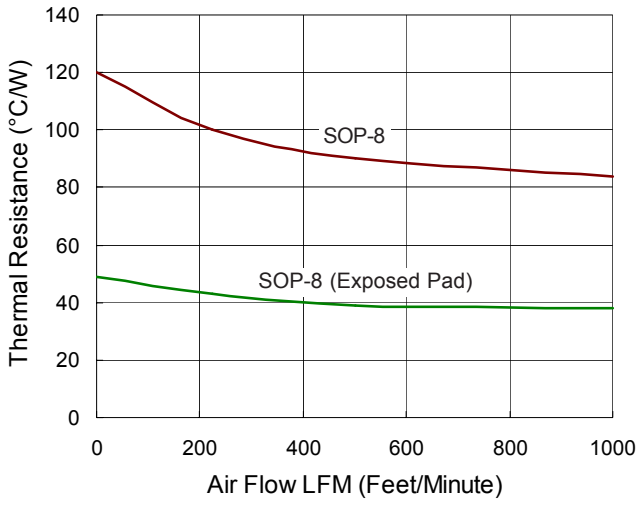

Figure 1. Thermal Resistance θ_{JA} vs. Air Flow Velocity

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The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

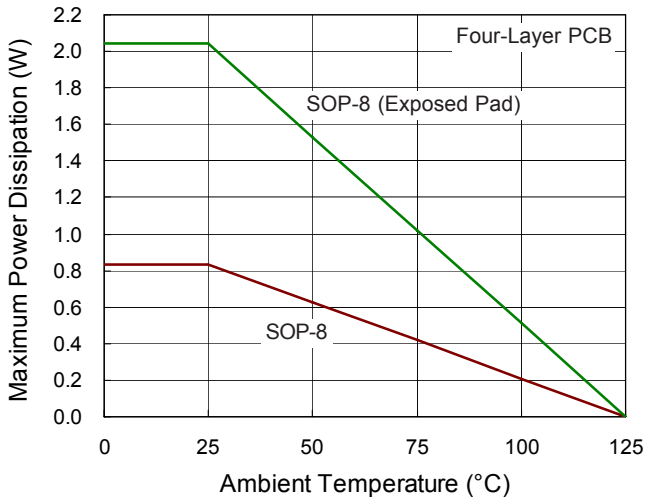

Figure 2. Derating Curve of Maximum Power Dissipation

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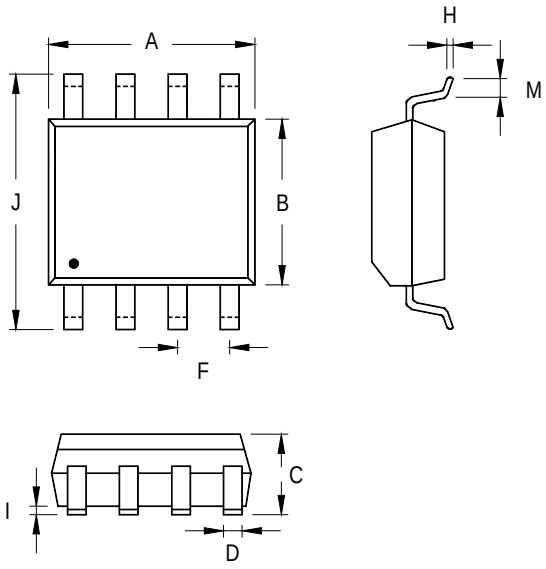
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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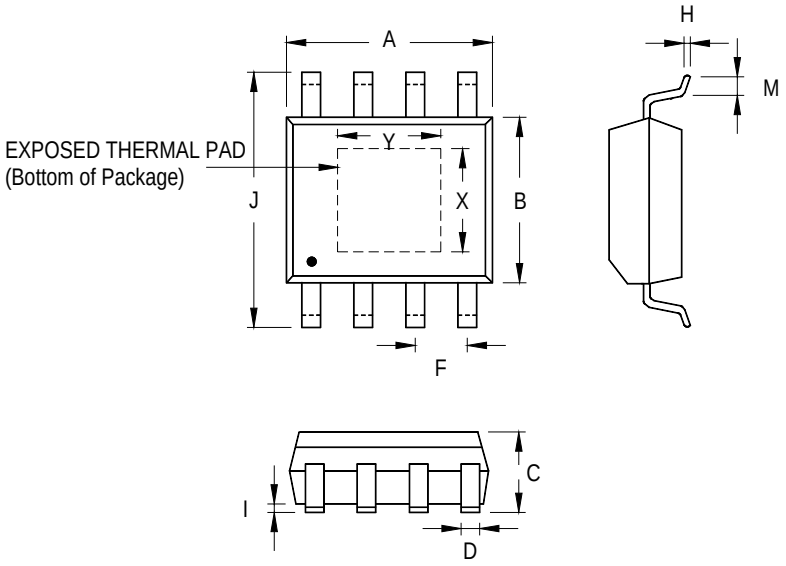

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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