Dual-Output PWM Controller with 3 Integrated Drivers for AMD SVI2 Mobile CPU Power Supply

General Description

The RT3662AM is a dual-output PWM controller with 3 integrated drivers, and it is compliant with AMD SVI2 Voltage Regulator Specification to support both CPU core (VDD) and Northbridge portion of CPU (VDDNB). The RT3662AM features CCRCOT (Constant Current Ripple Constant On-Time) with G-NAVP (Green-Native AVP), which is Richtek' s proprietary topology. G-NAVP makes it an easy setting controller to meet all AMD AVP (Adaptive Voltage Positioning) VDD/VDDNB requirements. The droop is easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance. The controller also uses the interface to issue VOTF Complete and to send digitally encoded voltage and current values for the VDD/VDDNB domains. The RT3662AM can operate in diode emulation mode to enhance the light load efficiency. And it provides the current gain adjustment capability by pin setting. The RT3662AM provides power good indication, thermal indication (VRHOT_L), and it features complete fault protection functions including over current, over voltage and under voltage.

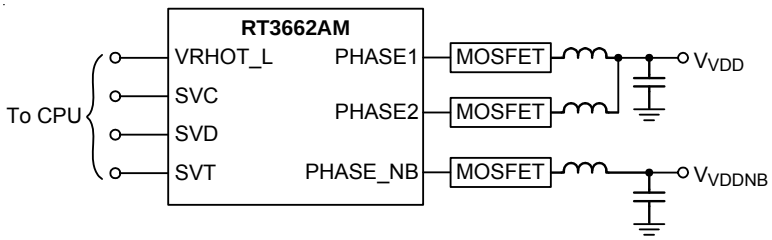
Features

- **2/1-Phase (VDD) + 1/0-Phase (VDDNB) PWM Controller**
- **3 Embedded MOSFET Drivers**
- **G-NAVP™ Topology**
- **Support Dynamic Load-Line and Zero Load-Line**
- **Diode Emulation Mode at Light Load Condition**
- **SVI2 Interface to Comply with AMD Power Management Protocol**
- **Adjustable Current Gain Capability**
- **DVID Enhancement**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Build-in ADC for Pin Setting Programming, Thermal Indication and V_{OUT}, I_{OUT} Reporting**
- **Fast Transient Response**
- **Power Good Indicator**
- **Thermal Indicator (VRHOT_L)**
- **OVP, UVP and UVLO**
- **Over Current Protection**

Applications

- AMD SVI2 Mobile CPU
- Laptop Computer

Simplified Application Circuit



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Ordering Information

RT3662AM □□

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

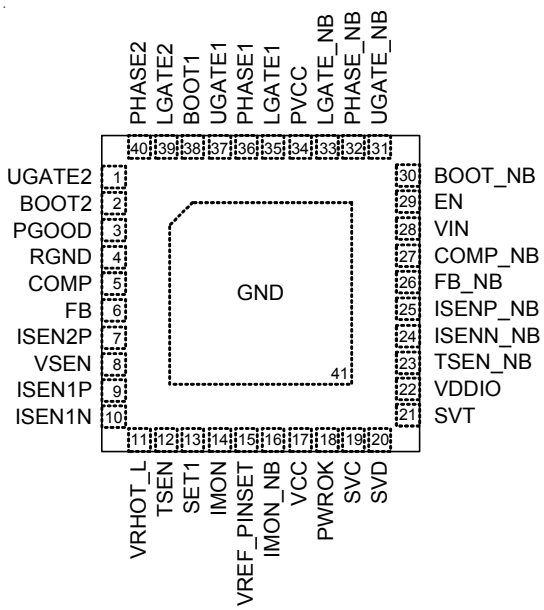
Marking Information

RT3662AMGQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

Functional Pin Description

Pin No	Pin Name	Pin Function
1	UGATE2	Upper gate driver output of Phase 2 for VDD controller. Connect this pin to the gate input of high side MOSFET.
2	BOOT2	Bootstrap supply of VDD controller for Phase 2 high side MOSFET. This pin powers high side MOSFET driver.
3	PGOOD	Power good indicator for the VDD and VDDNB controller. This pin is an open drain output.
4	RGND	Return ground of VDD and VDDNB controllers. This pin is the common negative input of output voltage differential remote sense of VDD and VDDNB controllers.
5	COMP	Error amplifier output pin of the VDD controller.
6	FB	Output voltage feedback input of VDD controller. This pin is the negative input of the error amplifier for the VDD controller.
7	ISEN2P	Positive current sense input of Phase 2 for VDD controller.
8	VSEN	VDD controller voltage sense input. This pin is connected to the terminal of VDD controller output voltage.
9	ISEN1P	Positive current sense input of Phase 1 for VDD controller.
10	ISEN1N	Common negative current sense input of Phase1 and Phase 2 for VDD controller.
11	VRHOT_L	Thermal indicator. This pin is an open drain output. (Active low)
12	TSEN	This pin provides two functions: platform setting, platform can use this pin to set frequency of VDD and VDDNB controllers, initial offset and per-phase OCP threshold of VDD controller. The other function is thermal sense input for VRHOT indicator. Connect the NTC network for thermal sensing to this pin.

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Pin No	Pin Name	Pin Function
13	SET1	Platform setting pin. Platform can use this pin to set the Ai gain of VDD and VDDNB controllers, VDDNB voltage reporting compensation bit1 to bit3 and VDD Controller QRTH.
14	IMON	Current monitor output for the VDD controller. This pin outputs a voltage proportional to the output current.
15	VREF_PINSET	This pin provides two functions: The 3.2V power supply for pin setting function divided resistors. The other function is fixed 0.8V output reference voltage, and the voltage is only used to offset the output voltage of IMON and IMON_NB pins. Connect a RC circuit from this pin to GND. The recommended resistor is from 3.9Ω to 10Ω, and the capacitor is 0.47μF.
16	IMON_NB	Current monitor output for the VDDNB controller. This pin outputs a voltage proportional to the output current.
17	VCC	Controller power supply. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor is as close controller as possible.
18	PWROK	System power good input. If PWROK is low, the SVI interface is disabled and VR returns to BOOT-VID state with initial load-line slope and initial offset. If PWROK is high, the SVI interface is running and the DAC decodes the received serial VID codes to determine the output voltage.
19	SVC	Serial VID clock input.
20	SVD	Serial VID data input. This pin is a serial data line.
21	SVT	Serial VID telemetry output from VR. This pin is a push-pull output.
22	VDDIO	Processor memory interface power rail and serves as the reference for PWROK, SVD, SVC and SVT. This pin is used by the VR to reference the SVI pins.
23	TSEN_NB	This pin provides two functions: platform setting, platform can use this pin to set initial offset, BOOT VID, voltage reporting compensation bit0 and per-phase OCP threshold of VDDNB controller. The other function is thermal sense input for VRHOT indicator. Connect the NTC network for thermal sensing to this pin.
24	ISENN_NB	Negative current sense input for VDDNB controller.
25	ISENP_NB	Positive current sense input for VDDNB controller.
26	FB_NB	Output voltage feedback input of VDDNB controller. This pin is the negative input of the error amplifier for the VDDNB controller.
27	COMP_NB	Error amplifier output pin of the VDDNB controller.
28	VIN	VIN input pin. Connect a low pass filter to this pin.
29	EN	Controller enable input pin.
30	BOOT_NB	Bootstrap supply of VDDNB controller for high side MOSFET. This pin powers high side MOSFET driver.
31	UGATE_NB	Upper gate driver output of VDDNB controller. Connect this pin to the gate input of high side MOSFET.
32	PHASE_NB	Switch nodes of high side driver for VDDNB controller. Connect this pin to high side MOSFET source together with the low side MOSFET drain and the inductor.
33	LGATE_NB	Lower gate driver output of VDDNB controller. Connect this pin to the gate input of low side MOSFET.
34	PVCC	Driver power supply. Connect this pin to GND by the 2.2μF ceramic capacitor at least. The decoupling capacitor is as close controller as possible.

Pin No	Pin Name	Pin Function
35	LGATE1	Lower gate driver output of Phase 1 for VDD controller. Connect this pin to the gate input of low side MOSFET.
36	PHASE1	Phase 1 switch nodes of high side driver for VDD controller. Connect this pin to high side MOSFET source together with the low side MOSFET drain and the inductor.
37	UGATE1	Upper gate driver output of Phase 1 for VDD controller. Connect this pin to the gate input of high side MOSFET.
38	BOOT1	Bootstrap supply of VDD controller for Phase 1 high side MOSFET. This pin powers high side MOSFET driver.
39	LGATE2	Lower gate driver output of Phase 2 for VDD controller. Connect this pin to the gate input of low side MOSFET.
40	PHASE2	Phase 2 switch nodes of high side driver for VDD controller. Connect this pin to high side MOSFET Source together with the low side MOSFET drain and the inductor.
41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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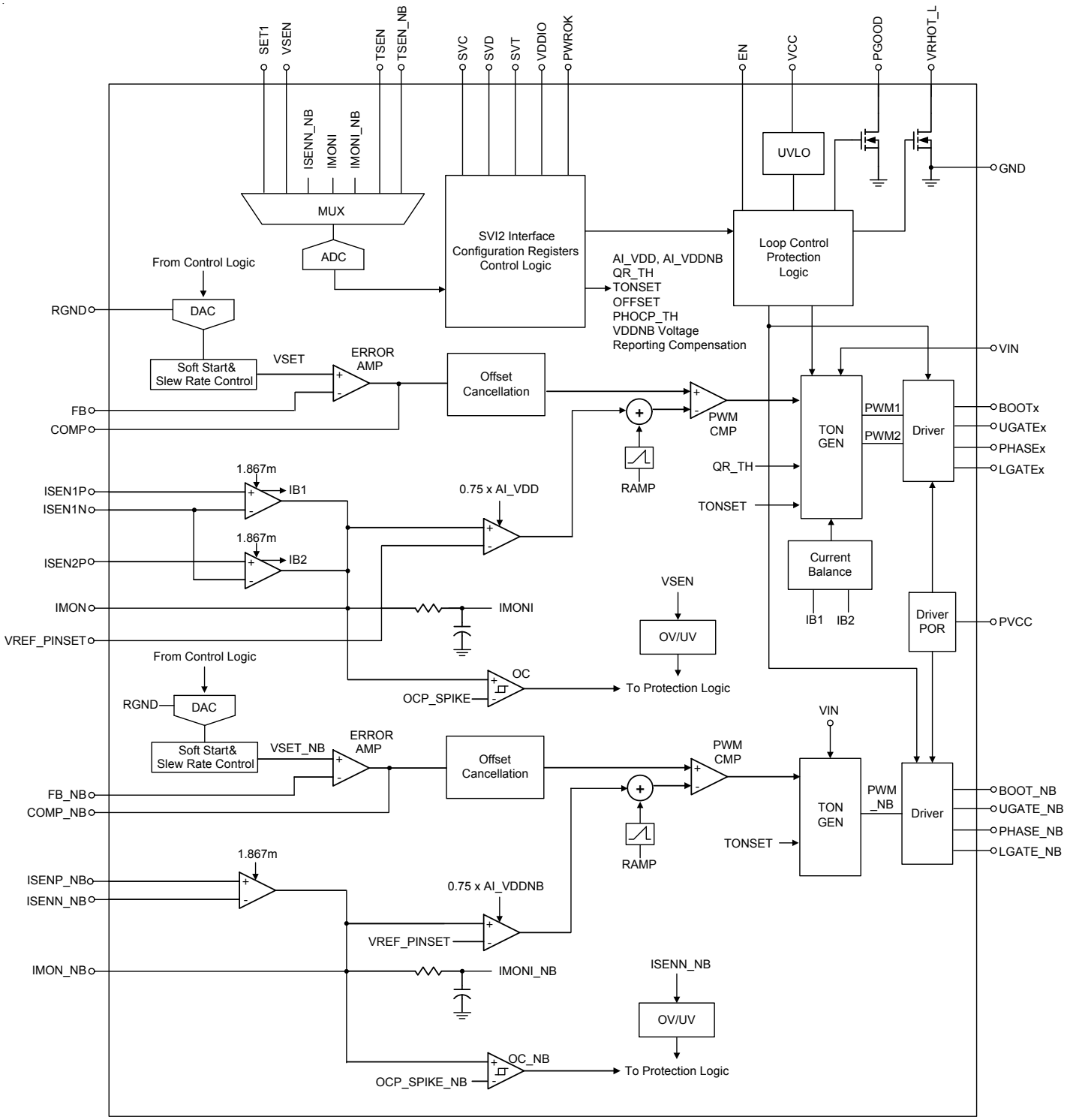
Functional Block Diagram



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Operation

The RT3662AM adopts G-NAVP™ (Green Native AVP) which is Richtek' s proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all AMD CPU requirements of AVP (Adaptive Voltage Positioning). The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, it generates an on-time width to achieve PWM modulation.

MUX and ADC

The MUX supports the inputs from SET1, TSEN, TSEN_NB, IMONI, IMONI_NB, ISENN_NB and VSEN. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

SVI2 Interface/Configuration Registers/Control Logic

The SVI2 interface uses the SVC, SVD, and SVT pins to communicate with CPU. The configuration registers save the digital data from ADC output for reporting or performance adjustment. The Control Logic controls the ADC timing and generates the digital code of the VID for VDD/VDDNB voltage.

Loop Control Protection Logic

Loop control protection logic detects EN and UVLO signals to initiate the soft-start function, and the PGOOD and VRHOT_L will be controlled after the soft-start is finished. When VRHOT indication event occurs, the VRHOT_L pin voltage will be pulled low.

DAC

The DAC receives VID codes from the SVI2 control logic to generate an internal reference voltage (VSET/VSET_NB) for controller.

Soft-Start and Slew-Rate Control

This block controls the slew rate of the internal reference voltage when output voltage changes.

Error Amplifier

Error amplifier generates COMP/COMP_NB signal by the difference between VSET/VSET_NB and FB/FB_NB.

Offset Cancellation

This block cancels the output offset voltage from voltage ripple and current ripple to achieve accurate output voltage.

UVLO

Detect the VCC pin voltage for under voltage lockout protection and power on reset operation.

Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

PWM CMP

The PWM comparator compares COMP signal (COMP/COMP_NB) and current feedback signal to generate a signal for TONGEN.

TONGEN

This block generates an on-time pulse which high interval is based on the on-time setting.

RAMP

The Ramp generator is designed to improve noise immunity and reduce jitter.

OC/OV/UV

Output voltage and output current are sensed for over current, over voltage and under voltage protection.

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Table 1. Serial VID Codes

SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
0000_0000	1.55000	0010_0111	1.30625	0100_1110	1.06250	0111_0101	0.81875
0000_0001	1.54375	0010_1000	1.30000	0100_1111	1.05625	0111_0110	0.81250
0000_0010	1.53750	0010_1001	1.29375	0101_0000	1.05000	0111_0111	0.80625
0000_0011	1.53125	0010_1010	1.28750	0101_0001	1.04375	0111_1000	0.80000
0000_0100	1.52500	0010_1011	1.28125	0101_0010	1.03750	0111_1001	0.79375
0000_0101	1.51875	0010_1100	1.27500	0101_0011	1.03125	0111_1010	0.78750
0000_0110	1.51250	0010_1101	1.26875	0101_0100	1.02500	0111_1011	0.78125
0000_0111	1.50625	0010_1110	1.26250	0101_0101	1.01875	0111_1100	0.77500
0000_1000	1.50000	0010_1111	1.25625	0101_0110	1.01250	0111_1101	0.76875
0000_1001	1.49375	0011_0000	1.25000	0101_0111	1.00625	0111_1110	0.76250
0000_1010	1.48750	0011_0001	1.24375	0101_1000	1.00000	0111_1111	0.75625
0000_1011	1.48125	0011_0010	1.23750	0101_1001	0.99375	1000_0000	0.75000
0000_1100	1.47500	0011_0011	1.23125	0101_1010	0.98750	1000_0001	0.74375
0000_1101	1.46875	0011_0100	1.22500	0101_1011	0.98125	1000_0010	0.73750
0000_1110	1.46250	0011_0101	1.21875	0101_1100	0.97500	1000_0011	0.73125
0000_1111	1.45625	0011_0110	1.21250	0101_1101	0.96875	1000_0100	0.72500
0001_0000	1.45000	0011_0111	1.20625	0101_1110	0.96250	1000_0101	0.71875
0001_0001	1.44375	0011_1000	1.20000	0101_1111	0.95625	1000_0110	0.71250
0001_0010	1.43750	0011_1001	1.19375	0110_0000	0.95000	1000_0111	0.70625
0001_0011	1.43125	0011_1010	1.18750	0110_0001	0.94375	1000_1000	0.70000
0001_0100	1.42500	0011_1011	1.18125	0110_0010	0.93750	1000_1001	0.69375
0001_0101	1.41875	0011_1100	1.17500	0110_0011	0.93125	1000_1010	0.68750
0001_0110	1.41250	0011_1101	1.16875	0110_0100	0.92500	1000_1011	0.68125
0001_0111	1.40625	0011_1110	1.16250	0110_0101	0.91875	1000_1100	0.67500
0001_1000	1.40000	0011_1111	1.15625	0110_0110	0.91250	1000_1101	0.66875
0001_1001	1.39375	0100_0000	1.15000	0110_0111	0.90625	1000_1110	0.66250
0001_1010	1.38750	0100_0001	1.14375	0110_1000	0.90000	1000_1111	0.65625
0001_1011	1.38125	0100_0010	1.13750	0110_1001	0.89375	1001_0000	0.65000
0001_1100	1.37500	0100_0011	1.13125	0110_1010	0.88750	1001_0001	0.64375
0001_1101	1.36875	0100_0100	1.12500	0110_1011	0.88125	1001_0010	0.63750
0001_1110	1.36250	0100_0101	1.11875	0110_1100	0.87500	1001_0011	0.63125
0001_1111	1.35625	0010_0110	1.11250	0110_1101	0.86875	1001_0100	0.62500
0010_0000	1.35000	0100_0111	1.10625	0110_1110	0.86250	1001_0101	0.61875
0010_0001	1.34375	0100_1000	1.10000	0110_1111	0.85625	1001_0110	0.61250
0010_0010	1.33750	0100_1001	1.09375	0111_0000	0.85000	1001_0111	0.60625
0010_0011	1.33125	0100_1010	1.08750	0111_0001	0.84375	1001_1000	0.60000
0010_0100	1.32500	0100_1011	1.08125	0111_0010	0.83750	1001_1001	0.59375
0010_0101	1.31875	0100_1100	1.07500	0111_0011	0.83125	1001_1010	0.58750
0010_0110	1.31250	0100_1101	1.06875	0111_0100	0.82500	1001_1011	0.58125

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SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
1001_1100	0.57500	1011_0101 *	0.41875	1100_1110 *	0.26250	1110_0111*	0.10625
1001_1101	0.56875	1011_0110 *	0.41250	1100_1111 *	0.25625	1110_1000*	0.10000
1001_1110	0.56250	1011_0111 *	0.40625	1101_0000 *	0.25000	1110_1001*	0.09375
1001_1111	0.55625	1011_1000 *	0.40000	1101_0001 *	0.24375	1110_1010*	0.08750
1010_0000	0.55000	1011_1001 *	0.39375	1101_0010 *	0.23750	1110_1011*	0.08125
1010_0001	0.54375	1011_1010 *	0.38750	1101_0011 *	0.23125	1110_1100*	0.07500
1010_0010	0.53750	1011_1011 *	0.38125	1101_0100 *	0.22500	1110_1101*	0.06875
1010_0011	0.53125	1011_1100 *	0.37500	1101_0101 *	0.21875	1110_1110*	0.06250
1010_0100	0.52500	1011_1101 *	0.36875	1101_0110 *	0.21250	1110_1111*	0.05625
1010_0101	0.51875	1011_1110 *	0.36250	1101_0111 *	0.20625	1111_0000*	0.05000
1010_0110	0.51250	1011_1111 *	0.35625	1101_1000 *	0.20000	1111_0001*	0.04375
1010_0111	0.50625	1100_0000 *	0.35000	1101_1001 *	0.19375	1111_0010*	0.03750
1010_1000 *	0.50000	1100_0001 *	0.34375	1101_1010 *	0.18750	1111_0011*	0.03125
1010_1001 *	0.49375	1100_0010 *	0.33750	1101_1011 *	0.18125	1111_0100*	0.02500
1010_1010 *	0.48750	1100_0011 *	0.33125	1101_1100 *	0.17500	1111_0101*	0.01875
1010_1011 *	0.48125	1100_0100 *	0.32500	1101_1101 *	0.16875	1111_0110*	0.01250
1010_1100 *	0.47500	1100_0101 *	0.31875	1101_1110 *	0.16250	1111_0111*	0.00625
1010_1101 *	0.46875	1100_0110 *	0.31250	1101_1111 *	0.15625	1111_1000*	0.00000
1010_1110 *	0.46250	1100_0111 *	0.30625	1110_0000*	0.15000	1111_1001*	OFF
1010_1111 *	0.45625	1100_1000 *	0.30000	1110_0001*	0.14375	1111_1010*	OFF
1011_0000 *	0.45000	1100_1001 *	0.29375	1110_0010*	0.13750	1111_1011*	OFF
1011_0001 *	0.44375	1100_1010 *	0.28750	1110_0011*	0.13125	1111_1100*	OFF
1011_0010 *	0.43750	1100_1011 *	0.28125	1110_0100*	0.12500	1111_1101*	OFF
1011_0011 *	0.43125	1100_1100 *	0.27500	1110_0101*	0.11875	1111_1110*	OFF
1011_0100 *	0.42500	1100_1101 *	0.26875	1110_0110*	0.11250	1111_1111*	OFF

* Indicates TOB is 80mV for this VID code; unconditional VR controller stability required at all VID codes

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Table 2. SET1 Pin Setting for VDD Controller AI Gain Ratio and VDDNB Voltage Reporting Offset

SET1 Pin Setting Voltage $\left(V_{SET1_DIV} = 3.2 \times \frac{R_D}{R_U + R_D}\right)$				AI_VDD	VDDNB_RPT_OFS [3:1] bits
Min	Typical	Max	Unit		
6.75	25	43.25	mV	25%	000
57.25	75	92.75	mV		001
107.75	125	142.25	mV		010
158.25	175	191.75	mV		011
208.75	225	241.25	mV		100
259.25	275	290.75	mV		101
309.75	325	340.25	mV		110
360.25	375	389.75	mV		111
410.75	425	439.25	mV	50%	000
461.25	475	488.75	mV		001
511.75	525	538.25	mV		010
562.25	575	587.75	mV		011
612.75	625	637.25	mV		100
663.25	675	686.75	mV		101
713.75	725	736.25	mV		110
764.25	775	785.75	mV		111
814.75	825	835.25	mV	100%	000
865.25	875	884.75	mV		001
915.75	925	934.25	mV		010
966.25	975	983.75	mV		011
1016.75	1025	1033.25	mV		100
1067.25	1075	1082.75	mV		101
1117.75	1125	1132.25	mV		110
1168.25	1175	1181.75	mV		111
1218.75	1225	1231.25	mV	0LL	000
1269.25	1275	1280.75	mV		001
1319.75	1325	1330.25	mV		010
1370.25	1375	1379.75	mV		011
1420.75	1425	1429.25	mV		100
1471.25	1475	1478.75	mV		101
1521.75	1525	1528.25	mV		110
1572.25	1575	1577.75	mV		111

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Table 3. SET1 Pin Setting for VDDNB Controller AI Gain Ratio, VDD Controller QR Threshold

SET1 Pin Setting Voltage $\left(V_{SET1_IR} = 80\mu \times \frac{R_U \times R_D}{R_U + R_D}\right)$				AI_VDDNB	QR Threshold (VDD)
Min	Typical	Max	Unit		
7.84	50	92.16	mV	25%	Disable
213.2	250	286.8			20mV
315.88	350	384.12			25mV
418.56	450	481.44		50%	Disable
623.92	650	676.08			20mV
726.6	750	773.4			25mV
829.28	850	870.72		100%	Disable
1034.64	1050	1065.36			20mV
1137.32	1150	1162.68			25mV
1240	1250	1260		0LL	Disable
1445.36	1450	1454.64			20mV
1548.04	1550	1551.96			25mV

Table 4. TSEN Pin Setting for the Frequency of VDD/VDDNB Controller, VDD Controller Initial Offset and PHOCP Setting Ratio

TSEN Pin Setting Voltage $\left(V_{TSEN_DIV} = 3.2 \times \frac{R_D}{R_U + R_D}\right)$				Frequency (VDD/VDDNB)	Initial Offset (VDD)	VDD PHOCP Setting Ratio (Percentage of OCP_SPIKE)
Min	Typical	Max	Unit			
6.75	25	43.25	mV	300kHz	–25mV	150%
57.25	75	92.75	mV			200%
208.75	225	241.25	mV		0mV	150%
259.25	275	290.75	mV			200%
410.75	425	439.25	mV		25mV	150%
461.25	475	488.75	mV			200%
612.75	625	637.25	mV		50mV	150%
663.25	675	686.75	mV			200%
814.75	825	835.25	mV	400kHz	–25mV	150%
865.25	875	884.75	mV			200%
1016.75	1025	1033.25	mV		0mV	150%
1067.25	1075	1082.75	mV			200%
1218.75	1225	1231.25	mV		25mV	150%
1269.25	1275	1280.75	mV			200%
1420.75	1425	1429.25	mV		50mV	150%
1471.25	1475	1478.75	mV			200%
PHOCP_TH = OCP_SPIKE × (PHOCP Setting Ratio) / M (M : Phase Number)						

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Table 5. TSEN_NB Pin Setting for VDDNB Controller Initial Offset, Voltage Reporting Offset and PHOCP Setting Ratio

TSEN_NB Pin Setting Voltage $\left(V_{TSEN_NB_DIV} = 3.2 \times \frac{R_D}{R_U + R_D}\right)$				Initial Offset (VDDNB)	VDDNB_RPT_OFS [0]	VDDNB PHOCP Setting Ratio (Percentage of OCP_SPIKE_NB)
Min	Typical	Max	Unit			
6.75	25	43.25	mV	−25mV (PS0)	0	150%
57.25	75	92.75	mV			200%
107.75	125	142.25	mV		1	150%
158.25	175	191.75	mV			200%
208.75	225	241.25	mV	0mV (PS0)	0	150%
259.25	275	290.75	mV			200%
309.75	325	340.25	mV		1	150%
360.25	375	389.75	mV			200%
410.75	425	439.25	mV	25mV (PS0)	0	150%
461.25	475	488.75	mV			200%
511.75	525	538.25	mV		1	150%
562.25	575	587.75	mV			200%
612.75	625	637.25	mV	50mV (PS0)	0	150%
663.25	675	686.75	mV			200%
713.75	725	736.25	mV		1	150%
764.25	775	785.75	mV			200%
814.75	825	835.25	mV	Fixed 1.5V (PS2)	0	150%
865.25	875	884.75	mV			200%
915.75	925	934.25	mV		1	150%
966.25	975	983.75	mV			200%
1016.75	1025	1033.25	mV	Fixed 1.35V (PS2)	0	150%
1067.25	1075	1082.75	mV			200%
1117.75	1125	1132.25	mV		1	150%
1168.25	1175	1181.75	mV			200%
1218.75	1225	1231.25	mV	Fixed 1.25V (PS2)	0	150%
1269.25	1275	1280.75	mV			200%
1319.75	1325	1330.25	mV		1	150%
1370.25	1375	1379.75	mV			200%
1420.75	1425	1429.25	mV	0mV (PS2)	0	150%
1471.25	1475	1478.75	mV			200%
1521.75	1525	1528.25	mV		1	150%
1572.25	1575	1577.75	mV			200%

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Table 6. VDDNB Voltage Reporting Offset Table

VDDNB_RPT_OFS [3:0]	VDDNB Voltage Reporting Offset (VDDNB_RPT_OFS) (Bits)
0000	DIMON_NB x 1/128
0001	DIMON_NB x 2/128
0010	DIMON_NB x 3/128
0011	DIMON_NB x 4/128
0100	DIMON_NB x 5/128
0101	DIMON_NB x 6/128
0110	DIMON_NB x 7/128
0111	DIMON_NB x 8/128
1000	DIMON_NB x 9/128
1001	DIMON_NB x 10/128
1010	DIMON_NB x 11/128
1011	DIMON_NB x 12/128
1100	DIMON_NB x 13/128
1101	DIMON_NB x 14/128
1110	DIMON_NB x 15/128
1111	DIMON_NB x 16/128

$$DIMON_NB = \frac{V_{IMON_NB} - 0.8}{0.8} \times 255 \quad (Bits)$$

DIMON_NB : VDDNB Current Reporting Digital Code

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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- BOOTx to PHASEx
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –5V to 7.5V
- PHASEx to GND
  - DC ---------- –0.3V to 32V
  - < 100ns ---------- –10V to 38V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –2.5V to 7.5V
- VIN to GND ---------- –0.3V to 28V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)
  - WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  - WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Supply Voltage, PVCC ---------- 4.5V to 5.5V
- Supply Voltage, VIN ---------- 4.5V to 24V
- Junction Temperature Range ---------- –40°C to 125°C

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Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply							
Supply Voltage		V_{CC}		4.5	5	5.5	V
Supply Current		I_{VCC}	V_{EN} = 3V, not switching	--	9	15	mA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	5	--	μA
PVCC Supply Voltage		V_{PVCC}		4.5	5	5.5	V
PVCC Supply Current		I_{PVCC}	V_{BOOTX} = 5V, not switching	--	150	--	μA
Input Power Supply							
Driver POR Threshold		V_{POR_r}	PVCC POR rising	--	3.85	4.1	V
		V_{POR_f}	PVCC POR falling	3.4	3.65	--	V
Driver POR Hysteresis		V_{POR_Hys}		100	200	350	mV
Reference and DAC							
Reference Voltage Output		V_{REF}		0.795	0.8	0.805	V
DAC Accuracy		V_{FB}	V_{DAC} = 1.0000 to 1.5500 (No load, CCM mode)	–0.5	0	0.5	%SVID
			V_{DAC} = 0.8000 to 1.0000	–5	0	5	mV
			V_{DAC} = 0.3000 to 0.8000	–8	0	8	mV
			V_{DAC} = 0.2500 to 0.3000	–80	0	80	mV
RGND Current		I_{RGND}	EN = 3V, Not switching	150	200	250	μA
Slew Rate							
Dynamic VID Slew Rate		SR	Set VID fast	7.5	10	15	mV/μs
Error Amplifier							
Input Offset		V_{EAOFS}		–4	--	4	mV
DC Gain		ADC	R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product		GBW	C_{LOAD} = 5pF	--	5	--	MHz
Output Voltage Range		V_{COMP}	R_{LOAD} = 47kΩ	0.3	--	3.6	V
EA Source/Sink Current		$I_{EA,SRC}/I_{EA,SNK}$	V_{COMP} = 2V	--	5	--	mA
Current Sensing Amplifier							
Input Offset Voltage		V_{OSCS}		–0.4	--	0.4	mV
Impedance Input	Negative	R_{ISENxN}		1	--	--	MΩ
	Positive	R_{ISENxP}		1	--	--	MΩ
Input Range		V_{ISEN_IN}	V_{DAC} = 1.1V, (ISENxP – ISENxN)	–40	--	40	mV
Current Sense Gain Error		A_{ISEN_Err}	V_{DAC} = 1.1V	–2	--	2	%
EN and Logic Inputs							
EN Threshold		V_{IH_EN}	V_{IN} = 10V, V_{DAC} = 1V, Freq. = 400k	2	--	--	V
		V_{IL_EN}	V_{DAC} = 1	--	--	0.8	V
Leakage Current of EN		I_{LEK_EN}	Lower limit to 1V	–1	--	1	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SVC, SVD, PWROK	V_{IH_SVI}	Respect to VDDIO	70	--	100	%
	V_{IH_SVI}	Respect to VDDIO	0	--	35	%
Hysteresis of SVC, SVD, PWROK	V_{HYS_SVI}	Respect to VDDIO	10	--	--	%
SVI2 Bus						
SVC Frequency	f_{SVC}	(Note 5)	0.1	--	30	MHz
Thermal Management						
VRHOT Indicator Threshold	V_{TH_VRHOT}		2.16	2.2	2.24	V
VRHOT Indicator Hysteresis	V_{HYS_VRHOT}		50	75	100	mV
TON Setting						
On-Time Setting	t_{ON}	V_{IN} = 19V,V_{DAC} = 1V, [PSI0_L:PSI1_L] = 11 (Note 6)	150	175	200	ns
Minimum Off Time	t_{OFF}	V_{DAC} = 1V	--	250	400	ns
ITSEN						
TSEN Source Current	I_{TSEN}	V_{CC} = 5V	--	80	--	μA
Protection						
Under Voltage Lockout Threshold	V_{UVLO}	VCC falling edge	3.9	4.1	4.3	V
Under Voltage Lockout Hysteresis	ΔV_{UVLO}		--	200	--	mV
Over Voltage Protection Threshold	V_{OVP}		1.8	1.85	1.9	V
Delay of OVP	t_{OVP}	VSEN rising above threshold	0.3	1	3	μs
Under Voltage Protection Threshold	V_{UVP}	Respect to VID voltage	–600	–500	–400	mV
Delay of UVP	t_{UVP}	VSEN falling below threshold	0.5	3	7	μs
OCP_SPIKE Threshold	I_{OCP_SPIKE}	DCR = 1.1mΩ, KAG = 0.6, RIMON = 8.433kΩ	73.15	77	80.85	A
OCP_SPIKE Trigger Delay	$t_{OCPSPIKE_DLY}$		8	14	20	μs
Delay of Per Phase OCP	t_{PHOCP}		0.1	0.5	1	μs
VRHOT_L and PGOOD						
Output Low Voltage at VRHOT_L	V_{VRHOT_L}	I_{VRHOT_L} = 4mA	0	--	0.2	V
VRHOT_L Assertion Time	t_{VRHOTL}		2	--	--	μs
Output Low Voltage at PGOOD	V_{PGOOD}	I_{PGOOD} = 4mA	0	--	0.2	V
PGOOD Threshold	V_{TH_PGOOD}	Respect to BOOT VID	--	–300	--	mV
PGOOD Delay Time	t_{PGOOD}	BOOT VID to PGOOD high	60	110	160	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Report						
Maximum Reported Current (FFh = OCP_SPIKE)			--	100	--	%IDD_SPIKE_OCP
Minimum Reported Current (00h)			--	0	--	%IDD_SPIKE_OCP
IDDSPIKE Current Accuracy			--	--	3	%
Voltage Report						
Maximum Reported Voltage (0_00h)			--	3.15	--	V
Minimum Reported Voltage (1_F8h)			--	0	--	V
Voltage Accuracy			–2	--	2	LSB
Switching Time						
UGATEx Rise Time	t_{UGATEr}	3nF load	--	8	--	ns
UGATEx Fall Time	t_{UGATEf}	3nF load	--	8	--	ns
LGATEx Rise Time	t_{LGATEr}	3nF load	--	8	--	ns
LGATEx Fall Time	t_{LGATEf}	3nF load	--	4	--	ns
UGATEx Turn-On Propagation Delay	$t_{UGATEpdh}$	Output unloaded	--	20	--	ns
LGATEx Turn-On Propagation Delay	$t_{LGATEpdh}$	Output unloaded	--	20	--	ns
Output						
UGATEx Driver Source Resistance	$R_{UGATEsr}$	100mA source current	--	1	--	Ω
UGATEx Driver Source Current	$I_{UGATEsr}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
UGATEx Driver Sink Resistance	$R_{UGATEsk}$	100mA sink current	--	1	--	Ω
UGATEx Driver Sink Current	$I_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
LGATEx Driver Source Resistance	$R_{LGATEsr}$	100mA source current	--	1	--	Ω
LGATEx Driver Source Current	$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	2	--	A
LGATEx Driver Sink Resistance	$R_{LGATEsk}$	100mA sink current	--	0.5	--	Ω
LGATEx Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	4	--	A

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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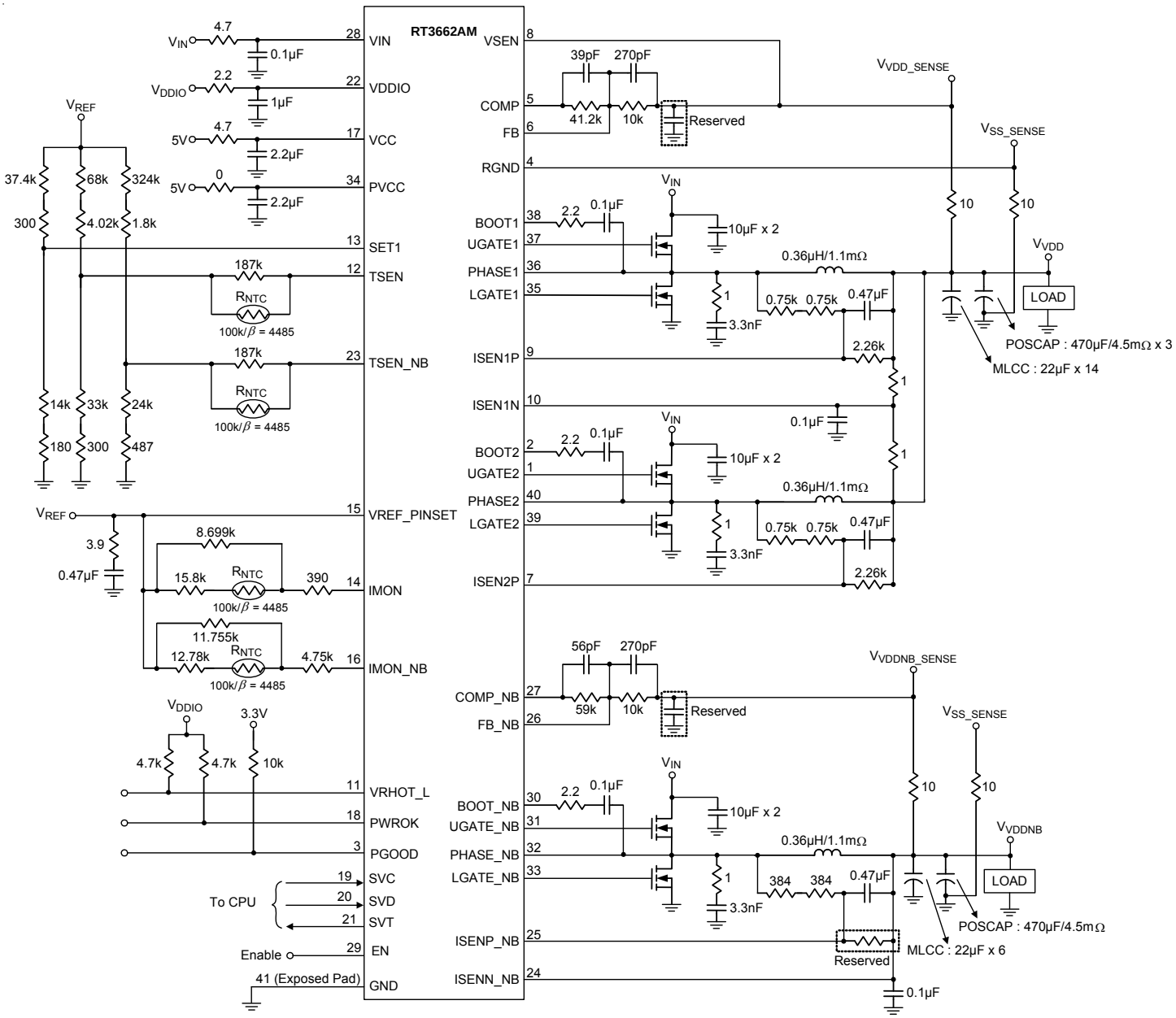
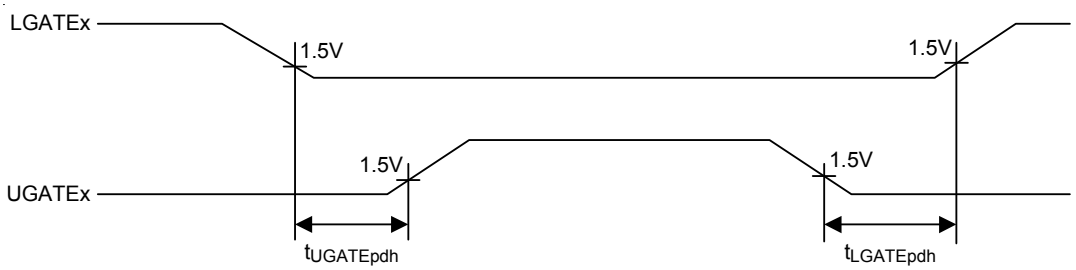
Typical Application Circuit



Timing Diagram



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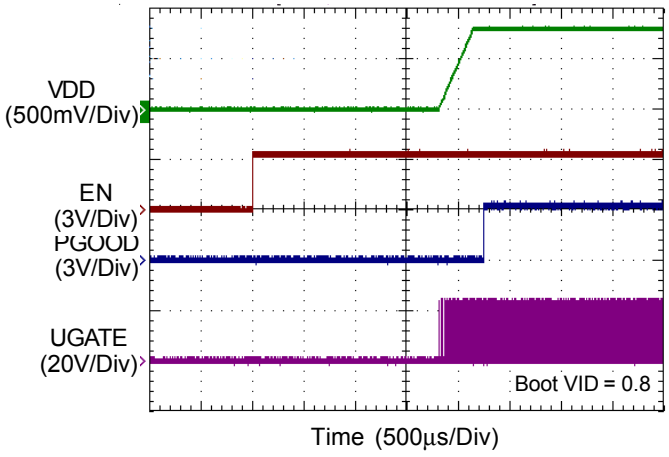
Typical Operating Characteristics

CORE VR Power On from EN



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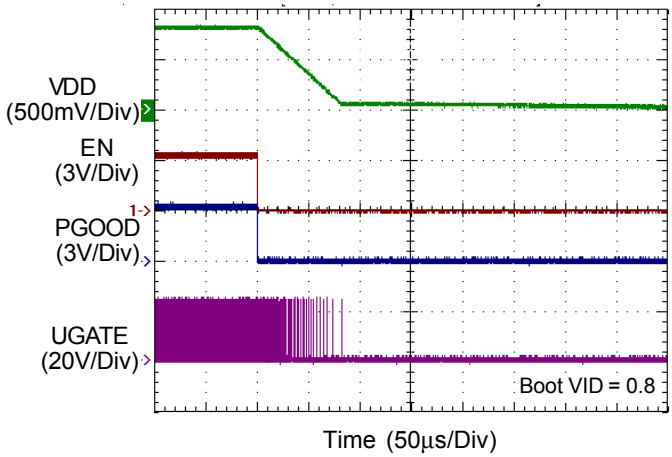
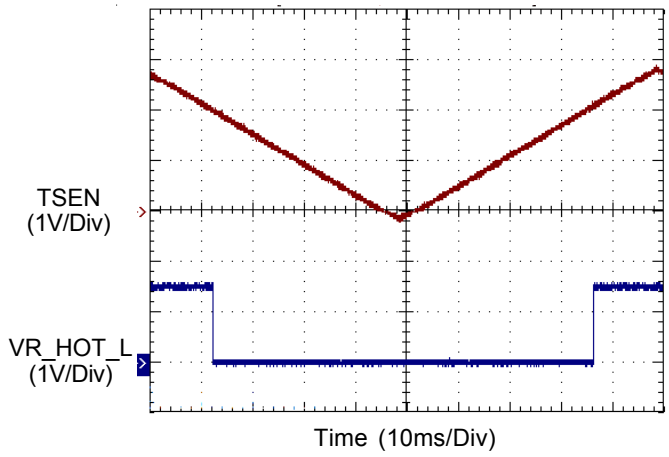
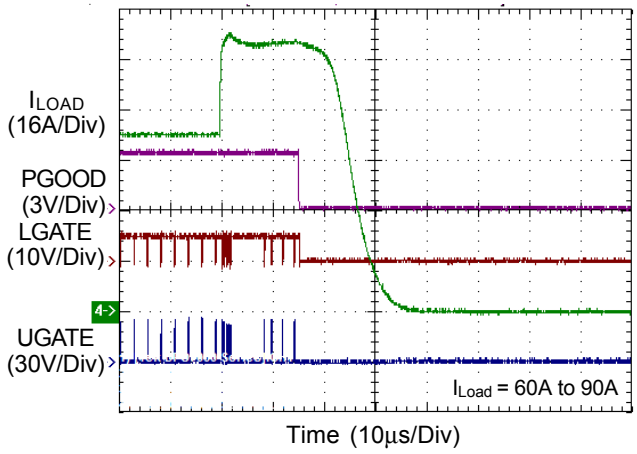


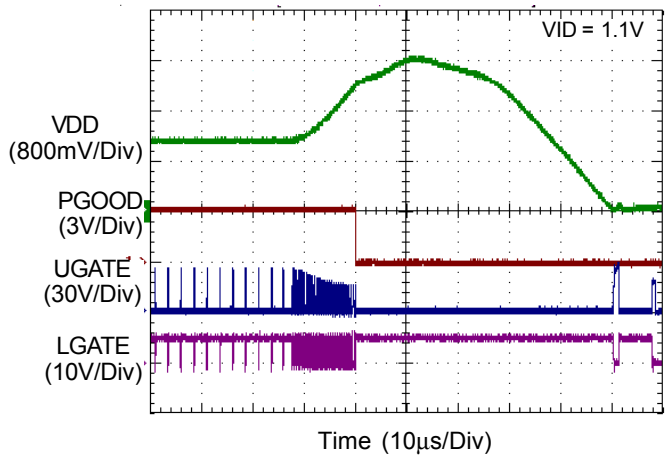
CORE VR Thermal Monitoring



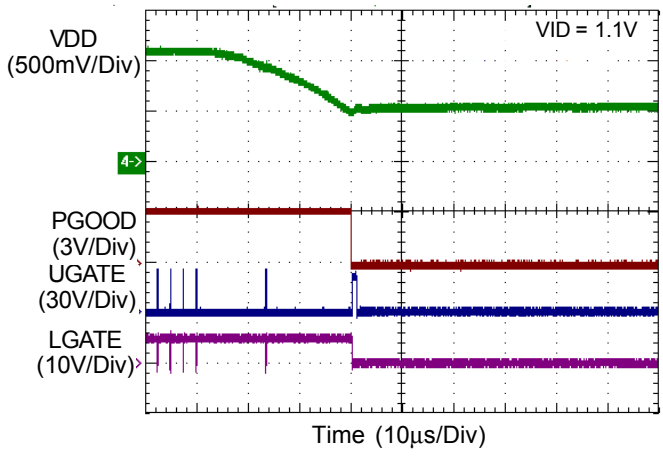
CORE VR OCP_SPIKE



CORE VR OVP



CORE VR UVP



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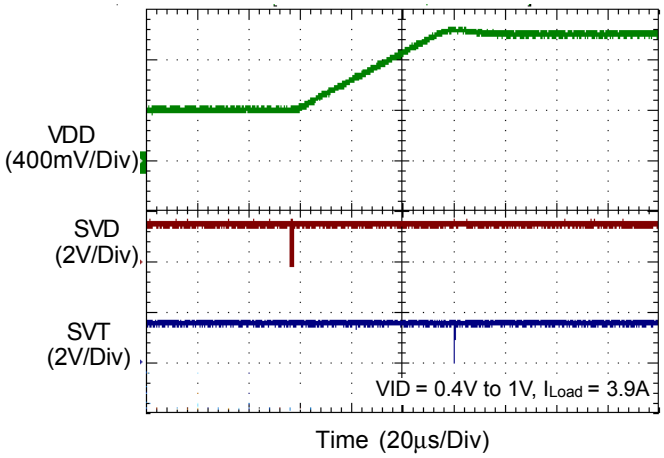
CORE VR Dynamic VID Up



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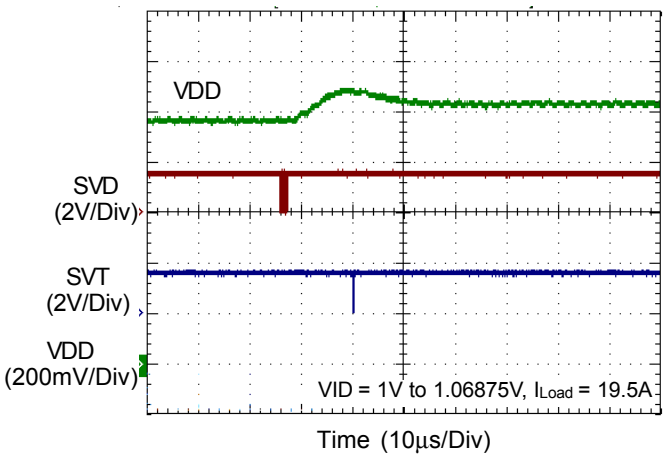

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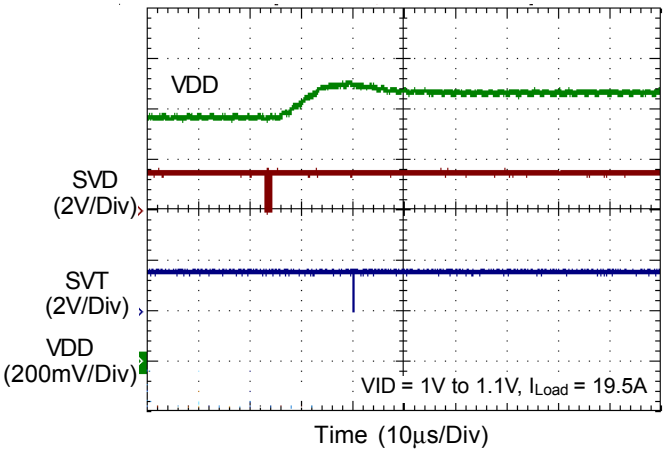

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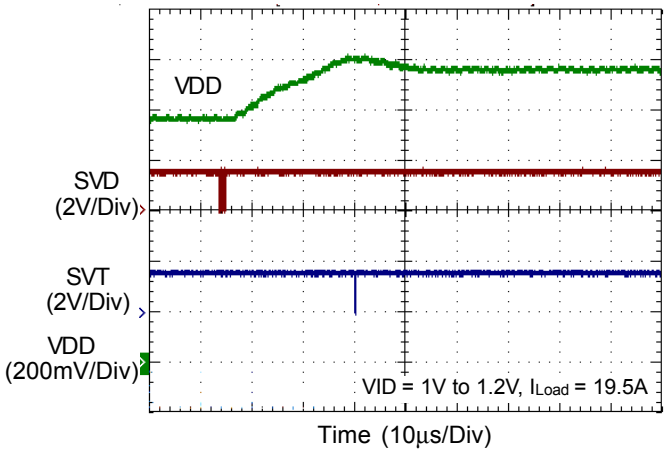

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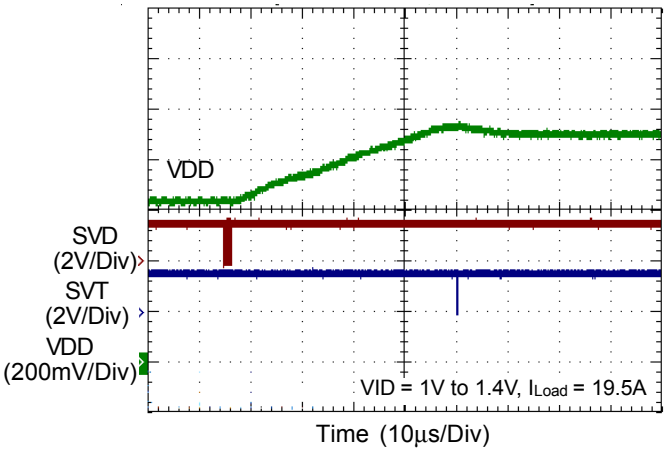
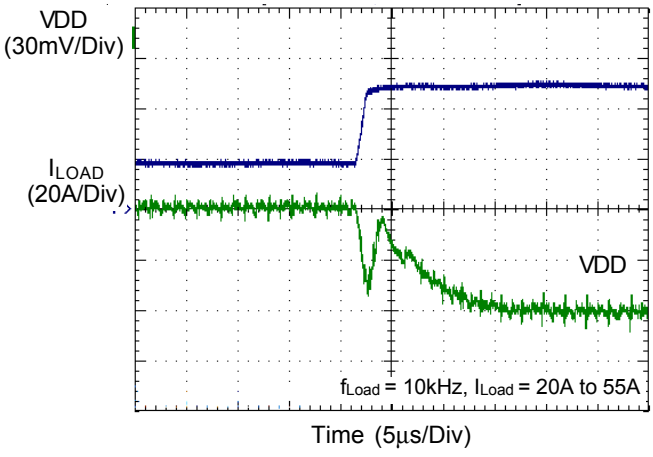


CORE VR Load Transient



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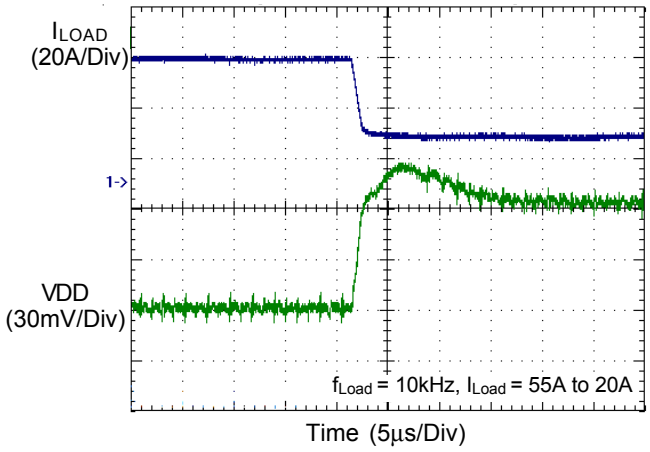
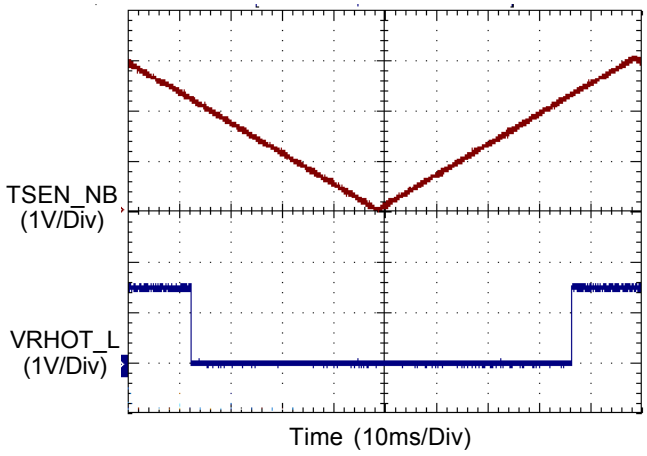
CORE VR Load Transient



NB VR Thermal Monitoring



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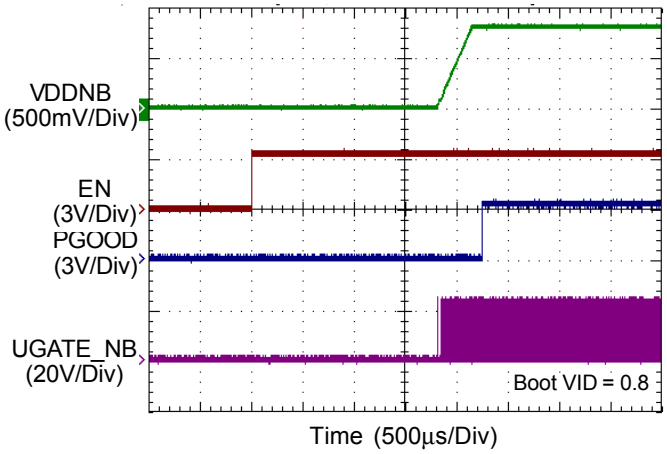

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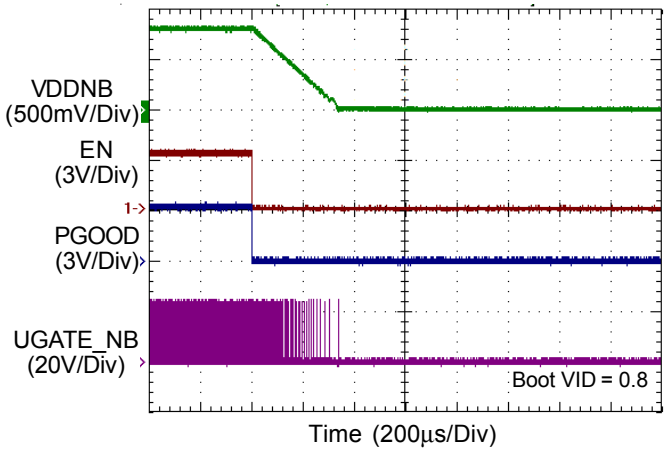

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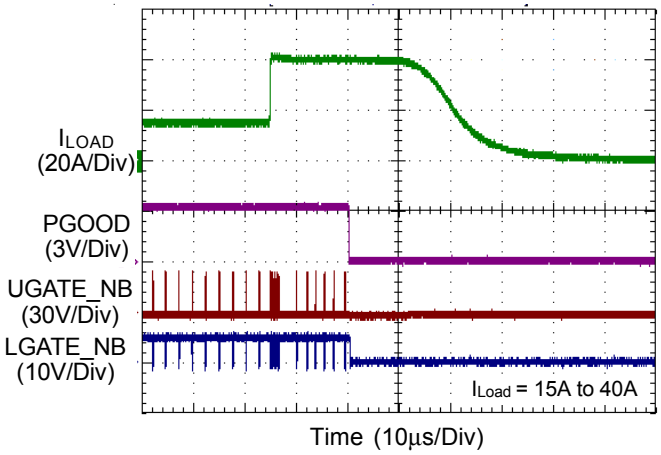

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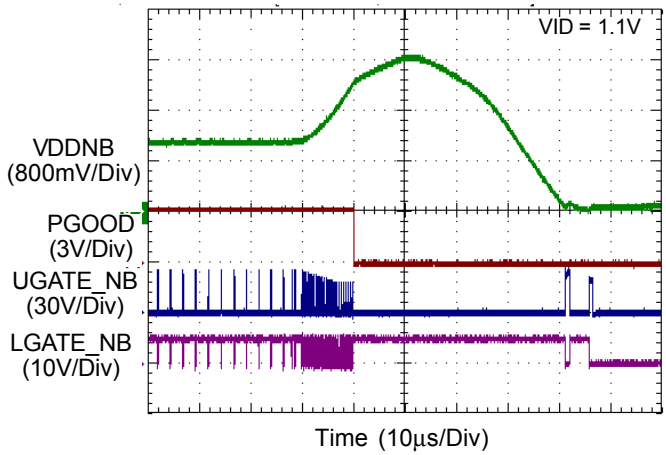

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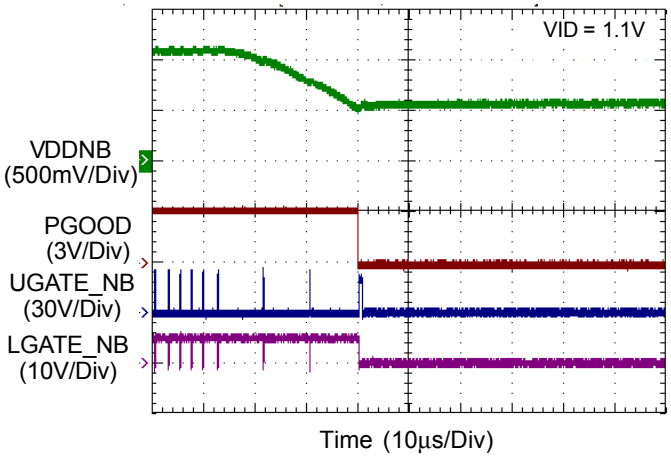
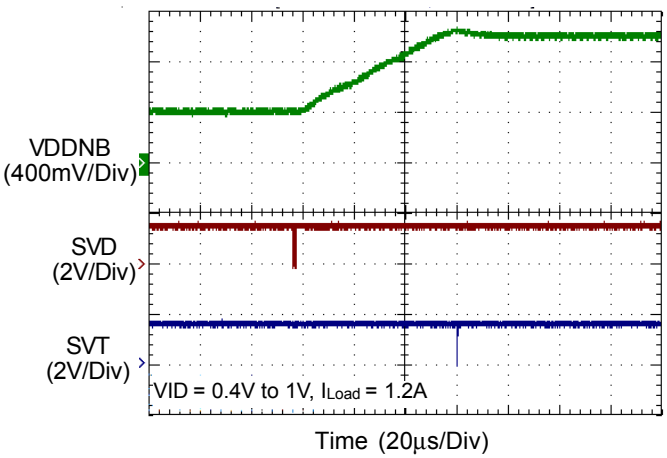
NB VR UVP



NB VR Dynamic VID Up



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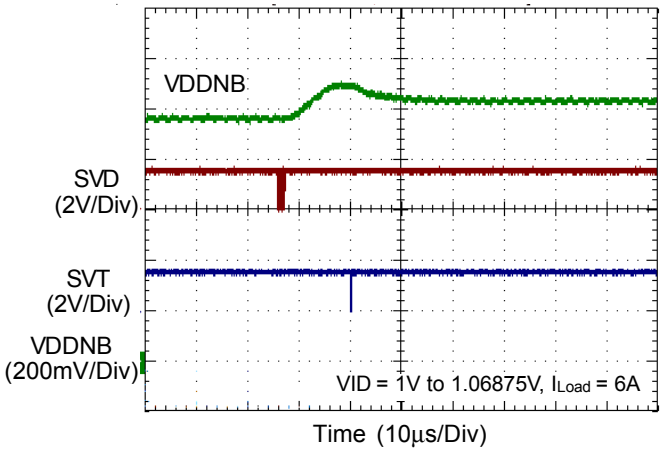

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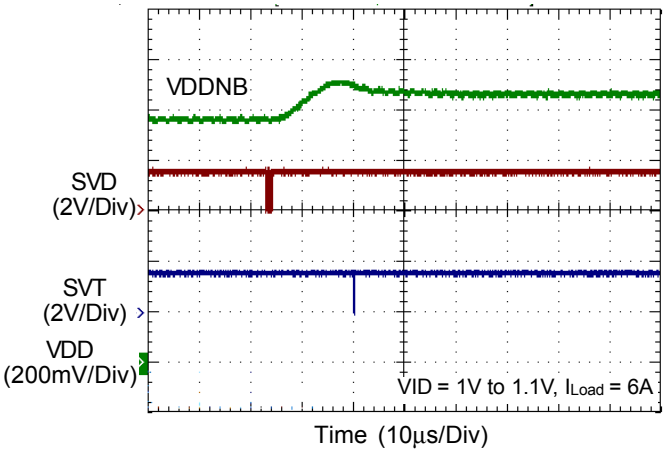

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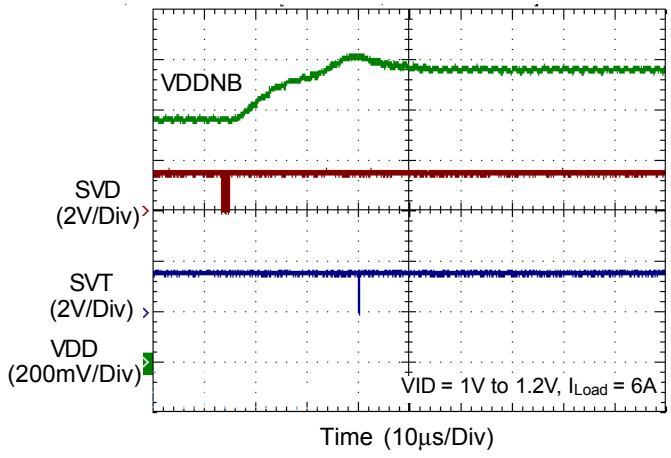

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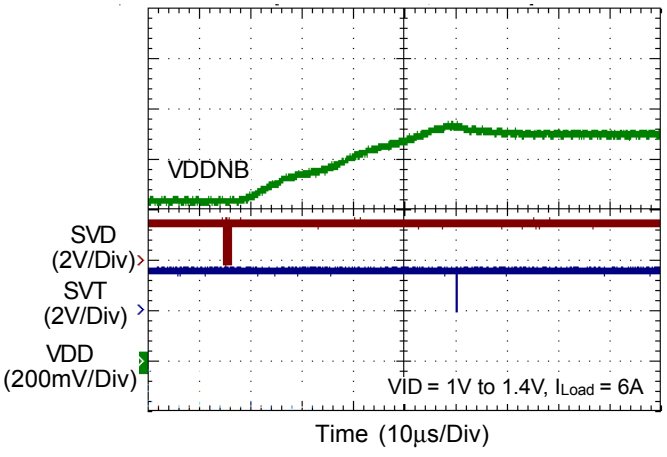

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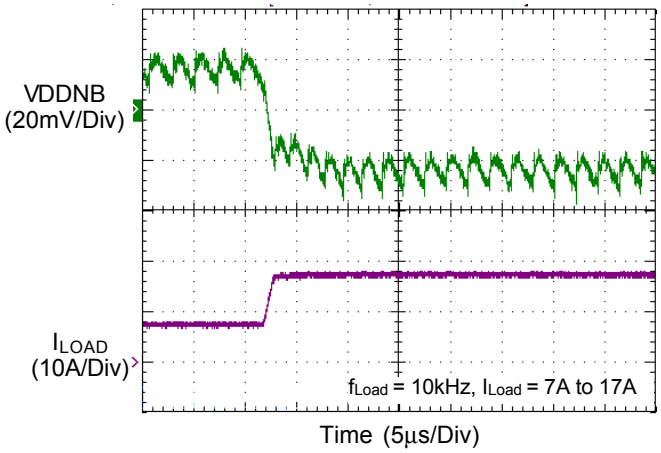
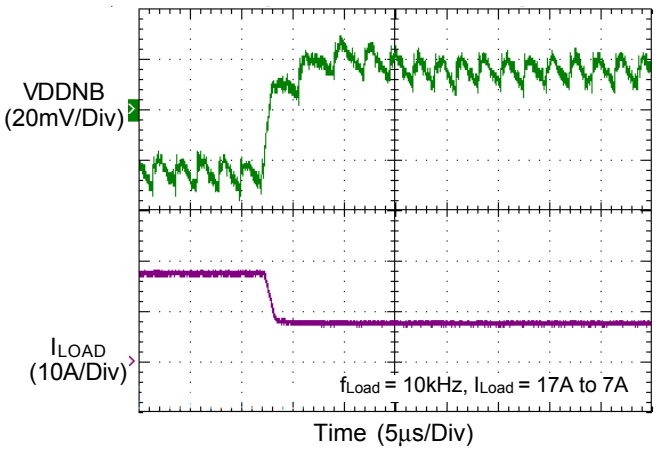
NB VR Load Transient



NB VR Load Transient



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Application Information

Power Ready (POR) Detection

During start-up, the RT3662AM will detect the voltage at the voltage input pins: VCC, PVCC and EN. When VCC > 4.3V and PVCC > 3.85V, the IC will recognize the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and V_{EN} > 2V, the IC will enter start-up sequence for both VDD and VDDNB rail. If the voltage of VCC and EN pin drop below low threshold, the IC will enter power down sequence and all the functions will be disabled. Normally, connecting system power to the EN pin is recommended. The SVID will be ready in 2ms (max) after the chip has been enabled. All the protection latches (OVP, OCP, UVP) will be cleared only after POR = low. The condition of V_{EN} = low will not clear these latches.

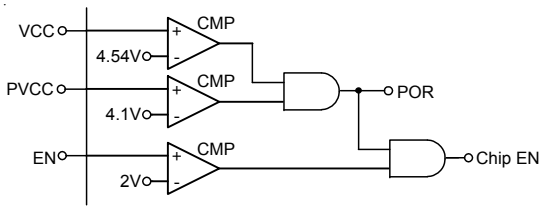

Figure 1. Power Ready (POR) Detection

Boot VID

When EN goes high, both VDD and VDDNB output begin to soft-start to the Boot VID in CCM. Table 7 shows the Boot VID setting. The Boot VID is determined by the SVC and SVD input states at EN rising edge and it is in the internal register. The digital soft-start circuit ramps up the reference voltage at a controlled slew rate to reduce inrush current during start-up. When all the output voltages are above power good threshold (300mV below Boot VID) at the end of soft-start, the controller asserts power good (PGOOD) after a time delay.

Table 7. 2-Bit Boot VID Code

Initial Startup VID (Boot VID)		
SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Start-Up Sequence

After EN goes high, the RT3662AM starts up and operates according to the initial settings. Figure 2 shows the simplified sequence timing diagram. The detailed operation is described in the following.

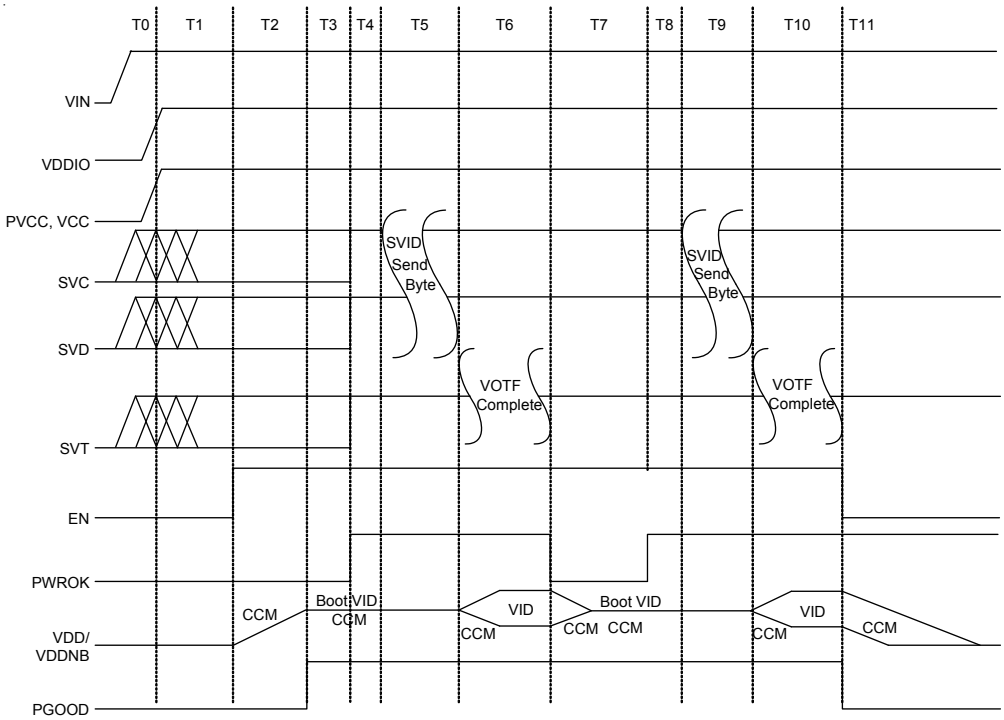

Figure 2. Simplified Sequence Timing Diagram

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Description of Figure 2 :

T0: When the VIN power is ready, the RT3662AM will wait for VCC and PVCC POR.

T1: VDDIO power is ready, and the BOOT VID can be set by SVC pin and SVD pin, and latched at EN rising edge. SVT is driven high by the RT3662AM.

T2: The enable signal goes high and all output voltages ramp up to the Boot VID in CCM. The soft-start slew rate is 2.5mV/ms.

T3: All output voltages are within the regulation limits and the PGOOD signal goes high.

T4: The PWROK pin goes high and the SVI2 interface starts running. The RT3662AM waits for SVID command from processor.

T5: A valid SVID command transaction occurs between the processor and the RT3662AM.

T6: The RT3662AM starts VOTF (VID on-the-Fly) transition according to the received SVID command and send a VOTF Complete if the VID is greater than BOOT VID and reaches target VID.

T7: The PWROK pin goes low and the SVI2 interface stops running. All output voltages go back to the Boot VID in CCM.

T8: The PWROK pin goes high again and the SVI2 interface starts running. The RT3662AM waits for SVID command from processor.

T9: A valid SVID command transaction occurs between the processor and the RT3662AM.

T10: The action is same with T6. The RT3662AM starts VID on-the-Fly transition and send a VOTF Complete if the VID up and reaches target VID.

T11: The enable signal goes low and all output voltages enter soft-shutdown mode. The soft-shutdown slew rate is 2.5mV/ms.

Power-Down Sequence

If the voltage at the EN pin falls below the enable falling threshold, the controller is disabled. The voltage at the PGOOD pin will immediately go low when EN pin signal goes low, and the controller executes soft-shutdown operation. The internal digital circuit ramps down the reference voltage at the same slew rate as that of in soft-start, making VDD and VDDNB output voltages gradually decrease in CCM. The Boot VID information stored in the internal register is cleared at POR. This event forces the RT3662AM to check the SVC and SVD inputs for a new boot VID when the EN voltage goes high again.

PGOOD

The PGOOD is open-drain logic output. It provides the power good signal when VDD and VDDNB output voltage are within the regulation limits and no protection is triggered. The pin is typically tied to 3.3V or 5V power source through a pull-high resistor. During shutdown state (EN = low) and the soft-start period, the PGOOD voltage is pulled low. After a successful soft-start and VDD and VDDNB output voltages are within the regulation limits, the PGOOD is released high.

The voltage at the PGOOD pin will be pulled low when any of the following events occurs : over-voltage protection, under-voltage protection, over-current protection, and logic low EN voltage. If one rail triggers protection, the PGOOD will be pull low.

SVI2 Wire Protocol

The RT3662AM complies with AMD' s Voltage Regulator Specification, which defines the Serial VID Interface 2.0 (SVI2) protocol. With SVI2 protocol, the processor directly controls the reference voltage level of each individual controller channel and determines which controller operates in power saving mode. The SVI2 interface is a three-wire bus that connects a single master to one or above slaves. The master initiates and terminates SVI2 transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave drives the telemetry, SVT during a transaction. The AMD processor is always the master. The voltage regulator controller (RT3662AM) is always the slave. The RT3662AM receives the SVID code and acts accordingly. The SVI protocol supports 20MHz high speed mode I^2C, which is based on SVD data packet. Table 8 shows the SVD data packet. A SVD packet consists of a "Start" signal, three data bytes after each byte, and a "Stop" signal. The 8-bit serial VID codes are listed in Table1. After the RT3662AM has received the

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stop sequence, it decodes the received serial VID code and executes the command. The controller has the ability to sample and report voltage and current for the VDD and VDDNB domains. The controller reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. A bit TFN at SVD packet along with the VDD and VDDNB domain selector bits are used by the processor to change the telemetry functionality. The telemetry bit definition is listed in Figure 3. The detailed SVI2 specification is outlined in the AMD Voltage Regulator and Voltage Regulator Module (VRM) and Serial VID Interface 2.0 (SVI2) Specification.

Table 8. SVD Data Packet

Bit Time	Description
1 : 5	Always 11000b
6	VDD domain selector bit, if set then the following two data bytes contain the VID, the PSI state, and the load-line slope trim and offset trim state for VDD.
7	VDDNB domain selector bit, if set then the following two data bytes contain the VID, the PSI state, and the load-line slope trim and offset trim state for VDDNB.
8	Always 0b
10	PSI0_L
11 : 17	VID Code bits [7:1]
19	VID Code bit [0]
20	PSI1_L
21	TFN (Telemetry Functionality)
22 : 24	Load Line Slope Trim [2:0]
25 : 26	Offset Trim [1:0]

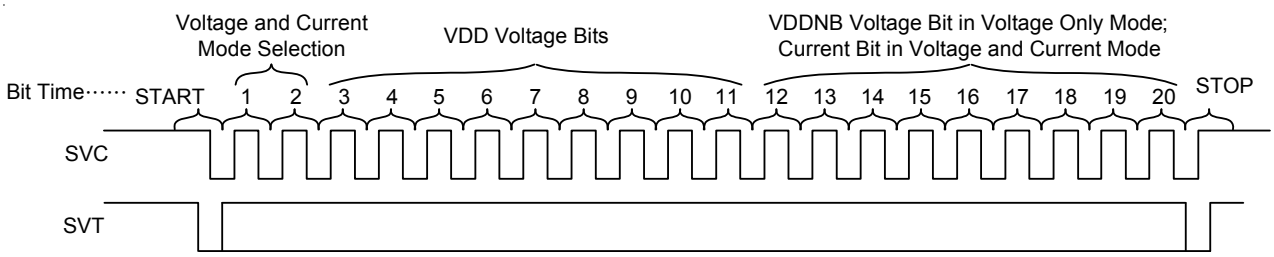

Figure 3. Telemetry Bit Definition

PWROK and SVI2 Operation

The PWROK pin is an input pin, which is connected to the global power good signal from the platform. Logic high at this pin enables the SVI2 interface, allowing data transaction between processor and the RT3662AM. Once the RT3662AM receives a valid SVID code, it decodes the information from processor to determine which output plane is going to move to the target VID. The internal DAC then steps the reference voltage in a controlled slew rate, making the output voltage shift to the required new VID. Depending on the SVID code, more than one controller channel can be targeted simultaneously in the VID transition. For example, VDD and VDDNB voltages can ramp up/down at the same time.

If the PWROK input goes low during normal operation, the SVI2 protocol stops running. The RT3662AM immediately drives SVT high and modifies all output voltages back to the Boot VID, which is stored in the internal register right after the controller is enabled. The controller does not read SVD and SVC inputs after the loss of PWROK. If the PWROK input goes high again, the SVI2 protocol resumes running. The RT3662AM then waits to decode the SVID command from processor for a new VID and acts as previously described. The SVI2 protocol is only runs when the PWROK input goes high after the voltage at the EN pin goes high.

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VID On-the-Fly Transition

After the RT3662AM has received a valid SVID code, it executes the VID on-the-Fly transition by stepping up/down the reference voltage of the required controller channel in a controlled slew rate, hence allowing the output voltage to ramp up/down to target VID.

During the VID on-the-Fly transition, the RT3662AM will force CCM operation in high performance mode. If the controller channel operates in the power-saving mode prior to the VID on-the-Fly transition, it will change to high performance mode and implement CCM operation when the controller implement VID up, and then back to the VID up PS command after VID achieve target voltage at 20μs to 40μs; if the controller implement VID down in power-saving mode, it will decay down and keep in power-saving mode. The voltage at the PGOOD pin will keep high during the VID on-the-Fly transition. The RT3662AM send a VOTF complete only at the end of VID up transition. In the event of receiving a VID off code, the RT3662AM steps the reference voltage of required controller channel down to zero, hence making the required output voltage decrease to zero, and the voltage at the PGOOD pin will remain high since the VID code is valid.

Power State Transition

The RT3662AM supports power state transition function in VDD and VDDNB VR for the PSI[x]_L command from AMD processor. The PSI[x]_L bit in the SVI2 protocol controls the operating mode of the RT3662AM controller channels. The default operation mode of VDD and VDDNB VR is full-phase CCM.

When the VDD VR is in N phase configuration and receives PSI0_L = 0 and PSI1_L = 0 or 1, the VDD VR will entry 1-phase diode emulation mode. When the VDD VR receives PSI0_L = 1 and PSI1_L = 0, the VDD VR remains 1-phase diode emulation mode. In reverse, the VDD VR goes back to N phase operation in CCM upon receiving PSI0_L = 1 and PSI1_L = 1, see Table 9. When the VDDNB VR receives PSI0_L = 0 and PSI1_L = 0 or 1, it enters 1-phase diode emulation mode. If the VDDNB VR receives PSI0_L = 1 and PSI1_L = 0, it remains 1-phase diode emulation mode. The VDDNB VR will go back to 1-phase CCM operation after receiving PSI0_L = 1 and PSI1_L = 1, see Table 10.

Table 9. VDD VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
2	11	2 phase CCM
	10	1 phase DEM
	01	
	00	
1	11	1 phase CCM
	10	1 phase DEM
	01	
	00	

Table 10. VDDNB VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
1	11	1 phase CCM
	10	1 phase DEM
	01	
	00	

Differential Remote Sense Setting

The VDD and VDDNB controllers have differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, processor internal power routes and socket contacts. The processor contains on-die sense pins, including of VDD_SENSE, VDDNB_SENSE and VSS_SENSE. Connect RGND to VSS_SENSE. For VDD controller, connect FB to VDD_SENSE with a resistor to build the negative input path of the error amplifier. Connect FB_NB to VDDNB_SENSE with a resistor using the same way in VDD controller. Connect VSS_SENSE to RGND using separate trace as shown in Figure 4. The precision reference voltages refer to RGND for accurate remote sensing.

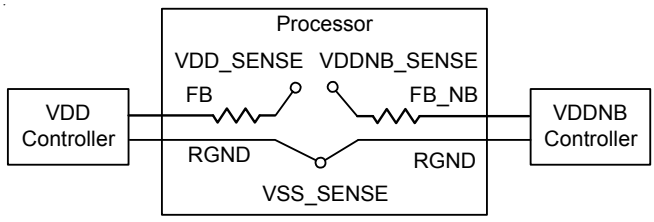

Figure 4. Differential Remote Voltage Sense Connection

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SET1 Pin Setting

The RT3662AM provides the SET1 pin for platform users to set the VDD and VDDNB controller current gain ratio (AI_VDD, AI_VDDNB), VDD controller QR threshold (QR_TH) and VDDNB voltage reporting offset bit[1:3] (VDDNB_RPT_OFS). Platform designers should use resistive voltage divider on the pin, refer to Figure 5. The voltage (VREF) at VREF_PINSET pin will be pulled up to 3.2V for SET1 pin setting after power ready (POR), and then the voltage will change and fix to 0.8V with a delay time for normal operation.

The divided voltage at the SET1 pin as below :

$$V_{SET1_DIV} = 3.2 \times \frac{R_D}{R_U + R_D}$$

The ADC monitors and decodes the voltage at this pin only once after power up. After ADC decoding (only once), a 80μA current (when VCC = 5V) will be generated at the SET1 pin for pin setting. That is the voltage at SET1 pin described as below:

$$V_{SET1_IR} = 80\mu \times \frac{R_U \times R_D}{R_U + R_D}$$

From equation (1) and (2) and Table 2 and 3, platform users can set the above described pin setting functions.

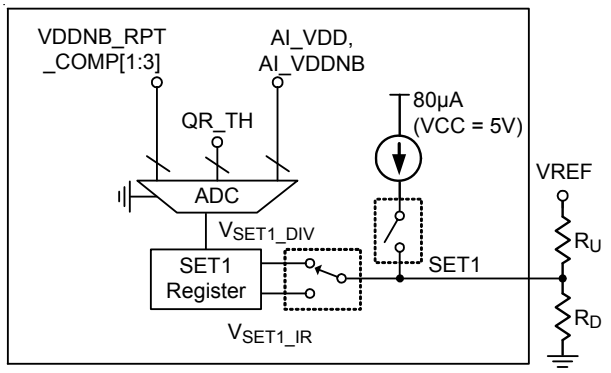

Figure 5. SET1 Pin Setting

TSEN and TSEN_NB Pin Setting

The RT3662AM provides the TSEN and TSEN_NB pins for platform users to set the pin setting functions, including the VDD and VDDNB controller switching frequency (F_{SW}), Initial offset, Per-phase over current protection (PHOCP) and VDDNB voltage reporting offset bit[0] (VDDNB_RPT_OFS). Platform designers should use resistive voltage divider on the pins, refer to Figure 6. The voltage (VREF) at VREF_PINSET pin will be pulled up to 3.2V for TSEN and TSEN_NB pin setting after power ready (POR), and then the voltage will change and fix to 0.8V with a delay time for normal operation.

The divided voltage at the TSEN and TSEN_NB pin described as below:

$$V_{TSEN_DIV} = 3.2 \times \frac{R_{p2}}{R_{p1} + R_{p2}}$$

$$V_{TSEN_NB_DIV} = 3.2 \times \frac{R_{p4}}{R_{p3} + R_{p4}}$$

The ADC monitors and decodes the voltage at this pin only once after power up. After ADC decoding (only once), a 80mA current (when VCC = 5V) will be generated at the TSEN and TSEN_NB pin for thermal indicator and protection functions.

From equation (3) and (4) and Table 4 and 5, platform users can set the above described pin setting functions.

Thermal Indicator

Refer to Figure 6, the RT3662AM provides the thermal indicator function. The VRHOT_L pin is an open-drain output which is used for VR thermal indicator. When the sensed voltage at TSEN or TSEN_NB pin is less than 2.2V, the VRHOT_L signal will be pulled low to notify CPU that the temperature is over the VRHOT temperature threshold.

After TSEN and TSEN_NB pin setting, a 80mA current (when VCC = 5V) will be generated at the TSEN and TSEN_NB pin for thermal indicator function. And the voltage at TSEN and TSEN_NB pin as below:

$$V_{TSEN} = 80\mu A \cdot \left[\left(\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}} \right) + \left(\frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} \right) \right] + VREF \cdot \left(\frac{R_{p2}}{R_{p1} + R_{p2}} \right)$$

$$V_{TSEN_NB} = 80\mu A \cdot \left[\left(\frac{R_2 \cdot R_{NTC}}{R_2 + R_{NTC}} \right) + \left(\frac{R_{p3} \cdot R_{p4}}{R_{p3} + R_{p4}} \right) \right] + VREF \cdot \left(\frac{R_{p4}}{R_{p3} + R_{p4}} \right)$$

Due to the VREF reference voltage cause the thermal compensation become complex. In this way, the sensed voltage related VREF will be eliminated in ADC block. The actual sensed voltage at TSEN and TSEN_NB pin described as below:

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$$V_{TSEN_ADC} = 80\mu A \cdot \left[\left(\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}} \right) + \left(\frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} \right) \right]$$

$$V_{TSEN_NB_ADC} = 80\mu A \cdot \left[\left(\frac{R_2 \cdot R_{NTC}}{R_2 + R_{NTC}} \right) + \left(\frac{R_{p3} \cdot R_{p4}}{R_{p3} + R_{p4}} \right) \right]$$

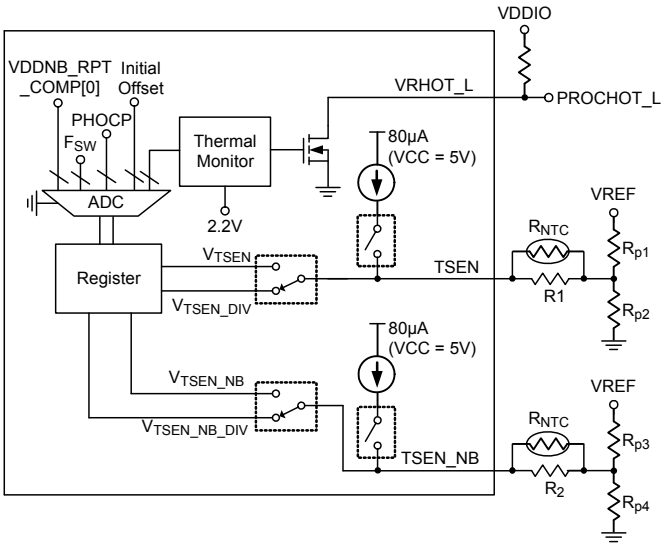

Figure 6. TSEN and TSEN_NB Circuit

VDD Controller

Active Phase Determination

The number of active phases is determined by the internal circuitry that monitors the ISEN2P voltage during start-up. Normally, the VDD controller operates as a 2-phase PWM controller. Pulling ISEN2P to VCC programs a 1-phase operation. At EN rising edge, VDD controller detects whether the voltage of ISEN2P is higher than "VCC - 0.5V" to decide how many phases should be active and the active phase number is determined and latched.

Loop Control

The VDD controller adopts Richtek's proprietary G-NAVP™ topology. The G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{VDD} will decrease with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 7.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases (V_{CS} increases), the steady state COMP voltage also increases and induces V_{VDD_SENSE} to decrease, thus achieving AVP. A near -DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

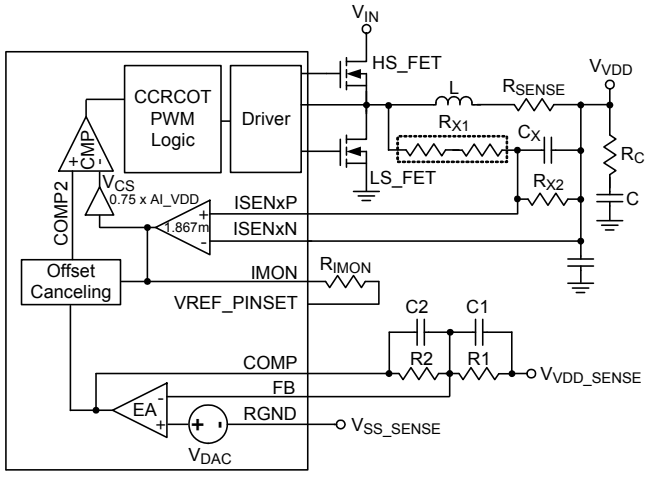

Figure 7. VDD Controller: Simplified Schematic with Voltage Loop and Current Loop

Current Signal Sensing

Refer to Figure 7, for different R_{SENSE} resistor, the current sense method can classify as two types. The method1 only use R_{X1} for lower R_{SENSE} application, and the method2 use R_{X1} and R_{X2} to divide the current signal for higher R_{SENSE} application. Richtek also provide Excel based design tool to let user choose the appropriate components quickly.

The current sense topology of the VDD controller is continuous inductor current sensing. Therefore, the controller has less noise sensitive. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENxP and ISEN1N pins denote the positive and negative input of the current sense amplifier.

In order to optimize transient performance, the recommended R_{eq} and C_X will be set according to the equations as below, t recommended set to 1.1.

$$R_{eq} \times C_X = \tau \times \frac{L}{R_{SENSE}}$$

Method1 : $R_{eq} = R_{X1}$

Method1 : $R_{eq} = \frac{R_{X1} \times R_{X2}}{R_{X1} + R_{X2}}$

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Considering the inductance tolerance, the resistor R_{eq} has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load-line requirement and the response time is too fast causing a ring back, the value of resistance should be increased. Vice versa, with a high resistance, the output voltage transient has only a small initial dip with a slow response time. R_X is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. C_X is suggested X7R type for the application.

Droop Setting

It is very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics as shown in Figure 8. This target is to have

$V_{VDD} = V_{DAC} - I_{LOAD} \times R_{DROOP}$

Then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 7 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}}$$

$$G_I = R_{SENSE} \times 1.867m \times R_{IMON} \times 0.75 \times AI_VDD$$

$$G_I = R_{SENSE} \times \frac{R_{X2}}{R_{X1} + R_{X2}} \times 1.867m \times R_{IMON} \times 0.75 \times AI_VDD$$

Where G_I is the current sense amplifier gain. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the equivalent resistance of the inductor. R_{IMON} is the IMON equivalent resistance. For the PHOCP accuracy, the R_{IMON} resistor need to set in 8kΩ to 70kΩ. AI_VDD is the VDD controller current gain ratio set by SET1 pin setting. R_{DROOP} is the equivalent load-line resistance as well as the desired static output impedance.

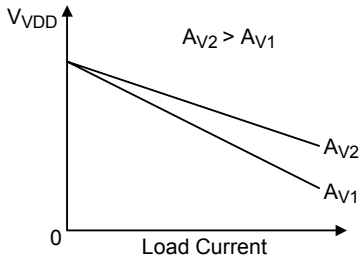

Figure 8. VDD Controller: Error Amplifier gain (A_V) Influence on V_{VDD} Accuracy

Loop Compensation

Optimized compensation of the VDD controller allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 9 shows the compensation circuit. Previous design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero:

$$f_P = \frac{1}{2\pi \times C \times R_C}$$

Where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows:

$$C2 = \frac{C \times R_C}{R2}$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}}$$

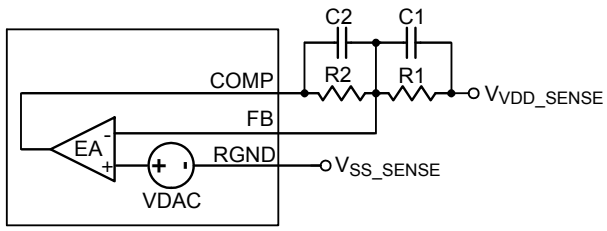

Figure 9. VDD Controller: Compensation Circuit

Current Balance

The VDD controller implements internal current balance mechanism in the current loop. The VDD controller senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase will be adjusted to be shorter.

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Figure 10 is the recommended current balance circuit for two phase application due to R_{PCB1} and R_{PCB2} are difficult to control very close. Detail derivative equations are as below.

$$V_{ISEN1P} = \frac{(V_{1P} + V_2)}{2}$$

$$V_{ISEN2P} = \frac{(V_{2P} + V_1)}{2}$$

$$V_A = \frac{(V_1 + V_2)}{2}$$

$$V_{1P\text{-}1N} = V_{ISEN1P} - V_A = \frac{(V_{1P} - V_1)}{2}$$

$$V_{2P\text{-}1N} = V_{ISEN2P} - V_A = \frac{(V_{2P} - V_2)}{2}$$

$$\because \frac{(V_{1P} - V_1)}{2} = \frac{(V_{2P} - V_2)}{2}$$

$$\because \frac{(V_{1P} - V_1)}{2} = \frac{(V_{2P} - V_2)}{2}$$

$$\because I_{L1} \times DCR_1 = I_{L2} \times DCR_2$$

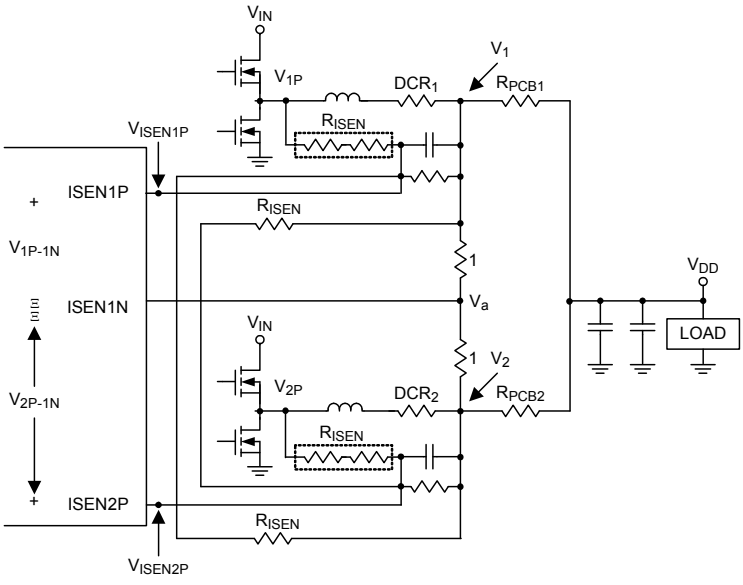

Figure 10. Recommended Current Balance Circuit for Two Phase Application

Initial and Dynamic Offset

The VDD controller features initial and dynamic offset function. The VDD rail initial offset function can be implemented through the TSEN pin setting. And the dynamic offset can be implemented by SVI2 interface, it controlled by CPU. Consider the offset factor, the VDD output voltage described as below:

$$V_{VDD} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{INI_OFS} + V_{DYN_OFS}$$

V_{INI_OFS} is the initial offset voltage set by pin setting function, and the dynamic offset voltage, V_{DYN_OFS}, controlled by CPU, and it can be set through the SVI2 interface.

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The RT3662AM will hold the inductor current to hold the load-line during a dynamic VID event. The VDD controller will always enter full-phase configuration when it receives dynamic VID up command; If VDD controller receives dynamic VID down command, it will hold the operating state.

When the VID CCM down on light loading condition, the negative inductor current will be produced, and it may cause the audio noise and phase ring effect. For improving the problems, the controller set the dynamic VID down slew rate to 0.625mV/ms, the action will reduce the negative current and phase ring effect.

Ramp Compensation

G-NAVP™ topology is one type of ripple based control that has fast transient response. However, ripple based control usually don't have good noise immunity. The RT3662AM provides a ramp compensation to increase noise immunity and reduce jitter at the switching node, refer to Figure 11 shows the ramp compensation. When the VDD controller takes phase shedding operation and enters diode emulation mode, the internal ramp of VDD controller will be modified for the reason of stability.

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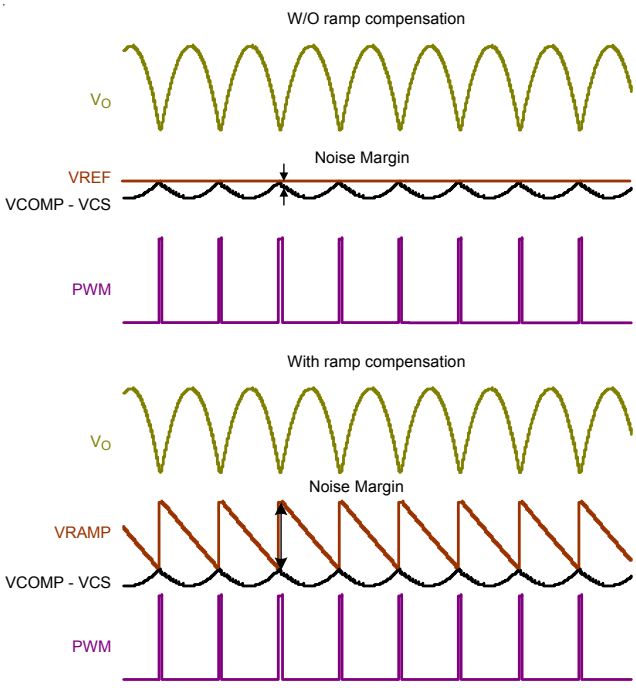

Figure 11. Ramp Compensation

Current Monitoring and Reporting

The VDD controller provides current monitoring function via inductor current sensing. In the G-NAVP™ technology, the output voltage is dependent on output current, and the current monitoring function is achieved by this characteristic of output voltage. The equivalent output current will be sensed from inductor current sensing and mirrored to the IMON pin. The resistor connected to the IMON pin determines voltage of the IMON output.

For Method1 current sensing :

$$V_{IMON} = I_{L,SUM} \times DCR_L \times 1.867m \times R_{IMON} + 0.8$$

Where $I_{L,SUM}$ is the VDD output current, DCR_L is the current sense resistance, R_{IMON} is the IMON pin equivalent setting resistor, and the current sense gain equal to 1.867m.

The ADC circuit of the VDD controller monitors the voltage variation at the IMON pin, and this voltage is decoded into digital format and stored into output current register.

$$DIMON = \frac{V_{IMON} - 0.8}{0.8} \times 255 \quad \text{(Bits)}$$

Quick Response

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, the output voltage generate undershoot to fail specification. The RT3662AM has Quick Response (QR) mechanism which is able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping. The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. Refer to Figure 12, the output voltage signal is via a remote sense line to connect at the VSEN pin. The QR threshold can be set by SET1 pin setting for VDD controller refers to Table 3.

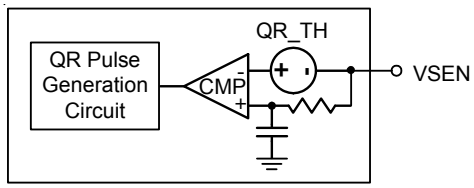

Figure 12. VDD Controller: Quick Response Triggering Circuit

Over-Current Protection

The RT3662AM provides the over current protection function. The OCP_SPIKE threshold will be set by the current monitor resistor R_{IMON} as below :

For Method1 current sensing :

$$OCP_SPIKE = \frac{1.6 - 0.8}{DCR_L \times 1.867m \times R_{IMON}}$$

For prevent the OCP false trigger, the trigger delay is requirement, refer to Electrical Characteristics. When output current is still higher than the OCP_SPIKE after the trigger delay time, the OCP will be latched, and then the VDD controller will turn off both high-side and low-side MOSFETs of all channels.

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Per-Phase Over Current Protection

The VDD controller provides per-phase over current protection (PHOCP) function in each phase. If the VDD controller force 1 phase operation by pulling ISEN2P pin to 5V, it only detected at soft-start duration when VR power on. The VDD PHOCP threshold is set by TSEN pin setting described as below :

$$PHOCP_TH = OCP_SPIKE \times \frac{N}{M}$$

N is the VDD PHOCP setting ratio, M is the operation phase number.

If the PHOCP is triggered, the controller will turn off all high-side and low-side MOSFETs to protect CPU.

Over-Voltage Protection (OVP)

The OVP circuit of the VDD controller monitors the output voltage via the VSEN pin after POR. When the VSEN voltage exceeds the OVP threshold 1.85V, OVP is triggered and latched. The VDD controller will try to turn on low-side MOSFET and turn off high-side MOSFET of all active phases to protect the CPU. When OVP is triggered by one rail, the other rail will also enter soft shut down sequence. A 1ms delay is used in OVP detection circuit to prevent false trigger.

Under-Voltage Protection (UVP)

The VDD controller implements UVP of VSEN pin. If VSEN voltage is less than the internal reference by 500mV, the VDD controller will trigger UVP latch. The UVP latch will turn off both high-side and low-side MOSFETs. When UVP is triggered by one rail, the other rail will also enter soft shutdown sequence. A 3ms delay is used in UVP detection circuit to prevent false trigger.

Under-Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below IC POR threshold, the VDD controller will trigger UVLO. The UVLO protection forces all high-side and low-side MOSFETs off by shutting down internal PWM logic drivers. A 3ms delay is used in UVLO detection circuit to prevent false trigger.

VDDNB Controller

VDDNB Controller Disable

The VDDNB controller can be disabled by connecting ISENP_NB to a voltage higher than “VCC - 0.5V”. If not in use, ISENN_NB is recommended to be connected to VCC. When VDDNB controller is disabled, all SVID commands related to VDDNB controller will be rejected.

Loop Control

The VDDNB controller adopts Richtek’s proprietary G-NAVP™ topology. The G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{VDDNB} will decrease with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 13.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and induces V_{VDDNB_SENSE} to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

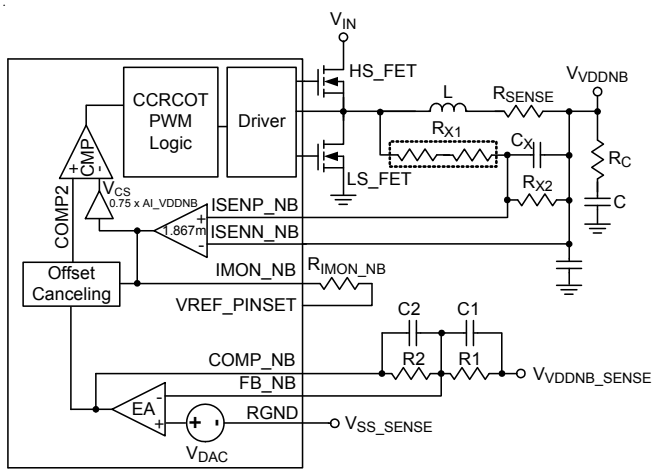

Figure 13. VDDNB Controller : Simplified Schematic with Voltage Loop and Current Loop

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Current Sense Setting

Refer to Figure 13, for different R_{SENSE} resistor, the current sense method can classify as two types. The method1 only use R_{X1} for lower R_{SENSE} application, and the method2 use R_{X1} and R_{X2} to divide the current signal for higher R_{SENSE} application. Richtek also provide Excel based design tool to let user choose the appropriate components quickly.

The current sense topology of the VDDNB controller is continuous inductor current sensing. Therefore, the controller has less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The ISENP_NB and ISENN_NB pins denote the positive and negative input of the current sense amplifier.

In order to optimize transient performance, the recommended R_{eq} and C_X will be set according to the equation as below, and t recommended set to 1.1.

$$R_{eq} \times C_X = \tau \times \frac{L}{R_{SENSE}}$$

Method1 : $R_{eq} = R_{X1}$

Method2 : $R_{eq} = \frac{R_{X1} \times R_{X2}}{R_{X1} + R_{X2}}$

Considering the inductance tolerance, the resistor R_{eq} has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load-line requirement and the response time is too fast causing a ring back, the value of resistance should be increased. Vice versa, with a high resistance, the output voltage transient has only a small initial dip with a slow response time. R_X is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. C_X is suggested X7R type for the application.

Droop Setting

It is very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics as shown in Figure 14. This target is to have

$V_{VDDNB} = V_{DAC} - I_{LOAD} \times R_{DROOP}$

Then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 12 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}}$$

Method1:

$$G_I = R_{SENSE} \times 1.867m \times R_{IMON} \times 0.75 \times AI_VDDNB$$

Method2:

$$G_I = R_{SENSE} \times \frac{R_{X2}}{R_{X1} + R_{X2}} \times 1.867m \times R_{IMON} \times 0.75 \times AI_VDDNB$$

Where G_I is the current sense amplifier gain. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the equivalent resistance of the inductor. R_{IMON_NB} is the IMON_NB equivalent resistance. For the PHOCP accuracy, the R_{IMON_NB} resistor need to set in 8kΩ to 70kΩ. AI_VDDNB is the VDDNB controller current gain ratio set by SET1 pin setting. R_{DROOP} is the equivalent load-line resistance as well as the desired static output impedance.

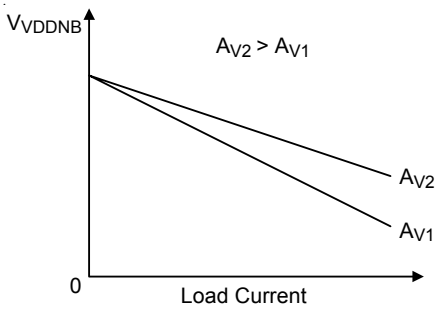

Figure 14. VDDNB Controller : Error Amplifier gain (A_V) Influence on V_{VDDNB} Accuracy

Loop Compensation

Optimized compensation of the VDDNB controller allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 15 shows the compensation circuit. Previous design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2\pi \times C \times R_C}$$

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Where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2}$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}}$$

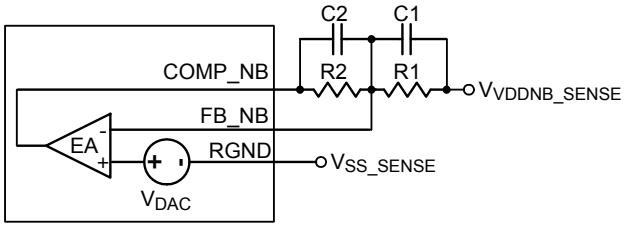

Figure 15. VDDNB Controller : Compensation Circuit

Initial and Dynamic Offset

The VDDNB controller features initial and dynamic offset function. The initial offset function can be implemented through the TSEN pin setting. And the Dynamic offset can be implemented by SVI2 interface, it controlled by CPU. Consider the offset factor, the VDDNB output voltage described as below :

$$V_{VDDNB} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{INI_OFS} + V_{DYN_OFS}$$

V_{INI_OFS} is the initial offset voltage set by pin setting function, and the dynamic offset voltage, V_{DYN_OFS}, controlled by CPU, and it can be set through the SVI2 interface.

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The RT3662AM will hold the inductor current to hold the load-line during a dynamic VID event. The VDDNB controller will always enter CCM operation when it receives dynamic VID up command; If VDD controller receives dynamic VID down command, it will hold the operating state.

When the VID CCM down on light loading condition, the negative inductor current will be produced, and it may cause the audio noise and phase ring effect. For improving the problems, the controller set the dynamic VID down slew rate to 0.625mV/ms, the action will reduce the negative current and phase ring effect.

Ramp Compensation

G-NAVP™ topology is one type of ripple based control that has fast transient response. However, ripple based control usually don't have good noise immunity. The RT3662AM provides a ramp compensation to increase noise immunity and reduce jitter at the switching node refer to Figure 11 shows the ramp compensation. When the VDDNB controller takes phase shedding operation and enters diode emulation mode, the internal ramp of VDDNB controller will be modified for the reason of stability.

Current Monitoring and Reporting

The VDDNB controller provides current monitoring function via inductor current sensing. In the G-NAVP™ technology, the output voltage is dependent on output current, and the current monitoring function is achieved by this characteristic of output voltage. The equivalent output current will be sensed from inductor current sensing and mirrored to the IMON_NB pin. The resistor connected to the IMON_NB pin determines voltage of the IMON_NB output.

For Method1 current sensing :

$$V_{IMON_NB} = I_{L,SUM} \times DCR_L \times 1.867m \times R_{IMON_NB} + 0.8$$

Where $I_{L,SUM}$ is the VDDNB output current, DCR_L is the current sense resistance, R_{IMON_NB} is the IMON_NB pin equivalent setting resistor, and the current sense gain equal to 1.867m.

The ADC circuit of the VDDNB controller monitors the voltage variation at the IMON_NB pin, and this voltage is decoded into digital format and stored into output current register.

$$DIMON_NB = \frac{V_{IMON_NB} - 0.8}{0.8} \times 255 \quad \text{(Bits)}$$

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VDDNB Voltage Reporting Offset

The VDDNB controller senses the ISENN_NB voltage for voltage reporting. In Figure 16, due to the PCB trace (R_{PCB}) from ISENN_NB to output capacitor, it will cause the voltage drop on loading, as the loading current become bigger, the drop will affect the voltage reporting seriously. Through the voltage reporting offset function, it can be improved, and the voltage reporting of VDDNB controller (V_{VDDNB_RPT}) can be described as below :

$$V_{VDDNB_RPT(d)} = V_{ISENN_NB_ADC(d)} - V_{VDDNB_RPT_OFS(d)}$$

V_{VDDNB_RPT} is the VDDNB voltage reporting digital code, $V_{ISENN_NB_ADC}$ is the ISENN_NB sensed voltage digital code and $V_{VDDNB_RPT_OFS}$ is the VDDNB voltage reporting offset bits.

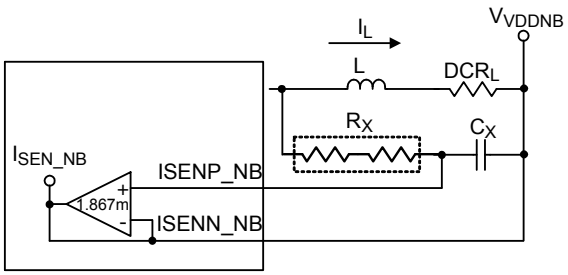

Figure 16. The Description of PCB trace from ISENN_NB to Output Capacitor

Over-Current Protection

The RT3662AM provides the over current protection function. The OCP_SPIKE_NB threshold will be set by the current monitor resistor R_{IMON_NB} as below :

For Method1 current sensing :

$$OCP_SPIKE_NB = \frac{1.6 - 0.8}{DCR_L \times 1.867m \times R_{IMON_NB}}$$

For prevent the OCP false trigger, the trigger delay is requirement, refer to Electrical Characteristics. When output current is still higher than the OCP_SPIKE_NB after the trigger delay time, the OCP will be latched, and then the VDDNB controller will turn off both high-side and low-side MOSFETs.

Per-Phase Over Current Protection

The VDDNB controller provides per-phase over current protection (PHOCP) function, it only detected at soft-start duration when VR power on. The PHOCP threshold is set by TSEN_NB pin setting described as below :

PHOCP_TH = OCP_SPIKE_NB x N

N is the VDDNB PHOCP setting ratio.

If the PHOCP is triggered, the controller will turn off all high-side and low-side MOSFETs to protect CPU.

Over-Voltage Protection (OVP)

The OVP circuit of the VDDNB controller monitors the output voltage via the ISENN_NB pin after POR. When the ISENN_NB voltage exceeds the OVP threshold 1.85V, OVP is triggered and latched. The VDDNB controller will try to turn on low-side MOSFET and turn off high-side MOSFET of all active phases to protect the CPU. When OVP is triggered by one rail, the other rail will also enter soft shut down sequence. A 1ms delay is used in OVP detection circuit to prevent false trigger.

Under-Voltage Protection (UVP)

The VDDNB controller implements UVP of ISENN_NB pin. If ISENN_NB voltage is less than the internal reference by 500mV, the VDDNB controller will trigger UVP latch. The UVP latch will turn off both high-side and low-side MOSFETs. When UVP is triggered by one rail, the other rail will also enter soft shutdown sequence. A 3ms delay is used in UVP detection circuit to prevent false trigger.

Under-Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below IC POR threshold, the VDDNB controller will trigger UVLO. The UVLO protection forces all high-side and low-side MOSFETs off by shutting down internal PWM logic drivers. A 3ms delay is used in UVLO detection circuit to prevent false trigger.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient

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temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.63W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 17 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

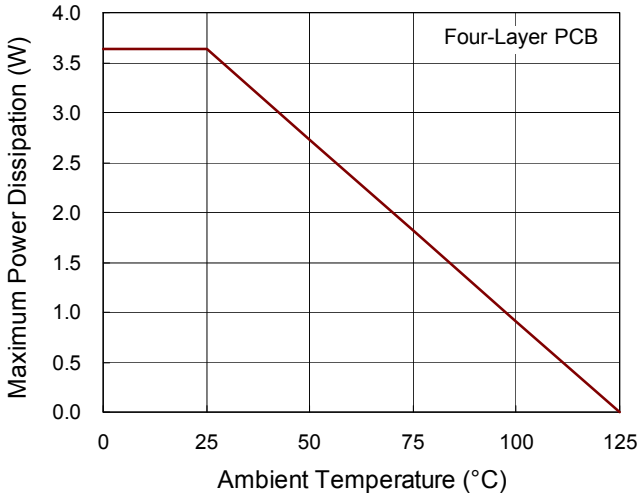

Figure 17. Derating Curve of Maximum Power Dissipation

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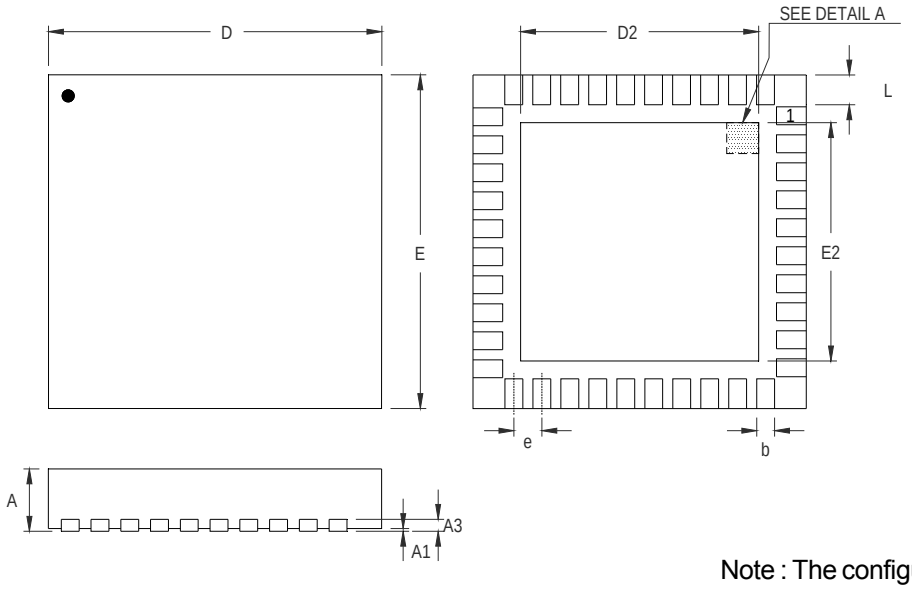
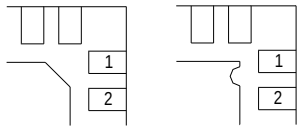
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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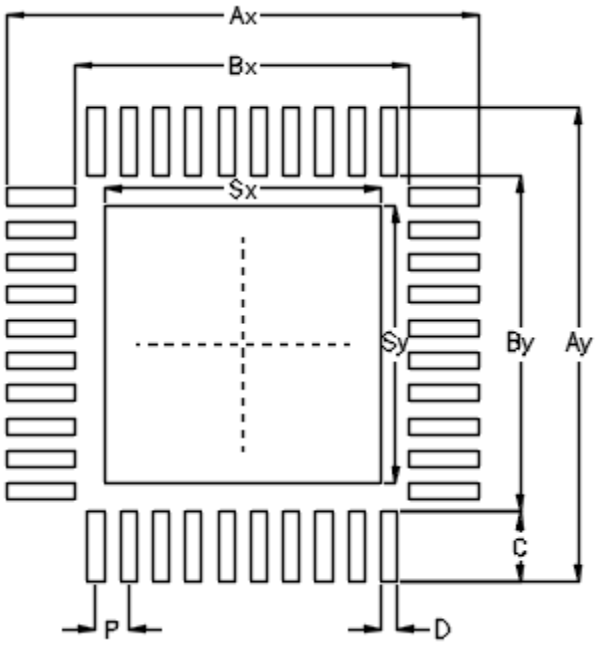
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

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