Dual-Output PWM Controller with 3 Integrated Drivers for AMD SVI2 Mobile CPU Power Supply

General Description

The RT3663BH is a 3 + 2 phases PWM controller, and is compliant with AMD SVI2 Voltage Regulator Specification to support both CPU core (VDD) and Northbridge portion of the CPU (VDDNB). The RT3663BH features CCRCOT (Constant Current Ripple Constant On-Time) with G-NAVP (Green-Native AVP), which is Richtek's proprietary topology. The G-NAVP makes it an easy setting controller to meet all AMD AVP (Adaptive Voltage Positioning) VDD/VDDNB requirements. The droop is easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance. The controller also uses the interface to issue VOTF Complete and to send digitally encoded voltage and current values for the VDD and VDDNB domains. It can operate in single phase and diode emulation mode and reach up to 90% efficiency in different modes according to different loading conditions. The RT3663BH provides special purpose offset capabilities by pin setting. The RT3663BH also provides power good indication, over-current indication (OCP_L) and dual OCP mechanism for AMD SVI2 CPU core and NB. It also features complete fault protection functions including over-voltage, under-voltage and negative-voltage protections.

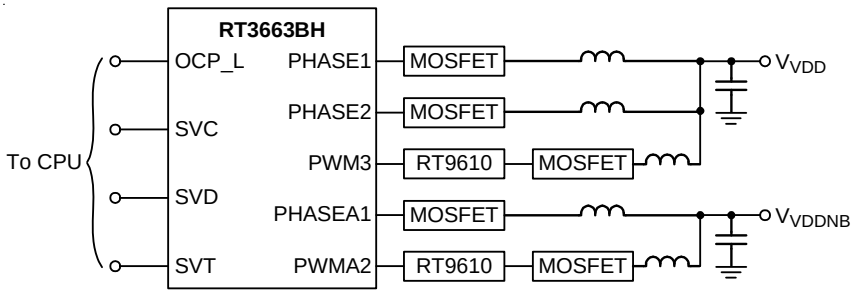
Features

- **3/2/1-Phase (VDD) + 2/1/0-Phase (VDDNB) PWM Controller**
- **3 Embedded MOSFET Drivers**
- **G-NAVP™ Topology**
- **Support Dynamic Load-Line and Zero Load-Line**
- **Diode Emulation Mode at Light Load Condition**
- **SVI2 Interface to Comply with AMD Power Management Protocol**
- **Built-In ADC for V_{OUT} and I_{OUT} Reporting**
- **Immediate OV, UV and NV Protections and UVLO**
- **Programmable Dual OCP Mechanism**
- **0.5% DAC Accuracy**
- **Fast Transient Response**
- **Power Good Indicator**
- **Over-Current Indicator**

Applications

- AMD SVI2 Mobile CPU
- Laptop Computer

Simplified Application Circuit



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Ordering Information

RT3663BH□□

Package Type
QW : WQFN-52L 6x6 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

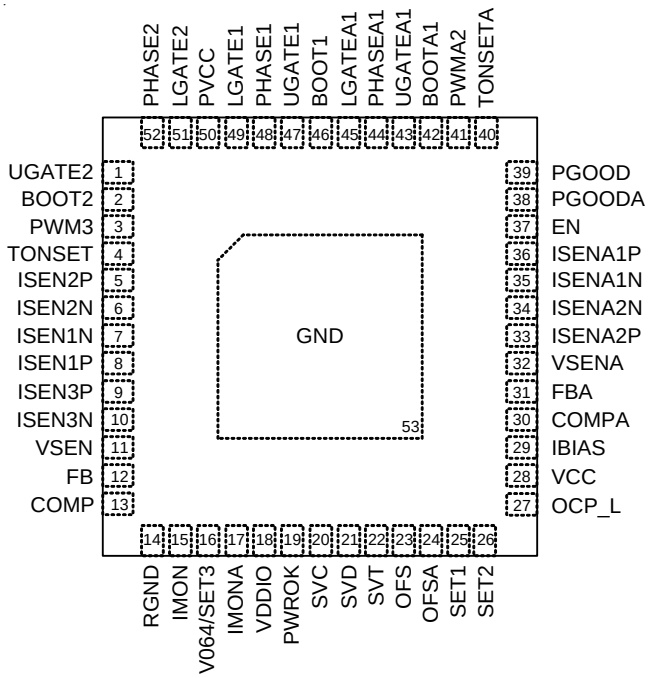
Marking Information

RT3663BHGQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-52L 6x6

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Functional Pin Description

Pin No.	Pin Name	Pin Function
3	PWM3	PWM outputs for Channel 3 VDD controller.
4	TONSET	VDD controller on-time setting. Connect this pin to the converter input voltage, VIN, through a resistor, RTON, to set the on-time of UGATE and also the output voltage ripple of VDD controller.
5, 8, 9	ISEN1P to ISEN3P	Positive current sense input of Channel 1, 2 and 3 for VDD controller.
6, 7, 10	ISEN1N to ISEN3N	Negative current sense input of Channel 1, 2 and 3 for VDD controller.
11	VSEN	VDD controller voltage sense input. This pin is connected to the terminal of VDD controller output voltage.
12	FB	Output voltage feedback input of VDD controller. This pin is the negative input of the error amplifier for the VDD controller.
13	COMP	Compensation node of the VDD controller.
14	RGND	Return ground of VDD and VDDNB controller. This pin is the common negative input of output voltage differential remote sense for VDD and VDDNB controllers.
15	IMON	Current monitor output for the VDD controller. This pin outputs a voltage proportional to the output current.
16	V064/SET3	This pin provides two functions: fixed 0.64v reference voltage output and current gain ratio setting for VDD and VDDNB controller. Connect a resistive voltage divider from VCC to GND and connect the joint of the voltage divider to this pin for current gain ratio setting. The pin also used to offset the output voltage of the IMON pin and the IMONA pin. Bypass this pin to GND with a 22nF ceramic capacitor for noise decoupling and pin setting accuracy.
17	IMONA	Current monitor output for the VDDNB controller. This pin outputs a voltage proportional to the output current.
18	VDDIO	Processor memory interface power rail and serves as the reference for PWROK, SVD, SVC and SVT. This pin is used by the VR to reference the SVI pins.
19	PWROK	System power good input. If PWROK is low, the SVI interface is disabled and VR returns to BOOT-VID state with initial load line slope and initial offset. If PWROK is high, the SVI interface is running and the DAC decodes the received serial VID codes to determine the output voltage.
20	SVC	Serial VID clock input from processor.
21	SVD	Serial VID data input from processor. This pin is a serial data line.
22	SVT	Serial VID telemetry input from VR. This pin is a push-pull output.
23	OFS	Over clocking offset setting for the VDD controller.
24	OFSA	Over clocking offset setting for the VDDNB controller.
25	SET1	1st platform setting. Platform can use this pin to set OCP_TDC threshold, DVID compensation bit1 and internal ramp slew rate.
26	SET2	2nd platform setting. Platform can use this pin to set quick response threshold, OCP_TDC trigger delay time, DVID compensation bit0 and over clocking offset enable setting.
27	OCP_L	Over-current indicator for dual OCP mechanism. This pin is an open-drain output.

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Pin No.	Pin Name	Pin Function
28	VCC	Controller power supply input. Connect this pin to 5V with an 1μF or greater ceramic capacitor for decoupling.
29	IBIAS	Internal bias current setting. Connect only a 100kΩ resistor from this pin to GND to generate bias current for internal circuit. Place this resistor as close to the IBIAS pin as possible.
30	COMPA	Compensation node of the VDDNB controller.
31	FBA	Output voltage feedback input of VDDNB controller. This pin is the negative input of the error amplifier for the VDDNB controller.
32	VSENA	VDDNB controller voltage sense input. This pin is connected to the terminal of VDDNB controller output voltage.
33, 36	ISENA2P, ISENA1P	Positive current sense input of Channel 1 and 2 for VDDNB controller.
34, 35	ISENA2N, ISENA1N	Negative current sense input of Channel 1 and 2 for VDDNB controller.
37	EN	Controller enable control input. A logic high signal enables the controller.
38	PGOODA	Power good indicator for the VDDNB controller. This pin is an open-drain output.
39	PGOOD	Power good indicator for the VDD controller. This pin is an open-drain output.
40	TONSETA	VDDNB controller on-time setting. Connect this pin to the converter input voltage, VIN, through a resistor, RTONNB, to set the on-time of UGATE_VDDNB and also the output voltage ripple of VDDNB controller.
41	PWMA2	PWM output for Channel 2 of VDDNB controller.
46, 2, 42	BOOT1, BOOT2, BOOTA1	Bootstrap supply for high-side MOSFET. This pin powers high-side MOSFET driver.
47, 1, 43	UGATE1, UGATE2, UGATEA1	High-side gate driver outputs. Connect this pin to Gate of high-side MOSFET.
48, 52, 44	PHASE1, PHASE2, PHASEA1	Switch nodes of high-side driver. Connect this pin to high-side MOSFET Source together with the low-side MOSFET Drain and the inductor.
49, 51, 45	LGATE1, LGATE2, LGATEA1	Low-side gate driver outputs. This pin drives the Gate of low-side MOSFET.
50	PVCC	Driver power. Connect this pin to GND by ceramic capacitor larger than 1μF.
53 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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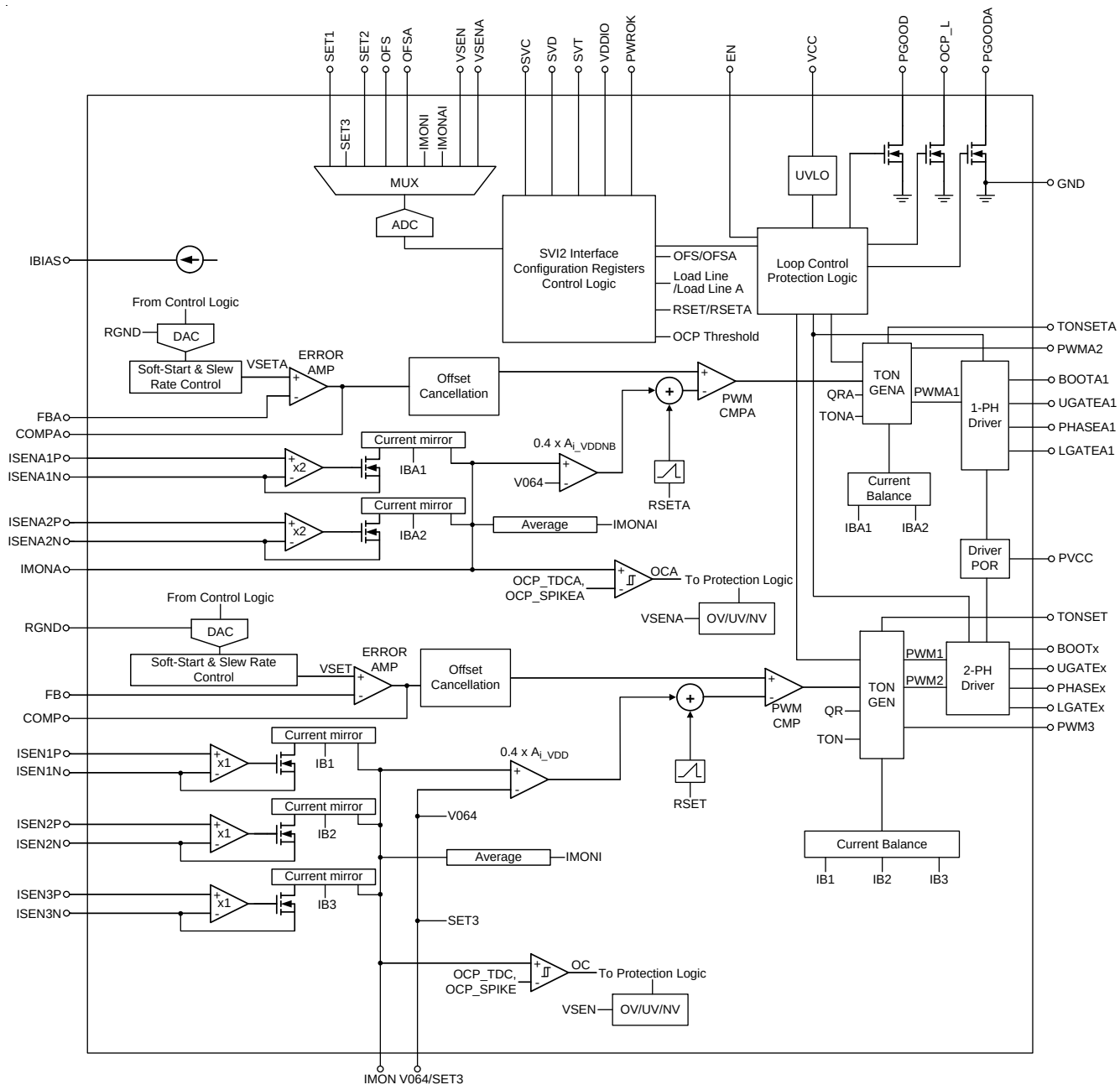
Functional Block Diagram



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Operation

MUX and ADC

The MUX supports the inputs from SET1, SET2, SET3, OFS, OFSA, IMON, IMONA, VSEN, or VSENA. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

SVI2 Interface

The SVI2 interface uses the SVC, SVD, and SVT pins to communicate with CPU. The RT3663BH's performance and behavior can be adjusted by commands sent by CPU or platform.

UVLO

The UVLO detects the VCC pin voltages for under voltage lockout protection and power on reset operation.

Loop Control Protection Logic

Loop control protection logic detects EN and UVLO signals to initiate soft-start function and control PGOOD, PGOODA and OCP_L signals after soft-start is finished. When dual OCP event occurs, the OCP_L pin voltage is pulled low.

DAC

The DAC receives VID codes from the SVI2 control logic to generate an internal reference voltage (VSET/VSETA) for controller.

Soft-Start and Slew-Rate Control

This block controls the slew rate of the internal reference voltage when output voltage changes.

Error Amplifier

The Error amplifier generates COMP/COMPA signal by the difference between VSET/VSETA and FB/FBA.

Offset Cancellation

This block cancels the output offset voltage from voltage ripple and current ripple to achieve accurate output voltage.

PWM CMPx

The PWM comparator compares COMP signal and current feedback signal to generate a signal for TONGENx.

TONGEN/TONGENA

This block generates an on-time pulse which high interval is based on the on-time setting and current balance.

Current Balance

Per-phase current is sensed and adjusted by adjusting on-time of each phase to achieve current balance for each phase.

OC/OV/UV/NV

VSEN/VSENA and output current are sensed for over-current, over-voltage, under-voltage, and negative-voltage protections.

RSET/RSETA

The Ramp generator is designed to improve noise immunity and reduce jitter.

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Table 1. Serial VID Codes

SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
0000_0000	1.55000	0010_0111	1.30625	0100_1110	1.06250	0111_0101	0.81875
0000_0001	1.54375	0010_1000	1.30000	0100_1111	1.05625	0111_0110	0.81250
0000_0010	1.53750	0010_1001	1.29375	0101_0000	1.05000	0111_0111	0.80625
0000_0011	1.53125	0010_1010	1.28750	0101_0001	1.04375	0111_1000	0.80000
0000_0100	1.52500	0010_1011	1.28125	0101_0010	1.03750	0111_1001	0.79375
0000_0101	1.51875	0010_1100	1.27500	0101_0011	1.03125	0111_1010	0.78750
0000_0110	1.51250	0010_1101	1.26875	0101_0100	1.02500	0111_1011	0.78125
0000_0111	1.50625	0010_1110	1.26250	0101_0101	1.01875	0111_1100	0.77500
0000_1000	1.50000	0010_1111	1.25625	0101_0110	1.01250	0111_1101	0.76875
0000_1001	1.49375	0011_0000	1.25000	0101_0111	1.00625	0111_1110	0.76250
0000_1010	1.48750	0011_0001	1.24375	0101_1000	1.00000	0111_1111	0.75625
0000_1011	1.48125	0011_0010	1.23750	0101_1001	0.99375	1000_0000	0.75000
0000_1100	1.47500	0011_0011	1.23125	0101_1010	0.98750	1000_0001	0.74375
0000_1101	1.46875	0011_0100	1.22500	0101_1011	0.98125	1000_0010	0.73750
0000_1110	1.46250	0011_0101	1.21875	0101_1100	0.97500	1000_0011	0.73125
0000_1111	1.45625	0011_0110	1.21250	0101_1101	0.96875	1000_0100	0.72500
0001_0000	1.45000	0011_0111	1.20625	0101_1110	0.96250	1000_0101	0.71875
0001_0001	1.44375	0011_1000	1.20000	0101_1111	0.95625	1000_0110	0.71250
0001_0010	1.43750	0011_1001	1.19375	0110_0000	0.95000	1000_0111	0.70625
0001_0011	1.43125	0011_1010	1.18750	0110_0001	0.94375	1000_1000	0.70000
0001_0100	1.42500	0011_1011	1.18125	0110_0010	0.93750	1000_1001	0.69375
0001_0101	1.41875	0011_1100	1.17500	0110_0011	0.93125	1000_1010	0.68750
0001_0110	1.41250	0011_1101	1.16875	0110_0100	0.92500	1000_1011	0.68125
0001_0111	1.40625	0011_1110	1.16250	0110_0101	0.91875	1000_1100	0.67500
0001_1000	1.40000	0011_1111	1.15625	0110_0110	0.91250	1000_1101	0.66875
0001_1001	1.39375	0100_0000	1.15000	0110_0111	0.90625	1000_1110	0.66250
0001_1010	1.38750	0100_0001	1.14375	0110_1000	0.90000	1000_1111	0.65625
0001_1011	1.38125	0100_0010	1.13750	0110_1001	0.89375	1001_0000	0.65000
0001_1100	1.37500	0100_0011	1.13125	0110_1010	0.88750	1001_0001	0.64375
0001_1101	1.36875	0100_0100	1.12500	0110_1011	0.88125	1001_0010	0.63750
0001_1110	1.36250	0100_0101	1.11875	0110_1100	0.87500	1001_0011	0.63125
0001_1111	1.35625	0010_0110	1.11250	0110_1101	0.86875	1001_0100	0.62500
0010_0000	1.35000	0100_0111	1.10625	0110_1110	0.86250	1001_0101	0.61875
0010_0001	1.34375	0100_1000	1.10000	0110_1111	0.85625	1001_0110	0.61250
0010_0010	1.33750	0100_1001	1.09375	0111_0000	0.85000	1001_0111	0.60625
0010_0011	1.33125	0100_1010	1.08750	0111_0001	0.84375	1001_1000	0.60000
0010_0100	1.32500	0100_1011	1.08125	0111_0010	0.83750	1001_1001	0.59375
0010_0101	1.31875	0100_1100	1.07500	0111_0011	0.83125	1001_1010	0.58750
0010_0110	1.31250	0100_1101	1.06875	0111_0100	0.82500	1001_1011	0.58125

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SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
1001_1100	0.57500	1011_0101 *	0.41875	1100_1110 *	0.26250	1110_0111*	0.10625
1001_1101	0.56875	1011_0110 *	0.41250	1100_1111 *	0.25625	1110_1000*	0.10000
1001_1110	0.56250	1011_0111 *	0.40625	1101_0000 *	0.25000	1110_1001*	0.09375
1001_1111	0.55625	1011_1000 *	0.40000	1101_0001 *	0.24375	1110_1010*	0.08750
1010_0000	0.55000	1011_1001 *	0.39375	1101_0010 *	0.23750	1110_1011*	0.08125
1010_0001	0.54375	1011_1010 *	0.38750	1101_0011 *	0.23125	1110_1100*	0.07500
1010_0010	0.53750	1011_1011 *	0.38125	1101_0100 *	0.22500	1110_1101*	0.06875
1010_0011	0.53125	1011_1100 *	0.37500	1101_0101 *	0.21875	1110_1110*	0.06250
1010_0100	0.52500	1011_1101 *	0.36875	1101_0110 *	0.21250	1110_1111*	0.05625
1010_0101	0.51875	1011_1110 *	0.36250	1101_0111 *	0.20625	1111_0000*	0.05000
1010_0110	0.51250	1011_1111 *	0.35625	1101_1000 *	0.20000	1111_0001*	0.04375
1010_0111	0.50625	1100_0000 *	0.35000	1101_1001 *	0.19375	1111_0010*	0.03750
1010_1000 *	0.50000	1100_0001 *	0.34375	1101_1010 *	0.18750	1111_0011*	0.03125
1010_1001 *	0.49375	1100_0010 *	0.33750	1101_1011 *	0.18125	1111_0100*	0.02500
1010_1010 *	0.48750	1100_0011 *	0.33125	1101_1100 *	0.17500	1111_0101*	0.01875
1010_1011 *	0.48125	1100_0100 *	0.32500	1101_1101 *	0.16875	1111_0110*	0.01250
1010_1100 *	0.47500	1100_0101 *	0.31875	1101_1110 *	0.16250	1111_0111*	0.00625
1010_1101 *	0.46875	1100_0110 *	0.31250	1101_1111 *	0.15625	1111_1000*	0.00000
1010_1110 *	0.46250	1100_0111 *	0.30625	1110_0000*	0.15000	1111_1001*	OFF
1010_1111 *	0.45625	1100_1000 *	0.30000	1110_0001*	0.14375	1111_1010*	OFF
1011_0000 *	0.45000	1100_1001 *	0.29375	1110_0010*	0.13750	1111_1011*	OFF
1011_0001 *	0.44375	1100_1010 *	0.28750	1110_0011*	0.13125	1111_1100*	OFF
1011_0010 *	0.43750	1100_1011 *	0.28125	1110_0100*	0.12500	1111_1101*	OFF
1011_0011 *	0.43125	1100_1100 *	0.27500	1110_0101*	0.11875	1111_1110*	OFF
1011_0100 *	0.42500	1100_1101 *	0.26875	1110_0110*	0.11250	1111_1111*	OFF

* Indicates TOB is 80mV for this VID code; unconditional VR controller stability required at all VID codes

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Table 2. SET1 Pin Setting for VDD Controller OCP_TDC threshold, DVID Compensation and RSET under V_{CC5} = 5V

SET1 Pin Voltage Before Current Injection V_{SET1} (mV)	OCP_TDC (Respect to OCP_SPIKE)	DVID Compensation [1]	RSET	SET1 Pin Voltage Before Current Injection V_{SET1} (mV)	OCP_TDC (Respect to OCP_SPIKE)	DVID Compensation [1]	RSET
34	60%	0	145%	836	60%	1	145%
59			130%	861			130%
85			115%	886			115%
110			100%	911			100%
135			85%	936			85%
160			70%	961			70%
235	70%	0	145%	1036	70%	1	145%
260			130%	1061			130%
285			115%	1086			115%
310			100%	1112			100%
335			85%	1137			85%
360			70%	1162			70%
435	75%	0	145%	1237	75%	1	145%
460			130%	1262			130%
485			115%	1287			115%
510			100%	1312			100%
535			85%	1337			85%
560			70%	1362			70%
636	Disable	0	145%	1437	Disable	1	145%
661			130%	1462			130%
686			115%	1487			115%
711			100%	1512			100%
736			85%	1537			85%
761			70%	1562			70%

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Table 3. SET1 Pin Setting for VDDNB Controller OCP_TDCA threshold, DVIDA Compensation and RSETA under V_{CC5} = 5V

SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)	OCP_TDCA (Respect to OCP_SPIKEA)	DVIDA Compensation [1]	RSETA	SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)	OCP_TDCA (Respect to OCP_SPIKEA)	DVIDA Compensation [1]	RSETA
34	60%	0	145%	836	60%	1	145%
59			130%	861			130%
85			115%	886			115%
110			100%	911			100%
135			85%	936			85%
160			70%	961			70%
235	70%	0	145%	1036	70%	1	145%
260			130%	1061			130%
285			115%	1086			115%
310			100%	1112			100%
335			85%	1137			85%
360			70%	1162			70%
435	75%	0	145%	1237	75%	1	145%
460			130%	1262			130%
485			115%	1287			115%
510			100%	1312			100%
535			85%	1337			85%
560			70%	1362			70%
636	Disable	0	145%	1437	Disable	1	145%
661			130%	1462			130%
686			115%	1487			115%
711			100%	1512			100%
736			85%	1537			85%
761			70%	1562			70%

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Table 4. SET2 Pin Setting for VDD Controller QR threshold,DVID Compensation and OCP Trigger Delay under V_{CC5} = 5V

SET2 Pin Voltage Before Current Injection V_{SET2} (mV)	QRTH (for VDD)	DVID Compensation [0]	OCPTRGDELAY (for VDD/VDDNB)
19	Disable	0	10ms
72			40ms
122			10ms
172			40ms
222	39mV	0	10ms
272			40ms
323			10ms
373			40ms
423	47mV	0	10ms
473			40ms
523			10ms
573			40ms
623	55mV	0	10ms
673			40ms
723			10ms
773			40ms
823	Disable	1	10ms
874			40ms
924			10ms
974			40ms
1024	39mV	1	10ms
1074			40ms
1124			10ms
1174			40ms
1224	47mV	1	10ms
1274			40ms
1324			10ms
1375			40ms
1425	55mV	1	10ms
1475			40ms
1525			10ms
1575			40ms

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Table 5. SET2 Pin Setting for VDDNB Controller QR threshold,DVIDA Compensation and External Offset Function under V_{CC5} = 5V

SET2 Pin Voltage Difference ΔV_{SET2} (Before and After Current Injection) (mV)	OFSENABLE	OFSAENABLE	DVIDA Compensation [0]	QRTHA (for VDDNB)
19	0	0	0	Disable
72				39mV
122				47mV
172				55mV
222			1	Disable
272				39mV
323				47mV
373				55mV
1224	1	1	0	Disable
1274				39mV
1324				47mV
1375				55mV
1425			1	Disable
1475				39mV
1525				47mV
1575				55mV

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Table 6. DVID Boost Compensation Setting

DVID Compensation [1]	DVID Compensation [0]	DVID Boost Compensation
0	0	22.5mV
0	1	18mV
1	0	13.5mV
1	1	9mV

Table 7. V064/SET3 Pin Setting for VDD and VDDNB Controller Current Gain Ratio under V_{CC5} =5V

V064/SET3 Pin Voltage (mV)	VDD Current Gain Ratio	VDDNB Current Gain Ratio	V064/SET3 Pin Voltage (mV)	VDD Current Gain Ratio	VDDNB Current Gain Ratio
1650	0LL	0LL	2450	50%	0LL
1750		25%	2550		25%
1850		50%	2650		50%
1950		100%	2750		100%
2050	25%	0LL	2850	100%	0LL
2150		25%	2950		25%
2250		50%	3050		50%
2350		100%	3150		100%

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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET, TONSETA to GND ---------- –0.3V to 28V
- BOOTx to PHASEx
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –5V to 7.5V
- PHASEx to GND
  - DC ---------- –0.3V to 32V
  - < 100ns ---------- –10V to 38V
- LGATEx to GND
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –2.5V to 7.5V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6.8V
  - < 100ns ---------- –5V to 7.5V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 2)
  - WQFN-52L 6x6, θ_{JA} ---------- 26.5°C/W
  - WQFN-52L 6x6, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC, PVCC ---------- 4.5V to 5.5V
- Input Voltage, VIN ---------- 4.5V to 24V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Supply Current	I_{VCC}	V_{EN} = 3V, not switching	--	12	--	mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
PVCC Supply Voltage	V_{PVCC}		4.5	--	5.5	V
PVCC Supply Current	I_{PVCC}	V_{BOOTx} = 5V, not switching	--	150	--	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Driver Power On Reset (Driver POR)						
Driver POR Threshold	V_{POR_R}	PVCC rising	--	3.85	4.1	V
	V_{POR_F}	PVCC falling	3.4	3.65	--	
Driver POR Hysteresis	V_{POR_HYS}		--	200	--	mV
Reference and DAC						
DC Accuracy	V_{FB}	V_{FB} = 1.0000 – 1.5500 (no load, CCM mode)	–0.5	0	0.5	%SVID
		V_{FB} = 0.8000 – 1.0000	–5	0	5	mV
		V_{FB} = 0.3000 – 0.8000	–8	0	8	
		V_{FB} = 0.2500 – 0.3000	–80	0	80	
RGND Current						
RGND Current	I_{RGND}	EN = 3V, not switching	--	200	--	μA
Slew Rate						
Dynamic VID Slew Rate	SR	Set VID	7.5	12	--	mV/μs
Error Amplifier						
Input Offset	V_{EAOFS}		--	--	2	mV
DC Gain	ADC	R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	10	--	MHz
Output Voltage Range	V_{COMP}		0.3	--	3.6	V
Maximum Source Current	IEA, SRC		1	--	--	mA
Maximum Sink Current	IEA, SNK		1	--	--	mA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–0.2	--	0.2	mV
Current Mirror Gain for CORE	$A_{MIRROR, VDD}$		97	--	103	%
Current Mirror Gain for NB	$A_{MIRROR, VDDNB}$		194	--	206	%
Internal Sum Current Sense DC Gain for CORE	Ai, VDD	VDD controller current gain ratio = 100%	--	0.4	--	V/V
Internal Sum Current Sense DC Gain for NB	Ai, VDDNB	VDDNB controller current gain ratio = 100%	--	0.8	--	V/V
Maximum Source Current	$I_{CS, SRC}$	0 < V_{FB} < 2.35	100	--	--	μA
Maximum Sink Current	$I_{CS, SNK}$	0 < V_{FB} < 2.35	10	--	--	μA
Zero Current Detection						
Zero Current Detection Threshold	V_{ZCD_TH}	V_{ZCD_TH} = GND – V_{PHASEx}	--	1	--	mV
Ton Setting						
TONSETx Pin Minimum Voltage	$V_{TON, MIN}$		--	0.5	--	V
TONSETx T_{ON}	t_{ON}	I_{RTON} = 80μA, V_{FB} = 1.1V	270	305	340	ns
TONSETx Input Current Range	I_{RTON}	V_{FB} = 1.1V	25	--	280	μA
Minimum T_{OFF}	t_{OFF}		--	250	--	ns

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS							
IBIAS Pin Voltage		V_{IBIAS}	R_{IBIAS} = 100k	1.97	2	2.03	V
V064							
Reference Voltage Output		V_{064}		0.56	0.64	0.72	V
Sink Current Capability		$I_{V064, SNK}$	V064 = 0.64V	800	--	--	μA
Source Current Capability		$I_{V064, SRC}$		--	--	100	μA
Board OFSx							
VFB Limit		$V_{FB, LIMIT}$		0	--	2.35	V
OFS Update Rate		f_{OFS}		--	50	--	kHz
Board Offset Resolution		ΔV_{OFS}		--	6.25	--	mV
Logic Inputs							
EN Input Voltage	Logic-High	V_{IH_EN}		2	--	--	V
	Logic-Low	V_{IL_EN}		--	--	0.8	
Leakage Current of EN		I_{LEK_EN}		–1	--	1	μA
SVC, SVD, SVT, PWROK	Logic-High	V_{IH_SVI}	Respect to VDDIO	70	--	100	%
	Logic-Low	V_{IL_SVI}	Respect to VDDIO	0	--	35	
Hysteresis of SVC, SVD, SVT, PWROK Input Voltage		V_{HYS_SVI}	Respect to VDDIO	10	--	--	%
Protection							
Under-Voltage Lockout Threshold		V_{UVLO}	VCC falling edge	4	4.2	4.4	V
Under-Voltage Lockout Hysteresis		ΔV_{UVLO}		--	100	--	mV
Under-Voltage Lockout Delay		t_{UVLO}	V_{CC} rising above UVLO threshold	--	3	--	μs
Over-Voltage Protection Threshold		V_{OVP}		275	325	375	mV
Over-Voltage Protection Delay		t_{OVP}	V_{SEN} rising above threshold	--	1	--	μs
Under-Voltage Protection Threshold		V_{UVP}	Respect to VID voltage	–575	–500	–425	mV
Under-Voltage Protection Delay		t_{UVP}	V_{SEN} falling below threshold	--	3	--	μs
Negative-Voltage Protection Threshold		V_{NV}		--	0	--	mV
Per Phase OCP Threshold		$I_{OCP_PERPHASE}$	I_{ISENxN} per-phase OCP threshold.	--	10	--	μA
Delay of Per Phase OCP		t_{PHOCP}		--	1	--	μs
OCP_SPIKE Threshold		I_{OCP_SPIKE}	DCR = 1.1mΩ, R_{SENSE} = 1.1kΩ, R_{IMON} = 34.3kΩ	63	75	86	A
OCP_SPIKE Action Delay		$t_{OCPSPIKE_ACTION_DLY}$		6	--	12	μs

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OCP_TDC Action Delay	$t_{OCPTDC_ACTION_DLY}$		12	--	24	μs
OCP_L, PGOOD and PGOODA						
Output Low Voltage at OCP_L	V_{OCP_L}	I_{OCP_L} = 4mA	0	--	0.2	V
OCP_L Assertion Time	t_{OCP_L}		2	--	--	μs
Output Low Voltage at PGOOD, PGOODA	V_{PGOOD}, V_{PGOODA},	I_{PGOOD} = 4mA, I_{PGOODA} = 4mA	0	--	0.2	V
PGOOD and PGOODA Threshold Voltage	V_{TH_PGOOD} V_{TH_PGOODA}	Respect to V_{BOOT}	--	–300	--	mV
PGOOD and PGOODA Delay Time	t_{PGOOD} t_{PGOODA}	V_{SEN} = V_{BOOT} to PGOOD/PGOODA high	70	100	130	μs
Current Report						
Maximum Reported Current (FFh = OCP)			--	100	--	%IDD_SPIKE_OCP
Minimum Reported Current (00h)			--	0	--	%IDD_SPIKE_OCP
IDDSpike Current Accuracy			--	--	3	%
Voltage Report						
Maximum Reported Voltage (0_00h)			--	3.15	--	V
Minimum Reported Voltage (1_F8h)			--	0	--	V
Voltage Accuracy			–2	--	2	LSB
PWM Driving Capability						
PWMx Source Resistance	R_{PWM_SRC}		--	20	--	Ω
PWMx Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
Switching Time						
UGATEx Rise Time	t_{UGATEr}	3nF load	--	8	--	ns
UGATEx Fall Time	t_{UGATEf}	3nF load	--	8	--	ns
LGATEx Rise Time	t_{LGATEr}	3nF load	--	8	--	ns
LGATEx Fall Time	t_{LGATEf}	3nF load	--	4	--	ns
UGATEx Turn-On Propagation Delay	t_{PDHU}	Outputs unloaded	--	20	--	ns
LGATEx Turn-On Propagation Delay	t_{PDHL}	Outputs unloaded	--	20	--	ns
Output						
UGATEx Driver Source Resistance	$R_{UGATEsr}$	100mA source current	--	1	--	Ω
UGATEx Driver Source Current	$I_{UGATEsr}$	V_{UGATE} – V_{PHASE} = 2.5V	--	2	--	A
UGATEx Driver Sink Resistance	$R_{UGATEsk}$	100mA sink current	--	1	--	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UGATEx Driver Sink Current	$I_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
LGATEx Driver Source Resistance	$R_{LGATEsr}$	100mA source current	--	1	--	Ω
LGATEx Driver Source Current	$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	2	--	A
LGATEx Driver Sink Resistance	$R_{LGATEsk}$	100mA sink current	--	0.5	--	Ω
LGATEx Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	4	--	A
SVI2 Bus						
SVC Frequency	f_{SVC}	(Note 5)	0.1	--	30	MHz

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Min. SVC frequency defined in electrical spec. is related with different application. As min. SVC < 1MHz, VR can't support telemetry reporting function. As min. SVC < 400kHz, VR can't support telemetry reporting function and VOTF complete function.

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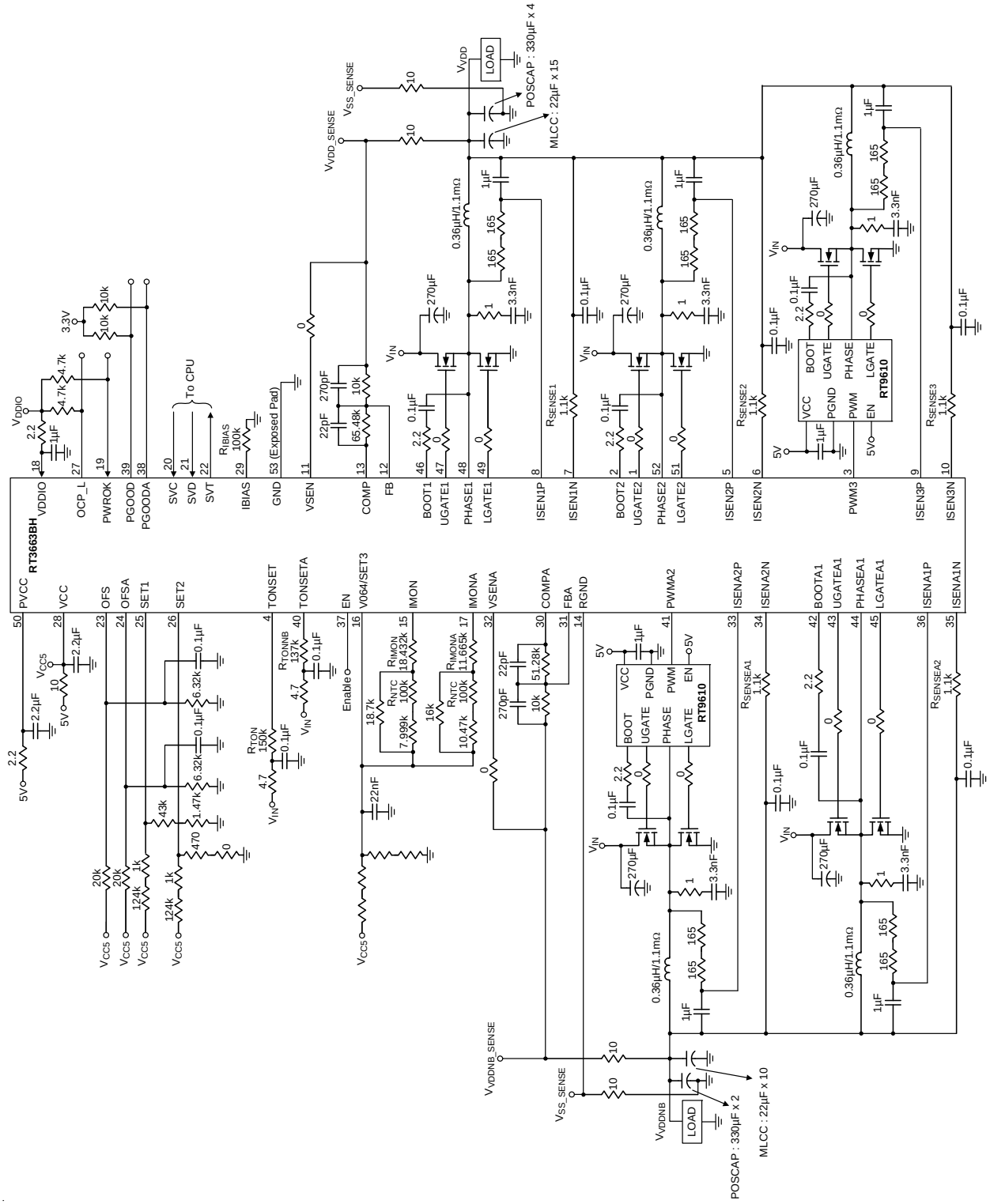
Typical Application Circuit



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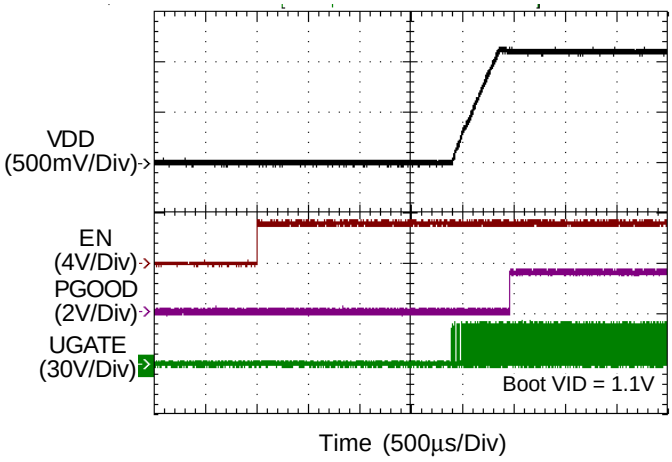
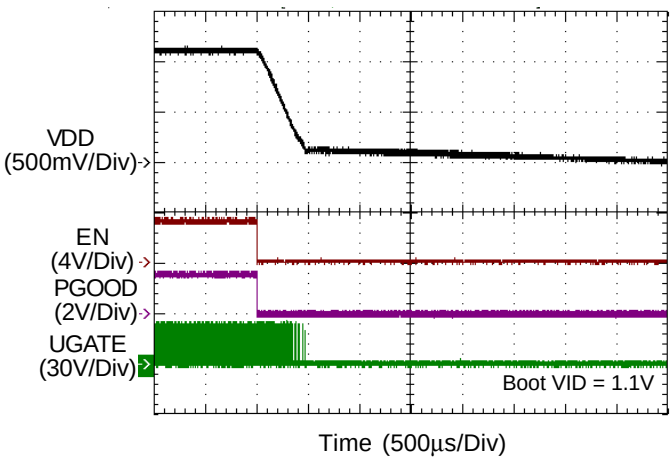
Typical Operating Characteristics

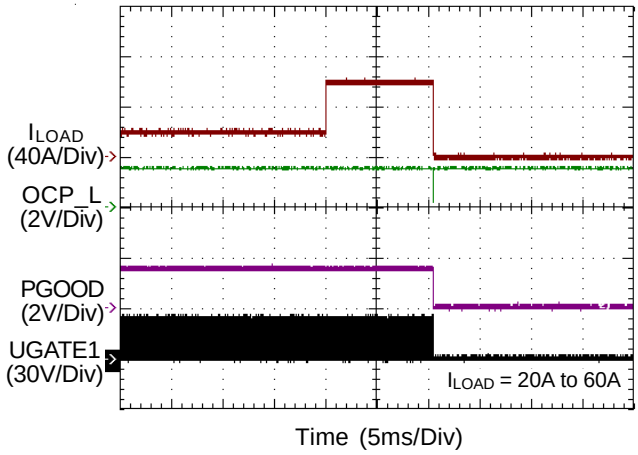
CORE VR Power On from EN



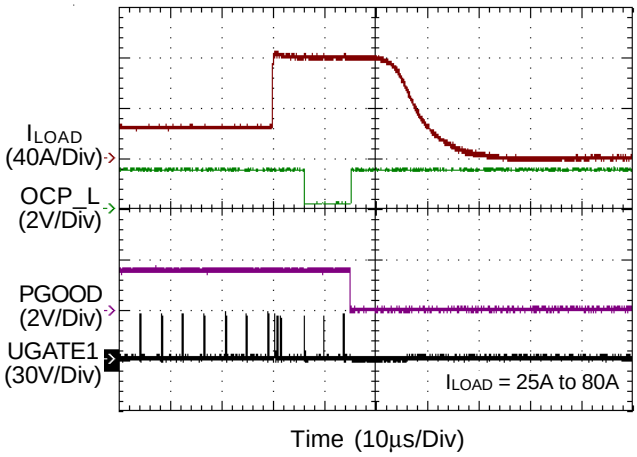
CORE VR Power Off from EN



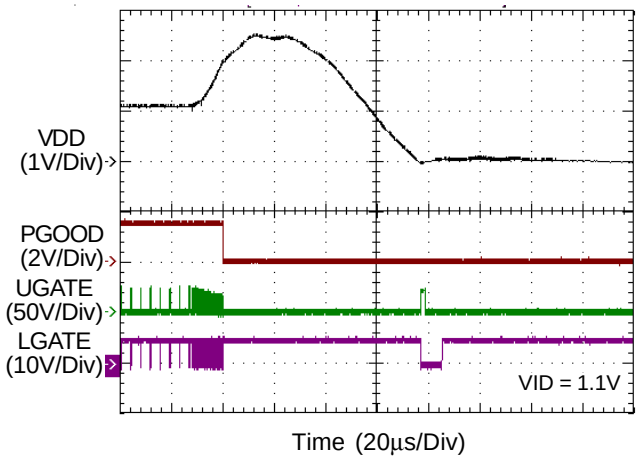
CORE VR OCP_TDC



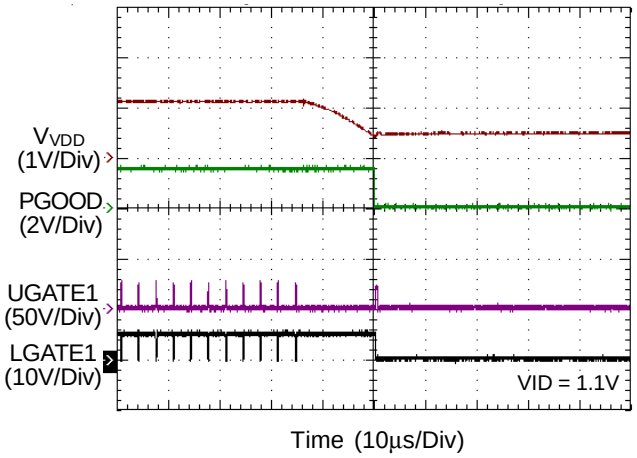
CORE VR OCP_SPIKE



CORE VR OVP and NVP



CORE VR UVP



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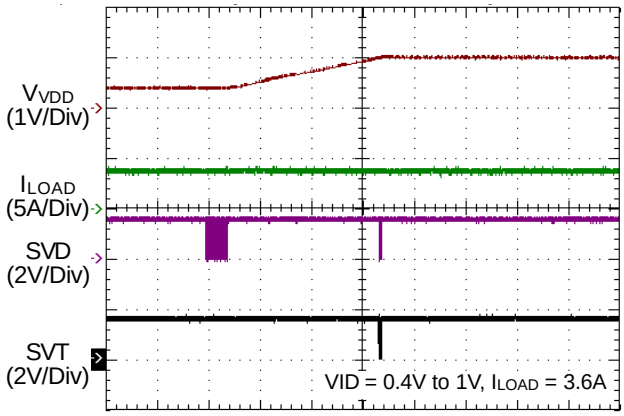
CORE VR Dynamic VID Up



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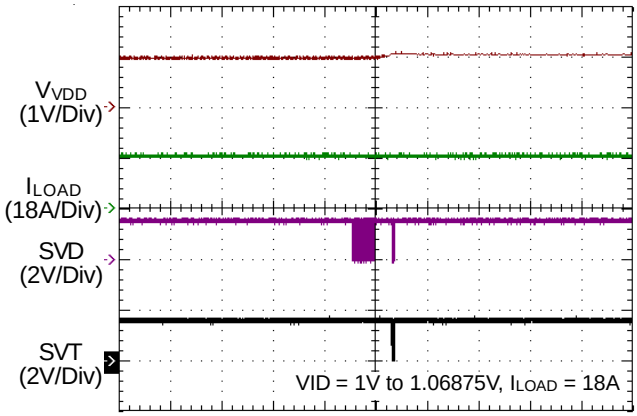

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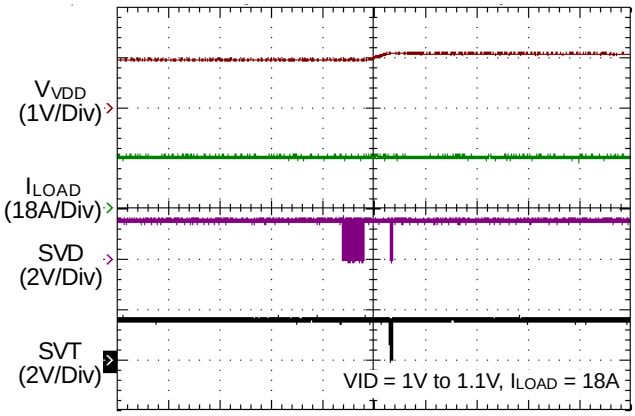

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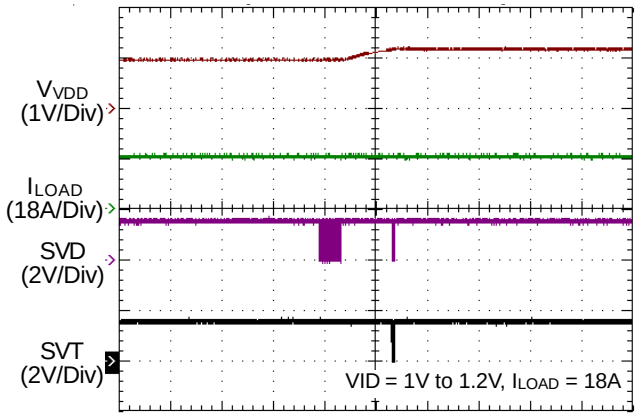
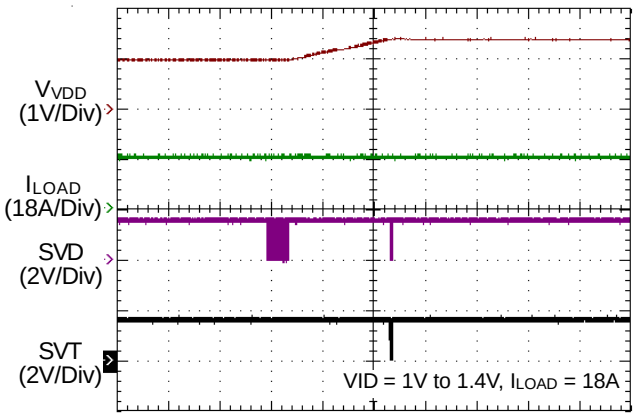
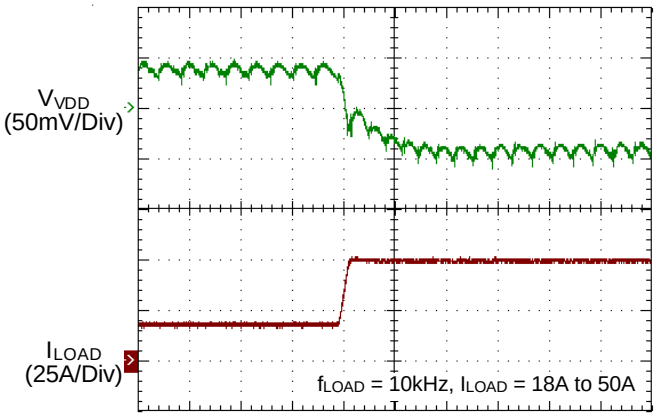


CORE VR Dynamic VID Up



CORE VR Load Transient



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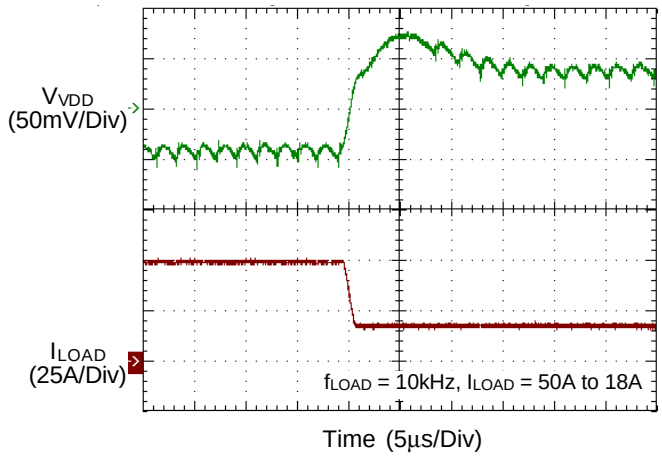
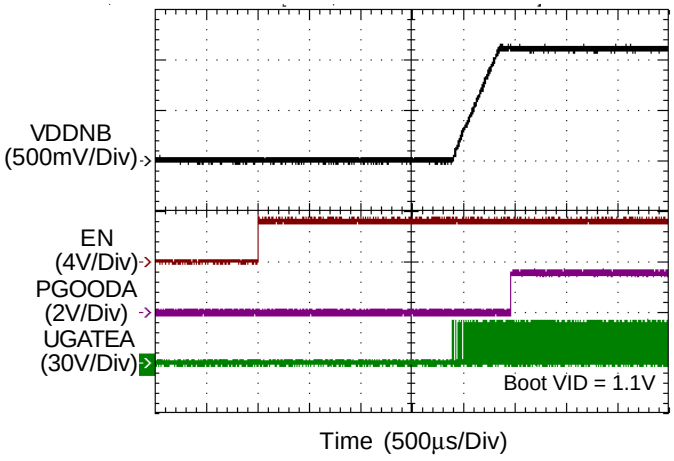
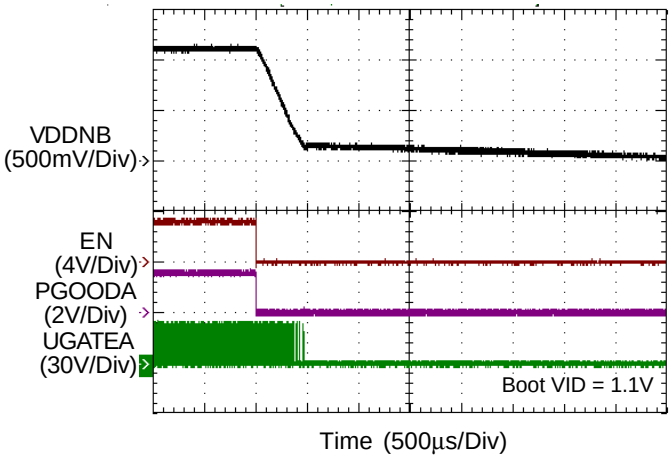
CORE VR Load Transient



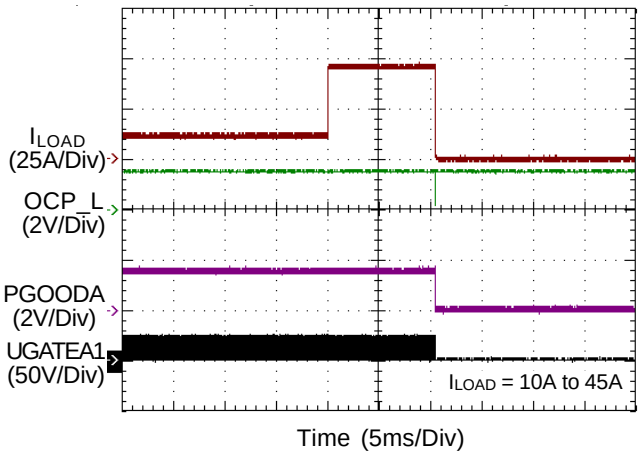
NB VR Power On from EN



NB VR Power Off from EN



NB VR OCP_TDC



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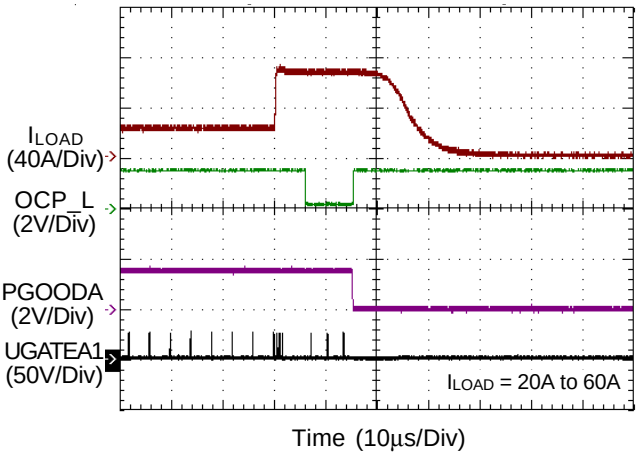
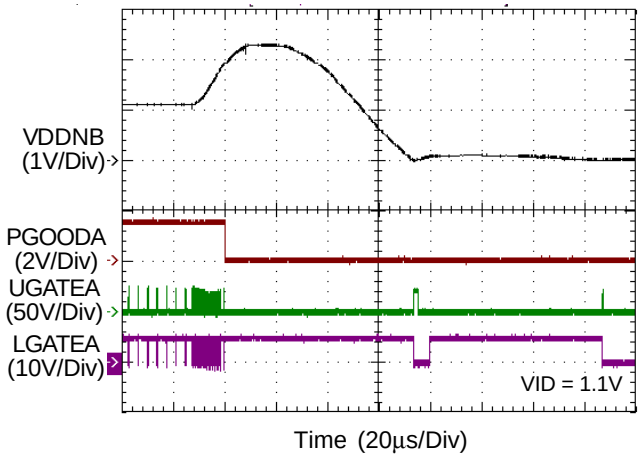


NB VR OVP and NVP



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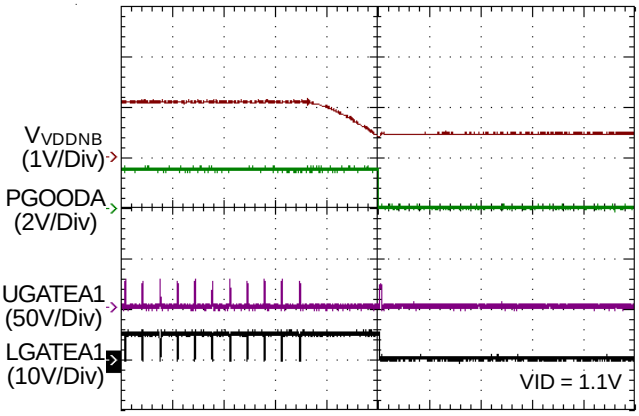
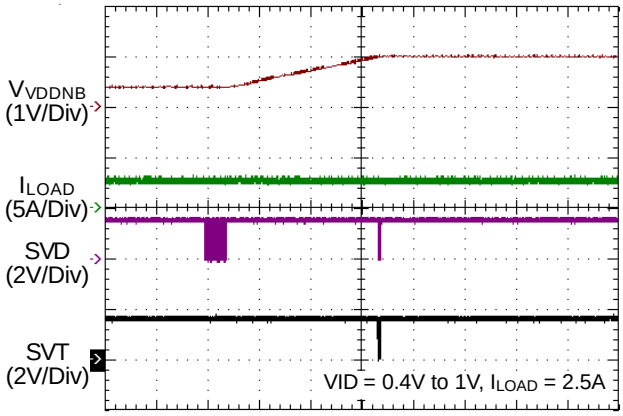
NB VR UVP



NB VR Dynamic VID Up



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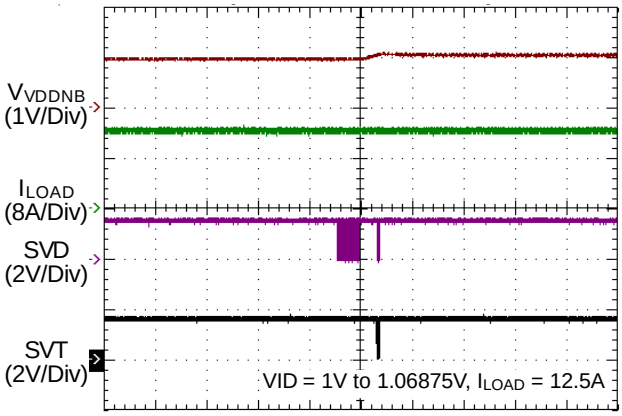

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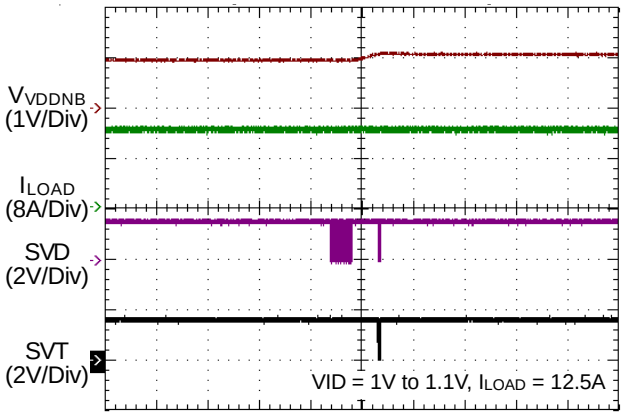

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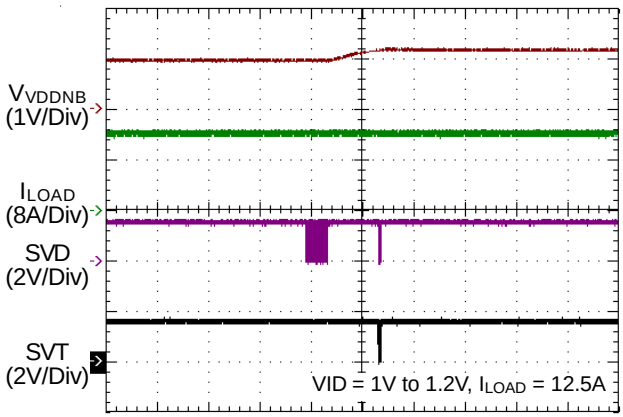

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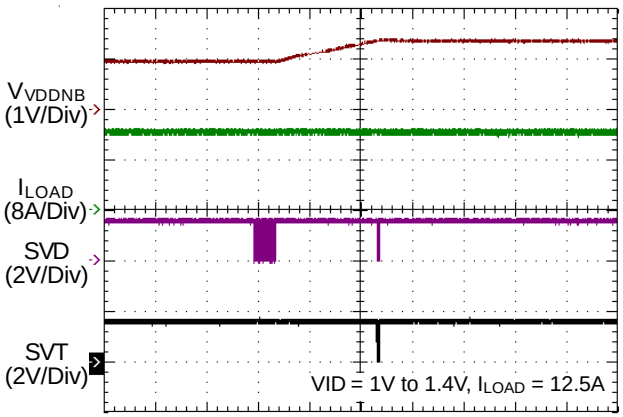

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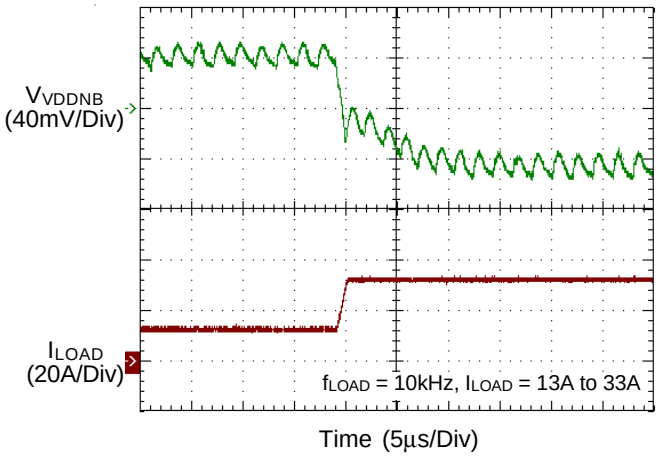
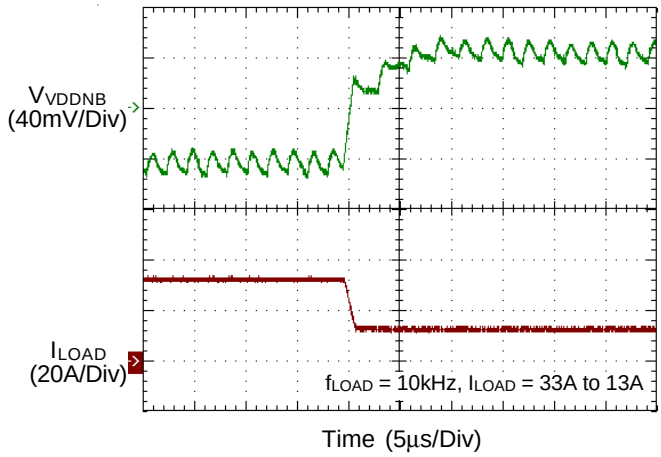
NB VR Load Transient



NB VR Load Transient



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Application Information

Power Ready (POR) Detection

During start-up, the RT3663BH detects the voltage at the voltage input pins : VCC, PVCC and EN. When VCC > 4.2V and PVCC > 3.85V, the IC recognizes the power state of system to be ready (POR = high) and wait for enable command at the EN pin. After POR = high and V_{EN} > 2V, the IC enters start-up sequence for both VDD rail and VDDNB rail. If the voltage at the pins of VCC and EN drop below low threshold, the IC enters power down sequence and all the functions are disabled. Normally, connecting system power to the EN pin is recommended. The SVID is ready in 2ms (max) after the chip has been enabled. All the protection latches (OVP, OCP, UVP) are cleared only after POR = low. The condition of V_{EN} = low does not clear these latches.

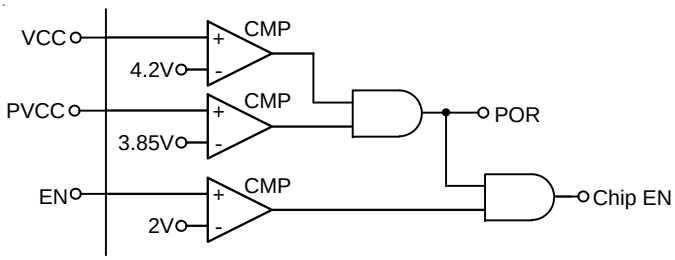

Figure 1. Power Ready (POR) Detection

Precise Reference Current Generation

The RT3663BH includes complicated analog circuits inside the controller. The IC needs very precise reference voltage/ current to drive these analog circuits. The IC generates a 2V voltage source at the IBIAS pin, and a 100kΩ resistor is required to be connected between IBIAS and analog ground, as shown in Figure 2. Through this connection, the IC generates a 20μA current from the IBIAS pin to analog ground, and this 20μA current is mirrored for internal use. Note that other type of connection or other values of resistance applied at the IBIAS pin may cause functional failure, such as slew rate control, OFS accuracy, etc. In other words, the IBIAS pin can only be connected with a 100kΩ resistor to GND. The resistance tolerance of this resistor is recommended to be 1% or lower.

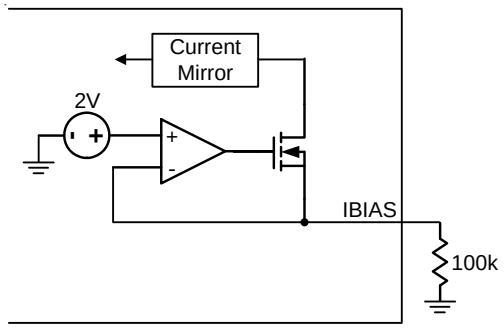

Figure 2. IBIAS Setting

Boot VID

When EN goes high, both VDD and VDDNB output begin to soft-start to the boot VID in CCM. Table 8 shows the Boot VID setting. The Boot VID is determined by the SVC and SVD input states at EN rising edge and it is stored in the internal register. The digital soft-start circuit ramps up the reference voltage at a controlled slew rate to reduce inrush current during start-up. When all the output voltages are above power good threshold (300mV below Boot VID) at the end of soft-start, the controller asserts power good after a time delay.

Table 8. 2-Bit Boot VID Code

Initial Startup VID (Boot VID)		
SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Start-Up Sequence

After EN goes high, the RT3663BH starts up and operates according to the initial settings. Figure 3 shows the simplified sequence timing diagram. The detailed operation is described in the following.

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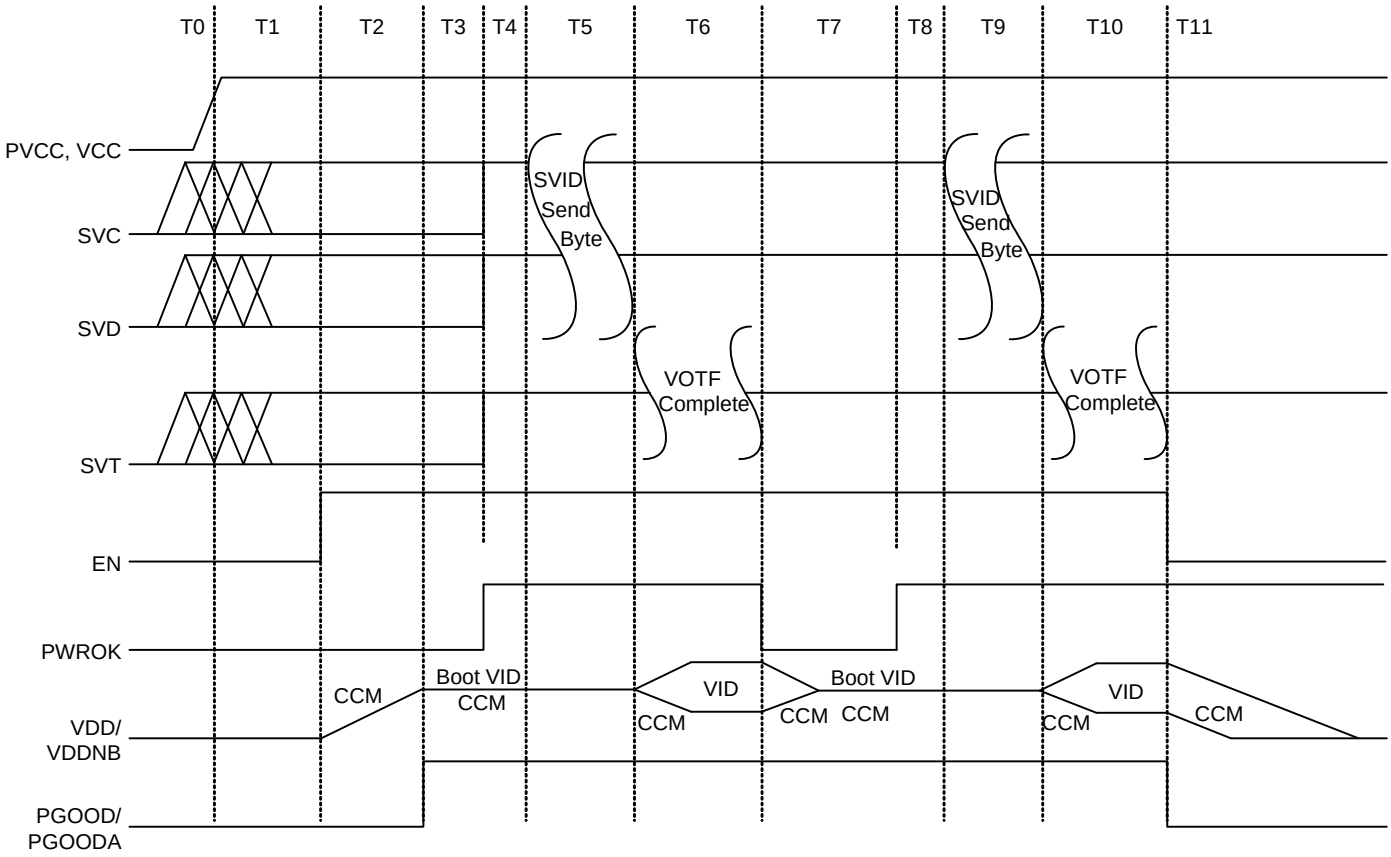

Figure 3. Simplified Sequence Timing Diagram

Description of Figure 3 :

T0 : The RT3663BH waits for VCC and PVCC POR.

T1 : The SVC pin and SVD pin set the Boot VID. Boot VID is latched at EN rising edge. SVT is driven high by the RT3663BH.

T2 : The enable signal goes high and all output voltages ramp up to the Boot VID in CCM. The soft-start slew rate is 3mV/μs.

T3 : All output voltages are within the regulation limits and the PGOOD and PGOODA signal goes high.

T4 : The PWROK pin goes high and the SVI2 interface starts running. The RT3663BH waits for SVID command from processor.

T5 : A valid SVID command transaction occurs between the processor and the RT3663BH.

T6 : The RT3663BH starts VOTF (VID on-the-Fly) transition according to the received SVID command and send a VOTF Complete if the VID reaches target VID.

T7 : The PWROK pin goes low and the SVI2 interface stops running. All output voltages go back to the boot VID in CCM.

T8 : The PWROK pin goes high again and the SVI2 interface starts running. The RT3663BH waits for SVID command from processor.

T9 : A valid SVID command transaction occurs between the processor and the RT3663BH.

T10 : The RT3663BH starts VID on-the-Fly transition according to the received SVID command and send a VOTF Complete if the VID reaches target VID.

T11 : The enable signal goes low and all output voltages enter soft-shutdown mode.

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Power-Down Sequence

If the voltage at the EN pin falls below the enable falling threshold, the controller is disabled. The voltage at the PGOOD and PGOODA pins immediately go low at the loss of enable signal at the EN pin and the controller executes soft-shutdown operation. The internal digital circuit ramps down the reference voltage at the same slew rate as that of in soft-start, making VDD and VDDNB output voltages gradually decrease in CCM. Each of the controller channels stops switching when the voltage at the voltage sense pin V_{SEN}/V_{SENA}, cross about 0.2V. The Boot VID information stored in the internal register is cleared at IC POR. This event forces the RT3663BH to check the SVC and SVD inputs for a new boot VID when the EN voltage goes high again.

PGOOD and PGOODA

The PGOOD and PGOODA are open-drain logic outputs. The two pins provide the power good signal when VDD and VDDNB output voltage are within the regulation limits and no protection is triggered. These pins are typically tied to 3.3V or 5V power source through a pull-high resistor. During shutdown state (EN = low) and the soft-start period, the PGOOD and PGOODA voltages are pulled low. After a successful soft-start and VDD and VDDNB output voltages are within the regulation limits, the PGOOD and PGOODA are released high individually.

The voltages at the PGOOD and PGOODA pins are pulled low individually during normal operation when any of the following events occurs : over-voltage protection, under-voltage protection, over-current protection, and logic low EN voltage. If one rail triggers protection, another rail's PGOOD is pulled low after 5μs delay.

SVI2 Wire Protocol

The RT3663BH complies with AMD's Voltage Regulator Specification, which defines the Serial VID Interface 2 (SVI2) protocol. With SVI2 protocol, the processor directly controls the reference voltage level of each individual controller channel and determines which controller operates in power saving mode. The SVI2 interface is a three-wire bus that connects a single master to one or more slaves. The master initiates and terminates SVI2 transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave drives the telemetry, SVT during a transaction. The AMD processor is always the master. The voltage regulator controller (RT3663BH) is always the slave. The RT3663BH receives the SVID code and acts accordingly. The SVI protocol supports 20MHz high speed mode I^2C, which is based on SVD data packet. Table 9 shows the SVD data packet. A SVD packet consists of a "Start" signal, three data bytes after each byte, and a "Stop" signal. The 8-bit serial VID codes are listed in Table1. After the RT3663BH has received the stop sequence, it decodes the received serial VID code and executes the command. The controller has the ability to sample and report voltage and current for the VDD and VDDNB domains. The controller reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. A bit TFN at SVD packet along with the VDD and VDDNB domain selector bits are used by the processor to change the telemetry functionality. The telemetry bit definition is listed in Figure 4. The detailed SVI2 specification is outlined in the AMD Voltage Regulator and Voltage Regulator Module (VRM) and Serial VID Interface 2.0 (SVI2) Specification.

Table 9. SVD Data Packet

Bit Time	Description
1 : 5	Always 11000b
6	VDD domain selector bit, if set then the following two data bytes contain the VID for VDD, the PSI state for VDD, and the load-line slope trim and offset trim state for VDD.
7	VDDNB domain selector bit, if set then the following two data bytes contain the VID for VDDNB, the PSI state for VDDNB, and the load-line slope trim and offset trim state for VDDNB.
8	Always 0b
10	PSI0_L
11 : 17	VID Code bits [7:1]
19	VID Code bit [0]

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Bit Time	Description
20	PSI1_L
21	TFN (Telemetry Functionality)
22 : 24	Load Line Slope Trim [2:0]
25 : 26	Offset Trim [1:0]

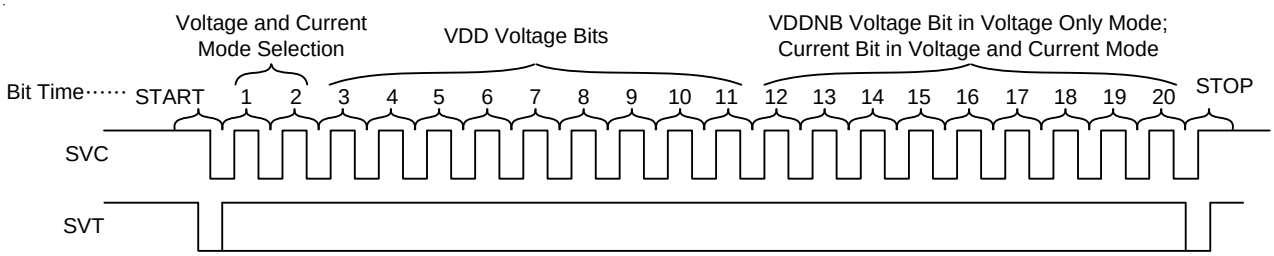

Figure 4. Telemetry Bit Definition

PWROK and SVI2 Operation

The PWROK pin is an input pin, which is connected to the global power good signal from the platform. Logic high at this pin enables the SVI2 interface, allowing data transaction between processor and the RT3663BH. Once the RT3663BH receives a valid SVID code, it decodes the information from processor to determine which output plane is going to move to the target VID. The internal DAC then steps the reference voltage in a controlled slew rate, making the output voltage shift to the required new VID. Depending on the SVID code, more than one controller channel can be targeted simultaneously in the VID transition. For example, VDD and VDDNB voltages can ramp up/down at the same time.

If the PWROK input goes low during normal operation, the SVI2 protocol stops running. The RT3663BH immediately drives SVT high and modifies all output voltages back to the boot VID, which is stored in the internal register right after the controller is enabled. The controller does not read SVD and SVC inputs after the loss of PWROK. If the PWROK input goes high again, the SVI2 protocol resumes running. The RT3663BH then waits to decode the SVID command from processor for a new VID and acts as previously described. The SVI2 protocol is only runs when the PWROK input goes high after the voltage at the EN pin goes high; otherwise, the RT3663BH does not soft-start due to incorrect signal sequence.

VID On-the-Fly Transition

After the RT3663BH has received a valid SVID code, it executes the VID on-the-Fly transition by stepping up/down the reference voltage of the required controller channel in a controlled slew rate, hence allowing the output voltage to ramp up/down to target VID.

During the VID on-the-Fly transition, the RT3663BH forces CCM operation in high performance mode. If the controller channel operates in the power-saving mode prior to the VID on-the-Fly transition, it changes to high performance mode and implement CCM operation when the controller implement VID up, and then remain in high performance mode; if the controller implement VID down in CCM, it slew rate is about 2.5mV/μs; if the controller implement VID down in power-saving mode, it decays down and keep in power-saving mode. The controller receives DACOFF in PSI=00 will change to PSI=11 multi-phase CCM down. The slew rate is 2.5mV/μs, when DACOFF finishes, controller enters power saving mode;control loop is shut down, only basic bias, sequence control and interface circuits are still active to achieve power saving.

However DACOFF by PSI=11 CCM down, VR can enter power saving mode earlier than PSI=00 decay down.

The voltage at the PGOOD pin keeps high during the VID on-the-Fly transition. The RT3663BH sends VOTF complete only at the end of VID up transition. In the event of receiving a VID off code, the RT3663BH steps the reference voltage of required controller channel down to zero, hence making the required output voltage decrease

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to zero, and the voltage at the PGOOD pin remains high since the VID code is valid.

Power State Transition

The RT3663BH supports power state transition function in VDD and VDDNB VR for the PSI[x]_L and command from AMD processor. The PSI[x]_L bit in the SVI2 protocol controls the operating mode of the RT3663BH controller channels. The default operation mode of VDD and VDDNB VR is CCM.

When the VDD VR is in N phase configuration and receives PSI0_L = 0 and PSI1_L = 1, the VDD VR enters single-phase diode emulation mode. When the VDD VR receives PSI0_L = 0 and PSI1_L = 0, the VDD VR remains in the single-phase diode emulation mode. In reverse, the VDD VR goes back to N phase operation in CCM upon receiving PSI0_L = 1 and PSI1_L = 0 or 1, see Table 10. When the VDDNB VR receives PSI0_L = 0 and PSI1_L = 1, it enters single-phase diode emulation mode, when the VDDNB VR receives PSI0_L = 0 and PSI1_L = 0, it remains in the single-phase diode emulation mode. The VDDNB VR goes back to full-phase CCM operation after receiving PSI0_L = 1 and PSI1_L = 0 or 1, see Table 11.

Table 10. VDD VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
3	11 or 10	3 phase CCM
	01	1 phase DEM
	00	1 phase DEM
2	11 or 10	2 phase CCM
	01	1 phase DEM
	00	1 phase DEM
1	11 or 10	1 phase CCM
	01	1 phase DEM
	00	1 phase DEM

Table 11. VDDNB VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
2	11 or 10	2 phase CCM
	01	1 phase DEM
	00	1 phase DEM
1	11 or 10	1 phase CCM
	01	1 phase DEM
	00	1 phase DEM

Differential Remote Sense Setting

The VDD and VDDNB controllers have differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, processor internal power routes and socket contacts. The processor contains on-die sense pins, VDD_SENSE, VDDNB_SENSE and VSS_SENSE. Connect RGND to VSS_SENSE. For VDD controller, connect FB to VDD_SENSE with a resistor to build the negative input path of the error amplifier. Connect FBA to VDDNB_SENSE with a resistor using the same way in VDD controller. Connect VSS_SENSE to RGND using separate trace as shown in Figure 5. The precision reference voltages refer to RGND for accurate remote sensing.

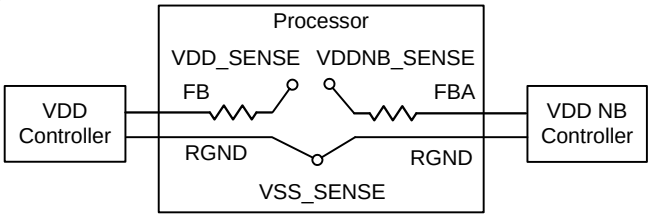

Figure 5. Differential Remote Voltage Sense Connection

SET1 and SET2 Pin Setting

The RT3663BH provides the SET1 pin for platform users to set the VDD and VDDNB controller OCP_TDC threshold, DVIDx compensation bit1 and internal ramp amplitude (RSET & RSETA), and the SET2 pin to set VDD and VDDNB controller OCP trigger delay (OCPTRGDELAY), DVIDx compensation bit0, external offset function and quick response threshold (QRTH & QRTHA). To set these pins, platform designers should use resistive voltage divider on these pins, refer to Figure 6 and Figure 7. The voltages at the the SET1 and SET2 pins are :

$$V_{SET1} = VCC \times \frac{R_{SET1,D}}{R_{SET1,U} + R_{SET1,D}} \quad (1)$$

$$V_{SET2} = VCC \times \frac{R_{SET2,D}}{R_{SET2,U} + R_{SET2,D}} \quad (2)$$

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The ADC monitors and decodes the voltage at this pin only once after power up. After ADC decoding (only once), a 40μA current (when VCC = 5V) is generated at the SET1 and SET2 pin for internal use. That is the voltage at SET1 and SET2 pin is

$$\Delta V_{SET1} = 40\mu A \times \frac{R_{SET1,U} \times R_{SET1,D}}{R_{SET1,U} + R_{SET1,D}} \quad (3)$$

$$\Delta V_{SET2} = 40\mu A \times \frac{R_{SET2,U} \times R_{SET2,D}}{R_{SET2,U} + R_{SET2,D}} \quad (4)$$

From equation (1) to equation (4) and Table 2 to Table 5, platform users can set the above described pin setting functions.

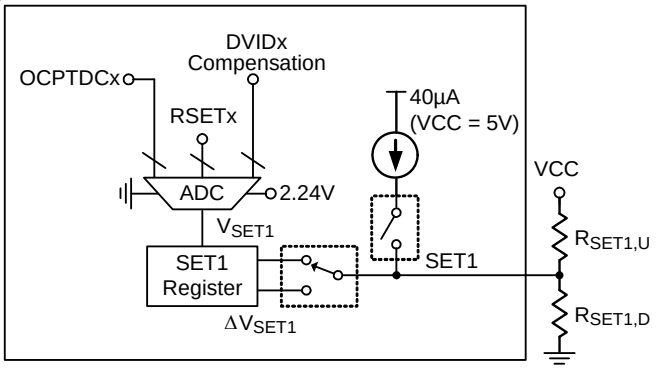

Figure 6. SET1 Pin Setting

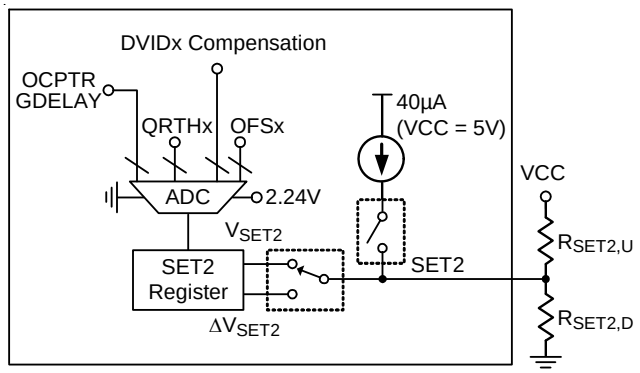

Figure 7. SET2 Pin Setting

V064/SET3 Pin Setting

The V064/SET3 pin provides two functions: fixed 0.64V reference voltage output during normal operation of VR controller and programmable current gain ratio for VDD and VDDNB controllers. Figure 8 (a) shows VDD and VDDNB current gain ratio setting with the V064/SET3 pin voltage V_{SET3}. User can set the application of zero loadline through the pin setting. When the EN pin goes high, the controller senses the voltage V_{SET3} represented as follows and sets VDD and VDDNB current gain ratio.

$$V_{SET3} = VCC \times \frac{R_{SET3,D}}{R_{SET3,U} + R_{SET3,D}}$$

After pin setting is finished, V064/SET3 pin is regulated at 0.64V as shown in Figure 8 (b).

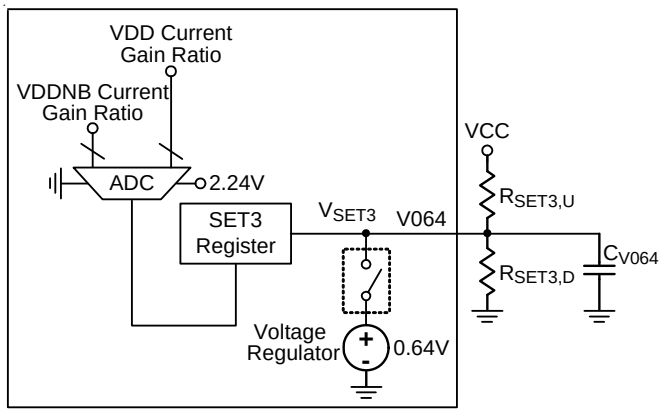

Figure 8 (a). V064/SET3 Pin Setting

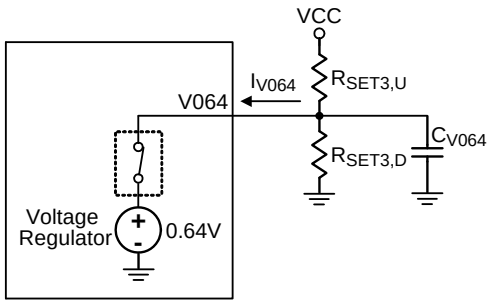

Figure 8 (b). Illustration of 0.64V Regulation at V064/SET3 Pin

In the application circuit as shown in Figure 9, the C_{V064} is used to stabilize the internal voltage regulator at V064/SET3 pin, and also related to the pin setting settling time. Therefore, the recommended capacitance is 22nF.

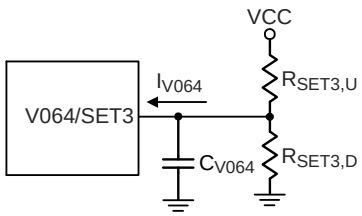

Figure 9. Illustration of Capacitor C_{V064} at V064/SET3 Pin

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The accuracy and settling time of the voltage at V064/SET3 pin should be considered when the EN pin goes high. So, the equivalent RC settling time at this pin should be smaller than 1ms. Therefore, the following equations can derive the $R_{SET3,D}$ and $R_{SET3,U}$.

$$4 \times R_{SET3,EQU} \times C_{V064} \leq 1ms$$

$$R_{SET3,EQU} = \frac{R_{SET3,U} \times R_{SET3,D}}{R_{SET3,U} + R_{SET3,D}}$$

$$R_{SET3,U} = \left| \frac{V_{CC}}{I_{V064}} \times \left(1 - \frac{0.64}{V_{SET3}} \right) \right|$$

$$R_{SET3,D} = R_{SET3,U} \times \frac{V_{SET3}}{V_{CC} - V_{SET3}}$$

VDD Controller

Active Phase Determination

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during start-up. Normally, the VDD controller operates as a 3-phase PWM controller. Pulling ISEN3N to VCC programs a 2-phase operation, and pulling ISEN2N to VCC programs a 1-phase operation. At EN rising edge, VDD controller detects whether the voltages of ISEN2N and ISEN3N are higher than "VCC – 0.5V" respectively to decide how many phases should be active. Phase selection is only active during IC POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

Loop Control

The VDD controller adopts Richtek's proprietary G-NAVP™ topology. The G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{VDD} will decrease with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 10.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMP voltage also increases and induces $V_{OUT,VDD}$ to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

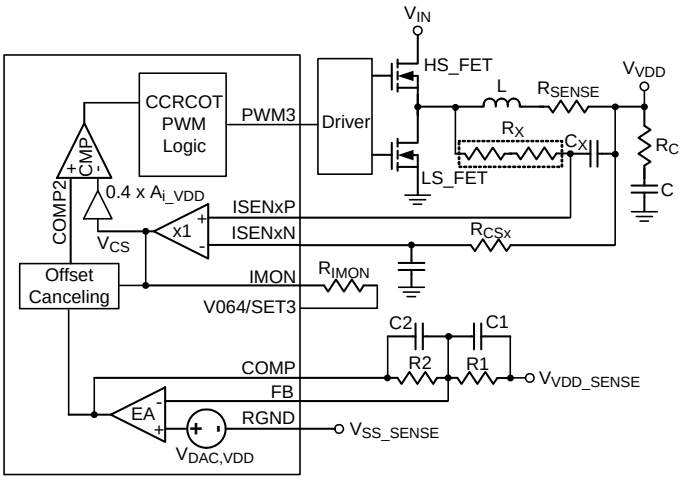

Figure 10. VDD Controller : Simplified Schematic for Droop and Remote Sense in CCM

Droop Setting

It is very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics as shown in Figure 11. This target is to have

$$V_{VDD} = V_{DAC,\,VDD} - I_{LOAD} \times R_{DROOP} \quad (5)$$

Then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 10 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}} \quad (6)$$

$$G_I = \frac{R_{SENSE}}{R_{CSx}} \times R_{IMON} \times \frac{4}{10} \times A_{i_VDD} \quad (7)$$

where G_I is the internal current sense amplifier gain and A_{i_VDD} is the VDD current gain ratio. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the equivalent resistance of the inductor. R_{DROOP} is the equivalent load-line resistance as well as the desired static output impedance.

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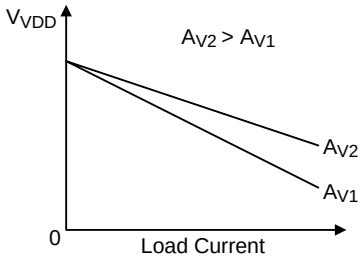

Figure 11. VDD Controller : Error Amplifier gain (A_V) Influence on V_{VDD} Accuracy

Loop Compensation

Optimized compensation of the VDD controller allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 12 shows the compensation circuit. Previous design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2\pi \times C \times R_C} \quad (8)$$

Where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (9)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad (10)$$

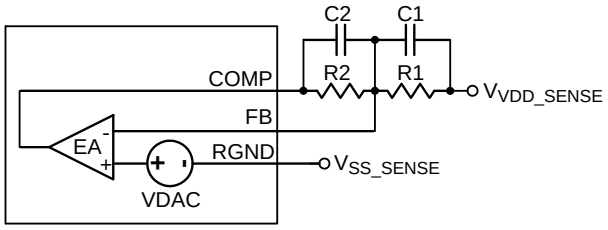

Figure 12. VDD Controller : Compensation Circuit

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 13 shows the On-Time setting circuit. Connect a resistor (R_{TON}) between V_{IN} and TONSET to set the on-time of UGATE :

$$t_{ON}\ (0.5V \le V_{DAC} < 1.8V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC}} \quad (11)$$

Where t_{ON} is the UGATE turn-on period, V_{IN} is the input voltage of the VDD controller, and V_{DAC} is the DAC voltage.

When V_{DAC} is larger than 1.8V, the equivalent switching frequency may be over 500kHz, and this too fast switching frequency is unacceptable. Therefore, the VDD controller implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When V_{DAC} is larger than 1.8V, the on-time equation is modified to :

$$t_{ON}\ (V_{DAC} \ge 1.8V) = \frac{13.55 \times 10^{-12} \times R_{TON} \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (12)$$

On-time translates only roughly to switching frequencies.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} = \frac{V_{DAC(MAX)} + I_{LOAD(MAX)} \times (DCR_L + R_{ON_LS\text{-}FET} - R_{DROOP})}{\left[V_{IN(MAX)} + I_{LOAD(MAX)} \times (R_{ON_LS\text{-}FET} - R_{ON_HS\text{-}FET})\right] \times (T_{ON} - T_D + T_{ON,VAR}) + I_{LOAD(MAX)} \times (R_{ON_LS\text{-}FET}) \times T_D} \quad (13)$$

Where $f_{S(MAX)}$ is the maximum switching frequency, T_D is the driver dead time, $T_{ON,VAR}$ is the TON variation value. $V_{DAC(MAX)}$ is the maximum V_{DAC} of application, $V_{IN(MAX)}$ is the maximum application input voltage, $I_{LOAD(MAX)}$ is the maximum load of application, $R_{ON_LS\text{-}FET}$ is the on-resistance of low side FET $R_{DS(ON)}$, $R_{ON_HS\text{-}FET}$ is the on-resistance of high side FET $R_{DS(ON)}$, DCR_L is the equivalent resistance of the inductor, and R_{DROOP} is the load-line setting.

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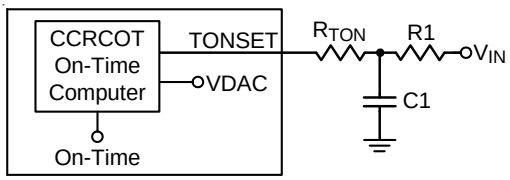

Figure 13. VDD Controller : On-Time Setting with RC Filter

Current Sense Setting

The current sense topology of the VDD controller is continuous inductor current sensing. Therefore, the controller is less sensitive to noise. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENxP and ISENxN pins denote the positive and negative input of the current sense amplifier of each phase.

Users can either use a current sense resistor or the inductor's DCR_L for current sensing. Using the inductor's DCR_L allows higher efficiency as shown in Figure 14.

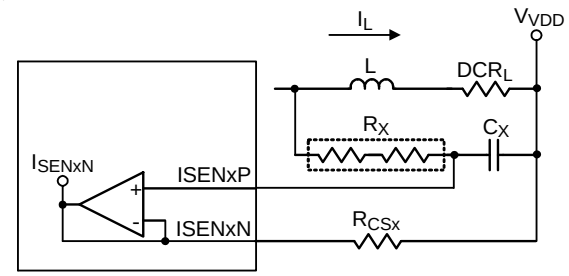

Figure 14. VDD Controller : Lossless Inductor Sensing

In order to optimize transient performance, R_X and C_X must be set according to the equation below :

$$\frac{L}{DCR_L} = R_X \times C_X \quad (14)$$

Then the proportion between the phase current, I_L, and the sensed current, I_{SENxN}, is driven by the value of the effective sense resistance, R_{CSx}, and the DCR_L of the inductor. The resistance value of R_{CSx} is limited by the internal circuitry. The recommended value is from 500Ω to 1.2kΩ.

$$I_{SENxN} = I_L \times \frac{DCR_L}{R_{CSx}} \quad (15)$$

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load-line requirement and the response time is too fast causing a ring back, the value of resistance should be increased. Vice versa, with a high resistance, the output voltage transient has only a small initial dip with a slow response time. R_X is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. C_X is suggested X7R type for the application.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor equivalent resistance sensing method.

Per-Phase Over Current Protection

The VDD controller provides over current protection in each phase. For VDD controller in three-phase configuration, either phase can trigger Per-Phase Over Current Protection (PHOCP).

The VDD controller senses each phase inductor current I_L, and PHOCP comparator compares sensed current with PHOCP threshold current, as shown in Figure 15.

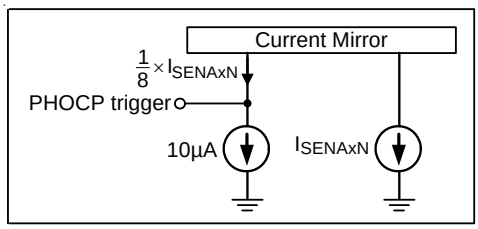

Figure 15. VDD Controller : Per-Phase OCP Setting

The resistor R_{CSx} determines PHOCP threshold.

$$I_{L,PERPHASE(MAX)} \times \frac{DCR_L}{R_{CSx}} \times \frac{1}{8} = 10\mu A \quad (16)$$

$$R_{CSx} = \frac{I_{L,PERPHASE(MAX)} \times DCR_L}{8 \times 10\mu A} \quad (17)$$

The controller turns off all high-side/low-side MOSFETs to protect CPU if the per-phase over current protection is triggered.

Current Balance

The VDD controller implements internal current balance mechanism in the current loop. The VDD controller senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase is adjusted to be shorter.

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Initial Offset and External Offset (Over Clocking Offset Function)

The VDD controller features over clocking offset function which provides the possibility of wide range offset of output voltage. Two kinds of offset settings are available, initial and external. To enable/disable these offset functions depends on the SET2 pin setting (refer Table 5 and Table 12).

While OFSENABLE and OFSAENABLE are "0", initial offset function is enabled and external offset function is disabled. Initial offset function is implemented through OFS/OFSA pin. Initial offset function is decided by the following descriptions :

(1) If the voltage of OFS/OFSA < 0.3V at EN rising edge then initial offset voltage is considered as 0V.

(2) If the voltage of OFS/OFSA > 0.3V at EN rising edge then initial offset voltage is enabled.

$V_{Initial_OFS} = V_{OFS/OFSA} - 1.2V$ (18-a)

Core rail initial offset is set by OFS pin voltage, and NB rail initial offset is set by OFSA pin voltage.

(3) $V_{VDD} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{Initial_OFS}$ (18-b)

While OFSENABLE and OFSAENABLE are "1", initial offset function is disabled and external offset function is enabled. External offset function is also implemented through OFS/OFSA pin. External offset function is decided by the following descriptions :

(1) $V_{External_OFS} = V_{OFS/OFSA} - 1.2V$ (18-c)

Core rail external offset is set by OFS pin voltage, and NB rail external offset is set by OFSA pin voltage.

(2) $V_{VDD} = V_{DAC} - I_{LOAD} \times R_{DROOP} + V_{External_OFS}$ (18-d)

To add a filter capacitor between OFS/OFSA and GND is recommended.

Table 12. Initial/External Offset Function Setting for VDD and VDDNB Controller

OFSENABLE	OFSAENABLE	Description
0	0	Enable Initial offset, disable external offset
1	1	Enable external offset, disable initial offset

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The RT3663BH holds the inductor current to hold the load-line during a dynamic VID event. The VDD controller always enter three-phase configuration when VDD controller receives dynamic VID up and VDD controller holds the operating state when VDD controller receives dynamic VID down.

The RT3663BH also has DVID compensation which can boost up the Dynamic VID slew rate and adjust the voltage on-the-fly complete timing. The DVID compensation parameter can be selected by DVIDx compensation bits using the SET1 and SET2 pins.

When the VID CCM down on light loading condition, the negative inductor current will be produced, and it may cause the audio noise and phase ringing effect. For improving the problems, the controller turns off the low side MOSFET to prevent the negative current when VID down, and return to normal CCM down operation after 4 PWM pulses.

Ramp Amplitude Adjust

When the VDD controller takes phase shedding operation and enters diode emulation mode, the internal ramp of VDD controller is modified for the reason of stability. In case of smooth transition into DEM, the CCM ramp amplitude should be designed properly. The RT3663BH provides the SET1 pin for platform users to set the ramp amplitude of the VDD controller in CCM.

Current Monitoring and Current Reporting

The VDD controller provides current monitoring function via inductor current sensing. In the G-NAVP™ technology, the output voltage is dependent on output current, and the current monitoring function is achieved by this characteristic of output voltage. The equivalent output current is sensed from inductor current sensing and mirrored to the IMON pin. The resistor connected to the IMON pin determines voltage of the IMON output.

$$V_{IMON} = I_{L,SUM} \times \frac{DCR_L}{R_{CSx}} \times R_{IMON} + 0.64 \quad (20)$$

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Where I_L is the phase current, R_{CSx} is the effective sense resistance, and R_{IMON} is the current monitor current setting resistor. Note that the IMON pin cannot be monitored.

The ADC circuit of the VDD controller monitors the voltage variation at the IMON pin from 0V to 3.19375V, and this voltage is decoded into digital format and stored into Output_Current register. The ADC divides 3.19375V into 511 levels, so LSB = 3.19375V / 511 = 6.25mV.

Quick Response

The VDD controller utilizes a quick response feature to support heavy load current demand during instantaneous load transient. The VDD controller monitors the current of the V_{VDD_SENSE}, and this current is mirrored to internal quick response circuit. At steady state, this mirrored current does not trigger a quick response. When the V_{VDD_SENSE} voltage drops abruptly due to load apply transient, the mirrored current flowing into quick response circuit also increases instantaneously.

The QR threshold setting for VDD controller refers to Table 4.

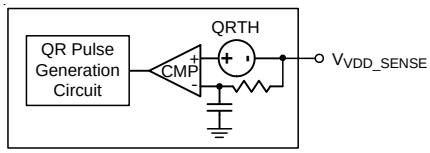

Figure 16. VDD Controller : Quick Response Triggering Circuit

When quick response is triggered, the quick response circuit generates a quick response pulse. The pulse width of quick response is almost the same as t_{ON}.

After generating a quick response pulse, the pulse is then applied to the on-time generating circuit, and all the active phases' on-time are overridden by the quick response pulse.

Over-Current Protection

The RT3663BH has dual OCP mechanism. The dual OCP mechanism has two types of thresholds. The first type, referred to as OCP-TDC, is a time and current based threshold. OCP-TDC should trip when the average output current exceeds TDC by some percentage and for a period of time. This period of time is referred to as the trigger delay. The second type, referred to as OCP-SPIKE, is a current based threshold. OCP-SPIKE should trip when the cycle-by-cycle output current exceeds IDDSPIKE by some percentage. If either mechanism trips, then the VDD controller asserts OCP_L and delays any further action. This delay is called an action delay. Refer to action delay time. After the action delay has expired and the VDD controller has allowed its current sense filter to settle out and the current has not decreased below the threshold, then the VDD controller turns off both high-side MOSFETs and low-side MOSFETs of all channels.

Users can set OCP-SPIKE threshold, $I_{L,SUM(SPIKE)}$, by the current monitor resistor R_{IMON} of the following equation :

$$I_{L,SUM\ (SPIKE)} = \frac{3.19375 - 0.64}{DCR_L} \times \frac{R_{CSx}}{R_{IMON}} \quad (21)$$

And set the OCP-TDC threshold, $I_{L(TDC)}$, by some percentage of OCP-SPIKE through Table 2.

Over-Voltage Protection (OVP)

The over-voltage protection circuit of the VDD controller monitors the output voltage via the VSEN pin after POR. When VID is lower than 0.9V, once VSEN voltage exceeds "0.9V + 325mV", OVP is triggered and latched. When VID is larger than 0.9V, once VSEN voltage exceeds the internal reference by 325mV, OVP is triggered and latched. The VDD controller tries to turn on low-side MOSFETs and turn off high-side MOSFETs of all active phases of the VDD controller to protect the CPU. When OVP is triggered by one rail, the other rail also enters soft shut down sequence. A 1μs delay is used in OVP detection circuit to prevent false trigger.

Negative-Voltage Protection (NVP)

During OVP latch state, the VDD controller also monitors the VSEN pin for negative voltage protection. Since the OVP latch continuously turns on all low-side MOSFETs of the VDD controller, the VDD controller may suffer negative output voltage. As a consequence, when the V_{SEN} voltage drops below 0V after triggering OVP, the VDD controller triggers NVP to turn off all low-side MOSFETs of the VDD controller while the high-side MOSFETs remain off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. The NVP function is active only after OVP is triggered.

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Under-Voltage Protection (UVP)

The VDD controller implements under-voltage protection of $V_{OUT,VDD}$. If VSEN voltage is less than the internal reference by 500mV, the VDD controller triggers UVP latch. The UVP latch turns off both high-side and low-side MOSFETs. When UVP is triggered by one rail, the other rail also enters soft shutdown sequence. A 3µs delay is used in UVP detection circuit to prevent false trigger.

Under-Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below IC POR threshold, the VDD controller triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers. A 3µs delay is used in UVLO detection circuit to prevent false trigger.

VDDNB Controller

VDDNB Controller Disable

The VDDNB controller can be disabled by connecting ISENA1N to a voltage higher than VCC. If not in use, ISENAxP is recommended to be connected to VCC, while PWMAx is left floating. When VDDNB controller is disabled, all SVID commands related to VDDNB controller are rejected.

Loop Control

The VDDNB controller adopts Richtek's proprietary G-NAVP™ topology. The G-NAVP™ is based on the finite gain peak current mode with CCRCOT (Constant Current Ripple Constant On-Time) topology. The output voltage, V_{VDDNB} decreases with increasing output load current. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 17.

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by CCRCOT on-time generator. When load current increases, V_{CS} increases, the steady state COMPA voltage also increases and induces V_{VDDNB} to decrease, thus achieving AVP. A near-DC offset canceling is added to the output of EA to eliminate the inherent output offset of finite gain peak current mode controller.

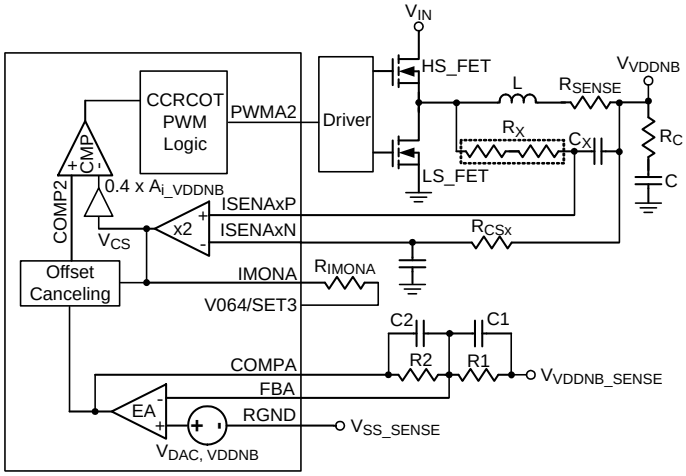

Figure 17. VDDNB Controller : Simplified Schematic for Droop and Remote Sense in CCM

Droop Setting

It is very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics as shown in Figure 18. This target is to have

$$V_{VDDNB} = V_{DAC,VDDNB} - I_{LOAD} \times R_{DROOP} \quad (22)$$

Then solving the switching condition $V_{COMP2} = V_{CS}$ in Figure 17 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{G_I}{R_{DROOP}} \quad (23)$$

$$\text{where } G_I = \frac{R_{SENSE}}{R_{CSx}} \times R_{IMON} \times \frac{8}{10} \times A_{i_VDDNB} \quad (24)$$

where G_I is the internal current sense amplifier gain and A_{i_VDDNB} is the VDDNB current gain ratio. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the equivalent resistance of the inductor. R_{DROOP} is the equivalent load-line resistance as well as the desired static output impedance.

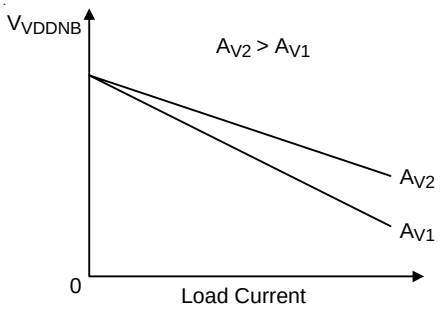

Figure 18. VDDNB Controller : Error Amplifier gain (A_V) Influence on V_{VDDNB} Accuracy

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Loop Compensation

Optimized compensation of the VDDNB controller allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 19 shows the compensation circuit. Previous design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2\pi \times C \times R_C} \quad (25)$$

Where C is the capacitance of output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (26)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad (27)$$

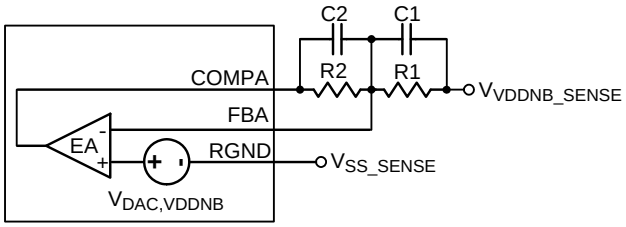

Figure 19. VDDNB Controller : Compensation Circuit

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 20 shows the On-Time setting circuit. Connect a resistor (R_{TON}) between V_{IN} and TONSETA to set the on-time of UGATE :

$$t_{ON}\ (0.5V \le V_{DAC} < 1.8V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC,VDDNB}} \quad (28)$$

Where t_{ON} is the UGATE turn-on period, V_{IN} is input voltage of the VDDNB controller, and $V_{DAC,VDDNB}$ is the DAC voltage.

When $V_{DAC,VDDNB}$ is larger than 1.8V, the equivalent switching frequency may be over 500kHz, and this too fast switching frequency is unacceptable. Therefore, the VDDNB controller implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When $V_{DAC,VDDNB}$ is larger than 1.8V, the on-time equation is modified to :

$$t_{ON}\ (V_{DAC} \ge 1.8V) = \frac{13.55 \times 10^{-12} \times R_{TON} \times V_{DAC,VDDNB}}{V_{IN} - V_{DAC,VDDNB}} \quad (29)$$

On-time translates only roughly to switching frequencies.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} = \frac{V_{DAC(MAX)} + I_{LOAD(MAX)} \times (DCR_L + R_{ON_LS\text{-}FET} - R_{DROOP})}{\left[V_{IN(MAX)} + I_{LOAD(MAX)} \times (R_{ON_LS\text{-}FET} - R_{ON_HS\text{-}FET})\right] \times (T_{ON} - T_D + T_{ON,VAR}) + I_{LOAD(MAX)} \times (R_{ON_LS\text{-}FET}) \times T_D} \quad (30)$$

Where $f_{S(MAX)}$ is the maximum switching frequency, T_D is the driver dead time, $T_{ON,VAR}$ is the TON variation value. $V_{DAC(MAX)}$ is the maximum $V_{DAC,VDDNB}$ of application, $V_{IN(MAX)}$ is the maximum application input voltage, $I_{LOAD(MAX)}$ is the maximum load of application, $R_{ON_LS\text{-}FET}$ is the on-resistance of low side FET $R_{DS(ON)}$, $R_{ON_HS\text{-}FET}$ is the on-resistance of high side FET $R_{DS(ON)}$, DCR_L is the inductor equivalent resistance of the inductor, and R_{DROOP} is the load-line setting.

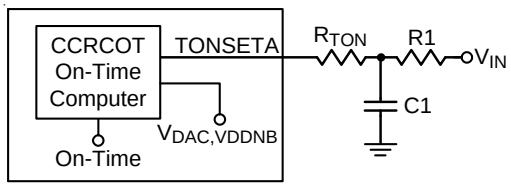

Figure 20. VDDNB Controller : On-Time Setting with RC Filter

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Current Sense Setting

The current sense topology of the VDDNB controller is continuous inductor current sensing. Therefore, the controller is less sensitive to noise. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENAxP and ISENAxN pins denote the positive and negative input of the current sense amplifier of each phase.

Users can either use a current sense resistor or the inductor's DCR_L for current sensing. Using the inductor's DCR_L allows higher efficiency as shown in Figure 21.

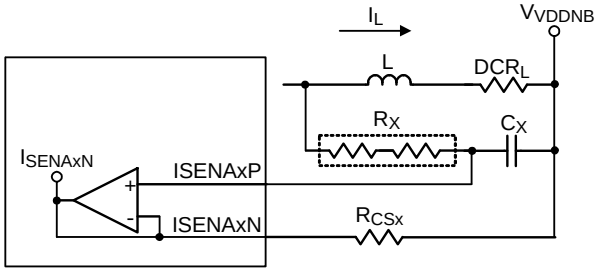

Figure 21. VDDNB Controller : Lossless Inductor Sensing

In order to optimize transient performance, R_X and C_X must be set according to the equation below :

$$\frac{L}{DCR_L} = R_X \times C_X \quad (31)$$

Then the proportion between the phase current, I_L, and the sensed current, I_{SENAxN}, is driven by the value of the effective sense resistance, R_{CSx}, and the DCR_L of the inductor. The resistance value of R_{CSx} is limited by the internal circuitry. The recommended value is from 500Ω to 1.2kΩ.

$$I_{SENAxN} = I_L \times \frac{DCR_L}{R_{CSx}} \quad (32)$$

Considering the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load-line requirement and the response time is too fast causing a ring back, the value of resistance should be increased. Vice versa, with a high resistance, the output voltage transient has only a small initial dip with a slow response time. R_X is highly recommended as two 0603 size resistors in series to enhance the Iout reporting accuracy. C_X is suggested X7R type for the application.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the above mentioned inductor equivalent resistance sensing method.

Per-Phase Over Current Protection

The VDDNB controller provides over current protection in each phase. For VDDNB controller in two-phase configuration, either phase can trigger Per-Phase Over Current Protection (PHOCP).

The VDDNB controller senses each phase inductor current I_L, and PHOCP comparator compares sensed current with PHOCP threshold current, as shown in Figure 22.

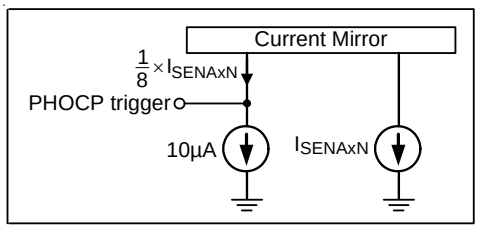

Figure 22. VDDNB Controller : Per-Phase OCP Setting

The resistor R_{CSx} determines PHOCP threshold.

$$I_{L,PERPHASE(MAX)} \times \frac{DCR_L}{R_{CSx}} \times \frac{1}{8} = 10\mu A \quad (33)$$

$$R_{CSx} = \frac{I_{L,PERPHASE(MAX)} \times DCR_L}{8 \times 10\mu A} \quad (34)$$

The controller will turns all high-side/low-side MOSFETs to protect CPU if the per-phase over current protection is triggered.

Initial Offset and External Offset (Over Clocking Offset Function)

The VDDNB controller features over clocking offset function which provides the possibility of wide range offset of output voltage. The initial offset function can be implemented through the SVI interface. When the OFSA pin voltage < 0.3V at EN rising edge, the initial offset is disabled.

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The external offset function can be implemented by the SET2 pin setting. For example, referring to Table 12, when the both rail external offset functions are enabled, the output voltage is :

$$V_{VDDNB} = V_{DAC,VDDNB} - I_{LOAD} \times R_{DROOP} + V_{External_OFSA} + V_{Initial_OFSA} \quad (35)$$

$V_{Initial_OFSA}$ is the initial offset voltage set by SVI interface, and the external offset voltage, $V_{External_OFSA}$ is set by supplying a voltage into the OFSA pin.

It can be calculated as below :

$$V_{External_OFSA} = V_{OFSA} - 1.2V \quad (36)$$

If supplying 1.3V at OFSA pin, it achieves 100mV offset at the output. Connecting a filter capacitor between the OFSA and GND pins is necessary. Designers can design the offset slew rate by properly setting the filter bandwidth.

Dynamic VID Enhancement

During a dynamic VID event, the charging (dynamic VID up) or discharging (dynamic VID down) current causes unwanted load-line effect which degrades the settling time performance. The RT3663BH holds the inductor current to hold the load-line during a dynamic VID event. The VDDNB controller always enters two-phase configuration when VDDNB controller receives dynamic VID up and VDDNB controller holds the operating state when VDDNB controller receives dynamic VID down.

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Current Monitoring and Current Reporting

The VDDNB controller provides current monitoring function via inductor current sensing. In the G-NAVP™ technology, the output voltage is dependent on output current, and the current monitoring function is achieved by this characteristic of output voltage. The equivalent output current is sensed from inductor current sensing and mirrored to the IMONA pin. The resistor connected to the IMONA pin determines voltage of the IMONA output.

$$V_{IMONA} = I_{L,SUM} \times 2 \times \frac{DCR_L}{R_{CSx}} \times R_{IMONA} + 0.64 \quad (37)$$

Where I_L is the phase current, R_{CSx} is the effective sense resistance, and R_{IMONA} is the current monitor current setting resistor. Note that the IMONA pin cannot be monitored.

The ADC circuit of the VDDNB controller monitors the voltage variation at the IMONA pin from 0V to 3.19375V, and this voltage is decoded into digital format and stored into Output_Current register. The ADC divides 3.19375V into 511 levels, so LSB = 3.19375V / 511 = 6.25mV.

Quick Response

The VDDNB controller utilizes a quick response feature to support heavy load current demand during instantaneous load transient. The VDDNB controller monitors the current of the V_{VDDNB_SENSE}, and this current is mirrored to internal quick response circuit. At steady state, this mirrored current does not trigger a quick response. When the V_{VDDNB_SENSE} voltage drops abruptly due to load transient, the mirrored current flowing into quick response circuit increases instantaneously.

The QR threshold setting for VDDNB controller refers to Table 5.

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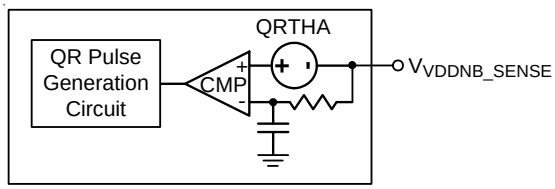

Figure 23. VDDNB Controller : Quick Response Triggering Circuit

When quick response is triggered, the quick response circuit generates a quick response pulse. The pulse width of quick response is almost the same as t_{ON}.

After generating a quick response pulse, the pulse is then applied to the on-time generation circuit, and all the active phases' on-times are overridden by the quick response pulse.

Over-Current Protection

The RT3663BH has dual OCP mechanism. The dual OCP mechanism has two types of thresholds. The first type, referred to as OCP-TDCA, is a time and current based threshold. OCP-TDCA should trip when the average output current exceeds TDCA by some percentage and for a period of time. This period of time is referred to as the trigger delay. The second type, referred to as OCP-SPIKEA, is a current based threshold. OCP-SPIKEA should trip when the cycle-by-cycle output current exceeds IDDSPIKEA by some percentage. If either mechanism trips, then the VDDNB controller asserts OCP_L and delays any further action. This delay is called an action delay. Refer to action delay time. After the action delay has expired and the VDDNB controller has allowed its current sense filter to settle out and the current has not decreased below the threshold, then the VDDNB controller turns off both high-side MOSFETs and low-side MOSFETs of all channels.

Users can set OCP-SPIKEA threshold, $I_{L,SUM(SPIKEA)}$, by the current monitor resistor R_{IMONA} of the following equation :

$$I_{L,SUM\ (SPIKE)} = \frac{3.19375 - 0.64}{2 \times DCR} \times \frac{R_{CSx}}{R_{IMONA}} \quad (38)$$

And set the OCP-TDCA threshold, $I_{L(TDCA)}$, by some percentage of OCP-SPIKEA through Table 3.

Over-Voltage Protection (OVP)

The over-voltage protection circuit of the VDDNB controller monitors the output voltage via the VSENA pin after POR. When VID is lower than 0.9V, once VSENA voltage exceeds "0.9V + 325mV", OVP is triggered and latched. When VID is larger than 0.9V, once VSENA voltage exceeds the internal reference by 325mV, OVP is triggered and latched. The VDDNB controller tries to turn on low-side MOSFETs and turn off high-side MOSFETs of all active phases of the VDDNB controller to protect the CPU. When OVP is triggered by one rail, the other rail also enters soft shut down sequence. A 1µs delay is used in OVP detection circuit to prevent false trigger.

Negative-Voltage Protection (NVP)

During OVP latch state, the VDDNB controller also monitors the VSENA pin for negative voltage protection. Since the OVP latch continuously turns on all low-side MOSFETs of the VDDNB controller, the VDDNB controller may suffer negative output voltage. As a consequence, when the VSENA voltage drops below 0V after triggering OVP, the VDDNB controller triggers NVP to turn off all low-side MOSFETs of the VDDNB controller while the high-side MOSFETs remain off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. The NVP function is active only after OVP is triggered.

Under-Voltage Protection (UVP)

The VDDNB controller implements under-voltage protection of $V_{OUT,VDDNB}$. If VSENA voltage is less than the internal reference by 500mV, the VDDNB controller triggers UVP latch. The UVP latch turns off both high-side and low-side MOSFETs. When UVP is triggered by one rail, the other rail also enters soft shutdown sequence. A 3µs delay is used in UVP detection circuit to prevent false trigger.

Under-Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below IC POR threshold, the VDDNB controller triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers. A 3µs delay is used in UVLO detection circuit to prevent false trigger.

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Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (26.5°C/W) = 3.77W for a WQFN-52L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 24 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

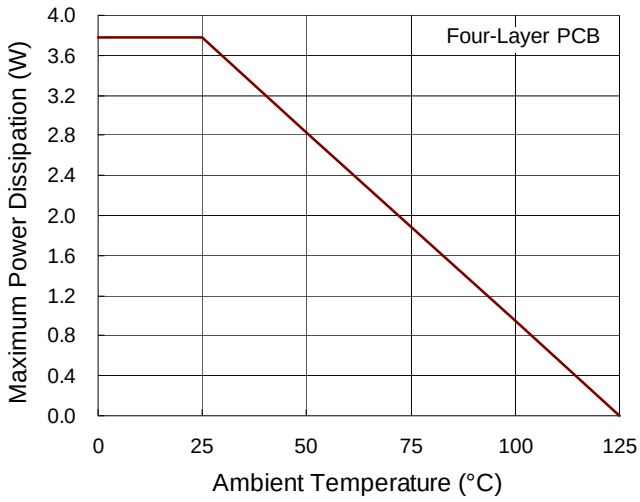

Figure 24. Derating Curve of Maximum Power Dissipation

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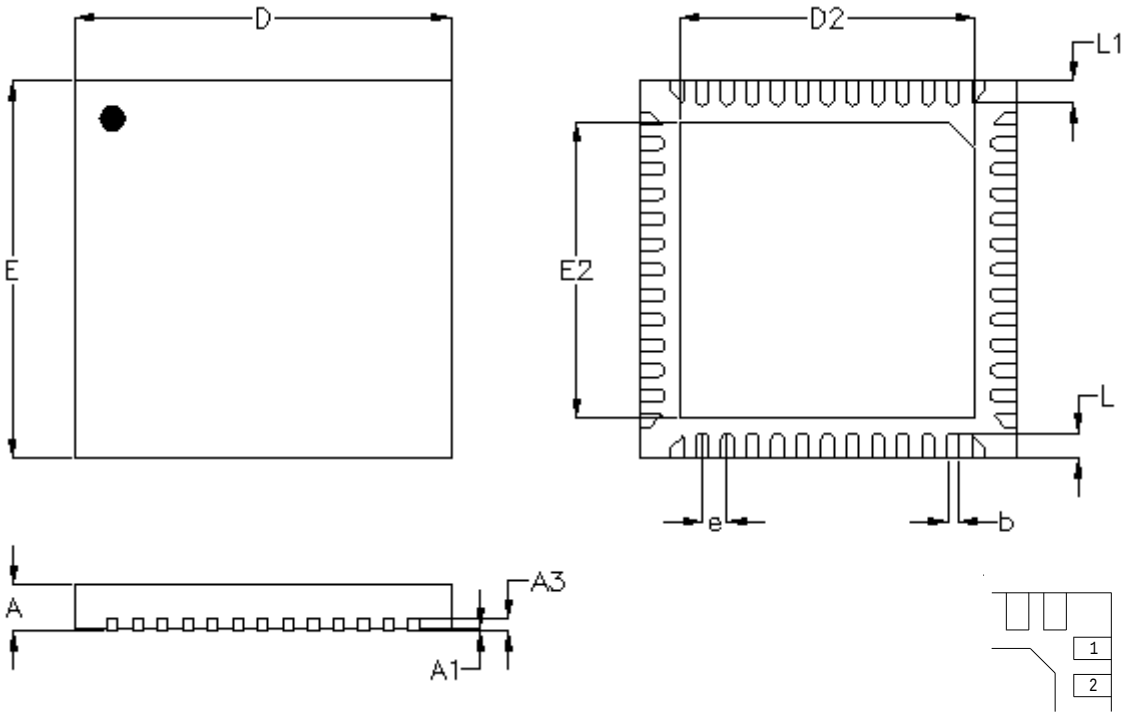
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

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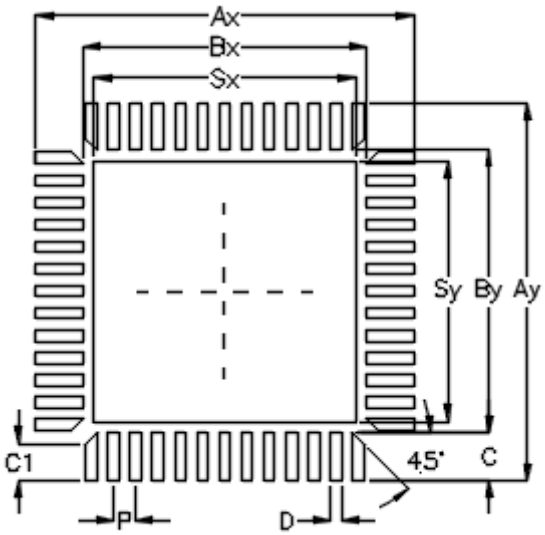
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C*52	C1*8	D	Sx	Sy	
V/W/U/XQFN6*6-52	52	0.40	6.80	6.80	5.10	5.10	0.85	0.65	0.20	4.70	4.70	±0.05

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