2-Phase PWM Controller with I²C Interface Control for AMD SVI3 Power Supply

General Description

The RT3672EE is a synchronous buck controller that supports single output rail and fully meets AMD SVI3 requirements. The RT3672EE adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all AMD CPU/GPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3672EE features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and to reduce output capacitors. The RT3672EE integrates a high accuracy ADC for reporting and a non-volatile memory (NVM) to store custom configurations, such as output current scale, auto phase add/drop threshold, switching frequency, overcurrent threshold or AQR trigger level. It also features full fault protection functions, including overvoltage (OV), undervoltage (UV), overcurrent (OC), undervoltage lockout (UVLO), over-temperature protection (OTP), VR-hot warning, CRC failure and communication failure. The RT3672EE provides enable, power good and temperature sensing. It also supports functions that can be set by the I²C interface.

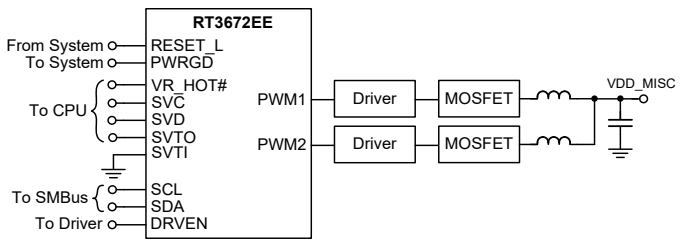
Applications

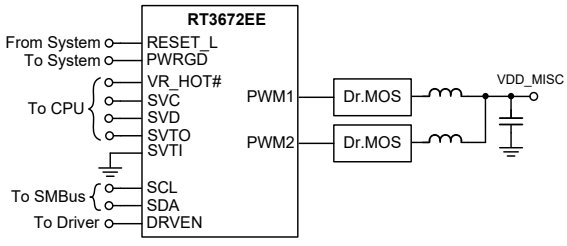
- AMD SVI3 VDD_MISC Rail
- Desktop and Notebook Computer
- AVP Step-Down Converter

Features

- **AMD SVI3 Rev 1.01 Compatible**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode (DEM) at Light Load**
- **Fast Transient Response: Adaptive Quick Response (AQR), Absolutely Quick Response (ABS_QR)**
- **OVP, OCP and UVP with Flag**
- **Switching Frequency Setting**
- **Auto Phase Add/Drop with DEM for Excellent Efficiency**
- **Voltage On-the-Fly (VOTF) Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-line**
- **Standard I²C Protocol Interface**
  - **Internal Non-Volatile Memory (NVM) to Store Custom Configurations**
  - **Current Balance Gain Adjustment for Thermal Balance**
  - **Dynamic Load-line Setting**
  - **Voltage Offset Setting**
  - **Fixed VID Setting**
  - **Protection Report and Protection Disable**
  - **Monitoring for Output Voltage/Output Current/ Temperature**
- **Soldering Good Detection**
- **Small 48-Lead WQFN Package**

Simplified Application Circuit





Ordering Information

RT3672EE □□-□

- The configuration code identifier for the register setting stored in the internal NVM
- Package Type
  QW: WQFN-48L 6x6 (W-Type)
  (Exposed Pad-Option 4)
- Lead Plating System
  G: Green (Halogen Free and Pb Free)

Note:

Richtek products are:

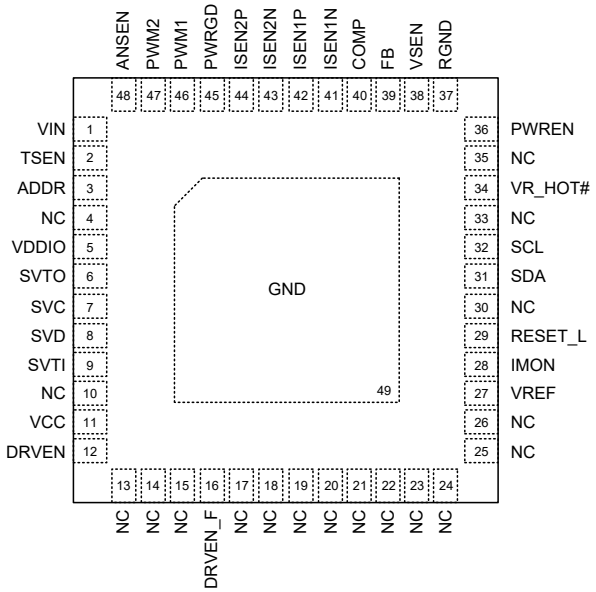
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT3672EEGQW: Product Code
YMDNN: Date Code

Pin Configuration

(TOP VIEW)`



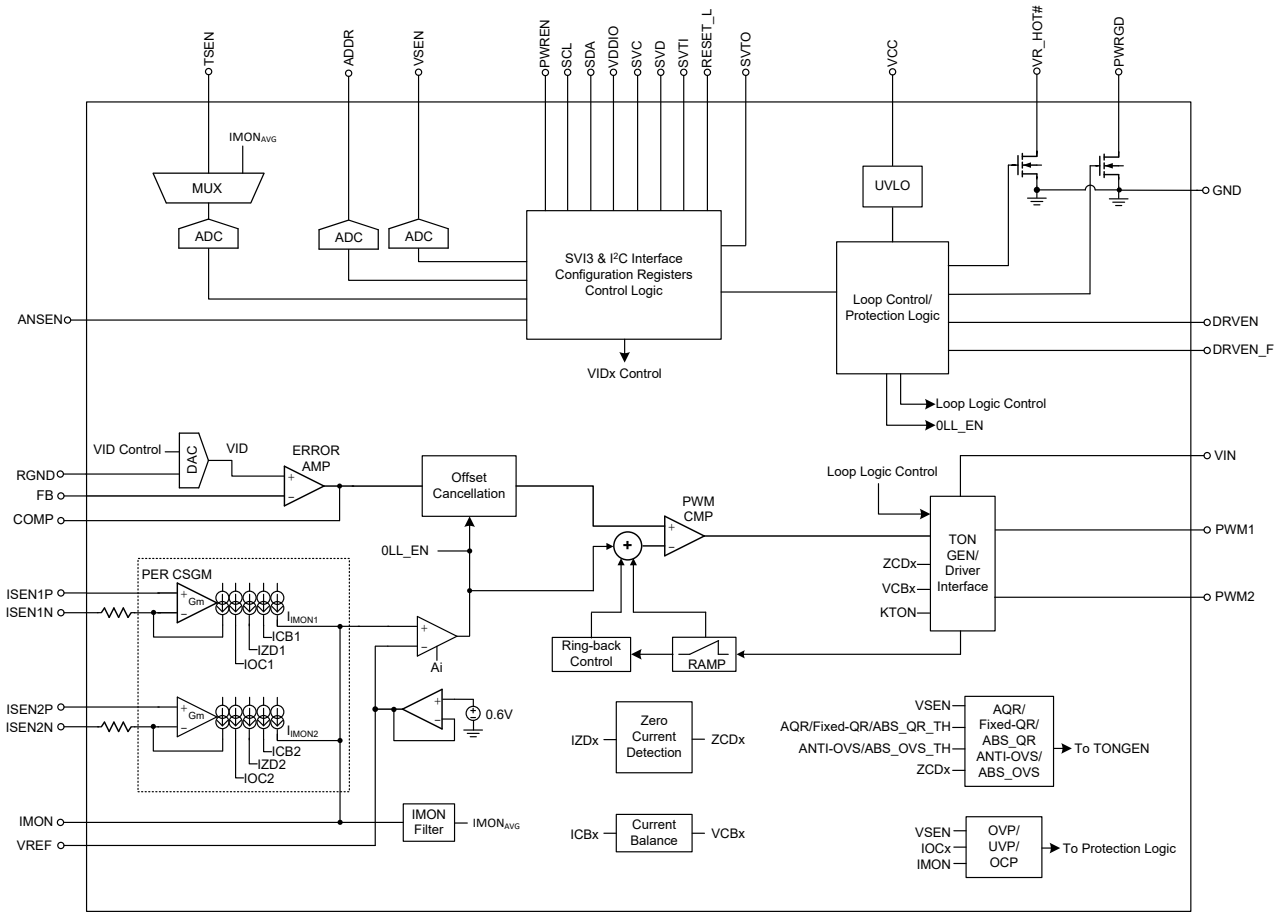
WQFN-48L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	VIN input pin. Connect a low pass filter to this pin to set on-time.
2	TSEN	External temperature sense input pin. Connect to NTC or integrated power stage temperature sensor.
3	ADDR	A resistor tied to ground sets SMBus address. For soldering check, connect the ADDR pin to 5V and pull the PWREN high. If the soldering is good, output voltage is 1.1V.
4, 10, 13, 14, 15, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 30, 33, 35	NC	No internal connection.
5	VDDIO	Supply voltage input of SVI3 interface. This pin serves as the reference for SVC, SVD, SVTI and SVTO.
6	SVTO	Serial VID Telemetry output. This pin is a push-pull output.
7	SVC	Serial VID Clock input. This pin is a push-pull signal that acts as a clock for SVD, SVTI and SVTO.
8	SVD	Serial VID Data input. This pin is a push-pull signal that transmits commands from the controller to the targets.
9	SVTI	Serial VID Telemetry input. This pin is driven by the next-furthest target on the telemetry daisy-chain.

Pin No.	Pin Name	Pin Function
11	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 1Ω and C = 2.2μF. The decoupling capacitor should be placed as close to PWM controller as possible. The recommended size of R_{VCC} is 0603.
12	DRVEN	External driver mode control. As PSI6 command is received, this pin is in low state. The output high level is VCC.
16	DRVEN_F	External driver mode control. As PSI6 command is received, this pin is in floating state. The output high level is VCC.
27	VREF	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of IMON pin. When the controller shuts down or sets in PSI6, voltage source shuts down. An external 0.47-μF decoupling capacitor and a 3.9-Ω resistor must be placed between this pin and GND.
28	IMON	VR current monitor output. This pin outputs a current proportional to the output current.
29	RESET_L	Input pin of SVI3 interface. Active low signal will reset all SVI3 state machines and SVI3 define registers to default values.
31	SDA	I^2C data signal.
32	SCL	I^2C clock signal.
34	VR_HOT#	Thermal warning flags. This open-drain output will be pulled low in the event of a sense over-temperature warning without disabling the regulator.
36	PWREN	Active high output enable input pin. Faults are cleared when PWREN is toggled but no effect on the sticky SVI3_FAULT_STATUS bits.
37	RGND	Negative differential voltage sense input for rail. Connect to negative remote sensing point.
38	VSEN	Positive differential voltage sense input for rail. Connect to positive remote sensing point and should be routed with RGND as a differential pair.
39	FB	Error amplifier voltage feedback.
40	COMP	Error amplifier output.
41	ISEN1N	Phase #1 current sense inputs. The ISEN1N and ISEN1P pins are used to differentially sense the corresponding channel current. Connect ISEN1P to VCC if rail is not used.
42	ISNE1P	
43	ISEN2N	Phase #2 current sense inputs of rail. The ISEN2N and ISEN2P pins are used to differentially sense the corresponding channel current. Connect ISEN2P to VCC programs single phase operation.
44	ISEN2P	
45	PWRGD	Power Good indicator. This open-drain output requires an external pull-up resistor. PWRGD is pulled low when a shutdown fault occurs.
46	PWM1	Phase #1 PWM output. This signal is used to drive the PWM input of the FET diver IC. Unused PWM pins should be left unconnected. The PWM tri-state windows can be selected by NVM. One is 1.6V to 2.2V and the other is 1.4V to 2.1V.
47	PWM2	Phase #2 PWM output. Refer to PWM1 description.
48	ANSEN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
49 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough via numbers for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVPTM Control Mode

The RT3672EE adopts G-NAVP^{TM} (Green Native AVP), which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3672EE generates a PWM pulse to achieve loop modulation.

Figure 1 shows the basic G-NAVP^{TM} behavior. The COMP signal is the inverted and amplified signal of the output voltage. The COMP rises due to output voltage droop, and the rising COMP forces PWM to turn on earlier and more closely. After inductor current reaches loading current, COMP enters another steady-state of higher voltage, and the corresponding output voltage is in the steady-state of lower voltage. The load-line, output voltage drooping proportional to loading current, is achieved.

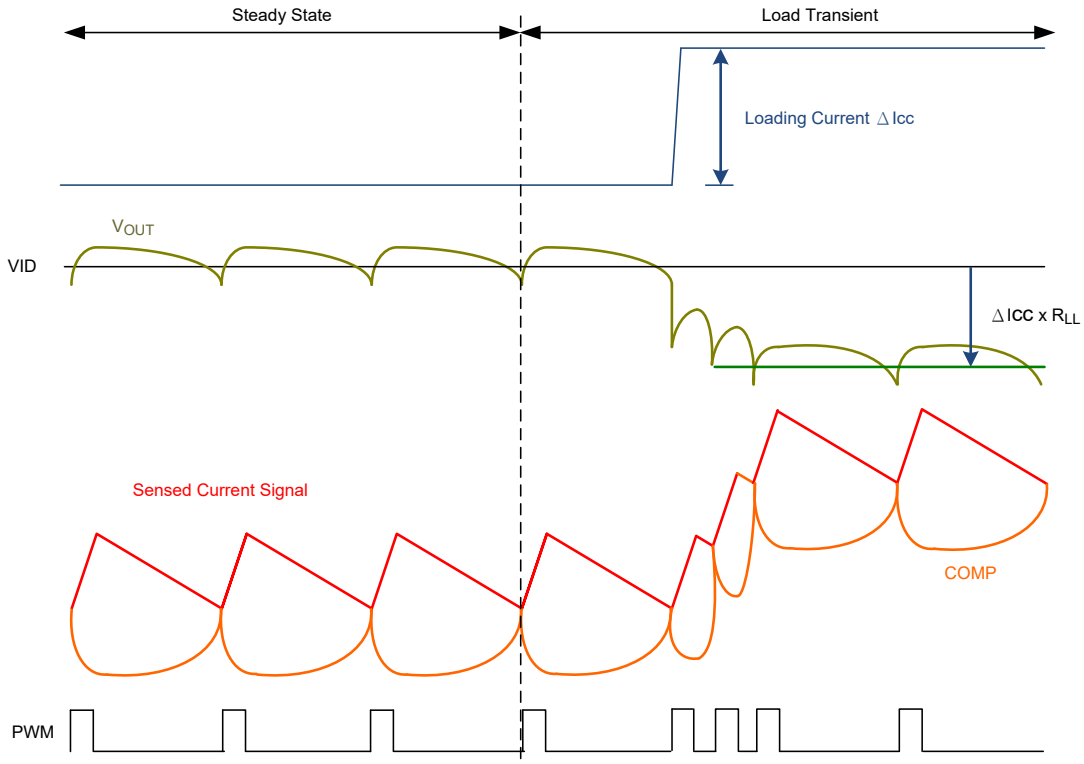


Figure 1. G-NAVP^{TM} Behavior Waveform

SVI3, I²C Interface, Control Logic and Configuration Registers

SVI3 Interface receives or transmits SVI3 signal with CPU. The I²C Interface receives or transmits I²C signal with SMBus. Control Logic executes command (Read/Write/Reset registers, VID/Address packets, Change Power State and Telemetry Request) and sends related signals to control VR. Configuration Registers include function setting registers and SVI3 required registers.

IMON Filter

IMON Filter is used to average current signal by an analog low-pass filter. It outputs IMON to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs for TSEN and IMON. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The UVLO detects the VCC voltage. As VCC exceeds the threshold, the controller issues POR = high and waits PWREN. After both POR and PWREN are ready, the controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to VID packets command, Control Logic dynamically changes VID voltage to the target voltage with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and overcurrent protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by NVM. It helps wide application range of DCR and load-line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal with sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accurately.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (Anti-overshoot Function).

AQR/Fixed-QR/ABS_QR/ANTI-OVS/ABS_OVS

The Adaptive Quick Response (AQR) is a new generation of quick response mechanism that detects loading rising edge and allows all PWMs to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by NVM. ANTI-OVS can help overshoot reduction to detect loading falling edge and to force all PWMs in tri-state until the zero current is detected.

TONGEN/Driver Interface

The PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWMs to turn on at the same time. Driver interface provides high/low/tri-state to drive external driver. In power saving mode, driver

interface forces PWM in tri-state to turn off high-side and low-side power MOSFETs according to zero current detection output. In addition, the PWM state is controlled by protection logic. Different protections force required PWM state.

VCC_UVLO/OVP/UVP/SSOCP/OCP/OTP/VR-HOT Warning/CRC Failure/Communication Failure

VCC undervoltage lockout/Overvoltage protection/ undervoltage protection/Soft-start overcurrent protection/Overcurrent protection/Over-temperature protection/VR-hot warning/CRC failure/Communication Failure.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- VIN to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4)

- WQFN-48L 6x6, θ_{JA} ---------- 26.5°C/W
- WQFN-48L 6x6, $\theta_{JC(Top)}$ ---------- 14.79°C/W

Electrical Characteristics

(V_{CC} = 5V, V_{VDDIO} = 1.8V, typical values are referenced to T_J = 25°C, Min. and Max. values are referenced to T_J from –10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	--	5.5	V
Supply Current	I_{VCC}	VCC = 5V, PWREN = H, no switching	--	--	40	mA
Supply Current at PSI6	I_{VCC_PSI6}	VCC = 5V, PWREN = H, in PSI6	--	--	180	μA
Shutdown Current	I_{SHDN}	VCC = 5V, PWREN = L	--	--	180	μA
VCC Power-ON Reset (POR)	$V_{CC\_POR\_R}$	Rising edge	4.2	4.32	4.45	V
	$\Delta V_{CC\_POR\_F\_HYS}$	Falling edge hysteresis	--	170	--	mV
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_R}$	Rising edge	--	3.6	3.75	V
	$V_{CC\_POR\_NVM\_F}$	Falling edge	3.32	3.47	--	
Reference and DAC						
DAC Accuracy	V_{FB}	0.50 to 0.995 T_A = 0 to 85°C	–5	--	5	mV
		1.000 to 2.800 T_A = 0 to 85°C	–0.5	--	0.5	%

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Slew Rate							
VOTF Slew Rate	Up	UP_SR	Measure VFB from 20% target VID to 80% target VID, ΔVOTF ≥ 100mV	−10%	--	10%	mV/μs
	Down	DN_SR	Default equals to UP_SR	−10%	--	10%	
Current Sensing Amplifier							
CS Input Voltage Range		V_{CSIN}	Differential voltage range of DCR sense.	−10	--	80	mV
Current Sense Gain Error		AMIRROR	Internal current mirror gain of per phase current sense IIMON/ICS,PERx	1.2125	1.25	1.2875	A/A
TON Setting							
On-Time Setting		t_{ON}	VIN = 12V, VID = 1V, K_{TON} = 0.8	--	208	--	ns
Minimum On-Time		t_{ON_MIN}		--	70	--	ns
Protections							
Overvoltage Protection Threshold		V_{OV}	Default threshold	360	400	440	mV
De-bounce Time of OVP		t_{D_OVP}		--	0.8	--	μs
Undervoltage Protection Threshold		V_{UV}	Default threshold	360	400	440	mV
De-bounce Time of UVP		t_{D_UVP}		--	3.3	--	μs
Overcurrent Protection Threshold		V_{OCP}		−3	--	3	%
Over-Temperature Protection Threshold		T_{OTP}		--	125	--	°C
VRHOT Warning Threshold		T_{VRHOT}		--	100	--	°C
PWREN and PWRGD							
PWREN	Logic-High	V_{IH_PWREN}		1.17	--	--	V
	Logic-Low	V_{IL_PWREN}		--	--	0.63	
Leakage Current of PWREN		I_{LEAK_PWREN}		−1	--	1	μA
PWRGD Pull Low Voltage		V_{PWRGD}	I_{PWRGD} = 8mA	--	--	0.2	V
VR_HOT#							
VR_HOT# Pull Low Voltage		$V_{VR\_HOT\#}$	$I_{VR\_HOT\#}$ = 8mA	--	--	0.2	V
VREF							
VREF Voltage		V_{VREF}	Normal operation	0.59	0.6	0.61	V
Acoustic Noise Suppression (ANS)							
ANS_EN	Logic-High	$V_{IH\_ANS\_EN}$		V_{CC} − 0.7	--	--	V
	Logic-Low	$V_{IL\_ANS\_EN}$		--	--	1	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SVI3 Interface							
VDDIO Level		VDDIO		1.08	--	1.98	V
SVC, SVD, SVTI	Logic-High	V_{IH}		0.65 x VDDIO	--	--	V
	Logic-Low	V_{IL}		--	--	0.35 x VDDIO	V
SVC, SVD, SVTO Output High Voltage		V_{OH}	@-8mA	VDDIO – 0.45	--	--	V
			@-4mA	VDDIO – 0.22	--	--	V
SVC, SVD, SVTO Output Low Voltage		V_{OL}	@8mA	--	--	0.45	V
			@4mA	--	--	0.22	V
RESET_L	Logic-High	$V_{IH\_RESET\_L}$		1.17	--	--	V
	Logic-Low	$V_{IL\_RESET\_L}$		--	--	0.63	V
Leakage Current of SVC, SVD, SVTI, SVTO		I_{LEAK_SVI3}		–10	--	10	μA
I^2C Interface							
SCL, SDA	Logic-High	V_{IH_I2C}		1	--	--	V
	Logic-Low	V_{IL_I2C}		--	--	0.6	V
Standard/Fast Mode							
SCL Clock Rate		f_{SCL}	Standard mode	--	--	100	kHz
			Fast mode	--	--	400	
Hold Time (Repeated) Start Condition. After this period, the first clock pulse is generated.		t_{HD_STA}		0.6	--	--	μs
Low Period Of the SCL Clock		t_{LOW}		1.3	--	--	μs
High Period Of the SCL Clock		t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition		t_{SU_STA}		0.6	--	--	μs
Data Hold Time		t_{HD_DAT}	Standard mode	0	--	--	μs
			Fast mode	0	--	0.9	
Data Set-Up Time		t_{SU_DAT}	Standard mode	250	--	--	ns
			Fast mode	100	--	--	
Set-Up Time for STOP Condition		t_{SU_STO}		0.6	--	--	μs
Bus Free Time Between a STOP and START Condition		t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA and SCL Signals		t_R	Standard mode	--	--	300	ns
			Fast mode	20	--	300	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Falling Time of Both SDA and SCL signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
ADC						
ADC Resolution			--	10	--	bits
ADC Reference Voltage			--	3.2	--	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
ITSEN						
TSEN Source Current	I_{TSEN}	V_{TSEN} = 1.6V	79.2	80	80.8	μA
DIMON						
Digital IMON	D_{VIMON}	V_{IMON} - V_{VREF} = 0.4V	--	1023	--	Decimal
Telemetry						
Accuracy of Output Voltage Telemetry (10-bit Telemetry, 1LSB = 5mV)	$VOUT_{TEL}$	0.50 to 0.995 T_A = 0 to 85°C	–7.5	--	7.5	mV
		1.000 to 2.800 T_A = 0 to 85°C	–0.75	--	0.75	%
Temperature Reporting Accuracy (10-bit Telemetry, 1LSB = 1°C)	$TEMP_{TEL}$	Between 50°C to 125°C	–5	--	5	°C
Temperature Reporting Range			-40	--	150	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

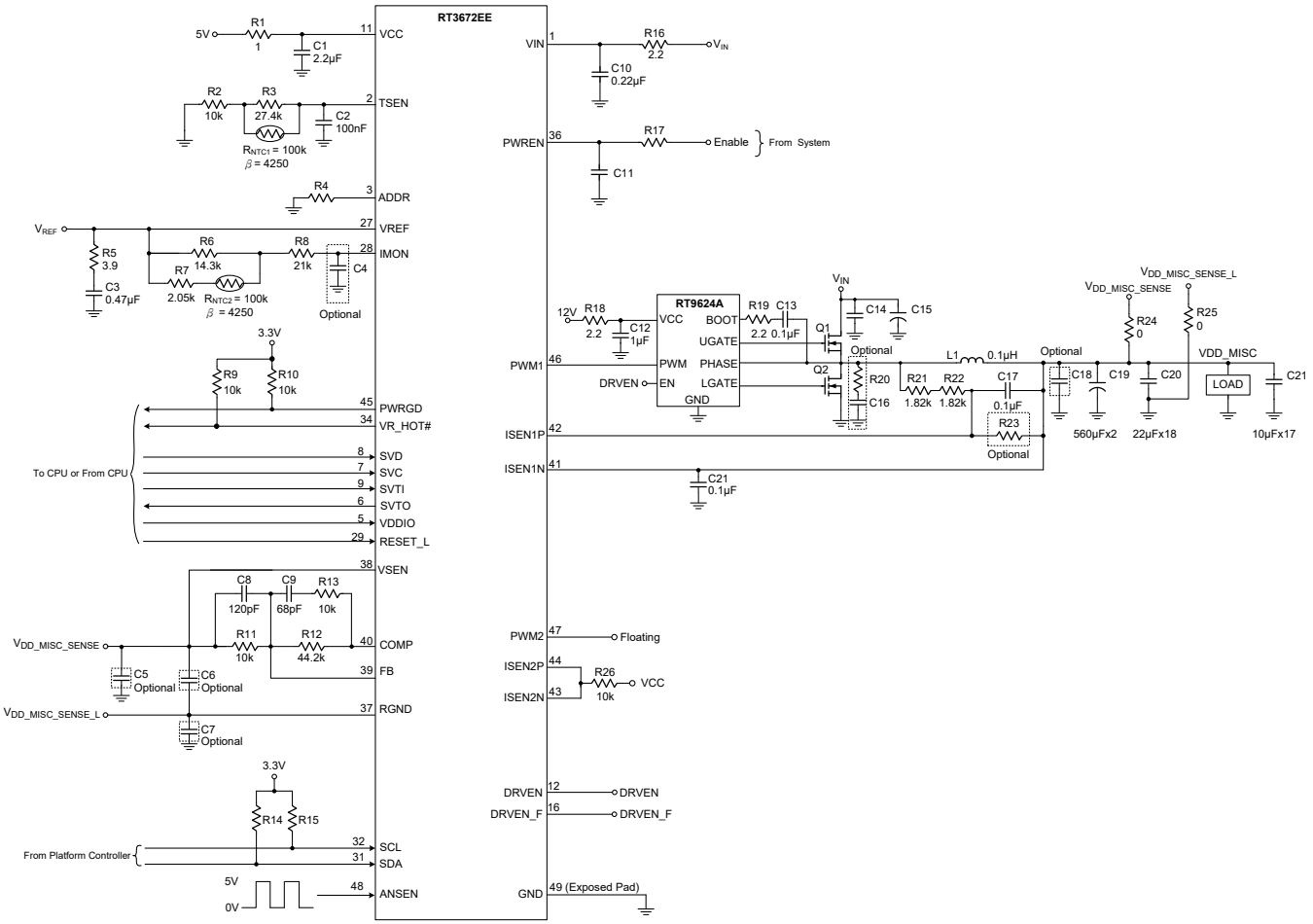
Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

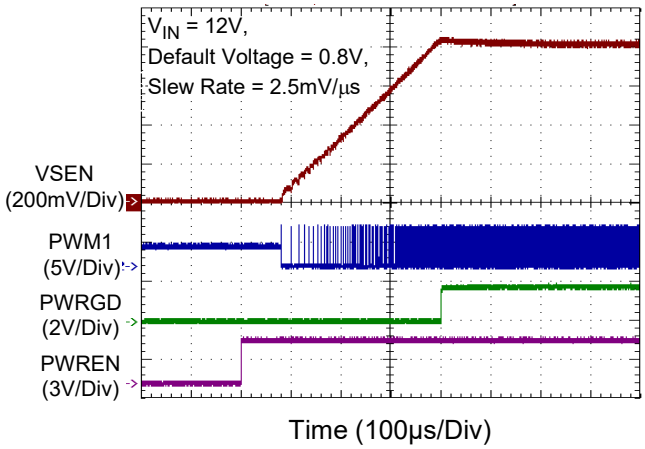
Typical Application Circuit

Platform: AM5

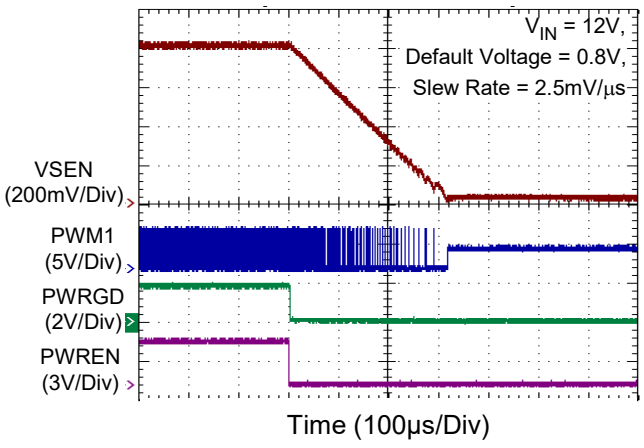


Typical Operating Characteristics

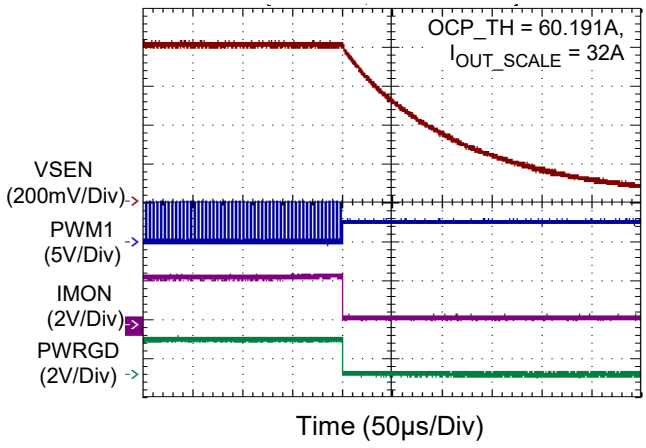
Power On from PWREN



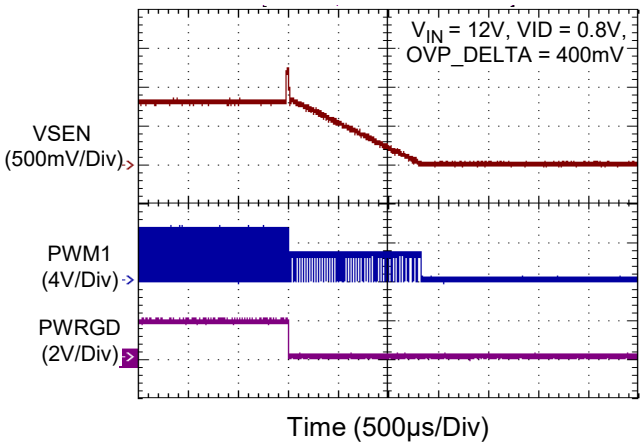
Power Off from PWREN



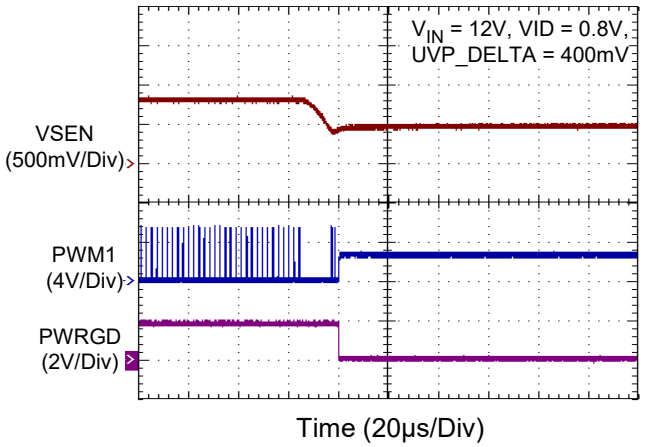
OCP



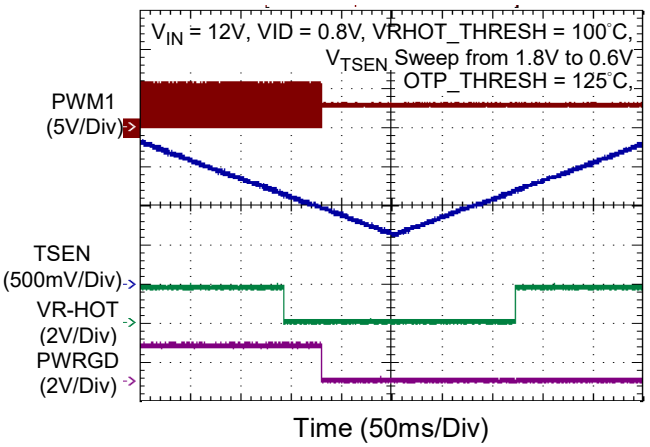
OVP



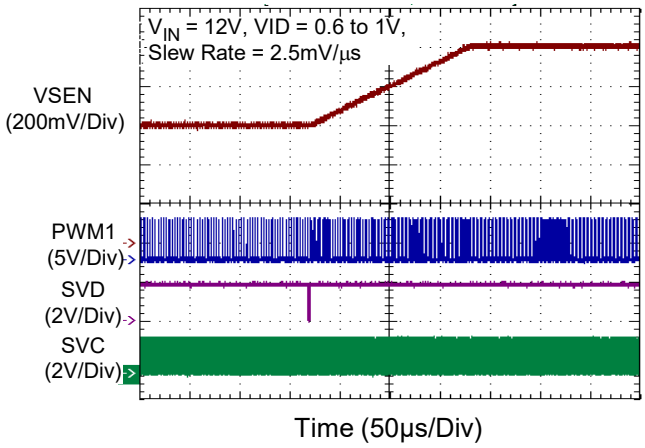
UVP



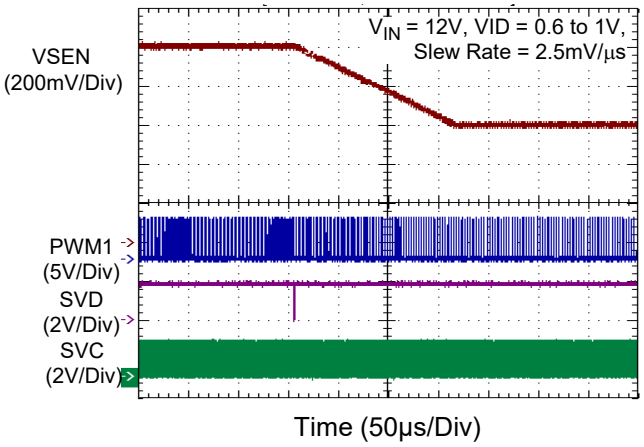
OTP and VR-HOT Warning



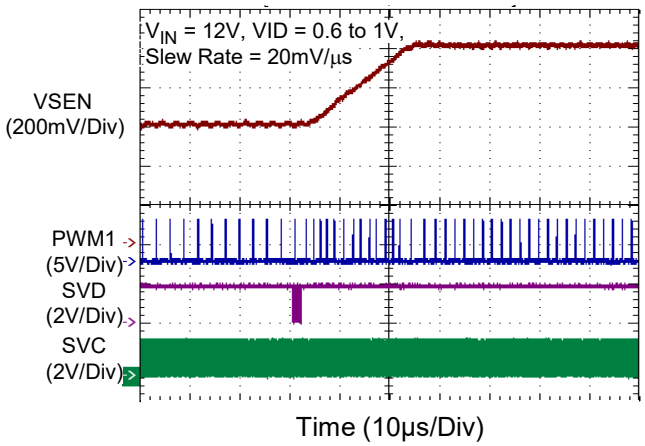
Positive VOTF Transition



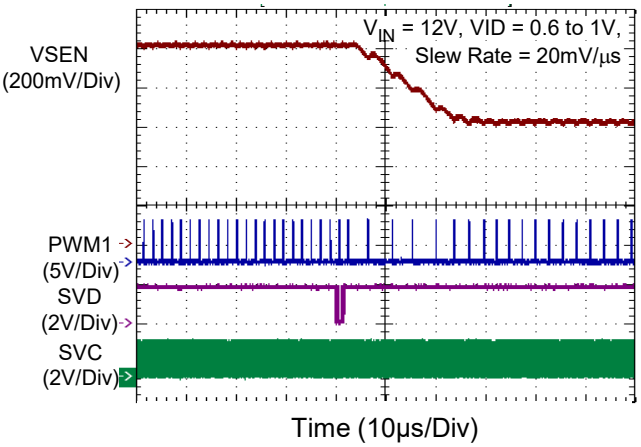
Negative VOTF Transition



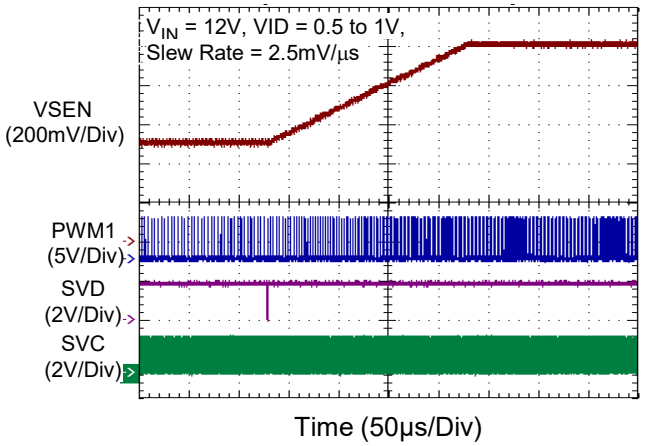
Positive VOTF Transition



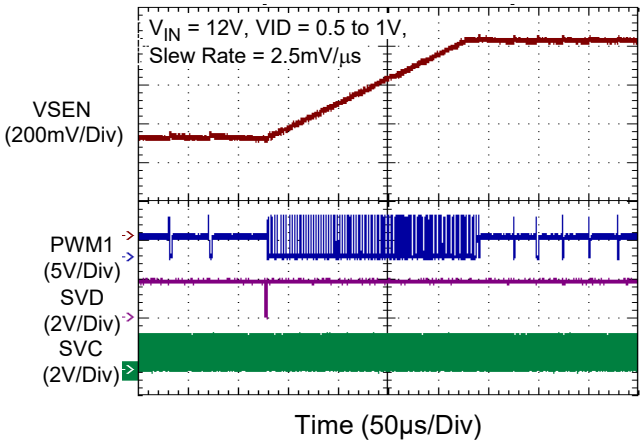
Negative VOTF Transition



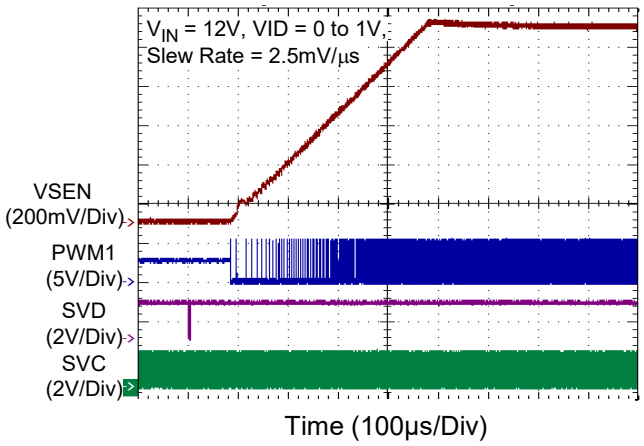
Positive VOTF Transition in PSI0



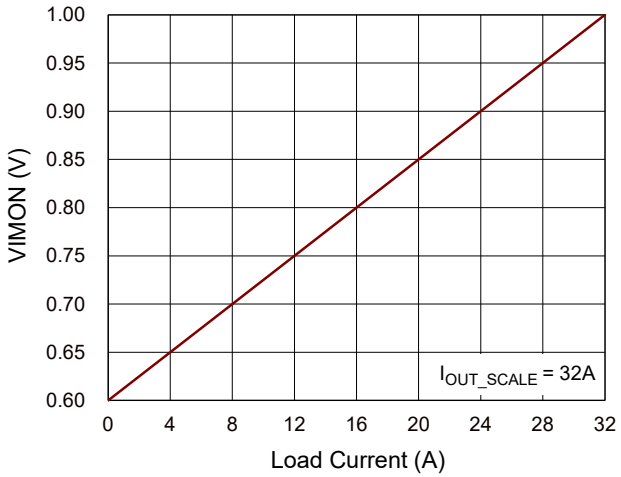
Positive VOTF Transition in PSI3



Exit Time in PSI6



VIMON vs. Load Current



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The RT3672EE is a 2/1-phase synchronous buck controller that supports single voltage rail. The RT3672EE is designed to meet AMD SVI3 compatible CPUs specification. The controller provides built-in non-volatile memory (NVM) and I^2C interface to store customized configuration. The RT3672EE is designed for notebook computers or desktop applications.

Power-On Sequence

Supply a single 5V (VCC) to the RT3672EE to start power-on. Figure 2 shows the power-on timings. NVM loading of the RT3672EE begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RT3672EE will download NVM into the control registers. When VCC exceeds VCC_POR, the RT3672EE starts initialization including internal circuit offset correction and function settings. During this period, the PWM outputs are held in high impedance (Hi-Z) state. Set the correct default levels for static input signals with pull-down resistors (such as for the I^2C address setting). The time from VCC exceeding VCC_POR threshold to assertion of PWREN is t_{VCC_EN}. The minimum t_{VCC_EN} is 8ms. When initialization is done, the controller is in ultra-low power mode. It will ramp up to default voltage with default slew rate when PWREN is high. When the start-up process is completed, PWRGD is asserted within 5μs after the output voltage exceeds minimum tolerance of output voltage. Users can set multi-functions through NVM by I^2C interface when initialization is done.

Driver power (PVCC) is strongly suggested to be ready after controller VCC. This can prevent current flowing back from driver PVCC to controller VCC through PWMx pins or DRVEN/DRVEN_F pins.

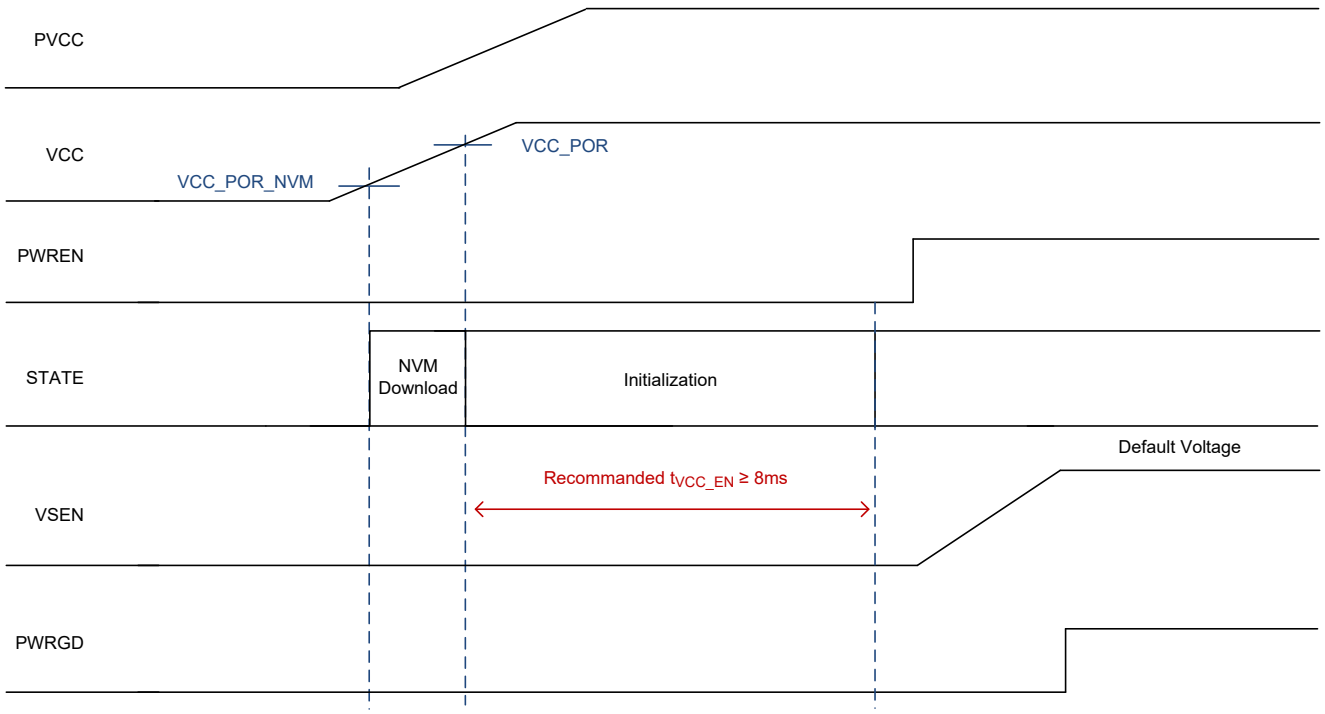


Figure 2. Typical Timing of Controller Power-ON

I²C Address Setting

The RT3672EE provides multiple I²C addresses to support multiple devices connected in one I²C bus. To properly set the I²C address (7-bit and 8-bit format), resistors with 1% tolerance must be connected from ADDR pin to ground. The required resistance is listed in Table 1. The controller sends the first target address followed by write bit (0b). For example, the 8-bit target address combines 7-bit address and write bit (0b):

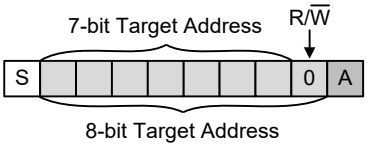


Table 1. I²C Address (HEX)

Resistance (kΩ) Typ.	I²C Address 7bit (Hex)	I²C Address 8-bit (Hex)
0.309	40	80
0.931	41	82
1.54	42	84
2.15	43	86
3.09	50	A0
4.64	51	A2
4.99	52	A4
5.9	53	A6
6.81	60	C0
8.06	61	C2
9.31	62	C4
10.7	63	C6
11.8	70	E0
13.7	71	E2
15.8	72	E4
17.4	73	E6

Acoustic Noise Suppression

The RT3672EE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band; the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3672EE adopts acoustic noise suppression function enabled by pulling ANS_EN pin to VCC to reduce ΔV during negative VOTF (Voltage On-the- Fly).

Maximum Active Phase Number Setting

The number of active phases is determined by ISENxP voltage. The detection is only active and latched at initialization state. When ISENxP voltage > (VCC−0.5V), the maximum active phase number is (x−1). For example, pulling ISEN2P and ISEN2N to VCC programs single phase operation. It is suggested that the unused pins (such as PWM2) can be left floating. Figure 3 is a single phase operation example.

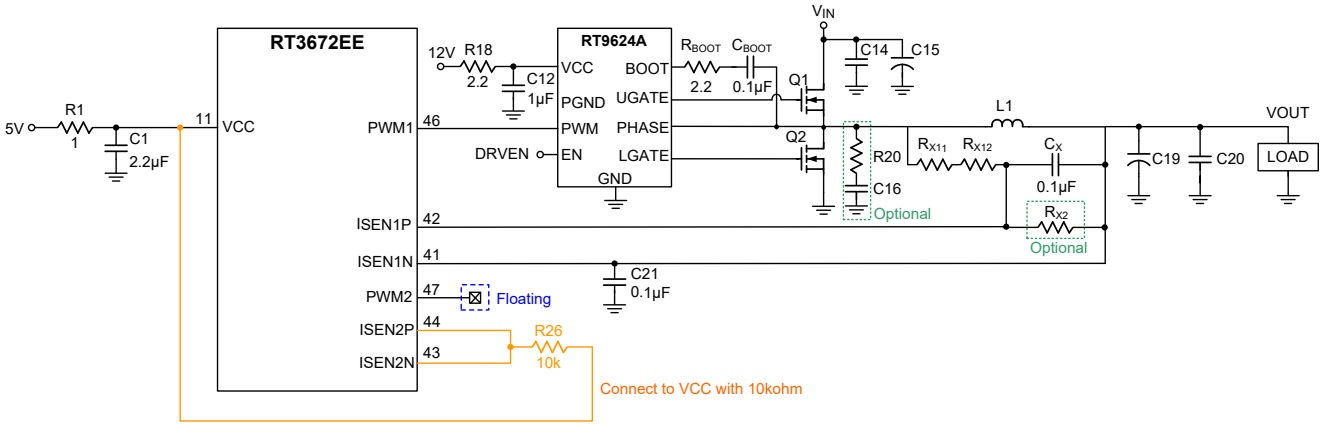


Figure 3. Single Phase Operation Setting

NVM Configuration Mechanism and SVI3 Registers

The RT3672EE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through NVM registers by the I^2C interface.

All setting functions are summarized in Table 2. Table 3 shows the functions that do not support on-line tuning. Table 4 shows the data and SVI3 registers for the SVI3 protocol. Table 5 shows the VID table of type 2 target.

Table 2. Summary of Setting Functions (Page 02)

Setting Register Map (Page 02)

Register Address/Name		Type	Default Value	Note	NVM
00h	PWM_TRI_STATE_LEVEL	R/W	01b	PWM tri-state window = 1.6V~2.2V	Yes
01h	RESERVED	R/W	04h	RESERVED	Yes
10h	CODE_VERSION_L	R/W	00h	NVM code version low byte	Yes
11h	CODE_VERSION_H	R/W	00h	NVM code version high byte	Yes
60h	VID_DEFAULT_VOLTAGE	R/W	41h	VID_DEFAULT_VOLTAGE = 0.8V	Yes
61h	RESERVED	R/W	3Ch	RESERVED	Yes
62h	RESERVED	R/W	64h	RESERVED	Yes
64h	SSOCP_EN & RATIO & I_OUT_SCALE	R/W	F1h	Soft-start OCP enabled, SSOCP_RATIO = 5, I_OUT_SCALE = Scale1: 31.96875A	Yes
65h	EN_0LL & AI_GAIN	R/W	BCh	Zero load-line enabled, AI_GAIN = 0.125	Yes
66h	ZCD_TH	R/W	E9h	ZCD_TH = -1.9mV	Yes
67h	KTON	R/W	47h	KTON = 1	Yes
68h	ANTI-OVS & VOTF_LIFT	R/W	E0h	Anti-overshoot disabled with LL, VOTF_LIFT = 0μA	Yes
69h	LPF_LIMIT_MUTI_PH & SINGLE_PH	R/W	23h	LPF_LIMIT_MUTI_PH = 100mV with LL, LPF_LIMIT_SINGLE_PH = 60mV with LL	Yes
6Ah	FIXED&ABS_QR_WD & QR_TH	R/W	FFh	PWM pulse = 2.25 × TON, QR disabled	Yes
6Bh	FIXED_QR_WD_1PH QR_TH_1PH	R/W	FFh	PWM pulse = 2.25 × TON when QR triggered, QR disabled	Yes
6Ch	AR_TH_1PH & EN_EXTD_TON & EXTD_TON_TH & EXTD_WD_MAX	R/W	63h	Adaptive ramp threshold = Disabled, TON Extend = Disabled, TON extend threshold = 150mV, TON max extend width = 1.25 × TON	Yes
6Dh	RESERVED	R/W	09h	RESERVED	Yes
6Eh	RESERVED	R/W	00h	RESERVED	Yes
6Fh	RESERVED	R/W	8Ah	RESERVED	Yes
70h	MIN_TOFF & QR_SEL & QR_SEL_1PH	R/W	C8h	MIN_TOFF = 50ns, QR_SEL = Fixed-QR QR_SEL_1PH = Fixed-QR	Yes
71h	EAGM_GAIN & SLL_RATIO & TSEN_SEL	R/W	80h	EAGM_GAIN = 1, SLL_RATIO = 100%, TSEN_SEL = External NTC thermistor.	Yes
72h	QR_TRIGGER_SEL & ABS_OVS_TH & ABS_QR	R/W	18h	QR_TRIGGER_SEL = ABS_QR Absolute-OVS threshold = 30mV with 0LL, Absolute-QR threshold = Disabled with 0LL	Yes
80h	SPM_HYS_2PH	R/W	2Eh	SPM_HYS_2PH = 7.66A	Yes
83h	SPM_TH_2PH	R/W	92h	SPM_TH_2PH = 24.31A	Yes
8Ah	IOUT_CAL_OFFSET	R/W	00h	IOUT_CAL_OFFSET = 0 LSB	Yes

Register Address/Name		Type	Default Value	Note	NVM
8Bh	IOUT_CAL_GAIN	R/W	80h	IOUT_CAL_GAIN = 100%	Yes
90h	SVI3_20h_DECAY_CONDITIONS	R/W	00h	Please refer to SVI3 specification. SVI3_20h_UP_SLEW_RATE = 2.5mV/μs.	Yes
	SVI3_20h_DOWN_SLEW_RATE				
	SVI3_20h_UP_SLEW_RATE				
91h	RESERVED	R/W	0Ah	RESERVED	Yes
92h	SVI3_22h_VOUT_OFFSET	R/W	00h	No offset	Yes
93h	SVI3_23h_VID_MAX	R/W	00h	Please refer to SVI3 specification.	Yes
94h	SVI3_24h_VID_MIN	R/W	00h	Please refer to SVI3 specification.	Yes
95h	SVI3_25h_TEN_BIT_TEL_EN	R/W	00h	Please refer to SVI3 specification.	Yes
96h	SVI3_26h_SIXTEN_BIT_TEL_EN	R/W	00h	Please refer to SVI3 specification.	Yes
97h	SVI3_27h_OCP_THRESH	R/W	F1h	NVM configurable, based on platform	Yes
98h	RESERVED	R/W	5Ch	RESERVED	Yes
99h	SVI3_29h_OCP_FAULT_DELAY	R/W	37h	NVM configurable, based on platform	Yes
9Ah	SVI3_2Ah_VRHOT_THRESH	R/W	8Ch	Please refer to SVI3 specification.	Yes
9Bh	SVI3_2Bh_OTP_THRESH	R/W	A5h	Please refer to SVI3 specification.	Yes
9Ch	SVI3_2Ch_OVP_REF	R/W	33h	Please refer to SVI3 specification.	Yes
	SVI3_2Ch_OVP_DELTA				
	SVI3_2Ch_UVP_REF				
	SVI3_2Ch_UVP_DELTA				
9Dh	RESERVED	R/W	11h	RESERVED	Yes
A0h	CRC-8 Code	R	Current status	NVM registers CRC-8 code. The Data is updated when VCC POR or restore NVM. The polynomial is $X^8 + X^2 + X^1 +1$.	No

Register Address	Bits	Register Name	Description
0x00	[7:3]	RESERVED	**Reserved bit(s).** [7:3] = 00000 (Default). All other combinations are not defined.
	[2]	PWM_TRI_STATE_LEVEL	**Set PWM tri-state window.** [2] = 0: PWM tri-state level is 1.6V to 2.2V. [2] = 1: PWM tri-state level is 1.4V to 2.1V.
	[1:0]	RESERVED	**Reserved bit(s).** [1:0] = 01 (Default). All other combinations are not defined.
0x01	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 04h (Default). All other combinations are not defined.
0x10	[7:0]	CODE_VERSION_L	**MTP Code Version.**
0x11	[7:0]	CODE_VERSION_H	**MTP Code Version.**
0x60	[7:4]	VID_DEFAULT_VOLTAGE	**Default VID setting.** SVI3 register VID_DEFAULT_VOLTAGE_08h[3:0]. [7:4] = 0000: OFF, [7:4] = 1000: 1.2V, [7:4] = 0001: 0.5V, [7:4] = 1001: 1.3V, [7:4] = 0010: 0.6V, [7:4] = 1010: 1.4V, [7:4] = 0011: 0.7V, [7:4] = 1011: 1.5V, [7:4] = 0100: 0.8V, [7:4] = 1100: 1.8V, [7:4] = 0101: 0.9V, [7:4] = 1101: 2.5V, [7:4] = 0110: 1V, [7:4] = 1110: 3.3V, [7:4] = 0111: 1.1V, [7:4] = 1111: 5V.
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 0001 (Default). All other combinations are not defined.
0x61	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 3Ch (Default). All other combinations are not defined.
0x62	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 64h (Default). All other combinations are not defined.
0x64	[7]	SSOCP_EN	**Enable soft-start overcurrent protection.** [7] = 0: Disable. [7] = 1: Enable
	[6:4]	SSOCP_RATIO	**Soft-start overcurrent protection ratio.** SSOCP_TH = I_OUT_SCALE × SSOCP_RATIO [6:4] = 000: 1.25, [6:4] = 100: 3.125, [6:4] = 001: 1.875, [6:4] = 101: 3.75, [6:4] = 010: 2.1875, [6:4] = 110: 4.375, [6:4] = 011: 2.5, [6:4] = 111: 5.
	[3]	RESERVED	**Reserved bit(s).** [3] = 0 (Default). All other combinations are not defined.
	[2:0]	I_OUT_SCALE	**Output current scale selections.** SVI3 register I_OUT_SCALE_09h[5:3]. [2:0] = 000: CUSTOM, [2:0] = 100: Reserved, [2:0] = 001: Scale 1 = 31.96875A, [2:0] = 101: Reserved, [2:0] = 010: Scale 2 = 63.9375A, [2:0] = 110: Reserved, [2:0] = 011: Reserved, [2:0] = 111: Reserved.

Register Address	Bits	Register Name	Description
0x65	[7:4]	RESERVED	**Reserved bit(s).** [7:4] = 1011 (Default). All other combinations are not defined.
	[3]	EN_0LL	**Enable zero load-line.** [3] = 0: Disable. [3] = 1: Enable.
	[2:0]	AI_GAIN	**Ai Gain is the gain of current sense amplifier.** [2:0] = 000: 0.250, [2:0] = 100: 0.125, [2:0] = 001: 0.500, [2:0] = 101: 0.375, [2:0] = 010: 0.750, [2:0] = 110: 0.625, [2:0] = 011: 1.000, [2:0] = 111: 0.875.
0x66	[7:6]	RESERVED	**Reserved bit(s).** [7:6] = 11 (Default). All other combinations are not defined.
	[5:0]	ZCD_TH	**Zero current threshold setting of each phase sensed current.** [5]: Sign bit, 0 stands for positive values and 1 for negative. [4:0]: 0.2083mV/step. Ex: [5:0] = 000000: ZCD_TH = 0mV, [5:0] = 000001: ZCD_TH = 0.2083mV, [5:0] = 000010: ZCD_TH = 0.4167mV, [5:0] = 011111: ZCD_TH = 6.4573mV, [5:0] = 100000: ZCD_TH = 0mV, [5:0] = 100001: ZCD_TH = –0.2083mV, [5:0] = 100010: ZCD_TH = –0.4167mV, [5:0] = 111111: ZCD_TH = –6.4573mV.
0x67	[7:5]	RESERVED	Reserved bit(s). [7:5] = 010 (Default). All other combinations are not defined.
	[4:0]	KTON	**On-time (TON) K-Factor setting.** **When reg. addr 0x67[4] = 0:** KTON = 0.3 + [3:0] × 0.1 **When reg. addr 0x67[4] = 1:** KTON = 1.2 + [3:0] × 0.1 For example, [4:0] = 00000: KTON = 0.3, [4:0] = 00101: KTON = 0.8, [4:0] = 01001: KTON = 1.2, [4:0] = 01111: KTON = 1.8, [4:0] = 10000: KTON = 1.2, [4:0] = 10101: KTON = 1.7, [4:0] = 11111: KTON = 2.7.

Register Address	Bits	Register Name	Description
0x68	[7:5]	ANTI-OVS	**Anti-overshoot threshold setting with load-line.** [7:5] = 000: 90mV, [7:5] = 100: 300mV, [7:5] = 001: 120mV, [7:5] = 101: 360mV, [7:5] = 010: 180mV, [7:5] = 110: 420mV, [7:5] = 011: 240mV, [7:5] = 111: Disable.
	[4:0]	VOTF_LIFT	**Output compensation setting for VOTF (Voltage On-the-Fly).** **When VOTF_LIFT[4] = 1** [3:0] = 0000: disable, [3:0] = 1000: 9μA, [3:0] = 0001: 2μA, [3:0] = 1001: 10μA, [3:0] = 0010: 3μA, [3:0] = 1010: 12μA, [3:0] = 0011: 4μA, [3:0] = 1011: 14μA, [3:0] = 0100: 5μA, [3:0] = 1100: 16μA, [3:0] = 0101: 6μA, [3:0] = 1101: 18μA, [3:0] = 0110: 7μA, [3:0] = 1110: 20μA, [3:0] = 0111: 8μA, [3:0] = 1111: 24μA. **When VOTF_LIFT[4] = 0** [3:0] = 0000: disable, [3:0] = 1000: 18μA, [3:0] = 0001: 4μA, [3:0] = 1001: 20μA, [3:0] = 0010: 6μA, [3:0] = 1010: 24μA, [3:0] = 0011: 8μA, [3:0] = 1011: 28μA, [3:0] = 0100: 10μA, [3:0] = 1100: 32μA, [3:0] = 0101: 12μA, [3:0] = 1101: 36μA, [3:0] = 0110: 14μA, [3:0] = 1110: 40μA, [3:0] = 0111: 16μA, [3:0] = 1111: 48μA.
0x69	[7:4]	LPF_LIMIT_MUTI_PH	**High frequency ACLL compensation setting for multi-phase operation with load-line.** LPF_LIMIT_MUTI_PH = 60mV + [7:4] × 20mV For example, [7:4] = 0000, LPF_LIMIT_MUTI_PH = 60mV, [7:4] = 0010, LPF_LIMIT_MUTI_PH = 100mV, [7:4] = 1111, LPF_LIMIT_MUTI_PH = 360mV.
	[3:0]	LPF_LIMIT_SINGLE_PH	**High frequency ACLL compensation setting for single phase operation with load-line.** LPF_LIMIT_SINGLE_PH = 30mV + [7:4] × 10mV For example, [3:0] = 0000, LPF_SINGLE_MUTI_PH = 30mV, [3:0] = 0011, LPF_SINGLE _MUTI_PH = 60mV, [3:0] = 1111, LPF_SINGLE _MUTI_PH = 180mV.
0x6A	[7:5]	FIXED&ABS_QR_WD	**Setting width of Fixed-QR and ABS_QR for multi-phase operation.** [7:5] = 000: 0.50 × TON, [7:5] = 100: 1.50 × TON, [7:5] = 001: 0.75 × TON, [7:5] = 101: 1.75 × TON, [7:5] = 010: 1.00 × TON, [7:5] = 110: 2.00 × TON, [7:5] = 011: 1.25 × TON, [7:5] = 111: 2.25 × TON.
	[4:0]	QR_TH	**Setting QR triggering level for multi-phase operation with load-line.** QR_TH = 240mV + [4:0] × 80mV For example, [4:0] = 00000: QR_TH = 240mV, [4:0] = 00001: QR_TH = 320mV, [4:0] = 01000: QR_TH = 880mV, [4:0] = 01111: QR_TH = 1440mV, [4:0] = 11111: Disable.

Register Address	Bits	Register Name	Description
0x6B	[7:5]	FIXED_QR_WD_1PH	**Setting width of Fixed-QR with single phase operation.** [7:5] = 000: 0.50 × TON, [7:5] = 100: 1.50 × TON, [7:5] = 001: 0.75 × TON, [7:5] = 101: 1.75 × TON, [7:5] = 010: 1.00 × TON, [7:5] = 110: 2.00 × TON, [7:5] = 011: 1.25 × TON, [7:5] = 111: 2.25 × TON.
	[4:0]	QR_TH_1PH	**Setting QR triggering level with single phase operation.** QR_TH_1PH = 40mV + [4:0] × 40mV For example, [4:0] = 00000: QR_TH_1PH = 40mV, [4:0] = 00001: QR_TH_1PH = 80mV, [4:0] = 01000: QR_TH_1PH = 360mV, [4:0] = 01111: QR_TH_1PH = 640mV, [4:0] = 11111: Disable.
0x6C	[7:5]	AR_TH_1PH	**Setting adaptive ramp threshold with single phase operation.** [7:5] = 000: 175mV [7:5] = 100: 275mV [7:5] = 001: 150mV [7:5] = 101: 225mV [7:5] = 010: 125mV [7:5] = 110: 200mV [7:5] = 011: Disable [7:5] = 111: Disable
	[4]	EN_EXTD_TON	**Enable TON Extend function.** [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	EXTD_TON_TH	**Setting the threshold to extend TON.** [3:2] = 00: 150mV, [3:2] = 01: 200mV, [3:2] = 10: 250mV, [3:2] = 11: 300mV.
	[1:0]	EXTD_WD_MAX	**Extend max TON setting.** [1:0] = 00: 1.625 × TON, [1:0] = 01: 1.500 × TON, [1:0] = 10: 1.375 × TON, [1:0] = 11: 1.250 × TON.
0x6D	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 09h (Default). All other combinations are not defined.
0x6E	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 00h (Default). All other combinations are not defined.
0x6F	[7:0]	RESERVED	Reserved bit(s). [7:0] = 8Ah (Default). All other combinations are not defined.
0x70	[7:6]	MIN_TOFF	**PWM minimum off-time setting.** [7:6] = 00: 300ns, [7:6] = 01: 200ns, [7:6] = 10: 120ns, [7:6] = 11: 50ns.
	[5]	QR_SEL	**Select QR type with multi-phase operation and load-line.** [5] = 0: Fixed-QR, [5] = 1: Adaptive-QR.
	[4]	QR_SEL_1PH	**Select QR type with multi-phase operation and load-line.** [4] = 0: Fixed-QR, [4] = 1: Adaptive-QR.
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 1000 (Default). All other combinations are not defined.

Register Address	Bits	Register Name	Description
0x71	[7]	EAGM_GAIN	**Setting transconductance gain of error amplifier.** [7] = 0: EAGM_GAIN = 2/3 [7] = 1: EAGM_GAIN = 1
	[6:4]	SLL_RATIO	**Short-term voltage target ratio during AC transient.** Short-term voltage target = VID − ΔIcc × RLL × SLL_RATIO [6:4] = 000: 100%, [6:4] = 100: 75%, [6:4] = 001: 95%, [6:4] = 101: 65%, [6:4] = 010: 90%, [6:4] = 110: 55%, [6:4] = 011: 85%, [6:4] = 111: 50%.
	[3:2]	RESERVED	**Reserved bit(s).** [3:2] = 00 (Default). All other combinations are not defined.
	[1]	TSEN_SEL	**Temperature source selection**. [1] = 0: External NTC thermistor (NTC is 100kΩ/Beta = 4250), [1] = 1: Integrated power stage temperature sensor. V_{TSEN} voltage represents temperature information at 8mV/°C + 0.6V.
	[0]	RESERVED	**Reserved bit(s).** [0] = 0 (Default). All other combinations are not defined.
0x72	[7]	RESERVED	**Reserved bit(s).** [7] = 0 (Default). All other combinations are not defined.
	[6]	QR_TRIGGER_SEL	**Setting trigger mechanism of QR.** [6] = 0: Absolute (ABS_QR) with zero load-line, [6] = 1: Differential (AQR & Fixed-QR) with load-line.
	[5:3]	ABS_OVS_TH	**Absolutely Overshoot threshold setting with zero load-line.** [5:3] = 000: Disabled, [5:3] = 100: 35mV, [5:3] = 001: 20mV, [5:3] = 101: 40mV, [5:3] = 010: 25mV, [5:3] = 110: 45mV, [5:3] = 011: 30mV, [5:3] = 111: 50mV.
	[2:0]	ABS_QR_TH	**Absolutely QR threshold setting with zero load-line.** [2:0] = 000: Disabled, [2:0] = 100: 35mV, [2:0] = 001: 20mV, [2:0] = 101: 40mV, [2:0] = 010: 25mV, [2:0] = 110: 45mV, [2:0] = 011: 30mV, [2:0] = 111: 50mV
0x80	[7:0]	SPM_HYS_2PH	**Set Smart Phase Management (SPM) current hysteresis with 2-phase down to 1-phase when EN_PSI_12[1] = 1b.** 1LSB = I_OUT_SCALE/192A When I_OUT_SCALE = Scale 2, LSB = 0.333A, [7:0] = 00h: SPM_HYS = 0A, [7:0] = 12h: SPM_HYS = 5.994A, [7:0] = C0h: SPM_HYS = 63.9375A.
0x83	[7:0]	SPM_TH_2PH	**Set Smart Phase Management (SPM) current threshold with 1-phase up to 2-phase when EN_PSI_12[1] = 1b.** Please refer to SPM_HYS_2PH_B for detailed description.
0x8A	[7:0]	IOUT_CAL_OFFSET	**IOUT telemetry offset** [7]: sign bit, as part of two's complement, [6:0]: 1LSB = I_OUT_SCALE/1023 A For example, [7:0] = 00h: IOUT_CAL_OFFSET = 0, [7:0] = 01h: IOUT_CAL_OFFSET = +1 LSB, [7:0] = 7Fh: IOUT_CAL_OFFSET = +127 LSB, [7:0] = FFh: IOUT_CAL_OFFSET = -1 LSB, [7:0] = 80h: IOUT_CAL_OFFSET = -128 LSB,

Register Address	Bits	Register Name	Description
0x8B	[7:0]	IOUT_CAL_GAIN	**IOUT telemetry gain** IOUT telemetry = $IMON_{ADC}$ × IOUT_CAL_GAIN + IOUT_CAL_OFFSET [7:0] = 00h: IOUT_CAL_GAIN = 75%, [7:0] = 80h: IOUT_CAL_GAIN = 100%, [7:0] = FFh: IOUT_CAL_GAIN = 124.8%.
0x90	[7:5]	SVI3_20h_DECAY_CONDITIONS	Please refer to SVI3 specification.
	[4]	SVI3_20h_DOWN_SLEW_RATE	
	[3:0]	SVI3_20h_UP_SLEW_RATE	**Slew rate for positive VID change.** SVI3 register UP_SLEW_RATE_20h[3:0]. Slew rate = 90h[3:0] x 2.5 + 2.5 mV/μs
0x91	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 0Ah (Default). All other combinations are not defined.
0x92	[7:0]	SVI3_22h_VOUT_OFFSET	**Voltage offset applied to VID, VID_MIN, VID_MAX, OVP_THRESH and UVP_THRESH.** SVI3 register VOUT_OFFSET_20h[7:0]. [7:0] = 00h: Disabled (no offset) Offset = 92h[7:0] x 20 - 500mV
0x93	[7:0]	SVI3_23h_VID_MAX	Please refer to SVI3 specification.
0x94	[7:0]	SVI3_24h_VID_MIN	Please refer to SVI3 specification.
0x95	[7:0]	SVI3_25h_TEN_BIT_TEL_EN	Please refer to SVI3 specification.
0x96	[7:0]	SVI3_26h_SIXTEEN_BIT_TEL_EN	Please refer to SVI3 specification.
0x97	[7:0]	SVI3_27h_OCP_THRESH	**Overcurrent protection threshold level.** SVI3 register OCP_THRESH_20h[7:0]. [7:0] = 00h: Disabled (no OCP protection) OCP Threshold = 97h[7:0] x 4 x MAX_CURRENT/512 A Note: MAX_CURRENT = 3FFh of selected current scale.
0x98	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 5Ch (Default). All other combinations are not defined.
0x99	[7:3]	RESERVED	**Reserved bit(s).** [7:3] = 00110 (Default). All other combinations are not defined.
	[2:0]	SVI3_29h_OCP_FAULT_DELAY	**Continuous time that current must exceed OCP_THRESH before triggering fault.** SVI3 register OCP_FAULT_DELAY_29h[2:0]. [2:0] = 000: Instantaneous fault Fault delay = 99h[2:0] x 5 μs.
0x9A	[7:0]	SVI3_2Ah_VRHOT_THRESH	Please refer to SVI3 specification.
0x9B	[7:0]	SVI3_2Bh_OTP_THRESH	Please refer to SVI3 specification.
0x9C	[7]	SVI3_2Ch_OVP_REF	Please refer to SVI3 specification.
	[6:4]	SVI3_2Ch OVP_DELTA	
	[3]	SVI3_2Ch UVP_REF	
	[2:0]	SVI3_2Ch UVP_DELTA	
0x9D	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 11h (Default). All other combinations are not defined.

Table 3. Functions that Do Not Support On-line Tuning

Register Address	Function	Support On-line Tuning
60h[7:4]	VID_DEFAULT_VOLTAGE	No
64h[6:4]	SSOCP_RATIO	No
64h[2:0]	I_OUT_SCALE	No
65h[3]	EN_0LL	No
65h[2:0]	AI_GAIN	No
71h[7]	EAGM_GAIN	No
71h[1]	TSEN_SEL	No
90h[3:0]	UP_SLEW_RATE	No
92h[7:0]	SVI3_22h_VOUT_OFFSET	No
97h[7:0]	SVI3_27h_OCP_THRESH	No
99h[2:0]	SVI3_29h_OCP_FAULT_DELAY	No

Table 4. SVI3 Registers for SVI3 Protocol

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
01h	[7:0]	SVI3_VERSION	R	01h	Rev. 1
02h	[7:5]	TYPE_ID	R	001b	Type 2
	[4:0]	MGF_ID	R	00100b	04h = Richtek
03h	[7:0]	MODEL_ID	R	00h	
04h	[7:0]	TEN_BIT_TEL_AVAIL	R	07h	Temp 1, Output voltage and Output current of 10-bit telemetry are available.
05h	[7:0]	SIXTEEN_BIT_TEL_AVAIL	R	00h	Reserved
06h	[7]	CRC_ENABLED	R	1b	CRC is enabled
	[4:2]	PSI	R	000b	PSI0. Indicates the PSI state of the target.
	[0]	VID[8]	R	Platform	Indicates the MSB of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
07h	[7:0]	VID[7:0]	R	Platform	Indicates the 8 LSBs of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
08h	[5:4]	DEFAULT_SLEW_RATE	R	Platform	NVM configurable, based on platform
08h	[3:0]	VID_DEFAULT_VOLTAGE	R	Platform	NVM configurable, based on platform
09h	[7:6]	V_IN_SCALE	R	00b	Not supported
	[5:3]	I_OUT_SCALE	R	Platform	NVM configurable, based on platform
	[2:0]	I_IN_SCALE	R	Platform	Not supported
0Ah	[7:0]	MAX_VOUT_SUPPORTED	R	8Ch	MAX_VOUT_SUPPORTED = 2.4V
0Bh	[7:0]	MIN_VOUT_SUPPORTED	R	32h	MIN_VOUT_SUPPORTED = 0.5V
10h	[7:0]	FAULT_STATUS	R	Current status	
11h	[7:0]	NACK_STATUS	R	Current status	
20h	[7:5]	DECAY_CONDITIONS	R/W	000b	Down voltage decay disabled
20h	[4]	DOWN_SLEW_RATE	R/W	0b	Negative slew rate = positive slew rate
20h	[3:0]	UP_SLEW_RATE	R/W	Platform	Copied from DEFAULT_SLEW_RATE
21h	[4:0]	LL_ADJUST	R/W	01010b	Not supported
22h	[7:0]	VOUT_OFFSET	R/W	00h	No offset
23h	[7:0]	VID_MAX	R/W	00h	Disabled
24h	[7:0]	VID_MIN	R/W	00h	Disabled
25h	[7:0]	TEN_BIT_TEL_EN	R/W	00h	Disabled
26h	[7:0]	SIXTEEN_BIT_TEL_EN	R/W	00h	Reserved
27h	[7:0]	OCP_THRESH	R/W	Platform	NVM configurable, based on platform
28h	[7:0]	OCP_WARN_THRESH	R/W	Platform	Not supported
29h	[7:3]	OCP_WARN_MIN_PULSE	R/W	Platform	Not supported
29h	[2:0]	OCP_FAULT_DELAY	R/W	Platform	NVM configurable, based on platform

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
2Ah	[7:0]	VRHOT_THRESH	R/W	8Ch	100°C
2Bh	[7:0]	OTP_THRESH	R/W	A5h	125°C
2Ch	[7]	OVP_REF	R/W	0b	VID
2Ch	[6:4]	OVP_DELTA	R/W	011b	400mV
2Ch	[3]	UVP_REF	R/W	0b	VID
2Ch	[2:0]	UVP_DELTA	R/W	011b	400mV
40h	[7:0]	DEBUG_ENABLED	R/W	00h	
41h	[7:0]	DEBUG_TEMP1_OVERRIDE	R/W	00h	
42h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
43h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
44h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
45h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
46h	[2:0]	DEBUG_OUTPUT_OVERRIDE	R/W	000b	
50h	[7:0]	GEN_PURPOSE_0	R/W	00b	
51h	[7:0]	GEN_PURPOSE_1	R/W	00b	
52h	[7:0]	GEN_PURPOSE_2	R/W	00b	
53h	[7:0]	GEN_PURPOSE_3	R/W	00b	
54h	[7:0]	GEN_PURPOSE_4	R/W	00b	
55h	[7:0]	GEN_PURPOSE_5	R/W	00b	
56h	[7:0]	GEN_PURPOSE_6	R/W	00b	
57h	[7:0]	GEN_PURPOSE_7	R/W	00b	

Table 5. SVI3 Type 2 Target VID Table

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
000000000	000	OFF	000100000	020	0.810	001000000	040	1.130	001100000	060	1.450
000000001	001	0.500	000100001	021	0.820	001000001	041	1.140	001100001	061	1.460
000000010	002	0.510	000100010	022	0.830	001000010	042	1.150	001100010	062	1.470
000000011	003	0.520	000100011	023	0.840	001000011	043	1.160	001100011	063	1.480
000000100	004	0.530	000100100	024	0.850	001000100	044	1.170	001100100	064	1.490
000000101	005	0.540	000100101	025	0.860	001000101	045	1.180	001100101	065	1.500
000000110	006	0.550	000100110	026	0.870	001000110	046	1.190	001100110	066	1.510
000000111	007	0.560	000100111	027	0.880	001000111	047	1.200	001100111	067	1.520
000001000	008	0.570	000101000	028	0.890	001001000	048	1.210	001101000	068	1.530
000001001	009	0.580	000101001	029	0.900	001001001	049	1.220	001101001	069	1.540
000001010	00A	0.590	000101010	02A	0.910	001001010	04A	1.230	001101010	06A	1.550
000001011	00B	0.600	000101011	02B	0.920	001001011	04B	1.240	001101011	06B	1.560
000001100	00C	0.610	000101100	02C	0.930	001001100	04C	1.250	001101100	06C	1.570
000001101	00D	0.620	000101101	02D	0.940	001001101	04D	1.260	001101101	06D	1.580
000001110	00E	0.630	000101110	02E	0.950	001001110	04E	1.270	001101110	06E	1.590
000001111	00F	0.640	000101111	02F	0.960	001001111	04F	1.280	001101111	06F	1.600
000010000	010	0.650	000110000	030	0.970	001010000	050	1.290	001110000	070	1.610
000010001	011	0.660	000110001	031	0.980	001010001	051	1.300	001110001	071	1.620
000010010	012	0.670	000110010	032	0.990	001010010	052	1.310	001110010	072	1.630
000010011	013	0.680	000110011	033	1.000	001010011	053	1.320	001110011	073	1.640
000010100	014	0.690	000110100	034	1.010	001010100	054	1.330	001110100	074	1.650
000010101	015	0.700	000110101	035	1.020	001010101	055	1.340	001110101	075	1.660
000010110	016	0.710	000110110	036	1.030	001010110	056	1.350	001110110	076	1.670
000010111	017	0.720	000110111	037	1.040	001010111	057	1.360	001110111	077	1.680
000011000	018	0.730	000111000	038	1.050	001011000	058	1.370	001111000	078	1.690
000011001	019	0.740	000111001	039	1.060	001011001	059	1.380	001111001	079	1.700
000011010	01A	0.750	000111010	03A	1.070	001011010	05A	1.390	001111010	07A	1.710
000011011	01B	0.760	000111011	03B	1.080	001011011	05B	1.400	001111011	07B	1.720
000011100	01C	0.770	000111100	03C	1.090	001011100	05C	1.410	001111100	07C	1.730
000011101	01D	0.780	000111101	03D	1.100	001011101	05D	1.420	001111101	07D	1.740
000011110	01E	0.790	000111110	03E	1.110	001011110	05E	1.430	001111110	07E	1.750
000011111	01F	0.800	000111111	03F	1.120	001011111	05F	1.440	001111111	07F	1.760

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SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
010000000	080	1.770	010100000	0A0	2.090	011000000	0C0	2.410	011100000	0E0	2.730
010000001	081	1.780	010100001	0A1	2.100	011000001	0C1	2.420	011100001	0E1	2.740
010000010	082	1.790	010100010	0A2	2.110	011000010	0C2	2.430	011100010	0E2	2.750
010000011	083	1.800	010100011	0A3	2.120	011000011	0C3	2.440	011100011	0E3	2.760
010000100	084	1.810	010100100	0A4	2.130	011000100	0C4	2.450	011100100	0E4	2.770
010000101	085	1.820	010100101	0A5	2.140	011000101	0C5	2.460	011100101	0E5	2.780
010000110	086	1.830	010100110	0A6	2.150	011000110	0C6	2.470	011100110	0E6	2.790
010000111	087	1.840	010100111	0A7	2.160	011000111	0C7	2.480	011100111	0E7	2.800
010001000	088	1.850	010101000	0A8	2.170	011001000	0C8	2.490	011101000	0E8	2.810
010001001	089	1.860	010101001	0A9	2.180	011001001	0C9	2.500	011101001	0E9	2.820
010001010	08A	1.870	010101010	0AA	2.190	011001010	0CA	2.510	011101010	0EA	2.830
010001011	08B	1.880	010101011	0AB	2.200	011001011	0CB	2.520	011101011	0EB	2.840
010001100	08C	1.890	010101100	0AC	2.210	011001100	0CC	2.530	011101100	0EC	2.850
010001101	08D	1.900	010101101	0AD	2.220	011001101	0CD	2.540	011101101	0ED	2.860
010001110	08E	1.910	010101110	0AE	2.230	011001110	0CE	2.550	011101110	0EE	2.870
010001111	08F	1.920	010101111	0AF	2.240	011001111	0CF	2.560	011101111	0EF	2.880
010010000	090	1.930	010110000	0B0	2.250	011010000	0D0	2.570	011110000	0F0	2.890
010010001	091	1.940	010110001	0B1	2.260	011010001	0D1	2.580	011110001	0F1	2.900
010010010	092	1.950	010110010	0B2	2.270	011010010	0D2	2.590	011110010	0F2	2.910
010010011	093	1.960	010110011	0B3	2.280	011010011	0D3	2.600	011110011	0F3	2.920
010010100	094	1.970	010110100	0B4	2.290	011010100	0D4	2.610	011110100	0F4	2.930
010010101	095	1.980	010110101	0B5	2.300	011010101	0D5	2.620	011110101	0F5	2.940
010010110	096	1.990	010110110	0B6	2.310	011010110	0D6	2.630	011110110	0F6	2.950
010010111	097	2.000	010110111	0B7	2.320	011010111	0D7	2.640	011110111	0F7	2.960
010011000	098	2.010	010111000	0B8	2.330	011011000	0D8	2.650	011111000	0F8	2.970
010011001	099	2.020	010111001	0B9	2.340	011011001	0D9	2.660	011111001	0F9	2.980
010011010	09A	2.030	010111010	0BA	2.350	011011010	0DA	2.670	011111010	0FA	2.990
010011011	09B	2.040	010111011	0BB	2.360	011011011	0DB	2.680	011111011	0FB	3.000
010011100	09C	2.050	010111100	0BC	2.370	011011100	0DC	2.690	011111100	0FC	3.010
010011101	09D	2.060	010111101	0BD	2.380	011011101	0DD	2.700	011111101	0FD	3.020
010011110	09E	2.070	010111110	0BE	2.390	011011110	0DE	2.710	011111110	0FE	3.030
010011111	09F	2.080	010111111	0BF	2.400	011011111	0DF	2.720	011111111	0FF	3.040

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SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
100000000	100	3.050	100100000	120	3.370	101000000	140	3.690	101100000	160	4.010
100000001	101	3.060	100100001	121	3.380	101000001	141	3.700	101100001	161	4.020
100000010	102	3.070	100100010	122	3.390	101000010	142	3.710	101100010	162	4.030
100000011	103	3.080	100100011	123	3.400	101000011	143	3.720	101100011	163	4.040
100000100	104	3.090	100100100	124	3.410	101000100	144	3.730	101100100	164	4.050
100000101	105	3.100	100100101	125	3.420	101000101	145	3.740	101100101	165	4.060
100000110	106	3.110	100100110	126	3.430	101000110	146	3.750	101100110	166	4.070
100000111	107	3.120	100100111	127	3.440	101000111	147	3.760	101100111	167	4.080
100001000	108	3.130	100101000	128	3.450	101001000	148	3.770	101101000	168	4.090
100001001	109	3.140	100101001	129	3.460	101001001	149	3.780	101101001	169	4.100
100001010	10A	3.150	100101010	12A	3.470	101001010	14A	3.790	101101010	16A	4.110
100001011	10B	3.160	100101011	12B	3.480	101001011	14B	3.800	101101011	16B	4.120
100001100	10C	3.170	100101100	12C	3.490	101001100	14C	3.810	101101100	16C	4.130
100001101	10D	3.180	100101101	12D	3.500	101001101	14D	3.820	101101101	16D	4.140
100001110	10E	3.190	100101110	12E	3.510	101001110	14E	3.830	101101110	16E	4.150
100001111	10F	3.200	100101111	12F	3.520	101001111	14F	3.840	101101111	16F	4.160
100010000	110	3.210	100110000	130	3.530	101010000	150	3.850	101110000	170	4.170
100010001	111	3.220	100110001	131	3.540	101010001	151	3.860	101110001	171	4.180
100010010	112	3.230	100110010	132	3.550	101010010	152	3.870	101110010	172	4.190
100010011	113	3.240	100110011	133	3.560	101010011	153	3.880	101110011	173	4.200
100010100	114	3.250	100110100	134	3.570	101010100	154	3.890	101110100	174	4.210
100010101	115	3.260	100110101	135	3.580	101010101	155	3.900	101110101	175	4.220
100010110	116	3.270	100110110	136	3.590	101010110	156	3.910	101110110	176	4.230
100010111	117	3.280	100110111	137	3.600	101010111	157	3.920	101110111	177	4.240
100011000	118	3.290	100111000	138	3.610	101011000	158	3.930	101111000	178	4.250
100011001	119	3.300	100111001	139	3.620	101011001	159	3.940	101111001	179	4.260
100011010	11A	3.310	100111010	13A	3.630	101011010	15A	3.950	101111010	17A	4.270
100011011	11B	3.320	100111011	13B	3.640	101011011	15B	3.960	101111011	17B	4.280
100011100	11C	3.330	100111100	13C	3.650	101011100	15C	3.970	101111100	17C	4.290
100011101	11D	3.340	100111101	13D	3.660	101011101	15D	3.980	101111101	17D	4.300
100011110	11E	3.350	100111110	13E	3.670	101011110	15E	3.990	101111110	17E	4.310
100011111	11F	3.360	100111111	13F	3.680	101011111	15F	4.000	101111111	17F	4.320

Continued

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
110000000	180	4.330	110100000	1A0	4.650	111000000	1C0	4.970	111100000	1E0	5.290
110000001	181	4.340	110100001	1A1	4.660	111000001	1C1	4.980	111100001	1E1	5.300
110000010	182	4.350	110100010	1A2	4.670	111000010	1C2	4.990	111100010	1E2	5.310
110000011	183	4.360	110100011	1A3	4.680	111000011	1C3	5.000	111100011	1E3	5.320
110000100	184	4.370	110100100	1A4	4.690	111000100	1C4	5.010	111100100	1E4	5.330
110000101	185	4.380	110100101	1A5	4.700	111000101	1C5	5.020	111100101	1E5	5.340
110000110	186	4.390	110100110	1A6	4.710	111000110	1C6	5.030	111100110	1E6	5.350
110000111	187	4.400	110100111	1A7	4.720	111000111	1C7	5.040	111100111	1E7	5.360
110001000	188	4.410	110101000	1A8	4.730	111001000	1C8	5.050	111101000	1E8	5.370
110001001	189	4.420	110101001	1A9	4.740	111001001	1C9	5.060	111101001	1E9	5.380
110001010	18A	4.430	110101010	1AA	4.750	111001010	1CA	5.070	111101010	1EA	5.390
110001011	18B	4.440	110101011	1AB	4.760	111001011	1CB	5.080	111101011	1EB	5.400
110001100	18C	4.450	110101100	1AC	4.770	111001100	1CC	5.090	111101100	1EC	5.410
110001101	18D	4.460	110101101	1AD	4.780	111001101	1CD	5.100	111101101	1ED	5.420
110001110	18E	4.470	110101110	1AE	4.790	111001110	1CE	5.110	111101110	1EE	5.430
110001111	18F	4.480	110101111	1AF	4.800	111001111	1CF	5.120	111101111	1EF	5.440
110010000	190	4.490	110110000	1B0	4.810	111010000	1D0	5.130	111110000	1F0	5.450
110010001	191	4.500	110110001	1B1	4.820	111010001	1D1	5.140	111110001	1F1	5.460
110010010	192	4.510	110110010	1B2	4.830	111010010	1D2	5.150	111110010	1F2	5.470
110010011	193	4.520	110110011	1B3	4.840	111010011	1D3	5.160	111110011	1F3	5.480
110010100	194	4.530	110110100	1B4	4.850	111010100	1D4	5.170	111110100	1F4	5.490
110010101	195	4.540	110110101	1B5	4.860	111010101	1D5	5.180	111110101	1F5	5.500
110010110	196	4.550	110110110	1B6	4.870	111010110	1D6	5.190	111110110	1F6	5.510
110010111	197	4.560	110110111	1B7	4.880	111010111	1D7	5.200	111110111	1F7	5.520
110011000	198	4.570	110111000	1B8	4.890	111011000	1D8	5.210	111111000	1F8	5.530
110011001	199	4.580	110111001	1B9	4.900	111011001	1D9	5.220	111111001	1F9	5.540
110011010	19A	4.590	110111010	1BA	4.910	111011010	1DA	5.230	111111010	1FA	5.550
110011011	19B	4.600	110111011	1BB	4.920	111011011	1DB	5.240	111111011	1FB	5.560
110011100	19C	4.610	110111100	1BC	4.930	111011100	1DC	5.250	111111100	1FC	5.570
110011101	19D	4.620	110111101	1BD	4.940	111011101	1DD	5.260	111111101	1FD	5.580
110011110	19E	4.630	110111110	1BE	4.950	111011110	1DE	5.270	111111110	1FE	5.590
110011111	19F	4.640	110111111	1BF	4.960	111011111	1DF	5.280	111111111	1FF	5.600

Thermal Monitoring and Indicator

The RT3672EE supports thermal monitoring by external NTC thermistor or integrated power stage temperature sensor, and it can be set by NVM registers TSEN_SEL_71h[1].

When external NTC thermistor is used for thermal monitoring, TSEN pin voltage can be represented as:

$$V_{TSEN} = 80\mu A \times (R_1 // R_{NTC} + R_2)$$

The NTC thermistor network for temperature sensing is shown in Figure 4. The NTC thermistor is recommended to be placed around the hottest component of the VR, i.e. MOSFET, and must be routed as differential pair on the same PCB layer.

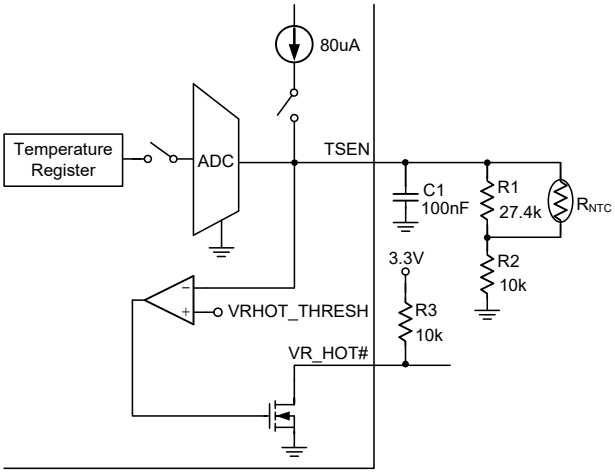


Figure 4. TSEN Network with NTC Thermistor

The RT3672EE supports the telemetry function for temperature. The device continually digitizes the sensed corresponding channel temperature with TSEN pin, and averages it to reduce measurement noise. Then the current value is stored in the TEMP_RPT (23h) register.

The resistance accuracy of TSEN network is recommended to be less than 1% error. The NTC thermistor is suggested to be 100kΩ with β = 4250 and with accuracy less than 1% error. The NCP15WF104F03RC NTC thermistor from Murata is recommended. When integrated power stage temperature sensor is used for thermal monitoring, the RT3672EE controller senses the temperature reported by TMON pin of integrated power stage. In this application, the relation between VTSEN voltage and the sensed temperature is:

$$\text{Temp.}\left(^{\circ}C\right) = \frac{V_{TSEN} - 0.6V}{8mV/^{\circ}C}$$

The sensed temperature can be read via SVI3 from the register READ_TEMPERATURE_1 (8Dh), and via I^2C from the register TEMP_RPT (23h). The update rate of temperature reporting register is 700μs and the averaging interval is 5.6ms.

Zero Load-line and AC-droop

The RT3672EE supports zero load-line applications by NVM register setting EN_0LL_65h[3], and builds in AC-droop feature. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current. The AC-droop can effectively suppress load transient ring-back and control overshoot in zero load-line application. Figure 5 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring-back ΔV2 due to electrical charge integrated in C area. Figure 6 shows the load transient condition with AC-droop control. When load transient occurs, the controller changes VID to short-term voltage target temporarily. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as:

Short-term Voltage Target =

$$VID - \Delta I_{CC} \times R_{LL} \times SLL\_RATIO$$

Whether zero load-line is enabled or disabled, the equation of R_{LL} is the same as load-line system. Zero load-line function can be set by NVM register EN_0LL_65h[3]. The detailed application is described in the Load-line Setting section. SLL_RATIO is a ratio of short-term voltage target during AC transient, and it can be set by NVM register SLL_RATIO_71h[6:4]. The short-term voltage target returns to VID slowly after a period of time. The short-term voltage target can prevent inductor current from exceeding loading current too much and the ring-back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

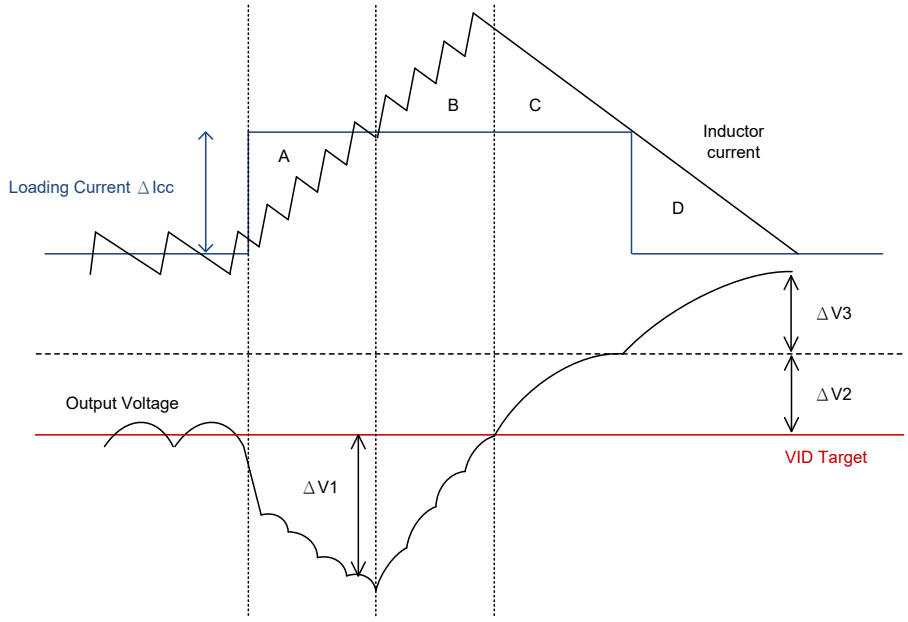


Figure 5. Zero Load-line without AC-droop Control

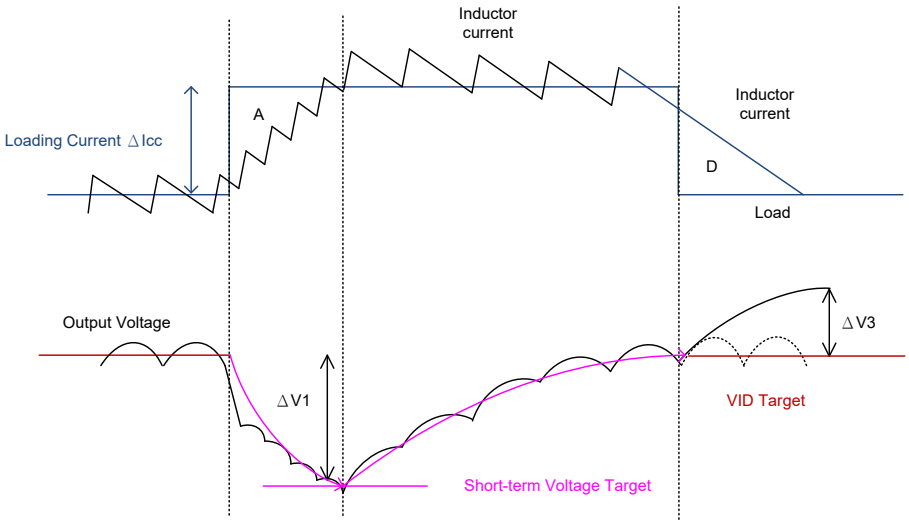


Figure 6. Zero Load-line with AC-droop Control

DCR Current Sense

To achieve higher efficiency, the RT3672EE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 7. An external low-pass filter R_{X1} (R_{X11}+R_{X12}) and C_X reconstruct the current signal. It is necessary to fine-tune R_{X1} (R_{X11}+R_{X12}) and C_X for transient performance and current telemetry. The time constant of R_{X1} x C_X should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}}$$

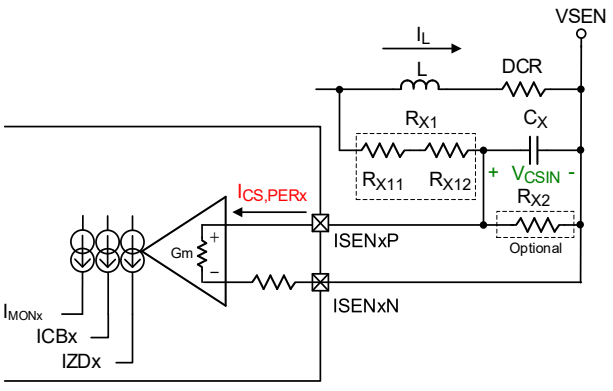


Figure 7. DCR Current Sensing Network of Inductor

Figure 8 shows the waveforms of output voltage according to the time constant of RC network. If R_{X1} x C_X = $\frac{L}{DCR}$, an ideal load transient waveform can be designed. If R_{X1} x C_X > $\frac{L}{DCR}$, VSEN waveform has a sluggish droop during load transient. If R_{X1} x C_X < $\frac{L}{DCR}$, VSEN waveform sags to create an undershoot that might fail the specification and can trigger overcurrent protections (OCP). It is strongly suggested to use two 0603 size resistors connected in series for R_{X1} (R_{X11}+R_{X12}) to enhance the output current telemetry accuracy, and both resistance of R_{X11} and R_{X12} must be the same. The capacitor C_X is suggested to be 0.1μF X7R/0603 to avoid capacitance de-rating at high frequency.

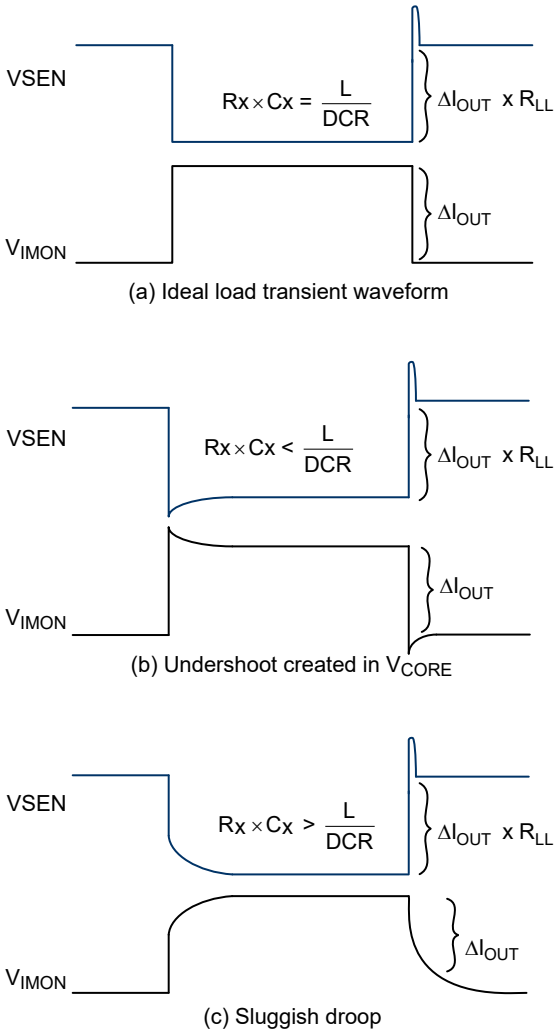


Figure 8. Effects of Different RC Time Constants

R_{X2} in Figure 7 is optional to prevent V_{CSIN} from exceeding the range of current sense amplifier. The time constant of (R_{X1} // R_{X2}) x C_X should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}} \times \frac{R_{X2}}{R_{X1} + R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero current detection. The mirrored current to IMONx pin is 1.25 time of $I_{CS,PER}$

$$I_{IMONx} = A_{MIRROR} \times I_{CS,PERx},\ A_{MIRROR} = 1.25$$

The current sense signal must be routed as differential pair from inductor to the controller on the same PCB layer. Proper differential routing of current sense signal will provide accurate current telemetry for current balance, load-line regulation and OCP.

The DCR value of inductor increases as the temperature of inductor increases, due to the positive temperature coefficient of the copper windings. To compensate the effect of DCR positive temperature coefficient, conventional current sense method requires an NTC thermistor for each phase current sensing. The RT3672EE adopts a patented total current sense method that requires only one NTC thermistor for thermal compensation. The NTC thermistor is designed within IMON resistor network on the IMON pin. It is suggested to place the NTC thermistor close to the inductor of phase 1.

The total DCR current sense method is shown in Figure 9. All phase current signals are mirrored to the IMON pin and converted into a voltage signal V_{IMON} by $R_{IMON,EQ}$. The VREF pin provides 0.6V voltage source (denoted as V_{VREF}) during normal operation. The relationship between V_{IMON} and inductor current I_{Lx} is:

$$V_{IMON} - V_{VREF} =$$

$$(I_{L1} + I_{L2}) \times \frac{DCR}{1000} \times A_{MIRROR} \times R_{IMON,EQ}$$

V_{IMON} − V_{VREF} is proportional to output current and is used for output current telemetry, load-line control and sum overcurrent protection. V_{IMON} − V_{VREF} is linearly mapped to NVM register I_OUT_SCALE_64h [2:0], which is user selectable. The $R_{IMON,EQ}$ should be designed according to maximum current of

I_OUT_SCALE. V_{IMON} − V_{VREF} is 0.4V while (I_{L1} + I_{L2}) = maximum current of I_OUT_SCALE.

For load-line control, V_{IMON} − V_{VREF} is scaled by NVM register AI_GAIN_65h[2:0]. The detailed application is described in the Load-line Setting section.

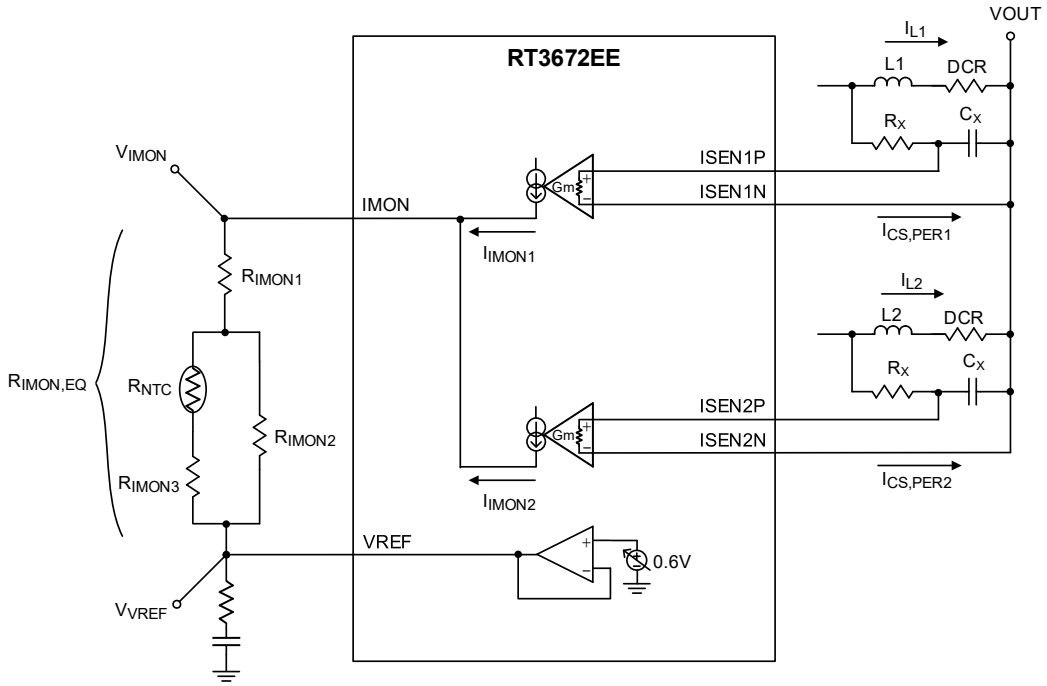


Figure 9. Total DCR Current Sensing

Load-line Setting (R_{LL})

The mechanism of load-line is that the output voltage decreases by an amount proportional to the loading current. The slope between output voltage and loading current is the load-line (R_{LL}) as shown in Figure 10. Figure 11 shows the circuit of voltage loop and current loop for the load-line control. The detailed equation is described as below:

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{CS}} \times \frac{R_{IMON,EQ}}{A_{EAGM}} \times \frac{A_i}{A_v} \times 2.5$$

A_i is the gain of current sense amplifier, and it can be set by NVM register AI_GAIN_65h[2:0]. A_{EAGM} is the transconductance ratio of ERROR AMP, and it can be set by NVM register EAGM_GAIN_71h[7]. A_V is the gain of voltage loop compensator, which equals to $\frac{R_{EA2}}{R_{EA1}}$, and it is suggested to be 2 to 4.5 for better transient response. Table 6 and 7 show NVM register setting of A_i and A_V.

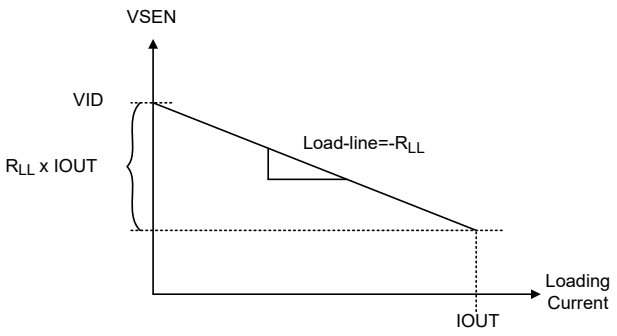


Figure 10. Load-line (Adaptive Voltage Positioning)

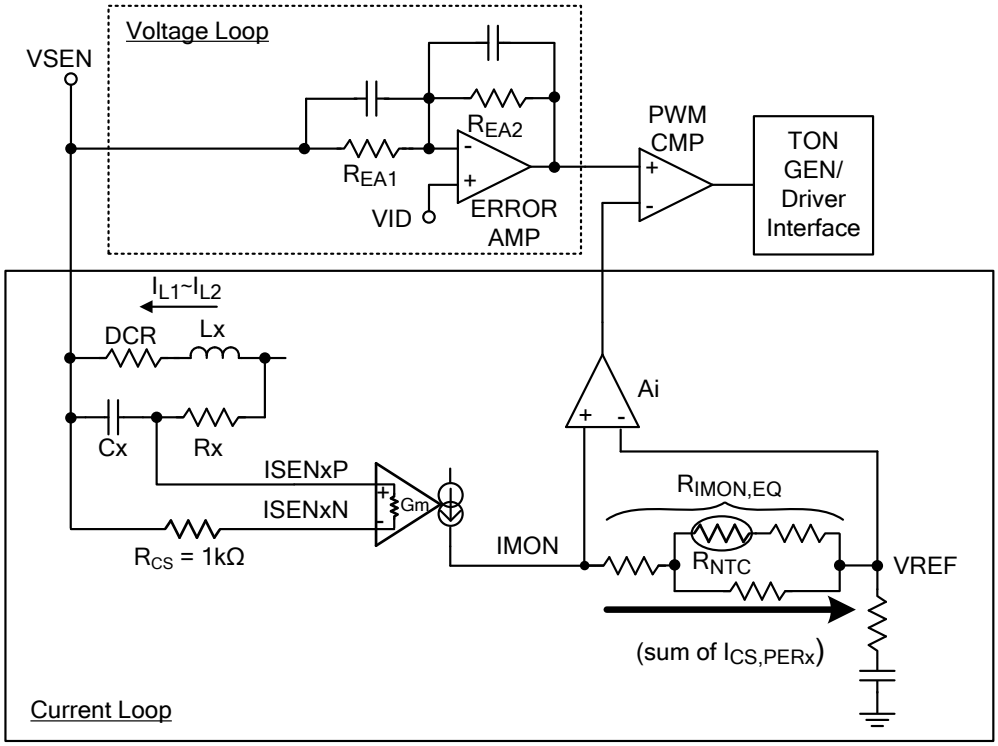


Figure 11. Voltage Loop and Current Loop for Load-line Control

Table 6. NVM Configuration of A_i

AI_GAIN_65h[2:0]	Current Sense Gain
000	0.25
001	0.5
010	0.75
011	1.00
100	0.125
101	0.375
110	0.625
111	0.875

Table 7. NVM Configuration of A_{EAGM}

EAGM_GAIN_71h[7]	A_{EAGM} Gain
0	2/3
1	1

Voltage On-the-Fly (VOTF) Compensation

During VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the VOTF slew rate and output capacitance as shown in the equation below. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. This extra voltage drop can be seen:

V_{Droop} = VOTF Slew Rate x Output Capacitance x R_{LL}

Where R_{LL} is the load-line slope, mΩ.

This is called droop effect. How the charging current affects VOTF transition is illustrated in Figure 12.

The RT3672EE provides VOTF compensation function as shown in Figure 13. During VOTF, an internal current I_{VOTF_LIFT} sinks from FB pin to generate VOTF compensation, I_{VOTF_LIFT} x R_{EA1}. For different scales of VOTF slew rate, I_{VOTF_LIFT} can be set by NVM register VOTF_LIFT_68h [4:0]. Compensating magnitude can be adjusted by R_{EA1}. When DAC output reaches the target, inductor current is still high and needs a period of time to settle down to the DC loading current. During the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, VOTF compensation can be less than VOTF Slew Rate x Output Capacitance x R_{LL} (De-rating of capacitance should be considered).

If the output capacitance is too large to be covered by VOTF compensation, adding extra resistor and capacitor in series from FB to GND can also provide similar effect. The ERROR AMP compensation (Resistance and capacitance network among VSEN, FB and COMP) network also affects VOTF behavior. The final setting should be based on actual measurement.

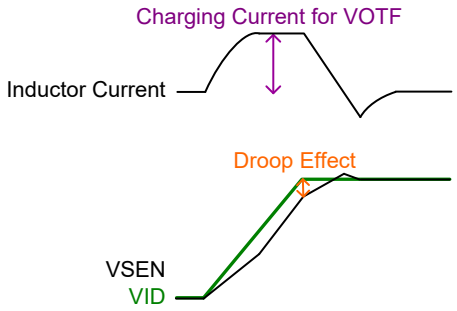


Figure 12. Droop Effect in VOTF Transition

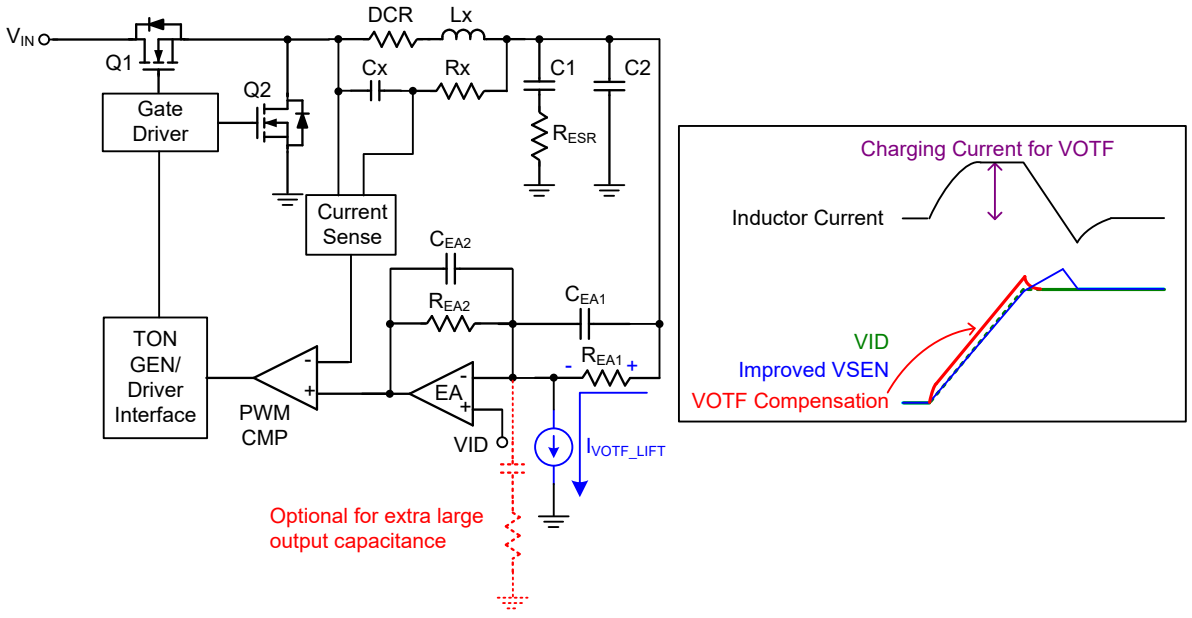


Figure 13. VOTF Compensation

Compensator Design

The compensator of the RT3672EE does not need a complex type III compensator to optimize control loop performance. It can adopt a simple type II compensator (single pole, single zero) in the G-NAVP™ topology to fine-tune ACLL performance. The single pole and single zero compensator is shown in Figure 14. For SVI3 transient specification, it is suggested to adjust compensator according to load transient ring-back level. Refer to the design tool for default compensator values.

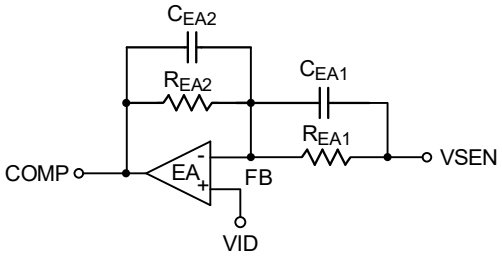


Figure 14. Type II Compensator

Differential Remote Sense

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PCB traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, VCC_SENSE and VSS_SENSE. The related connection is shown in Figure 15. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback. VSEN and RGND must be routed as differential pair all the way from controller to CPU socket without crossing any phase node, gate driver, VIN power delivery path and high speed signal. They should be well spaced on an internal signal layer between two monolithic ground planes.

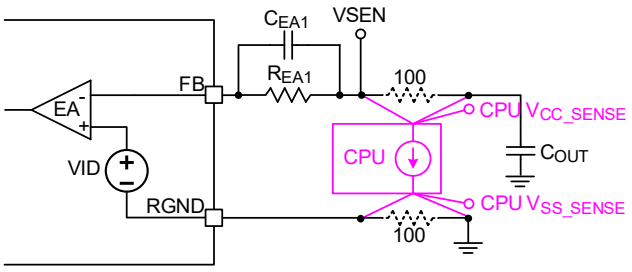


Figure 15. Remote Sensing Circuit

Switching Frequency

The G-NAVP™ (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive tON pulse (PWM) based on input voltage for better line regulation. The tON width is adaptive to VID voltage to achieve constant frequency. The constant switching frequency operation makes the thermal estimation easier. The RT3672EE provides a parameter setting of KTON to define tON width, and KTON can be set by NVM register KTON_67h[4:0]. Table 8 shows the KTON table for tON width setting. The equations of tON are listed as below:

$$VID>0.9V,\ t_{ON} = 2\mu \times \frac{VID}{K_{TON} \times VIN}$$

$$VID \leq 0.9V,\ t_{ON} = 2\mu \times \frac{0.9}{K_{TON} \times VIN}$$

Table 8. NVM Configuration of KTON_67h[4:0]

KTON_67h[4]	KTON
0	KTON = 0.3 + 67h[3:0] x 0.1
1	KTON = 1.2 + 67h[3:0] x 0.1

The switching frequency can be derived from tON as shown below. The power dissipation in the power stage and driver characteristics are considered.

$$Fsw = \frac{VID + \frac{I_{CC}}{N} \times (DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL})}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}}\right)\right] \times (t_{ON} - t_D + t_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times t_D}$$

VID: VID voltage

VIN: Input voltage

I_{CC}: Loading current

N: Total phase number

$R_{ONHS,max}$: Maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: Number of high-side MOSFETs

$R_{ONLS,max}$: Maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: Number of low-side MOSFETs.

t_D: Sum of the high-side MOSFET delay time and rising time

$t_{ON, VAR}$: On-time variation value

DCR: Inductor DCR

R_{LL}: Load-line setting (Ω)

Quick Response (AQR/Fixed-QR/ABS_QR)

The RT3672EE provides Absolutely Quick Response (ABS_QR) and Adaptive Quick Response (AQR)/Fixed Quick Response (Fixed QR) to optimize transient response for zero load-line and load-line system respectively. Table 9 and Table 10 summarize the settings of quick response.

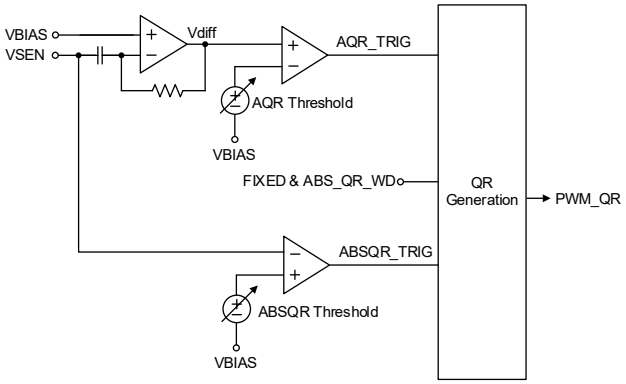


Figure 16. Mechanism of Quick Response

In zero load-line system, the RT3672EE provides Absolute Quick Response (ABS_QR) technique to optimize transient performance and can be set via QR_TRIGGER_SEL_72h [6] = 0b: Absolute. Since the output voltage does not change with loading current in zero load-line system, the RT3672EE detects the absolute value of output voltage drop. Figure 17 illustrates the ABS_QR mechanism. When the absolute value of output voltage drops below VID minus ABS_QR threshold, the controller will turn on all PWMs simultaneously until VSEN climbs up above the threshold. The QR threshold can be selected via NVM registers ABS_QR_TH_72h [2:0]. The QR on-time width can be selected via NVM registers of FIXED&ABS_QR_WD_6Ah [7:5]. Note that the threshold should be larger than output voltage ripple to avoid triggering ABS_QR mechanism in steady-state.

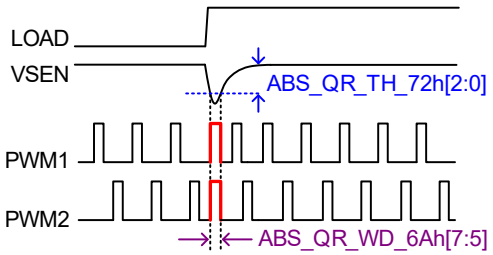


Figure 17. Absolutel Quick Response (ABS_QR) in No Load-line System (QR_TRIGGER_SEL_72h[6] = 0b: Differential)

In load-line system, ABS_QR is not applicable because output voltage decreases as the loadline current increases. Instead of ABS_QR, the RT3672EE provides Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR) to optimize transient performance.

Figure 18 and Figure 19 show the mechanisms and differences between AQR and Fixed QR. They can be set by NVM register QR_SEL_70h[5]. In the mechanism of AQR and Fixed-QR, the controller detects the falling slew rate of output voltage drop. When the slew rate of output voltage drop exceeds the QR threshold, the controller turns on all PWMs simultaneously until the output derivative drops below AQR threshold. Since loading requirement in PSI0 and PSI3 is different, the RT3672EE provides two settings of AQR/Fixed QR threshold QR_TH_6Ah[4:0] and QR_TH_1PH_6Bh[4:0], both can be selected via NVM registers. The t_{ON} width of AQR is adaptive to loading step current. The Fixed QR on-time width can be selected via NVM registers FIXED&ABS_QR_WD_6Ah [4:0] in PSI0 state and FIXED_QR_WD_1PH_6Bh [7:5] in PSI3 state. It should be noticed that the threshold for AQR and Fixed QR should be set larger than falling slew rate of output voltage ripple in the steady-state and the falling slew rate of overshoot to avoid false triggering. The following equation can initially decide the QR threshold of AQR and Fixed-QR:

$$\text{QR Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$

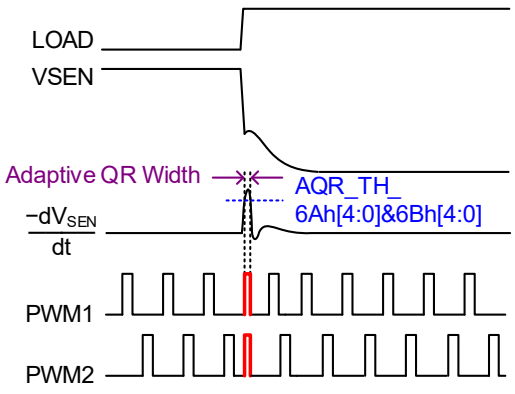


Figure 18. Adaptive Quick Response (AQR)
(QR_TRIGGER_SEL_72h[6] = 1b: Differential)

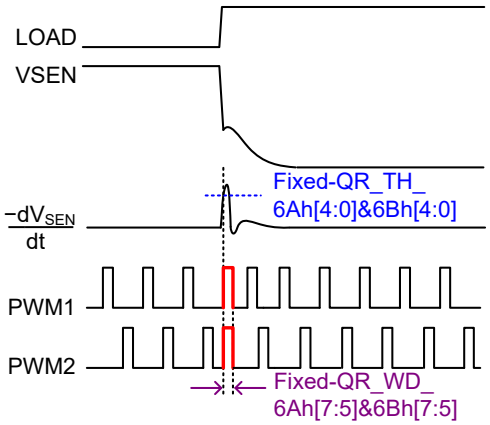


Figure 19. Fixed Quick Response (Fixed-QR)
(QR_TRIGGER_SEL_72h[6] = 1b: Differential)

Table 9. Quick Response in Load-line/No Load-line System

Quick Response	Z Load-line (EN_0LL_65h[3] = 1b: Enable)	Load-line (EN_0LL_65h[3] = 0b: Disabled)
Adaptive Quick Response (AQR)	Supported	Supported
Fixed Quick Response (Fixed-QR)	Supported	Supported
Absolutely Quick Response (ABS_QR)	Supported	No Supported

Table 10. Summary of Quick Response

QR Trigger Mechanism	Absolutel	Differential	
Trigger Mechanism	QR_TRIGGER_SEL_72h[6] = 0: Absolute(ABS_QR*)	QR_TRIGGER_SEL_72h[6] = 1: Differential(AQR & Fixed-QR)	
Type	QR_SEL_70h[5]	QR_SEL_70h[5]/QR_SEL_1PH_70h[4]	
	0: Fixed-QR	0: Fixed-QR	1: Adaptive-QR
Threshold	ABS_QR_TH_ 72h[2:0]	QR_TH_6Ah[4:0]/ QR_TH_1PH_6Bh[4:0]	
QR Width of Ton	FIXED&ABS_QR_ WD_6Ah[7:5]	FIXED&ABS_QR_ WD_6Ah[7:5]	Adaptive

* ABS_QR is only available with zero load-line system.

Absolute-Overshoot (ABS_OVS)/Anti-Overshoot (ANTI-OVS)

The RT3672EE provides Absolute-Overshoot (ABS_OVS) function and Anti-Overshoot (ANTI-OVS) function to suppress output voltage overshoot for no load-line and load-line system respectively.

In zero load-line system, the RT3672EE provides Absolute-Overshoot (ABS_OVS) function as shown in Figure 20. Since the output voltage does not change with loading current in zero load-line system, the RT3672EE detects the absolute value of output voltage overshoot. When output overshoot exceeds ABS_OVS threshold, the controller will force all PWMs in tri-state until zero current is detected or VSEN returns to normal level. The threshold of ABS_OVS can be selected via NVM registers ABSOVS_TH_72h[5:3].

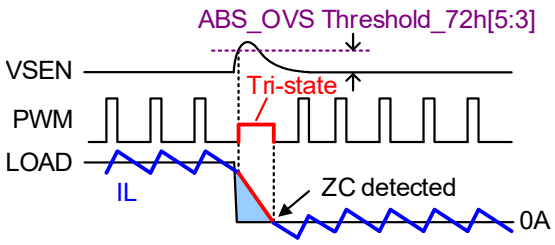


Figure 20. Absolute-Overshoot Function in No Load-Line System

In load-line system, the RT3672EE provides Anti-overshoot (ANTI-OVS) function to suppress output voltage overshoot. The controller detects the internal COMP signal which can vary with voltage loop compensation. The following equation can be used to initially decide the threshold of ANTI-OVS function:

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be based on actual Error AMP compensator design and measurement. When output overshoot exceeds the trigger level, the controller will force all PWMs in tri-state until zero current is detected or VSEN returns to normal level. The threshold of ANTI-OVS can be selected via NVM registers ANTI-OVS_68h[7:5].

Overshoot suppression is achieved by turning off both high-side and low-side switches, forcing the inductor current to flow through low-side body diode. The extra forward voltage can accelerate the inductor discharging slope and hence reduce overshoot significantly.

ACLL Performance Enhancement

In single phase configuration, the RT3672EE provides Adaptive Ramp (AR) function to suppress undershoot when load applied. The controller detects internal COMP signal and compares it with steady-state signal. When COMP signal variation exceeds a specified threshold, the controller will force to generate PWM earlier. The threshold of Adaptive Ramp (AR) function can be selected via NVM registers AR_TH_1PH_6Ch [7:5]. Figure 21 shows UDS behavior in single phase operation. Note that the threshold of AR should be large enough to avoid false triggering in steady-state. Since the internal COMP signal can vary with ERROR AMP compensator, the final setting should be based on actual Error AMP compensator design and measurement.

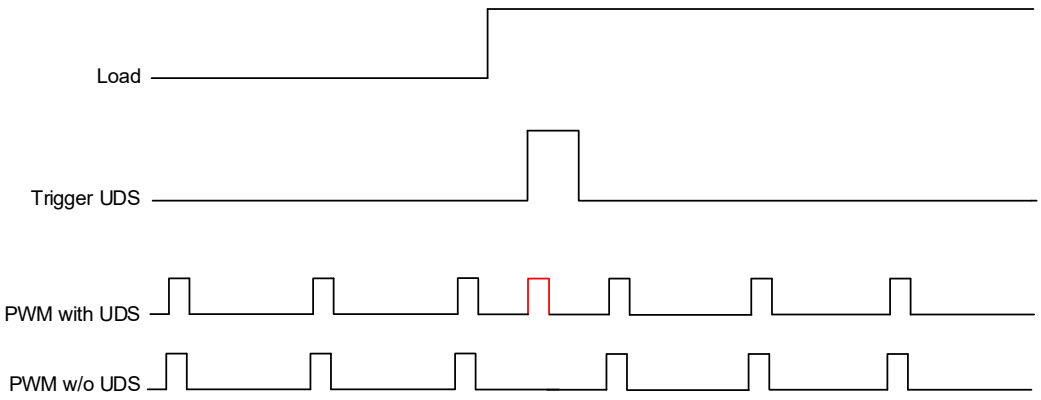


Figure 21. Adaptive Ramp (AR) Function in Single Phase

Smart Phase Management (SPM)

The RT3672EE provides Smart Phase Management (SPM) function to improve light load efficiency in 2-phase configuration. The SPM function can be enabled and disabled via I²C register EN_FORCE_SPM_12h[1]. As shown in Figure 22, the controller compares VIMON with current threshold SPM_TH_2PH to determine the number of operating phases. The threshold of SPM can be set via NVM register SPM_TH_2PH_83h[7:0]. There is no delay during phase adding. Figure 23 shows the hysteresis of SPM_TH and delay time exit during phase drop. The hysteresis of SPM_TH can be set via NVM register SPM_HYS_2PH_80h[7:0]. When VIMON is lower than (SPM_TH_2PH − SPM_HYS_2PH), the controller goes to single phase operation. When the inductor current is lower than zero current detector threshold, the controller automatically enters diode emulation mode (DEM). In addition to the output current comparison, the RT3672EE provides four events to operate in full phase immediately:

(a) During positive VOTF transitions,

(b) During negative VOTF transitions without decay mode,

(c) While the QR functions (AQR/Fixed-QR/ABS_QR) are triggered,

(d) I²C register EN_FORCE_PSI0_12h[0] = 1: Enable.

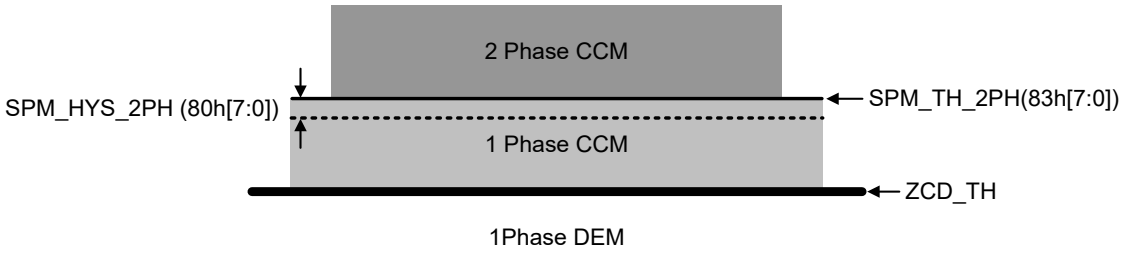


Figure 22. Smart Phase Management in 2-Phase

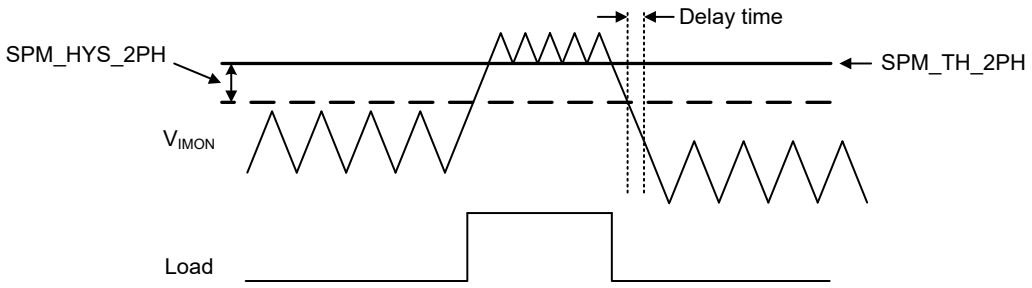


Figure 23. Phase Adding and Shedding

Telemetry for VOUT/IOUT/Temperature

The RT3672EE supports the telemetry function for VOUT/IOUT/Temperature.

For VOUT telemetry, the controller continually digitizes the sensed output voltage from differential voltage sense input (VSEN pin and RGND pin), and averages the data to reduce measurement noise. The current value is stored in the I²C register VOUT_RPT [9:0] = {VOUT_RPT_H_25h [1:0], VOUT_RPT_L_24h [7:0]}.

For IOUT telemetry, the controller continually senses and digitizes the corresponding per-phase currents, and averages the data to reduce the measurement noise. (VIMON−VVREF) is coded by 10-bit ADC and mapped to user selectable I_OUT_SCALE_64h[2:0]. The RT3672EE flexibly provides gain and offset calibrate function for IOUT telemetry, which can be set via NVM register IOUT_CAL_OFFSET_8Ah[7:0] and IOUT_CAL_GAIN_8Bh[7:0] to calibrate systematic errors related to board layout after PCB assembly. IOUT telemetry data can be read in I²C register IOUT_RPT[9:0] = {IOUT_RPT_H[1:0], IOUT_RPT_L[7:0]}.

For temperature telemetry, the device continually senses and digitizes the temperature by the TSEN pin,

and averages the data to reduce measurement noise. Temperature register is updated every 700μs and the averaging interval is 5.6ms. The filtered temperature can be read in the I²C register TEMP_RPT_23h[7:0].

Undervoltage Lockout (UVLO)

To ensure sufficient power supply for proper operation, the RT3672EE provides undervoltage lockout (UVLO) protection for VCC. The controller triggers VCC_UVLO protection if VCC drops below (VCC_POR_R-ΔVCC_POR_F_HYS). The controller will shut down, and PWMs are in tri-state to turn off both high-side and low-side MOSFETs.

Soft-start Overcurrent Protection (SSOCP)

The RT3672EE provides soft-start overcurrent protection (SSOCP) while output ramps up from 0V. Figure 24 illustrates the mechanism for SSOCP. When the inductor current exceeds the threshold of SSOCP within 5μs, the controller will turn off both the high-side and low-side MOSFETs immediately, and assert I²C register I2C_FAULT_STATUS_1Ah[6]. The SSOCP threshold can be set via NVM register SSOCP_RATIO_64h[6:4]. To avoid false triggering, the SSOCP threshold is recommended to be higher than the charging current that approximates to the product of output capacitance and DEFAULT_SLEW_RATE. The SSOCP threshold is defined as:

$$SSOCP\_TH = I\_OUT\_SCALE \times SSOCP\_RATIO$$

After SSOCP event is removed, the controller can be restarted, and the I2C_FAULT_STATUS_1Ah[6] can be cleared by toggling VCC power or PWREN pin.

Overcurrent Protection (OCP)

The RT3672EE supports Overcurrent Protection (OCP) detection. Figure 25 illustrates the mechanism for OCP. When the inductor current exceeds the threshold of OCP continuously with a period of OCP delay time, the controller will turn off both the high-side and low-side MOSFETs immediately, de-assert PWRGD, and assert I²C register I2C_FAULT_STATUS_1Ah[0]. The continuous time that current must exceed OCP_THRESH before triggering fault can be set via NVM register OCP_FAULT_DELAY_99h[2:0]. It is recommended that the OCP threshold should be set at the number of active phases multiplied by the current capability of MOSFET. The threshold of OCP can be set via NVM register OCP_THRESH_97h[7:0]. The OCP threshold level for PSIx is defined as:

$$I_{OCP\_PSI0,3} = OCP\_THRESH[7:0] \times \frac{4 \times I\_OUT\_SCALE}{512A} \times \frac{ACTIVE\_PH}{N}$$

where ACTIVE_PH = active number of phase, N = phase number in PSI0.

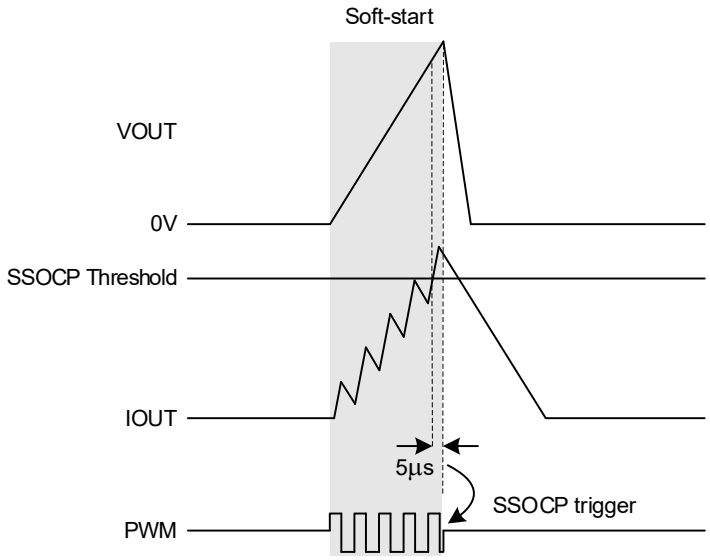


Figure 24. Soft-start Overcurrent Protection Mechanism

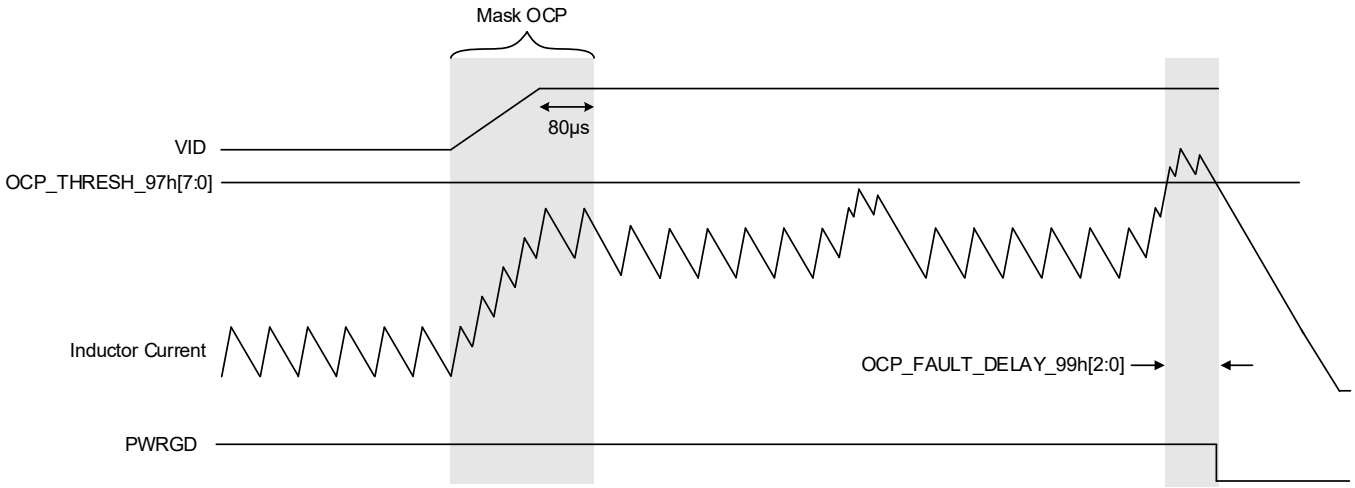


Figure 25. Overcurrent Protection Mechanism

After OCP event is removed, the controller can be restarted, and the I2C_FAULT_STATUS_1Ah[0] can be cleared by toggling VCC power or PWREN pin. During VOTF period plus 80µs (After VID settles + 80µs), OCP is masked to avoid trigger.

Overvoltage Protection (OVP)

The RT3672EE monitors the output voltage with the VSEN pin for overvoltage detection. The OVP threshold is related to VID condition. Table 11 summarizes the OVP mechanism. The OVP mechanism is illustrated in Figure 26 and Figure 27.

OVP is masked when VID = 0V.

During active regulation, the OVP threshold is VID/VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET, where VID/VID_MAX can be selected via SVI3 register OVP_REF_2Ch[7], OVP_DELTA can be set via SVI3 register OVP_DELTA_2Ch[6:4], VOUT_OFFSET can be set via SVI3 register VOUT_OFFSET_22h[7:0], and I2C_VOUT_OFFSET can set via I^2C register I2C_VOUT_OFS_08h[7:0].

During positive/negative VOTF transitions period + 80µs, the OVP threshold is VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET, where VID_MAX can be set via SVI3 register VID_MAX_23h[7:0].

The RT3672EE also provides flexible OVP threshold by I^2C register. When I2C_OVP_DELTA_16h[6:4] = 000: Disabled, the OVP threshold follows SVI3 setting. When I2C_OVP_DELTA_16h[6:4] ≠ 000: Enable I2C_OVP, the VID/VID_MAX follows I^2C setting via I^2C register I2C_OVP_REF_16h[7], and the OVP_DELTA follows I^2C setting via I^2C register I2C_OVP_DELTA_16h[6:4].

When OVP is triggered with 0.8µs filter time, the controller de-asserts PWRGD and forces all PWMs low to turn on low-side power MOSFETs. The PWM remains low until the output voltage is pulled down below OVP_VID. After 60µs from OVP is triggered, VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE.

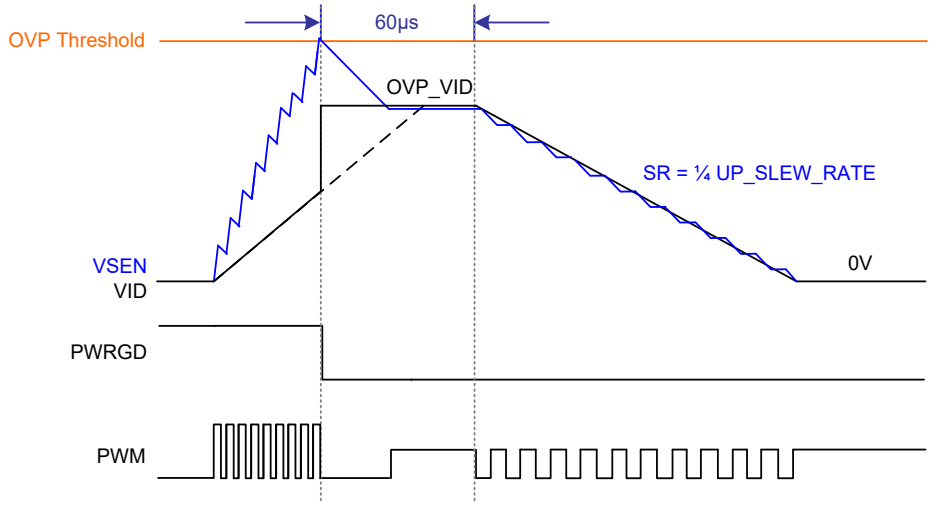


Figure 26. Overvoltage Protection Mechanism during Positive VOTF Transitions

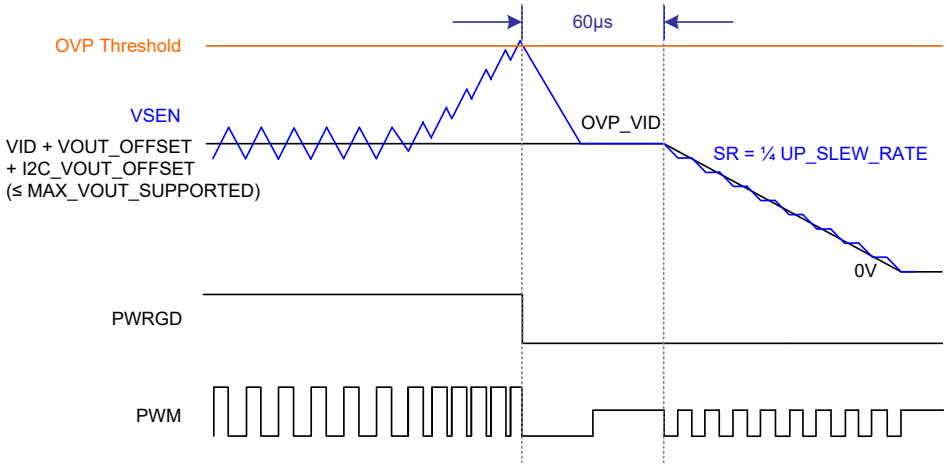


Figure 27. Overvoltage Protection Mechanism during Active Regulation

Table 11. Summary of Overvoltage Protection

Condition	OVP Threshold	Behavior	Protection Reset
VID = 0	OVP is masked.	NA	VCC /PWREN Re-toggled
During VOTF transitions period + 80μs (positive and negative)	OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET **VID_MAX ≠ 0V** VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **VID_MAX = 0V** MAX_VOUT_SUPPORTED is used to calculate OVP threshold. New OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. **VID_MAX ≠ 0V** OVP_VID = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **VID_MAX = 0V** MAX_VOUT_SUPPORTED is used to calculate OVP_VID. OVP_VID = MAX_VOUT_SUPPORTED	
During Active Regulation	**OVP_REF: VID** OVP_TH = VID + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET (VID + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED) **OVP_REF: VID_MAX** OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. **VID_MAX ≠ 0V:** VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED 2. **VID_MAX = 0V:** MAX_VOUT_SUPPORTED is used to calculate OVP threshold. New OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. **OVP_REF: VID** OVP_VID = VID + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **OVP_REF: VID_MAX** 1. **VID_MAX ≠ 0V:** VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED 2. **VID_MAX = 0V:** MAX_VOUT_SUPPORTED is used to calculate OVP_VID. New OVP_VID = MAX_VOUT_SUPPORTED	
During VOTF transitions period + 80μs in VFIX mode (positive and negative)	**VFIX_EN: Enable** OVP_TH = VFIX_MAX + OVP_DELTA (VFIX_MAX ≤ MAX_VOUT_SUPPORTED)	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID = VFIX_MAX ≤ MAX_VOUT_SUPPORTED	

Continued

Condition	OVP Threshold	Behavior	Protection Reset
During Active Regulation in VFIX mode	**VFIX_EN: Enable** OVP_TH = VFIX + OVP_DELTA (VFIX ≤ VFIX_MAX)	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID = VFIX ≤ VFIX_MAX	VCC /PWREN Re-toggled
Change OVP_TH during VOTF transitions period + 80μs (positive and negative)	**New OVP_TH > Previous OVP_TH** The controller changes new OVP_TH immediately. **New OVP_TH < Previous OVP_TH** After VOTF transitions period + 80μs, the controller changes previous OVP_TH to new OVP_TH.	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID is the same in the four conditions: 1. During VOTF transitions period + 80μs 2. During Active Regulation 3. During VOTF transitions period + 80μs in VFIX mode 4. During Active Regulation in VFIX mode	

Undervoltage Protection (UVP)

The RT3672EE monitors the output voltage with the VSEN pin for undervoltage detection. The UVP threshold is related to VID condition. Table 12 summarizes the UVP mechanism.

The UVP mechanism is illustrated in Figure 28. During active regulation, the UVP threshold is VID/VID_MIN - UVP_DELTA + VOUT_OFFSET +I2C_VOUT_OFFSET, where VID/VID_MAX can be selected via SVI3 register UVP_REF_2Ch[3], UVP_DELTA can be set via SVI3 register UVP_DELTA_2Ch[2:0], VOUT_OFFSET can be set via SVI3 register VOUT_OFFSET_22h[7:0], and I2C_VOUT_OFFSET can be set via I^2C register I2C_VOUT_OFS_08h[7:0].

UVP is masked during positive/negative VOTF transitions period.

When UVP is triggered with 3.3ms filter time, the controller de-asserts PWRGD and forces all PWMs in tri-state to turn off both high-side and low-side MOSFETs.

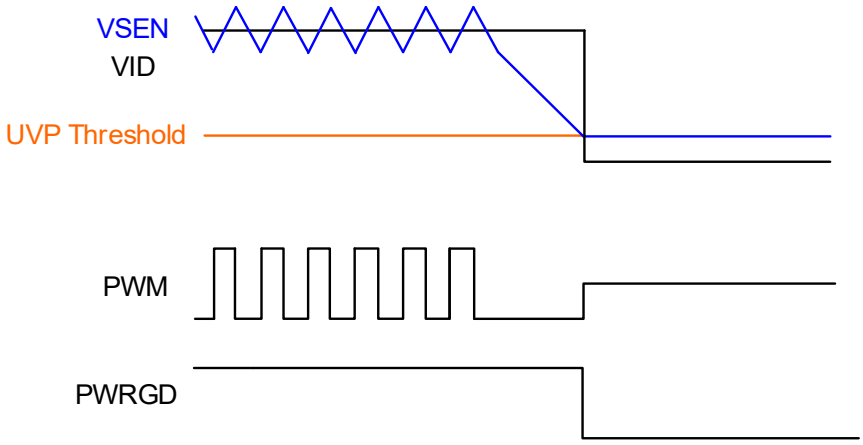


Figure 28. Undervoltage Protection Mechanism during Active Regulation

Table 12. Summary of Undervoltage Protection

Condition	OVP Threshold	Behavior	Protection Reset
VID = 0	UVP is masked.	NA	VCC /PWREN Re-toggled
During VOTF transitions period (positive and negative)	UVP is masked.	NA	
During Active Regulation	**UVP_REF: VID** UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET (MIN_VOUT_SUPPORTED ≤ VID + VOUT_OFFSET + I2C_VOUT_OFFSET) **UVP_REF: VID_MIN** UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. VID_MIN ≠ 0V: MIN_VOUT_SUPPORTED ≤ VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET 2. VID_MIN = 0V: MIN_VOUT_SUPPORTED is used to calculate UVP threshold. New UVP_TH = MIN_VOUT_SUPPORTED - UVP_DELTA	PWRGD de-assertion. All PWMs are in tri-state to turn off both high-side and low-side MOSFETs.	
During VOTF transitions period in VFIX mode (positive and negative)	UVP is masked.	NA	
During Active Regulation in VFIX mode	**VFIX_EN: Enable** UVP_TH = VFIX - UVP_DELTA	PWRGD de-assertion. All PWMs are in tri-state to turn off both high-side and low-side MOSFETs.	

VR-Hot Warning and Over-Temperature Protection (OTP)

The RT3672EE provides VR-Hot Warning and Over-Temperature Protection (OTP) to monitor the temperature from TESN pin. The VR_HOT# pin is an open-drain output, and an external pull-up resistor is required.

The mechanism of VR-HOT Warning is illustrated in Figure 29. When the sensed temperature is higher than VR-HOT threshold, the controller asserts the VR_HOT bit in the temperature telemetry packet, PWRGD pin keeps high, all PWM signals remain normal regulation, and VR_HOT# pin is asserted to indicate a thermal warning. The VR-HOT threshold can be set via SVI3 register VRHOT_THRESH_2Ah[7:0]. The VR_HOT# can be used to inform the temperature of power stage, and it helps to reduce power consumption when temperature exceeds VR-HOT threshold. VR_HOT# is de-asserted if the VR temperature drops below (VRHOT_THRESH – I2C_VRHOT_HYS). The hysteresis of VR-HOT threshold can be set via I^2C register I2C_VRHOT_HYS_19h[2:0].

The mechanism of OTP is illustrated in Figure 30. When the sensed temperature is higher than OTP threshold, the controller de-asserts PWRGD, asserts the OTP bit in the temperature telemetry packet, and forces all PWMs tri-state to turn off both high-side and low-side MOSFETs. The OTP threshold can be set via SVI3 register OTP_THRESH_2Bh[7:0].

The RT3672EE also provides flexible threshold of VRHOT and OTP by I^2C register. When EN_I2C_VRHOT_16h[1] = 0, the VRHOT threshold follows SVI3 setting. When EN_I2C_VRHOT_16h[1] = 1, the VRHOT threshold follows I^2C setting via I^2C register I2C_VRHOT_TH_18h[7:0]. When EN_I2C_OTP_16h[0] = 0, the OTP threshold follows SVI3 setting. When EN_I2C_OTP_16h[0] = 1, the OTP threshold follows I^2C setting via I^2C register I2C_OTP_TH_17h[7:0].

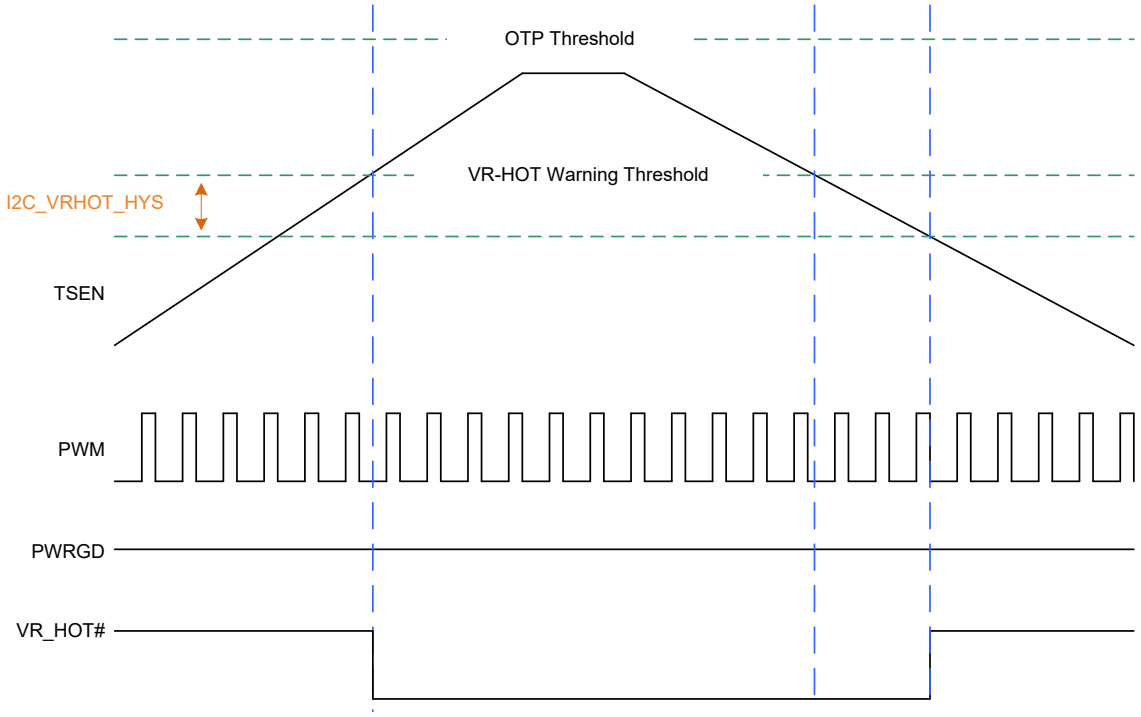


Figure 29. VR-HOT Warning Mechanism

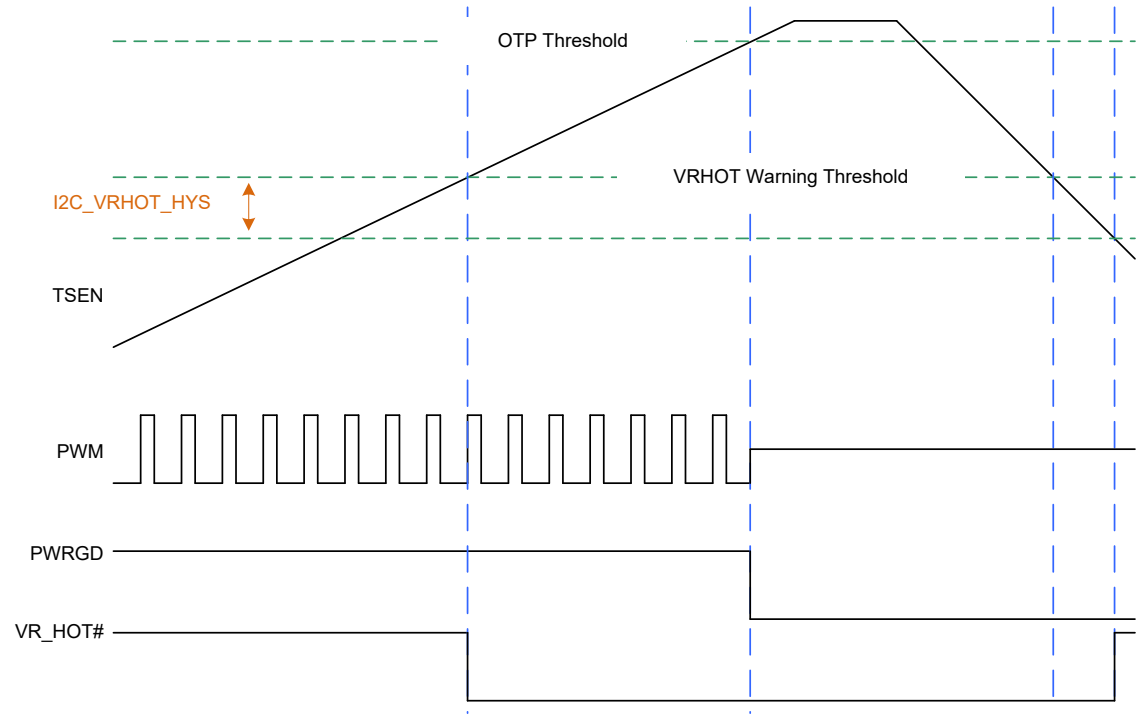


Figure 30. Over-Temperature Protection Mechanism

CRC Failure

NVM loading of the RT3672EE begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RT3672EE will download NVM into the control registers. CRC check ensures the completion of configuration download from NVM to the RT3672EE control register. A configuration download CRC failure prevents the controller from leaving the Inactive state and asserts I2C register NVM_PROGRAM_STATUS_ECh[1:0].

Communication Failure

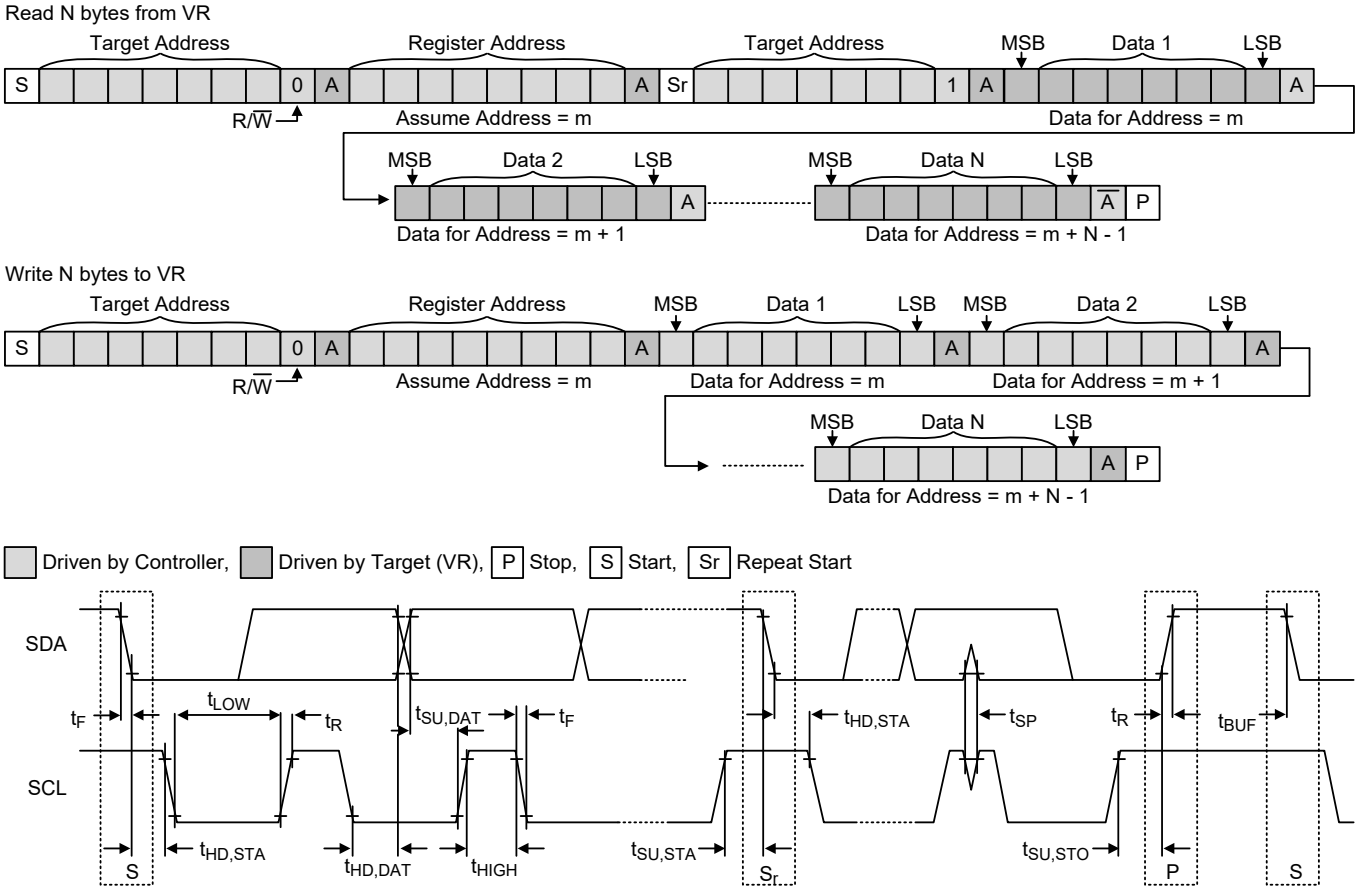
Attempts to access unimplemented commands are detected and reported as communication failures. RT3672EE can recode the SVI3 communication failure through I2C register SVI3_NACK_STATUS_1Bh. The SVI3_NACK_STATUS command returns one byte of information relating to the SVI3 NACK status: Command before ACK/Framing Error/CRC Error/Undefined Register Command/Undefined Payload/Not Executable/Not Supported.

I²C Interface

The I²C target address (7-bit format) by ADDR pin is summarized in Table 1.

This I²C does not have a stretch function.

The I²C interface supports standard target mode (100 kbps), and fast mode (400kbps). The write or read bit stream (N>1) is shown below:



General Register Map (Page 04)

Register Address/NAME		Type	Default Value	NVM	Note
00h	PH1_CURRENT_BALANCE_GAIN	R/W	04h	Yes	PH1_CBG = 100%
01h	PH2_CURRENT_BALANCE_GAIN	R/W	04h	Yes	PH2_CBG = 100%
08h	I2C_VOUT_OFS	R/W	00h	Yes	I2C_VOUT_OFS = 0mV
09h	VFIX_MAX_L	R/W	BFh	No	VFIX_MAX = 2.4V
0Ah	VFIX_MAX_H	R/W	00h	No	
0Bh	EN_VFIX	R/W	00h	No	EN_VFIX = Disable
0Ch	VFIX_L	R/W	33h	Yes	VFIX = 1V
0Dh	VFIX_H	R/W	00h	Yes	
0Eh	VOFS_BY_IOUT_RPT	R/W	00h	No	VOFS_BY_IOUT_RPT = 0mV
0Fh	VOFS_BY_IOUT_RPT_TH_L	R/W	00h	No	VOFS_BY_IOUT_RPT_TH = Disabled
10h	VOFS_BY_IOUT_RPT_TH_H	R/W	00h	No	
11h	EM_MASK_TIME & VOFS_BY_IOUT_RPT_HYS	R/W	08h	No	Mask VOFS_BY_IOUT during VOTF+200μs, VOFS_BY_IOUT_RPT_HYS = 12A
12h	EN_PSI	R/W	00h	Yes	PSI state follows SVI3
13h	I2C_LL_SEL & I2C_LL_ADJ	R/W	0Ah	No	LL_ADJ follow SVI3, I2C_LL_ADJ = 100%
14h	EN_PROTECTION	R/W	7Fh	No	Enable all protections
16h	I2C_OVP_REF & I2C_OVP_DELTA & EN_I2C_VRHOT & OTP_TH	R/W	00h	Yes	OVP_TH, VRHOT_TH and OTP_TH follow SVI3
17h	I2C_OTP_TH	R/W	A5h	Yes	I2C_OTP_TH = 125˚C
18h	I2C_VRHOT_TH	R/W	8Ch	Yes	I2C_VRHOT_TH = 100˚C
19h	I2C_VRHOT_HYS	R/W	00h	Yes	I2C_VRHOT_HYS = 0˚C
1Ah	I2C_FAULT_STATUS	R	Current status	No	
1Bh	SVI3_NACK_STATUS	R	Current status	No	
20h	IOUT_RPT_RATIO	R/W	00h	No	IOUT_RPT_RATIO = 100%
21h	IOUT_RPT_L	R	Current status	No	
22h	IOUT_RPT_H	R	Current status	No	
23h	TEMP_RPT	R	Current status	No	
24h	VOUT_RPT_L	R	Current status	No	
25h	VOUT_RPT_H	R	Current status	No	
DDh	PRODUCT_ID	R	72h	No	RT3672EE
DEh	REVISION_CODE	R	00h	No	
DFh	WDR	R/W	03h	Yes	Watchdog-Reset = Enabled, Watchdog-Reset period = 1600ms

Register Address/NAME		Type	Default Value	NVM	Note
ECh	NVM_PROGRAM_STATUS	R	Current status	No	
EDh	STORE_RESTORE_CFG	R/W	00h	No	
EFh	PAGE	R/W	03h	No	EFh = 02h: Page 02. Setting registers, EFh = 04h: Page 04. General registers.

Register Address: 00h **Description**: Setting phase 1 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH1_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH1_CBG		[2:0] = 000: 69.2%, [2:0] = 001: 79.2%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (Default). [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08%.				

Register Address: 01h **Description**: Setting phase 2 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH2_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH2_CBG		Please refer to register 00h for detailed description.					

Register Address: 08h
Description: VOUT offset setting. RT3672EE supports output voltage from 0.5V to 2.4V (i.e. 0.5V ≤ VID setting ± SVI3_VOUT_OFFSET ± I2C_VOUT_OFFSET ≤ 2.4V). RT3672EE will slew VOUT to target voltage at the slew rate of 1/4 of SVI3_UP_SLEW_RATE, while the minimum slew rate is limited at 2.5 mV/μs. The VR will return to PSI0 and begin to ramp up when an offset command is issued. The VR will return to its original PSI state after the output voltage is within tolerance band. If CPU sends a PSI-changing command, the controller follows the command with VOUT offset remain existing. When CPU sends VID off command, the output voltage is 0V regardless of the value of offset register.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VOUT_OFS							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	I2C_VOUT_OFS	[7]: sign bit (as part of two's complement). [6:0]: 5mV/LSB For example, [7:0] = 00h: 0mV (Default), [7:0] = 01h: 5mV, [7:0] = 7Fh: 635mV, [7:0] = FFh: 5mV, [7:0] = 80h: 640mV.

Register Address: 09h
Description: Setting the maximum value of Fixed-VID mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_L							
Default Value	0xBF							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

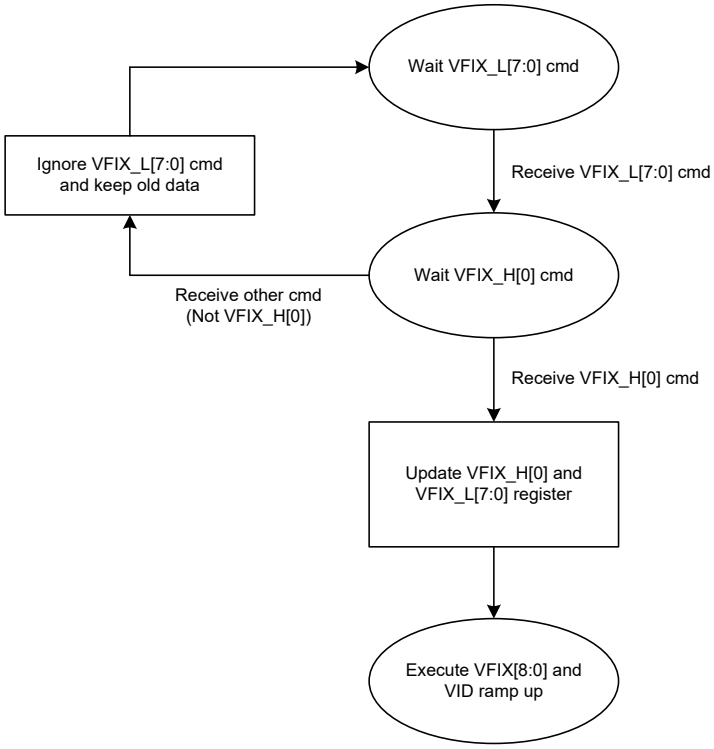
Bits	Name	Description
[7:0]	VFIX_MAX_L	Default value of VFIX_MAX[8:0] is 0BFh = 2.4V. VFIX_MAX[8:0] = { VFIX_MAX_H[0], VFIX_MAX_L[7:0] }, Please refer to SVI3 Type II Target VID Table. RT3672EE supports output voltage from 0.5V~2.4V. VFIX_MAX will be limited at 2.4V if a value greater than 2.4V is given.

Register Address: 0Ah
Description: Setting the maximum value of Fixed-VID mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_H							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
[7:1]	RESERVED	Reserved bit(s). [7:1] = 0000000 (Default).
[0]	VFIX_MAX_H	Please refer to the description of VFIX_MAX_L.

Register Address: 0Bh **Description**: Enable/disable Fixed-VID mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_VFIX							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R/W
Bits	**Name**		**Description**					
[7:1]	RESERVED		Reserved bit(s). [7:1] = 0000000 (Default).					
[0]	EN_VFIX		[0] = 0: Disable Fixed-VID mode (Default), [0] = 1: Enable Fixed-VID mode.					



Register Address: 0Ch **Description**: A 9-bit VOUT command for Fixed-VID mode. If Fixed-VID mode is enabled, VR skips all VID and offset commands and responds to PSI-changing command when necessary. When Fixed-VID mode is disabled, VR returns to its original VID and PSI state set by last SVI3 command(s). The VOUT slew rate of Fixed-VID mode entry and exit is 1/4 of SVI3_UP_SLEW_RATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_L							
Default Value	0x33							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	VFIX_L		Default value of VFIX[8:0] is 033h = 1V. VFIX[8:0] = { VFIX_H[0], VFIX_L[7:0] }. Please refer to SVI3 Type II Target VID Table. VFIX[8:0] command can be set within VFIX_MAX. If VFIX[8:0] command is beyond VFIX_MAX, VOUT will keep the previous VFIX[8:0] command.					

Register Address: 0Dh
Description: Please refer to the description of VFIX_L (I^2C register 0x0C).

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_H							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
[7:1]	RESERVED	Reserved bit(s). [7:1] = 0000000 (Default).
[0]	VFIX_H	Please refer to the description of VFIX_L.

Register Address: 0Eh
Description: Changing VOUT offset dynamically based on IOUT reporting. If IOUT telemetry exceeds the threshold defined in I^2C register 0x0F and 0x10, the offset of VOFS_BY_IOUT_RPT(0x0E) will be added to VOUT automatically without additional communication required.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VOFS_BY_IOUT_RPT	[7]: sign bit (as part of two's complement). [6:0]: 5mV/LSB For example, [7:0] = 00h: 0mV (Default), [7:0] = 01h: 5mV, [7:0] = 7Fh: 635mV, [7:0] = FFh: 5mV, [7:0] = 80h: 640mV.

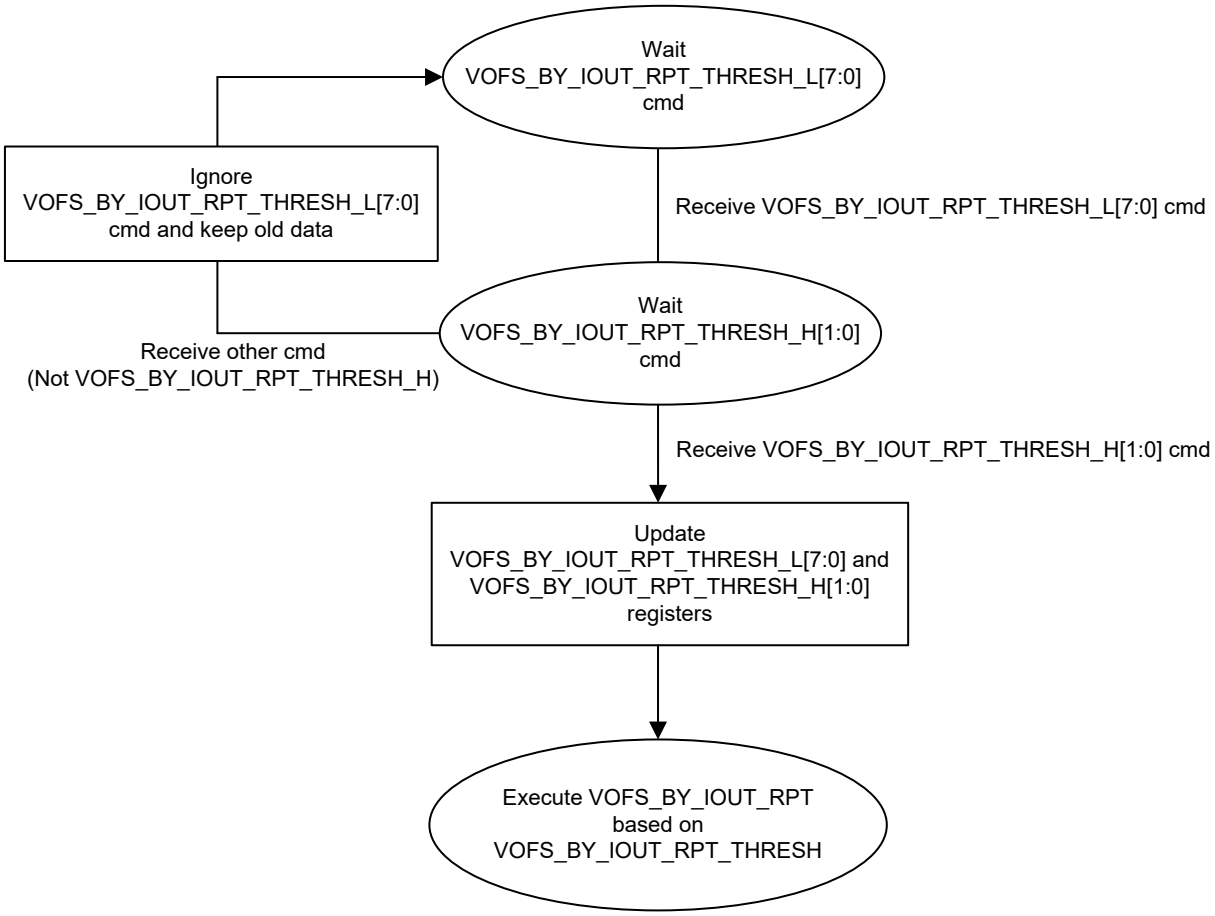
Register Address: 0Fh
Description: A 10-bit IOUT threshold for changing VOUT offset dynamically. It should be noticed that VOFS_BY_IOUT_RPT_THRESH_L needs to be programmed prior to VOFS_BY_IOUT_RPT_THRESH_H in order to successfully set the IOUT threshold.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT_THRESH_L							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VOFS_BY_IOUT_RPT_THRESH_L	VOFS_BY_IOUT_RPT_THRESH[9:0] = { 0x10[1:0], 0x0F[7:0] }. IOUT_THRESH = VOFS_BY_IOUT_RPT_THRESH[9:0] × I_OUT_SCALE/1023. This function is disabled if VOFS_BY_IOUT_RPT_THRESH[9:0] = 0000h (Default).

Register Address: 10h **Description**: Please refer to the description of VOFS_BY_IOUT_RPT_THRESH_L (I^2C register 0x0F).								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT_THRESH_H							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	**Name**	**Description**
[7:2]	RESERVED	Reserved bit(s). [7:2] = 0000000 (Default).
[1:0]	VOFS_BY_IOUT_RPT_THRESH_H	Please refer to the description of VOFS_BY_IOUT_RPT_THRESH_L (I^2C register 0x0F).



Register Address: 11h
Description: The function of offsetting VOUT based on IOUT can be masked during VOTF + 200μs to avoid false triggering by capacitor charging current. The hysteresis is also defined to avoid repeated entry and exit of VOFS_BY_IOUT_RPT_HYS.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_MASK_TIME & VOFS_BY_IOUT_RPT_HYS							
Default Value	0x08							
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:4]	RESERVED	Reserved bit(s). [7:4] = 0000 (Default).
[3]	EN_MASK_TIME	[3] = 0: Always keep VOFS_BY_IOUT_RPT function. [3] = 1: Mask VOFS_BY_IOUT_RPT during VOTF + 200μs (Default).
[2:0]	VOFS_BY_IOUT_RPT_HYS	[2:0] = 000: 12A (Default) [2:0] = 001: 16A [2:0] = 010: 20A [2:0] = 011: 24A [2:0] = 100: 28A [2:0] = 101: 32A [2:0] = 110: 36A [2:0] = 111: 40A

Register Address: 12h
Description: Set EN_FORCE_SPM, EN_FORCE_PSI0.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PSI							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s). [7:2] = 000000 (Default).
[1]	EN_FORCE_SPM	[1] = 0: Disable, follow SVI3 power states (Default), [1] = 1: Enable, Force VR to operate in SPM and ignore other PSI commands, i.e., the smart phase management (SPM) function is always enabled. The PSI state register will follow SVI3 specification and ACK PSI-changing commands.
[0]	EN_FORCE_PSI0	[0] = 0: Disable, follow SVI3 power states (Default), [0] = 1: Enable, Force VR to operate in PSI0 and ignore other PSIx commands, i.e., VR always operates in full-phase count. The SVI3 register PSI state follows SVI3 specification and ACK PSI-changing commands.

VR Operation Mode by EN_PSI_12h[1:0]:

EN_FORCE_SPM_12h[1]	EN_FORCE_PSI0_12h[0]	VR Operation Mode
Disable	Disable	Follow SVI3 power states.
Disable	Enable	Force PSI0.
Enable	Disable	Force SPM
Enable	Enable	Force PSI0.

Register Address: 13h **Description**: Setting load-line adjustment and ratio.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_LL_SEL & I2C_LL_ADJ							
Default Value	0x0A							
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7]	I2C_LL_SEL		[7] = 0: LL_ADJ follows SVI3 (Default), [7] = 1: LL_ADJ follows I^2C register.					
[6:5]	RESERVED		Reserved bit(s). [6:5] = 100 (Default).					
[4:0]	I2C_LL_ADJ		Load-line adjustment relative to nominal load-line. RLL = I2C_LL_ADJ × 10% × Nominal LL 10101b~11111b = invalid (out of range). The default value of I2C_LL_ADJ is 01010b (100% of nominal LL).					

Register Address: 14h **Description**: Enable/Disable protection functions.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PROTECTION							
Default Value	0x7F							
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7]	RESERVED		Reserved bit(s).					
[6]	EN_VRHOT		[6] = 0: Disable VRHOT function, [6] = 1: Enable VRHOT function (Default).					
[5]	EN_OTP		[5] = 0: Disable OT protection, [5] = 1: Enable OT protection (Default).					
[4]	RESERVED		Reserved bit(s). [4] = 1 (Default).					
[3]	EN_OCP		[3] = 0: Disable sum OC protection, [3] = 1: Enable sum OC protection (Default).					
[2]	RESERVED		Reserved bit(s). [4] = 1 (Default).					
[1]	EN_UVP		[1] = 0: Disable UV protection, [1] = 1: Enable UV protection (Default).					
[0]	EN_OVP		[0] = 0: Disable OV protection, [0] = 1: Enable OV protection (Default).					

Register Address: 16h **Description**: Setting the control mode for OVP, VRHOT and OTP threshold.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_OVP_REF & I2C_OVP_DELTA & EN_I2C_VRHOT & EN_I2C_OTP							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Bits	**Name**		**Description**					
[7]	I2C_OVP_REF		Reference to set overvoltage protection threshold. [7] = 0: VID [7] = 1: VID_MAX					
[6:4]	I2C_OVP_DELTA		Delta value to set overvoltage protection threshold. [6:4] = 000: Disable, follow SVI3 [6:4] = 001: 350mV [6:4] = 010 to 111: 16h[6:4] x 50mV + 350 mV					
[3:2]	RESERVED		Reserved bit(s). [3:2] = 00 (Default).					
[1]	EN_I2C_VRHOT		[1] = 0: VRHOT threshold is controlled by SVI3 (Default), [1] = 1: VRHOT threshold is controlled by I^2C.					
[0]	EN_I2C_OTP		[0] = 0: OTP threshold is controlled by SVI3 (Default), [0] = 1: OTP threshold is controlled by I^2C.					

Register Address: 17h **Description**: Setting OTP threshold in I^2C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_OTP_TH							
Default Value	0xA5							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	I2C_OTP_TH		Over-temperature protection threshold. if EN_I2C_OTP = 1, OTP Threshold = I2C_OTP_TH[7:0] - 40˚C. [7:0] = 00h: Disable, [7:0] = A5h: 125˚C (Default).					

Register Address: 18h **Description**: Setting VRHOT threshold in I^2C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VRHOT_TH							
Default Value	0x8C							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	I2C_VRHOT_TH		Voltage regulator hot warning threshold. if EN_I2C_VRHOT = 1, VRHOT Threshold = I2C_VRHOT_TH [7:0] - 40˚C. [7:0] = 00h: Disable, [7:0] = 8Ch: 100˚C (Default).					

Register Address: 19h **Description**: Setting VRHOT de-assertion hysteresis in I²C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VRHOT_HYS							
Default Value	0x00							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	I2C_VRHOT_HYS		[2:0] = 000: No hysteresis (Default), [2:0] = 001: 3°C, [2:0] = 010: 6°C, [2:0] = 011: 9°C, [2:0] = 100: 12°C, [2:0] = 101: 15°C, [2:0] = 110: 18°C, [2:0] = 111: 21°C.					

Register Address: 1Ah **Description**: The I2C_FAULT_STATUS command returns one byte of information relating to the fault status.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_FAULT_STATUS							
Default Value	Current status							
Read/Write	R	R	R/W	R	R	R	R	R
Bits	**Name**		**Description**					
[7]	RESERVED		Reserved bit(s). [7] = 0 (Default).					
[6]	SSOCP Fault		Output Soft-start Overcurrent Fault.					
[5]	VRHOT		Voltage Regulator Hot Warning. This bit is writeable 1b to clear.					
[4]	RESERVED		Reserved bit(s). [4] = 0 (Default).					
[3]	OTP Fault		Over-temperature Fault					
[2]	UVP Fault		Output Undervoltage Fault.					
[1]	OVP Fault		Output Overvoltage Fault.					
[0]	OCP Fault		Output Overcurrent Fault.					

Register Address: 1Bh
Description: The SVI3_NACK_STATUS command returns one byte of information relating to the SVI3 NACK status.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SVI3_NACK_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:6]	RESERVED	Reserved bit(s).
[5]	Communication Error	Command before ACK
[4]	Communication Error	Framing Error
[3]	Communication Error	CRC Error
[2]	Invalid Command	Undefined Register Command
[1]	Invalid Command	Undefined Payload
[0]	Invalid Command	Not Executable/Not Supported.

Register Address: 20h
Description: Setting output current reporting ratio adjustment.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_RATIO							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s). [7:2] = 000000 (Default).
[1:0]	IOUT_RPT_RATIO	[1:0] = 00: IOUT_RPT_RATIO = 100% (Default), [1:0] = 01: IOUT_RPT_RATIO = 87.5% [1:0] = 10: IOUT_RPT_RATIO = 75% [1:0] = 11: IOUT_RPT_RATIO = 50%

Register Address: 21h
Description: The IOUT_RPT command returns the actual measured output current shown in the least-significant byte of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_L							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	IOUT_RPT_L	IOUT_RPT[9:0] = { IOUT_RPT_H[1:0], IOUT_RPT_L[7:0] } IOUT = IOUT_RPT[9:0] × I_OUT_SCALE /1023.

Register Address: 22h
Description: The IOUT_RPT command returns the actual measured output current shown in the two most-significant bits of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_H							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s).
[1:0]	IOUT_RPT_H	Please refer to the description of IOUT_RPT_L (I^2C register 0x21).

Register Address: 23h
Description: The TEMP_RPT command returns the actual measured temperature in ˚C shown in the 8-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEMP_RPT							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	TEMP_RPT	Temperature (˚C) = TEMP_RPT[7:0] - 40.

Register Address: 24h
Description: The VOUT_RPT command returns the actual measured output voltage shown in the least-significant byte of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_L							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	VOUT_RPT_L	VOUT_RPT[9:0] = { VOUT_RPT_H[1:0], VOUT_RPT_L [7:0] } VOUT (V) = VOUT_RPT[9:0] × 10mV.

Register Address: 25h
Description: The VOUT_RPT command returns the actual measured output voltage shown in the two most-significant bits of the 10-bit output voltage reporting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_H							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s).
[1:0]	VOUT_RPT_H	Please refer to the description of VOUT_RPT_L (I^2C register 0x24).

Register Address: DDh **Description**: The PRODUCT_ID is a read-only register that shows the code identifier of RT3672EE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRODUCT_ID							
Default Value	0x72							
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
[7:0]	PRODUCT_ID		[7:0] = 72h (Default).					

Register Address: DEh **Description**: A read-only shows the unique model code defined by manufacturer.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REVISION_CODE							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	**Name**		**Description**					
[7:0]	REVISION_CODE		Copy from SVI3 register MODEL_ID[7:0]. Unique model code defined by manufacturer.					

Register Address: DFh **Description**: Watchdog-reset status, enable/disable watchdog function and setting watchdog-reset period.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	WDR							
Default Value	0x03							
Read/Write	R	R	R	R	R	R	R/W	R/W
Bits	**Name**		**Description**					
[7]	WATCHDOG_STATUS		**Watchdog-Reset Status** [7] = 0: Normal SMBus transmission [7] = 1: SMBus transmission hanging exceeds watchdog-reset period					
[6:2]	RESERVED		Reserved bit(s).					
[1]	EN_WATCHDOG_RESET		**Enable/Disable watchdog function** [1] = 0: Disable Watchdog-Reset (If SMBus transition hanging exceeds 30ms, VR I^2C interface state machine is reset but all registers keep the latest value.) [1] = 1: Enable Watchdog-Reset (Watchdog period is based on WATCHDOG_RESET_PERIOD[0] setting. When SMBus transmission hanging exceeds the setting, all I^2C registers reset to the default value.) (Default)					
[0]	WATCHDOG_RESET_PERIOD		**Watchdog-Reset period** [0] = 0: 800ms [0] = 1: 1600ms (Default)					

Register Address: ECh
Description: The NVM_PROGRAM_STATUS command returns one byte of information relating to the NVM program status.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NVM_PROGRAM_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7]	RESTORE_FLAG	Restore process done.
[6]	STORE_FLAG	Store process done.
[5]	STORE_ALLOW	Store process allowed.
[4]	RESTORE_BUSY	NVM restore busy.
[3]	STORE_BUSY	NVM store busy.
[2]	RESERVED	Reserved bit(s).
[1]	CRC_FAILURE_NVM	NVM check fail.
[0]	CRC_FAILURE_NVM_Total	Total NVM check fail.

Register Address: EDh
Description: NVM stores and restores command register. A STORE command instructs the device to copy all the contents of the operating memory into corresponding location of non-volatile memory. A RESTORE command instructs the device to copy the entire contents of non-volatile memory into corresponding addresses of operating memory. It is suggested to disable all the outputs of VR before sending STORE and RESTORE commands.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	STORE_RESTORE_CFG							
Default Value	0x00							
Read/Write	W	W	W	W	W	W	W	W

Bits	Name	Description
[7:0]	STORE_RESTORE_CFG	[7:0] = 66h: Restore all storable register settings from NVM, [7:0] = AAh: Store all storable register settings into NVM as new defaults. Except the two instructions mentioned above, all the other combinations are not defined.

Register Address: EFh
Description: The PAGE command configures, controls and monitors multiple PWM channels through only one physical address.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PAGE							
Default Value	0x03							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	PAGE	[7:0] = 02h: Page 02. Setting registers, [7:0] = 04h: Page 04. General registers. All the other combinations are not defined.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-48L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(26.5°C/W) = 3.77W for a WQFN-48L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 30 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

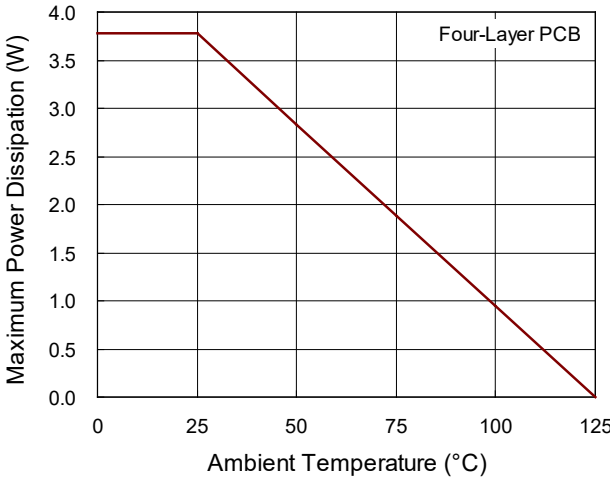
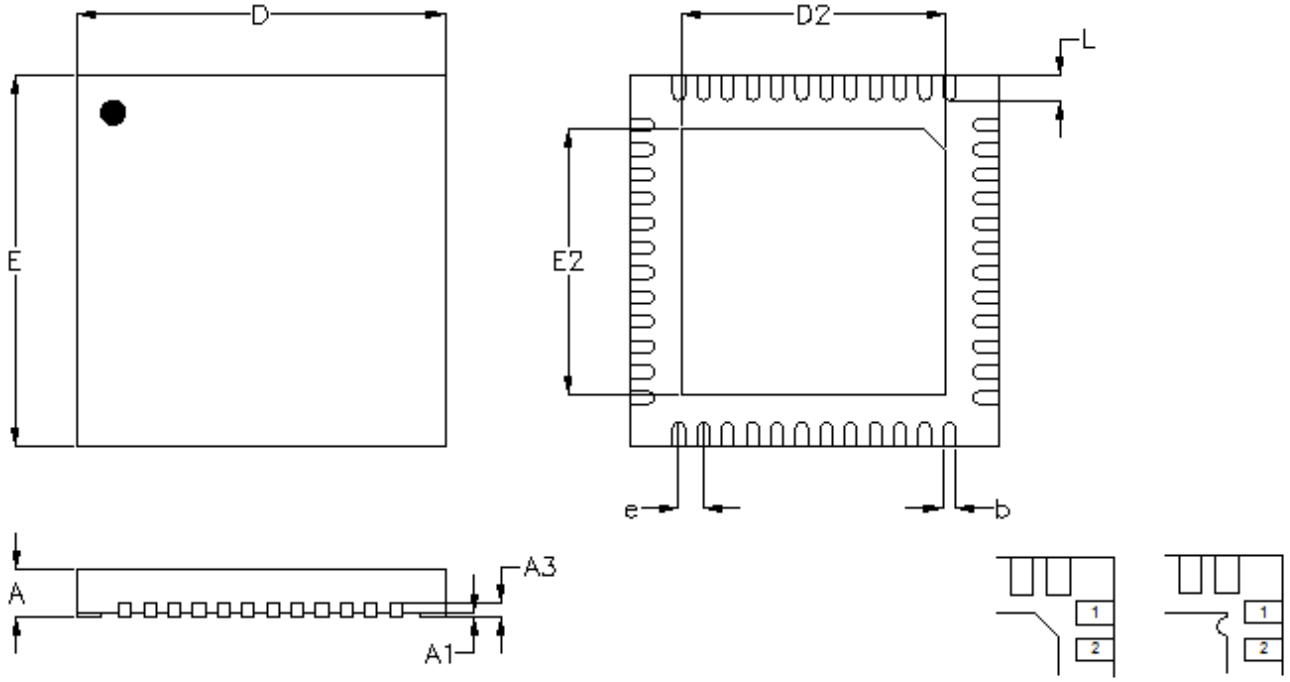


Figure 30. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

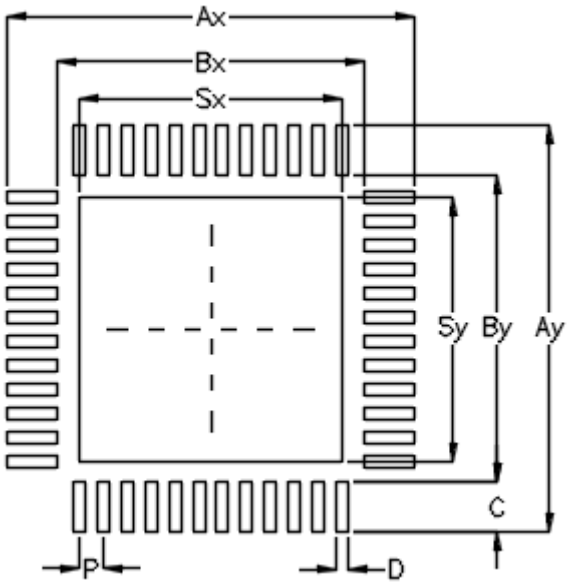
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		5.950	6.050	0.234	0.238
D2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
	Option 4	4.450	4.550	0.175	0.179
E		5.950	6.050	0.234	0.238
E2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
	Option 4	4.450	4.550	0.175	0.179
e		0.400		0.016	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 6x6 Package

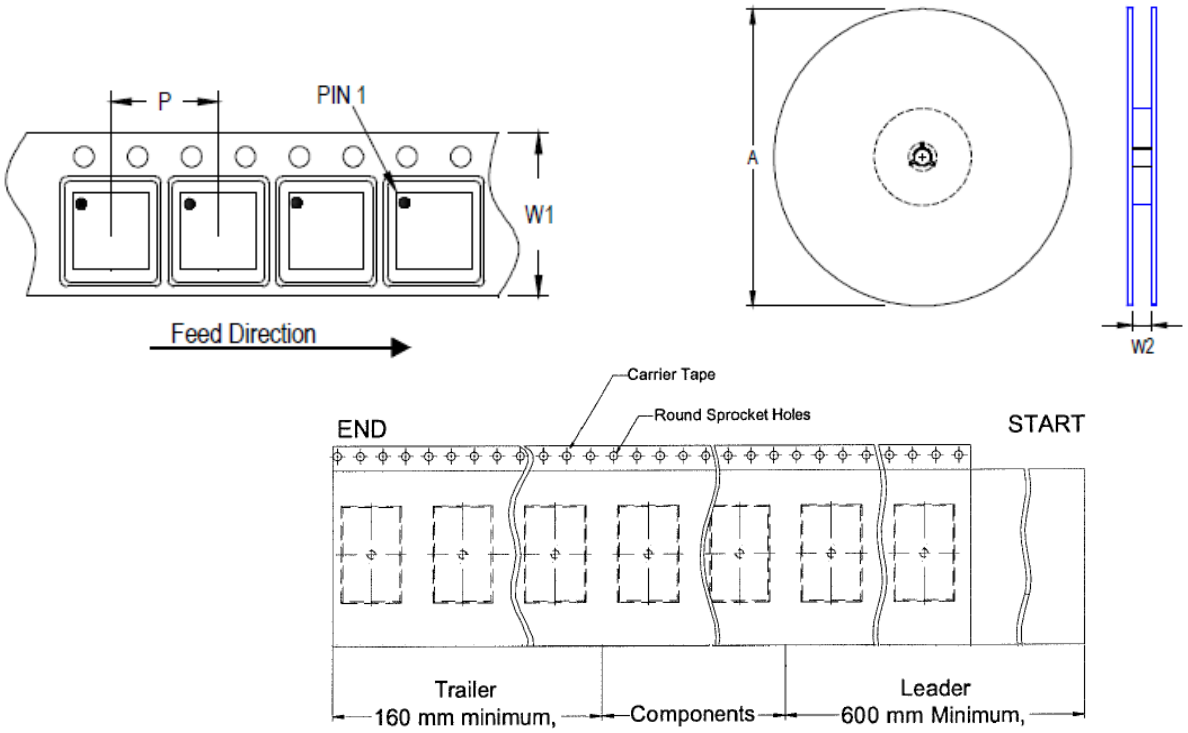
Footprint Information



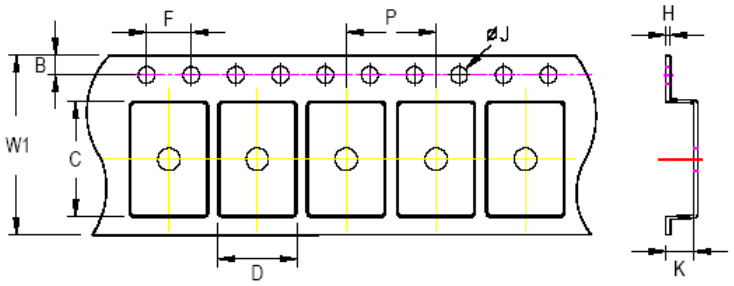
Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN6x6-48	Option1	48	0.40	6.80	6.80	5.10	5.10	0.85	0.20	4.40	4.40	±0.05
	Option2									4.50	4.50	
	Option3									4.70	4.70	
	Option4									4.60	4.60	

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 6x6	16	12	330	13	2,500	160	600	16.4/18.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton		
	Size	Units	Item	Weight(kg)	Reels	Units	Item	Boxes	Units
QFN and DFN 6x6	13”	2,500	Box G	1.11	1	2,500	Carton A	6	15,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/2/7	Final	