RICHTEK® **RT3674AJ**

Triple Channel PWM Controller for AMD SVI3 CPU/GPU Core Power Supply

1 General Description

The RT3674AJ is a synchronous buck controller that supports triple output rails and can fully meet AMD SVI3 requirements. The RT3674AJ adopts G-NAVP (Green Native AVP), which is Richtek's proprietary topology derived from the finite DC gain of the EA amplifier with current mode control, making it easy to set the droop to meet all AMD CPU/GPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3674AJ features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transients and reduce output capacitors. The RT3674AJ integrates a high-accuracy ADC for reporting and a non-volatile memory (NVM) to store custom configurations, such as output current scale, auto phase add/drop threshold, switching frequency, overcurrent thresholds, or AQR trigger level. It also features complete fault protection functions including overvoltage (OV), undervoltage (UV), overcurrent (OC) and undervoltage-lockout (UVLO). The RT3674AJ provides independent enable, power-good indicator, and temperature sense for each output rail. It also supports several functions set by the I^2C interface. The recommended junction temperature range is –40°C to 125°C.

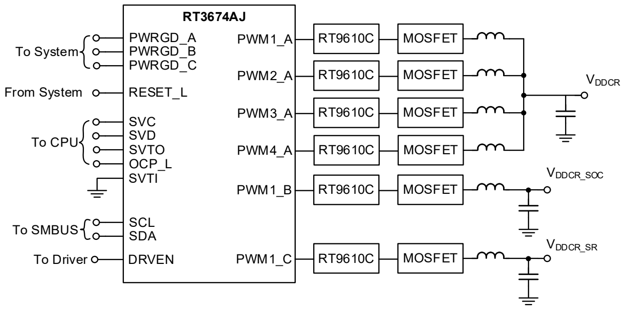
2 Applications

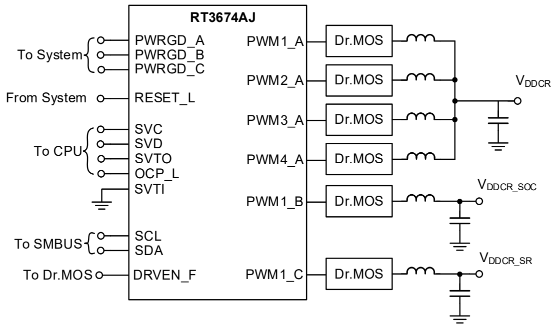
- SVI3 AMD Core Supply
- Desktop and Notebook Computer
- AVP Buck Converter

3 Features

- **AMD SVI3 Rev 1.01 Compatible**
- **4/3/2/1 Phase (Rail A) +1 Phase (Rail B) +1 Phase (Rail C) PWM Controller**
- **G-NAVP (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-In ADC for Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode (DEM) at Light Load**
- **Fast Transient Response: Adaptive Quick Response (AQR)**
- **OVP, OCP, and UVP with Flag**
- **Switching Frequency Setting**
- **Auto Phase Add/Drop with DEM for Excellent Efficiency**
- **Voltage on the Fly (VOTF) Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-Line**
- **Standard I^2C Protocol Interface**
  - **Internal Non-Volatile Memory (NVM) to Store Custom Configurations**
  - **Current Balance Gain Adjustment for Thermal Balance**
  - **Dynamic Load-Line Setting**
  - **Voltage Offset Setting**
  - **Fixed VID Setting**
  - **Protection Report and Protection Disable**
  - **Output Voltage/Output Current/Temperature/ Input Power Monitoring**
- **Soldering Good Detection**
- **Small 60-Lead WQFN Package**

4 Simplified Application Circuit





5 Ordering Information

RT3674AJ □□-□

- The configuration code identifier for the register setting stored in the internal NVM
- **Package Type**(1)
  QW: WQFN-60L 7x7 (W-Type)
- **Lead Plating System**
  G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information

RT3674AJ
GQW
YMDAN

RT3674AJGQW: Product Code
YMDAN: Date Code

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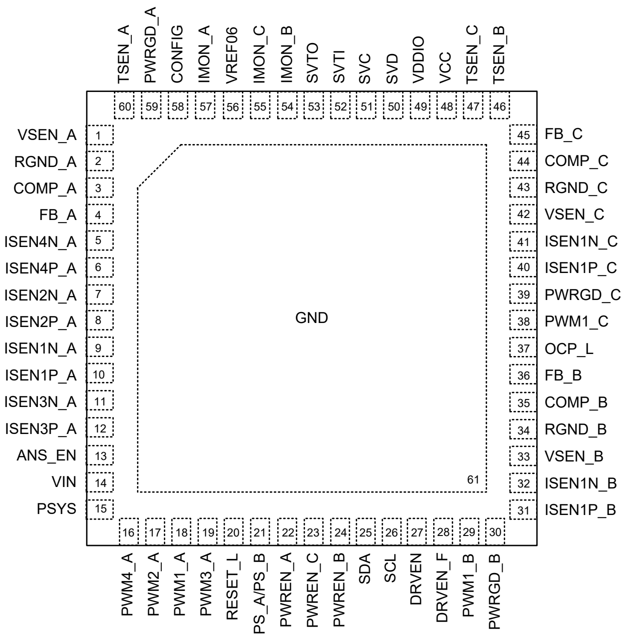
7 Pin Configuration

(TOP VIEW)



WQFN-60L 7x7

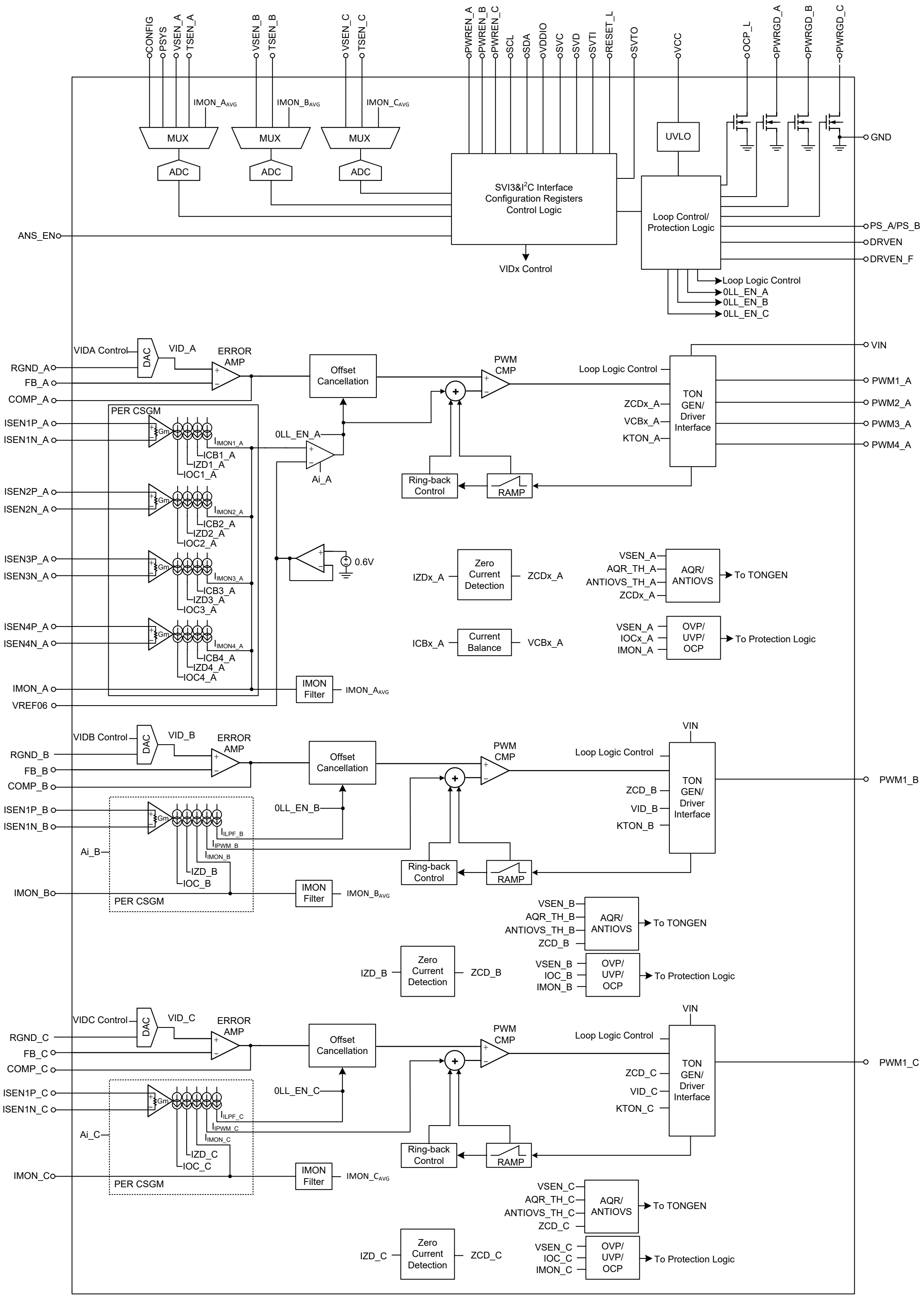
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VSEN_A	Positive differential voltage sense input for rail A. Connect to the positive remote sensing point and should be routed with RGND_A as a differential pair.
2	RGND_A	Negative differential voltage sense input for rail A. Connect to the negative remote sensing point.
3	COMP_A	Error amplifier output of rail A.
4	FB_A	Error amplifier voltage feedback of rail A.
5	ISEN4N_A	Phase #4 current sense inputs of rail A. The ISEN4N_A and ISEN4P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN4P_A to VCC programs 3-phase operation.
6	ISEN4P_A	
7	ISEN2N_A	Phase #2 current sense inputs of rail A. The ISEN2N_A and ISEN2P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN2P_A to VCC programs 1-phase operation.
8	ISEN2P_A	
9	ISEN1N_A	Phase #1 current sense inputs of rail A. The ISEN1N_A and ISEN1P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN1P_A to VCC if rail A is not used.
10	ISNE1P_A	
11	ISNE3N_A	Phase #3 current sense inputs of rail A. The ISEN3N_A and ISEN3P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN3P_A to VCC programs 2-phase operation.
12	ISEN3P_A	
13	ANS_EN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
14	VIN	VIN input pin. Connect a low-pass filter to this pin to set on-time.
15	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. Pulling this pin to VCC can disable the PSYS function.

Pin No.	Pin Name	Pin Function
16	PWM4_A	Phase #4 rail A PWM output. This signal is used to drive the PWM input of the MOSFET diver IC. Unused PWM pins should be left unconnected. The PWM tri-state windows can be selected by NVM. One is 1.6V to 2.2V and the other is 1.4V to 2.1V. The PWM output high level is pulled up to VCC (5V) and low level is pulled down to GND.
17	PWM2_A	Phase #2 rail A PWM output. Refer to PWM4_A description.
18	PWM1_A	Phase #1 rail A PWM output. Refer to PWM4_A description.
19	PWM3_A	Phase #3 rail A PWM output. Refer to PWM4_A description.
20	RESET_L	SVI3 interface input pin. An active low signal causes all SVI3 state machines and SVI3 define registers to reset to default states.
21	PS_A/PS_B	External driver mode control. The PS_A/PS_B pin can be configured as rail A or rail B by NVM. This pin can work with the RT9637 to drive two power stages with single PWM signal. As the PSI0 command is received, this pin is in low state. As the PSI1 or PSI2 command is received and the phase count is 1, this pin is in floating state. As the PSI3 or PSI6 command is received, this pin is in high state.
22	PWREN_A	Active high output enable input pin for rail A. Faults are cleared when PWREN_A is toggled, but no effect on the sticky FAULT_STATUS bits.
23	PWREN_C	Active high output enable input pin for rail C. Faults are cleared when PWREN_C is toggled, but no effect on the sticky FAULT_STATUS bits.
24	PWREN_B	Active high output enable input pin for rail B. Faults are cleared when PWREN_B is toggled, but no effect on the sticky FAULT_STATUS bits.
25	SDA	I^2C data signal.
26	SCL	I^2C clock signal.
27	DRVEN	External driver mode control. As the PSI6 command is received, this pin is in low state. The output high level is VCC.
28	DRVEN_F	External driver mode control. As the PSI6 command is received, this pin is in floating state. The output high level is VCC.
29	PWM1_B	Phase #1 Rail B PWM output. Refer to PWM4_A description.
30	PWRGD_B	Power-Good indicator for rail B. This open-drain output requires an external pull-up resistor. PWRGD_B is pulled low when a shutdown fault occurs.
31	ISEN1P_B	Phase #1 current sense inputs of rail B. The ISEN1N_B and ISEN1P_B pins are used to differentially sense the corresponding channel current. Connect ISEN1P_B to VCC if rail B is not used.
32	ISEN1N_B	
33	VSEN_B	Positive differential voltage sense input for rail B. Connect to positive remote sensing point and should be routed with RGND_B as a differential pair.
34	RGND_B	Negative differential voltage sense input for rail B. Connect to negative remote sensing point.
35	COMP_B	Error amplifier output of rail B.
36	FB_B	Error amplifier voltage feedback of rail B.
37	OCP_L	SVI3 interface output pin. This open-drain output requires an external pull-up resistor. Asserted when the output current is greater than the OCP threshold or the OCP warning threshold. The three rails of the controller share one OCP_L pin.
38	PWM1_C	Phase #1 rail C PWM output. Refer to PWM4_A description.

Pin No.	Pin Name	Pin Function
39	PWRGD_C	Power-Good indicator for rail C. This open-drain output requires an external pull-up resistor. PWRGD_C is pulled low when a shutdown fault occurs.
40	ISEN1P_C	Phase #1 current sense inputs of rail C. The ISEN1N_C and ISEN1P_C pins are used to differentially sense the corresponding channel current. Connect ISEN1P_C to VCC if rail C is not used.
41	ISEN1N_C	
42	VSEN_C	Positive differential voltage sense input for rail C. Connect to positive remote sensing point and should be routed with RGND_C as a differential pair.
43	RGND_C	Negative differential voltage sense input for rail C. Connect to negative remote sensing point.
44	COMP_C	Error amplifier output of rail C.
45	FB_C	Error amplifier voltage feedback of rail C.
46	TSEN_B	Rail B external temperature measurement input pin.
47	TSEN_C	Rail C external temperature measurement input pin.
48	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 2.2Ω and C = 4.7μF. The decoupling capacitor should be placed as close to the PWM controller as possible. The recommended size of R_{VCC} is 0603.
49	VDDIO	Supply voltage input of the SVI3 interface. This pin serves as the reference for SVC, SVD, SVTI, and SVTO.
50	SVD	Serial VID Data input. This pin is a push-pull signal, which transmits commands from the master to the slaves.
51	SVC	Serial VID Clock input. This pin is a push-pull signal, which acts as a clock for SVD, SVTI, and SVTO.
52	SVTI	Serial VID Telemetry input. This pin is driven by the next-furthest slave on the telemetry daisy-chain.
53	SVTO	Serial VID Telemetry output. This pin is a push-pull output.
54	IMON_B	Rail B VR current monitor output. This pin outputs a current proportional to the output current.
55	IMON_C	Rail C VR current monitor output. This pin outputs a current proportional to the output current.
56	VREF06	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. While the controller shuts down or sets all rails in PSI6, voltage source shuts down. An exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND.
57	IMON_A	A rail VR current monitor output. This pin outputs a current proportional to the output current.
58	CONFIG	NVM configuration selection pin to select the stored custom configurations. For soldering check, connect the CONFIG pin to 5V and pull the PWREN high. If the soldering is good, the output is 0.9V for rail A, 1V for rail B, and 1.1V for rail C.
59	PWRGD_A	Power-Good indicator for rail A. This open-drain output requires an external pull-up resistor. PWRGD_A is pulled low when a shutdown fault occurs.
60	TSEN_A	Rail A external temperature measurement input pin.
61 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough via numbers for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- HBM (Human Body Model) ---------- 2Kv

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- VIN to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.75V to 5.25V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

- WQFN-60L 7x7, θ_{JA} ---------- 25.5°C/W
- WQFN-60L 7x7, $\theta_{JC(Top)}$ ---------- 12.9°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

(V_{CC} = 5V, V_{VDDIO} = 1.8V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from −10°C to 105°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.75	--	5.25	V
VCC Power-ON Reset (POR)	$V_{CC\_POR\_R}$		4.25	4.35	4.45	V
VCC Power-ON Reset (POR)	$\Delta V_{CC\_POR\_F\_HYS}$		--	200	--	mV
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_R}$		--	3.66	3.99	V
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_F}$		2.74	3.45	--	V
Supply Current	I_{VCC}	VCC = 5V, PWREN = H, no switching	--	--	40	mA
Supply Current at PSI6	I_{VCC_PSI6}	VCC = 5V, PWREN = H, all rails in PSI6	--	--	180	μA
Shutdown Current	I_{SHDN}	VCC = 5V, PWREN = L	--	--	180	μA
Slew Rate						
VOTF Slew Rate Up	UP_SR	Measure VFB from 20% target VID to 80% target VID, ΔVOTF≥100mV	−10%	--	10%	mV/μs
VOTF Slew Rate Down	DN_SR	Default equals to UP_SR	−10%	--	10%	mV/μs
EA Amplifier						
Current Sensing Amplifier						
CS Input Voltage	V_{CSIN}	Recommend Input Voltage Range for High Accuracy	−10	--	80	mV
Current Sense Gain Error	GAIN_PCS		1.2125	1.25	1.2875	A/A
TON Setting						
On-Time Setting, Rail A	t_{ON}	VIN = 19V, VID = 0.9V, K_{TON} = 1.2	--	79	--	ns
On-Time Setting, Rail B	t_{ON}	VIN = 19V, VID = 0.9V, K_{TON} = 1.27	--	111	--	ns
On-Time Setting, Rail C	t_{ON}	VIN = 19V, VID = 0.9V, K_{TON} = 1.27	--	111	--	ns
Minimum On-Time, Rail A	$t_{ON(min)}$		--	70	--	ns
Minimum On-Time, Rail B	$t_{ON(min)}$		--	50	--	ns
Minimum On-Time, Rail C	$t_{ON(min)}$		--	50	--	ns
Protections						
Overvoltage Protection Threshold	V_{OV}	Default threshold	315	350	385	mV
De-bounce Time of OVP	DT_{OVP}		--	0.8	--	μs
Undervoltage Protection Threshold	V_{UV}	Default threshold	315	350	385	mV
De-bounce Time of UVP	DT_{UVP}		--	3.3	--	μs
Overcurrent Protection Threshold	V_{OCP}		−3	--	3	%

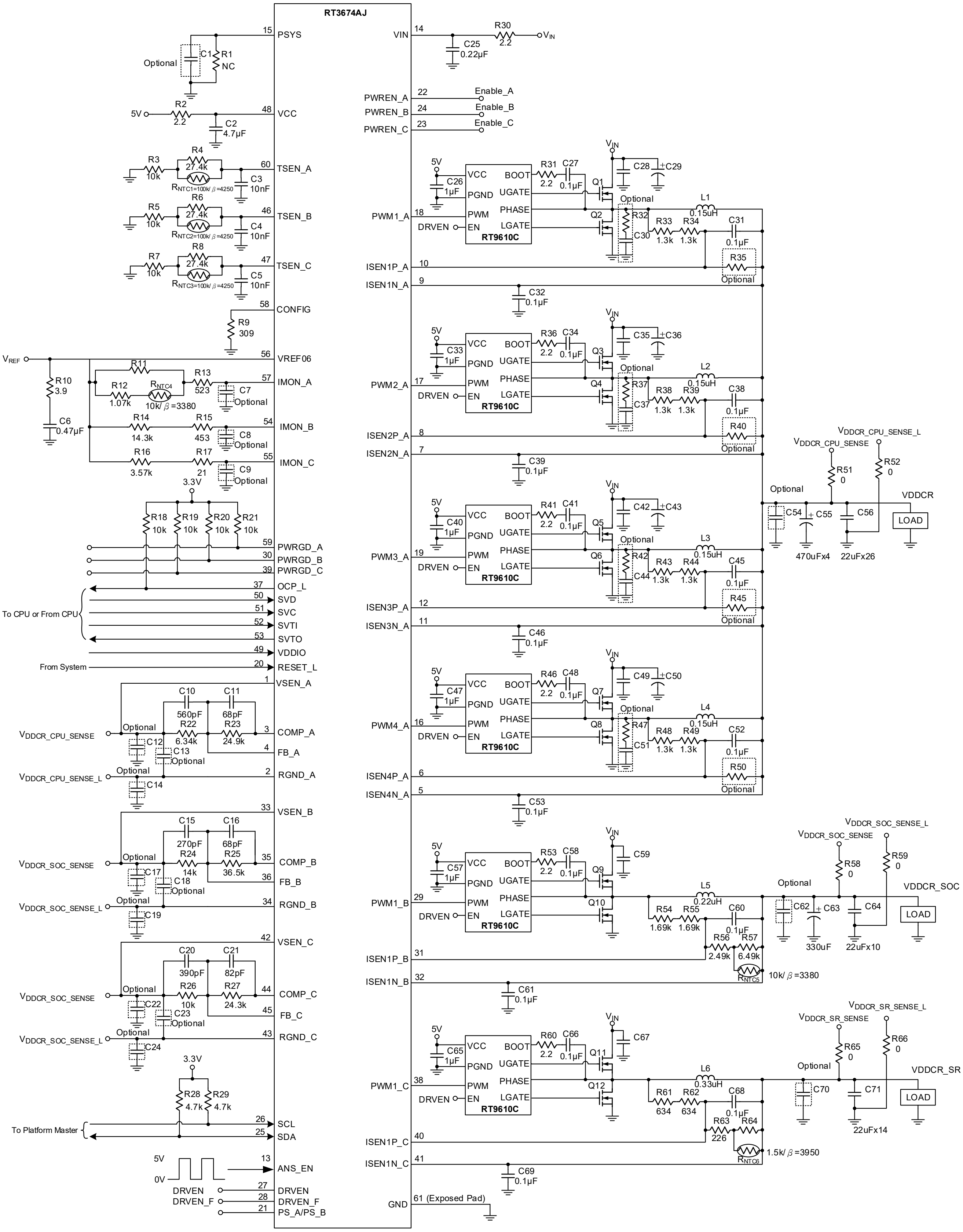
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overcurrent Warning Threshold	V_{OC_WARN}		–3	--	3	%
Over-Temperature Protection Threshold	T_{OTP}		--	125	--	°C
VRHOT Warning Threshold	T_{VRHOT}		--	100	--	°C
PWREN, PWRGD and OCP_L						
PWREN Logic-High	V_{IH_PWREN}		1.17	--	--	V
PWREN Logic-Low	V_{IL_PWREN}		--	--	0.63	
Leakage Current of PWREN	I_{LEAK_PWREN}		-1	--	1	μA
PWRGD, OCP_L Pull Low Voltage	V_{PWRGD/OCP_L}	I_{PWRGD} = 8mA	--	--	0.2	V
VREF						
VREF06 Voltage	V_{VREF06}	Normal operation	0.59	0.6	0.61	V
Acoustic Noise Suppression (ANS)						
ANS_EN Logic-High	$V_{IH\_ANS\_EN}$		V_{CC} – 0.7	--	--	V
ANS_EN Logic-Low	$V_{IL\_ANS\_EN}$		--	--	1	V
SVI3 Interface						
SVC, SVD, SVTI Logic-High	V_{IH}		0.65 x V_{VDDIO}	--	--	V
SVC, SVD, SVTI Logic-Low	V_{IL}		--	--	0.35 x V_{VDDIO}	V
SVTO Output High Voltage	V_{OH}	I = –8mA	V_{VDDIO} – 0.45	--	--	V
		I = –4mA	V_{VDDIO} – 0.22	--	--	V
SVTO Output Low Voltage	V_{OL}	I = 8mA			0.45	V
		I = 4mA			0.22	V
RESET_L Logic-High	$V_{IH\_RESET\_L}$		1.17	--	--	V
RESET_L Logic-Low	$V_{IL\_RESET\_L}$		--	--	0.63	
Leakage Current of SVC, SVD, SVTI, SVTO	I_{LEAK_SVI3}		–10	--	10	μA
I²C interface						
SCL, SDA Logic-High	V_{IH_I2C}		1	--	--	V
SCL, SDA Logic-Low	V_{IL_I2C}		--	--	0.6	
Standard/Fast Mode						
SCL Clock Rate	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	
Hold Time (Repeated) Start Condition. After this	$t_{HD;STA}$		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Period, the First Clock Pulse is Generated						
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$	Standard mode	0	--	--	μs
		Fast mode	0	--	0.9	
Data Set-Up Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA and SCL Signals	t_R	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
Falling Time of Both SDA and SCL signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
ADC						
ADC Resolution			--	10	--	bits
ADC reference voltage			--	3.2	--	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
I_{TSEN}						
TSEN Source Current	I_{TSEN}	V_{TSEN} = 1.6V	79.2	80	80.8	μA
PSYS and DIMON						
Digital PSYS Reporting	D_{PSYS}	V_{PSYS} = 1.6V	--	1023	--	Decimal
Digital IMON_A set	D_{VIMON_A}	$V_{IMON\_A} - V_{VREF06}$ = 0.4V	--	1023	--	Decimal
Digital IMON_B set	D_{VIMON_B}	$V_{IMON\_B} - V_{VREF06}$ = 0.4V	--	1023	--	Decimal
Digital IMON_C set	D_{VIMON_C}	$V_{IMON\_C} - V_{VREF06}$ = 0.4V	--	1023	--	Decimal
Telemetry						
Output Voltage Reporting Accuracy (10-bit Telemetry; 1LSB = 5mV)	$VOUT_{TEL}$	0.250 to 0.995 T_A = 0 to 85°C	−7.5	--	7.5	mV
		1.000 to 2.800 T_A = 0 to 85°C	−0.75	--	0.75	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Temperature Reporting Accuracy (10-Bit Telemetry; 1LSB = 1°C)	$TEMP_{TEL}$	Between 50°C to 125°C	–5	--	5	°C
Temperature Reporting Range	TEMP		–40	--	150	°C

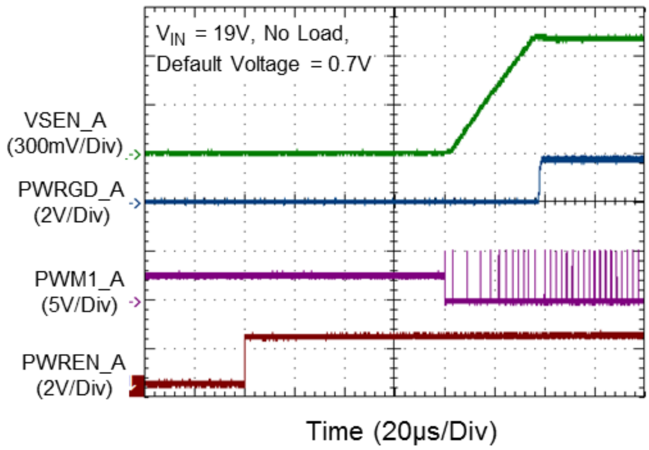
15 Typical Application Circuit

15.1 Platform: FP7-45W

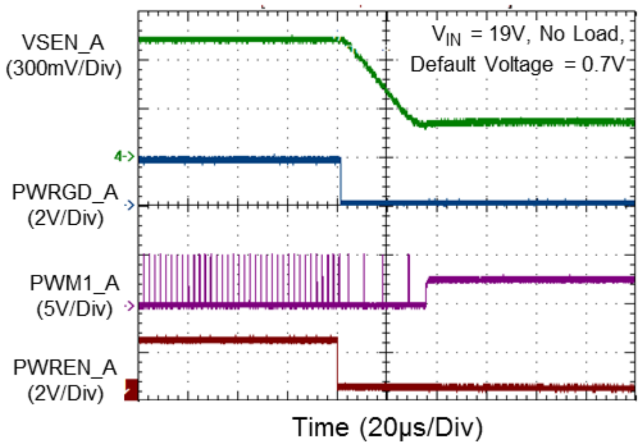


16 Typical Operating Characteristics

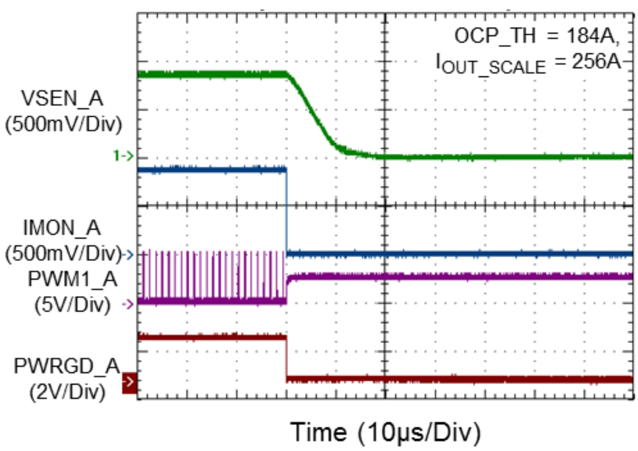
Rail A Power On from PWREN



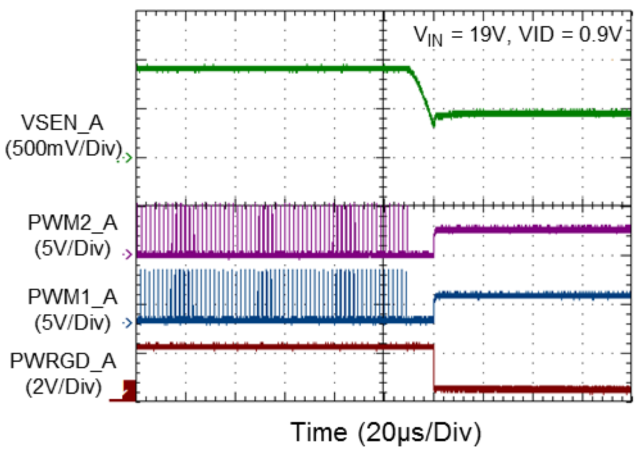
Rail A Power Off from PWREN



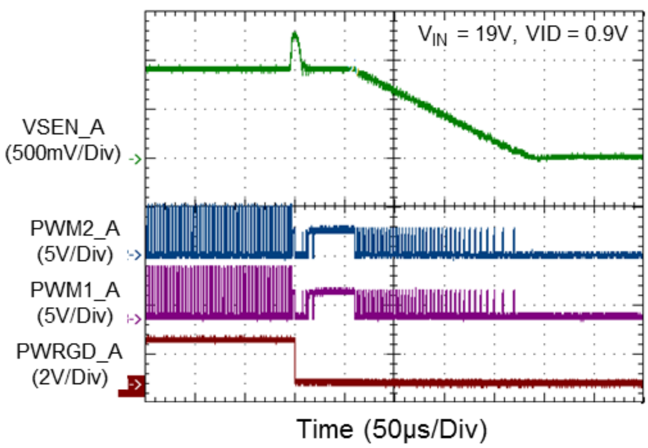
Rail A OCP



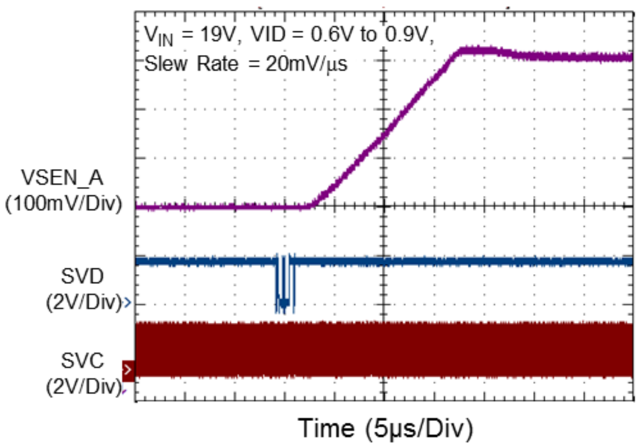
Rail A UVP



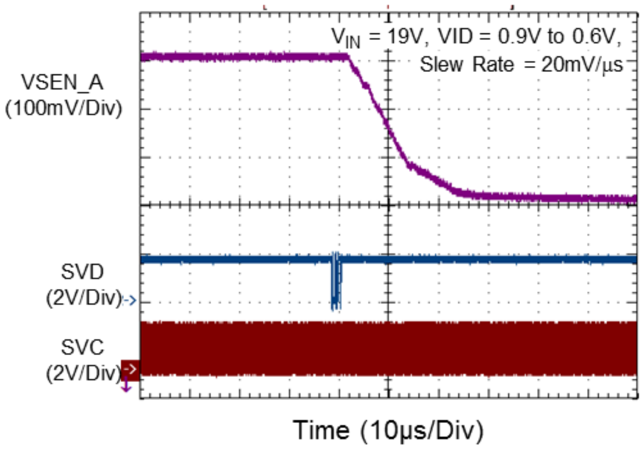
Rail A OVP



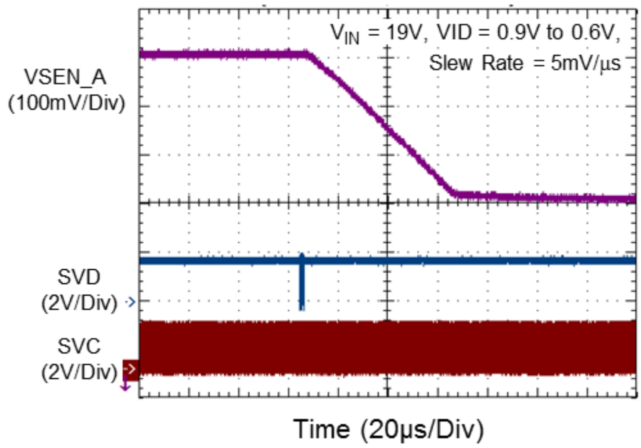
Rail A VOTF Up



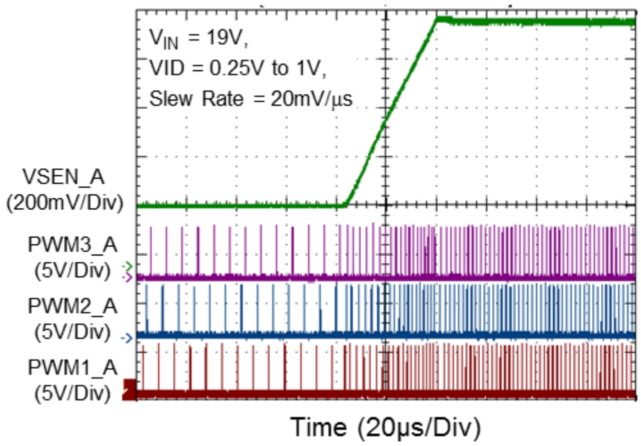
Rail A VOTF Down



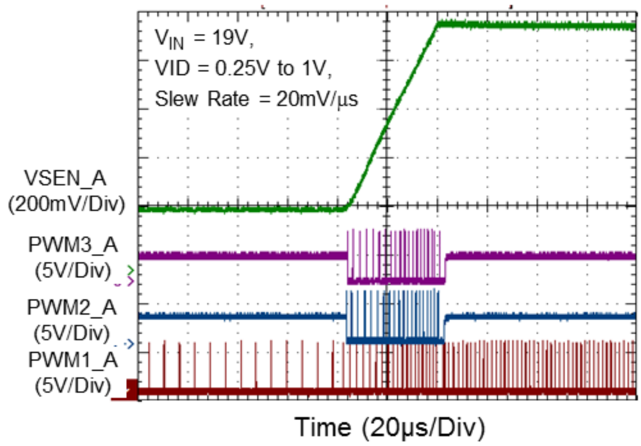
Rail A VOTF Slow Down



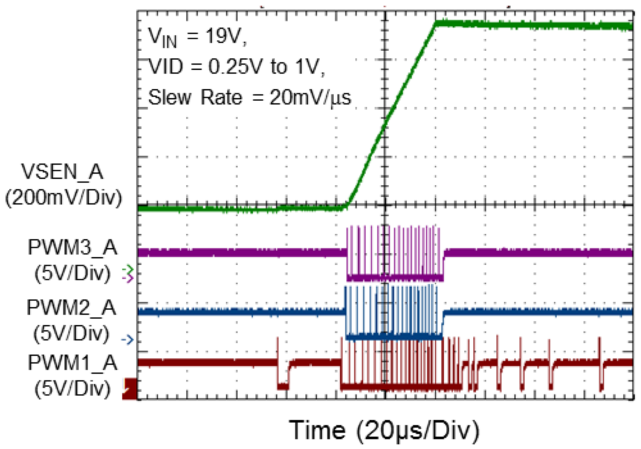
Rail A PSI0 Test



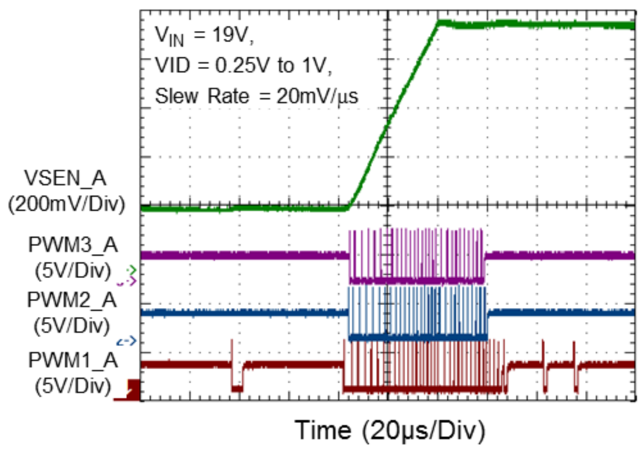
Rail A PSI1 Test



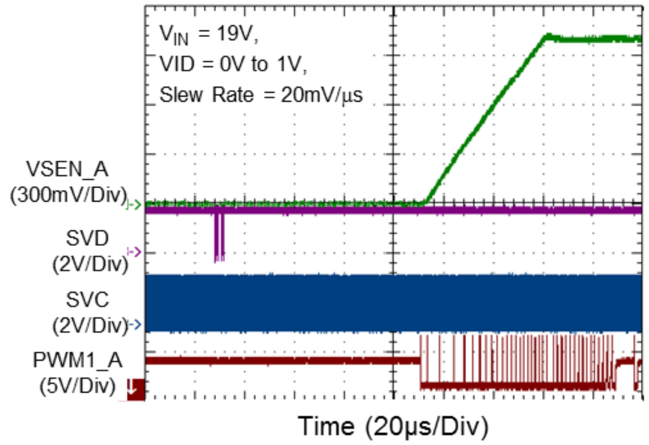
Rail A PSI3 Test



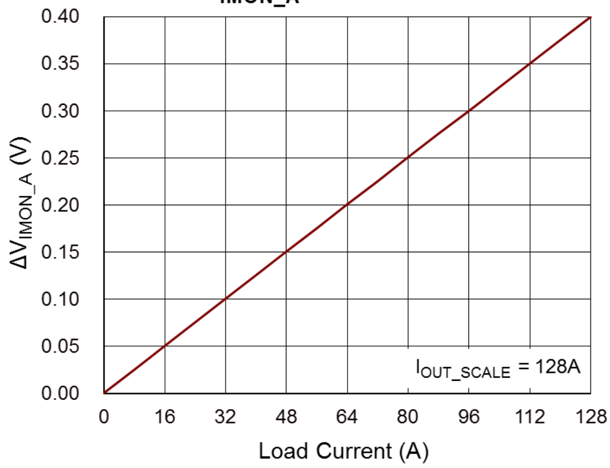
Rail A PSI7 Test



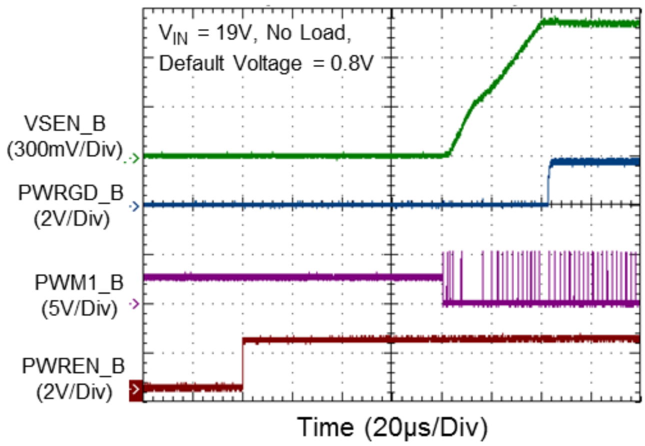
Rail A PSI6 Exit Time Test



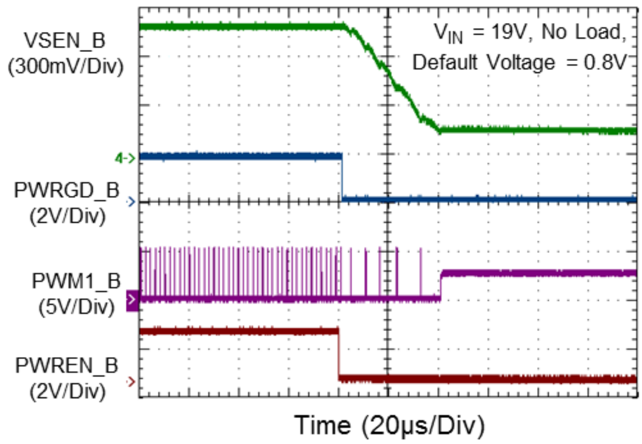
ΔV_{IMON_A} vs. Load Current



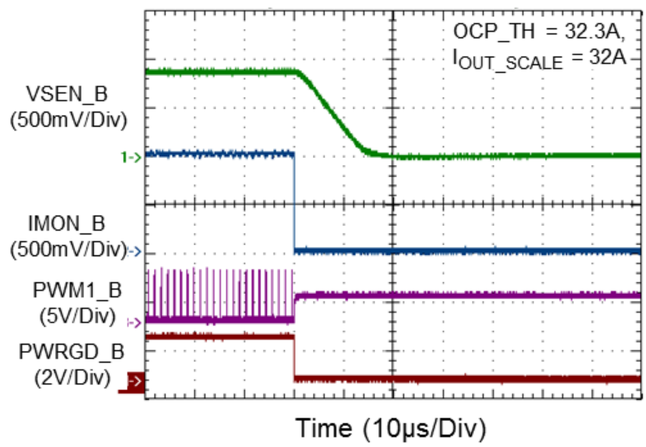
Rail B Power On from PWREN



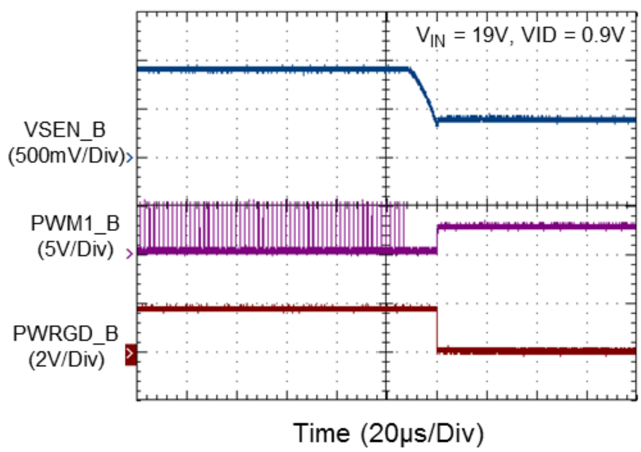
Rail B Power Off from PWREN



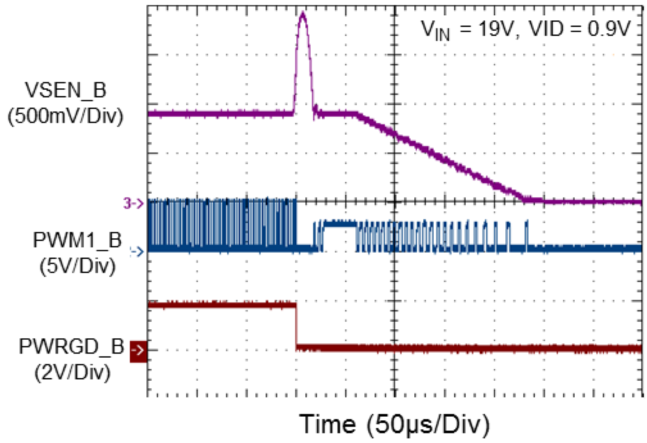
Rail B OCP



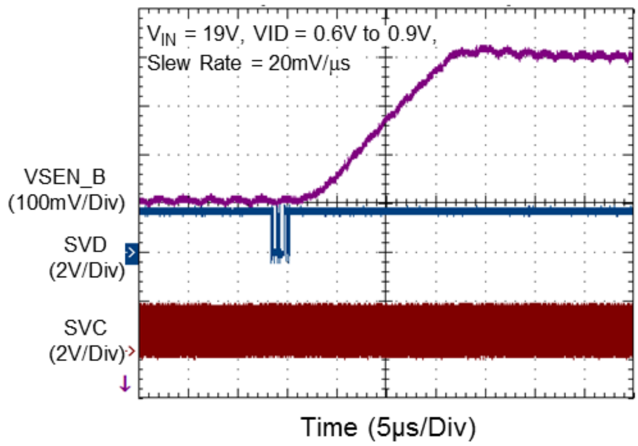
Rail B UVP



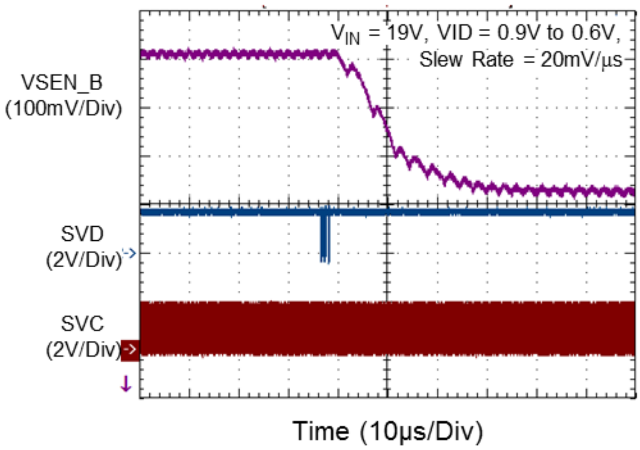
Rail B OVP



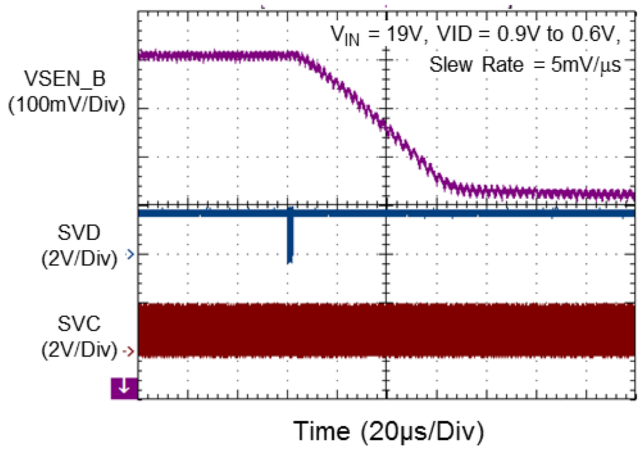
Rail B VOTF Up



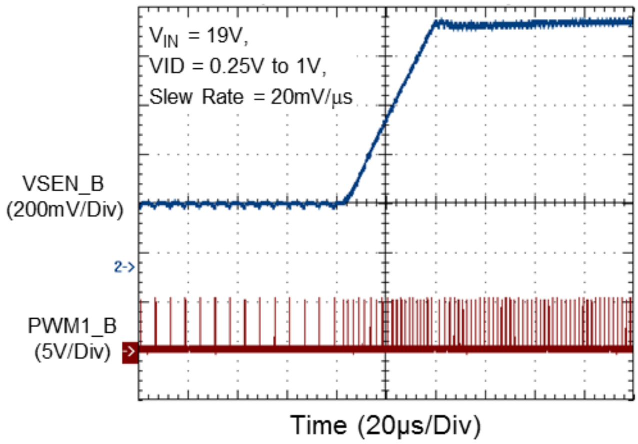
Rail B VOTF Down



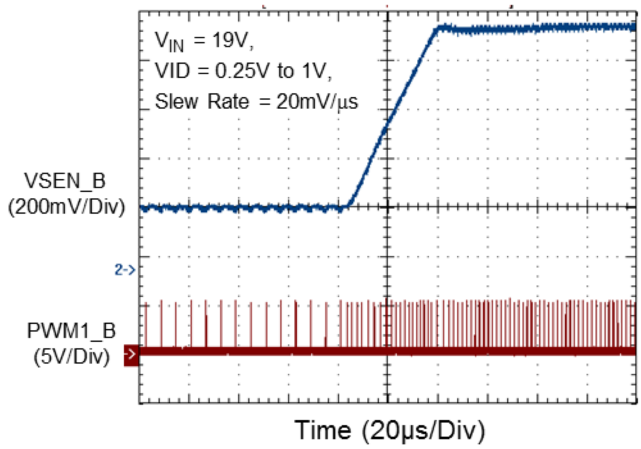
Rail B VOTF Slow Down



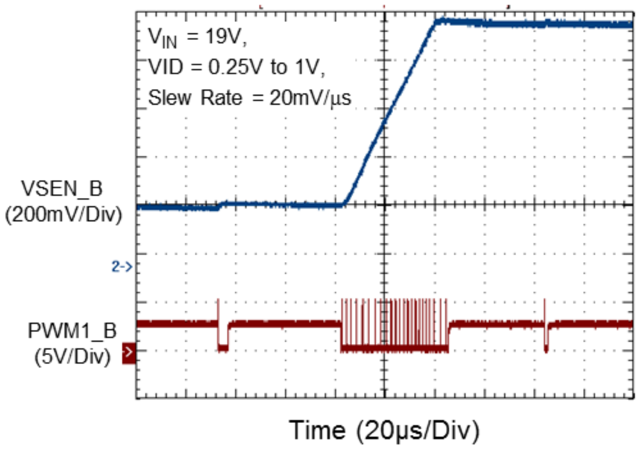
Rail B PSI0 Test



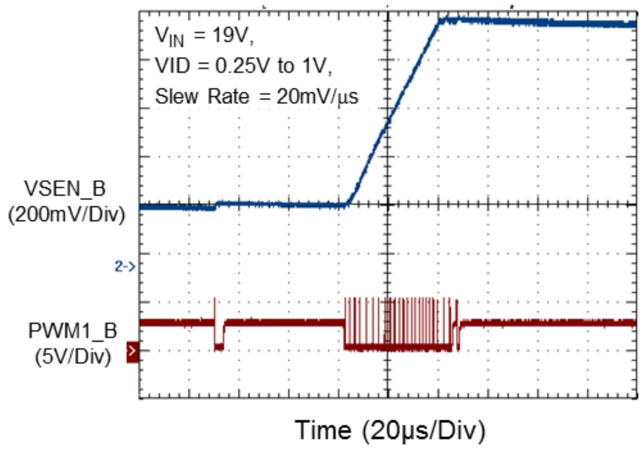
Rail B PSI1 Test



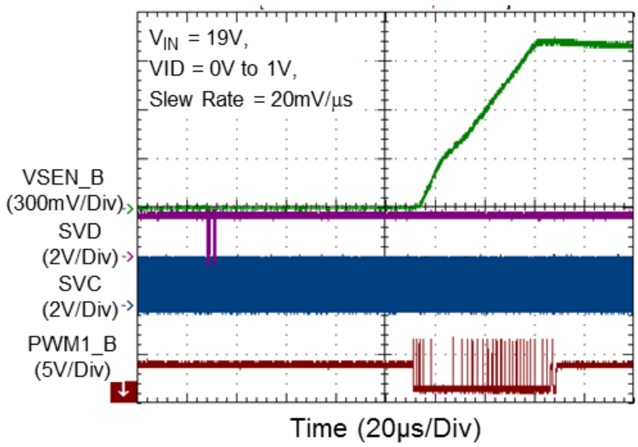
Rail B PSI3 Test



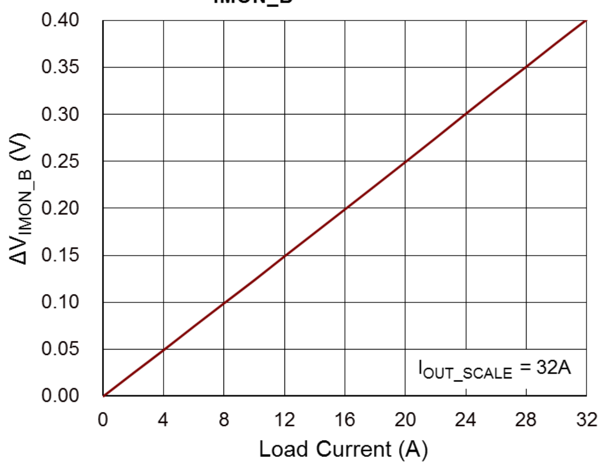
Rail B PSI7 Test



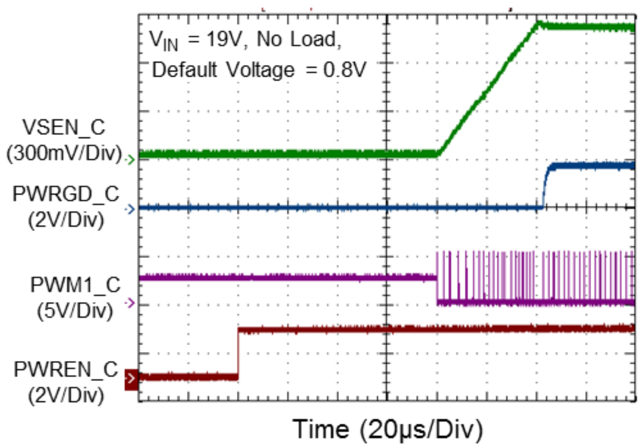
Rail B PSI6 Exit Time Test



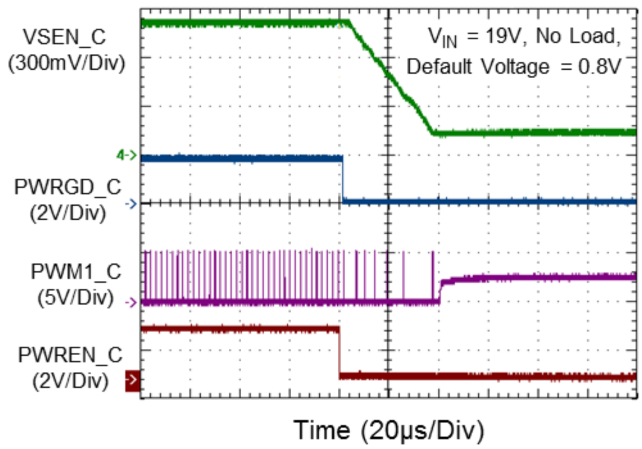
ΔV_{IMON_B} vs. Load Current



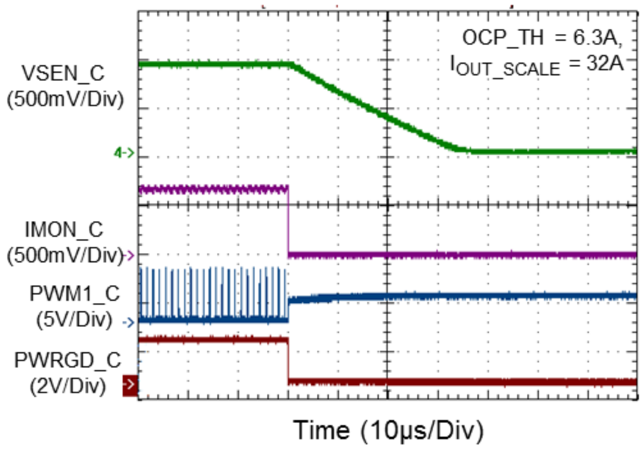
Rail C Power On from PWREN



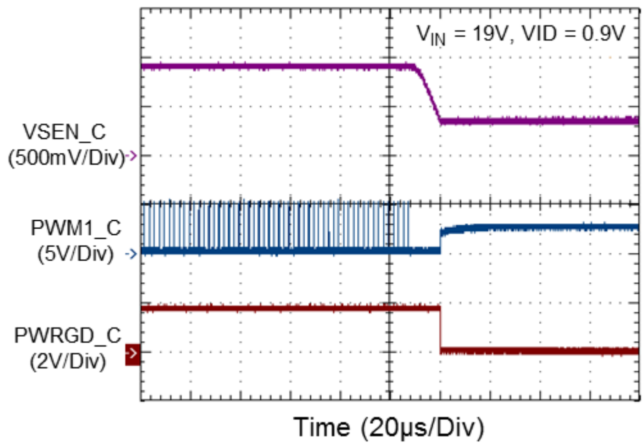
Rail C Power Off from PWREN



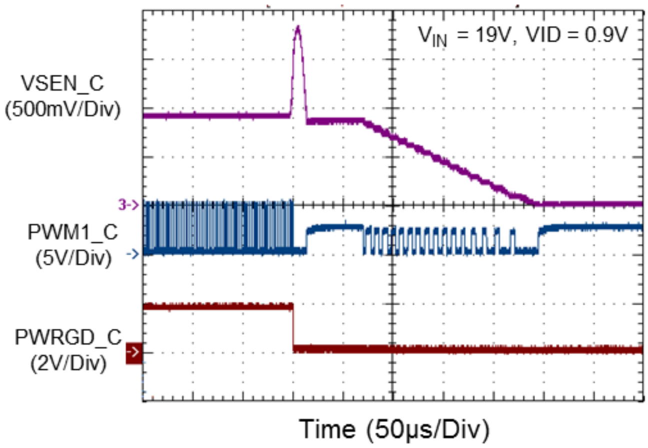
Rail C OCP



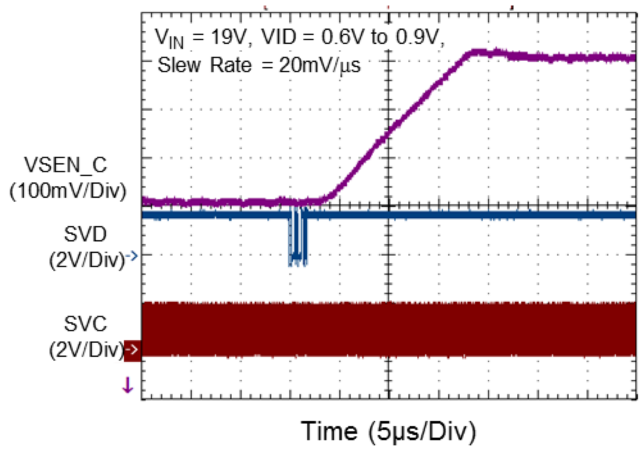
Rail C UVP



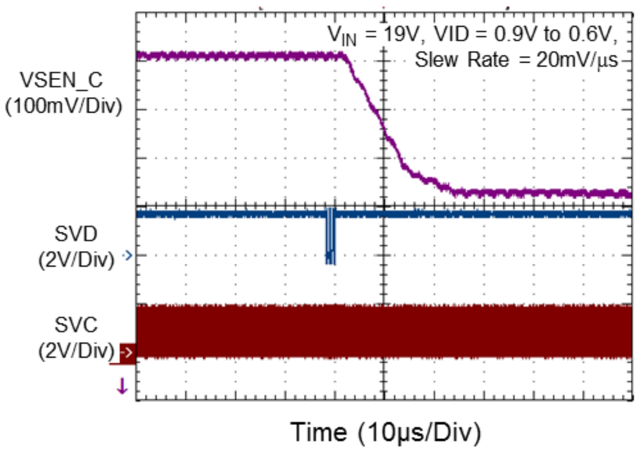
Rail C OVP



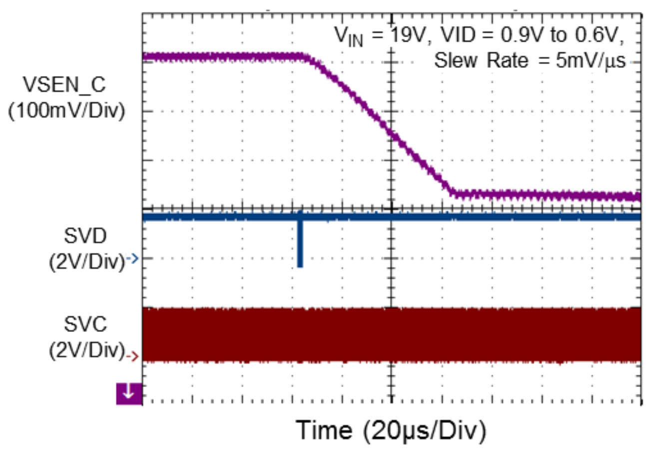
Rail C VOTF Up



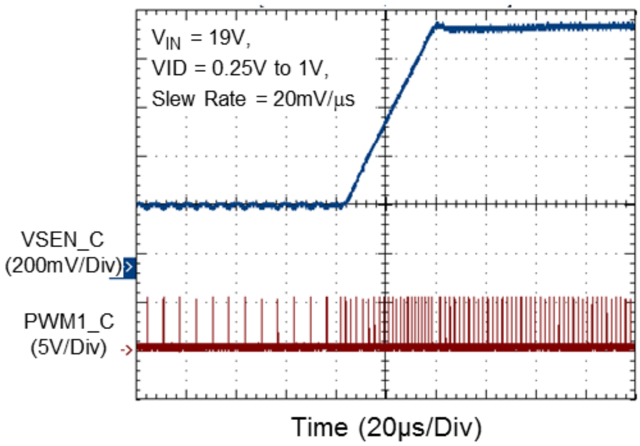
Rail C VOTF Down



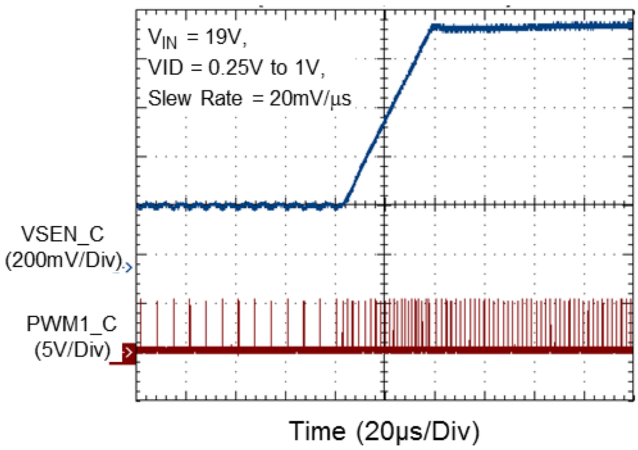
Rail C VOTF Slow Down



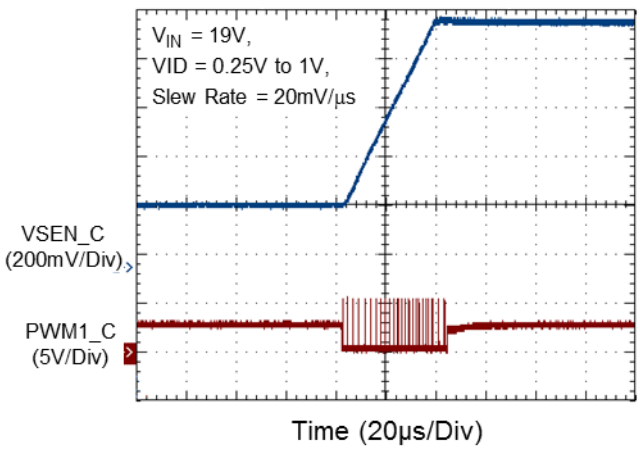
Rail C PSI0 Test



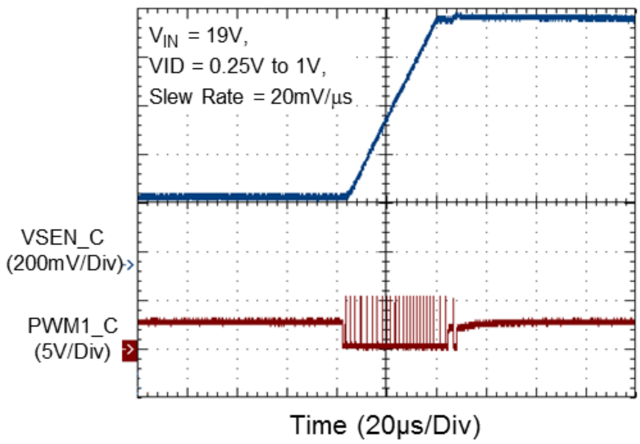
Rail C PSI1 Test



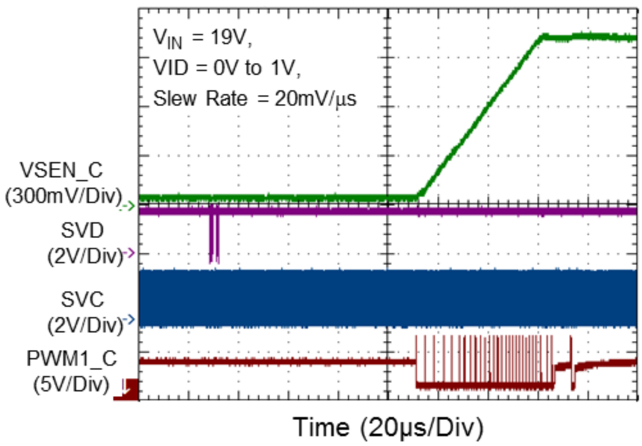
Rail C PSI3 Test



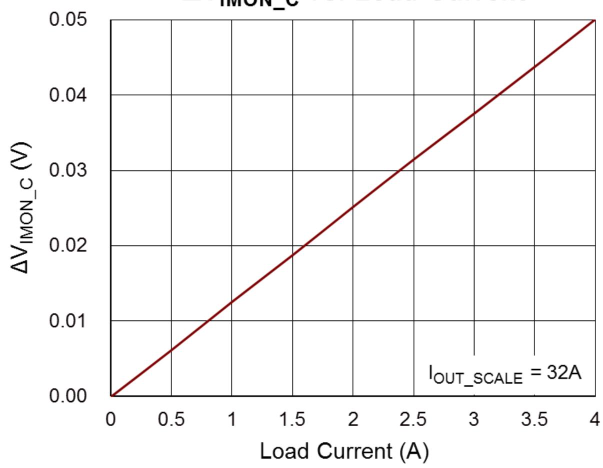
Rail C PSI7 Test



Rail C PSI6 Exit Time Test



ΔV_{IMON_C} vs. Load Current



17 Operation

17.1 G-NAVP Control Mode

The RT3674AJ adopts G-NAVP (Green Native AVP), which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3674AJ generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP behavior waveforms. The COMP signal is the sensed voltage inverted and amplified signal of the output voltage while the current loading increases. The COMP rises due to output voltage droop. Then, rising COMP forces PWM to turn on earlier and closely. While the inductor current reaches the load current, COMP enters another steady state at a higher voltage, and the corresponding output voltage is in the steady state at a lower voltage. The load-line, output voltage drooping proportional to load current, is achieved.

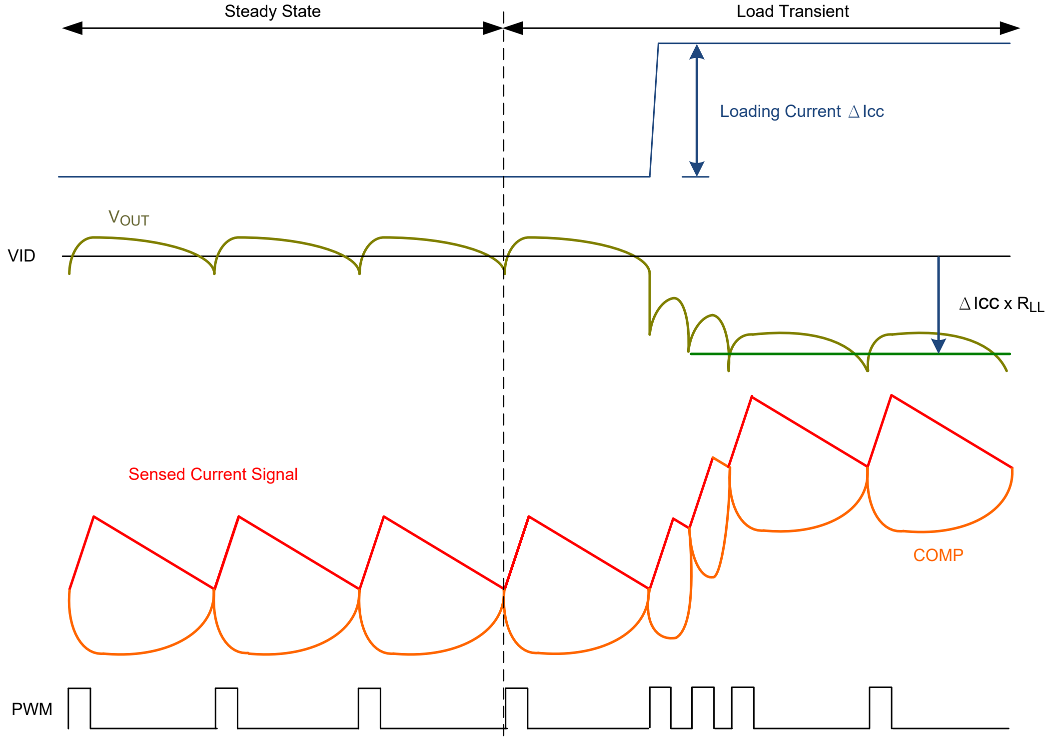


Figure 1. G-NAVP Behavior Waveform

17.2 SVI3 and I2C Interface/Control Logic/Configuration Registers

The SVI3 interface receives or transmits SVI3 signals from/to CPU/GPU. The I2C Interface receives or transmits I2C signals from/to SMBus. The control Logic executes commands (Read/Write/Reset registers, VID/Address packets, Change Power State, and Telemetry Request) and sends related signals to control the VR. Configuration Registers include function setting registers and CPU/GPU required registers.

17.3 IMON Filter

The IMON Filter is used to average the current signal using an analog low-pass filter. It outputs $IMON\_A_{AVG}$, $IMON\_B_{AVG}$, and $IMON\_C_{AVG}$ to the MUX of ADC for current reporting.

17.4 MUX and ADC

The MUX supports the inputs for TSEN_A, TSEN_B, TSEN_C, PSYS, $IMON\_A_{AVG}$, $IMON\_B_{AVG}$, and $IMON\_C_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

17.5 UVLO

The UVLO detects the VCC voltage. As VCC exceeds the threshold, the controller issues POR = high and waits PWREN. After both POR and PWREN are ready, then the controller is enabled.

17.6 Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

17.7 DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to VID packets command, Control Logic dynamically changes the VID voltage to the target voltage with required slew rate.

17.8 ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

17.9 PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting, and overcurrent protection.

17.10 SUM CSGM

The SUM CSGM senses the total inductor current with the RIMON gain adjustment. The SUM CSGM output current ratio can also be set by NVM. It helps wide application range of DCR and load-line. The SUM CSGM output is used for PWM trigger.

17.11 RAMP

The RAMP helps loop stability and transient response.

17.12 PWM CMP

The PWM comparator compares the COMP signal with sum current signal based on RAMP to trigger PWM.

17.13 Offset Cancellation

The offset cancellation is based on the VID, COMP voltage, and the current signal from SUM CSGM to control output voltage accurately.

17.14 Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

17.15 Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (anti-overshoot function).

17.16 AQR/ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) that detects loading rising edge and allows all PWMs to turn on. The PWM pulse width triggered by AQR is adaptive to load level. The AQR trigger level can be set by NVM. ANTIOVS can help overshoot reduction by detecting loading falling edge and forcing all PWMs in tri-state until the zero current is detected.

17.17 TONGEN/Driver Interface

The PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output, and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWM to turn on at the same time. Driver interface provides high/low/tri-state to drive external driver. In power-saving mode, the driver interface forces PWM in tri-state to turn off the high-side and low-side power MOSFETs according to the zero current detection output. In addition, the PWM state is controlled by protection logic. Different protections force required PWM state.

17.18 OVP/UVP/OCP

See Overvoltage Protection (OVP), Overcurrent Protection (OCP), and Undervoltage Protection.

18 Application Information

(Note 6)

The RT3674AJ includes three voltage rails: Rail A, a 4/3/2/1 phase synchronous buck controller; Rail B, a single-phase synchronous buck controller; and Rail C, another single-phase synchronous buck controller.

The RT3674AJ is designed to meet AMD SVI3 compatible CPUs specification. The controller features built-in non-volatile memory (NVM) and an I^2C interface to store customized configuration. The RT3674AJ is ideal for notebook computers or desktop computers.

18.1 Power-ON Sequence

To ensure sufficient power supply for proper operation, the VR triggers UVLO if the VCC voltage drops below 4.2V (maximum). The UVLO protection shuts down the controller and forces high-side MOSFET and low-side MOSFET off. Figure 2 shows the typical controller power-on timing. When VCC> VCC_POR_NVM, the RT3674AJ begins to download data to registers from NVM. When VCC > VCC_POR, the RT3674AJ starts initialization, which includes internal circuit offset correction and function settings. The maximum time from when VCC exceeds the VCC_POR threshold to completion of initialization is 7.6ms. Accordingly, the $t_{VCC\text{-}EN}$ is recommended to be larger than 8ms. When initialization is complete, the controller is in ultra-low power mode. It will ramp up to the default voltage with the default slew rate when PWREN is high. PWRGD is asserted within 5μs after the output voltage is within tolerance and start-up ramping is complete. Users can set multi-functions through NVM by the I^2C interface when initialization is complete.

It is strongly recommended that Driver power (PVCC) be ready after VCC. This can prevent current flowing back to VCC from PVCC through the PWMx pin or the DRVEN/DRVEN_F pin.

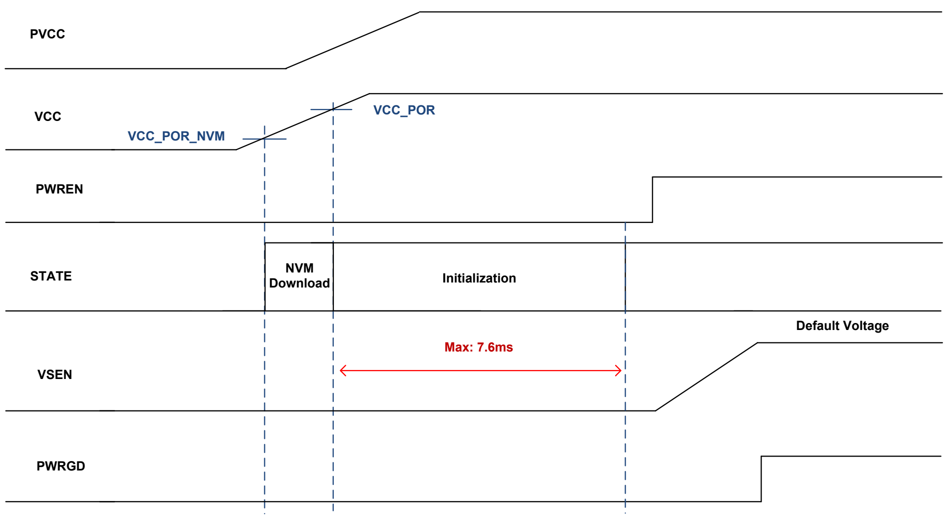


Figure 2. Typical Timing of Controller Power-ON

18.2 I²C Address Setting

The RT3674AJ provides multiple I²C addresses to support the use of multiple devices on the I²C interface. To properly set the I²C address (7-bit and 8-bit format), resistors with 1% tolerance must be connected from the CONFIG pin to ground and the resistor values are described in Table 1.

Table 1. I²C Address (7-Bit And 8-Bit Format) (HEX)

CONFIG		I²C Address (7-bit)	I²C Address (8-bit)
Max.	Min.		
325Ω	301Ω	20	40
975Ω	901Ω	21	42
1.625kΩ	1.501kΩ	22	44
2.275kΩ	2.101kΩ	23	46

18.3 Maximum Active Phases Number Setting

The number of active phases is determined by ISENxP voltages. The detection is only active and latched at initialization state. While voltage at ISENxP > (VCC – 0.5V), maximum active phase number is (x-1). For example, pulling ISEN4P_A to VCC programs a 3-phase operation, while pulling ISEN3P_A to VCC programs a 2-phase operation. The unused ISENxN pins are recommended to connect to VCC and the unused PWMx pins can be floating. Figure 3 is a 3-phase operation example. For smart power stage (SPS) application, the unused ISENxN pins must be floating.

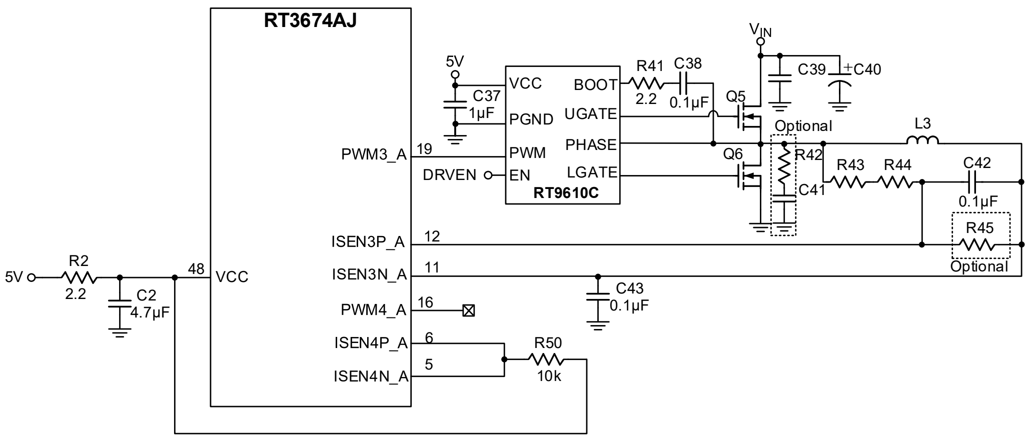


Figure 3. 3-Phases Operation Setting (For DCR Current Sense Application)

18.4 Rail Disable

Pulling ISEN1P_A to VCC disables rail A. The unused ISENxN_A pins are recommended to connect to VCC and the unused PWMx_A, VSEN_A, FB_A, COMP_A, IMON_A, TSEN_A, PWRGD_A, and PWREN_A pins can be floating. Pulling ISEN1P_B to VCC disables rail B. The unused ISEN1N_B pin should be connected to VCC, and the unused PWM1_B, VSEN_B, FB_B, COMP_B, IMON_B, TSEN_B, PWRGD_B, and PWREN_B pins can be floating. Pulling ISEN1P_C to VCC disables rail C. The unused ISEN1N_C pin should be connected to VCC and the unused PWM1_C, VSEN_C, FB_C, COMP_C, IMON_C, TSEN_C, PWRGD_C, and PWREN_C pins can be floating.

18.5 Acoustic Noise Suppression

The RT3674AJ supports an acoustic noise suppression function for reducing acoustic noise induced by the piezoelectric effect from MLCC. During output voltage transitions, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band, and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3674AJ adopts acoustic noise suppression function, which is enabled by pulling the ANS_EN pin to VCC to reduce ΔV when Negative VID transitions.

18.6 NVM Configuration Mechanism

The RT3674AJ provides multiple parameters for platform settings and BOM optimization. These parameters can be set through NVM by the I^2C protocol interface. Richtek provides a Microsoft Excel-based design tool for user configuration and provide programing flowchart for customers. All setting functions are summarized in Table 2. Table 3 shows the functions that do not support on-line tuning.

Table 2. Summary of Setting Functions (Page 02) (Group 1)

Register Map (Page 02)

Register Address	NAME	Type	PAGED	Default Value	NVM
00h	PWM_TRI_SLAVE_SEQ	R/W	Yes	0x09	Yes(GP1)
01h	SSOCP_RATIO	R/W	Yes	0x04	Yes(GP1)
02h	DEFAULT_VOLTAGE_SR_A	R/W	Yes	0x38	Yes(GP1)
03h	OCP_TH_A	R/W	Yes	0x5C	Yes(GP1)
04h	OCP_WARN_TH_A	R/W	Yes	0x5C	Yes(GP1)
05h	OCP_MIN_PULSE_DELAY_A	R/W	Yes	0x37	Yes(GP1)
06h	AQR_INC_A	R/W	Yes	0x4A	Yes(GP1)
07h	EN_0LL_SSOCP_ANTIOVS_A	R/W	Yes	0x40	Yes(GP1)
08h	DBLR_Ai_A	R/W	Yes	0x30	Yes(GP1)
09h	LPF_LIMIT_A	R/W	Yes	0x23	Yes(GP1)
0Ah	KTON_A	R/W	Yes	0x05	Yes(GP1)
0Bh	SPM_DROP_HYS_TH	R/W	Yes	0x0A	Yes(GP1)
0Ch	SPM_4PH_TH	R/W	Yes	0x24	Yes(GP1)
0Dh	SPM_3PH_TH	R/W	Yes	0x1A	Yes(GP1)
0Eh	SPM_2PH_TH	R/W	Yes	0x12	Yes(GP1)
0Fh	DEFAULT_VOLTAGE_SR_B	R/W	Yes	0x48	Yes(GP1)
10h	OCP_TH_B	R/W	Yes	0x81	Yes(GP1)
11h	OCP_WARN_TH_B	R/W	Yes	0x81	Yes(GP1)
12h	OCP_MIN_PULSE_DELAY_B	R/W	Yes	0x37	Yes(GP1)
13h	LPF_LIMIT_FLRAMP_B	R/W	Yes	0x23	Yes(GP1)
14h	Ai_ANTIOVS_B	R/W	Yes	0x00	Yes(GP1)
15h	AQR_TH_B	R/W	Yes	0x02	Yes(GP1)
16h	SRKTON_KTON_B	R/W	Yes	0x37	Yes(GP1)
17h	DEFAULT_VOLTAGE_SR_C	R/W	Yes	0x48	Yes(GP1)
18h	OCP_TH_C	R/W	Yes	0x19	Yes(GP1)

Register Address	NAME	Type	PAGED	Default Value	NVM
19h	OCP_WARN_TH_C	R/W	Yes	0x19	Yes(GP1)
1Ah	OCP_MIN_PULSE_DELAY_C	R/W	Yes	0x37	Yes(GP1)
1Bh	LPF_LIMIT_FLRAMP_C	R/W	Yes	0x43	Yes(GP1)
1Ch	Ai_ANTIOVS_C	R/W	Yes	0x12	Yes(GP1)
1Dh	AQR_TH_C	R/W	Yes	0x12	Yes(GP1)
1Eh	SRKTON_KTON_C	R/W	Yes	0x37	Yes(GP1)
1Fh	TSEN_SPS	R/W	Yes	0x00	Yes(GP1)
20h	PSYS	R/W	Yes	0x02	Yes(GP1)
21h	I_OUT_SCALE	R/W	Yes	0x54	Yes(GP1)
22h	SLL_RATIO_ZCD_A	R/W	Yes	0x02	Yes(GP1)
23h	Reserved	R/W	Yes	0xE1	Yes(GP1)
25h	AQR_TH_A	R/W	Yes	0x23	Yes(GP1)
26h	Reserved	R/W	Yes	0x70	Yes(GP1)
28h	INC_TON_TH_A	R/W	Yes	0x20	Yes(GP1)
29h	AR_AQR_1PH_A	R/W	Yes	0x1F	Yes(GP1)
2Bh	Reserved	R/W	Yes	0xE0	Yes(GP1)
2Ch	QR_WD_1PH_A	R/W	Yes	0xB1	Yes(GP1)
2Dh	VOTF_LIFT_TH_A	R/W	Yes	0x01	Yes(GP1)
2Eh	SLL_RATIO_ZCD_B	R/W	Yes	0x14	Yes(GP1)
2Fh	Reserved	R/W	Yes	0x71	Yes(GP1)
30h	AR_TH_B	R/W	Yes	0x52	Yes(GP1)
31h	INC_TON_B	R/W	Yes	0x00	Yes(GP1)
32h	VOTF_LIFT_TH_B	R/W	Yes	0x00	Yes(GP1)
33h	QR_WD_B	R/W	Yes	0x21	Yes(GP1)
34h	EN_0LL_DBLR_SSOCP_AEAGM_B	R/W	Yes	0x27	Yes(GP1)
35h	SLL_RATIO_ZCD_C	R/W	Yes	0x24	Yes(GP1)
36h	Reserved	R/W	Yes	0x71	Yes(GP1)
37h	AR_TH_C	R/W	Yes	0x42	Yes(GP1)
38h	INC_TON_C	R/W	Yes	0x1B	Yes(GP1)
39h	VOTF_LIFT_TH_C	R/W	Yes	0x13	Yes(GP1)
3Ah	QR_WD_C	R/W	Yes	0x21	Yes(GP1)
3Bh	EN_0LL_DBLR_SSOCP_AEAGM_C	R/W	Yes	0xA7	Yes(GP1)
3Ch	Reserved	R/W	Yes	0x11	Yes(GP1)
3Dh	Reserved	R/W	Yes	0x11	Yes(GP1)
3Eh	IOUT_TELEMETRY_OFFSET_A	R/W	Yes	0x00	Yes(GP1)
3Fh	IOUT_TELEMETRY_OFFSET_B	R/W	Yes	0x00	Yes(GP1)
40h	IOUT_TELEMETRY_OFFSET_C	R/W	Yes	0x00	Yes(GP1)
41h	CODE_VERSION_LSB	R/W	Yes	0x00	Yes(GP1)

Register Address	NAME	Type	PAGED	Default Value	NVM
42h	CODE_VERSION_MSB	R/W	Yes	0x00	Yes(GP1)
43h	Group1 CRC-8 Code	R	YES	Current status	NO

Register Address	Bits	Symbol	Description
0x00	[7:5]	RESERVED	Reserved bit
	[4]	PWM TRI-STATE LEVEL	**Set PWM tri-state level within DrMOS tri-state window.** [4] = 0: PWM tri-state level is 1.6V to 2.2V. [4] = 1: PWM tri-state level is 1.4V to 2.1V.
	[3:0]	SLAVE SEQUENCE	**Set slave1, slave2 and slave3 sequence.** [3:0] = 1001: A-B-C, [3:0] = 1010: A-C-B, [3:0] = 1011: B-A-C, [3:0] = 1100: B-C-A, [3:0] = 1101: C-A-B, [3:0] = 1110: C-B-A. [3:0] = 0000 to 1000 and 1111: Reserved, all other combinations are not defined.
0x01	[7]	RESERVED	Reserved bit
	[6:4]	SSOCP_RATIO_A	**Soft-start overcurrent protection ratio of rail A.** SSOCP_TH_A = I_OUT_SCALE_A×SSOCP_RATIO_A [6:4] = 000: SSOCP_RATIO_A = 1.25, [6:4] = 001: SSOCP_RATIO_A = 1.875, [6:4] = 010: SSOCP_RATIO_A = 2.1875, [6:4] = 011: SSOCP_RATIO_A = 2.5, [6:4] = 100: SSOCP_RATIO_A = 3.125, [6:4] = 101: SSOCP_RATIO_A = 3.75, [6:4] = 110: SSOCP_RATIO_A = 4.375, [6:4] = 111: SSOCP_RATIO_A = 5.
	[3:2]	SSOCP_RATIO_B	**Soft-start overcurrent protection ratio of rail B.** SSOCP_TH_B = I_OUT_SCALE_B×SSOCP_RATIO_B [3:2] = 00: SSOCP_RATIO_B = 1.25, [3:2] = 01: SSOCP_RATIO_B = 2.5, [3:2] = 10: SSOCP_RATIO_B = 5, [3:2] = 11: SSOCP_RATIO_B = 6.
	[1:0]	SSOCP_RATIO_C	**Soft-start overcurrent protection ratio of rail C.** SSOCP_TH_C = I_OUT_SCALE_C×SSOCP_RATIO_C [1:0] = 00: SSOCP_RATIO_C = 1.25, [1:0] = 01: SSOCP_RATIO_C = 2.5, [1:0] = 10: SSOCP_RATIO_C = 5, [1:0] = 11: SSOCP_RATIO_C = 6.
0x02	[7:4]	VID_DEFAULT_VOLTAGE_A	**Default voltage setting of rail A. SVI3 register 0x08[3:0].** [7:4] = 0000: VBOOT = 0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_A	**Default slew rate setting of rail A. SVI3 register 0x08[5:4].** [3:2] = 00: SR = 2.5mV/μs, [3:2] = 01: SR = 10mV/μs, [3:2] = 10: SR = 20mV/μs, [3:2] = 11: SR = 40mV/μs.
	[1:0]	RESERVED	Reserved bit

Register Address	Bits	Symbol	Description
0x03	[7:0]	OCP_THRESH_A	**Overcurrent protection threshold level of rail A. SVI3 register 0x27[7:0].** [7:0] = 00h: Disabled (no OCP) OCP_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x04	[7:0]	OCP_WARN_THRESH_A	**Overcurrent warning threshold level of rail A. SVI3 register 0x28[7:0].** [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x05	[7:3]	OCP_WARN_MIN_PULSE_A	**Minimum asserted pulse width of OCP_WARN signal of rail A. SVI3 register 0x29[7:3].** Minimum pulse(ns) = [7:3]×500
	[2:0]	OCP_FAULT_DELAY_A	**Set continuous time that current must exceed OCP_THRESH_A before triggering fault. SVI3 register 0x29[2:0]** [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]×5
0x06	[7]	EN_EXTEND_TON_A	**Enable/Disable Extend T_{ON} width of rail A.** [7] = 0: Disable, [7] = 1: Enable.
	[6]	ADPTV_FIX_QR_A	**Selection kind of QR in multi-phase of rail A.** [6] = 0: Fixed QR [6] = 1: Adaptive-QR(AQR).
	[5:4]	RESERVED	Reserved bit
	[3:2]	SEL_EXTD_TON_WD_A	**Selection extend T_{ON} width of rail A** [3:2] = 00: 1.625 x T_{ON}, [3:2] = 01: 1.5 x T_{ON}, [3:2] = 10: 1.375 x T_{ON}, [3:2] = 11: 1.25 x T_{ON}
	[1:0]	QR_WD_A	**Setting fixed QR width in multi-phase of rail A.** [1:0] = 00: 0.5×T_{ON}, [1:0] = 01: 0.75×T_{ON}, [1:0] = 10: 1.0×T_{ON}, [1:0] = 11: 1.25×T_{ON}.
0x07	[7]	EN_0LL_A	**Enable zero load-line of rail A.** [7] = 0: Disable 0LL. [7] = 1: Enable 0LL.
	[6]	EN_SSOCP_A	**Enable/Disable SSOCP function of rail A.** [6] = 0: Disable, [6] = 1: Enable
	[5]	RESERVED	Reserved bit
	[4]	EN_VOTF_ANTIOVS_A	**Enable/Disable ANTIOVS function when VOTF of rail A.** [4] = 0: Disable, [4] = 1: Enable
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_A	**ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail A.** [2:0] = 000: 120mV, [2:0] = 001: 180mV, [2:0] = 010: 240mV, [2:0] = 011: 300mV, [2:0] = 100: 360mV, [2:0] = 101: 420mV, [2:0] = 110: 480mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x08	[7]	RESERVED	Reserved bit
	[6]	EN_DBLR_A	**Enable/Disable rail A phase double function.** [6] = 0: Disable, [6] = 1: Enable.
	[5:4]	SET_DBLR_PH_A	**Phase number selection of rail A when EN_DBLR_A is enabled.** [5:4] = 00: Phase = 5-phase extension, [5:4] = 01: Phase = 6-phase extension, [5:4] = 10: Phase = 7-phase extension, [5:4] = 11: Phase = 6/8 phase doubler.
	[3]	RESERVED	Reserved bit
	[2:0]	Ai_A	**Current gain setting of rail A.** [2:0] = 000: 0.25, [2:0] = 001: 0.50, [2:0] = 010: 0.75, [2:0] = 011: 1.00, [2:0] = 100: 0.125, [2:0] = 101: 0.375, [2:0] = 110: 0.625, [2:0] = 111: 0.875.
0x09	[7:4]	LPF_LIMIT_MPH_A	**High-frequency-ACLL voltage compensation threshold in multi-phase operation of rail A** LPF_LIMIT = 100mV+[7:4]×20mV
	[3:0]	LPF_LIMIT_1PH_A	**High-frequency-ACLL voltage compensation threshold in 1-phase operation of rail A** LPF_LIMIT = 50mV+[3:0]×10mV
0x0A	[7:5]	RESERVED	Reserved bit
	[4:0]	KTON_A	**On-time (T_{ON}) K Factor Setting of rail A.** **While Reg. Addr 0x0A[4] = 0,** KTON = 0.5+[3:0]×0.1 **While Reg. Addr 0x0A[4] = 1,** KTON = 1.2+[3:0]×0.1
0x0B	[6:0]	SPM_DROP_HYS_TH	**Set Smart Phase Management (SPM) drop hysteresis of rail A.** 1LSB = I_OUT_SCALE/192 A
0x0C	[7:0]	SPM_4PH_TH	**Set Smart Phase Management (SPM) 3-phase to 4-phase threshold.** 1LSB = I_OUT_SCALE/192 A
0x0D	[7:0]	SPM_3PH_TH	**Set Smart Phase Management (SPM) 2-phase to 3-phase threshold.** 1LSB = I_OUT_SCALE/192 A
0x0E	[7:0]	SPM_2PH_TH	**Set Smart Phase Management (SPM) 1-phase to 2-phase threshold.** 1LSB = I_OUT_SCALE/192 A

Register Address	Bits	Symbol	Description
0x0F	[7:4]	VID_DEFAULT_VOLTAGE_B	**Default voltage setting of rail B. SVI3 register 0x08[3:0].** [7:4] = 0000: VBOOT = 0.0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_B	**Default slew rate setting of rail B. SVI3 register 0x08[5:4].** [3:2] = 00: SR = 2.5mV/μs, [3:2] = 01: SR = 10mV/μs, [3:2] = 10: SR = 20mV/μs, [3:2] = 11: SR = 40mV/μs.
	[1:0]	RESERVED	Reserved bit
0x10	[7:0]	OCP_THRESH_B	**Overcurrent protection threshold level of rail B. SVI3 register 0x27[7:0].** [7:0] = 00h: Disabled (no OCP) OCP_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x11	[7:0]	OCP_WARN_THRESH_B	**Overcurrent warning threshold level of rail B. SVI3 register 0x28[7:0].** [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x12	[7:3]	OCP_WARN_MIN_PULSE_B	**Minimum asserted pulse width of OCP_WARN signal of rail B. SVI3 register 0x29[7:3].** Minimum pulse(ns) = [7:3]×500
	[2:0]	OCP_FAULT_DELAY_B	**Set continuous time that current must exceed OCP_THRESH_B before triggering fault. SVI3 register 0x29[2:0]** [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]×5
0x13	[7]	RESERVED	Reserved bit
	[6:4]	LPF_LIMIT_B	**High-frequency-ACLL voltage compensation threshold of rail B.** [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3]	RESERVED	Reserved bit
	[2:0]	FLRAMP_TH_B	**Select floating ramp threshold of rail B.** [2:0] = 000: 25mV, [2:0] = 001: 75mV, [2:0] = 010: 125mV, [2:0] = 011: Disable, [2:0] = 100: 50mV, [2:0] = 101: 100mV, [2:0] = 110: 150mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x14	[7]	RESERVED	Reserved bit
	[6:4]	Ai_B	**Current gain setting of rail B.** Ai_B = 0.125+[6:4]x0.125
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_B	**ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail B.** [2:0] = 000: 90mV, [2:0] = 001: 120mV, [2:0] = 010: 150mV, [2:0] = 011: 180mV, [2:0] = 100: 210mV, [2:0] = 101: 240mV, [2:0] = 110: Disable, [2:0] = 111: Disable.
0x15	[7:5]	RESERVED	Reserved bit
	[4:0]	AQR_TH_B	**AQR starting trigger threshold of rail B.** [4:0] = 00h: 240mV, [4:0] = 01h: 320mV, [4:0] = 02h: 400mV, [4:0] = 03h: 480mV, [4:0] = 04h: 560mV, [4:0] = 05h: 640mV, [4:0] = 06h: 720mV, [4:0] = 07h: 800mV, [4:0] = 08h: 880mV, [4:0] = 09h: 960mV, [4:0] = 0Ah: 1040mV, [4:0] = 0Bh: 1120mV, [4:0] = 0Ch: 1200mV, [4:0] = 0Dh: 1280mV, [4:0] = 0Eh: Disable, [4:0] = 0Fh: Disable, [4:0] = 10h: 720mV, [4:0] = 11h: 800mV, [4:0] = 12h: 880mV, [4:0] = 13h: 960mV, [4:0] = 14h: 1040mV, [4:0] = 15h: 1120mV, [4:0] = 16h: 1200mV, [4:0] = 17h: 1280mV, [4:0] = 18h: 1360mV, [4:0] = 19h: 1440mV, [4:0] = 1Ah: 1520mV, [4:0] = 1Bh: 1600mV, [4:0] = 1Ch: 1680mV, [4:0] = 1Dh: 1760mV, [4:0] = 1Eh: Disable, [4:0] = 1Fh: Disable.
0x16	[7:6]	RESERVED	[7:6] = 00. All other combinations are not defined.
	[5:4]	SRKTON_PSI3_B	**Shrink T_{ON} in PSI3 of rail B.** [5:4] = 00: 85%, [5:4] = 01: 75%, [5:4] = 10: 66%, [5:4] = 11: 100%(Disable).
	[3:0]	KTON_B	**On-time (T_{ON}) K Factor Setting of rail B.** [3:0] = 0000: 0.73, [3:0] = 0001: 0.82, [3:0] = 0010: 0.91, [3:0] = 0011: 1.00, [3:0] = 0100: 1.09, [3:0] = 0101: 1.18, [3:0] = 0110: 1.27, [3:0] = 0111: 1.36, [3:0] = 1000: 1.55, [3:0] = 1001: 1.64, [3:0] = 1010: 1.73, [3:0] = 1011: 1.82, [3:0] = 1100: 2.00, [3:0] = 1101: 2.18, [3:0] = 1110: 2.36, [3:0] = 1111: 2.55.

Register Address	Bits	Symbol	Description
0x17	[7:4]	VID_DEFAULT_VOLTAGE_C	**Default voltage setting of rail C. SVI3 register 0x08[3:0].** [7:4] = 0000: VBOOT = 0.0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_C	**Default slew rate setting of rail C. SVI3 register 0x08[5:4].** [3:2] = 00: SR = 2.5mV/µs, [3:2] = 01: SR = 10mV/µs, [3:2] = 10: SR = 20mV/µs, [3:2] = 11: SR = 40mV/µs.
	[1:0]	RESERVED	Reserved bit
0x18	[7:0]	OCP_THRESH_C	**Overcurrent protection threshold level of rail C. SVI3 register 0x27[7:0].** [7:0] = 00h: Disabled (no OCP) OCP_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x19	[7:0]	OCP_WARN_THRESH_C	**Overcurrent warning threshold level of rail C. SVI3 register 0x28[7:0].** [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]×4×MAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x1A	[7:3]	OCP_WARN_MIN_PULSE_C	**Minimum asserted pulse width of OCP_WARN signal of rail C. SVI3 register 0x29[7:3].** Minimum pulse(ns) = [7:3]×500
	[2:0]	OCP_FAULT_DELAY_C	**Set continuous time that current must exceed OCP_THRESH_C before triggering fault. SVI3 register 0x29[2:0]** [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]×5
0x1B	[7]	RESERVED	Reserved bit
	[6:4]	LPF_LIMIT_C	**High-frequency-ACLL voltage compensation threshold of rail C.** [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3]	RESERVED	Reserved bit
	[2:0]	FLRAMP_TH_C	**Select floating ramp threshold of rail C.** [2:0] = 000: 25mV, [2:0] = 001: 75mV, [2:0] = 010: 125mV, [2:0] = 011: Disable, [2:0] = 100: 50mV, [2:0] = 101: 100mV, [2:0] = 110: 150mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x1C	[7]	RESERVED	Reserved bit
	[6:4]	Ai_C	**Current gain setting of rail C.** Ai_C = 0.125+[6:4]x0.125
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_C	**ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail C.** [2:0] = 000: 90mV, [2:0] = 001: 120mV, [2:0] = 010: 150mV, [2:0] = 011: 180mV, [2:0] = 100: 210mV, [2:0] = 101: 240mV, [2:0] = 110: Disable, [2:0] = 111: Disable.
0x1D	[7:5]	RESERVED	Reserved bit
	[4:0]	AQR_TH_C	**AQR starting trigger threshold of rail C.** [4:0] = 00h: 240mV, [4:0] = 01h: 320mV, [4:0] = 02h: 400mV, [4:0] = 03h: 480mV, [4:0] = 04h: 560mV, [4:0] = 05h: 640mV, [4:0] = 06h: 720mV, [4:0] = 07h: 800mV, [4:0] = 08h: 880mV, [4:0] = 09h: 960mV, [4:0] = 0Ah: 1040mV, [4:0] = 0Bh: 1120mV, [4:0] = 0Ch: 1200mV, [4:0] = 0Dh: 1280mV, [4:0] = 0Eh: Disable, [4:0] = 0Fh: Disable, [4:0] = 10h: 720mV, [4:0] = 11h: 800mV, [4:0] = 12h: 880mV, [4:0] = 13h: 960mV, [4:0] = 14h: 1040mV, [4:0] = 15h: 1120mV, [4:0] = 16h: 1200mV, [4:0] = 17h: 1280mV, [4:0] = 18h: 1360mV, [4:0] = 19h: 1440mV, [4:0] = 1Ah: 1520mV, [4:0] = 1Bh: 1600mV, [4:0] = 1Ch: 1680mV, [4:0] = 1Dh: 1760mV, [4:0] = 1Eh: Disable, [4:0] = 1Fh: Disable.

Register Address	Bits	Symbol	Description
0x1E	[7:6]	RESERVED	[7:6] = 00. All other combinations are not defined.
	[5:4]	SRKTON_PSI3_C	**Shrink T_{ON} in PSI3 of rail C.** [5:4] = 00: 85%, [5:4] = 01: 75%, [5:4] = 10: 66%, [5:4] = 11: 100%(Disable).
	[3:0]	KTON_C	**On-time (T_{ON}) K Factor Setting of rail C.** [3:0] = 0000: 0.73, [3:0] = 0001: 0.82, [3:0] = 0010: 0.91, [3:0] = 0011: 1.00, [3:0] = 0100: 1.09, [3:0] = 0101: 1.18, [3:0] = 0110: 1.27, [3:0] = 0111: 1.36, [3:0] = 1000: 1.55, [3:0] = 1001: 1.64, [3:0] = 1010: 1.73, [3:0] = 1011: 1.82, [3:0] = 1100: 2.00, [3:0] = 1101: 2.18, [3:0] = 1110: 2.36, [3:0] = 1111: 2.55.
0x1F	[7:6]	RESERVED	Reserved bit
	[5]	TSEN_C	**Temperature source selection for rail C.** [5] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [5] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0°C with an offset of 0.6V at 0°C.
	[4]	EN_SPS_C	**Enable/Disable rail C SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b.** [4] = 0: Disable (DCR or Rshunt), [4] = 1: Enable (SPS).
	[3]	TSEN_B	**Temperature source selection for rail B.** [3] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [3] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0°C with an offset of 0.6V at 0°C.
	[2]	EN_SPS_B	**Enable/Disable rail B SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b.** [2] = 0: Disable(DCR or Rshunt), [2] = 1: Enable (SPS).
	[1]	TSEN_A	**Temperature source selection for rail A.** [1] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [1] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0 °C with an offset of 0.6V at 0°C.
	[0]	EN_SPS_A	**Enable/Disable rail A SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b.** [0] = 0: Disable(DCR or Rshunt), [0] = 1: Enable (SPS).
0x20	[7:5]	RESERVED	Reserved bit
	[4]	P_SYS_MAX_Voltage	**PSYS voltage range selection.** [4] = 0: 1.6V, [4] = 1: 3.2V.
	[3]	RESERVED	Reserved bit
	[2:0]	P_SYS_SCALE	**System power scale. SVI3 register 0x0C[2:0].** [2:0] = 000: Custom Scale(Reserved), [2:0] = 001: Scale 1, [2:0] = 010: Scale 2, [2:0] = 011: Scale 3, [2:0] = 100: Scale 4, [2:0] = 101: Scale 5, [2:0] = 110: Scale 6, [2:0] = 111: Scale 7.

Register Address	Bits	Symbol	Description
0x21	[7:6]	I_OUT_SCALE_C	**Output current scale setting of rail C. SVI3 register 0x09[5:3].** [7:6] = 00: Custom Scale, [7:6] = 01: Scale1, [7:6] = 10: Scale2, [7:6] = 11: Scale3.
	[5:4]	I_OUT_SCALE_B	**Output current scale setting of rail B. SVI3 register 0x09[5:3].** [5:4] = 00: Custom Scale, [5:4] = 01: Scale1, [5:4] = 10: Scale2, [5:4] = 11: Scale3.
	[3]	RESERVED	Reserved bit
	[2:0]	I_OUT_SCALE_A	**Output current scale setting of rail A. SVI3 register 0x09[5:3].** [2:0] = 000: Custom Scale, [2:0] = 001: Scale1, [2:0] = 010: Scale2, [2:0] = 011: Scale3, [2:0] = 100: Scale4, [2:0] = 101: Scale5, [2:0] = 110: Scale6, [2:0] = 111: Scale7.
0x22	[7:6]	SLL_RATIO_A	**Short-term voltage target ratio of rail A for AC transient.** Short_term_voltage_target = VID-$\Delta I_{cc} \times R_{LL} \times$SLL_RATIO_A [7:6] = 00: 100%(Normal), [7:6] = 01: 95%, [7:6] = 10: 90%, [7:6] = 11: 50%.
	[5:0]	ZCD_TH_A	**Detect whether each phase current crosses zero current of rail A. Set trigger level.** [5]: sign bit, 0 is positive. [4:0]: 0.2083mV/step Ex. [5:0] = 01h, ZCD_TH_A = 0.2083mV. [5:0] = 00h or 20h, ZCD_TH_A = 0mV. [5:0] = 21h, ZCD_TH_A = -0.2083mV.
0x23	[7:0]	RESERVED	[7:0] = E1h. All other combinations are not defined.
0x25	[7:5]	RESERVED	[7:5] = 001. All other combinations are not defined.
	[4:0]	AQR_TH_A	**AQR starting trigger threshold in multi-phase operation of rail A.** [4:0] = 1Fh: Disabled AQR_TH = 240mV+[4:0]×80mV
0x26	[7:0]	RESERVED	[7:0] = 70h. All other combinations are not defined.
0x28	[7:6]	INC_TON_TH_A	**Setting increase T_{ON} threshold of rail A.** [7:6] = 00: 2.4V + 150mV, [7:6] = 01: 2.4V + 200mV, [7:6] = 10: 2.4V + 250mV, [7:6] = 11: 2.4V + 300mV.
	[5:0]	RESERVED	[5:0] = 20h. All other combinations are not defined.
0x29	[7:5]	AR_TH_1PH_A	**Adaptive ramp trigger threshold in 1-phase of rail A.** [7:5] = 000: 125mV, [7:5] = 001: 150mV, [7:5] = 010: 175mV, [7:5] = 011: Disable, [7:5] = 100: 200mV, [7:5] = 101: 225mV, [7:5] = 110: 250mV, [7:5] = 111: Disable,
	[4:0]	AQR_TH_1PH_A	**AQR starting trigger threshold in 1-phase operation of rail A.** [4:0] = 1Fh: Disabled AQR_TH = 40mV+[4:0]×40mV

Register Address	Bits	Symbol	Description
0x2B	[7:0]	RESERVED	RESERVED
0x2C	[7:6]	QR_WD_1PH_A	**Setting fixed QR width in 1-phase of rail A.** [7:6] = 00: 0.5xT_{ON}, [7:6] = 01: 0.75xT_{ON}, [7:6] = 10: 1.0xT_{ON}, [7:6] = 11: 1.25 x T_{ON}.
	[5:2]	RESERVED	[5:2] = 1100. All other combinations are not defined.
	[1:0]	Reset_LPF_TH_A	**Setting reset LPF threshold of rail A.** [1:0] = 00: 0.5µA, [1:0] = 01: 1.0µA, [1:0] = 10: 1.5µA, [1:0] = 11: 2.0µA.
0x2D	[7]	VOTF_LIFT_TH_A	Voltage on the Fly (VOTF) compensation during VOTF ramp up of Rail A. Refer to Reg. Addr 0x2D[3:0]
	[6:4]	RESERVED	Reserved bit
	[3:0]	VOTF_LIFT_TH_A	**Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail A.** **While Reg. Addr 0x2D[7] = 0,** [3:0] = 0000: Disable, [3:0] = 0001: 2µA, [3:0] = 0010: 3µA, [3:0] = 0011: 4µA, [3:0] = 0100: 5µA, [3:0] = 0101: 6µA, [3:0] = 0110: 7µA, [3:0] = 0111: 8µA, [3:0] = 1000: 9µA, [3:0] = 1001: 10µA, [3:0] = 1010: 12µA, [3:0] = 1011: 14µA, [3:0] = 1100: 16µA, [3:0] = 1101: 18µA, [3:0] = 1110: 20µA, [3:0] = 1111: 24µA, **While Reg. Addr 0x2D[7] = 1,** [3:0] = 0000: Disable, [3:0] = 0001: 1µA, [3:0] = 0010: 1.5µA, [3:0] = 0011: 2µA, [3:0] = 0100: 2.5µA, [3:0] = 0101: 3µA, [3:0] = 0110: 3.5µA, [3:0] = 0111: 4µA, [3:0] = 1000: 4.5µA, [3:0] = 1001: 5µA, [3:0] = 1010: 6µA, [3:0] = 1011: 7µA, [3:0] = 1100: 8µA, [3:0] = 1101: 9µA, [3:0] = 1110: 10µA, [3:0] = 1111: 12µA,
0x2E	[7:6]	SLL_RATIO_B	**Short-term voltage target ratio of rail B at AC transient .** Short_term_voltage_target = VID-ΔI_{cc}×R_{LL}×SLL_RATIO_B [7:6] = 00: 100%(Normal), [7:6] = 01: 84%, [7:6] = 10: 76%, [7:6] = 11: 60%.
	[5:0]	ZCD_TH_B	**Detect whether each phase current crosses zero current of rail B. Set trigger level.** ZCD_TH = -4mV+[5:0]×0.125mV Ex. [5:0] = 00h, ZCD_TH = -4mV [5:0] = 20h, ZCD_TH = 0mV [5:0] = 3Fh, ZCD_TH = 3.875mV
0x2F	[7:0]	RESERVED	[7:0] = 71h. All other combinations are not defined.
0x30	[7]	RESERVED	Reserved bit
	[6:4]	AR_TH_B	**Adaptive ramp trigger threshold of rail B.** [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3:0]	RESERVED	[3:0] = 2h. All other combinations are not defined.

Register Address	Bits	Symbol	Description
0x31	[7:5]	RESERVED	[7:5] = 000. All other combinations are not defined.
	[4]	EN_EXTEND_TON_B	**Enable/Disable Extend T_{ON} width of rail B.** [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	INC_TON_TH_B	**Setting increase T_{ON} threshold of rail B.** [3:2] = 00: 2.4V + 150mV, [3:2] = 01: 2.4V + 200mV, [3:2] = 10: 2.4V + 250mV, [3:2] = 11: 2.4V + 300mV.
	[1:0]	SEL_EXTD _TON_WD_B	**Selection extend T_{ON} width of rail B** [1:0] = 00: 2.66 x T_{ON}, [1:0] = 01: 2.00 x T_{ON}, [1:0] = 10: 1.60 x T_{ON}, [1:0] = 11: 1.33 x T_{ON}
0x32	[7:6]	RESERVED	Reserved bit
	[5:4]	VOTF_LIFT_TH_B	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail A. Refer to Reg. Addr 0x32[2:0]
	[3]	RESERVED	Reserved bit
	[2:0]	VOTF_LIFT_TH_B	**Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail B.** **While Reg. Addr 0x32[5:4] = 00,** [2:0] = 000: Disable, [2:0] = 001: 0.125μA, [2:0] = 010: 0.25μA, [2:0] = 011: 0.375μA, [2:0] = 100: 0.5μA, [2:0] = 101: 0.625μA, [2:0] = 110: 0.875μA, [2:0] = 111: 1.25μA. **While Reg. Addr 0x32[5:4] = 01,** [2:0] = 000: Disable, [2:0] = 001: 0.25μA, [2:0] = 010: 0.50μA, [2:0] = 011: 0.75μA, [2:0] = 100: 1.00μA, [2:0] = 101: 1.25μA, [2:0] = 110: 1.75μA, [2:0] = 111: 2.50μA. **While Reg. Addr 0x32[5:4] = 10,** [2:0] = 000: Disable, [2:0] = 001: 0.3125μA, [2:0] = 010: 0.625μA, [2:0] = 011: 0.9375μA, [2:0] = 100: 1.25μA, [2:0] = 101: 1.5625μA, [2:0] = 110: 2.1875μA, [2:0] = 111: 3.125μA. **While Reg. Addr 0x32[5:4] = 11,** [2:0] = 000: Disable, [2:0] = 001: 0.625μA, [2:0] = 010: 1.25μA, [2:0] = 011: 1.875μA, [2:0] = 100: 2.50μA, [2:0] = 101: 3.125μA, [2:0] = 110: 4.375μA, [2:0] = 111: 6.25μA.
0x33	[7:2]	RESERVED	[7:2] = 001000. All other combinations are not defined.
	[1:0]	QR_WD_B	**Setting QR width of rail B.** [1:0] = 00: 0.4×T_{ON}, [1:0] = 01: 0.55×T_{ON}, [1:0] = 10: 0.75×T_{ON}, [1:0] = 11: 0.92×T_{ON}.

Register Address	Bits	Symbol	Description
0x34	[7]	EN_0LL_B	**Enable zero load-line of rail B.** [7] = 0: Disable 0LL. [7] = 1: Enable 0LL.
	[6]	EN_DBLR_B	**Enable/Disable rail B phase double function.** [6] = 0: Disable, [6] = 1: Enable.
	[5]	EN_SSOCP_B	**Enable/Disable SSOCP function of rail B.** [5] = 0: Disable, [5] = 1: Enable
	[4]	AEAGM_B	**AEAGM gain setting of rail B.** [4] = 0: 2/3. [4] = 1: 1.
	[3:0]	RESERVED	[3:0] = 0110. All other combinations are not defined.
0x35	[7:6]	SLL_RATIO_C	**Short-term voltage target ratio of rail C at AC transient.** Short_term_voltage_target = VID-ΔI_{cc}×R_{LL}×SLL_RATIO_C [7:6] = 00: 100%(Normal), [7:6] = 01: 84%, [7:6] = 10: 76%, [7:6] = 11: 60%.
	[5:0]	ZCD_TH_C	**Detect whether each phase current crosses zero current of rail C. Set trigger level.** $\text{ZCD\_TH} = -4\text{mV} + [5:0] \times 0.125mV$ Ex. [5:0] = 00h, ZCD_TH = -4mV [5:0] = 20h, ZCD_TH = 0mV [5:0] = 24h, ZCD_TH = 0.5mV [5:0] = 3Fh, ZCD_TH = 3.875mV
0x36	[7:0]	RESERVED	[7:0] = 71h. All other combinations are not defined.
0x37	[7]	RESERVED	Reserved bit
	[6:4]	AR_TH_C	**Adaptive ramp trigger threshold of rail C.** [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3:0]	RESERVED	[3:0] = 2h. All other combinations are not defined.
0x38	[7:5]	RESERVED	[7:5] = 000. All other combinations are not defined.
	[4]	EN_EXTEND_TON_C	**Enable/Disable Extend T_{ON} width of rail C.** [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	INC_TON_TH_C	**Setting increase T_{ON} threshold of rail C.** [3:2] = 00: 2.4V + 150mV, [3:2] = 01: 2.4V + 200mV, [3:2] = 10: 2.4V + 250mV, [3:2] = 11: 2.4V + 300mV.
	[1:0]	SEL_EXTD _TON_WD_C	**Selection extend T_{ON} width of rail C** [1:0] = 00: 2.66 x T_{ON}, [1:0] = 01: 2.00 x T_{ON}, [1:0] = 10: 1.60 x T_{ON}, [1:0] = 11: 1.33 x T_{ON}

Register Address	Bits	Symbol	Description
0x39	[7:6]	RESERVED	Reserved bit
	[5:4]	VOTF_LIFT_TH_C	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail C. Refer to Reg. Addr 0x39[2:0]
	[3]	RESERVED	Reserved bit
	[2:0]	VOTF_LIFT_TH_C	**Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail C.** **While Reg. Addr 0x39[5:4] = 00,** [2:0] = 000: Disable, [2:0] = 001: 0.125μA, [2:0] = 010: 0.25μA, [2:0] = 011: 0.375μA, [2:0] = 100: 0.5μA, [2:0] = 101: 0.625μA, [2:0] = 110: 0.875μA, [2:0] = 111: 1.25μA. **While Reg. Addr 0x39[5:4] = 01,** [2:0] = 000: Disable, [2:0] = 001: 0.25μA, [2:0] = 010: 0.50μA, [2:0] = 011: 0.75μA, [2:0] = 100: 1.00μA, [2:0] = 101: 1.25μA, [2:0] = 110: 1.75μA, [2:0] = 111: 2.50μA. **While Reg. Addr 0x39[5:4] = 10,** [2:0] = 000: Disable, [2:0] = 001: 0.3125μA, [2:0] = 010: 0.625μA, [2:0] = 011: 0.9375μA, [2:0] = 100: 1.25μA, [2:0] = 101: 1.5625μA, [2:0] = 110: 2.1875μA, [2:0] = 111: 3.125μA. **While Reg. Addr 0x39[5:4] = 11,** [2:0] = 000: Disable, [2:0] = 001: 0.625μA, [2:0] = 010: 1.25μA, [2:0] = 011: 1.875μA, [2:0] = 100: 2.50μA, [2:0] = 101: 3.125μA, [2:0] = 110: 4.375μA, [2:0] = 111: 6.25μA.
0x3A	[7:2]	RESERVED	[7:2] = 001000h. All other combinations are not defined.
	[1:0]	QR_WD_C	**Setting QR width of rail C.** [5:4] = 00: 0.4×T_{ON}, [5:4] = 01: 0.55×T_{ON}, [5:4] = 10: 0.75×T_{ON}, [5:4] = 11: 0.92×T_{ON}.
0x3B	[7]	EN_0LL_C	**Enable zero load-line of rail C.** [7] = 0: Disable 0LL. [7] = 1: Enable 0LL.
	[6]	RESERVED	Reserved bit
	[5]	EN_SSOCP_C	**Enable/Disable SSOCP function of rail C.** [5] = 0: Disable, [5] = 1: Enable
	[4]	AEAGM_C	**AEAGM gain setting of rail C.** [4] = 0: 2/3. [4] = 1: 1.
	[3:0]	RESERVED	[3:0] = 0110. All other combinations are not defined.
0x3C	[7:0]	RESERVED	Reserved bit
0x3D	[7:0]	RESERVED	Reserved bit

Register Address	Bits	Symbol	Description
0x3E	[7:0]	IOUT_TELEMETRY_OFFSET_A	**Set IOUT telemetry offset of rail A.** [7]: sign bit, 0 is positive. (as part of two's complement) [6:0]: 1LSB = MAX_CURRENT/1023 IOUT_TELEMETRY = $IMON_{ADC}$-IOUT_TELEMTERY_OFFSET Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.] 01h = +1 LSB FFh = -1 LSB 7Fh = +127 LSB 80h = -128 LSB
0x3F	[7:0]	IOUT_TELEMETRY_OFFSET_B	**Set IOUT telemetry offset of rail B.** [7]: sign bit, 0 is positive. (as part of two's complement) [6:0]: 1LSB = MAX_CURRENT/1023 IOUT_TELEMETRY = $IMON_{ADC}$-IOUT_TELEMTERY_OFFSET Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.] 01h = +1 LSB FFh = -1 LSB 7Fh = +127 LSB 80h = -128 LSB
0x40	[7:0]	IOUT_TELEMETRY_OFFSET_C	**Set IOUT telemetry offset of rail C.** [7]: sign bit, 0 is positive. (as part of two's complement) [6:0]: 1LSB = MAX_CURRENT/1023 IOUT_TELEMETRY = $IMON_{ADC}$-IOUT_TELEMTERY_OFFSET Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.] 01h = +1 LSB FFh = -1 LSB 7Fh = +127 LSB 80h = -128 LSB
0x41	[7:0]	CODE_VERSION_LSB	It is used to provide the unique code identifier assigned by the vendor for different customers and different projects.
0x42	[7:0]	CODE_VERSION_MSB	It is used to provide the unique code identifier assigned by the vendor for different customers and different projects.
0x43	[7:0]	Group1 CRC-8 Code	Group1 Registers CRC code. The Data update when VCC POR or restore NVM. The polynomial is $x^8 + x^2 + x^1 + 1$.

Table 3. Functions that Cannot Support On-Line Tuning (Group 1)

Register Address	Function	Support On-Line Tunning
0x00[3:0]	SLAVE SEQUENCE	No
0x02,0x0F,0x17	VID_DEFAULT_VOLTAGE_A/B/C DEFAULT_SLEW_RATE_A/B/C	No
0x03,0x1FCh 0,0x18	OCP_THRESH_A/B/C	No
0x04,0x11,0x19	OCP_WARN_THRESH_A/B/C	No
0x05,0x12,0x1A	OCP_WARN_MIN_PULSE_A/B/C OCP_FAULT_DELAY_A/B/C	No
0x08[6:4],0x34[6],0x3B[6]	EN_DBLR_A/B/C SET_DBLR_PH_A	No
0x08[2:0],0x14[6:4],0x1C[6:4]	Ai_A/B/C	No
0x1F[0],0x1F[2],0x1F[4]	EN_SPS_A/B/C	No
0x21	IOUT_SCALE	No
0x34[4], 0x3B[4]	AEAGM_B/C	No

18.7 Thermal Monitoring and Indicator

The TSEN pin supports thermal monitoring using either an NTC thermistor or the temperature monitor of the smart power stage and it can be set by NVM.

When an NTC thermistor is used as thermal monitoring, the TSEN pin voltage = 80μA x (R1//RNTC+R2), is defined as Thermal Voltage, the NTC thermistor network to sense temperature as shown in Figure 4. It is recommended to place the NTC thermistor near the MOSFET, the hottest area in the PCB.

The controller processes the TSEN pin voltage to report temperature telemetry. When the TSEN pin voltage is less than the VRHOT_THRESH voltage, the controller asserts the VR_HOT bit in the temperature telemetry packet to indicate thermal alert. The VRHOT_THRESH can be changed through the SVI3 register.

Temperature Register data is updated every 700μs and the averaging interval is 5.6ms. The resistance accuracy of the TSEN network is recommended to be less than 1% error. NTC thermistor is 100k/Beta = 4250 and accuracy is 1%.

When thermal monitoring is implemented by TMON of smart power stage (SPS), the NVM registers of TSEN need to select the SPS temperature sensor and the TSEN pin operates as an input terminal to receive the TMON output from SPS. The RT3674AJ offers the thermal register of 0.6 V at 0°C and 1.4 V at 100°C with 8 mV/°C typical slope.

$$\text{Temp.}(^\circ C) = \frac{V_{TMON} - 0.6V}{8mV/^\circ C}$$

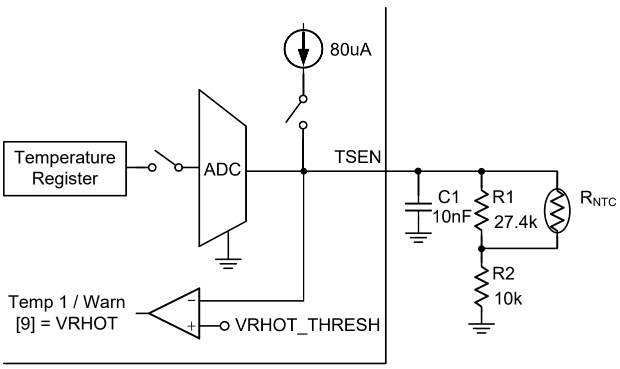


Figure 4. Multi-Function Pin Setting Mechanism for TSEN

18.8 System Input Power Monitoring (PSYS)

The RT3674AJ provides a PSYS function to monitor total system power and report it to the CPU via the SVI3 interface.

The PSYS function is illustrated in Figure 5. The PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the P_{SYS} voltage = 1.6V or 3.2V with maximum I_{PSYS} for 100% system input power. The full scale voltage of PSYS can be set by NVM.

System power telemetry consists of a 10-bit encoding that is mapped to eight user-selectable scales. The user-selectable scales can be set by NVM. Pull the PSYS pin to VCC can disable the PSYS function.

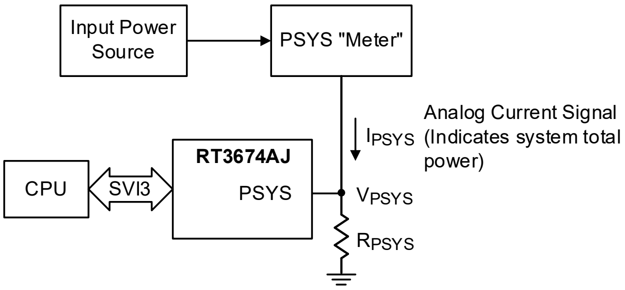


Figure 5. PSYS Function Block Diagram

18.9 Zero Load-Line

The RT3674AJ also supports enable the zero load-line function. When the zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3674AJ adopts AC-droop to effectively suppress load transient ring-back and control overshoot for zero load-line applications. Figure 6 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring-back ΔV2 due to charge in the C area. Figure 7 shows the condition with AC-droop control. While loading occurs, the controller changes the VID target to a short-term voltage target temporarily. The short-term voltage target is related to the transient load current ΔI_{CC} and can be represented as follows:

$$Short\_Term\_Voltage\_Target = VID - \Delta I_{CC} \times R_{LL}$$

The method to set R_{LL} is the same as in load-line systems. The short-term voltage target reverts to the VID target slowly after a certain period. The short-term voltage target can help prevent the inductor current from significantly exceeding the load current and then the ring-back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

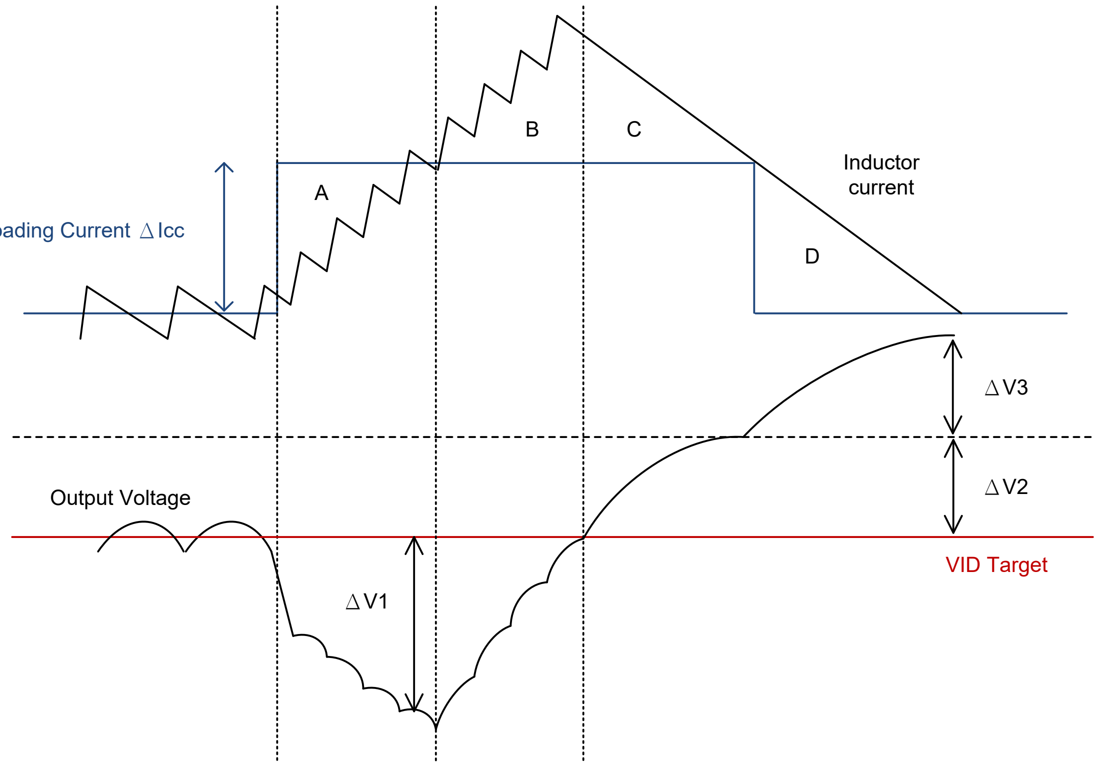


Figure 6. Zero Load-Line without AC-Droop Control

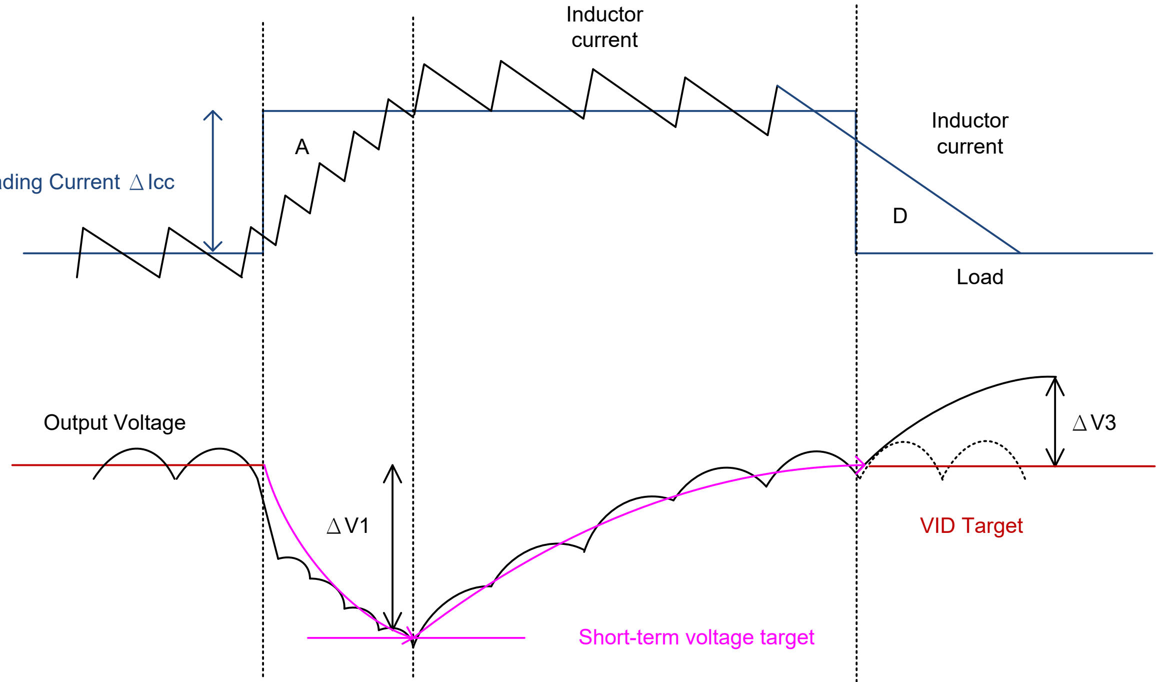


Figure 7. Zero Load-Line with AC-Droop Control

18.10 Rail A VR

18.10.1 Current Sense

The RT3674AJ supports two different current sense mechanisms, one is DCR current sensing and the other is Smart Power Stage (SPS) current sensing.

18.10.2 DCR Current Sense

To achieve higher efficiency, the RT3674AJ adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 8. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant R_{X1} x C_X should match time constant $\frac{L}{DCR}$ of the inductance and DCR. It is necessary to fine tune R_{X1} and C_X for transient performance and current telemetry. If the RC network time constant matched inductor time constant, an ideal load transient waveform can be designed. If the RC network time constant is larger than the inductor time constant $\frac{L}{DCR}$, the VSEN waveform has a sluggish droop during load transient. If the RC network is smaller than the inductor time constant $\frac{L}{DCR}$, the VSEN waveform sags to create an undershooting to fail the specification and mis-trigger overcurrent protections (sum OCP). Figure 9 shows the output waveforms according to the RC network time constant. The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the output current telemetry accuracy. The C_X is suggested to be 0.1μF X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}}$$

The R_{X2} is optional to prevent V_{CSIN} exceeding current sense amplifier input range. The time constant of (R_{X1}//R_{X2}) x C_X should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance, and zero current. The mirrored current to the IMONx pin is 1.25 time of $I_{CS,PER}$

$$I_{IMONx} = A_{MIRROR} \times I_{CS,PERx},\ A_{MIRROR} = 1.25$$

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

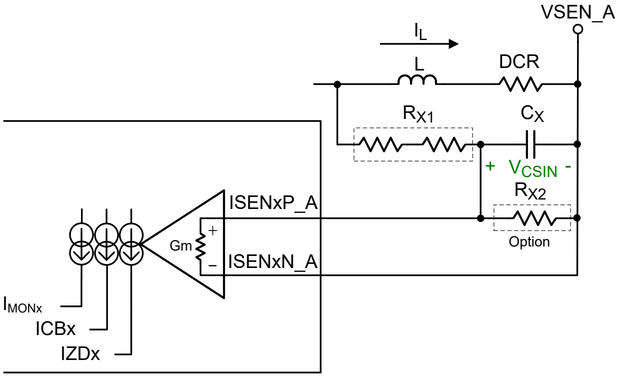


Figure 8. Inductor DCR Current Sensing Method

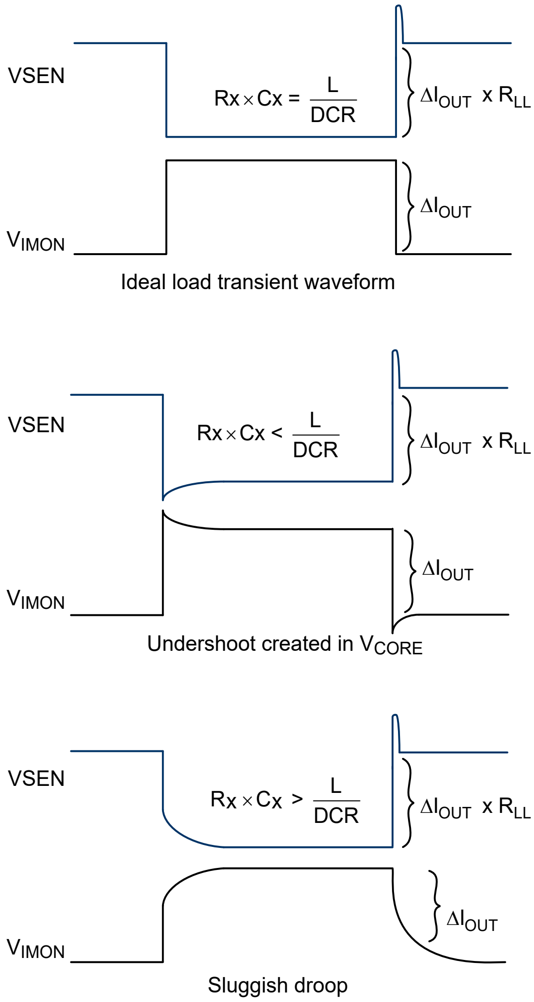


Figure 9. All Kinds of RC Network Time Constant

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3674AJ adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within the IMON resistor network at the IMON pin. It is suggested to be placed near the inductor of the first phase.

All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON_A} by $R_{IMON,EQ}$ based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as V_{VREF}) during normal operation. The relationship between V_{IMON_A} and inductor current I_{Lx} is:

$$V_{IMON\_A}-V_{VREF}$$
$$=(I_{L1}+I_{L2}+I_{L3}+I_{L4})\times\frac{DCR}{1K\Omega}\times A_{MIRROR}\times R_{IMON,EQ}$$

$V_{IMON\_A} - V_{VREF}$ is proportional to the output current. $V_{IMON\_A} - V_{VREF}$ is used for output current telemetry, and load-line loop-control, and sum overcurrent protection. For the telemetry, $V_{IMON\_A} - V_{VREF}$ is averaged by analog low-pass filter and then coded by 10-bit ADC and mapped to user-selectable I_OUT_SCALE_A. The I_OUT_SCALE_A can be set by NVM. The $R_{IMON,\ EQ}$ should be designed according to the Max. current of I_OUT_SCALE_A value, that is $V_{IMON\_A} - V_{VREF} = 0.4V$ while $(I_{L1}+I_{L2}+I_{L3}+I_{L4})$ = Max. current of I_OUT_SCALE_A. The maximum current sense gain error of the controller is ±2%.

For load-line loop control, $V_{IMON\_A} - V_{VREF}$ is scaled by Ai, and it can be selected by register Ai_A. The detailed application is described in the Load-Line Setting (R_{LL}) section.

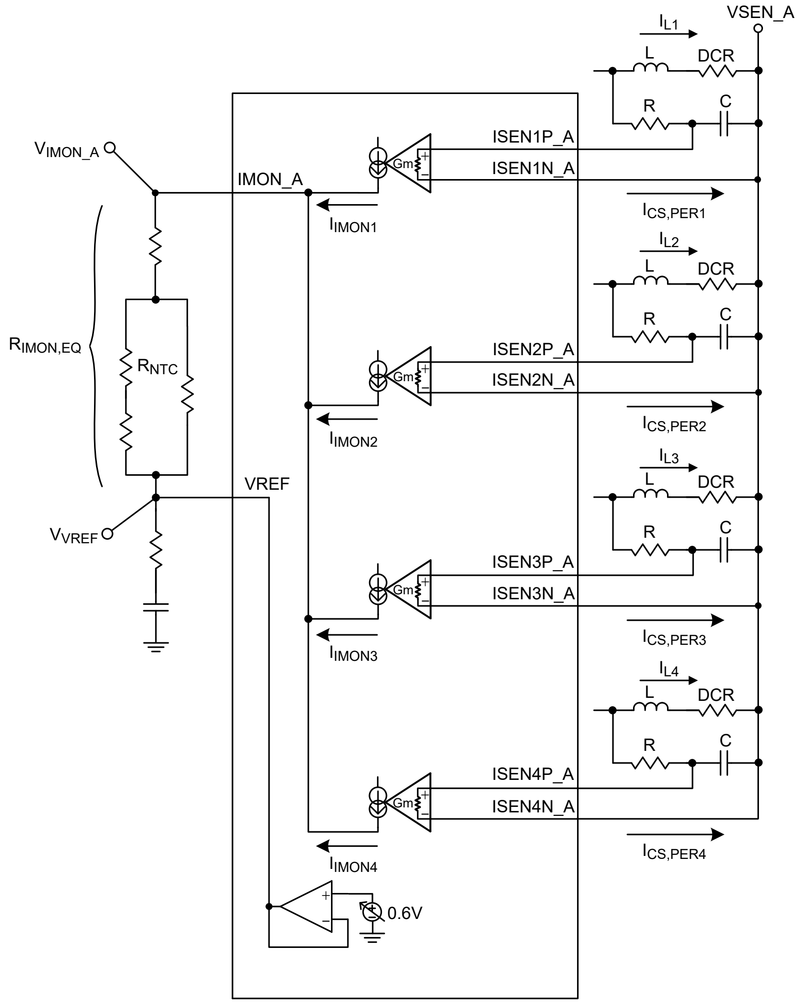


Figure 10. Total DCR Current Sense Method

18.10.3 Smart Power Stage (SPS) Current Sense

As SPS current sense is used, the register of EN_SPS_A needs to be enabled and ISEN1N_A operates as the output terminals, which offer the reference voltage of 1.3V for the reference inputs of SPS. The ISENxN_A of each phase is connected by internal and a capacitor of 0.22μF to 1μF is suggested to be connected between ISEN1N_A to GND. Figure 11 shows the implementation of SPS current sensing report. The V_{IMON} and current reporting from SPS can be calculated as:

$$V_{IMON\_A} - V_{VREF}$$
$$= (I_{OUT\_SPS1} + I_{OUT\_SPS2} + I_{OUT\_SPS3} + I_{OUT\_SPS4})$$
$$\times \frac{R_{SENSE}}{1K\Omega} \times A_{MIRROR} \times R_{IMON,EQ}$$

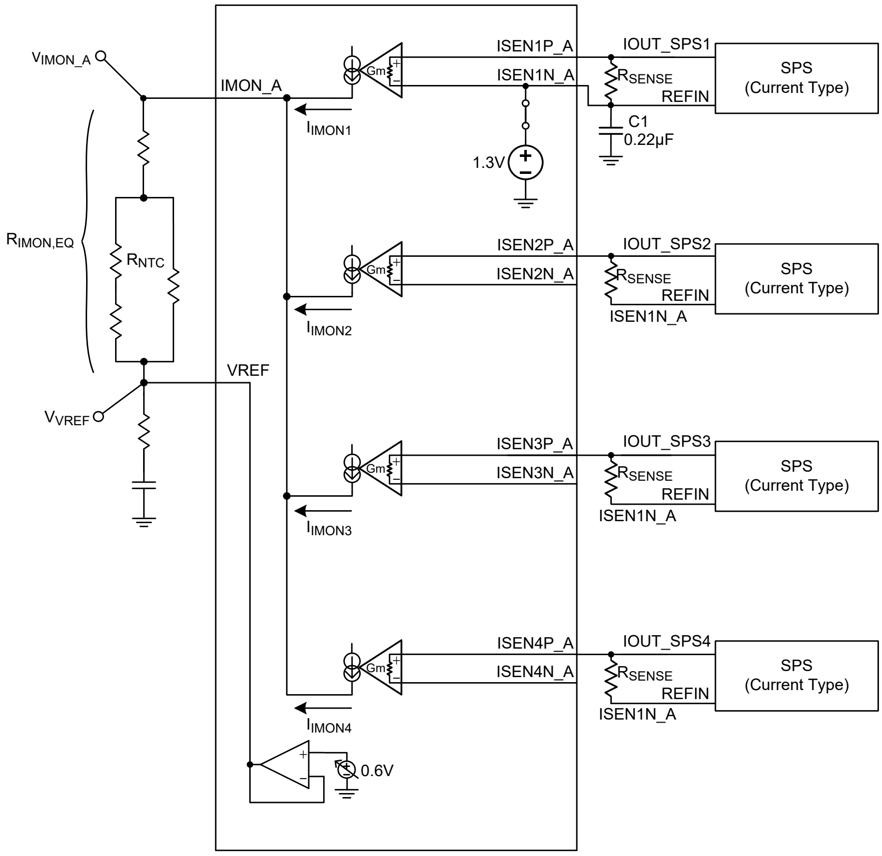


Figure 11. SPS Current Sense

18.10.4 Load-Line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is defined by the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current (R_{LL}) is shown in Figure 12. Figure 13 shows the voltage and current loop circuits of the RT3674AJ for the load-line control. The detailed equation is described as below:

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{1K\Omega} \times A_{MIRROR} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times 3$$

, where Ai is current gain and $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested as 2~4.5 for better transient response. R_{LL} can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be

selected by the registers of Ai_A[2:0], which is listed in Table 4.

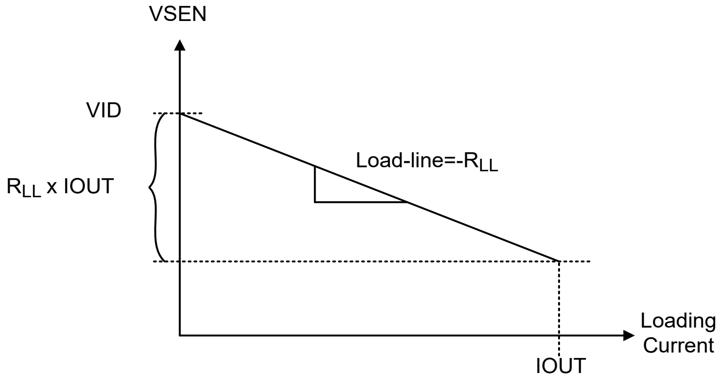


Figure 12. Load-Line (Droop)

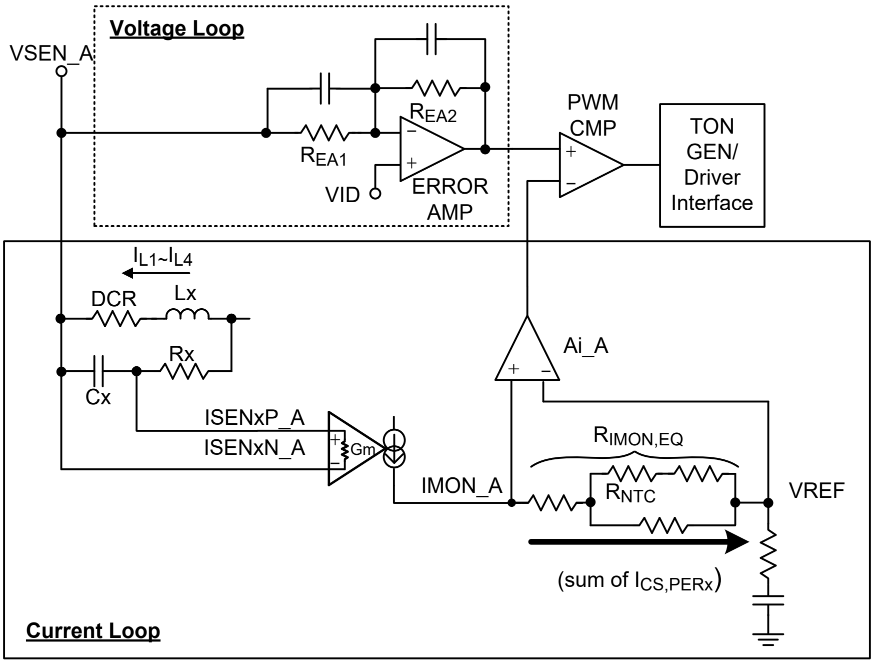


Figure 13. Voltage Loop and Current Loop for Load-Line

Table 4. Setting of Ai_A[2:0]

Ai_A[2:0]	Current Gain Setting
000	0.25
001	0.5
010	0.75
011	1.00
100	0.125
101	0.375
110	0.625
111	0.875

18.10.5 Voltage-On-The Fly (VOTF) Compensation

During the VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the VOTF slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to VOTF Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, mΩ). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 14. The RT3674AJ provides one VOTF compensation function as shown in Figure 15. An internal current I_{VOTF_LIFT} sinks internally from the FB pin to generate the VOTF compensation, $I_{DVID\_LIFT} \times R_{EA1}$. I_{VOTF_LIFT} for fast VOTF SR can be set from registers of VOTF_LIFT_TH_A. For different scales of VOTF SR, I_{VOTF_LIFT} is internally adjusted.

Compensating magnitude can also be adjusted by R_{EA1}. When the DAC output reaches the target voltage, the inductor current is still high and needs a time to settle down to the DC load current. In the settling time, the decreasing inductor current keeps charging the output capacitor (The magnitude is related with inductor, capacitance, and VID). Thus, the VOTF compensation can be less than VOTF Slew Rate x Output Capacitance (capacitance deration should be considered). If the output capacitance is so large that the VOTF compensation cannot cover, adding a resistor and capacitor from FB to GND can also provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects VOTF behavior. The final setting should be based on actual measurement.

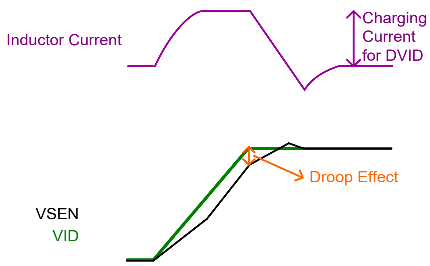


Figure 14. Droop Effect in VID Transition

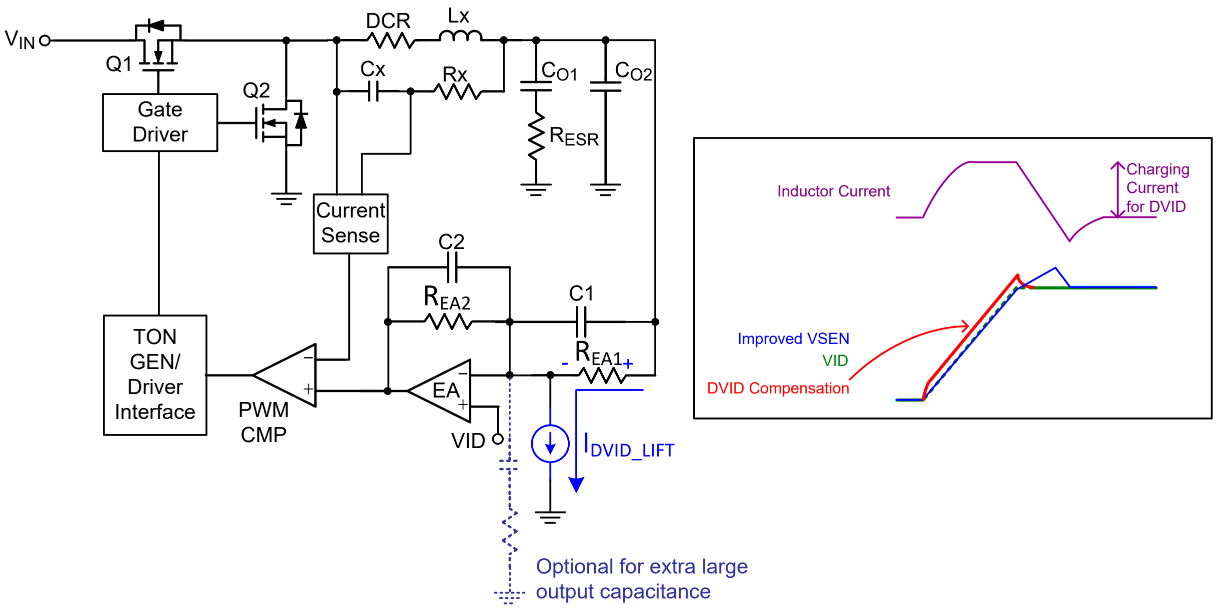


Figure 15. VOTF Compensation

18.10.6 Compensator Design

The compensator of the RT3674AJ does not need a complex type III compensator to optimize control loop performance. It can adopt a simple type II compensator (one pole, one zero) in the G-NAVP topology to fine tune the ACLL performance. The one pole and one zero compensator is shown in Figure 16. For SVI3 transient specifications, it is recommended to adjust the compensator according to the load transient ring-back level. Refer to the design tool for default compensator values.

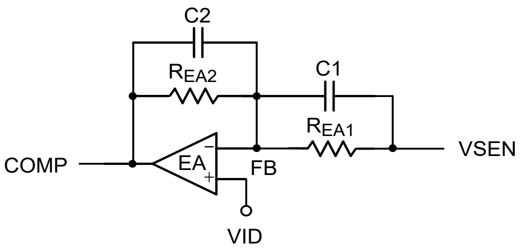


Figure 16. Type II Compensator

18.10.7 Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 17. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide the output voltage feedback.

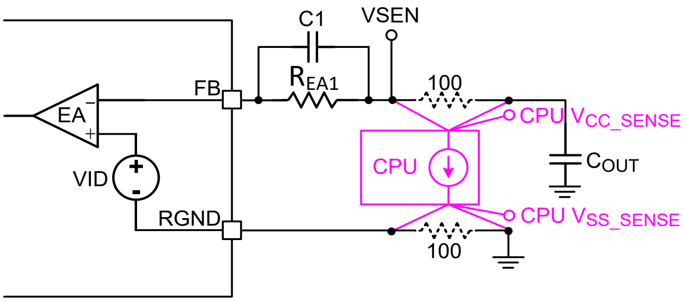


Figure 17. Remote Sensing Circuit

18.10.8 Switching Frequency Setting

The G-NAVP (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive t_{ON} (PWM) with input voltage (VIN) for better line regulation. The t_{ON} is also adaptive to VID voltage to achieve constant frequency. The constant switching frequency operation makes the thermal estimation easy. The RT3674AJ provides a parameter setting of K_{TON} to design t_{ON} width. K_{TON} is set by NVM register of KTON_A. The related setting table is listed in Table 5.

The equations of t_{ON} are listed as below:

VID>0.9V,

$$ton = 2u \times \frac{VID}{K_{TON} \cdot (VIN)}$$

VID≤0.9V,

$$Ton = 2u \times \frac{0.9}{K_{TON} \cdot (VIN)}$$

Table 5. Setting of KTON_A[4:0]

KTON_A[4]	KTON
0	KTON = 0.5 + [3:0] x 0.1
1	KTON = 1.2 + [3:0] x 0.1

The switching frequency can be derived from t_{ON} as below. The losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times \left(DCR + \frac{R_{ON_{LS,max}}}{n_{LS}} - N \times R_{LL}\right)}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ON_{LS,max}}}{n_{LS}} - \frac{R_{ON_{HS,max}}}{n_{HS}}\right)\right] \times \left(t_{ON} - t_D + t_{ON,\ VAR}\right) + \frac{I_{CC}}{N} \times \frac{R_{ON_{LS,max}}}{n_{LS}} \times T_D}$$

VID: VID voltage

VIN: Input voltage

I_{CC}: Loading current

N: Total phase number

$R_{ON_{HS,max}}$: Maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: Number of high-side MOSFETs

$R_{ON_{LS,max}}$: Maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: Number of low-side MOSFETs.

t_D: Summation of the high-side MOSFET delay time and rising time

$t_{ON,\ VAR}$: On-time variation value

DCR: Inductor DCR

R_{LL}: Load-line setting (Ω)

18.10.9 Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR)

The RT3674AJ adopts Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR) to optimize transient response. Figure 18 shows the mechanism for AQR and Fixed QR. Under the AQR mechanism, the controller detects the output voltage drop slew rate. When the slew rate exceeds the AQR trigger threshold, all PWMs turn on until the output voltage slew rate significantly slows down. AQR PWM width is adaptive to variable loading step. Under the Fixed QR mechanism, the controller detects the output voltage drop slew rate. While the slew rate exceeds the AQR trigger threshold, all PMWs turn on and PWM width can be selected through NVM registers of QR_WD_A in multi-phase operation and QR_WD_1PH_A in single-phase operation.

The AQR trigger threshold can be selected through NVM registers of AQR_TH_A in multi-phase operation and AQR_TH_1PH_A in single-phase operation.

The following equation can initially decide the AQR and Fixed QR starting trigger threshold. Note that the threshold should be larger than the steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid mis-triggering.

$$\text{Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$

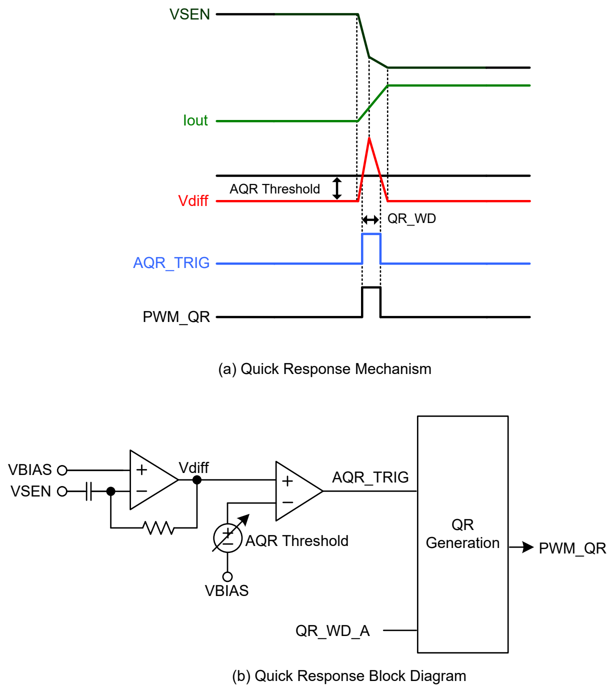


Figure 18. Adaptive Quick Response and Fixed Quick Response Mechanism

18.10.10 Anti-Overshoot (ANTI-OVS)

The RT3674AJ provides the anti-overshoot function to suppress output voltage overshoot. The controller detects overshoot by signals related to the output voltage. The overshoot trigger level can be adjusted by the NVM register of ANTIOVS_TH_A. The main detecting signal comes from COMP. However, COMP characteristic varies with compensation. Initial trigger level setting is based on the following equation:

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be determined according to actual Error AMP compensator design and measurement.

When the overshoot exceeds the set trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN returns to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

18.10.11 ACLL Performance Enhancement

The RT3674AJ provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. The controller detects the COMP signal and compares it with steady state. When V_{COMP} variation exceeds a threshold, an additional positive offset is added to the output voltage. The undershoot suppression threshold can be selected through NVM register of AR_TH_1PH_A.

The smaller index indicates that the detection is triggered easily. Figure 19 shows undershoot suppression behavior in single phase. For different platforms, the optimized settings are different. The final setting must be based on the actual measurement.

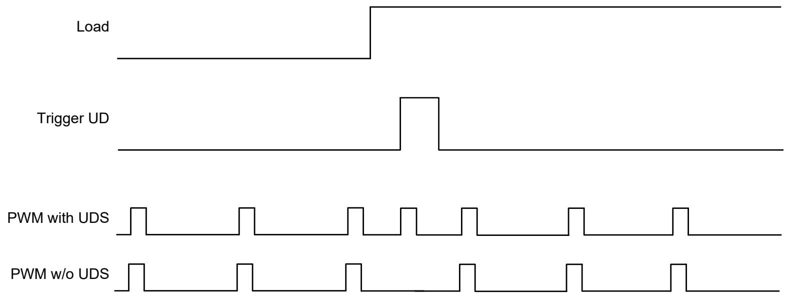
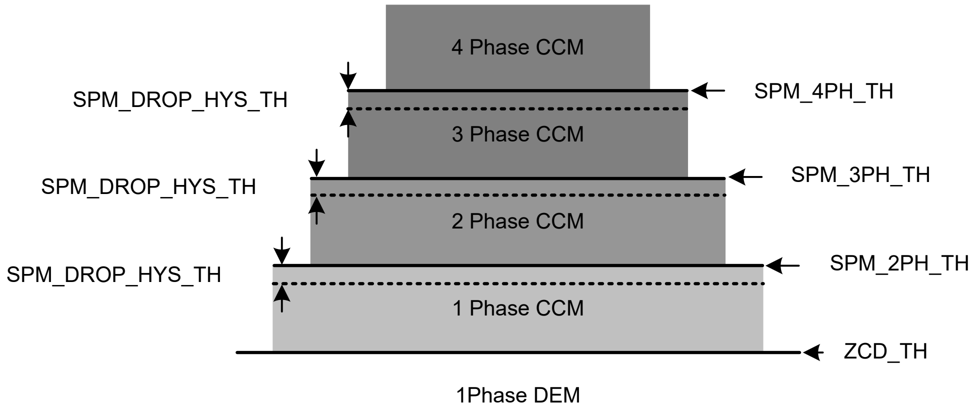


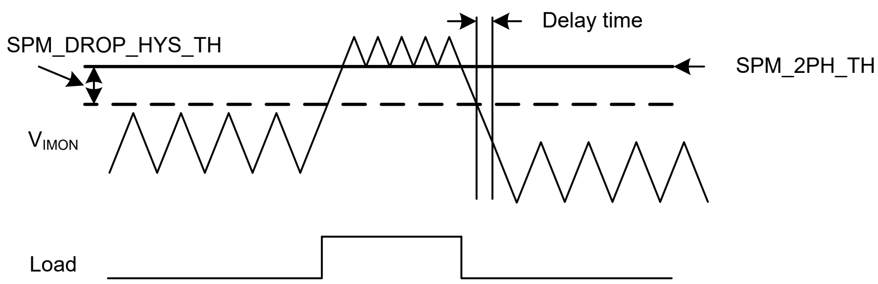
Figure 19. Undershoot Suppression Behavior in Single Phase

18.10.12 Smart Phase Management (SPM)

Automated phase shedding function is required in the SVI3 protocol. The RT3674AJ provides smart phase management to meet the spec and improve light load efficiency. When CPU sends PSI7 command to the VR, the VR will enter SPM mode. It can always enable and disable through the I^2C register (FORCE_PSI7 and IGNORE_PSI7). The SVI3 Register PSI state follows the SVI3 command and the ACK PSI change command when force/ignore PSI7. The IMON pin voltage (V_{IMON}) represents the total current. The controller compares V_{IMON} with SPM_2PH_TH, SPM_3PH_TH, and SPM_4PH_TH to decide the number of operating phase. There is no delay during up phase. The hysteresis (SPM_DROP_HYS_TH) and delay time exist during a down phase decision. When V_{IMON} is lower than (SPM_2PH_TH-SPM_DROP_HYS_TH), (SPM_3PH_TH-SPM_DROP_HYS_TH), or (SPM_4PH_TH-SPM_DROP_HYS_TH), the controller goes to lower phase number operation and automatically enters to diode emulation mode (DEM) when the inductor current is lower than the zero current detector threshold. In addition to the output current comparison, the RT3674AJ provides four events to operate in full phase immediately. One is VOTF up, another is VOTF down without enabling decay mode, another is triggering the AQR/Fixed QR function and the other is enabling Force_PSI0 through the I^2C register. Figure 20 shows the smart phase management mechanism.



(a) Smart Phase Management 4 Phase Operator Phase Diagram



(b) Smart Phase Management Up and Down Phase Diagram

Figure 20. Smart Phase Management Mechanism

18.11 Rail B/C VR

18.11.1 Current Sense

The RT3674AJ supports two different current sense mechanisms, one is DCR current sensing and the other is Smart Power Stage (SPS) current sensing.

18.11.2 DCR Current Sense

To achieve higher efficiency, the RT3674AJ adopts inductor DCR current sensing to get per-phase current signal, as illustrated in Figure 21. An external low-pass filter ($R_{X1}//R_{EQ}$) and C_X reconstruct the current signal. The low-pass filter time constant $(R_{X1}//R_{EQ})\times C_X$ should match time constant $\frac{L}{DCR}$ of inductance and DCR. It is necessary to fine tune ($R_{X1}//R_{EQ}$) and C_X for transient performance and current telemetry. If the RC network time constant matched inductor time constant, an ideal load transient waveform can be designed. If the RC network time constant is larger than the inductor time constant $\frac{L}{DCR}$, the VSEN waveform has a sluggish droop during load transient. If the RC network is smaller than the inductor time constant $\frac{L}{DCR}$, the VSEN waveform sags to create an undershooting to fail the specification and mis-trigger overcurrent protections (sum OCP). Figure 22 shows the output waveforms according to the RC network time constant. The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the output current telemetry accuracy. The C_X is suggested to be 0.1μF X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PER} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}} \times \frac{R_{EQ}}{R_{X1}+R_{EQ}}$$

The current signal $I_{CS,PER}$ is mirrored for load-line control/current reporting and zero current. The mirrored current to IMON_X pin is 1.25 time of $I_{CS,PER}$

$$I_{IMON\_X} = A_{MIRROR} \times I_{CS,PER},\ A_{MIRROR} = 1.25$$

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

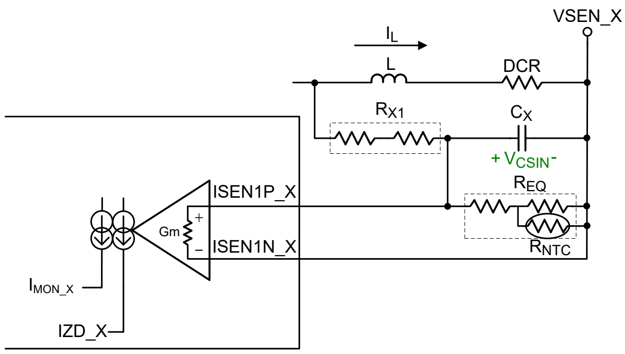


Figure 21. Inductor DCR Current Sensing Method

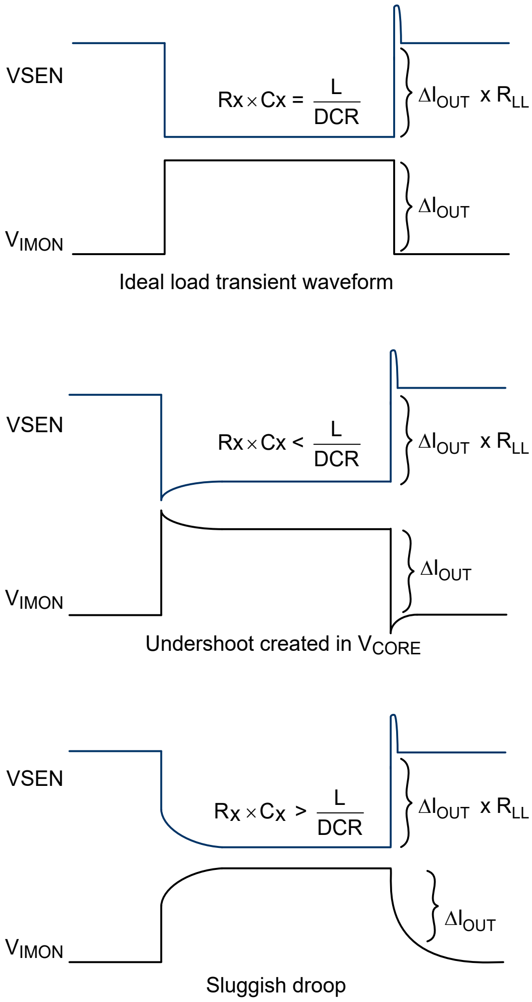


Figure 22. All Kinds of RC Network Time Constant

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The NTC resistor is designed within DCR current sense network. It is suggested to be placed near the inductor of the first phase.

The current signal is gathered to the IMON_X pin and converted to a voltage signal V_{IMON_X} by R_{IMON_X} based on the VREF pin. The VREF pin provides 0.6V voltage source (as presented as V_{VREF}) during normal operation. The relationship between V_{IMON_X} and inductor current I_L is:

$$V_{IMON\_X} - V_{VREF} = I_L \times \frac{DCR}{1K\Omega} \times \frac{R_{EQ}}{R_{X1} + R_{EQ}} \times A_{MIRROR} \times R_{IMON\_X}$$

$V_{IMON\_X} - V_{VREF}$ is proportional to the output current. $V_{IMON\_X} - V_{VREF}$ is used for output current telemetry and load-line loop-control and sum overcurrent protection. For the telemetry, $V_{IMON\_X} - V_{VREF}$ is averaged by analog low-pass filter and then coded by 10-bit ADC and mapped to user-selectable I_OUT_SCALE_B and I_OUT_SCALE_C for Rail B and Rail C, respectively. The I_OUT_SCALE_B and I_OUT_SCALE_C can be set by NVM.

The R_{IMON_X} should be designed according to Max. current of I_OUT_SCALE value, that is $V_{IMON\_X} - V_{VREF}$ = 0.4V while I_L = Max. current of I_OUT_SCALE. The maximum current sense gain error by controller is ±2%.

For load-line loop control, $V_{IMON\_X} - V_{VREF}$ is scaled by Ai, and it can be selected by registers of Ai_B and Ai_C for Rail B and Rail C respectively. The detailed application is described in the Load-Line Setting (R_{LL}) section.

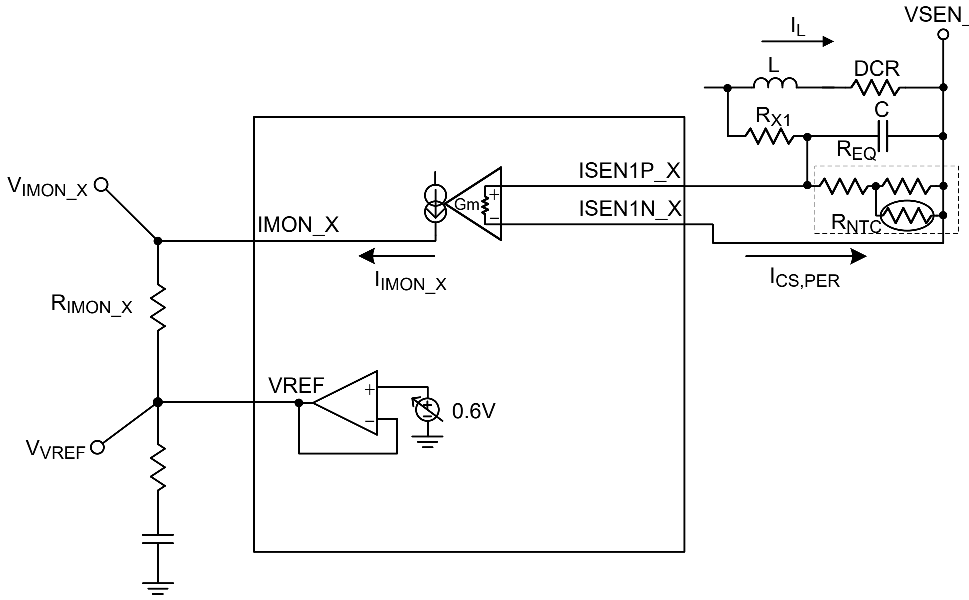


Figure 23. Total DCR Current Sense Method

18.11.3 Smart Power Stage (SPS) Current Sense

As SPS current sense is used, the registers of EN_SPS_B and EN_SPS_C need to be enabled for Rail B and Rail C respectively and ISEN1N operates as the output terminals which offer the reference voltage of 1.3V for the reference inputs of SPS. A capacitor of 0.22μF to 1μF is suggested to be connected between ISEN1N to GND. Figure 24 shows the implementation of SPS current sensing report. The V_{IMON_X} and current reporting from SPS can be calculated as:

$$V_{IMON\_X}-V_{VREF}=I_{OUT\_SPS}\times\frac{R_{SENSE}}{1K\Omega}\times A_{MIRROR}\times R_{IMON\_X}$$

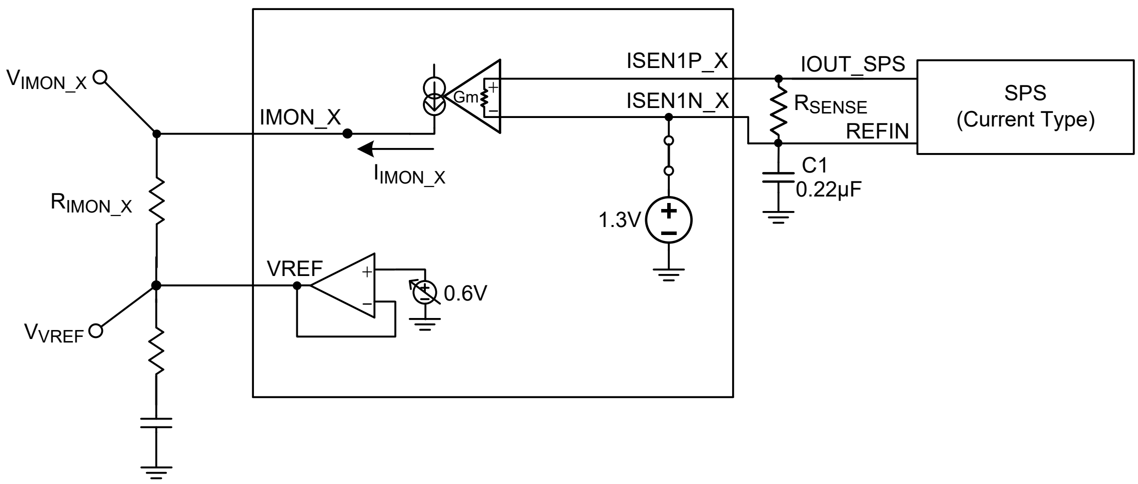


Figure 24. SPS Current Sense

18.11.4 Load-Line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current (R_{LL}) is shown in Figure 25. Figure 26 shows the voltage and current loop circuits of the RT3674AJ for the load-line control. The detailed equation is described as below:

$$R_{LL}=\frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}}=\frac{DCR}{1K\Omega}\times\frac{R_{EQ}}{R_{X1}+R_{EQ}}\times\frac{20k}{AEAGM}\times\frac{A_i}{\frac{R_{EA2}}{R_{EA1}}}$$

, where Ai is current gain, AEAGM is error amp GM ratio and $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested 1~4 for better transient response. R_{LL} can be programmed by Ai, AEAGM and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by the registers of Ai_B[6:4] and Ai_C[6:4], which is listed in Table 6. AEAGM can be selected by the registers of AEAGM_B[4] and AEAGM_C[4], which is listed in Table 7.

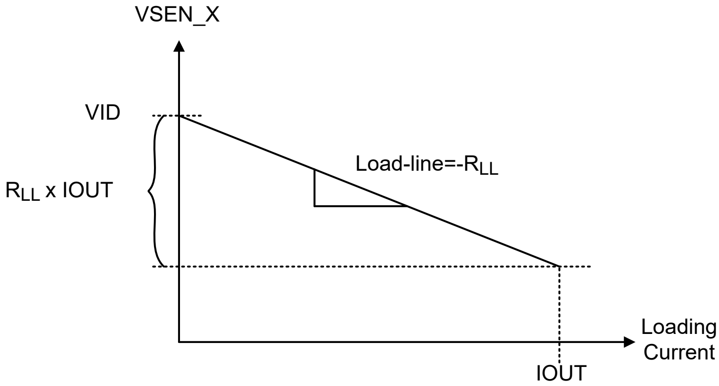


Figure 25. Load-line (Droop)

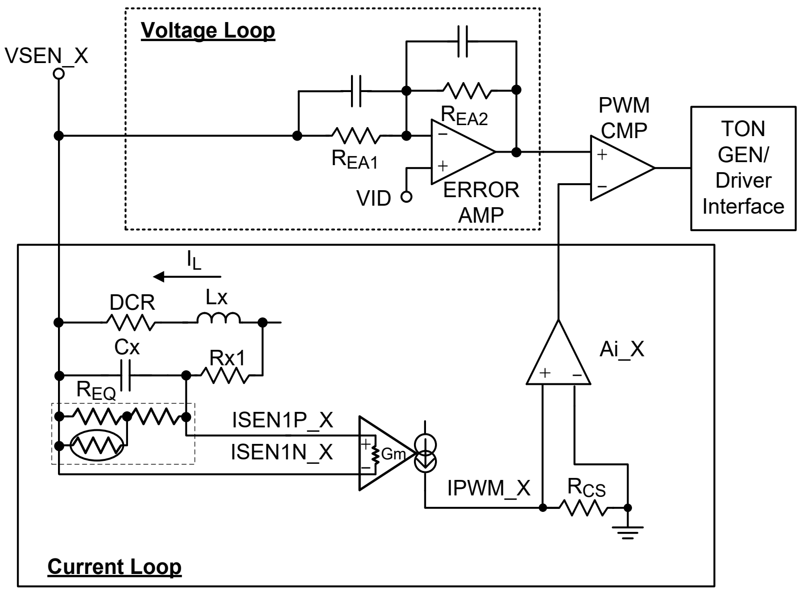


Figure 26. Voltage Loop and Current Loop for Load-line

Table 6. Setting of Ai_B[6:4] and Ai_C[6:4]

Ai_B[6:4] Ai_C[6:4]	Current Gain Setting
000	0.125
001	0.250
010	0.375
011	0.500
100	0.625
101	0.750
110	0.875
111	1.000

Table 7. Setting of AEAGM_B[4]and AEAGM_C[4]

AEAGM_B[4] AEAGM_C[4]	AEAGM Ratio
0	2/3
1	1

18.11.5 Voltage-On-The Fly (VOTF) Compensation

During VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the VOTF slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to VOTF Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, mΩ). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 27. The RT3674AJ provides one VOTF compensation function as shown in Figure 28. An internal current I_{VOTF_LIFT} sinks internally from FB pin to generate VOTF compensation, $I_{DVID\_LIFT} \times R_{EA1}$. I_{VOTF_LIFT} for fast VOTF SR can be set from registers of VOTF_LIFT_TH_B/C. For different scales of VOTF SR, I_{VOTF_LIFT} is internally adjusted.

Compensating magnitude can also be adjusted by R_{EA1}. When DAC output reaches the target, inductor current is still high and needs a period of time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, VOTF compensation can be less than VOTF Slew Rate x Output Capacitance (capacitance deration should be considered). If output capacitance is so large that VOTF compensation cannot cover, adding a resistor and capacitor from FB to GND can also provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects VOTF behavior. The final setting should be based on actual measurement.

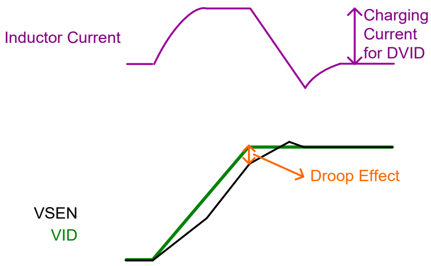


Figure 27. Droop Effect in VID Transition

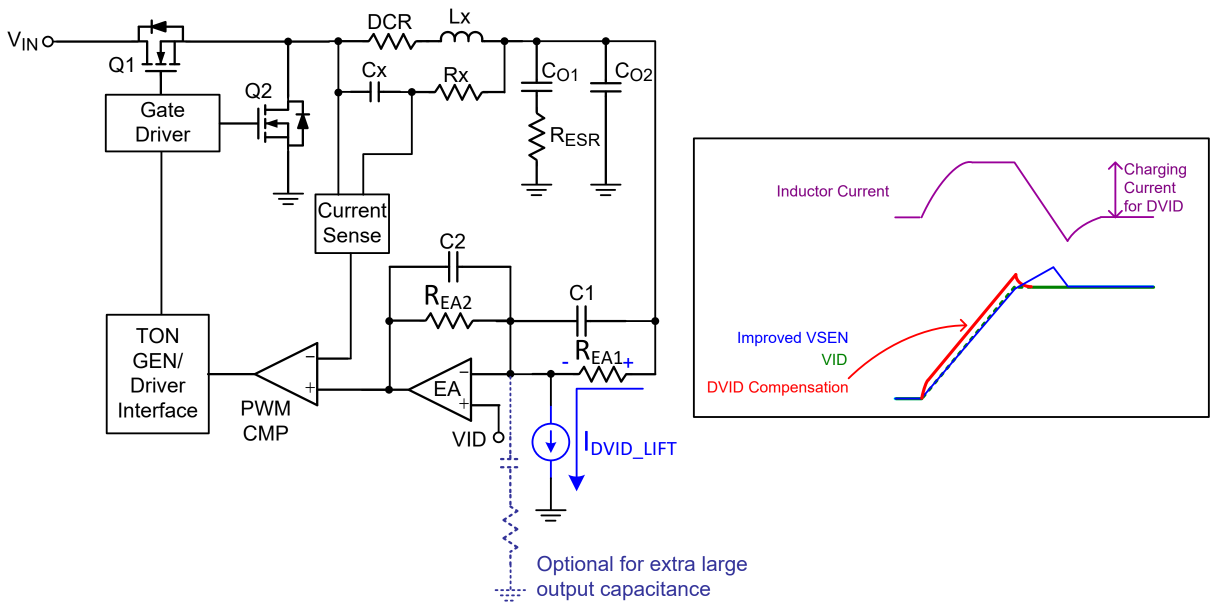


Figure 28. VOTF Compensation

18.11.6 Compensator Design

The compensator of the RT3674AJ does not need a complex type III compensator to optimize control loop performance. It can adopt a simple type II compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 29. For SVI3 transient specification, it is recommended to adjust compensator according to load transient ring-back level. Refer to the design tool for default compensator values.

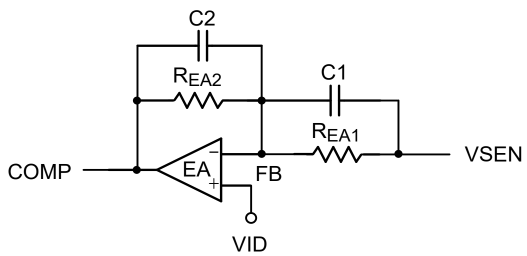


Figure 29. Type II Compensator

18.11.7 Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 30. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

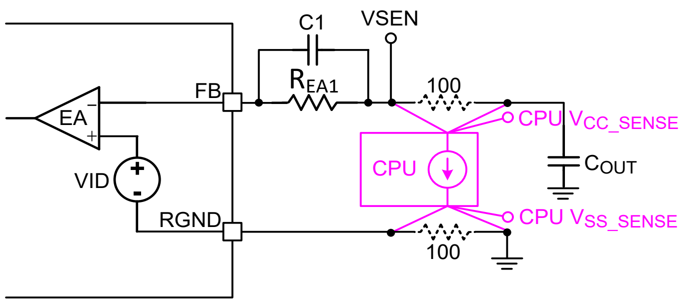


Figure 30. Remote Sensing Circuit

18.11.7.1 Switching Frequency Setting

The G-NAVP[TM] (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive T_{ON} (PWM) with input voltage (VIN) for better line regulation. The T_{ON} is also adaptive to VID voltage to achieve constant frequency concept. The constant switching frequency operation makes the thermal estimation easy. The RT3674AJ provides a parameter setting of K_{TON} to design T_{ON} width. K_{TON} is set by NVM register of KTON_B and KTON_C for rail B and C correspondingly. The related setting table is listed in Table 8.

The equations of T_{ON} are listed as below:

VID≥0.9V,

$$Ton = 2.206u\times\frac{VID}{K_{TON}\cdot(VIN-0.9)}+15ns$$

0.3V<VID<0.9V,

$$Ton = 1.9854u\times\frac{1}{K_{TON}\cdot(VIN-VID)}+15ns$$

VID≤0.3V,

$$Ton = 1.9854u\times\frac{1}{K_{TON}\cdot(VIN-0.3)}+15ns$$

Table 8. Setting of KTON_B[3:0] and KTON_C[3:0]

KTON_B[3:0] KTON_C[3:0]	KTON
0000	0.73
0001	0.82
0010	0.91
0011	1.00
0100	1.09
0101	1.18
0110	1.27
0111	1.36
1000	1.55
1001	1.64
1010	1.73
1011	1.82
1100	2.00
1101	2.18
1110	2.36
1111	2.55

The switching frequency can be derived from T_{ON} as shown below. The losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID+\frac{I_{CC}}{N}\times\left(DCR+\frac{R_{ONLS,max}}{n_{LS}}-N\times R_{LL}\right)}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ONLS,max}}{n_{LS}}-\frac{R_{ONHS,max}}{n_{HS}}\right)\right]\times\left(T_{ON}-T_{D}+T_{ON,\ VAR}\right)+\frac{I_{CC}}{N}\times\frac{R_{ONLS,max}}{n_{LS}}\times T_{D}}$$

VID: VID voltage

VIN: input voltage

I_{CC}: loading current

N: total phase number

$R_{ON_{HS,max}}$: maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

$T_{ON, VAR}$: on-time variation value

DCR: inductor DCR

R_{LL}: load-line setting (Ω)

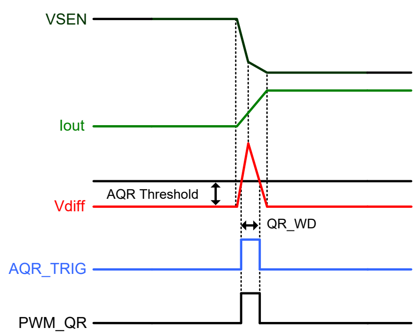
18.11.8 Adaptive Quick Response (AQR)

The RT3674AJ adopts Adaptive Quick Response (AQR) to optimize transient response. Figure 31 shows the mechanism concept for AQR and Fixed QR. Under AQR mechanism, the controller detects output voltage drop slew rate. When the slew rate exceeds the AQR trigger threshold, all PWMs turn on until output voltage slew rate significantly slows down. AQR PWM width is adaptive to variable loading step. Under Fixed QR mechanism, the controller detects output voltage drop slew rate. While the slew rate exceeds the AQR trigger threshold, all PMWs turn on and PWM width can be selected through NVM registers of QR_WD_B and QR_WD_C.

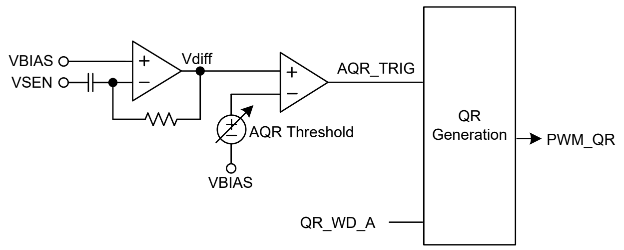
The AQR trigger threshold can be selected through NVM registers of AQR_TH_B and AQR_TH_C.

The following equation can initially decide the AQR and Fixed QR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid miss trigger.

$$\text{Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$



(a) Quick Response Mechanism



(b) Quick Response Block Diagram

Figure 31. Adaptive Quick Response and Fixed Quick Response Mechanism

18.11.9 Anti-Overshoot (ANTI-OVS)

The RT3674AJ provides anti-overshoot function to suppress output voltage overshoot. The controller detects overshoot by signals related to output voltage. The overshoot trigger level can be adjusted by NVM register of ANTIOVS_TH_B and ANTIOVS_TH_C. The main detecting signal comes from COMP. However, COMP characteristic varies with compensation. Initial trigger level setting is based on the following equation:

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be determined according to actual Error AMP compensator design and measurement.

When overshoot exceeds the set trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN returns to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

18.11.10 ACLL Performance Enhancement

The RT3674AJ provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. The controller detects the COMP signal and compares it with steady state. When V_{COMP} variation exceeds a threshold, an additional positive offset is added to the output voltage. The undershoot suppression threshold can be selected through NVM register of AR_TH_B and AR_TH_C.

The smaller index indicates that the detection is triggered easily. Figure 32 shows undershoot suppression behavior in single phase. For different platforms, the optimized settings are different. The final setting must be based on the actual measurement.

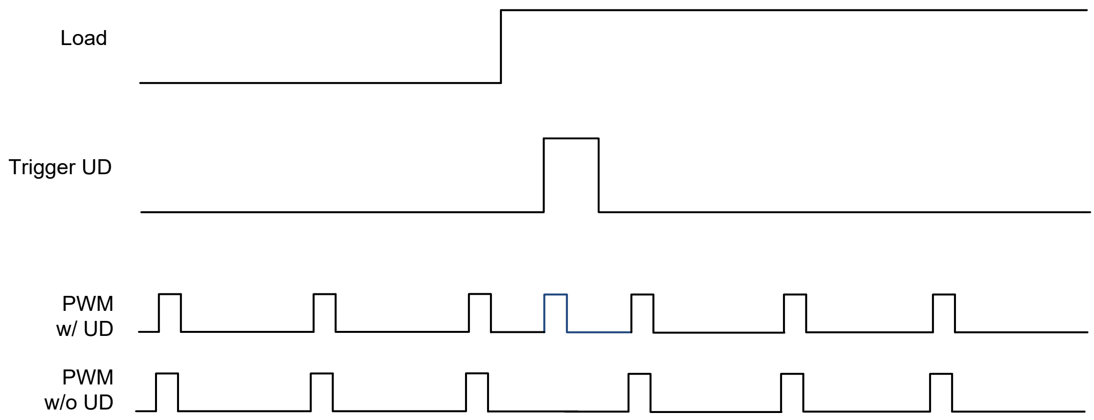


Figure 32. Undershoot Suppression Behavior in Single Phase

18.11.11 Overcurrent Protection (OCP)

The RT3674AJ supports two-level overcurrent protection for all rails, OCP fault, and OCP warning. The first level is OCP warning. Set the minimum pulse and threshold via OCP_WARN_THRESH Reg0x28[7:0] with a period of time OCP_WARN_MIN_PULSE Reg0x29[7:3] for assertion OCP_L. OCP_WARN bit is sticky in the TEMP1/WARN telemetry packet and FAULT_STATUS Reg0x10[4]. During a warning condition, the controller behavior will be unaffected.

The first level, the threshold of OCP warning for PSx is defined as:

$I_{SUM\_OC\_PSI0, 1, 2, 3, 7}$ = OCP_WARN_THRESH Reg0x28[7:0] x 4/512

The second level is the OCP fault. When the inductor current exceeds the OCP_THRESH Reg0x27[7:0] continuously for a duration specified by OCP_FAULT_DELAY Reg0x29[2:0], and the controller shall latch the assertion OCP_L and FAULT_STATUS Reg0x10[0]. The OCP_L pin will be de-asserted after the OCP fault is cleared, either by toggling PWR_ENABLE toggling or by cycling VCC power,.

The second level, the threshold of the sum OCP for PSx is defined as:

$I_{SUM\_OC\_PSI0,\ 1,\ 2,\ 3,\ 7}$ = OCP_THRESH Reg0x27[7:0] x 4/512 x O_PH/N;

where O_PH = operation phase number; N = phase number in PSI0 OCP is masked during the VOTF period plus 80μs after VID has settled. It is also masked when VID = 0V.

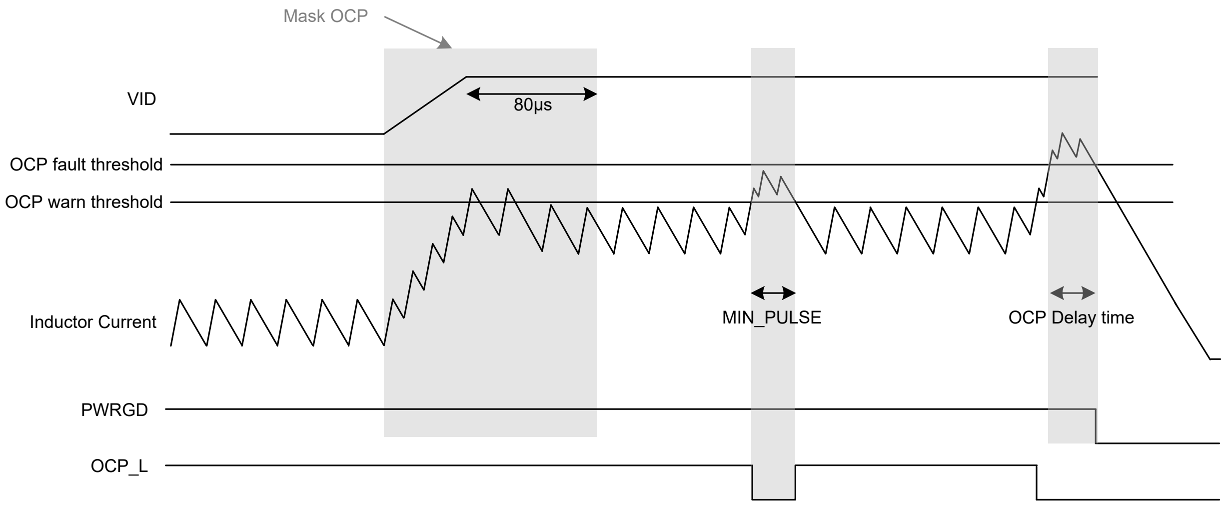


Figure 33. OC Protection Mechanism

18.11.12 Overvoltage Protection (OVP)

The OVP threshold is linked with VID. The classification table is illustrated in

Table 9. While VID = 0V, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, the OVP threshold is VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET to allow not-fully-discharged VSEN. However, the OVP threshold (select via OVP_DELTA Reg0x2C[6:4]) is combined by the VID or VID_MAX (select via OVP_REF Reg0x2C[7]). Those parameters can be programmable through the SVI3 command.

The OV protection mechanism is illustrated in Figure 34 and Figure 35. When OVP is triggered with 0.8μs filter time, the controller de-asserts PWRGD and forces all PWMs low to turn on low-side power MOSFETs. PWM remains low until the output voltage is pulled down to below new VID target for VOTF up from 0V and below VID for other conditions. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. The controller controls PWM to be low or in tri-state to pull down the output voltage along with VID.

Table 9. Summary of Overvoltage Protection

VID Condition	OVP Threshold	Protection Action	Protection Reset
VID = 0	OVP is masked.		VCC/PWREN Toggle
VOTF period + 80μs from zero/non-zero VID	OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤MAX_VOUT_SUPPORTED. 2. If VID_MAX = 0V, MAX_VOUT_SUPPORTED is used to calculate OVP threshold. OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA.	PWRGD de-assertion. The output voltage is pulled down to new VID target = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. 1. New VID target ≤MAX_VOUT_SUPPORTED 2. If VID_MAX = 0V, the new VID target be updated. New VID target = MAX_VOUT_SUPPORTED.	
VID≠0	VID or VID_MAX (select via 0x2C[7]) **0x2C[7] = 0b: VID** OVP_TH = VID + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET (VID + VOUT_OFFSET + I2C_VOUT_OFFSET ≤MAX_VOUT_SUPPORTED) **0x2C[7] = 1b: VID_MAX** OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤MAX_VOUT_SUPPORTED 2. If VID_MAX = 0V, MAX_VOUT_SUPPORTED is used to calculate OVP threshold. OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA.	**0x2C[7] = 0b: VID** PWRGD de-assertion. The output voltage is pulled down to new VID target = VID + VOUT_OFFSET + I2C_VOUT_OFFSET. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. (New VID target ≤MAX_VOUT_SUPPORTED) **0x2C[7] = 1b: VID_MAX** PWRGD de-assertion. The output voltage is pulled down to new target = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. 1. New VID target ≤MAX_VOUT_SUPPORTED. 2. If VID_MAX = 0V, the new VID target be updated. New VID target = MAX_VOUT_SUPPORTED.	
VOTF period + 80μs from zero/non-zero VID in VFIX mode	(I2C VFIX Mode) VFIX_EN = 1b: Enable OVP_TH = VFIX_MAX + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to VFIX_MAX. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate.	
VID≠0 in VFIX mode	(I2C VFIX Mode) VFIX_EN = 1b: Enable OVP_TH = VFIX + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to VFIX_MAX. After 60μs from OVP	

		trigger, VID starts to ramp down to 0V with slow slew rate. VFIX ≤ VFIX_MAX	
			continued…
VID Condition	**OVP Threshold**	**Protection Action**	**Protection Reset**
Change OVP_TH during VOTF period +80μs	**Previous OVP_TH < New OVP_TH** Change new OVP_TH immediately. **Previous OVP_TH > New OVP_TH** Remain Previous OVP_TH during VOTF period + 80μs, and then change new OVP_TH.	PWRGD de-assertion. The output voltage is pulled down to new VID target. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. New VID Target 1. VID/VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET 2. VFIX/VFIX_MAX (New VID target ≤MAX_VOUT_SUPPORTED) (If VID_MAX = 0V, the new VID target be updated. New VID target = MAX_VOUT_SUPPORTED.) (VFIX ≤ VFIX_MAX)	VCC/PWREN Toggle

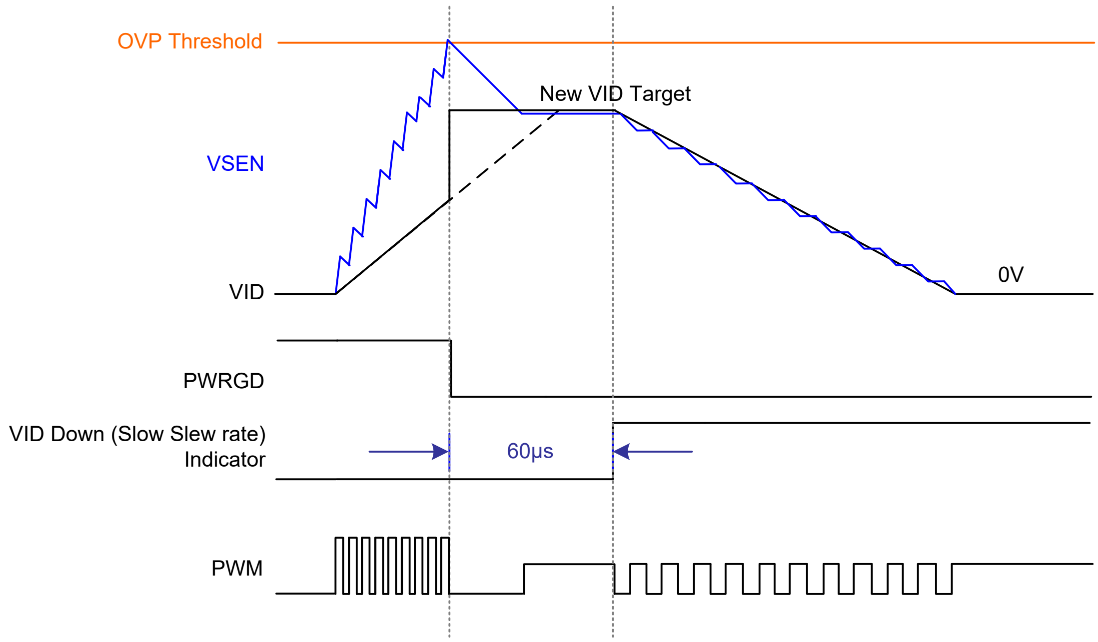


Figure 34. Overvoltage Protection Mechanism for VOTF up from 0V

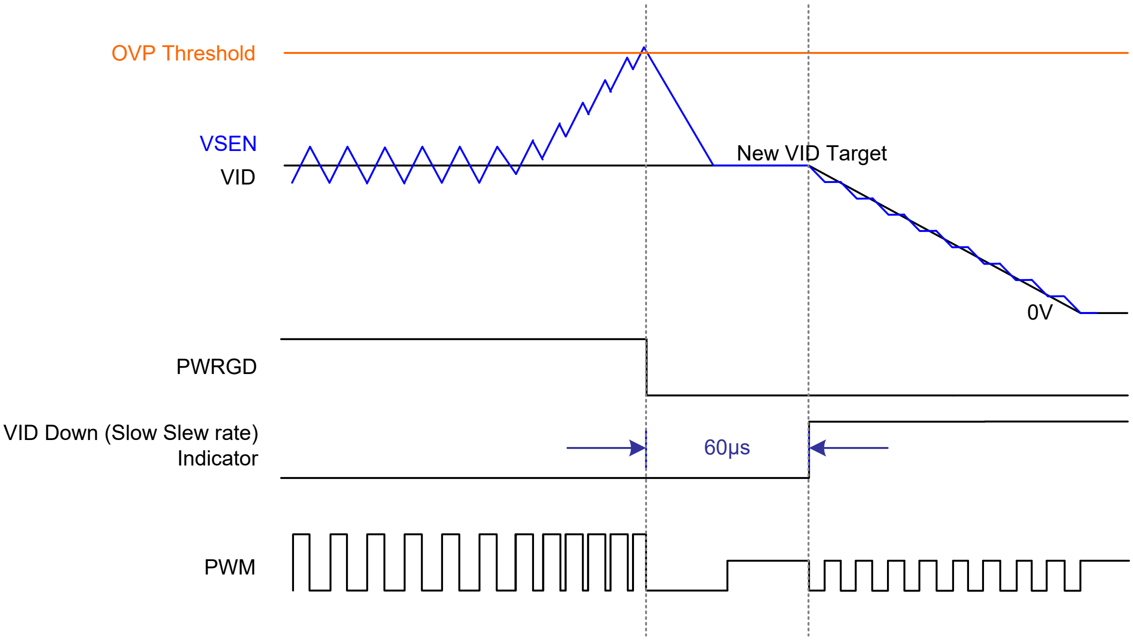


Figure 35. Overvoltage Protection Mechanism

18.11.13 Undervoltage Protection

The UVP threshold is linked with VID. The classification table is illustrated in Table 10. The UVP threshold (select via UVP_DELTA Reg0x2C[2:0]) is combined by the VID or VID_MIN (select via UVP_REF Reg0x2C[3]). Those parameters can be programmable through the SVI3 command. When the output voltage is lower than the UVP threshold with 3.3µs filter time, UVP is triggered and PWRGD is de-asserted and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during the VOTF period and 80µs after VID settles. The mechanism is illustrated in Figure 36.

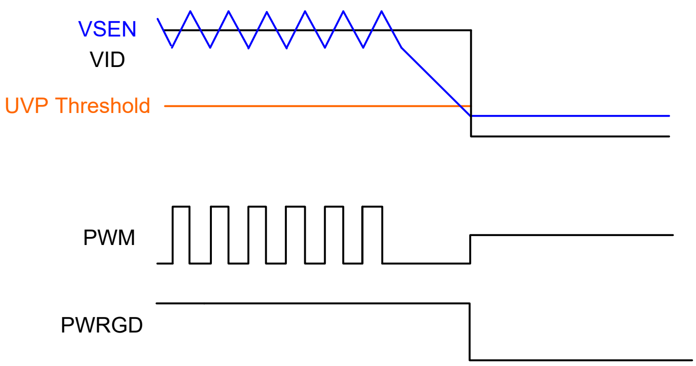


Figure 36. Undervoltage Protection Mechanism

Table 10. Summary of UVP Protection

<table>
<tr><th>VID Condition</th><th>OVP Threshold</th><th>Protection Action</th><th>Protection Reset</th></tr>
<tr><td>VID = 0</td><td>UVP is masked.</td><td></td><td rowspan="5">VCC/PWREN Toggle</td></tr>
<tr><td>VOTF period from zero/non-zero VID</td><td>(VOTF period) UVP is masked

0x2C[3] = 0b: VID
UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET
(MIN_VOUT_SUPPORTED ≤ VID + VOUT_OFFSET + I2C_VOUT_OFFSET)

0x2C[3] = 1b: VID_MIN
UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET
(MIN_VOUT_SUPPORTED ≤ VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET)
(If VID_MIN = 0V, MIN_VOUT_SUPPORTED is used to calculate UVP threshold. UVP_th = MIN_VOUT_SUPPORTED - UVP_DELTA)</td><td rowspan="3">PWRGD de-assertion. all PWMs are in tri-state to turn off high-side and low-side power MOSFETs.</td></tr>
<tr><td>VID≠0</td><td>VID or VID_MAX(select via 0x2C[3])

0x2C[3] = 0b: VID
UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET
(MIN_VOUT_SUPPORTED ≤ VID + VOUT_OFFSET + I2C_VOUT_OFFSET)

0x2C[3] = 1b: VID_MIN
UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET
(MIN_VOUT_SUPPORTED ≤ VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET)
(If VID_MIN = 0V, MIN_VOUT_SUPPORTED is used to calculate UVP threshold. UVP_th = MIN_VOUT_SUPPORTED - UVP_DELTA)</td></tr>
<tr><td>VOTF period from zero/non-zero VID in VFIX mode</td><td>(VOTF period) UVP is masked
(I2C VFIX Mode) VFIX_EN = 1b: Enable
UVP_TH = VFIX - UVP_DELTA</td></tr>
</table>

VID≠0 in VFIX mode	**(I2C VFIX Mode) VFIX_EN = 1b: Enable** UVP_TH = VFIX - UVP_DELTA		

18.12 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-

ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-60L 7x7 package, the thermal resistance, θ_{JA}, is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C)/(25.5°C/W) = 3.92W for a WQFN-60L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 37 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

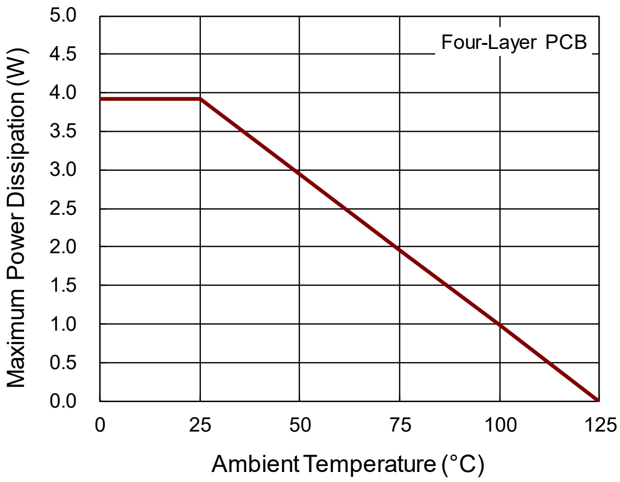


Figure 37. Derating Curve of Maximum Power Dissipation

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

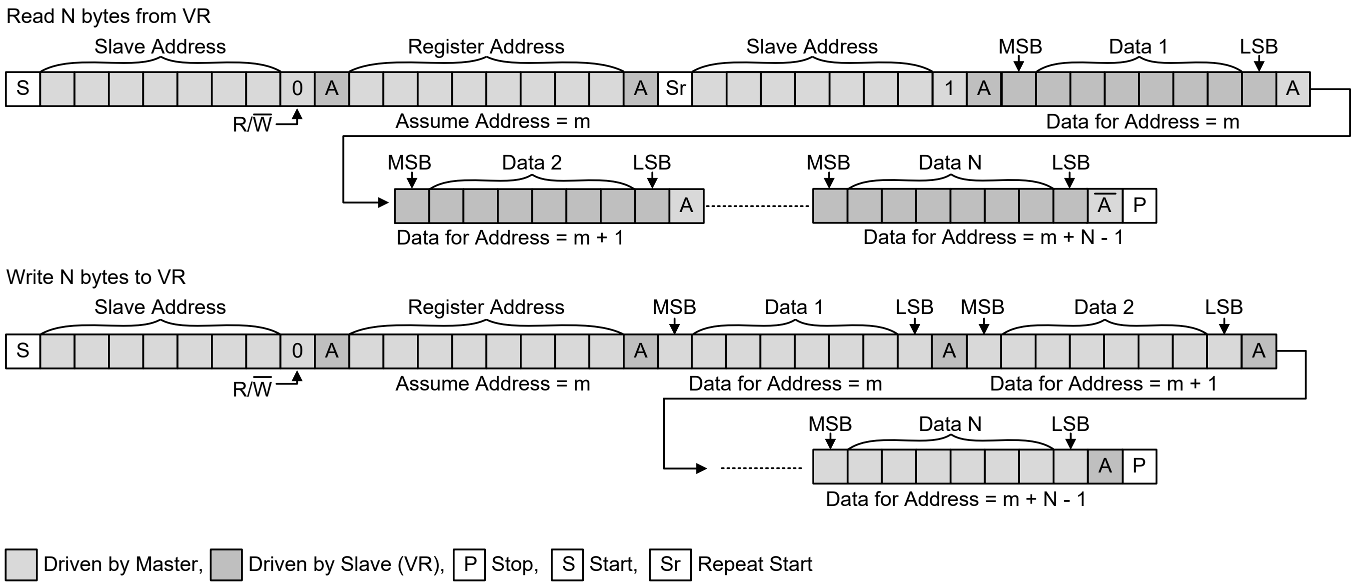
19 Functional Register Description

19.1 I^2C Interface

The I^2C slave address = 0x20, 0x21, 0x22 or 0x23 by CONFIG pin set.

This I^2C does not have a stretch function.

The I^2C interface supports standard slave mode (100 kbps), and fast mode (400 kbps). The write or read bit stream (N>1) is shown below:



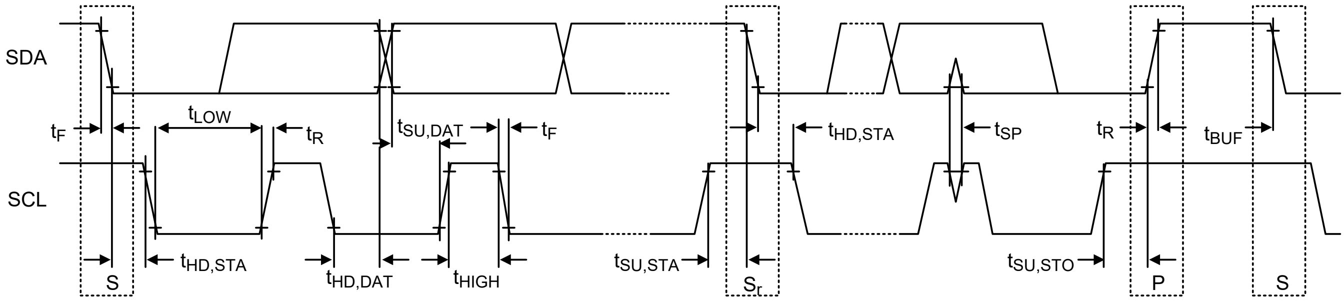


Table 11. Register Map

Register Address	NAME	Type	PAGED	Default Value	NVM
DFh	WDR	R/W	No	0x03	Yes(GP1)
ECh	NVM_PROGRAM_STATUS	R	No	Current status	No
EDh	STORE_RESTORE_CFG	W	No	0x00	No
EFh	PAGE	R/W	No	0x03	No
FBh	PRODUCT_ID	R	No	0x74	No
FCh	MODEL_ID	R	No	0x03	No

Register Address: DFh
Description: Watchdog-reset status, enable/disable watchdog function and setting watchdog-reset period.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	WDR							
Default Value	0x03							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7]	WATCHDOG_STATUS	**Watchdog-Reset Status** [7] = 0: Normal SMBus transmission [7] = 1: SMBus transmission hanging exceeds watchdog-reset period
[6:2]	Reserved	Reserved bits
[1]	EN_WATCHDOG_RESET	**Enable/Disable watchdog function** [1] = 0: Disable Watchdog-Reset (If SMBus transition hanging exceeds 30ms, VR I^2C interface state machine is reset but all registers keep the latest value.) [1] = 1: Enable Watchdog-Reset (Watchdog period is based on WATCHDOG_RESET_PERIOD[0] setting. When SMBus transmission hanging exceeds the setting, all I^2C registers reset to the default value. (Default)The default value can be set by NVM.
[0]	WATCHDOG_RESET_PERIOD	**Watchdog-Reset period** [0] = 0: 800ms [0] = 1: 1600ms (Default) The default value can be set by NVM.

Register Address: ECh
Description: NVM status indicator.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NVM_PROGRAM_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7]	RESTORE_FLAG	[7] = 1: Restore done.
[6]	STORE_FLAG	[6] = 1: Store done.
[5]	STORE_ALLOW	[5] = 1: Allow to store.
[4]	RESTORE_BUSY	[4] = 1: NVM restore busy.
[3]	STORE_BUSY	[3] = 1: NVM store busy.
[2]	CRC_GROUP_0	[2] = 1: GROUP_0 (Page 03, 04 and 05) check fails.
[1]	CRC_GROUP_1	[1] = 1: GROUP_1 (Page 02) check fails.
[0]	CRC_GP0_GP1	[0] = 1: Group 0 or group 1 check fails.

Register Address: EDh **Description**: Store command instructs the device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory. Restore command instructs the device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory. This command should only be used while all outputs are disabled.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	STORE_RESTORE_CFG							
Default Value	0x00							
Read/Write	W	W	W	W	W	W	W	W

Bits	**Name**	**Description**
[7:0]	STORE_RESTORE_CFG	[7:0] = 66h: Restore all storable register settings from NVM. [7:0] = AAh: Store all current storable register settings into NVM as new defaults. All other combinations are not defined.

Register Address: EFh **Description**: The PAGE command provides the ability to configure, control and monitor multiple PWM channels through only one physical address. Each PAGE contains the operating commands for one PWM channel.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PAGE							
Default Value	0x03							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	Channel	[7:0] = 02h: All rail setting functions (Page 02). [7:0] = 03h: rail A (Page 03). [7:0] = 04h: rail B (Page 04). [7:0] = 05h: rail C (Page 05). All other combinations are not defined.

Register Address: FBh **Description**: The Product_ID command indicates the device code is 74 - code identifier for RT3674AJ.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Product_ID							
Default Value	0x74							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	Product_ID	[7:0] = 74h

Register Address: FCh **Description**: Unique model code defined by manufacturer. (Same as SVI3 Reg. 03h.)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MODEL_ID							
Default Value	0x03							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	MODEL_ID	[7:0] = 03h

Register Map Rail A (Page 03)

Register Address	NAME	Type	PAGED	Default Value	NVM
74h	CBG1_A	R/W	Yes	0x04	Yes(GP1)
75h	CBG2_A	R/W	Yes	0x04	Yes(GP1)
76h	CBG3_A	R/W	Yes	0x04	Yes(GP1)
77h	CBG4_A	R/W	Yes	0x04	Yes(GP1)
80h	I2C_VOUT_OFS_A	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_A	R/W	Yes	0x00	No
82h	VFIX_LSB_A	R/W	Yes	0x83	No
83h	VFIX_MSB_A	R/W	Yes	0x00	No
84h	FORCE_PSI0_A	R/W	Yes	0x00	No
85h	EN_PRT_A	R/W	Yes	0x7F	No
86h	LL_SEL_A	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_A	R	Yes	Current status	No
88h	IOUT_RPT_LSB_A	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_A	R/W	Yes	0x00	No
8Ah	TEMP_RPT_A	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_A	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_A	R	Yes	Current status	No
8Dh	PRT_FLAG_A	R/W	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_A	R	Yes	Current status	No
A2h	VFIX_MAX_LSB_A	R/W	Yes	0xFF	No
A3h	VFIX_MAX_MSB_A	R/W	Yes	0x01	No
A4h	OCP_WARN_HYS_A	R/W	Yes	0x00	Yes(GP1)
A5h	MISC_A	R/W	Yes	0x00	Yes(GP1)
A6h	VRHOT_TH_A	R/W	Yes	0x8C	Yes(GP1)
A7h	OTP_TH_A	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

Register Address: 74h
Description: Adjustment phase1 current balance gain of rail A.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CBG1_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	Name	Description
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).

Register Address: 75h **Description**: Adjustment phase2 current balance gain of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CBG2_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).

Register Address: 76h **Description**: Adjustment phase3 current balance gain of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CBG3_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).

Register Address: 77h **Description**: Adjustment phase4 current balance gain of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CBG4_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).

Register Address: 80h Description: Setting VOUT offset of rail A. The capability of controller is 0.25V~2.8V. (i.e. 0.25V ≤ VID setting ± SVI3 VOUT_OFFSET ± I2C VOUT_OFFSET ≤ 2.8V). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/μs. The VR begins ramping up and return to PSI0 when setting VOUT offset. PSI state returns to the original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VOUT_OFS_A							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OFS	[7:0] = 00h: no offset [7]: sign bit (as part of two's complement) [6:0]: 5mV/step [e.g.] 00000001 = current VID + (1 x VID step) 00000011 = current VID + (3 x VID steps) 11111111 = current VID - (1 x VID step) The default value can be set by NVM.(Page 03)

Register Address: 81h Description: Enable/Disable fixed VID mode of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_VFIX_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

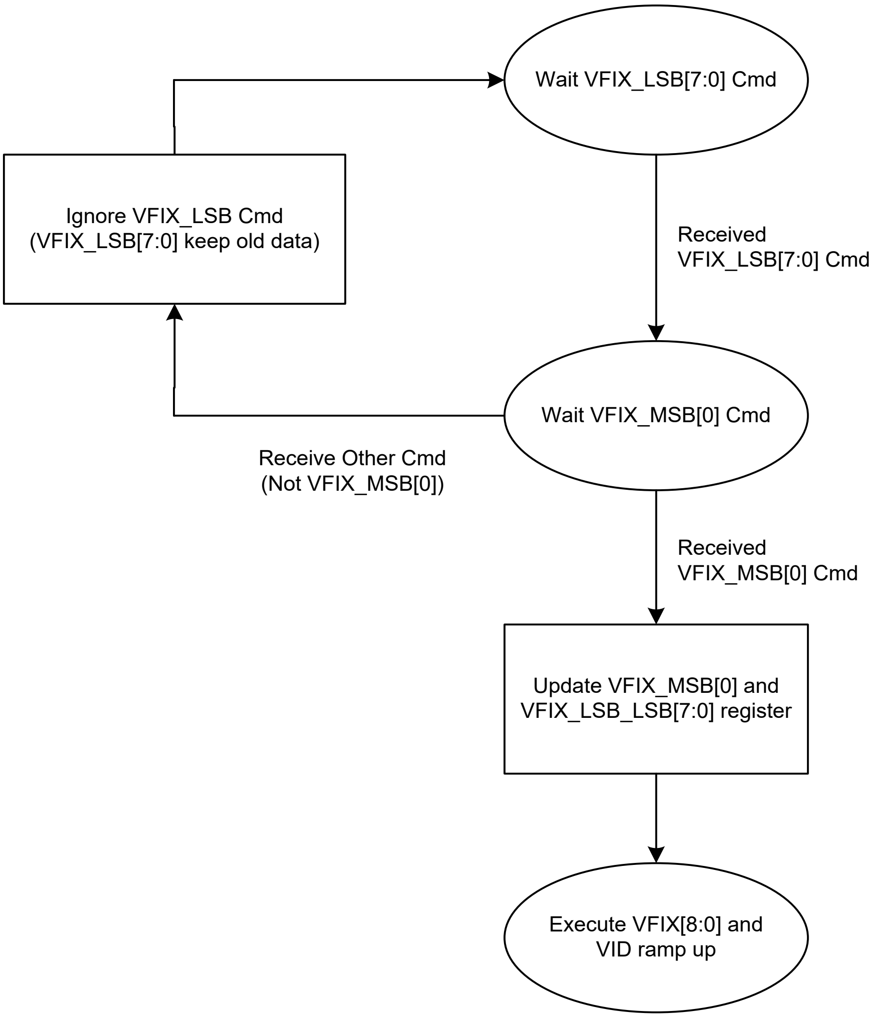
Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	EN_VFIX	[0] = 0: Disable fixed VID mode [0] = 1: Enable fixed VID mode

Register Address: 82h Description: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail A. In fixed VID mode, VR skips VID packet and changes PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_LSB_A							
Default Value	0x83							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VFIX_LSB	VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receives an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 83h **Description**: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail A. In fixed VID mode, VR skips VID packet and changes PSI commands. While Fixed VID is enable, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MSB_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MSB	VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receives an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.



Register Address: 84h **Description**: Enable/Disable FORCE_PSI0 function of rail A, and the controller still operates in PSI0 when change PSI command is received. The PSI status follow SVI3.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Force_PSI0_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	FORCE_PSI0	[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.

Register Address: 85h **Description**: Enable/Disable protection function of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PRT_A							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	EN_VRHOT	[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)
[5]	EN_OTP	[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)
[4]	EN_OCP_WARN	[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).
[3]	EN_OCP_SUM	[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).
[2]	EN_NV	[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)
[1]	EN_UV	[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)
[0]	EN_OV	[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)

Register Address: 86h Description: Selection load-line of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LL_SEL_A							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	SVI3_I2C_LL_SEL	It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C
[6:5]	Reserved	Reserved bits
[4:0]	SEL_LL	Load-line adjustment relative to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)

Register Address: 87h Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_A. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_MSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

egister Address: 88h Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_A. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_LSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address: 89h **Description**: Output current reporting ratio adjustment of SVI3 telemetry for rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_RATIO_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT_RATIO	[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%

Register Address: 8Ah **Description**: Temperature reporting of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEMP_RPT_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	TEMP_RPT	Temperature(℃) = TEMP_RPT[7:0]-40

Register Address: 8Bh **Description**: Output voltage reporting data payloads consist of 10 bits for rail A. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_MSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Ch **Description**: Output voltage reporting data payloads consist of 10 bits for rail A. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_LSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Dh **Description**: Protection indicator of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRT_FLAG_A							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	VRHOT assertion	[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.
[5]	OCP_WARN assertion	[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.
[4]	OTP	[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP
[3]	UVP	[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP
[2]	OVP	[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP
[1]	OCP	[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP
[0]	SSOCP	[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP

Register Address: 8Eh **Description**: SVI3 NACKs states of rail A. (Same as SVI3 Reg. 11h.)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SVI3_NACK_STATUS_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved bits
[5:0]	SVI3_NACK_STATUS	[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable/Not Supported

Register Address: A2h **Description**: 9-bit fixed VID (Reg. A2h + Reg. A3h). Set maximum voltage in fixed VID mode of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_LSB_A							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VFIX_MAX_LSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receives an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: A3h **Description**: 9-bit fixed VID (Reg. A2h + Reg. A3h). Set maximum voltage in fixed VID mode of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_MSB_A							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MAX_MSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receives an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: A4h **Description**: It is used to set overcurrent warning hysteresis of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCP_WARN_HYS_A							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OCP_WARN_HYS	1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 03).

Register Address: A5h **Description**: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I^2C_VRHOT and SVI3_I^2C_OTP.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MISC_A							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:4]	Reserved	Reserved bits
[3]	IGNORE_PSI7	[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 03).
[2]	FORCE_PSI7	[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enable smart phase management function. The SVI3 Register PSI state follow SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 03).
[1]	SVI3_I2C_VRHOT	It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I^2C The default value can be set by NVM. (Page 03).
[0]	SVI3_I2C_OTP	It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I^2C The default value can be set by NVM. (Page 03).

VR Operation Mode:

FORCE_PSI0	**IGNORE_PSI7**	**FORCE_PSI7**	**VR Operation mode**
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	**Enable**	Force PSI7.
Disable	**Enable**	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	**Enable**	**Enable**	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	**Enable**	Force PSI0.
Enable	**Enable**	**Disable**	Force PSI0.
Enable	**Enable**	**Enable**	Force PSI0.

Register Address: A6h **Description**: It is used to set VRHOT threshold of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VRHOT_TH_A							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VRHOT_TH	Voltage regulator hot warning threshold when control mode is I^2C. VRHOT Threshold = Reg[7:0]-40℃ [7:0] = 00h: Disabled [7:0] = 8Ch: 100°C (default) The default value can be set by NVM. (Page 03).

Register Address: A7h **Description**: It is used to set OTP threshold of rail A.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP_TH_A							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OTP_TH	Over-temperature protection threshold when control mode is I^2C. OTP Threshold = Reg[7:0]-40℃ [7:0] = 00h: Disabled [7:0] = A5h: 125°C (default) The default value can be set by NVM. (Page 03).

Register Address: A9h **Description**: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Register Address: AAh
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Register Map Rail B (Page 04)

Register Address	NAME	Type	PAGED	Default Value	NVM
80h	I2C_VOUT_OFS_B	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_B	R/W	Yes	0x00	No
82h	VFIX_LSB_B	R/W	Yes	0x83	No
83h	VFIX_MSB_B	R/W	Yes	0x00	No
84h	FORCE_PSI0_B	R/W	Yes	0x00	No
85h	EN_PRT_B	R/W	Yes	0x7F	No
86h	LL_SEL_B	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_B	R	Yes	Current status	No
88h	IOUT_RPT_LSB_B	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_B	R/W	Yes	0x00	No
8Ah	TEMP_RPT_B	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_B	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_B	R	Yes	Current status	No
8Dh	PRT_FLAG_B	R/W	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_B	R	Yes	Current status	No
9Ch	VFIX_MAX_LSB_B	R/W	Yes	0xFF	No
9Dh	VFIX_MAX_MSB_B	R/W	Yes	0x01	No
9Eh	OCP_WARN_HYS_B	R/W	Yes	0x00	Yes(GP1)
9Fh	MISC_B	R/W	Yes	0x00	Yes(GP1)
A1h	VRHOT_TH_B	R/W	Yes	0x8C	Yes(GP1)
A2h	OTP_TH_B	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

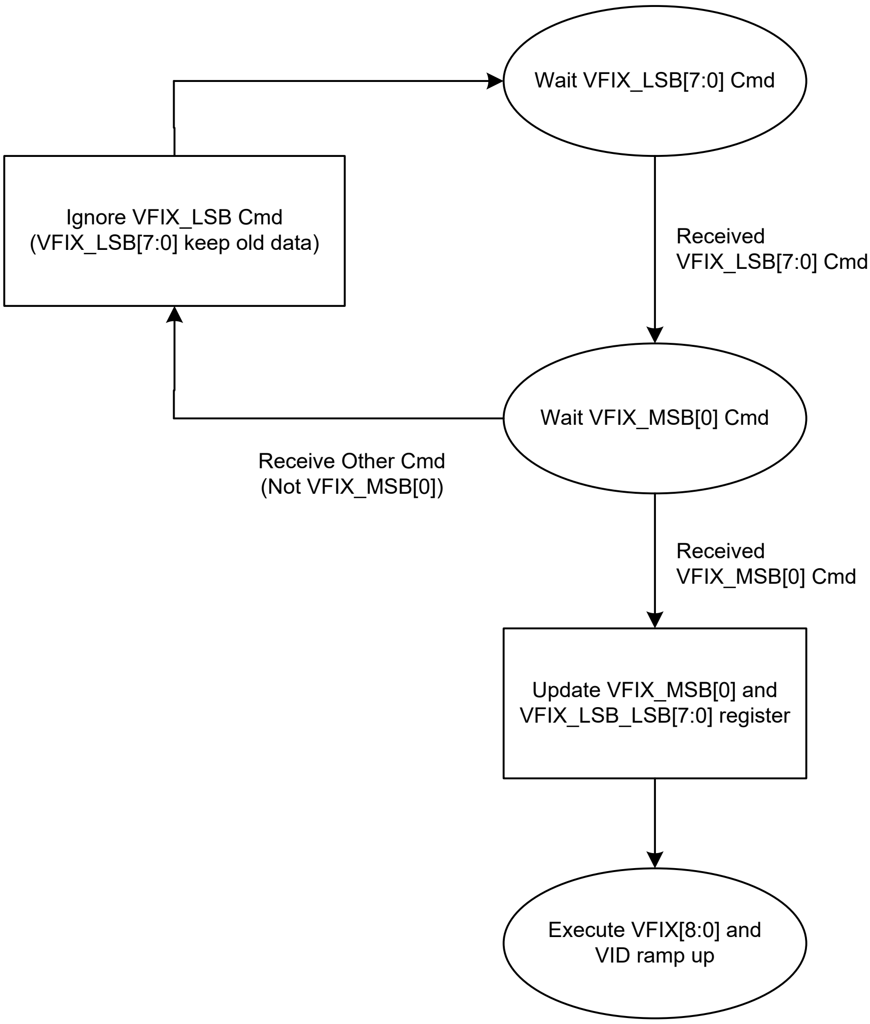
<table>
<tr><td colspan="9">Register Address: 80h
Description: Setting VOUT offset of rail B. The capability of controller is 0.25V~2.8V. (i.e. 0.25V ≤ VID setting ± SVI3 VOUT_OFFSET ± I2C VOUT_OFFSET ≤ 2.8V). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/μs. The VR begins ramping up and returns to PSI0 when setting VOUT offset. PSI state returns to original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.</td></tr>
<tr><td>Bits</td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>Name</td><td colspan="8">I2C_VOUT_OFS_B</td></tr>
<tr><td>Default Value</td><td colspan="8">0x00</td></tr>
<tr><td>Read/Write</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
<tr><td>Bits</td><td colspan="2">Name</td><td colspan="6">Description</td></tr>
<tr><td>[7:0]</td><td colspan="2">OFS</td><td colspan="6">[7:0] = 00h: no offset
[7]: sign bit (as part of two's complement)
[6:0]: 5mV/step
[e.g.]
00000001 = current VID + (1 x VID step)
00000011 = current VID + (3 x VID steps)
11111111 = current VID - (1 x VID step)
The default value can be set by NVM. (Page 04).</td></tr>
</table>

<table>
<tr><td colspan="9">Register Address: 81h
Description: Enable/Disable fixed VID mode of rail B.</td></tr>
<tr><td>Bits</td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>Name</td><td colspan="8">EN_VFIX_B</td></tr>
<tr><td>Default Value</td><td colspan="8">0x00</td></tr>
<tr><td>Read/Write</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td>RW</td></tr>
<tr><td>Bits</td><td colspan="2">Name</td><td colspan="6">Description</td></tr>
<tr><td>[7:1]</td><td colspan="2">Reserved</td><td colspan="6">Reserved bits</td></tr>
<tr><td>[0]</td><td colspan="2">EN_VFIX</td><td colspan="6">[0] = 0: Disable fixed VID mode
[0] = 1: Enable fixed VID mode</td></tr>
</table>

<table>
<tr><td colspan="9">Register Address: 82h
Description: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail B. In fixed VID mode, VR skips VID packet and change PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.</td></tr>
<tr><td>Bits</td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>Name</td><td colspan="8">VFIX_LSB_B</td></tr>
<tr><td>Default Value</td><td colspan="8">0x83</td></tr>
<tr><td>Read/Write</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
<tr><td>Bits</td><td colspan="2">Name</td><td colspan="6">Description</td></tr>
<tr><td>[7:0]</td><td colspan="2">VFIX_LSB</td><td colspan="6">VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0]
Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h)
Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.</td></tr>
</table>

Register Address: 83h									
Description: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail B. In fixed VID mode, VR skips VID packet and change PSI commands. While Fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.									
Bits		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name		VFIX_MSB_B							
Default Value		0x00							
Read/Write		R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MSB	VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.



Register Address: 84h **Description**: Enable/Disable FORCE_PSI0 function of rail B, and the controller still operates in PSI0 when change PSI command is received. The PSI status follows SVI3.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Force_PSI0_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	FORCE_PSI0	[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.

Register Address: 85h **Description**: Enable/Disable protection function of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PRT_B							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	EN_VRHOT	[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)
[5]	EN_OTP	[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)
[4]	EN_OCP_WARN	[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).
[3]	EN_OCP_SUM	[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).
[2]	EN_NV	[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)
[1]	EN_UV	[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)
[0]	EN_OV	[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)

Register Address: 86h **Description**: Selection load-line of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LL_SEL_B							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	SVI3_I2C_LL_SEL	It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C
[6:5]	Reserved	Reserved bits
[4:0]	SEL_LL	Load-line adjustment corresponding to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)

Register Address: 87h **Description**: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_B. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_MSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT/1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address: 88h **Description**: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_B. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_LSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT/1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address: 89h **Description**: Output current reporting ratio adjustment of SVI3 telemetry for rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_RATIO_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT_RATIO	[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%

Register Address: 8Ah **Description**: Temperature reporting of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEMP_RPT_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	TEMP_RPT	Temperature(℃) = TEMP_RPT[7:0]-40

Register Address: 8Bh **Description**: Output voltage reporting data payloads consist of 10 bits for rail B. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_MSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Ch **Description**: Output voltage reporting data payloads consist of 10 bits for rail B. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_LSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Dh Description: Protection indicator of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRT_FLAG_B							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	VRHOT assertion	[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.
[5]	OCP_WARN assertion	[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.
[4]	OTP	[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP
[3]	UVP	[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP
[2]	OVP	[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP
[1]	OCP	[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP
[0]	SSOCP	[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP

Register Address: 8Eh Description: SVI3 NACKs states of rail B. (Same as SVI3 Reg. 11h.)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SVI3_NACK_STATUS_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved bits
[5:0]	SVI3_NACK_STATUS	[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable/Not Supported

Register Address: 9Ch **Description**: 9-bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_LSB_B							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VFIX_MAX_LSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 9Dh **Description**: 9-bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_MSB_B							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MAX_MSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 9Eh **Description**: It is used to set overcurrent warning hysteresis of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCP_WARN_HYS_B							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OCP_WARN_HYS	1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 04).

Register Address: 9Fh **Description**: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I^2C_VRHOT and SVI3_I^2C_OTP.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MISC_B							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:4]	Reserved	Reserved bits
[3]	IGNORE_PSI7	[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 04).
[2]	FORCE_PSI7	[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enables smart phase management function. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 04).
[1]	SVI3_I2C_VRHOT	It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I^2C The default value can be set by NVM. (Page 04).
[0]	SVI3_I2C_OTP	It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I^2C The default value can be set by NVM. (Page 04).

VR Operation Mode:

FORCE_PSI0	**IGNORE_PSI7**	**FORCE_PSI7**	**VR Operation mode**
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	**Enable**	Force PSI7.
Disable	**Enable**	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	**Enable**	**Enable**	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	**Enable**	Force PSI0.
Enable	**Enable**	**Disable**	Force PSI0.
Enable	**Enable**	**Enable**	Force PSI0.

Register Address: A1h Description: It is used to set VRHOT threshold of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VRHOT_TH_B							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VRHOT_TH	Voltage regulator hot warning threshold when control mode is I^2C. VRHOT Threshold = Reg[7:0]-40℃ [7:0] = 00h: Disabled [7:0] = 8Ch: 100°C (default) The default value can be set by NVM. (Page 04).

Register Address: A2h Description: It is used to set OTP threshold of rail B.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP_TH_B							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OTP_TH	Over-temperature protection threshold when control mode is I^2C. OTP Threshold = Reg[7:0]-40℃ [7:0] = 00h: Disabled [7:0] = A5h: 125°C (default) The default value can be set by NVM. (Page 04).

Register Address: A9h Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Register Address: AAh

Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Register Map Rail C (Page 05)

Register Address	NAME	Type	PAGED	Default Value	NVM
80h	I2C_VOUT_OFS_C	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_C	R/W	Yes	0x00	No
82h	VFIX_LSB_C	R/W	Yes	0x83	No
83h	VFIX_MSB_C	R/W	Yes	0x00	No
84h	FORCE_PSI0_C	R/W	Yes	0x00	No
85h	EN_PRT_C	R/W	Yes	0x7F	No
86h	LL_SEL_C	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_C	R	Yes	Current status	No
88h	IOUT_RPT_LSB_C	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_C	RW	Yes	0x00	No
8Ah	TEMP_RPT_C	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_C	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_C	R	Yes	Current status	No
8Dh	PRT_FLAG_C	R	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_C	R	Yes	Current status	No
9Ch	VFIX_MAX_LSB_C	R/W	Yes	0xFF	No
9Dh	VFIX_MAX_MSB_C	R/W	Yes	0x01	No
9Eh	OCP_WARN_HYS_C	R/W	Yes	0x00	Yes(GP1)
9Fh	MISC_C	R/W	Yes	0x00	Yes(GP1)
A1h	VRHOT_TH_C	R/W	Yes	0x8C	Yes(GP1)
A2h	OTP_TH_C	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

Register Address: 80h **Description**: Setting VOUT offset of rail C. The capability of controller is 0.25V to 2.8V. (i.e. 0.25V ≤ VID setting ± SVI3 VOUT_OFFSET ± I2C VOUT_OFFSET ≤ 2.8V). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/μs. The VR begins ramping up and returns to PSI0 when setting VOUT offset. PSI state returns to original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VOUT_OFS_C							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OFS	[7:0] = 00h: no offset [7]: sign bit (as part of two's complement) [6:0]: 5mV/step [e.g.] 00000001 = current VID + (1 x VID step) 00000011 = current VID + (3 x VID steps) 11111111 = current VID - (1 x VID step) The default value can be set by NVM. (Page 05).

Register Address: 81h **Description**: Enable/Disable fixed VID mode of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_VFIX_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

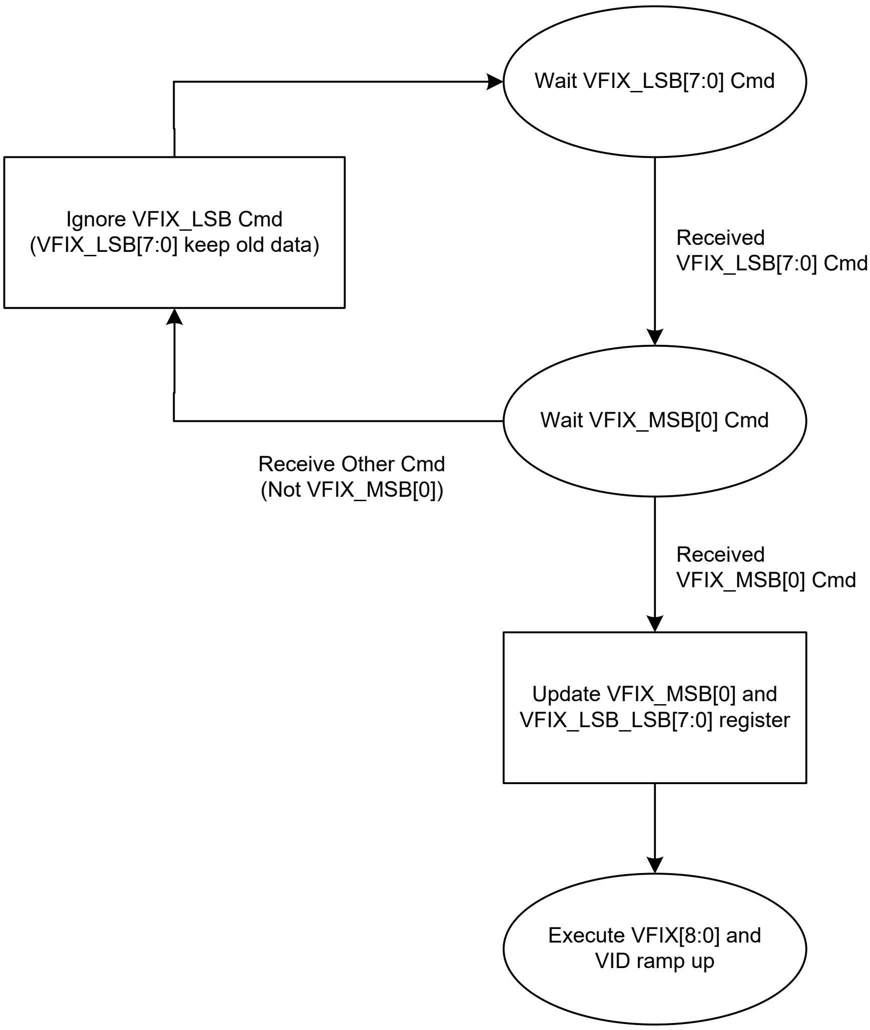
Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	EN_VFIX	[0] = 0: Disable fixed VID mode [0] = 1: Enable fixed VID mode

Register Address: 82h **Description**: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips VID packet and change PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_LSB_C							
Default Value	0x83							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VFIX_LSB	VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 83h **Description**: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips VID packet and change PSI commands. While Fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MSB_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MSB	VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.



Register Address: 84h **Description**: Enable/Disable FORCE_PSI0 function of rail C, and the controller still operates in PSI0 when change PSI command is received. The PSI status follows SVI3.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Force_PSI0_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	FORCE_PSI0	[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.

Register Address: 85h **Description**: Enable/Disable protection function of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PRT_C							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	EN_VRHOT	[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)
[5]	EN_OTP	[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)
[4]	EN_OCP_WARN	[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).
[3]	EN_OCP_SUM	[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).
[2]	EN_NV	[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)
[1]	EN_UV	[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)
[0]	EN_OV	[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)

Register Address: 86h Description: Selection load-line of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LL_SEL_C							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW

Bits	Name	Description
[7]	SVI3_I2C_LL_SEL	It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C
[6:5]	Reserved	Reserved bits
[4:0]	SEL_LL	Load-line adjustment corresponding to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)

Register Address: 87h Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_C. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_MSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address: 88h Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_C. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_LSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	IOUT_RPT	IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT\_RPT[9:0] \times MAX\_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address: 89h **Description**: Output current reporting ratio adjustment of SVI3 telemetry for rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_RATIO_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	IOUT_RPT_RATIO	[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%

Register Address: 8Ah **Description**: Temperature reporting of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEMP_RPT_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	TEMP_RPT	Temperature(°C) = TEMP_RPT[7:0]–40

Register Address: 8Bh **Description**: Output voltage reporting data payloads consist of 10 bits for rail C. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_MSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Ch **Description**: Output voltage reporting data payloads consist of 10 bits for rail C. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_LSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	VOUT_RPT	VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]×5mV

Register Address: 8Dh **Description**: Protection indicator of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRT_FLAG_C							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6]	VRHOT assertion	[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.
[5]	OCP_WARN assertion	[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.
[4]	OTP	[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP
[3]	UVP	[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP
[2]	OVP	[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP
[1]	OCP	[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP
[0]	SSOCP	[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP

Register Address: 8Eh **Description**: SVI3 NACKs states of rail C. (Same as SVI3 Reg. 11h.)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SVI3_NACK_STATUS_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved bits
[5:0]	SVI3_NACK_STATUS	[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable/Not Supported

Register Address: 9Ch **Description**: 9 bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_LSB_C							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VFIX_MAX_LSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 9Dh **Description**: 9 bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_MSB_C							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	VFIX_MAX_MSB	VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.

Register Address: 9Eh **Description**: It is used to set overcurrent warning hysteresis of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCP_WARN_HYS_C							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OCP_WARN_HYS	1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 05).

Register Address: 9Fh **Description**: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I2C_VRHOT and SVI3_I2C_OTP.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MISC_C							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:4]	Reserved	Reserved bits
[3]	IGNORE_PSI7	[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 05).
[2]	FORCE_PSI7	[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enables smart phase management function. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 05).
[1]	SVI3_I2C_VRHOT	It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I2C The default value can be set by NVM. (Page 05).
[0]	SVI3_I2C_OTP	It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I2C The default value can be set by NVM. (Page 05).

VR Operation mode:

FORCE_PSI0	**IGNORE_PSI7**	**FORCE_PSI7**	**VR Operation mode**
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	**Enable**	Force PSI7.
Disable	**Enable**	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	**Enable**	**Enable**	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	**Enable**	Force PSI0.
Enable	**Enable**	**Disable**	Force PSI0.
Enable	**Enable**	**Enable**	Force PSI0.

Register Address: A1h Description: It is used to set VRHOT threshold of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VRHOT_TH_C							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	VRHOT_TH	Voltage regulator hot warning threshold when control mode is I^2C. VRHOT Threshold = Reg[7:0]–40°C [7:0] = 00h: Disabled [7:0] = 8Ch: 100℃ (default) The default value can be set by NVM. (Page 05).

Register Address: A2h Description: It is used to set OTP threshold of rail C.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP_TH_C							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OTP_TH	Over-temperature protection threshold when control mode is I^2C. OTP_TH Threshold = Reg[7:0]–40°C [7:0] = 00h: Disabled [7:0] = A5h: 125℃ (default) The default value can be set by NVM. (Page 05).

Register Address: A9h Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:2]	Reserved	Reserved bits
[1:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Register Address: AAh
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	PSYS_RPT	PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale

Table 12. SVI3 Registers for SVI3 Protocol

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
01h	[7:0]	SVI3_VERSION	R	01h	Rev.1
02h	[7:5]	TYPE_ID	R	000b	Type 1
	[4:0]	MGF_ID	R	04h	04h = Richtek
03h	[7:0]	MODEL_ID	R	03h	
04h	[7:0]	TEN_BIT_TEL_AVAIL	R	47h	System Power, Temp 1, Output voltage and Output current of 10-bit telemetry are available.
05h	[7:0]	SIXTEEN_BIT_TEL_AVAIL	R	00h	Reserved
06h	[7]	CRC_ENABLED	R	1b	CRC is enabled
	[4:2]	PSI	R	000b	PSI0. Indicates the PSI state of the controller.
	[0]	VID[8]	R	Platform	Indicates the MSB of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
07h	[7:0]	VID[7:0]	R	Platform	Indicates the 8 LSBs of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
08h	[5:4]	DEFAULT_SLEW_RATE	R	Platform	NVM configurable, based on platform
	[3:0]	VID_DEFAULT_VOLTAGE	R	Platform	NVM configurable, based on platform
09h	[7:6]	V_IN_SCALE	R	00b	Not support
	[5:3]	I_OUT_SCALE	R	Platform	NVM configurable, based on platform
	[2:0]	I_IN_SCALE	R	000b	Not support
0Ah	[7:0]	MAX_VOUT_SUPPORTED	R	8Ch	MAX_VOUT_SUPPORTED = 2.8V
0Bh	[7:0]	MIN_VOUT_SUPPORTED	R	32h	MIN_VOUT_SUPPORTED = 0.25V
0Ch	[2:0]	P_SYS_SCALE	R	Platform	NVM configurable, based on platform
10h	[7:0]	FAULT_STATUS	R	Current status	
11h	[7:0]	NACK_STATUS	R	Current status	
20h	[7:5]	DECAY_CONDITIONS	R/W	000b	Down voltage decay disabled
	[4]	DOWN_SLEW_RATE	R/W	0b	Negative slew rate = positive slew rate
	[3:0]	UP_SLEW_RATE	R/W	Platform	Copied from DEFAULT_SLEW_RATE
21h	[4:0]	LL_ADJUST	R/W	01010b	100%
22h	[7:0]	VOUT_OFFSET	R/W	00h	No offset
23h	[7:0]	VID_MAX	R/W	00h	Disabled
24h	[7:0]	VID_MIN	R/W	00h	Disabled
25h	[7:0]	TEN_BIT_TEL_EN	R/W	00h	Disabled
26h	[7:0]	SIXTEEN_BIT_TEL_EN	R/W	00h	Reserved
27h	[7:0]	OCP_THRESH	R/W	Platform	NVM configurable, based on platform
28h	[7:0]	OCP_WARN_THRESH	R/W	Platform	NVM configurable, based on platform
29h	[7:3]	OCP_WARN_MIN_PULSE	R/W	Platform	NVM configurable, based on platform

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
	[2:0]	OCP_FAULT_DELAY	R/W	Platform	NVM configurable, based on platform
2Ah	[7:0]	VRHOT_THRESH	R/W	8Ch	100°C
2Bh	[7:0]	OTP_THRESH	R/W	A5h	125°C
2Ch	[7]	OVP_REF	R/W	0b	VID
	[6:4]	OVP_DELTA	R/W	110b	350mV
	[3]	UVP_REF	R/W	0b	VID
	[2:0]	UVP_DELTA	R/W	110b	350mV
2Dh	[7:4]	PHASE_SHED_1	R/W	0001b	1-phase when slave is in PSI1
	[3:0]	PHASE_SHED_2	R/W	0001b	1-phase when slave is in PSI2
40h	[7:0]	DEBUG_ENABLED	R/W	00h	
41h	[7:0]	DEBUG_TEMP1_OVERRIDE	R/W	00h	
42h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
43h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
44h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
45h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
46h	[2:0]	DEBUG_OUTPUT_OVERRIDE	R/W	000b	
50h	[7:0]	GEN_PURPOSE_0	R/W	00b	
51h	[7:0]	GEN_PURPOSE_1	R/W	00b	
52h	[7:0]	GEN_PURPOSE_2	R/W	00b	
53h	[7:0]	GEN_PURPOSE_3	R/W	00b	
54h	[7:0]	GEN_PURPOSE_4	R/W	00b	
55h	[7:0]	GEN_PURPOSE_5	R/W	00b	
56h	[7:0]	GEN_PURPOSE_6	R/W	00b	
57h	[7:0]	GEN_PURPOSE_7	R/W	00b	

Table 12. SVI3 Type 1 Slave VID Table

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
000000000	000	OFF	000100000	020	0.405	001000000	040	0.565	001100000	060	0.725
000000001	001	0.250	000100001	021	0.410	001000001	041	0.570	001100001	061	0.730
000000010	002	0.255	000100010	022	0.415	001000010	042	0.575	001100010	062	0.735
000000011	003	0.260	000100011	023	0.420	001000011	043	0.580	001100011	063	0.740
000000100	004	0.265	000100100	024	0.425	001000100	044	0.585	001100100	064	0.745
000000101	005	0.270	000100101	025	0.430	001000101	045	0.590	001100101	065	0.750
000000110	006	0.275	000100110	026	0.435	001000110	046	0.595	001100110	066	0.755
000000111	007	0.280	000100111	027	0.440	001000111	047	0.600	001100111	067	0.760
000001000	008	0.285	000101000	028	0.445	001001000	048	0.605	001101000	068	0.765
000001001	009	0.290	000101001	029	0.450	001001001	049	0.610	001101001	069	0.770
000001010	00A	0.295	000101010	02A	0.455	001001010	04A	0.615	001101010	06A	0.775
000001011	00B	0.300	000101011	02B	0.460	001001011	04B	0.620	001101011	06B	0.780
000001100	00C	0.305	000101100	02C	0.465	001001100	04C	0.625	001101100	06C	0.785
000001101	00D	0.310	000101101	02D	0.470	001001101	04D	0.630	001101101	06D	0.790
000001110	00E	0.315	000101110	02E	0.475	001001110	04E	0.635	001101110	06E	0.795
000001111	00F	0.320	000101111	02F	0.480	001001111	04F	0.640	001101111	06F	0.800
000010000	010	0.325	000110000	030	0.485	001010000	050	0.645	001110000	070	0.805
000010001	011	0.330	000110001	031	0.490	001010001	051	0.650	001110001	071	0.810
000010010	012	0.335	000110010	032	0.495	001010010	052	0.655	001110010	072	0.815
000010011	013	0.340	000110011	033	0.500	001010011	053	0.660	001110011	073	0.820
000010100	014	0.345	000110100	034	0.505	001010100	054	0.665	001110100	074	0.825
000010101	015	0.350	000110101	035	0.510	001010101	055	0.670	001110101	075	0.830
000010110	016	0.355	000110110	036	0.515	001010110	056	0.675	001110110	076	0.835
000010111	017	0.360	000110111	037	0.520	001010111	057	0.680	001110111	077	0.840
000011000	018	0.365	000111000	038	0.525	001011000	058	0.685	001111000	078	0.845
000011001	019	0.370	000111001	039	0.530	001011001	059	0.690	001111001	079	0.850
000011010	01A	0.375	000111010	03A	0.535	001011010	05A	0.695	001111010	07A	0.855
000011011	01B	0.380	000111011	03B	0.540	001011011	05B	0.700	001111011	07B	0.860
000011100	01C	0.385	000111100	03C	0.545	001011100	05C	0.705	001111100	07C	0.865
000011101	01D	0.390	000111101	03D	0.550	001011101	05D	0.710	001111101	07D	0.870
000011110	01E	0.395	000111110	03E	0.555	001011110	05E	0.715	001111110	07E	0.875
000011111	01F	0.400	000111111	03F	0.560	001011111	05F	0.720	001111111	07F	0.880

Continued

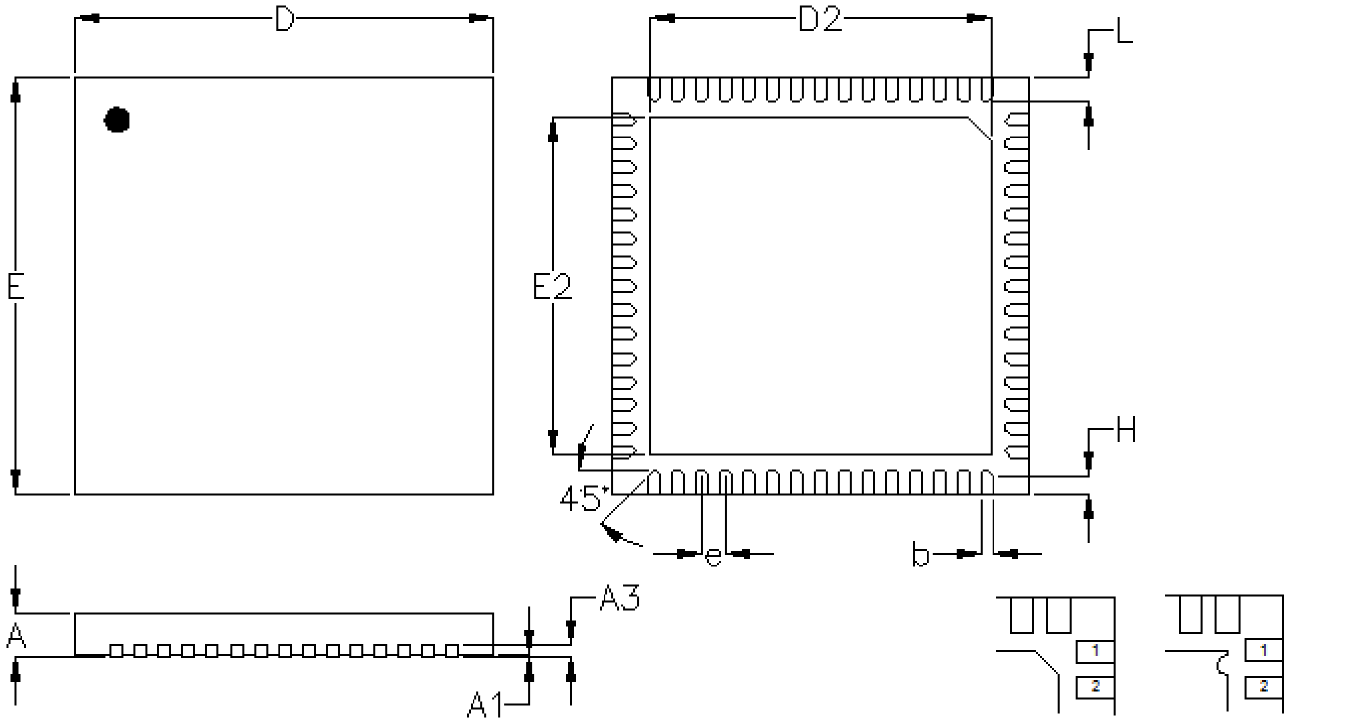
SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
010000000	080	0.885	010100000	0A0	1.045	011000000	0C0	1.205	011100000	0E0	1.365
010000001	081	0.890	010100001	0A1	1.050	011000001	0C1	1.210	011100001	0E1	1.370
010000010	082	0.895	010100010	0A2	1.055	011000010	0C2	1.215	011100010	0E2	1.375
010000011	083	0.900	010100011	0A3	1.060	011000011	0C3	1.220	011100011	0E3	1.380
010000100	084	0.905	010100100	0A4	1.065	011000100	0C4	1.225	011100100	0E4	1.385
010000101	085	0.910	010100101	0A5	1.070	011000101	0C5	1.230	011100101	0E5	1.390
010000110	086	0.915	010100110	0A6	1.075	011000110	0C6	1.235	011100110	0E6	1.395
010000111	087	0.920	010100111	0A7	1.080	011000111	0C7	1.240	011100111	0E7	1.400
010001000	088	0.925	010101000	0A8	1.085	011001000	0C8	1.245	011101000	0E8	1.405
010001001	089	0.930	010101001	0A9	1.090	011001001	0C9	1.250	011101001	0E9	1.410
010001010	08A	0.935	010101010	0AA	1.095	011001010	0CA	1.255	011101010	0EA	1.415
010001011	08B	0.940	010101011	0AB	1.100	011001011	0CB	1.260	011101011	0EB	1.420
010001100	08C	0.945	010101100	0AC	1.105	011001100	0CC	1.265	011101100	0EC	1.425
010001101	08D	0.950	010101101	0AD	1.110	011001101	0CD	1.270	011101101	0ED	1.430
010001110	08E	0.955	010101110	0AE	1.115	011001110	0CE	1.275	011101110	0EE	1.435
010001111	08F	0.960	010101111	0AF	1.120	011001111	0CF	1.280	011101111	0EF	1.440
010010000	090	0.965	010110000	0B0	1.125	011010000	0D0	1.285	011110000	0F0	1.445
010010001	091	0.970	010110001	0B1	1.130	011010001	0D1	1.290	011110001	0F1	1.450
010010010	092	0.975	010110010	0B2	1.135	011010010	0D2	1.295	011110010	0F2	1.455
010010011	093	0.980	010110011	0B3	1.140	011010011	0D3	1.300	011110011	0F3	1.460
010010100	094	0.985	010110100	0B4	1.145	011010100	0D4	1.305	011110100	0F4	1.465
010010101	095	0.990	010110101	0B5	1.150	011010101	0D5	1.310	011110101	0F5	1.470
010010110	096	0.995	010110110	0B6	1.155	011010110	0D6	1.315	011110110	0F6	1.475
010010111	097	1.000	010110111	0B7	1.160	011010111	0D7	1.320	011110111	0F7	1.480
010011000	098	1.005	010111000	0B8	1.165	011011000	0D8	1.325	011111000	0F8	1.485
010011001	099	1.010	010111001	0B9	1.170	011011001	0D9	1.330	011111001	0F9	1.490
010011010	09A	1.015	010111010	0BA	1.175	011011010	0DA	1.335	011111010	0FA	1.495
010011011	09B	1.020	010111011	0BB	1.180	011011011	0DB	1.340	011111011	0FB	1.500
010011100	09C	1.025	010111100	0BC	1.185	011011100	0DC	1.345	011111100	0FC	1.505
010011101	09D	1.030	010111101	0BD	1.190	011011101	0DD	1.350	011111101	0FD	1.510
010011110	09E	1.035	010111110	0BE	1.195	011011110	0DE	1.355	011111110	0FE	1.515
010011111	09F	1.040	010111111	0BF	1.200	011011111	0DF	1.360	011111111	0FF	1.520
											Continued

Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
100000000	100	1.525	100100000	120	1.685	101000000	140	1.845	101100000	160	2.005
100000001	101	1.530	100100001	121	1.690	101000001	141	1.850	101100001	161	2.010
100000010	102	1.535	100100010	122	1.695	101000010	142	1.855	101100010	162	2.015
100000011	103	1.540	100100011	123	1.700	101000011	143	1.860	101100011	163	2.020
100000100	104	1.545	100100100	124	1.705	101000100	144	1.865	101100100	164	2.025
100000101	105	1.550	100100101	125	1.710	101000101	145	1.870	101100101	165	2.030
100000110	106	1.555	100100110	126	1.715	101000110	146	1.875	101100110	166	2.035
100000111	107	1.560	100100111	127	1.720	101000111	147	1.880	101100111	167	2.040
100001000	108	1.565	100101000	128	1.725	101001000	148	1.885	101101000	168	2.045
100001001	109	1.570	100101001	129	1.730	101001001	149	1.890	101101001	169	2.050
100001010	10A	1.575	100101010	12A	1.735	101001010	14A	1.895	101101010	16A	2.055
100001011	10B	1.580	100101011	12B	1.740	101001011	14B	1.900	101101011	16B	2.060
100001100	10C	1.585	100101100	12C	1.745	101001100	14C	1.905	101101100	16C	2.065
100001101	10D	1.590	100101101	12D	1.750	101001101	14D	1.910	101101101	16D	2.070
100001110	10E	1.595	100101110	12E	1.755	101001110	14E	1.915	101101110	16E	2.075
100001111	10F	1.600	100101111	12F	1.760	101001111	14F	1.920	101101111	16F	2.080
100010000	110	1.605	100110000	130	1.765	101010000	150	1.925	101110000	170	2.085
100010001	111	1.610	100110001	131	1.770	101010001	151	1.930	101110001	171	2.090
100010010	112	1.615	100110010	132	1.775	101010010	152	1.935	101110010	172	2.095
100010011	113	1.620	100110011	133	1.780	101010011	153	1.940	101110011	173	2.100
100010100	114	1.625	100110100	134	1.785	101010100	154	1.945	101110100	174	2.105
100010101	115	1.630	100110101	135	1.790	101010101	155	1.950	101110101	175	2.110
100010110	116	1.635	100110110	136	1.795	101010110	156	1.955	101110110	176	2.115
100010111	117	1.640	100110111	137	1.800	101010111	157	1.960	101110111	177	2.120
100011000	118	1.645	100111000	138	1.805	101011000	158	1.965	101111000	178	2.125
100011001	119	1.650	100111001	139	1.810	101011001	159	1.970	101111001	179	2.130
100011010	11A	1.655	100111010	13A	1.815	101011010	15A	1.975	101111010	17A	2.135
100011011	11B	1.660	100111011	13B	1.820	101011011	15B	1.980	101111011	17B	2.140
100011100	11C	1.665	100111100	13C	1.825	101011100	15C	1.985	101111100	17C	2.145
100011101	11D	1.670	100111101	13D	1.830	101011101	15D	1.990	101111101	17D	2.150
100011110	11E	1.675	100111110	13E	1.835	101011110	15E	1.995	101111110	17E	2.155
100011111	11F	1.680	100111111	13F	1.840	101011111	15F	2.000	101111111	17F	2.160

Continued

Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
110000000	180	2.165	110100000	1A0	2.325	111000000	1C0	2.485	111100000	1E0	2.645
110000001	181	2.170	110100001	1A1	2.330	111000001	1C1	2.490	111100001	1E1	2.650
110000010	182	2.175	110100010	1A2	2.335	111000010	1C2	2.495	111100010	1E2	2.655
110000011	183	2.180	110100011	1A3	2.340	111000011	1C3	2.500	111100011	1E3	2.660
110000100	184	2.185	110100100	1A4	2.345	111000100	1C4	2.505	111100100	1E4	2.665
110000101	185	2.190	110100101	1A5	2.350	111000101	1C5	2.510	111100101	1E5	2.670
110000110	186	2.195	110100110	1A6	2.355	111000110	1C6	2.515	111100110	1E6	2.675
110000111	187	2.200	110100111	1A7	2.360	111000111	1C7	2.520	111100111	1E7	2.680
110001000	188	2.205	110101000	1A8	2.365	111001000	1C8	2.525	111101000	1E8	2.685
110001001	189	2.210	110101001	1A9	2.370	111001001	1C9	2.530	111101001	1E9	2.690
110001010	18A	2.215	110101010	1AA	2.375	111001010	1CA	2.535	111101010	1EA	2.695
110001011	18B	2.220	110101011	1AB	2.380	111001011	1CB	2.540	111101011	1EB	2.700
110001100	18C	2.225	110101100	1AC	2.385	111001100	1CC	2.545	111101100	1EC	2.705
110001101	18D	2.230	110101101	1AD	2.390	111001101	1CD	2.550	111101101	1ED	2.710
110001110	18E	2.235	110101110	1AE	2.395	111001110	1CE	2.555	111101110	1EE	2.715
110001111	18F	2.240	110101111	1AF	2.400	111001111	1CF	2.560	111101111	1EF	2.720
110010000	190	2.245	110110000	1B0	2.405	111010000	1D0	2.565	111110000	1F0	2.725
110010001	191	2.250	110110001	1B1	2.410	111010001	1D1	2.570	111110001	1F1	2.730
110010010	192	2.255	110110010	1B2	2.415	111010010	1D2	2.575	111110010	1F2	2.735
110010011	193	2.260	110110011	1B3	2.420	111010011	1D3	2.580	111110011	1F3	2.740
110010100	194	2.265	110110100	1B4	2.425	111010100	1D4	2.585	111110100	1F4	2.745
110010101	195	2.270	110110101	1B5	2.430	111010101	1D5	2.590	111110101	1F5	2.750
110010110	196	2.275	110110110	1B6	2.435	111010110	1D6	2.595	111110110	1F6	2.755
110010111	197	2.280	110110111	1B7	2.440	111010111	1D7	2.600	111110111	1F7	2.760
110011000	198	2.285	110111000	1B8	2.445	111011000	1D8	2.605	111111000	1F8	2.765
110011001	199	2.290	110111001	1B9	2.450	111011001	1D9	2.610	111111001	1F9	2.770
110011010	19A	2.295	110111010	1BA	2.455	111011010	1DA	2.615	111111010	1FA	2.775
110011011	19B	2.300	110111011	1BB	2.460	111011011	1DB	2.620	111111011	1FB	2.780
110011100	19C	2.305	110111100	1BC	2.465	111011100	1DC	2.625	111111100	1FC	2.785
110011101	19D	2.310	110111101	1BD	2.470	111011101	1DD	2.630	111111101	1FD	2.790
110011110	19E	2.315	110111110	1BE	2.475	111011110	1DE	2.635	111111110	1FE	2.795
110011111	19F	2.320	110111111	1BF	2.480	111011111	1DF	2.640	111111111	1FF	2.800

20 Outline Dimension



DETAIL A

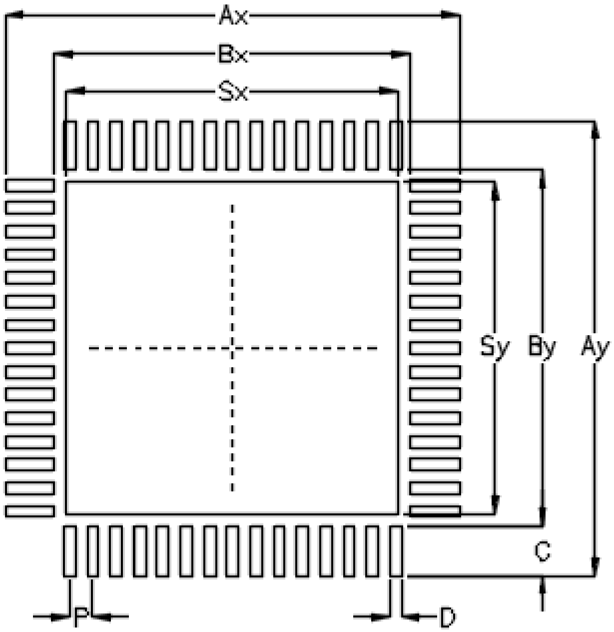
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

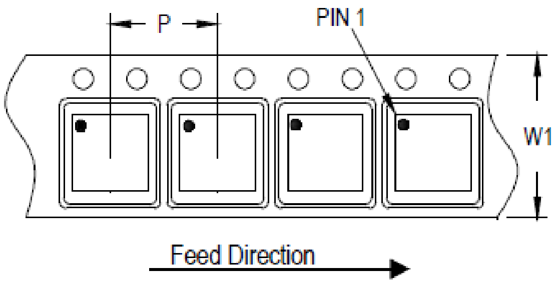
21 Footprint Information

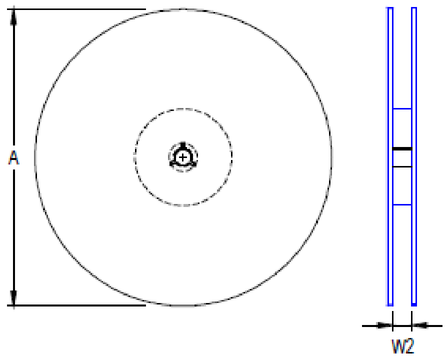


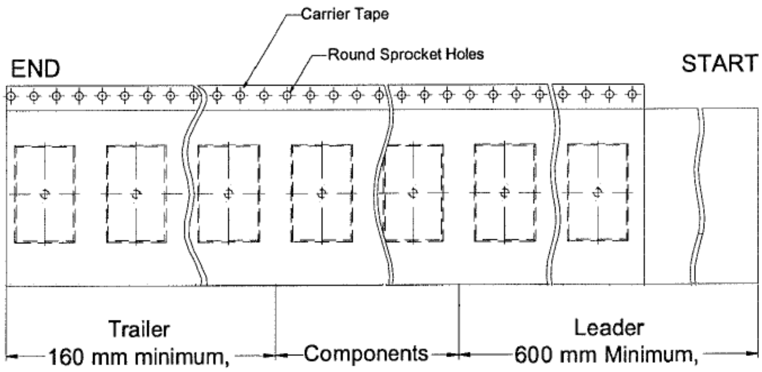
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-60	60	0.40	7.80	7.80	6.10	6.10	0.85	0.20	5.70	5.70	±0.05

22 Packing Information

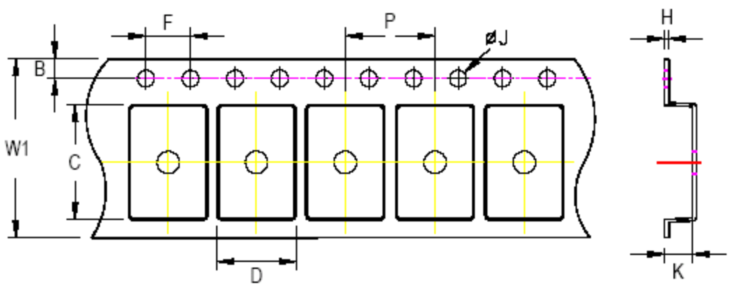
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 7x7	16	12	330	13	2,500	160	600	16.4/18.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 7x7	13”	2,500	Box G	1	2,500	Carton A	6	15,000

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description
00	2025/8/18	First Edition