Dual Channel PWM Controller with I²C Interface Control for AMD SVI3 CPU/GPU Core Power Supply

General Description

The RT3678BE is a synchronous buck controller which supports dual output rails and can fully meet AMD SVI3 requirements. The RT3678BE adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all AMD CPU/GPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3678BE features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3678BE integrates a high accuracy ADC for reporting and a non-volatile memory (NVM) to store custom configurations, such as output current scale, auto phase add/drop threshold, switching frequency, overcurrent threshold or AQR trigger level. It also features full fault protection functions, including overvoltage (OV), undervoltage (UV), overcurrent (OC) and undervoltage lockout (UVLO), over-temperature protection (OTP), VR-hot warning, CRC failure and communication failure. The RT3678BE provides independent enable, power good and temperature sensing for each output rail. It also supports several functions which can be set by the I²C interface.

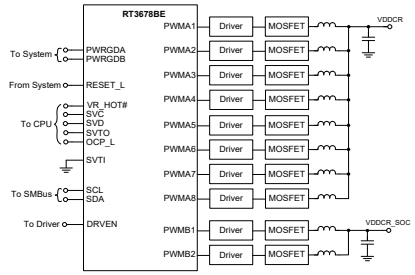
Applications

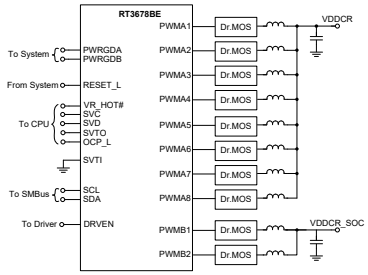
- AMD SVI3 VDDCR/VDDCR_SOC Rails
- Desktop and Notebook Computer
- AVP Step-Down Converter

Features

- **AMD SVI3 Rev 1.01 Compatible**
- **8 Phase (Rail A) + 2 Phase (Rail B) PWM Controller**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode (DEM) at Light Load**
- **Fast Transient Response: Adaptive Quick Response (AQR)**
- **OVP, OCP and UVP with Flag**
- **Switching Frequency Setting**
- **Auto Phase Add/Drop with DEM for Excellent Efficiency**
- **Voltage On-the-Fly (VOTF) Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-line**
- **Standard I²C Protocol Interface**
  - **Internal Non-Volatile Memory (NVM) to Store Custom Configurations**
  - **Current Balance Gain Adjustment for Thermal Balance**
  - **Dynamic Load-line Setting**
  - **Voltage Offset Setting**
  - **Fixed VID Setting**
  - **Protection Report and Protection Disable**
  - **Output Voltage / Output Current / Temperature / Input Power Monitoring**
- **Soldering Good Detection**
- **Small 68-Lead WQFN Package**

Simplified Application Circuit





Ordering Information

RT3678BE□□-□

- The configuration code identifier for the register setting stored in the internal NVM
- Package Type
  QW: WQFN-68L 8x8 (W-Type)
- Lead Plating System
  G: Green (Halogen Free and Pb Free)

Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

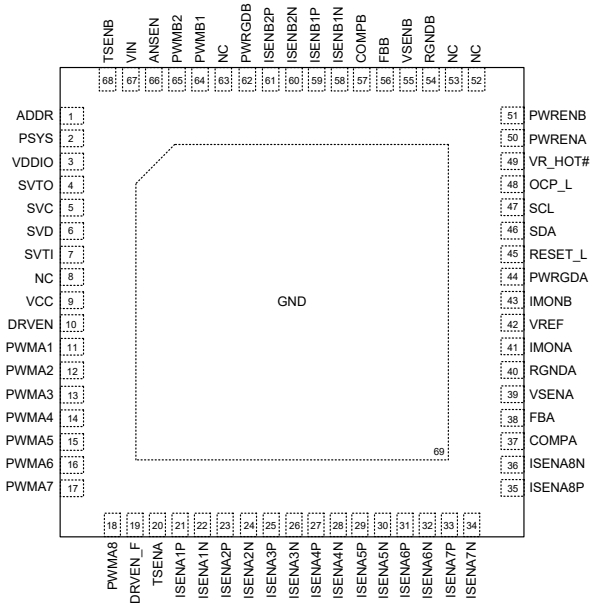
Marking Information

RT3678BEGQW: Product Code

YMDNN: Date Code

Pin Configuration

(TOP VIEW)



WQFN-68L 8x8

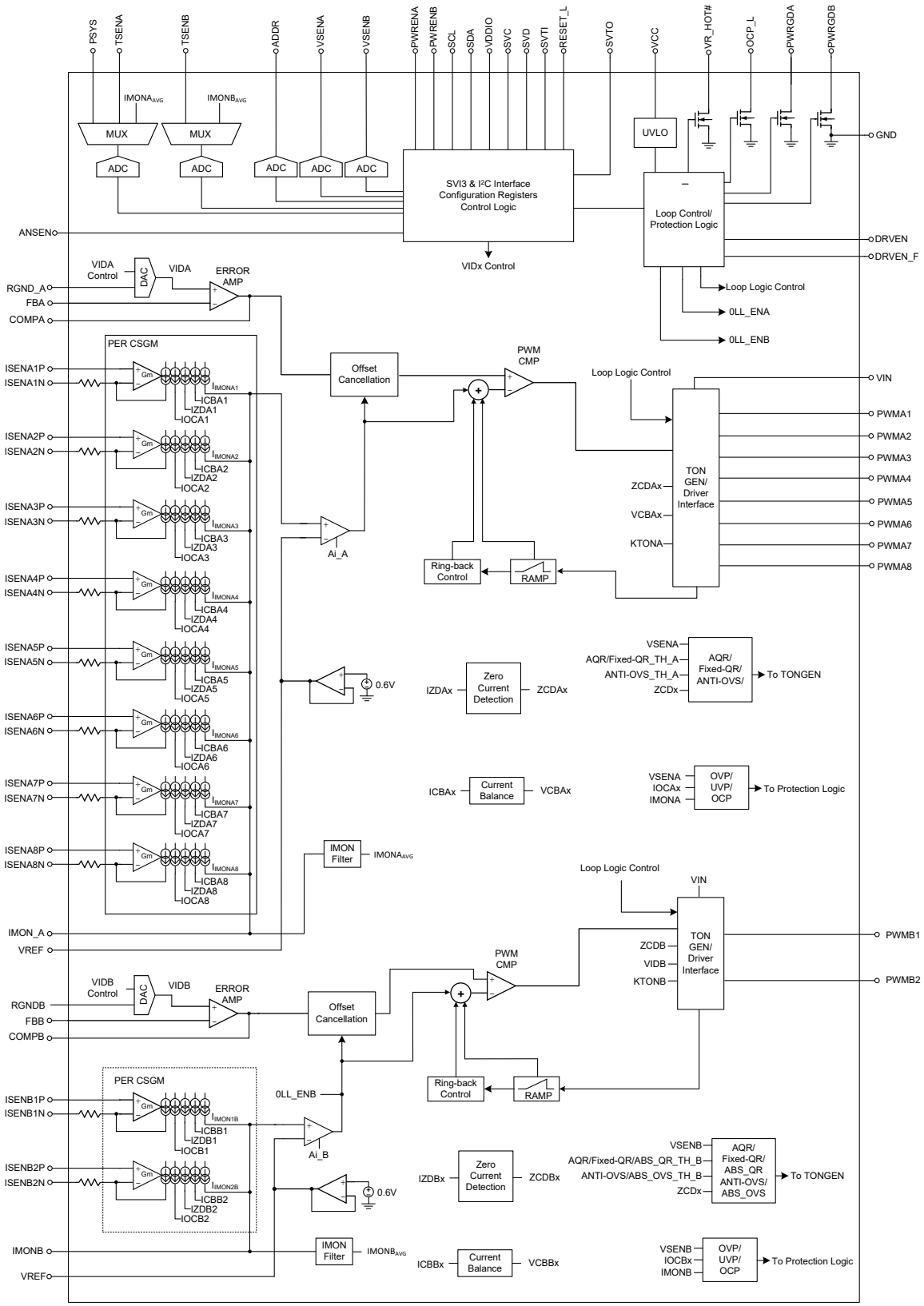
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ADDR	A resistor tied to ground sets I^2C address. For soldering check, connect the ADDR pin to 5V and pull the PWREN high. If the soldering is good, output voltage is 0.9V for rail A, 1V for rail B.
2	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible.
3	VDDIO	Supply voltage input of SVI3 interface. This pin serves as the reference for SVC, SVD, SVTI and SVTO.
4	SVTO	Serial VID Telemetry output. This pin is a push-pull output.
5	SVC	Serial VID Clock input. This pin is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.
6	SVD	Serial VID Data input. This pin is a push-pull signal which transmits commands from the controller to the targets.
7	SVTI	Serial VID Telemetry input. This pin is driven by the next-furthest target on the telemetry daisy-chain.
8, 52, 53, 63	NC	No internal connection.
9	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 1Ω and C = 2.2μF. The decoupling capacitor should be placed as close to PWM controller as possible. The recommended size of R_{VCC} is 0603.
10	DRVEN	External driver mode control. As PSI6 command is received, this pin is in low state. The output high level is VCC.

Pin No.	Pin Name	Pin Function
11	PWMA1	Phase #1 rail A PWM output. This signal is used to drive the PWM input of the FET diver IC. Unused PWM pins should be left unconnected. The PWM tri-state windows can be selected by NVM. One is 1.6V to 2.2V and the other is 1.4V to 2.1V.
12	PWMA2	Phase #2 rail A PWM output. Refer to PWMA1 description.
13	PWMA3	Phase #3 rail A PWM output. Refer to PWMA1 description.
14	PWMA4	Phase #4 rail A PWM output. Refer to PWMA1 description.
15	PWMA5	Phase #5 rail A PWM output. Refer to PWMA1 description.
16	PWMA6	Phase #6 rail A PWM output. Refer to PWMA1 description.
17	PWMA7	Phase #7 rail A PWM output. Refer to PWMA1 description.
18	PWMA8	Phase #8 rail A PWM output. Refer to PWMA1 description.
19	DRVEN_F	External driver mode control. As PSI6 command is received, this pin is in floating state. The output high level is VCC.
20	TSENA	External temperature sense input pin for rail A. Connect to NTC or integrated power stage temperature sensor.
21	ISENA1P	Phase #1 current sense inputs of rail A. The ISENA1P and ISENA1N pins are used to differentially sense the corresponding channel current. Connecting ISENA1P to VCC if rail A is not used.
22	ISENA1N	
23	ISENA2P	Phase #2 current sense inputs of rail A. The ISENA2P and ISENA2N pins are used to differentially sense the corresponding channel current. Connecting ISENA2P to VCC programs 1-phase operation.
24	ISENA2N	
25	ISNEA3P	Phase #3 current sense inputs of rail A. The ISENA3P and ISENA3N pins are used to differentially sense the corresponding channel current. Connecting ISENA3P to VCC programs 2-phase operation.
26	ISENA3N	
27	ISENA4P	Phase #4 current sense inputs of rail A. The ISENA4P and ISENA4N pins are used to differentially sense the corresponding channel current. Connecting ISENA4P to VCC programs 3-phase operation.
28	ISENA4N	
29	ISENA5P	Phase #5 current sense inputs of rail A. The ISENA5P and ISENA5N pins are used to differentially sense the corresponding channel current. Connecting ISENA5P to VCC programs 4-phase operation.
30	ISENA5N	
31	ISENA6P	Phase #6 current sense inputs of rail A. The ISENA6P and ISENA6N pins are used to differentially sense the corresponding channel current. Connecting ISENA6P to VCC programs 5-phase operation.
32	ISENA6N	
33	ISENA7P	Phase #7 current sense inputs of rail A. The ISENA7P and ISENA7N pins are used to differentially sense the corresponding channel current. Connecting ISENA7P to VCC programs 6-phase operation.
34	ISENA7N	
35	ISENA8P	Phase #8 current sense inputs of rail A. The ISENA8P and ISENA8N pins are used to differentially sense the corresponding channel current. Connecting ISENA8P to VCC programs 7-phase operation.
36	ISENA8N	
37	COMPA	Error amplifier output of rail A.
38	FBA	Error amplifier voltage feedback of rail A.
39	VSENA	Positive differential voltage sense input for rail A. Connect to positive remote sensing point and should be routed with RGNDA as a differential pair.
40	RGNDA	Negative differential voltage sense input for rail A. Connect to negative remote sensing point.
41	IMONA	Rail A VR current monitor output. This pin outputs a current proportional to the output current.

Pin No.	Pin Name	Pin Function
42	VREF	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. While controller shuts down or sets all rails in PSI6, voltage source shuts down. An external 0.47-μF decoupling capacitor and a 3.9-Ω resistor must be placed between this pin and GND.
43	IMONB	Rail B VR current monitor output. This pin outputs a current proportional to the output current.
44	PWRGDA	Power Good indicator for rail A. This open-drain output requires an external pull-up resistor. PWRGDA is pulled low when a shutdown fault occurs.
45	RESET_L	Input pin of SVI3 interface. Active low signal will reset all SVI3 state machines and SVI3 define registers to reset to default values.
46	SDA	I^2C data signal.
47	SCL	I^2C clock signal.
48	OCP_L	Output pin of SVI3 interface. This open-drain output requires an external pull-up resistor. Asserted when output current is greater than OCP threshold or OCP warning threshold. The two rails of the controller share one OCP_L pin.
49	VR_HOT#	Thermal warning flag. This open-drain output will be pulled low in an event of over-temperature warning without disabling the regulator.
50	PWRENA	Active high output enable input pin for rail A. Faults are cleared when PWRENA is toggled but no effect on the sticky FAULT_STATUS bits.
51	PWRENB	Active high output enable input pin for rail B. Faults are cleared when PWRENB is toggled but no effect on the sticky FAULT_STATUS bits.
54	RGNDB	Negative differential voltage sense input for rail B. Connect to negative remote sensing point.
55	VSENB	Positive differential voltage sense input for rail B. Connect to positive remote sensing point and should be routed with RGNDB as a differential pair.
56	FBB	Error amplifier voltage feedback of rail B.
57	COMPB	Error amplifier output of rail B.
58	ISENB1N	Phase #1 current sense inputs of rail B. The ISENB1P and ISENB1N pins are used to differentially sense the corresponding channel current. Connect ISENB1P to VCC if rail B is not used.
59	ISENB1P	
60	ISENB2N	Phase #2 current sense inputs of rail B. The ISENB2P and ISENB1N pins are used to differentially sense the corresponding channel current. Connect ISENB2P to VCC if rail B is not used.
61	ISENB2P	
62	PWRGDB	Power Good indicator for rail B. This open-drain output requires an external pull-up resistor. PWRGDB is pulled low when a shutdown fault occurs.
64	PWMB1	Phase #1 rail B PWM output. This signal is used to drive the PWM input of the FET diver IC. Unused PWM pins should be left unconnected. The PWM tri-state windows can be selected by NVM. One is 1.6V to 2.2V and the other is 1.4V to 2.1V.
65	PWMB2	Phase #2 rail B PWM output. Refer to PWMB1 description.
66	ANSEN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
67	VIN	VIN input pin. Connect a low pass filter to this pin to set on-time.
68	TSENB	External temperature sense input pin for rail B. Connect to NTC or integrated power stage temperature sensor.
69 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough via numbers for maximum power dissipation.

Functional Block Diagram



Operation

G-NAVP™ Control Mode

The RT3678BE adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3678BE generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior. The COMP signal is the inverted and amplified signal of the output voltage. The COMP rises due to output voltage droop and the rising COMP forces PWM to turn on earlier and more closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and the corresponding output voltage is in the steady state of lower voltage. The load-line, output voltage drooping proportional to loading current, is achieved.

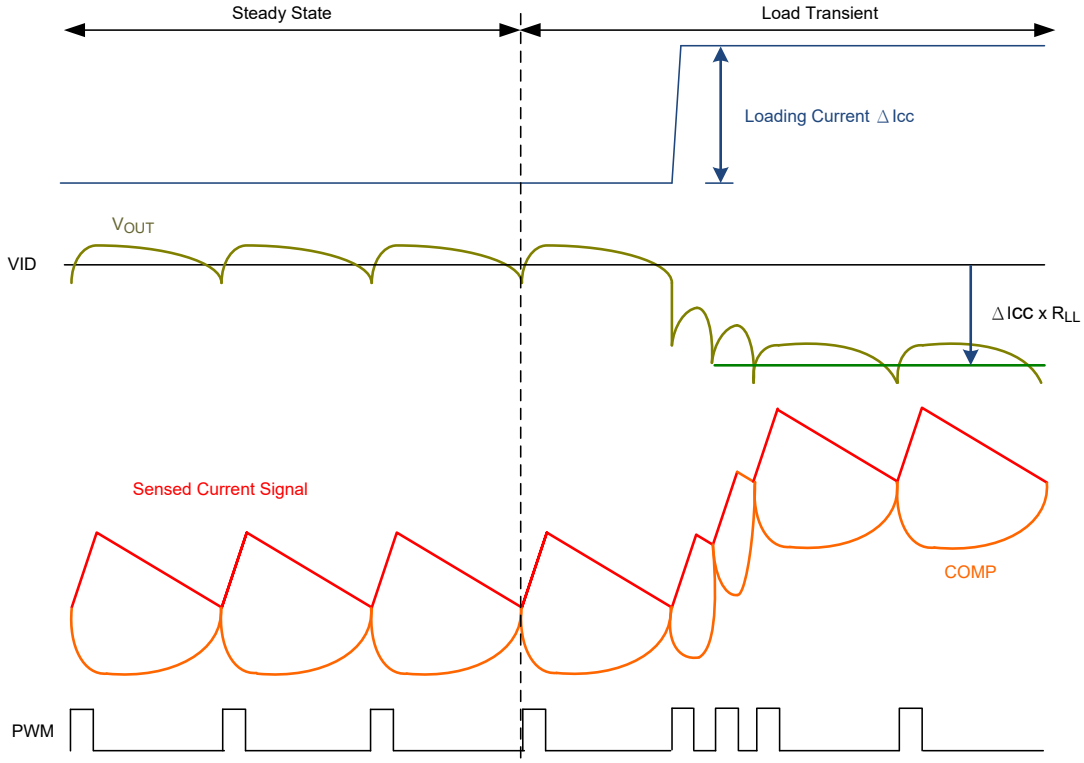


Figure 1. G-NAVP™ Behavior Waveform

SVI3, I²C Interface, Control Logic and Configuration Registers

SVI3 Interface receives or transmits SVI3 signal with CPU/GPU. The VR receives or transmits I²C signals using the I²C interface. Control Logic executes command (Read/Write/Reset registers, VID/Address packets, Change Power State and Telemetry Request) and sends related signals to control VR. Configuration Registers include function setting registers and SVI3 required registers.

IMON Filter

IMON Filter is used to average current signal by an analog low-pass filter. It outputs IMONA and IMONB to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs for TSENA, TSEN_B, PSYS, IMON_A and IMON_B. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The UVLO detects the VCC voltage. As VCC exceeds the threshold, the controller issues POR = high and waits PWREN. After both POR PWREN are ready, the controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to VID packets command, Control Logic dynamically changes VID voltage to the target voltage with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and overcurrent protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by NVM. It helps wide application range of DCR and load-line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal with sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accurately.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (anti-overshoot function).

AQR, Fixed-QR, ABS_QR, ANTI-OVS, and ABS_OVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWMs to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by NVM. ANTI-OVS can help overshoot reduction which detects loading falling edge and forces all PWMs in tri-state until the zero current is detected.

TONGEN and Driver Interface

The PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWM to turn on at the same time. Driver interface provides high/low/tri-state to

drive external driver. In power saving mode, driver interface forces PWM in tri-state to turn off high-side and low-side power MOSFET according to zero current detection output. In addition, the PWM state is controlled by protection logic. Different protections force required PWM state.

VCC_UVLO, OVP, UVP, SSOCP, OCP, OTP, OCP Warning, VR-HOT Warning, CRC Failure, and Communication Failure

The RT3678BE includes the following protections: VCC undervoltage lockout, overvoltage protection, undervoltage protection, soft-start overcurrent protection, overcurrent protection, over-temperature protection, overcurrent warning, VR-Hot warning, CRC. failure, and Communication Failure.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- VIN to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4)

- WQFN-68L 8x8, θ_{JA} ---------- 26.3°C/W
- WQFN-68L 8x8, $\theta_{JC(Top)}$ ---------- 9.5°C/W

Electrical Characteristics

(V_{CC} = 5V, V_{VDDIO} = 1.8V, typical values are referenced to T_J = 25°C, Min. and Max. values are referenced to T_J from –10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	--	5.5	V
Supply Current	I_{VCC}	VCC = 5V, PWREN = H, no switching	--	--	40	mA
Supply Current at PSI6	I_{VCC_PSI6}	VCC = 5V, PWREN = H, in PSI6	--	--	180	μA
Shutdown Current	I_{SHDN}	VCC = 5V, PWREN = L	--	--	180	μA
VCC Power-ON Reset (POR)	$V_{CC\_POR\_R}$	Rising edge	4.2	4.32	4.45	V
	$\Delta V_{CC\_POR\_HYS}$	Hysteresis	--	170	--	mV
VCC Power-ON Reset for NVM (POR_NVM)	$V_{CC\_POR\_NVM\_R}$	Rising edge	--	3.6	3.75	V
	$V_{CC\_POR\_NVM\_F}$	Falling edge	3.32	3.47	--	
Reference and DAC						
DAC Accuracy	V_{FB}	0.250 to 0.995 T_A = 0 to 85°C	–5	--	5	mV
		1.000 to 2.800 T_A = 0 to 85°C	–0.5	--	0.5	%

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Slew Rate							
VOTF Slew Rate	Up	UP_SR	Measure VFB from 20% target VID to 80% target VID with ΔVOTF ≥ 100mV	−10%	--	10%	mV/μs
	Down	DN_SR	Default equals to UP_SR	−10%	--	10%	
Current Sensing Amplifier							
CS Input Voltage Range		V_{CSIN}	Differential voltage range of DCR sense.	−10	--	80	mV
Current Sense Gain Error		AMIRROR	Internal current mirror gain of per phase current sense $I_{IMON}/I_{CS,PERx}$	1.2125	1.25	1.2875	A/A
t_{ON} Setting							
On-Time Setting	Rail A	t_{ON}	VIN = 12V, VID = 1V, KTON = 0.8V	--	208	--	ns
	Rail B		VIN = 12V, VID = 1V, KTON = 0.8V	--	208	--	ns
Minimum On-Time	Rail A	t_{ON_MIN}		--	70	--	ns
	Rail B			--	70	--	ns
Protections							
Overvoltage Protection Threshold		V_{OV}	Default threshold	315	350	385	mV
De-bounce Time of OVP		t_{D_OVP}		--	0.8	--	μs
Undervoltage Protection Threshold		V_{UV}	Default threshold	315	350	385	mV
De-bounce Time of UVP		t_{D_UVP}		--	3.3	--	μs
Overcurrent Protection Threshold		V_{OCP}		−3	--	3	%
Overcurrent Warning Threshold		V_{OC_WARN}		−3	--	3	%
Over-Temperature Protection Threshold		T_{OTP}		--	125	--	°C
VRHOT Warning Threshold		T_{VRHOT}		--	100	--	°C
PWREN and PWRGD							
PWREN	Logic-High	V_{IH_PWREN}		1.17	--	--	V
	Logic-Low	V_{IL_PWREN}		--	--	0.63	
Leakage Current of PWREN		I_{LEAK_PWREN}		−1	--	1	μA
PWRGD Pull Low Voltage		V_{PWRGD}	I_{PWRGD} = 8mA	--	--	0.2	V
VR_HOT#							
VR_HOT# Pull Low Voltage		$V_{VR\_HOT\#}$	$I_{VR\_HOT\#}$ = 8mA	--	--	0.2	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VREF							
VREF Voltage		V_{VREF}	Normal operation	0.59	0.6	0.61	V
Acoustic Noise Suppression (ANS)							
ANS_EN	Logic-High	$V_{IH\_ANS\_EN}$		V_{CC} – 0.7	--	--	V
	Logic-Low	$V_{IL\_ANS\_EN}$		--	--	1	V
SVI3 Interface							
VDDIO Level		VDDIO		1.08	--	1.98	V
SVC, SVD, SVTI	Logic-High	V_{IH}		0.65 x VDDIO	--	--	V
	Logic-Low	V_{IL}		--	--	0.35 x VDDIO	V
SVC, SVD, SVTO Output High Voltage		V_{OH}	I = –8mA	VDDIO – 0.45	--	--	V
			I = –4mA	VDDIO – 0.22	--	--	V
SVC, SVD, SVTO Output Low Voltage		V_{OL}	I = 8mA			0.45	V
			I = 4mA			0.22	V
RESET_L	Logic-High	$V_{IH\_RESET\_L}$		1.17	--	--	V
	Logic-Low	$V_{IL\_RESET\_L}$		--	--	0.63	V
Leakage Current of SVC, SVD, SVTI, and SVTO		I_{LEAK_SVI3}		–10	--	10	μA
I^2C interface							
SCL, SDA	Logic-High	V_{IH_I2C}		1	--	--	V
	Logic-Low	V_{IL_I2C}		--	--	0.6	V
Standard/Fast Mode							
SCL Clock Rate		f_{SCL}	Standard mode	--	--	100	kHz
			Fast mode	--	--	400	
Hold Time (Repeated) Start Condition. After this period, the first clock pulse is generated.		t_{HD_STA}		0.6	--	--	μs
Low Period of SCL Clock		t_{LOW}		1.3	--	--	μs
High Period of SCL Clock		t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition		t_{SU_STA}		0.6	--	--	μs
Data Hold Time		t_{HD_DAT}	Standard mode	0	--	--	μs
			Fast mode	0	--	0.9	
Data Set-Up Time		t_{SU_DAT}	Standard mode	250	--	--	ns
			Fast mode	100	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-Up Time for STOP Condition	t_{SU_STO}		0.6	--	--	μs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of Both SDA and CL Signals	t_R	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
Falling Time of Both SDA and SCL signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
ADC						
ADC Resolution			--	10	--	bits
ADC Reference Voltage			--	3.2	--	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
PWM Output						
PWMx Output High Level		I_{OUT} = 4mA	VCC – 0.16	--	--	V
PWMx Output Low Level		I_{OUT} = 4mA	--	--	0.08	
ITSEN						
TSEN Source Current	I_{TSEN}	V_{TSEN} = 1.6V	79.2	80	80.8	μA
PSYS and DIMON						
Digital PSYS Reporting	D_{PSYS}	V_{PSYS} = 1.6V	--	1023	--	Decimal
Digital IMON of Rail A	D_{VIMONA}	V_{IMONA} - V_{VREF} = 0.4V	--	1023	--	Decimal
Digital IMON of Rail B	D_{VIMONB}	V_{IMONB} - V_{VREF} = 0.4V	--	1023	--	Decimal
Telemetry						
Accuracy of Output Voltage Telemetry (10-bit Telemetry, 1LSB = 5mV)	$VOUT_{TEL}$	0.250 to 0.995 T_A = 0 to 85°C	–7.5	--	7.5	mV
		1.000 to 2.800 T_A = 0 to 85°C	–0.75	--	0.75	%
Temperature Reporting Accuracy (10-bit Telemetry, 1LSB = 1°C)	$TEMP_{TEL}$	Between 50°C to 125°C	–5	--	5	°C
Temperature Reporting Range			–40	--	150	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

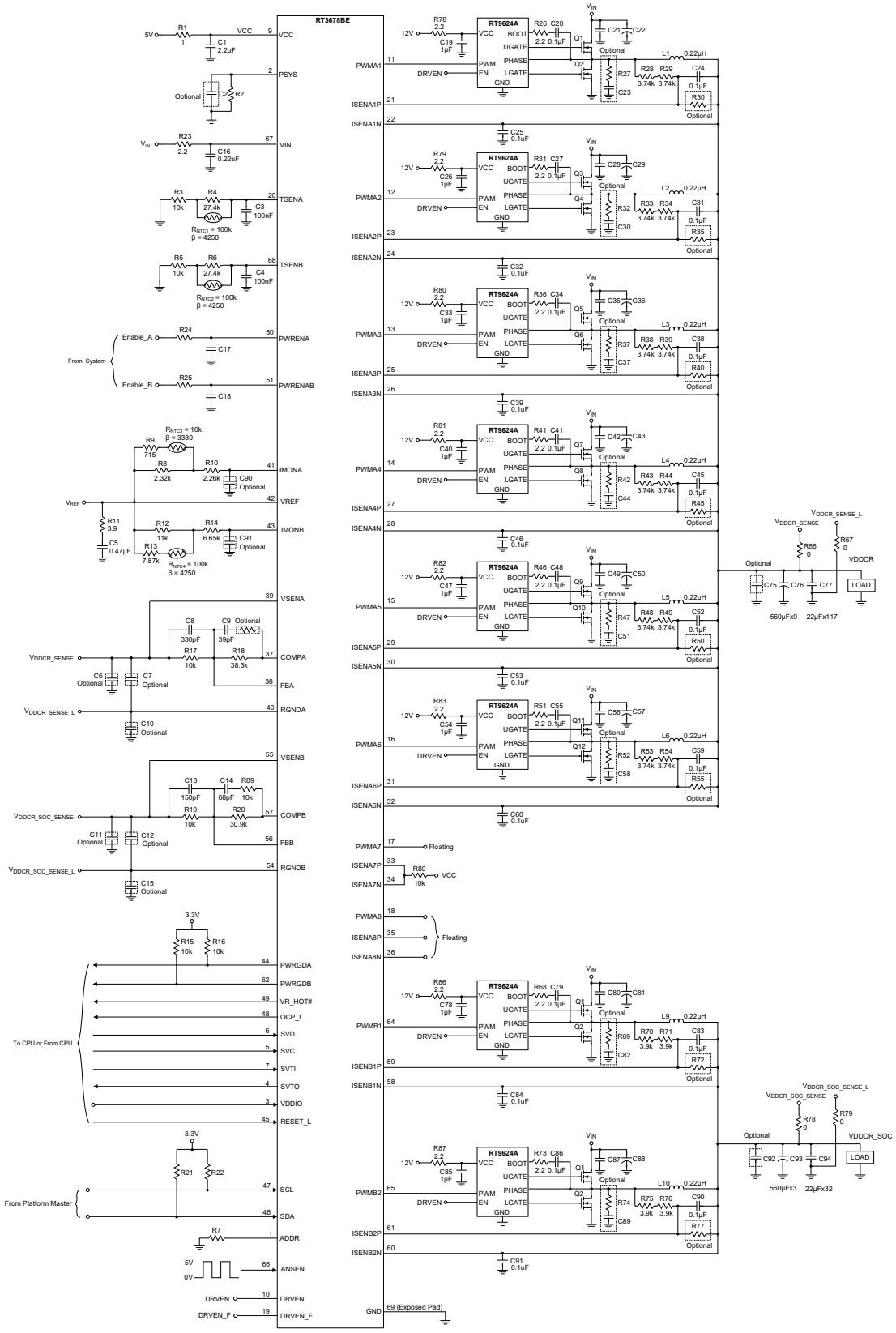
Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

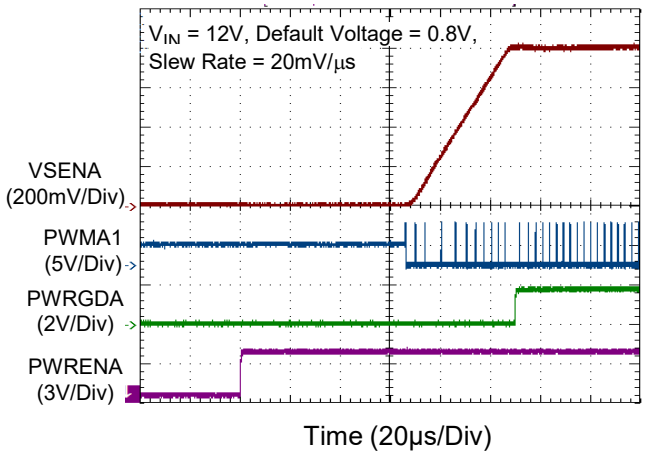
Typical Application Circuit

Platform: AM5 Group A-170W

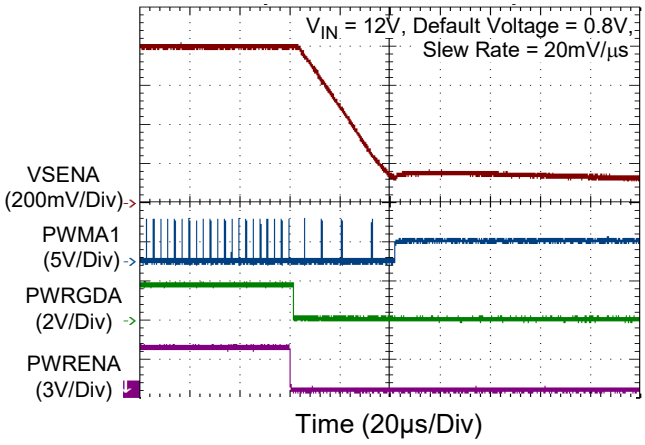


Typical Operating Characteristics

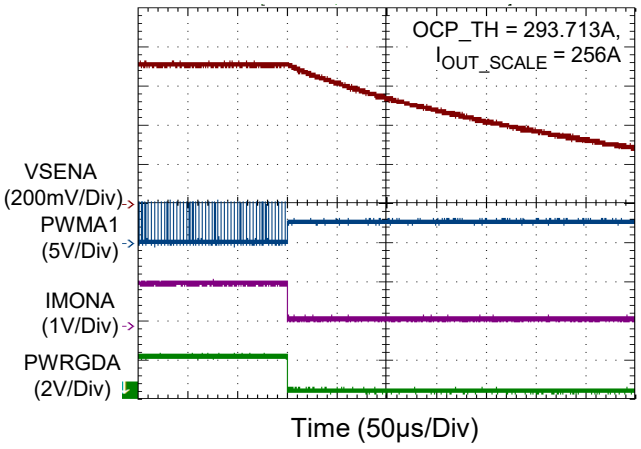
Rail A Power On from PWRENA



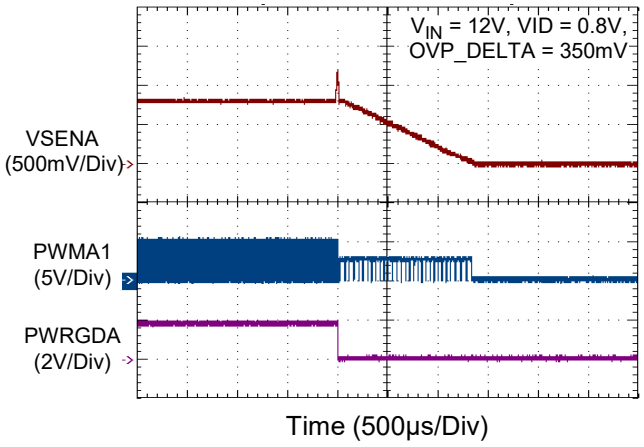
Rail A Power Off from PWRENA



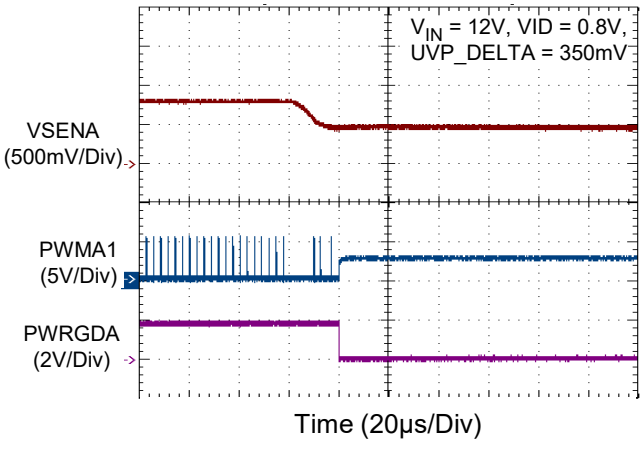
Rail A OCP



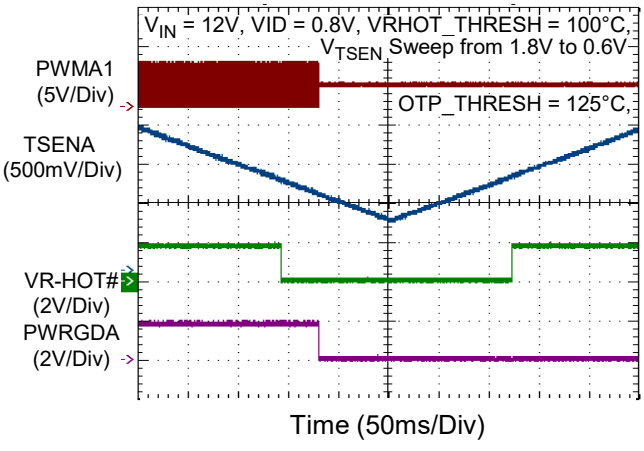
Rail A OVP



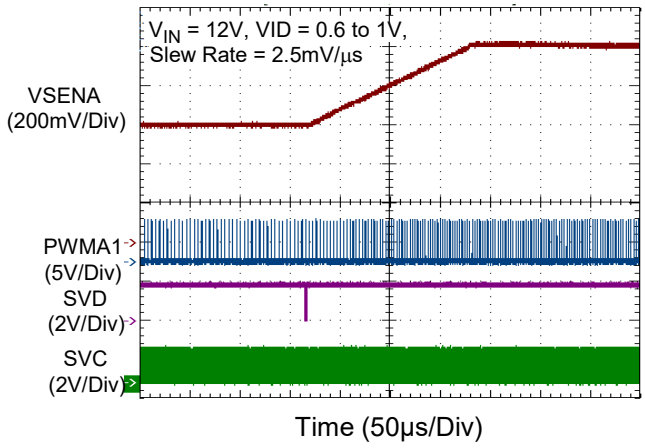
Rail A UVP



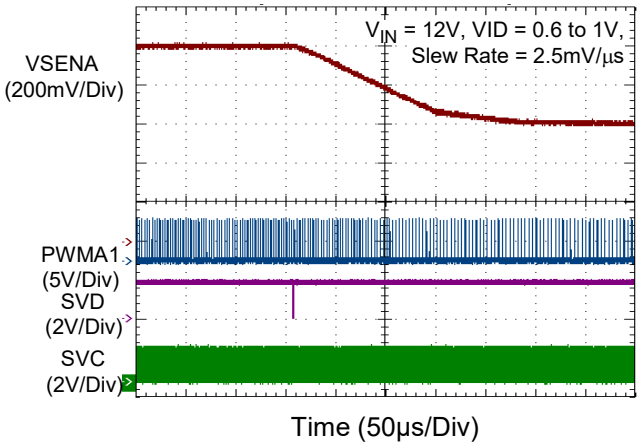
Rail A OTP and VR-HOT Warning



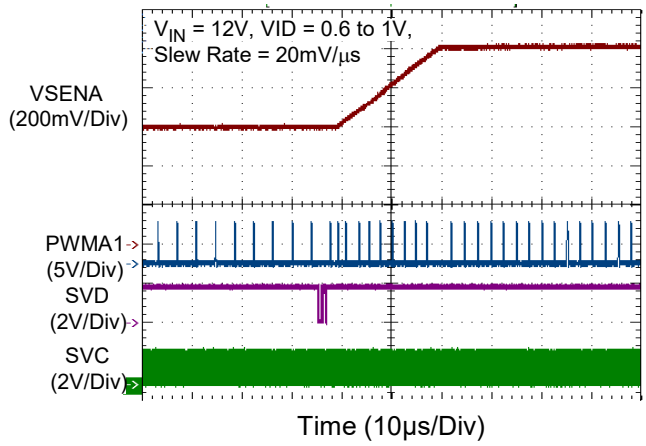
Rail A Positive VOTF Transition



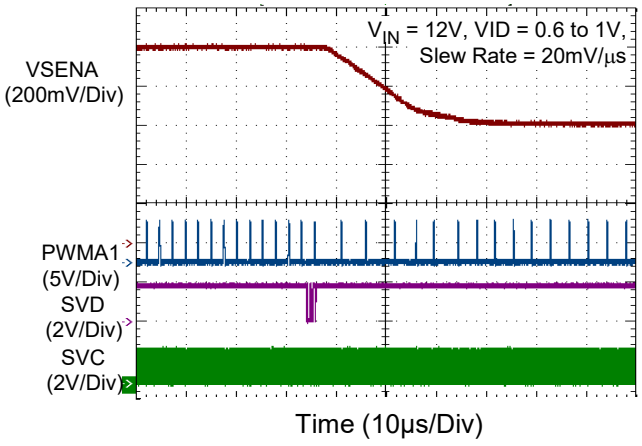
Rail A Negative VOTF Transition



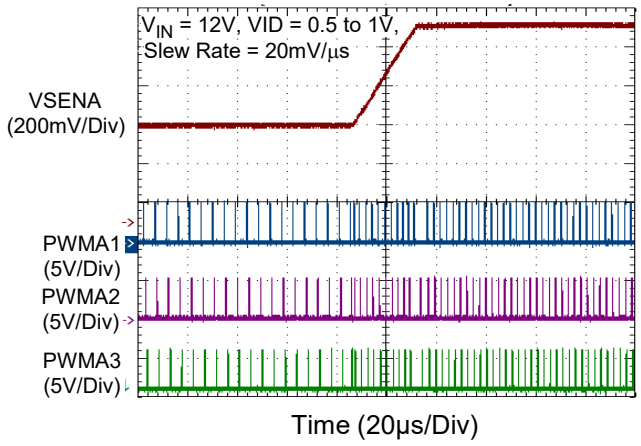
Rail A Positive VOTF Transition



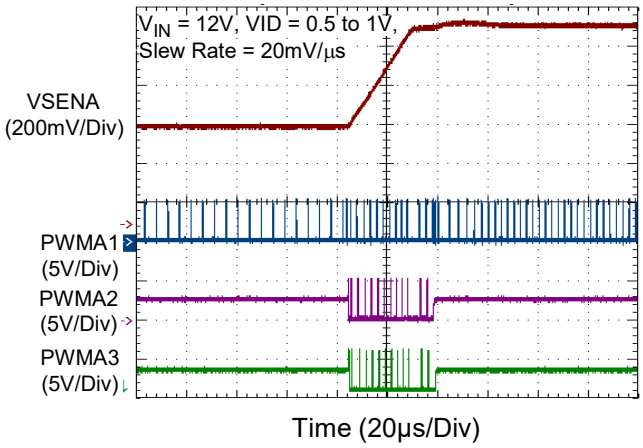
Rail A Negative VOTF Transition



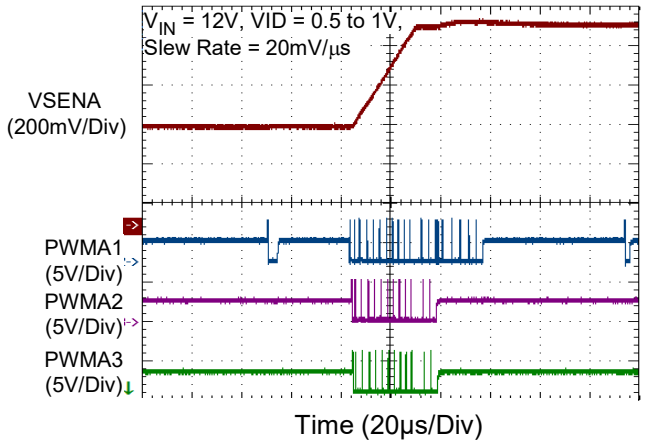
Rail A Positive VOTF Transition in PSI0



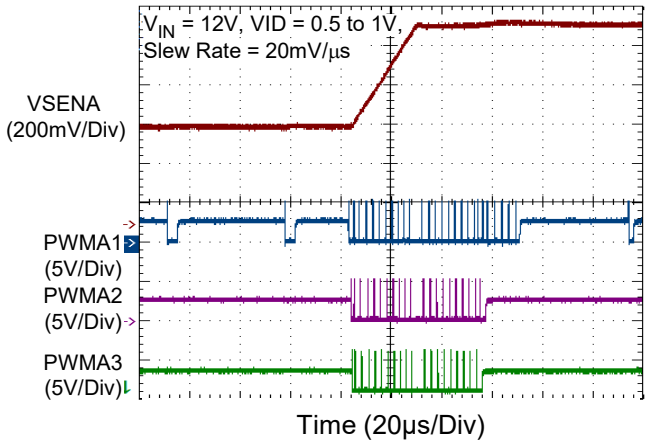
Rail A Positive VOTF Transition in PSI1



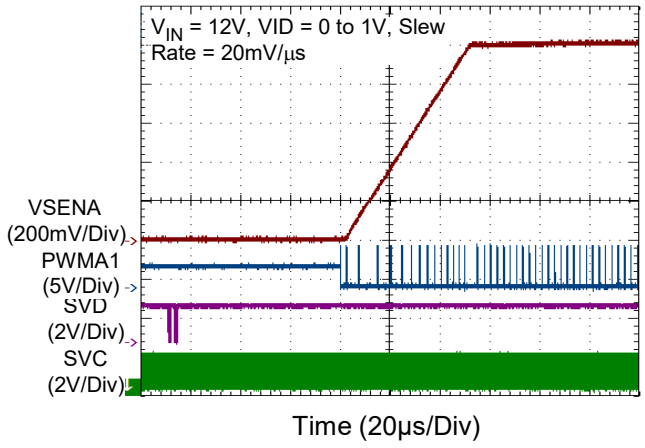
Rail A Positive VOTF Transition in PSI3



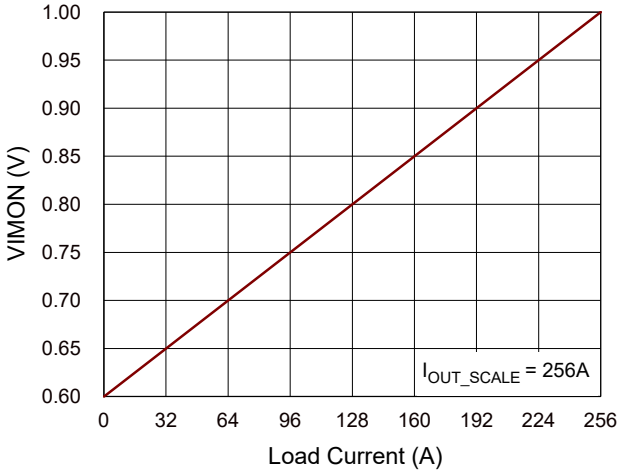
Rail A Positive VOTF Transition in PSI7



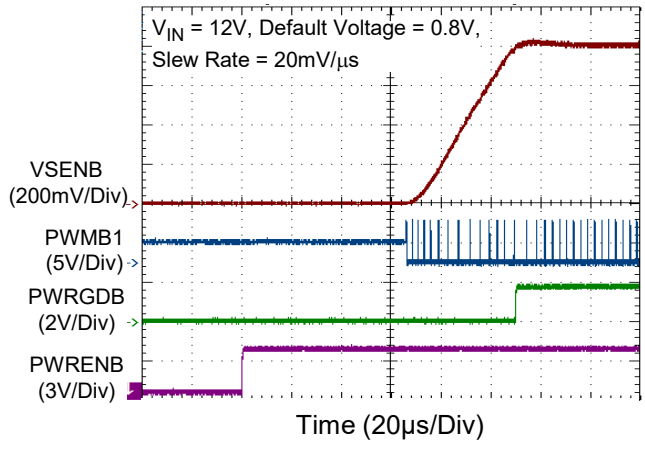
Rail A Exit Time in PSI6



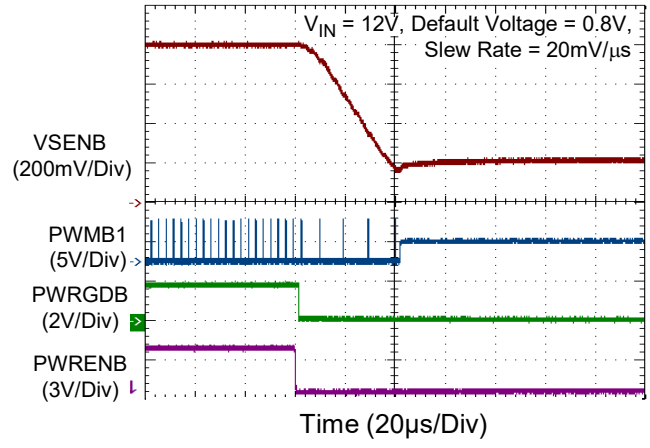
VIMON vs. Load Current



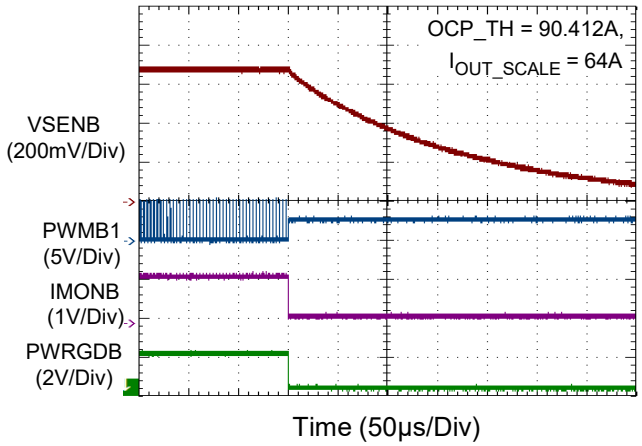
Rail B Power On from PWRENB



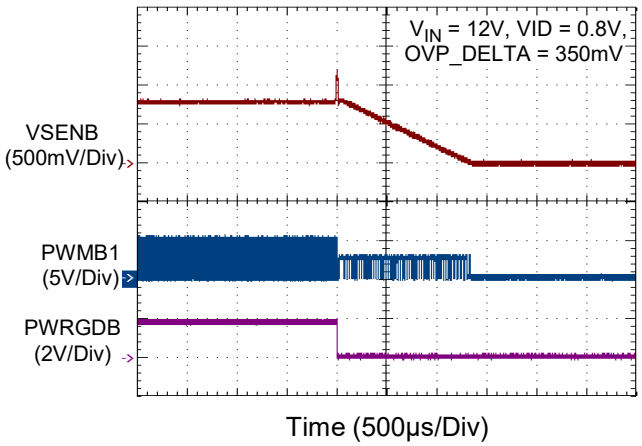
Rail B Power Off from PWRENB



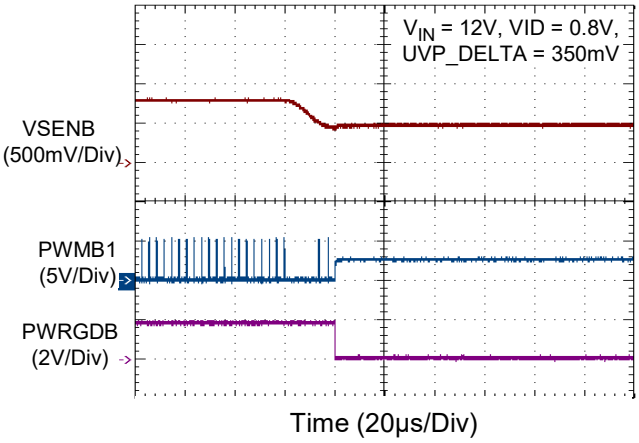
Rail B OCP



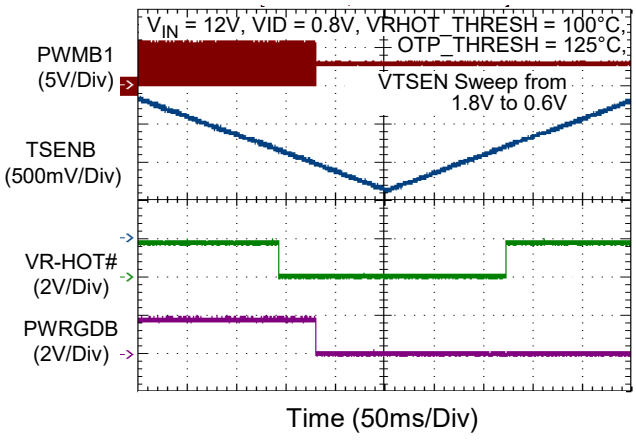
Rail B OVP



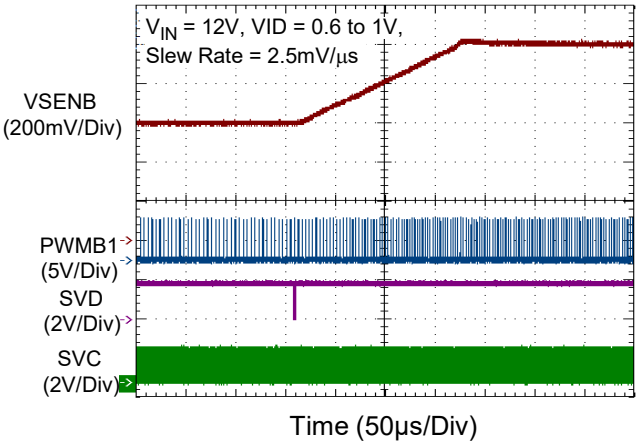
Rail B UVP



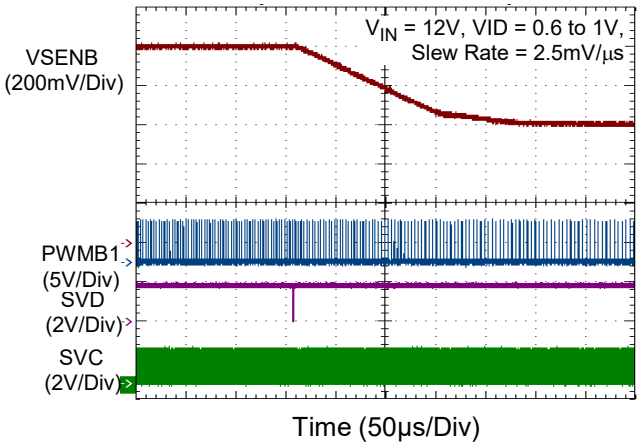
Rail B OTP and VR-HOT Warning



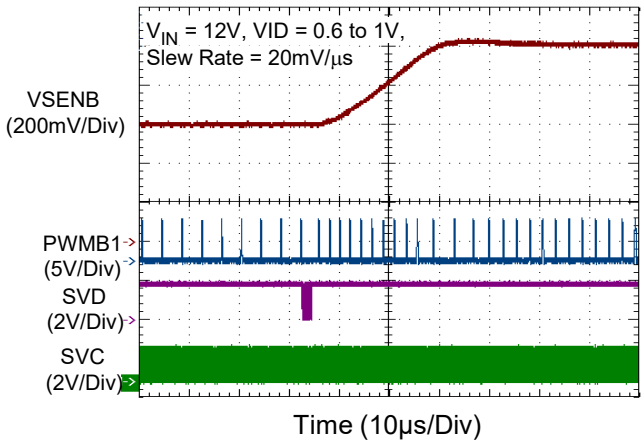
Rail B Positive VOTF Transition



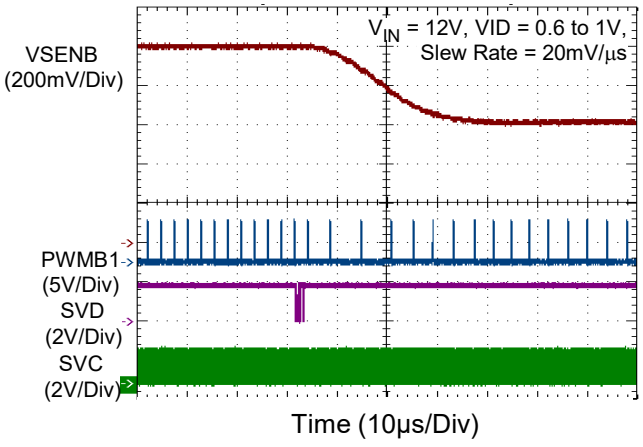
Rail B Negative VOTF Transition



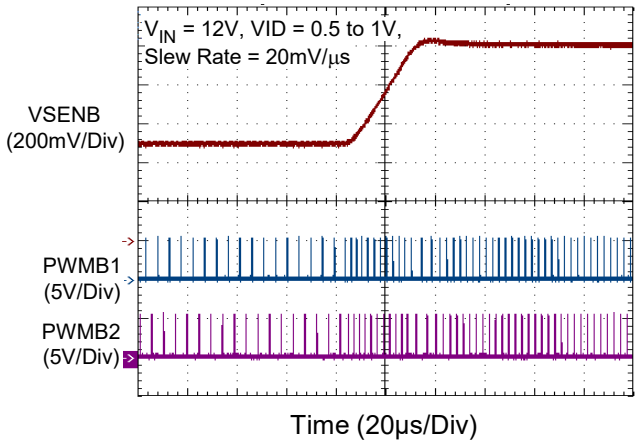
Rail B Positive VOTF Transition



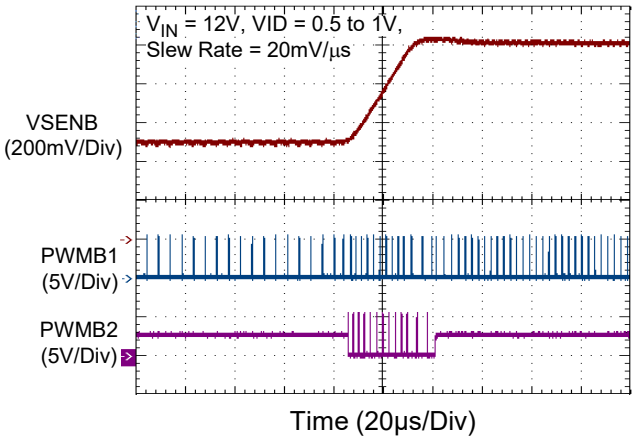
Rail B Negative VOTF Transition



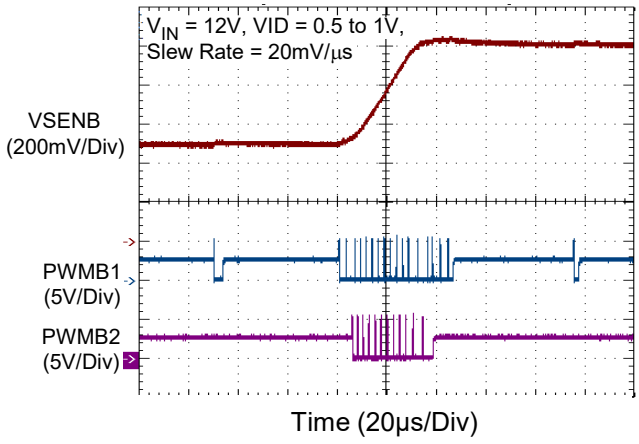
Rail B Positive VOTF Transition in PSI0



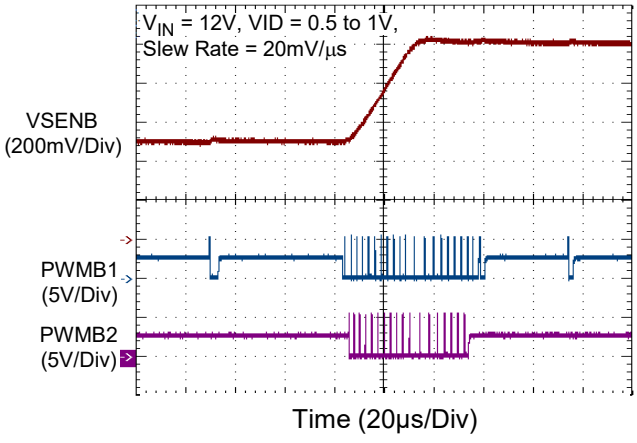
Rail B Positive VOTF Transition in PSI1



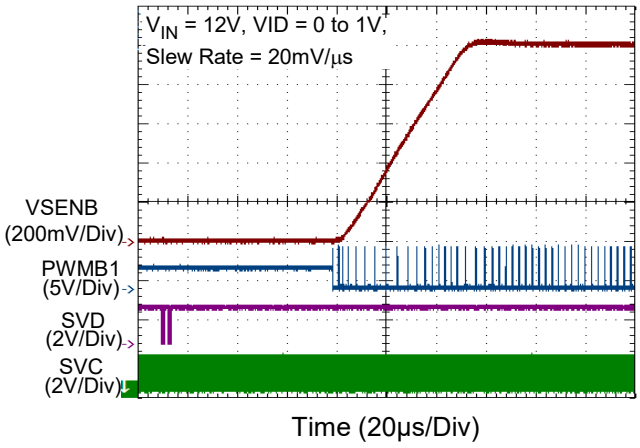
Rail B Positive VOTF Transition in PSI3



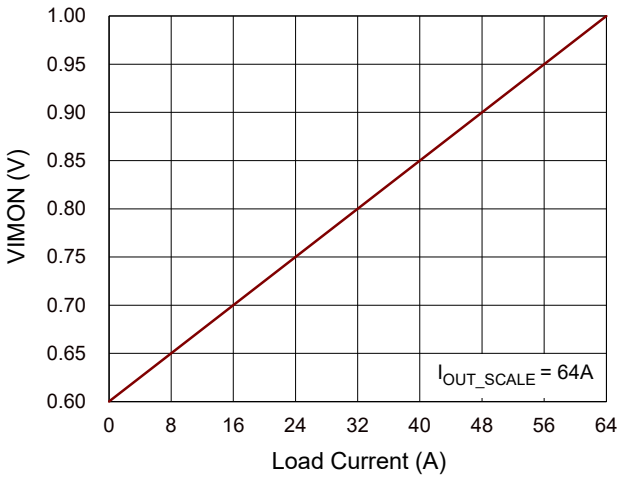
Rail B Positive VOTF Transition in PSI7



Rail B Exit Time in PSI6



VIMON vs. Load Current



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The RT3678BE is a 8-phase + 2-phase synchronous buck controller that supports two voltage rails. The RT3678BE is designed to meet AMD SVI3 compatible CPUs specification. The controller provides built-in non-volatile memory (NVM) and I^2C interface to store customized configuration. The RT3678BE is designed for notebook computers or desktop applications

Power-ON Sequence

Supply a single +5.0V (VCC) to the RT3678BE to start power-on. Figure 2 shows the power-on timings. NVM loading of the RT3678BE begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RT3678BE will download NVM into the control registers. When VCC exceeds VCC_POR, the RT3678BE starts initialization including internal circuit offset correction and function settings. During this period, the PWM outputs are held in high impedance (Hi-Z) state. Set the correct default levels for static input signals with pull-down resistors (such as for the I2C address setting). The time from VCC exceeding VCC_POR threshold to assertion of PWREN is t_{VCC_EN}. The minimum t_{VCC_EN} is 8ms. When initialization is done, the controller is in ultra-low power mode. It will ramp up to default voltage with default slew rate when PWREN is high. When the start-up process is completed, PWRGD is asserted within 5μs after the output voltage exceeds minimum tolerance of output voltage. Users can set multi-functions through NVM by I^2C interface when initialization is done.

Driver power (PVCC) is strongly suggested to be ready after controller VCC. This can prevent current flowing back from driver PVCC to controller VCC through PWMx pins or DRVEN/DRVEN_F pins.

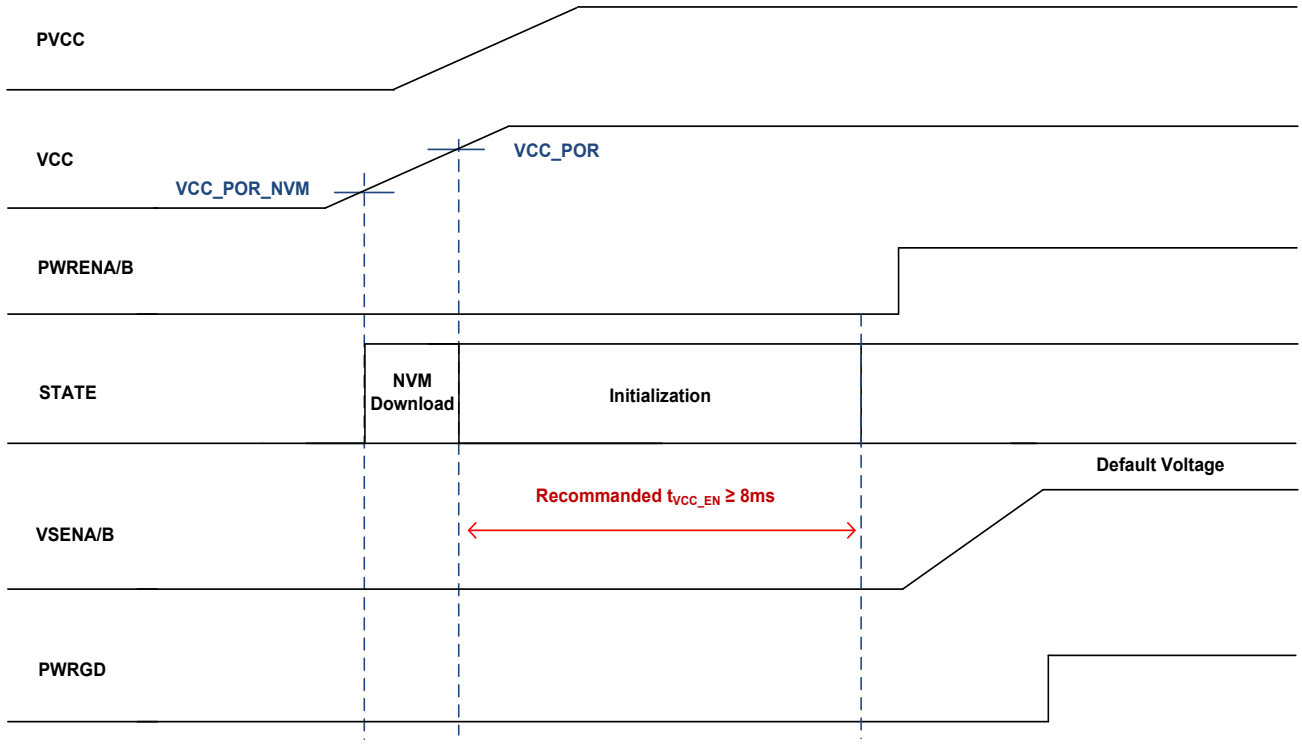


Figure 2. Typical Timing of Controller Power-ON

I²C Address Setting

The RT3678BE provides multiple I²C address to support multiple devices connected in one I²C bus. To properly set the I²C address (7-bit and 8-bit format), resistors with 1% tolerance must be connected from ADDR pin to ground. The required resistance is listed in Table 1. The controller sends the first target address followed by write bit (0b). For example, the 8-bit target address combines 7-bit address and write bit (0b):

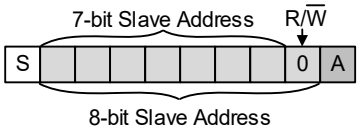


Table 1. I²C Address (HEX)

Resistance (kΩ) Typ.	I²C Address 7bit (Hex)	I²C Address 8-bit (Hex)
0.309	40	80
0.931	41	82
1.54	42	84
2.15	43	86
3.09	50	A0
4.64	51	A2
4.99	52	A4
5.9	53	A6
6.81	60	C0
8.06	61	C2
9.31	62	C4
10.7	63	C6
11.8	70	E0
13.7	71	E2
15.8	72	E4
17.4	73	E6

Acoustic Noise Suppression

The RT3678BE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band; the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3678BE adopts acoustic noise suppression function enabled by pulling ANS_EN pin to VCC to reduce ΔV during negative VOTF (Voltage On-the- Fly).

Maximum Active Phase Number Setting

The number of active phases is determined by ISENxP voltage. The detection is only active and latched at initialization state. When ISENxP voltage > (VCC−0.5V), the maximum active phase number is (x−1). For example, pulling ISENA7P and ISENA7N to VCC programs 6-phase operation. It is suggested that the unused pins (such as ISENxN, PWMx pins) can be left floating. Figure 3 is a 6-phase operation example.

Rail Disable

Pulling ISENA1P and ISENA1N to VCC disables the A rail. Pulling ISENB1P and ISENB1N to VCC disables the B rail. The unused pins (such as ISENxN, PWMx, VSEN, FB, COMP, IMON, TSEN, PWRGD and PWREN) can be left floating.

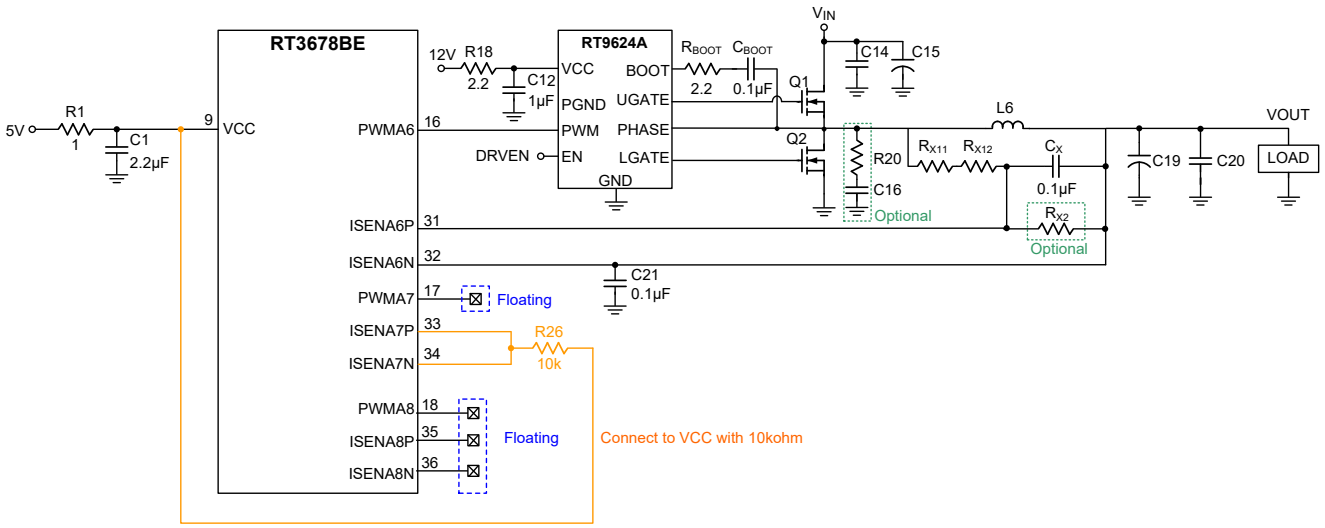


Figure 3. 6-Phase Operation Setting

NVM Configuration Mechanism and SVI3 Registers

The RT3678BE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through NVM registers by the I^2C interface. All setting functions are summarized in Table 2. Table 3 shows the functions that do not support on-line tuning. Table 4 shows the data and SVI3 registers for the SVI3 protocol. Table 5 shows the VID table of type 1 target.

Table 2. Summary of Setting Functions (Page 02)

Setting Register Map (Page 02)

Register Address/Name		Type	Default Value	Note	NVM
00h	PWM_TRI_STATE_LEVEL & TARGET_SEQ	R/W	02h	PWM tri-state window = 1.6V~2.2V, SVI3 target sequence = A → B.	Yes
01h	P_SYS_MAX & P_SYS_EN & P_SYS_SCALE	R/W	0Ch	P_SYS_MAX = 1.6V, System power telemetry enabled, P_SYS_SCALE = Scale 4: 256W	Yes
10h	CODE_VERSION_L	R/W	00h	NVM code version low byte	Yes
11h	CODE_VERSION_H	R/W	00h	NVM code version high byte	Yes
20h	VID_DEFAULT_VOLTAGE_A	R/W	48h	VID_DEFAULT_VOLTAGE_A = 0.8V	Yes
21h	RESERVED	R/W	8Ch	RESERVED	Yes
22h	RESERVED	R/W	32h	RESERVED	Yes
24h	SSOCP_EN_A & RATIO_A & I_OUT_SCALE_A	R/W	A4h	Soft-start OCP enabled for rail A, SSOCP_RATIO_A = 2.1875, I_OUT_SCALE_A = Scale 4: 255.75A.	Yes
25h	EN_0LL_A & AI_GAIN_A	R/W	50h	Zero load-line disable for A rail, AI_GAIN_A = 0.25.	Yes
26h	ZCD_TH_A	R/W	E4h	ZCD_TH_A = -0.8332mV	Yes
27h	KTON_A	R/W	04h	KTON_A = 0.7	Yes
28h	ANTI-OVS_A & VOTF_LIFT_A	R/W	E3h	Anti-overshoot disabled for rail A, VOTF_LIFT_A = 3μA.	Yes
29h	LPF_LIMIT_MUTI_PH_A & SINGLE_PH_A	R/W	63h	LPF_LIMIT_MUTI_PH_A = 220mV for rail A, LPF_LIMIT_SINGLE_PH_A = 80mV for rail A.	Yes
2Ah	FIXED_QR_WD_A & QR_TH_A	R/W	7Fh	PWM pulse = 1.25 × t_{ON}, QR with multi-phase disabled for rail A.	Yes
2Bh	FIXED_QR_WD_1PH_A & QR_TH_1PH_A	R/W	7Fh	PWM pulse = 1.25 × t_{ON}, QR with single phase disabled for rail A.	Yes
2Ch	AR_TH_1PH_A & EN_EXTD_TON_A & EXTD_TON_TH_A & EXTD_WD_MAX_A	R/W	62h	Adaptive ramp threshold for rail A = Disabled, t_{ON} extend disabled for rail A, t_{ON} extend threshold = 150mV, t_{ON} max extend width = 1.375 × t_{ON}	Yes
2Dh	RESERVED	R/W	00h	RESERVED	Yes
2Eh	RESERVED	R/W	00h	RESERVED	Yes
2Fh	RESERVED	R/W	8Ch	RESERVED	Yes
30h	MIN_TOFF_A & QR_SEL_A & QR_SEL_1PH_A	R/W	FAh	MIN_TOFF_A = 50ns, QR_SEL_A = AQR, QR_SEL_1PH_A = AQR.	Yes
31h	EAGM_GAIN_A & SLL_RATIO_A & TSEN_SEL_A	R/W	00h	EAGM_GAIN_A = 2/3, SLL_RATIO_A = 100%, TSEN_SEL_A = External NTC thermistor.	Yes
32h	RESERVED	R/W	00h	RESERVED	Yes
40h	SPM_HYS_2PH_A	R/W	03h	SPM_HYS_2PH_A = 4A	Yes
41h	SPM_HYS_3PH_A	R/W	02h	SPM_HYS_2PH_A = 2.66A	Yes
42h	SPM_HYS_45678PH_A	R/W	02h	SPM_HYS_45678PH_A = 2.66A	Yes

Register Address/Name		Type	Default Value	Note	NVM
43h	SPM_TH_2PH_A	R/W	0Dh	SPM_TH_2PH_A = 17.32A	Yes
44h	SPM_TH_3PH_A	R/W	12h	SPM_TH_3PH_A = 23.98A	Yes
45h	SPM_TH_4PH_A	R/W	19h	SPM_TH_4PH_A = 33.3A	Yes
46h	SPM_TH_5PH_A	R/W	22h	SPM_TH_5PH_A = 45.29A	Yes
47h	SPM_TH_6PH_A	R/W	2Ah	SPM_TH_6PH_A = 55.95A	Yes
48h	SPM_TH_7PH_A	R/W	2Fh	SPM_TH_7PH_A = 62.61A	Yes
49h	SPM_TH_8PH_A	R/W	38h	SPM_TH_8PH_A = 74.59A	Yes
4Ah	IOUT_CAL_OFFSET_A	R/W	00h	IOUT_CAL_OFFSET_A = 0 LSB	Yes
4Bh	IOUT_CAL_GAIN_A	R/W	80h	IOUT_CAL_GAIN_A = 100%	Yes
50h	SVI3_20h_DECAY_CONDITIONS_A	R/W	07h	Please refer to SVI3 specification. SVI3_20h_UP_SLEW_RATE_A= 20mV/μs	Yes
	SVI3_20h_DOWN_SLEW_RATE_A				
	SVI3_20h_UP_SLEW_RATE_A				
51h	SVI3_21h_LL_ADJUST_A	R/W	0Ah	Please refer to SVI3 specification.	Yes
52h	SVI3_22h_VOUT_OFFSET_A	R/W	00h	No offset.	Yes
53h	SVI3_23h_VID_MAX_A	R/W	00h	Please refer to SVI3 specification.	Yes
54h	SVI3_24h_VID_MIN_A	R/W	00h	Please refer to SVI3 specification.	Yes
55h	SVI3_25h_TEN_BIT_TEL_EN_A	R/W	00h	Please refer to SVI3 specification.	Yes
56h	SVI3_26h_SIXTEN_BIT_TEL_EN_A	R/W	00h	Please refer to SVI3 specification.	Yes
57h	SVI3_27h_OCP_THRESH_A	R/W	93h	NVM configurable, based on platform	Yes
58h	SVI3_28h_OCP_WARN_THRESH_A	R/W	93h	NVM configurable, based on platform	Yes
59h	SVI3_29h_OCP_WARN_MIN_PULSE_A	R/W	37h	NVM configurable, based on platform	Yes
	SVI3_29h_OCP_FAULT_DELAY_A				
5Ah	SVI3_2Ah_VRHOT_THRESH_A	R/W	8Ch	Please refer to SVI3 specification.	Yes
5Bh	SVI3_2Bh_OTP_THRESH_A	R/W	A5h	Please refer to SVI3 specification.	Yes
5Ch	SVI3_2Ch_OVP_REF_A	R/W	66h	Please refer to SVI3 specification.	Yes
	SVI3_2Ch_OVP_DELTA_A				
	SVI3_2Ch_UVP_REF_A				
	SVI3_2Ch_UVP_DELTA_A				
5Dh	SVI3_2Dh_PHASE_SHED_1_A	R/W	11h	Please refer to SVI3 specification.	Yes
	SVI3_2Dh_PHASE_SHED_2_A				

Register Address/Name		Type	Default Value	Note	NVM
60h	VID_DEFAULT_VOLTAGE_B	R/W	48h	VID_DEFAULT_VOLTAGE_B = 0.8V	Yes
61h	RESERVED	R/W	8Ch	RESERVED	Yes
62h	RESERVED	R/W	32h	RESERVED	Yes
64h	SSOCP_EN_B & RATIO_B & I_OUT_SCALE_B	R/W	B2h	Soft-start OCP enabled for rail B, SSOCP_RATIO_B = 2.5, I_OUT_SCALE_B = Scale 2: 63.9375A.	Yes
65h	EN_0LL_B & AI_GAIN_B	R/W	E0h	Zero load-line disable for B rail, AI_GAIN_B = 0.25.	Yes
66h	ZCD_TH_B	R/W	E2h	ZCD_TH_B = -0.4166mV	Yes
67h	KTON_B	R/W	44h	KTON_B = 0.7	Yes
68h	ANTI-OVS_B & VOTF_LIFT_B	R/W	32h	ANTI-OVS_B = 120mV VOTF_LIFT_B = 3μA	Yes
69h	LPF_LIMIT_MUTI_PH_B & SINGLE_PH_B	R/W	17h	LPF_LIMIT_MUTI_PH_A = 80mV for rail B, LPF_LIMIT_SINGLE_PH_A = 100mV for rail B.	Yes
6Ah	FIXED&ABS_QR_WD_B & QR_TH_B	R/W	7Fh	PWM pulse = 1.25 × t_{ON}, QR with multi-phase disabled for rail B.	Yes
6Bh	FIXED_QR_WD_1PH_B & QR_TH_1PH_B	R/W	5Fh	PWM pulse = 1 × t_{ON}, QR with single phase disabled for rail B.	Yes
6Ch	AR_TH_1PH_B & EN_EXTD_TON_B & EXTD_TON_TH_B & EXTD_WD_MAX_B	R/W	6Fh	Adaptive ramp threshold for rail B = Disabled, t_{ON} extend disabled for rail B, t_{ON} extend threshold = 300mV, t_{ON} max extend width = 1.25 × t_{ON}	Yes
6Dh	RESERVED	R/W	0Ch	RESERVED	Yes
6Eh	RESERVED	R/W	00h	RESERVED	Yes
6Fh	RESERVED	R/W	8Ch	RESERVED	Yes
70h	MIN_TOFF_B & QR_SEL_B & QR_SEL_1PH_B	R/W	FEh	MIN_TOFF_B = 50ns, QR_SEL_B = AQR, QR_SEL_1PH_B = AQR.	Yes
71h	EAGM_GAIN_B & SLL_RATIO_B & TSEN_SEL_B	R/W	80h	EAGM_GAIN_B = 1, SLL_RATIO_B = 100%, TSEN_SEL_B = External NTC thermistor.	Yes
72h	QR_TRIGGER_SEL & ABSOVS_TH_B & ABS_QR_B	R/W	00h	QR_TRIGGER_SE = Absolute (ABSQR), Absolute-OVS disabled for rail B, Absolute-QR disabled for rail B.	Yes
80h	SPM_HYS_2PH_B	R/W	0Dh	SPM_HYS_2PH = 4.33A	Yes
83h	SPM_TH_2PH_B	R/W	2Dh	SPM_TH_2PH = 14.99A	Yes
8Ah	IOUT_CAL_OFFSET_B	R/W	00h	IOUT_CAL_OFFSET_B = 0 LSB	Yes
8Bh	IOUT_CAL_GAIN_B	R/W	80h	IOUT_CAL_GAIN_B = 100%	Yes

Register Address/Name		Type	Default Value	Note	NVM
90h	SVI3_20h_DECAY_CONDITIONS_B	R/W	07h	Please refer to SVI3 specification. SVI3_20h_UP_SLEW_RATE_B= 20mV/μs.	Yes
	SVI3_20h_DOWN_SLEW_RATE_B				
	SVI3_20h_UP_SLEW_RATE_B	R/W			
91h	SVI3_21h_LL_ADJUST_B	R/W	0Ah	Please refer to SVI3 specification.	Yes
92h	SVI3_22h_VOUT_OFFSET_B	R/W	00h	No offset.	Yes
93h	SVI3_23h_VID_MAX_B	R/W	00h	Please refer to SVI3 specification.	Yes
94h	SVI3_24h_VID_MIN_B	R/W	00h	Please refer to SVI3 specification.	Yes
95h	SVI3_25h_TEN_BIT_TEL_EN_B	R/W	00h	Please refer to SVI3 specification.	Yes
96h	SVI3_26h_SIXTEN_BIT_TEL_EN_B	R/W	00h	Please refer to SVI3 specification.	Yes
97h	SVI3_27h_OCP_THRESH_B	R/W	B5h	NVM configurable, based on platform	Yes
98h	SVI3_28h_OCP_WARN_THRESH_B	R/W	B5h	NVM configurable, based on platform	Yes
99h	SVI3_29h_OCP_WARN_MIN_PULSE_B	R/W	37h	NVM configurable, based on platform	Yes
	SVI3_29h_OCP_FAULT_DELAY_B				
9Ah	SVI3_2Ah_VRHOT_THRESH_B	R/W	8Ch	Please refer to SVI3 specification.	Yes
9Bh	SVI3_2Bh_OTP_THRESH_B	R/W	A5h	Please refer to SVI3 specification.	Yes
9Ch	SVI3_2Ch_OVP_REF_B	R/W	66h	Please refer to SVI3 specification.	Yes
	SVI3_2Ch_OVP_DELTA_B				
	SVI3_2Ch_UVP_REF_B				
	SVI3_2Ch_UVP_DELTA_B				
9Dh	SVI3_2Dh_PHASE_SHED_1_B	R/W	11h	Please refer to SVI3 specification.	Yes
	SVI3_2Dh_PHASE_SHED_2_B				
A0h	CRC-8 Code	R	Current status	NVM registers CRC-8 code. The Data is updated when VCC POR or restore NVM. The polynomial is $X^8 + X^2 + X^1 +1$.	No

Register Address	Bits	Register Name	Description
0x00	[7:3]	RESERVED	**Reserved bit(s).** [7:3] = 00000 (Default). All other combinations are not defined.
	[2]	PWM_TRI_STATE_LEVEL	**Set PWM tri-state window.** [2] = 0: PWM tri-state level is 1.6V to 2.2V. [2] = 1: PWM tri-state level is 1.4V to 2.1V.
	[1:0]	TARGET_SEQ	**Set SVI3 target sequence.** [1:0] = 10: A → B, [1:0] = 11: B → A, [1:0] = 00 to 01: Reserved, all other combinations are not defined.
0x01	[7:5]	RESERVED	**Reserved bit(s)**. [7:5] = 000 (Default). All other combinations are not defined.
	[4]	P_SYS_MAX	**P_SYS voltage range selections.** [4] = 0: P_{SYS} max = 1.6V, [4] = 1: P_{SYS} max = 3.2V.
	[3]	P_SYS_EN	**Enable P_SYS reporting function.** [3] = 0: Disable, [3] = 1: Enable.
	[2:0]	P_SYS_SCALE	**System power scale.** SVI3 register P_SYS_SCALE_0Ch[2:0]. [2:0] = 000: CUSTOM, [2:0] = 100: Scale 4 = 255.75W, [2:0] = 001: Scale 1 = 31.96875W, [2:0] = 101: Scale 5 = 511.5W, [2:0] = 010: Scale 2 = 63.9375W, [2:0] = 110: Scale 6 = 1023W, [2:0] = 011: Scale 3 = 127.875W, [2:0] = 111: Scale 7 = 2046W.
0x10	[7:0]	CODE_VERSION_L	**MTP Code Version.**
0x11	[7:0]	CODE_VERSION_H	**MTP Code Version.**
0x20	[7:4]	VID_DEFAULT_VOLTAGE_A	**Default VID setting for rail A.** SVI3 register VID_DEFAULT_VOLTAGE_08h[3:0]. [7:4] = 0000: OFF, [7:4] = 1000: 1.2V, [7:4] = 0001: 0.5V, [7:4] = 1001: 1.3V, [7:4] = 0010: 0.6V, [7:4] = 1010: 1.4V, [7:4] = 0011: 0.7V, [7:4] = 1011: 1.5V, [7:4] = 0100: 0.8V, [7:4] = 1100: 1.8V, [7:4] = 0101: 0.9V, [7:4] = 1101: 2V, [7:4] = 0110: 1V, [7:4] = 1110: 2.5V, [7:4] = 0111: 1.1V, [7:4] = 1111: 2.8V.
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 1000 (Default). All other combinations are not defined.
0x21	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 8Ch (Default). All other combinations are not defined.
0x22	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 32h (Default). All other combinations are not defined.

Register Address	Bits	Register Name	Description
0x24	[7]	SSOCP_EN_A	**Enable soft-start overcurrent protection for rail A.** [7] = 0: Disable. [7] = 1: Enable.
	[6:4]	SSOCP_RATIO_A	**Soft-start overcurrent protection ratio for rail A.** SSOCP_TH = I_OUT_SCALE × SSOCP_RATIO [6:4] = 000: 1.25, [6:4] = 100: 3.125, [6:4] = 001: 1.875, [6:4] = 101: 3.75, [6:4] = 010: 2.1875, [6:4] = 110: 4.375, [6:4] = 011: 2.5, [6:4] = 111: 5.
	[3]	RESERVED	**Reserved bit(s).** [3] = 0 (Default). All other combinations are not defined.
	[2:0]	I_OUT_SCALE_A	**Output current scale selections for rail A.** SVI3 register I_OUT_SCALE_09h[5:3]. [2:0] = 000: CUSTOM, [2:0] = 100: Scale 4 = 255.75A, [2:0] = 001: Scale 1 = 31.96875A, [2:0] = 101: Scale 5 = 511.5A, [2:0] = 010: Scale 2 = 63.9375A, [2:0] = 110: Scale 6 = 1023A, [2:0] = 011: Scale 3 = 127.875A, [2:0] = 111: Scale 7 = 2046A.
0x25	[7:4]	RESERVED	**Reserved bit(s).** [7:4] = 1101 (Default). All other combinations are not defined.
	[3]	EN_0LL_A	**Enable zero load-line for rail A.** [3] = 0: Disable, [3] = 1: Enable.
	[2:0]	AI_GAIN_A	**Ai Gain is the gain of current sense amplifier for rail A.** [2:0] = 000: 0.250, [2:0] = 100: 0.125, [2:0] = 001: 0.500, [2:0] = 101: 0.375, [2:0] = 010: 0.750, [2:0] = 110: 0.625, [2:0] = 011: 1.000, [2:0] = 111: 0.875.
0x26	[7:6]	RESERVED	**Reserved bit(s).** [7:6] = 11 (Default). All other combinations are not defined.
	[5:0]	ZCD_TH_A	**Zero current threshold setting of each phase sensed current for rail A.** [5]: Sign bit, 0 stands for positive values and 1 for negative. [4:0]: 0.2083mV/step. For example, [5:0] = 000000: ZCD_TH = 0mV, [5:0] = 000001: ZCD_TH = 0.2083mV, [5:0] = 000010: ZCD_TH = 0.4166mV, [5:0] = 000011: ZCD_TH = 0.6249mV, [5:0] = 011111: ZCD_TH = 6.4573mV, [5:0] = 100000: ZCD_TH = 0mV, [5:0] = 100001: ZCD_TH = –0.2083mV, [5:0] = 100010: ZCD_TH = –0.4166mV, [5:0] = 100011: ZCD_TH = –0.6249mV, [5:0] = 111111: ZCD_TH = –6.4573mV.

Register Address	Bits	Register Name	Description
0x27	[7:5]	RESERVED	**Reserved bit(s).** [7:5] = 000 (Default). All other combinations are not defined.
	[4:0]	KTON_A	**On-time (tON) K-Factor setting for rail A.** **When reg. addr 0x27[4] = 0:** KTON = 0.3 + [3:0] × 0.1 **When reg. addr 0x27[4] = 1:** KTON = 1.2 + [3:0] × 0.1 Ex. [4:0] = 00000: KTON = 0.3, [4:0] = 00100: KTON = 0.7, [4:0] = 01111: KTON = 1.8, [4:0] = 10000: KTON = 1.2, [4:0] = 10100: KTON = 1.6, [4:0] = 11111: KTON = 2.7.
0x28	[7:5]	ANTI-OVS_A	**Anti-Overshoot threshold setting with load-line for rail A.** [7:5] = 000: 120mV, [7:5] = 100: 360mV, [7:5] = 001: 180mV, [7:5] = 101: 420mV, [7:5] = 010: 240mV, [7:5] = 110: 480mV, [7:5] = 011: 300mV, [7:5] = 111: disable.
	[4:0]	VOTF_LIFT_A	**Output compensation setting for VOTF (Voltage On-the-Fly) for rail A.** [4:0] = 00000: disable [4:0] = 10000: 21μA, [4:0] = 00001: 1μA, [4:0] = 10001: 24μA, [4:0] = 00010: 2μA, [4:0] = 10010: 27μA, [4:0] = 00011: 3μA, [4:0] = 10011: 28μA, [4:0] = 00100: 4μA, [4:0] = 10100: 30μA, [4:0] = 00101: 5μA, [4:0] = 10101: 32μA, [4:0] = 00110: 6μA, [4:0] = 10110: 36μA, [4:0] = 00111: 7μA, [4:0] = 10111: 40μA, [4:0] = 01000: 8μA, [4:0] = 11000: 42μA, [4:0] = 01001: 9μA, [4:0] = 11001: 48μA, [4:0] = 01010: 10μA, [4:0] = 11010: 54μA, [4:0] = 01011: 12μA, [4:0] = 11011: 56μA, [4:0] = 01100: 14μA, [4:0] = 11100: 60μA, [4:0] = 01101: 16μA, [4:0] = 11101: 64μA, [4:0] = 01110: 18μA, [4:0] = 11110: 72μA, [4:0] = 01111: 20μA, [4:0] = 11111: 80μA.
0x29	[7:4]	LPF_LIMIT_MUTI_PH_A	**High frequency ACLL compensation setting with multi-phase operation and load-line for rail A.** LPF_LIMIT_MUTI_PH = 100mV + [7:4] × 20mV Ex. [7:4] = 0000: LPF_LIMIT_MUTI_PH = 100mV, [7:4] = 0010: LPF_LIMIT_MUTI_PH = 140mV, [7:4] = 1111: LPF_LIMIT_MUTI_PH = 400mV.
	[3:0]	LPF_LIMIT_SINGLE_PH_A	**High frequency ACLL compensation setting with single phase operation and load-line for rail A.** LPF_LIMIT_SINGLE_PH = 50mV + [3:0] × 10mV Ex. [3:0] = 0000: LPF_LIMIT_SINGLE_PH = 50mV, [3:0] = 0010: LPF_LIMIT_SINGLE_PH = 70mV, [3:0] = 1111: LPF_LIMIT_SINGLE_PH = 200mV.

Register Address	Bits	Register Name	Description
0x2A	[7]	RESERVED	**Reserved bit(s).** [7] = 0 (Default). All other combinations are not defined.
	[6:5]	FIXED_QR_WD_A	**Setting Fixed-QR PWM width for multi-phase operation for rail A.** [6:5] = 00: 0.50 × t_{ON}, [6:5] = 01: 0.75 × t_{ON}, [6:5] = 10: 1.00 × t_{ON}, [6:5] = 11: 1.25 × t_{ON}.
	[4:0]	QR_TH_A	**Setting QR triggering level with multi-phase operation for rail A.** **QR_TH = 40mV + [4:0] x 80mV** Ex. [4:0] = 00000: QR_TH = 40mV, [4:0] = 00001: QR_TH = 120mV, [4:0] = 01000: QR_TH = 680mV, [4:0] = 01111: QR_TH = 1240mV, [4:0] = 11111: Disable.
0x2B	[7]	RESERVED	**Reserved bit(s).** [7] = 0 (Default). All other combinations are not defined.
	[6:5]	FIXED_QR_WD_1PH_A	**Setting width of Fixed-QR with single phase operation for rail A.** [6:5] = 00: 0.50 × t_{ON}, [6:5] = 01: 0.75 × t_{ON}, [6:5] = 10: 1.00 × t_{ON}, [6:5] = 11: 1.25 × t_{ON}.
	[4:0]	QR_TH_1PH_A	**Setting QR triggering level with single phase operation for rail A.** **QR_TH_1PH_A = 40mV + [4:0] x 40mV** Ex. [4:0] = 00000: QR_TH = 40mV, [4:0] = 00001: QR_TH = 80mV, [4:0] = 01000: QR_TH = 360mV, [4:0] = 01111: QR_TH = 640mV, [4:0] = 11111: Disable.
0x2C	[7:5]	AR_TH_1PH_A	**Setting Adaptive ramp threshold with single phase operation for rail A.** [7:5] = 000: 250mV, [7:5] = 100: 225mV, [7:5] = 001: 200mV, [7:5] = 101: 175mV, [7:5] = 010: 150mV, [7:5] = 110: 125mV, [7:5] = 011: Disable, [7:5] = 111: Disable.
	[4]	EN_EXTD_TON_A	**Enable t_{ON} Extend function for rail A.** [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	EXTD_TON_TH_A	**Setting the threshold to extend t_{ON} for rail A.** [3:2] = 00: 150mV, [3:2] = 01: 200mV, [3:2] = 10: 250mV, [3:2] = 11: 300mV.
	[1:0]	EXTD_WD_MAX_A	**Extend TON setting for rail A.** [1:0] = 00: 1.625 × t_{ON}, [1:0] = 01: 1.500 × t_{ON}, [1:0] = 10: 1.375 × t_{ON}, [1:0] = 11: 1.250 × t_{ON}.

Register Address	Bits	Register Name	Description
0x2D	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 00h (Default). All other combinations are not defined.
0x2E	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 00h (Default). All other combinations are not defined.
0x2F	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 8Ch (Default). All other combinations are not defined.
0x30	[7:6]	MIN_TOFF_A	**PWM minimum off-time setting for rail A.** [7:6] = 00: MIN_TOFF = 300ns, [7:6] = 01: MIN_TOFF = 200ns, [7:6] = 10: MIN_TOFF = 120ns, [7:6] = 11: MIN_TOFF = 50ns.
	[5]	QR_SEL_A	**Select QR type with multi-phase operation and load-line for rail A.** [5] = 0: Fixed-QR [5] = 1: Adaptive-QR
	[4]	QR_SEL_1PH_A	**Select QR type with single phase operation and load-line for rail A.** [4] = 0: Fixed-QR [4] = 1: Adaptive-QR
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 1010 (Default). All other combinations are not defined.
0x31	[7]	EAGM_GAIN_A	**Setting transconductance gain of error amplifier for rail A.** [7] = 0: EAGM_GAIN = 2/3 [7] = 1: EAGM_GAIN = 1
	[6:4]	SLL_RATIO_A	**Short-term voltage target ration during AC transient for rail A.** Short-term voltage target = VID − ΔIcc × RLL × SLL_RATIO [6:4] = 000: 100% [6:4] = 100: 75% [6:4] = 001: 95% [6:4] = 101: 65% [6:4] = 010: 90% [6:4] = 110: 55% [6:4] = 011: 85% [6:4] = 111: 50%
	[3:2]	RESERVED	**Reserved bit(s).** [3:2] = 00(Default). All other combinations are not defined.
	[1]	TSEN_SEL_A	**Temperature source selection for rail A.** [1] = 0: External NTC thermistor (NTC is 100kΩ/Beta = 4250), [1] = 1: Integrated power stage temperature sensor. V_{TSEN} voltage represents temperature information at 8mV/°C + 0.6V.
	[0]	RESERVED	**Reserved bit(s).** [0] = 0 (Default). All other combinations are not defined.
0x32	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 00h (Default). All other combinations are not defined.
0x40	[7:0]	SPM_HYS_2PH_A	**Set Smart Phase Management (SPM) current hysteresis with 2-phase down to 1 phase in PSI7 for rail A.** LSB = I_OUT_SCALE/192A For I_OUT_SCALE = Scale 4, LSB = 1.332A, [7:0] = 00h: SPM_HYS = 0A, [7:0] = 05h: SPM_HYS = 6.66A, [7:0] = 0Ah: SPM_HYS = 13.32A, [7:0] = C0h: SPM_HYS = 255.75A,
0x41	[7:0]	SPM_HYS_3PH_A	**Set Smart Phase Management (SPM) current hysteresis with 3-phase down to 2-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x42	[7:0]	SPM_HYS_4PH_A	**Set Smart Phase Management (SPM) current hysteresis with N phase down to (N-1) phase in PSI7 with N ≥ 4 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.

Register Address	Bits	Register Name	Description
0x43	[7:0]	SPM_TH_2PH_A	**Set Smart Phase Management (SPM) current threshold with 1-phase up to 2-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x44	[7:0]	SPM_TH_3PH_A	**Set Smart Phase Management (SPM) current threshold with 2-phase up to 3-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x45	[7:0]	SPM_TH_4PH_A	**Set Smart Phase Management (SPM) current threshold with 3-phase up to 4-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x46	[7:0]	SPM_TH_5PH_A	**Set Smart Phase Management (SPM) current threshold with 4-phase up to 5-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x47	[7:0]	SPM_TH_6PH_A	**Set Smart Phase Management (SPM) current threshold with 5-phase up to 6-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x48	[7:0]	SPM_TH_7PH_A	**Set Smart Phase Management (SPM) current threshold with 6-phase up to 7-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x49	[7:0]	SPM_TH_8PH_A	**Set Smart Phase Management (SPM) current threshold with 7-phase up to 8-phase in PSI7 for rail A.** Please refer to SPM_HYS_2PH_A for detailed description.
0x4A	[7:0]	IOUT_CAL_OFFSET_A	**IOUT telemetry offset for rail A.** [7]: sign bit, as part of two's complement, [6:0]: 1LSB = I_OUT_SCALE/1023 Ex. [7:0] = 00h: IOUT_CAL_OFFSET = 0, [7:0] = 01h: IOUT_CAL_OFFSET = +1 LSB, [7:0] = 7Fh: IOUT_CAL_OFFSET = +127 LSB, [7:0] = FFh: IOUT_CAL_OFFSET = -1 LSB, [7:0] = 80h: IOUT_CAL_OFFSET = -128 LSB,
0x4B	[7:0]	IOUT_CAL_GAIN_A	**IOUT telemetry gain for rail A.** LSB = 2^(-9), Telemetry = IMONADC × IOUT_CAL_GAIN + IOUT_CAL_OFFSET [7:0] = 00h: IOUT_CAL_GAIN = 75%, [7:0] = 80h: IOUT_CAL_GAIN = 100%, [7:0] = FFh: IOUT_CAL_GAIN = 124.8%.

Register Address	Bits	Register Name	Description
0x50	[7:5]	SVI3_20h_DECAY_CONDITIONS_A	Please refer to SVI3 specification.
	[4]	SVI3_20h DOWN_SLEW_RATE_A	
	[3:0]	SVI3_20h UP_SLEW_RATE_A	**Slew rate for positive VID change for rail A.** SVI3 register UP_SLEW_RATE_20h[3:0]. Slew rate = 50h[3:0] x 2.5 + 2.5 mV/μs
0x51	[7:5]	RESERVED	**Reserved bit(s).** [7:5] = 000 (Default). All other combinations are not defined.
	[4:0]	SVI3_21h LL_ADJUST_A	Please refer to SVI3 specification.
0x52	[7:0]	SVI3_22h_VOUT_OFFSET_A	**Voltage offset applied to VID, VID_MIN,VID_MAX, OVP_THRESH and UVP_THRESH for rail A.** SVI3 register VOUT_OFFSET_20h[7:0]. [7:0] = 00h: Disabled (no offset) Offset = 52h[7:0] x 20 - 250mV
0x53	[7:0]	SVI3_23h_VID_MAX_A	Please refer to SVI3 specification.
0x54	[7:0]	SVI3_24h_VID_MIN_A	Please refer to SVI3 specification.
0x55	[7:0]	SVI3_25h_TEN_BIT_TEL_EN_A	Please refer to SVI3 specification.
0x56	[7:0]	SVI3_26h_SIXTEEN_BIT_TEL_EN_A	Please refer to SVI3 specification.
0x57	[7:0]	SVI3_27h_OCP_THRESH_A	**Overcurrent protection threshold level for rail A.** SVI3 register OCP_THRESH_20h[7:0]. [7:0] = 00h: Disabled (no OCP protection) OCP Threshold = 57h[7:0] x 4 x MAX_CURRENT/512A Note: MAX_CURRENT = 3FFh of selected current scale.
0x58	[7:0]	SVI3_28h_OCP_WARN_THRESH_A	**Overcurrent warning threshold level for rail A.** SVI3 register OCP_WARN_THRESH_28h[7:0]. [7:0] = 00h: Disabled OCP Threshold = 98h[7:0] x 4 x MAX_CURRENT/512A Note: MAX_CURRENT = 3FFh of selected current scale.
0x59	[7:3]	SVI3_28h_OCP_WARN_MIN_PULSE_A	**Minimum asserted pulse width of OCP_WARN signal for rail A.** SVI3 register OCP_WARN_MIN_PULSE_28h[7:3]. Minimum pulse = 59h[7:3] x 500ns
	[2:0]	SVI3_29h_OCP_FAULT_DELAY_A	**Continuous time that current must exceed OCP_THRESH before triggering fault for rail A.** SVI3 register OCP_FAULT_DELAY_29h[2:0]. [2:0] = 000: Instantaneous fault Fault delay = 59h[2:0] x 5μs.
0x5A	[7:0]	SVI3_2Ah_VRHOT_THRESH_A	Please refer to SVI3 specification.
0x5B	[7:0]	SVI3_2Bh_OTP_THRESH_A	Please refer to SVI3 specification.
0x5C	[7]	SVI3_2Ch_OVP_REF_A	Please refer to SVI3 specification.
	[6:4]	SVI3_2Ch OVP_DELTA_A	
	[3]	SVI3_2Ch UVP_REF_A	
	[2:0]	SVI3_2Ch UVP_DELTA_A	
0x5D	[7:4]	SVI3_2Dh_PHASE_SHED_1	Please refer to SVI3 specification.
	[3:0]	SVI3_2Dh_PHASE_SHED_2	

Register Address	Bits	Register Name	Description
0x60	[7:4]	VID_DEFAULT_VOLTAGE_B	**Default VID setting for rail B.** SVI3 register VID_DEFAULT_VOLTAGE_08h[3:0]. [7:4] = 0000: OFF, [7:4] = 1000: 1.2V, [7:4] = 0001: 0.5V, [7:4] = 1001: 1.3V, [7:4] = 0010: 0.6V, [7:4] = 1010: 1.4V, [7:4] = 0011: 0.7V, [7:4] = 1011: 1.5V, [7:4] = 0100: 0.8V, [7:4] = 1100: 1.8V, [7:4] = 0101: 0.9V, [7:4] = 1101: 2V, [7:4] = 0110: 1V, [7:4] = 1110: 2.5V, [7:4] = 0111: 1.1V, [7:4] = 1111: 2.8V.
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 1000 (Default). All other combinations are not defined.
0x61	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 8Ch (Default). All other combinations are not defined.
0x62	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 32h (Default). All other combinations are not defined.
0x64	[7]	SSOCP_EN_B	**Enable soft-start overcurrent protection for rail B.** [7] = 0: Disable. [7] = 1: Enable.
	[6:4]	SSOCP_RATIO_B	**Soft-start overcurrent protection ratio for rail B.** SSOCP_TH = I_OUT_SCALE × SSOCP_RATIO [6:4] = 000: 1.25, [6:4] = 100: 3.125, [6:4] = 001: 1.875, [6:4] = 101: 3.75, [6:4] = 010: 2.1875, [6:4] = 110: 4.375, [6:4] = 011: 2.5, [6:4] = 111: 5.
	[3]	RESERVED	**Reserved bit(s).** [3] = 0 (Default). All other combinations are not defined.
	[2:0]	I_OUT_SCALE_B	**Output current scale selections for rail B.** SVI3 register I_OUT_SCALE_09h[5:3]. [2:0] = 000: CUSTOM, [2:0] = 100: Scale 4 = 255.75A, [2:0] = 001: Scale 1 = 31.96875A, [2:0] = 101: Scale 5 = 511.5A, [2:0] = 010: Scale 2 = 63.9375A, [2:0] = 110: Scale 6 = 1023A, [2:0] = 011: Scale 3 = 127.875A, [2:0] = 111: Scale 7 = 2046A.
0x65	[7:4]	RESERVED	**Reserved bit(s).** [7:4] = 1110 (Default). All other combinations are not defined.
	[3]	EN_0LL_B	**Enable zero load-line for rail B.** [3] = 0: Disable. [3] = 1: Enable.
	[2:0]	AI_GAIN_B	**Ai Gain is the gain of current sense amplifier for rail B.** [2:0] = 000: 0.250, [2:0] = 100: 0.125, [2:0] = 001: 0.500, [2:0] = 101: 0.375, [2:0] = 010: 0.750, [2:0] = 110: 0.625, [2:0] = 011: 1.000, [2:0] = 111: 0.875.

Register Address	Bits	Register Name	Description
0x66	[7:6]	RESERVED	**Reserved bit(s).** [7:6] = 11 (Default). All other combinations are not defined.
	[5:0]	ZCD_TH_B	**Zero current threshold setting of each phase sensed current for rail B.** [5]: Sign bit, 0 stands for positive values and 1 for negative. [4:0]: 0.2083mV/step. For example, [5:0] = 000000: ZCD_TH = 0mV, [5:0] = 000001: ZCD_TH = 0.2083mV, [5:0] = 000010: ZCD_TH = 0.4167mV, [5:0] = 011111: ZCD_TH = 6.4573mV, [5:0] = 100000: ZCD_TH = 0mV, [5:0] = 100001: ZCD_TH = –0.2083mV, [5:0] = 100010: ZCD_TH = –0.4167mV, [5:0] = 111111: ZCD_TH = –6.4573mV.
0x67	[7:5]	RESERVED	**Reserved bit(s).** [7:5] = 010 (Default). All other combinations are not defined.
	[4:0]	KTON_B	**On-time (t_{ON}) K-Factor setting for rail B.** **When reg. addr 0x67[4] = 0:** KTON = 0.3 + [3:0] × 0.1 **When reg. addr 0x67[4] = 1:** KTON = 1.2 + [3:0] × 0.1 Ex. [4:0] = 00000: KTON = 0.3, [4:0] = 00101: KTON = 0.8, [4:0] = 01111: KTON = 1.8, [4:0] = 10000: KTON = 1.2, [4:0] = 10101: KTON = 1.7, [4:0] = 11111: KTON = 2.7.

Register Address	Bits	Register Name	Description
0x68	[7:5]	ANTI-OVS_B	**Anti-Overshoot threshold setting with load-line for rail B.** [7:5] = 000: 90mV, [7:5] = 100: 300mV, [7:5] = 001: 120mV, [7:5] = 101: 360mV, [7:5] = 010: 180mV, [7:5] = 110: 420mV, [7:5] = 011: 240mV, [7:5] = 111: Disable.
	[4:0]	VOTF_LIFT_B	**Output compensation setting for VOTF (Voltage On-the-Fly) for rail B.** **When VOTF_LIFT_B[4] = 1** [3:0] = 0000: disable, [3:0] = 1000: 9μA, [3:0] = 0001: 2μA, [3:0] = 1001: 10μA, [3:0] = 0010: 3μA, [3:0] = 1010: 12μA, [3:0] = 0011: 4μA, [3:0] = 1011: 14μA, [3:0] = 0100: 5μA, [3:0] = 1100: 16μA, [3:0] = 0101: 6μA, [3:0] = 1101: 18μA, [3:0] = 0110: 7μA, [3:0] = 1110: 20μA, [3:0] = 0111: 8μA, [3:0] = 1111: 24μA. **When VOTF_LIFT_B[4] = 0** [3:0] = 0000: disable, [3:0] = 1000: 18μA, [3:0] = 0001: 4μA, [3:0] = 1001: 20μA, [3:0] = 0010: 6μA, [3:0] = 1010: 24μA, [3:0] = 0011: 8μA, [3:0] = 1011: 28μA, [3:0] = 0100: 10μA, [3:0] = 1100: 32μA, [3:0] = 0101: 12μA, [3:0] = 1101: 36μA, [3:0] = 0110: 14μA, [3:0] = 1110: 40μA, [3:0] = 0111: 16μA, [3:0] = 1111: 48μA.
0x69	[7:4]	LPF_LIMIT_MUTI_PH_B	**High frequency ACLL compensation setting with multi-phase operation and load-line for rail B.** LPF_LIMIT_MUTI_PH = 60mV + [7:4] × 20mV Ex. [7:4] = 0000: LPF_LIMIT_MUTI_PH = 60mV, [7:4] = 0010: LPF_LIMIT_MUTI_PH = 100mV, [7:4] = 1111: LPF_LIMIT_MUTI_PH = 360mV.
	[3:0]	LPF_LIMIT_SINGLE_PH_B	**High frequency ACLL compensation setting with single phase operation and load-line for rail B.** LPF_LIMIT_SINGLE_PH = 30mV + [7:4] × 10mV Ex. [3:0] = 0000: LPF_LIMIT_SINGLE_PH = 30mV, [3:0] = 0010: LPF_LIMIT_SINGLE_PH = 50mV, [3:0] = 1111: LPF_LIMIT_SINGLE_PH = 180mV.
0x6A	[7:5]	FIXED&ABS_QR_WD_B	**Setting width of Fixed-QR and ABS_QR with multi-phase operation for rail B.** [7:5] = 000: 0.50 × t_{ON}, [7:5] = 100: 1.50 × t_{ON}, [7:5] = 001: 0.75 × t_{ON}, [7:5] = 101: 1.75 × t_{ON}, [7:5] = 010: 1.00 × t_{ON}, [7:5] = 110: 2.00 × t_{ON}, [7:5] = 011: 1.25 × t_{ON}, [7:5] = 111: 2.25 × t_{ON}
	[4:0]	QR_TH_B	**Setting QR triggering level with multi-phase operation for rail B.** QR_TH = 240mV + [4:0] x 80mV Ex. [4:0] = 00000: QR_TH = 240mV, [4:0] = 00001: QR_TH = 320mV, [4:0] = 01000: QR_TH = 880mV, [4:0] = 01111: QR_TH = 1440mV, [4:0] = 11111: QR_TH = Disable.

Register Address	Bits	Register Name	Description
0x6B	[7:5]	FIXED_QR_WD_1PH_B	**Setting width of Fixed-QR with single phase operation for rail B.** [7:5] = 000: 0.50 × tON, [7:5] = 001: 0.75 × tON, [7:5] = 010: 1.00 × tON, [7:5] = 011: 1.25 × tON, [7:5] = 100: 1.50 × tON, [7:5] = 101: 1.75 × tON, [7:5] = 110: 2.00 × tON, [7:5] = 111: 2.25 × tON.
	[4:0]	QR_TH_1PH_B	**Setting QR triggering level with single phase operation for rail B.** QR_TH_1PH_B = 40mV + [4:0] x 40mV Ex. [4:0] = 00000: QR_TH_1PH_B = 40mV, [4:0] = 00001: QR_TH_1PH_B = 80mV, [4:0] = 01000: QR_TH_1PH_B = 360mV, [4:0] = 01111: QR_TH_1PH_B = 640mV, [4:0] = 11111: QR_TH_1PH_B = Disable.
0x6C	[7:5]	AR_TH_1PH_B	**Setting adaptive ramp threshold with single phase operation for rail B.** [7:5] = 000: 175mV [7:5] = 001: 150mV [7:5] = 010: 125mV [7:5] = 011: Disable [7:5] = 100: 275mV [7:5] = 101: 225mV [7:5] = 110: 200mV [7:5] = 111: Disable
	[4]	EN_EXTD_TON_B	**Enable tON Extend function for rail B.** [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	EXTD_TON_TH_B	**Setting the threshold to extend tON for rail B.** [3:2] = 00: 150mV, [3:2] = 01: 200mV, [3:2] = 10: 250mV, [3:2] = 11: 300mV.
	[1:0]	EXTD_WD_MAX_B	**Extend max tON setting for rail B.** [1:0] = 00: 1.625 × tON, [1:0] = 01: 1.500 × tON, [1:0] = 10: 1.375 × tON, [1:0] = 11: 1.250 × tON.
0x6D	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 0Ch (Default). All other combinations are not defined.
0x6E	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 00h (Default). All other combinations are not defined.
0x6F	[7:0]	RESERVED	**Reserved bit(s).** [7:0] = 8Ch (Default). All other combinations are not defined.

Register Address	Bits	Register Name	Description
0x70	[7:6]	MIN_TOFF_B	**PWM minimum off-time setting for rail B.** [7:6] = 00: 300ns, [7:6] = 01: 200ns, [7:6] = 10: 120ns, [7:6] = 11: 50ns.
	[5]	QR_SEL_B	**Select QR type with multi-phase operation and load-line for rail B.** [5] = 0: Fixed-QR, [5] = 1: Adaptive-QR.
	[4]	QR_SEL_1PH_B	**Select QR type with single phase operation and load-line for rail B.** [4] = 0: Fixed-QR, [4] = 1: Adaptive-QR.
	[3:0]	RESERVED	**Reserved bit(s).** [3:0] = 1110 (Default). All other combinations are not defined.
0x71	[7]	EAGM_GAIN_B	**Setting transconductance gain of error amplifier for rail B.** [7] = 0: EAGM_GAIN = 2/3, [7] = 1: EAGM_GAIN = 1.
	[6:4]	SLL_RATIO_B	**Short-term voltage target ration during AC transient for rail B.** Short-term voltage target = VID − ΔIcc × RLL × SLL_RATIO [6:4] = 000: 100%, [6:4] = 100: 75%, [6:4] = 001: 95%, [6:4] = 101: 65%, [6:4] = 010: 90%, [6:4] = 110: 55%, [6:4] = 011: 85%, [6:4] = 111: 50%.
	[3:2]	RESERVED	**Reserved bit(s).** [3:2] = 00 (Default). All other combinations are not defined.
	[1]	TSEN_SEL_B	**Temperature source selection for rail B.** [1] = 0: External NTC thermistor (NTC is 100kΩ/Beta = 4250), [1] = 1: Integrated power stage temperature sensor. V_{TSEN} voltage represents temperature information at 8mV/°C + 0.6V.
	[0]	RESERVED	**Reserved bit(s).** [0] = 0 (Default). All other combinations are not defined.
0x72	[7]	RESERVED	**Reserved bit(s).** [7] = 0 (Default). All other combinations are not defined.
	[6]	QR_TRIGGER_SEL	**Setting trigger mechanism of QR for rail B.** [6] = 0: Absolute(ABSQR) with zero load-line, [6] = 1: Differential(AQR & Fixed-QR) with load-line.
	[5:3]	ABSOVS_TH_B	**Absolute Anti-OVS threshold setting with zero load-line for rail B.** [5:3] = 000: Disabled, [5:3] = 100: 35mV, [5:3] = 001: 20mV, [5:3] = 101: 40mV, [5:3] = 010: 25mV, [5:3] = 110: 45mV, [5:3] = 011: 30mV, [5:3] = 111: 50mV.
	[2:0]	ABSQR_TH_B	**Absolute QR threshold setting with zero load-line for rail B.** [2:0] = 000: Disabled, [2:0] = 100: 35mV, [2:0] = 001: 20mV, [2:0] = 101: 40mV, [2:0] = 010: 25mV, [2:0] = 110: 45mV, [2:0] = 011: 30mV, [2:0] = 111: 50mV.

Register Address	Bits	Register Name	Description
0x80	[7:0]	SPM_HYS_2PH_B	**Set Smart Phase Management (SPM) current hysteresis with 2-phase down to 1 phase in PSI7 for rail B.** 1LSB = I_OUT_SCALE/192A When I_OUT_SCALE = Scale 2, LSB = 0.333A, [7:0] = 00h: SPM_HYS = 0A, [7:0] = 12h: SPM_HYS = 5.994A, [7:0] = C0h: SPM_HYS = 63.9375A.
0x83	[7:0]	SPM_TH_2PH_B	**Set Smart Phase Management (SPM) current threshold with 1-phase up to 2-phase in PSI7 for rail B.** Please refer to SPM_HYS_2PH_B for detailed description.
0x8A	[7:0]	IOUT_CAL_OFFSET_B	**IOUT telemetry offset for rail B.** [7]: sign bit, as part of two's complement, [6:0]: 1LSB = I_OUT_SCALE/1023 A Ex. [7:0] = 00h: IOUT_CAL_OFFSET = 0, [7:0] = 01h: IOUT_CAL_OFFSET = +1 LSB, [7:0] = 7Fh: IOUT_CAL_OFFSET = +127 LSB, [7:0] = FFh: IOUT_CAL_OFFSET = -1 LSB, [7:0] = 80h: IOUT_CAL_OFFSET = -128 LSB,
0x8B	[7:0]	IOUT_CAL_GAIN_B	**IOUT telemetry gain for rail B.** LSB = 2^(-9), Telemetry = $IMON_{ADC} \times$ IOUT_CAL_GAIN + IOUT_CAL_OFFSET [7:0] = 00h: IOUT_CAL_GAIN = 75%, [7:0] = 80h: IOUT_CAL_GAIN = 100%, [7:0] = FFh: IOUT_CAL_GAIN =124.8%.

Register Address	Bits	Register Name	Description
0x90	[7:5]	SVI3_20h_DECAY_CONDITIONS_B	Please refer to SVI3 specification.
	[4]	SVI3_20h_DOWN_SLEW_RATE_B	
	[3:0]	SVI3_20h_UP_SLEW_RATE_B	**Slew rate for positive VID change for rail B.** SVI3 register UP_SLEW_RATE_20h[3:0]. Slew rate = 90h[3:0] x 2.5 + 2.5 mV/μs
0x91	[7:5]	RESERVED	**Reserved bit(s).** [7:5] = 000 (Default). All other combinations are not defined.
	[4:0]	SVI3_21h_LL_ADJUST_B	Please refer to SVI3 specification.
0x92	[7:0]	SVI3_22h_VOUT_OFFSET_B	**Voltage offset applied to VID, VID_MIN, VID_MAX, OVP_THRESH and UVP_THRESH for rail B.** SVI3 register VOUT_OFFSET_20h[7:0]. [7:0] = 00h: Disabled (no offset) Offset = 92h[7:0] x 20 - 250mV
0x93	[7:0]	SVI3_23h_VID_MAX_B	Please refer to SVI3 specification.
0x94	[7:0]	SVI3_24h_VID_MIN_B	Please refer to SVI3 specification.
0x95	[7:0]	SVI3_25h_TEN_BIT_TEL_EN_B	Please refer to SVI3 specification.
0x96	[7:0]	SVI3_26h_SIXTEEN_BIT_TEL_EN_B	Please refer to SVI3 specification.
0x97	[7:0]	SVI3_27h_OCP_THRESH_B	**Overcurrent protection threshold level for rail B.** SVI3 register OCP_THRESH_20h[7:0]. [7:0] = 00h: Disabled (no OCP protection) OCP Threshold = 97h[7:0] x 4 x MAX_CURRENT/512A Note: MAX_CURRENT = 3FFh of selected current scale.
0x98	[7:0]	SVI3_28h_OCP_WARN_THRESH_B	**Overcurrent warning threshold level for rail B.** SVI3 register OCP_WARN_THRESH_28h[7:0]. [7:0] = 00h: Disabled OCP Threshold = 98h[7:0] x 4 x MAX_CURRENT/512A Note: MAX_CURRENT = 3FFh of selected current scale.
0x99	[7:3]	SVI3_28h_OCP_WARN_MIN_PULSE_B	**Minimum asserted pulse width of OCP_WARN signal for rail B.** SVI3 register OCP_WARN_MIN_PULSE_28h[7:3]. Minimum pulse = 99h[7:3] x 500ns
	[2:0]	SVI3_29h_OCP_FAULT_DELAY_B	**Continuous time that current must exceed OCP_THRESH before triggering fault for rail B.** SVI3 register OCP_FAULT_DELAY_29h[2:0]. [2:0] = 000: Instantaneous fault Fault delay = 99h[2:0] x 5μs.
0x9A	[7:0]	SVI3_2Ah_VRHOT_THRESH_B	Please refer to SVI3 specification.
0x9B	[7:0]	SVI3_2Bh_OTP_THRESH_B	Please refer to SVI3 specification.
0x9C	[7]	SVI3_2Ch_OVP_REF_B	Please refer to SVI3 specification.
	[6:4]	SVI3_2Ch OVP_DELTA_B	
	[3]	SVI3_2Ch UVP_REF_B	
	[2:0]	SVI3_2Ch UVP_DELTA_B	
0x9D	[7:4]	SVI3_2Dh_PHASE_SHED_1_B	Please refer to SVI3 specification.
	[3:0]	SVI3_2Dh_PHASE_SHED_2_B	

Table 3. Functions that Do Not Support On-line Tuning

Register Address	Function	Support On-line Tuning
00h[1:0]	TARGET_SEQ	No
01h[2:0]	P_SYS_SCALE	No
20h[7:4], 60h[7:4]	VID_DEFAULT_VOLTAGE_A/B	No
24h[6:4], 64h[6:4]	SSOCP_RATIO_A/B	No
24h[2:0], 64h[2:0]	I_OUT_SCALE_A/B	No
25h[3], 65h[3]	EN_0LL_A/B	No
25h[2:0], 65h[2:0]	AI_GAIN_A/B	No
31h[7], 71h[7]	EAGM_GAIN_A/B	No
31h[1], 71h[1]	TSEN_SEL_A/B	No
50h[3:0], 90h[3:0]	UP_SLEW_RATE_A/B	No
52h[7:0], 92h[7:0]	SVI3_22h_VOUT_OFFSET_A/B	No
57h[7:0], 97h[7:0]	SVI3_27h_OCP_THRESH_A/B	No
58h[7:0], 98h[7:0]	SVI3_28h_OCP_WARN_THRESH_A/B	No
59h[7:3], 99h[7:3]	SVI3_29h_OCP_WARN_MIN_PULSE_A/B	No
59h[2:0], 99h[2:0]	SVI3_29h_OCP_FAULT_DELAY_A/B	No

Table 4. SVI3 Registers for SVI3 Protocol

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
01h	[7:0]	SVI3_VERSION	R	01h	Rev. 1
02h	[7:5]	TYPE_ID	R	000b	Type 1
	[4:0]	MGF_ID	R	00100b	04h = Richtek
03h	[7:0]	MODEL_ID	R	00h	
04h	[7:0]	TEN_BIT_TEL_AVAIL	R	47h	System Power, Temp 1, Output voltage and Output current of 10-bit telemetry are available.
05h	[7:0]	SIXTEEN_BIT_TEL_AVAIL	R	00h	Reserved
06h	[7]	CRC_ENABLED	R	1b	CRC is enabled
	[4:2]	PSI	R	000b	PSI0. Indicates the PSI state of the target.
	[0]	VID[8]	R	Platform	Indicates the MSB of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
07h	[7:0]	VID[7:0]	R	Platform	Indicates the 8 LSBs of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
08h	[5:4]	DEFAULT_SLEW_RATE	R	Platform	NVM configurable, based on platform
	[3:0]	VID_DEFAULT_VOLTAGE	R	Platform	NVM configurable, based on platform
09h	[7:6]	V_IN_SCALE	R	00b	Not support
	[5:3]	I_OUT_SCALE	R	Platform	NVM configurable, based on platform
	[2:0]	I_IN_SCALE	R	Platform	Not support
0Ah	[7:0]	MAX_VOUT_SUPPORTED	R	8Ch	MAX_VOUT_SUPPORTED = 2.8V
0Bh	[7:0]	MIN_VOUT_SUPPORTED	R	32h	MIN_VOUT_SUPPORTED = 0.25V
0Ch	[2:0]	P_SYS_SCALE	R	Platform	NVM configurable, based on platform
10h	[7:0]	FAULT_STATUS	R	Current status	
11h	[7:0]	NACK_STATUS	R	Current status	
20h	[7:5]	DECAY_CONDITIONS	R/W	000b	Down voltage decay disabled
	[4]	DOWN_SLEW_RATE	R/W	0b	Negative slew rate = positive slew rate
	[3:0]	UP_SLEW_RATE	R/W	Platform	Copied from DEFAULT_SLEW_RATE
21h	[4:0]	LL_ADJUST	R/W	01010b	100%
22h	[7:0]	VOUT_OFFSET	R/W	00h	No offset
23h	[7:0]	VID_MAX	R/W	00h	Disabled
24h	[7:0]	VID_MIN	R/W	00h	Disabled
25h	[7:0]	TEN_BIT_TEL_EN	R/W	00h	Disabled
26h	[7:0]	SIXTEEN_BIT_TEL_EN	R/W	00h	Reserved
27h	[7:0]	OCP_THRESH	R/W	Platform	NVM configurable, based on platform
28h	[7:0]	OCP_WARN_THRESH	R/W	Platform	NVM configurable, based on platform

Addr (Hex)	Bits	Register Name	Type	Default Value	Note
29h	[7:3]	OCP_WARN_MIN_PULSE	R/W	Platform	NVM configurable, based on platform
	[2:0]	OCP_FAULT_DELAY	R/W	Platform	NVM configurable, based on platform
2Ah	[7:0]	VRHOT_THRESH	R/W	8Ch	100°C
2Bh	[7:0]	OTP_THRESH	R/W	A5h	125°C
2Ch	[7]	OVP_REF	R/W	0b	VID
	[6:4]	OVP_DELTA	R/W	110b	350mV
	[3]	UVP_REF	R/W	0b	VID
	[2:0]	UVP_DELTA	R/W	110b	350mV
2Dh	[7:4]	PHASE_SHED_1	R/W	0001b	1-phase when target is in PSI1
	[3:0]	PHASE_SHED_2	R/W	0001b	1-phase when target is in PSI2
40h	[7:0]	DEBUG_ENABLED	R/W	00h	
41h	[7:0]	DEBUG_TEMP1_OVERRIDE	R/W	00h	
42h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
43h	[7:0]	DEBUG_VOUT_OVERRIDE	R/W	00h	
44h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
45h	[7:0]	DEBUG_IOUT_OVERRIDE	R/W	00h	
46h	[2:0]	DEBUG_OUTPUT_OVERRIDE	R/W	000b	
50h	[7:0]	GEN_PURPOSE_0	R/W	00b	
51h	[7:0]	GEN_PURPOSE_1	R/W	00b	
52h	[7:0]	GEN_PURPOSE_2	R/W	00b	
53h	[7:0]	GEN_PURPOSE_3	R/W	00b	
54h	[7:0]	GEN_PURPOSE_4	R/W	00b	
55h	[7:0]	GEN_PURPOSE_5	R/W	00b	
56h	[7:0]	GEN_PURPOSE_6	R/W	00b	
57h	[7:0]	GEN_PURPOSE_7	R/W	00b	

Table 5. SVI3 Type 1 Target VID Table

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
000000000	000	OFF	000100000	020	0.405	001000000	040	0.565	001100000	060	0.725
000000001	001	0.250	000100001	021	0.410	001000001	041	0.570	001100001	061	0.730
000000010	002	0.255	000100010	022	0.415	001000010	042	0.575	001100010	062	0.735
000000011	003	0.260	000100011	023	0.420	001000011	043	0.580	001100011	063	0.740
000000100	004	0.265	000100100	024	0.425	001000100	044	0.585	001100100	064	0.745
000000101	005	0.270	000100101	025	0.430	001000101	045	0.590	001100101	065	0.750
000000110	006	0.275	000100110	026	0.435	001000110	046	0.595	001100110	066	0.755
000000111	007	0.280	000100111	027	0.440	001000111	047	0.600	001100111	067	0.760
000001000	008	0.285	000101000	028	0.445	001001000	048	0.605	001101000	068	0.765
000001001	009	0.290	000101001	029	0.450	001001001	049	0.610	001101001	069	0.770
000001010	00A	0.295	000101010	02A	0.455	001001010	04A	0.615	001101010	06A	0.775
000001011	00B	0.300	000101011	02B	0.460	001001011	04B	0.620	001101011	06B	0.780
000001100	00C	0.305	000101100	02C	0.465	001001100	04C	0.625	001101100	06C	0.785
000001101	00D	0.310	000101101	02D	0.470	001001101	04D	0.630	001101101	06D	0.790
000001110	00E	0.315	000101110	02E	0.475	001001110	04E	0.635	001101110	06E	0.795
000001111	00F	0.320	000101111	02F	0.480	001001111	04F	0.640	001101111	06F	0.800
000010000	010	0.325	000110000	030	0.485	001010000	050	0.645	001110000	070	0.805
000010001	011	0.330	000110001	031	0.490	001010001	051	0.650	001110001	071	0.810
000010010	012	0.335	000110010	032	0.495	001010010	052	0.655	001110010	072	0.815
000010011	013	0.340	000110011	033	0.500	001010011	053	0.660	001110011	073	0.820
000010100	014	0.345	000110100	034	0.505	001010100	054	0.665	001110100	074	0.825
000010101	015	0.350	000110101	035	0.510	001010101	055	0.670	001110101	075	0.830
000010110	016	0.355	000110110	036	0.515	001010110	056	0.675	001110110	076	0.835
000010111	017	0.360	000110111	037	0.520	001010111	057	0.680	001110111	077	0.840
000011000	018	0.365	000111000	038	0.525	001011000	058	0.685	001111000	078	0.845
000011001	019	0.370	000111001	039	0.530	001011001	059	0.690	001111001	079	0.850
000011010	01A	0.375	000111010	03A	0.535	001011010	05A	0.695	001111010	07A	0.855
000011011	01B	0.380	000111011	03B	0.540	001011011	05B	0.700	001111011	07B	0.860
000011100	01C	0.385	000111100	03C	0.545	001011100	05C	0.705	001111100	07C	0.865
000011101	01D	0.390	000111101	03D	0.550	001011101	05D	0.710	001111101	07D	0.870
000011110	01E	0.395	000111110	03E	0.555	001011110	05E	0.715	001111110	07E	0.875
000011111	01F	0.400	000111111	03F	0.560	001011111	05F	0.720	001111111	07F	0.880

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SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
010000000	080	0.885	010100000	0A0	1.045	011000000	0C0	1.205	011100000	0E0	1.365
010000001	081	0.890	010100001	0A1	1.050	011000001	0C1	1.210	011100001	0E1	1.370
010000010	082	0.895	010100010	0A2	1.055	011000010	0C2	1.215	011100010	0E2	1.375
010000011	083	0.900	010100011	0A3	1.060	011000011	0C3	1.220	011100011	0E3	1.380
010000100	084	0.905	010100100	0A4	1.065	011000100	0C4	1.225	011100100	0E4	1.385
010000101	085	0.910	010100101	0A5	1.070	011000101	0C5	1.230	011100101	0E5	1.390
010000110	086	0.915	010100110	0A6	1.075	011000110	0C6	1.235	011100110	0E6	1.395
010000111	087	0.920	010100111	0A7	1.080	011000111	0C7	1.240	011100111	0E7	1.400
010001000	088	0.925	010101000	0A8	1.085	011001000	0C8	1.245	011101000	0E8	1.405
010001001	089	0.930	010101001	0A9	1.090	011001001	0C9	1.250	011101001	0E9	1.410
010001010	08A	0.935	010101010	0AA	1.095	011001010	0CA	1.255	011101010	0EA	1.415
010001011	08B	0.940	010101011	0AB	1.100	011001011	0CB	1.260	011101011	0EB	1.420
010001100	08C	0.945	010101100	0AC	1.105	011001100	0CC	1.265	011101100	0EC	1.425
010001101	08D	0.950	010101101	0AD	1.110	011001101	0CD	1.270	011101101	0ED	1.430
010001110	08E	0.955	010101110	0AE	1.115	011001110	0CE	1.275	011101110	0EE	1.435
010001111	08F	0.960	010101111	0AF	1.120	011001111	0CF	1.280	011101111	0EF	1.440
010010000	090	0.965	010110000	0B0	1.125	011010000	0D0	1.285	011110000	0F0	1.445
010010001	091	0.970	010110001	0B1	1.130	011010001	0D1	1.290	011110001	0F1	1.450
010010010	092	0.975	010110010	0B2	1.135	011010010	0D2	1.295	011110010	0F2	1.455
010010011	093	0.980	010110011	0B3	1.140	011010011	0D3	1.300	011110011	0F3	1.460
010010100	094	0.985	010110100	0B4	1.145	011010100	0D4	1.305	011110100	0F4	1.465
010010101	095	0.990	010110101	0B5	1.150	011010101	0D5	1.310	011110101	0F5	1.470
010010110	096	0.995	010110110	0B6	1.155	011010110	0D6	1.315	011110110	0F6	1.475
010010111	097	1.000	010110111	0B7	1.160	011010111	0D7	1.320	011110111	0F7	1.480
010011000	098	1.005	010111000	0B8	1.165	011011000	0D8	1.325	011111000	0F8	1.485
010011001	099	1.010	010111001	0B9	1.170	011011001	0D9	1.330	011111001	0F9	1.490
010011010	09A	1.015	010111010	0BA	1.175	011011010	0DA	1.335	011111010	0FA	1.495
010011011	09B	1.020	010111011	0BB	1.180	011011011	0DB	1.340	011111011	0FB	1.500
010011100	09C	1.025	010111100	0BC	1.185	011011100	0DC	1.345	011111100	0FC	1.505
010011101	09D	1.030	010111101	0BD	1.190	011011101	0DD	1.350	011111101	0FD	1.510
010011110	09E	1.035	010111110	0BE	1.195	011011110	0DE	1.355	011111110	0FE	1.515
010011111	09F	1.040	010111111	0BF	1.200	011011111	0DF	1.360	011111111	0FF	1.520

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SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
100000000	100	1.525	100100000	120	1.685	101000000	140	1.845	101100000	160	2.005
100000001	101	1.530	100100001	121	1.690	101000001	141	1.850	101100001	161	2.010
100000010	102	1.535	100100010	122	1.695	101000010	142	1.855	101100010	162	2.015
100000011	103	1.540	100100011	123	1.700	101000011	143	1.860	101100011	163	2.020
100000100	104	1.545	100100100	124	1.705	101000100	144	1.865	101100100	164	2.025
100000101	105	1.550	100100101	125	1.710	101000101	145	1.870	101100101	165	2.030
100000110	106	1.555	100100110	126	1.715	101000110	146	1.875	101100110	166	2.035
100000111	107	1.560	100100111	127	1.720	101000111	147	1.880	101100111	167	2.040
100001000	108	1.565	100101000	128	1.725	101001000	148	1.885	101101000	168	2.045
100001001	109	1.570	100101001	129	1.730	101001001	149	1.890	101101001	169	2.050
100001010	10A	1.575	100101010	12A	1.735	101001010	14A	1.895	101101010	16A	2.055
100001011	10B	1.580	100101011	12B	1.740	101001011	14B	1.900	101101011	16B	2.060
100001100	10C	1.585	100101100	12C	1.745	101001100	14C	1.905	101101100	16C	2.065
100001101	10D	1.590	100101101	12D	1.750	101001101	14D	1.910	101101101	16D	2.070
100001110	10E	1.595	100101110	12E	1.755	101001110	14E	1.915	101101110	16E	2.075
100001111	10F	1.600	100101111	12F	1.760	101001111	14F	1.920	101101111	16F	2.080
100010000	110	1.605	100110000	130	1.765	101010000	150	1.925	101110000	170	2.085
100010001	111	1.610	100110001	131	1.770	101010001	151	1.930	101110001	171	2.090
100010010	112	1.615	100110010	132	1.775	101010010	152	1.935	101110010	172	2.095
100010011	113	1.620	100110011	133	1.780	101010011	153	1.940	101110011	173	2.100
100010100	114	1.625	100110100	134	1.785	101010100	154	1.945	101110100	174	2.105
100010101	115	1.630	100110101	135	1.790	101010101	155	1.950	101110101	175	2.110
100010110	116	1.635	100110110	136	1.795	101010110	156	1.955	101110110	176	2.115
100010111	117	1.640	100110111	137	1.800	101010111	157	1.960	101110111	177	2.120
100011000	118	1.645	100111000	138	1.805	101011000	158	1.965	101111000	178	2.125
100011001	119	1.650	100111001	139	1.810	101011001	159	1.970	101111001	179	2.130
100011010	11A	1.655	100111010	13A	1.815	101011010	15A	1.975	101111010	17A	2.135
100011011	11B	1.660	100111011	13B	1.820	101011011	15B	1.980	101111011	17B	2.140
100011100	11C	1.665	100111100	13C	1.825	101011100	15C	1.985	101111100	17C	2.145
100011101	11D	1.670	100111101	13D	1.830	101011101	15D	1.990	101111101	17D	2.150
100011110	11E	1.675	100111110	13E	1.835	101011110	15E	1.995	101111110	17E	2.155
100011111	11F	1.680	100111111	13F	1.840	101011111	15F	2.000	101111111	17F	2.160

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SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
110000000	180	2.165	110100000	1A0	2.325	111000000	1C0	2.485	111100000	1E0	2.645
110000001	181	2.170	110100001	1A1	2.330	111000001	1C1	2.490	111100001	1E1	2.650
110000010	182	2.175	110100010	1A2	2.335	111000010	1C2	2.495	111100010	1E2	2.655
110000011	183	2.180	110100011	1A3	2.340	111000011	1C3	2.500	111100011	1E3	2.660
110000100	184	2.185	110100100	1A4	2.345	111000100	1C4	2.505	111100100	1E4	2.665
110000101	185	2.190	110100101	1A5	2.350	111000101	1C5	2.510	111100101	1E5	2.670
110000110	186	2.195	110100110	1A6	2.355	111000110	1C6	2.515	111100110	1E6	2.675
110000111	187	2.200	110100111	1A7	2.360	111000111	1C7	2.520	111100111	1E7	2.680
110001000	188	2.205	110101000	1A8	2.365	111001000	1C8	2.525	111101000	1E8	2.685
110001001	189	2.210	110101001	1A9	2.370	111001001	1C9	2.530	111101001	1E9	2.690
110001010	18A	2.215	110101010	1AA	2.375	111001010	1CA	2.535	111101010	1EA	2.695
110001011	18B	2.220	110101011	1AB	2.380	111001011	1CB	2.540	111101011	1EB	2.700
110001100	18C	2.225	110101100	1AC	2.385	111001100	1CC	2.545	111101100	1EC	2.705
110001101	18D	2.230	110101101	1AD	2.390	111001101	1CD	2.550	111101101	1ED	2.710
110001110	18E	2.235	110101110	1AE	2.395	111001110	1CE	2.555	111101110	1EE	2.715
110001111	18F	2.240	110101111	1AF	2.400	111001111	1CF	2.560	111101111	1EF	2.720
110010000	190	2.245	110110000	1B0	2.405	111010000	1D0	2.565	111110000	1F0	2.725
110010001	191	2.250	110110001	1B1	2.410	111010001	1D1	2.570	111110001	1F1	2.730
110010010	192	2.255	110110010	1B2	2.415	111010010	1D2	2.575	111110010	1F2	2.735
110010011	193	2.260	110110011	1B3	2.420	111010011	1D3	2.580	111110011	1F3	2.740
110010100	194	2.265	110110100	1B4	2.425	111010100	1D4	2.585	111110100	1F4	2.745
110010101	195	2.270	110110101	1B5	2.430	111010101	1D5	2.590	111110101	1F5	2.750
110010110	196	2.275	110110110	1B6	2.435	111010110	1D6	2.595	111110110	1F6	2.755
110010111	197	2.280	110110111	1B7	2.440	111010111	1D7	2.600	111110111	1F7	2.760
110011000	198	2.285	110111000	1B8	2.445	111011000	1D8	2.605	111111000	1F8	2.765
110011001	199	2.290	110111001	1B9	2.450	111011001	1D9	2.610	111111001	1F9	2.770
110011010	19A	2.295	110111010	1BA	2.455	111011010	1DA	2.615	111111010	1FA	2.775
110011011	19B	2.300	110111011	1BB	2.460	111011011	1DB	2.620	111111011	1FB	2.780
110011100	19C	2.305	110111100	1BC	2.465	111011100	1DC	2.625	111111100	1FC	2.785
110011101	19D	2.310	110111101	1BD	2.470	111011101	1DD	2.630	111111101	1FD	2.790
110011110	19E	2.315	110111110	1BE	2.475	111011110	1DE	2.635	111111110	1FE	2.795
110011111	19F	2.320	110111111	1BF	2.480	111011111	1DF	2.640	111111111	1FF	2.800

Thermal Monitoring and Indicator

The RT3678BE supports thermal monitoring by external NTC thermistor or integrated power stage temperature sensor, and it can be set by NVM registers TSEN_SEL_31h[1] for Rail A and TSEN_SEL_71h[1] for Rail B.

When external NTC thermistor is used for thermal monitoring, TSEN pin voltage can be represented as:

$$V_{TSEN} = 80\mu A \times (R_1 // R_{NTC} + R_2)$$

The NTC thermistor network for temperature sensing is shown in Figure 4. The NTC thermistor is recommended to be placed around the hottest component of the VR, i.e. MOSFET, and must be routed as differential pair on the same PCB layer.

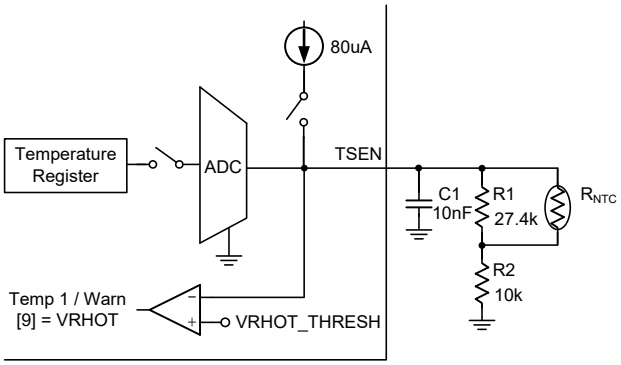


Figure 4. TSEN network with NTC thermistor

The RT3678BE supports the telemetry function for temperature. The device continually digitizes the sensed corresponding channel temperature with TSEN pin, and averages it to reduce measurement noise. Then the current value is stored in the TEMP_RPT (23h) register.

The resistance accuracy of TSEN network is recommended to be less than 1% error. The NTC thermistor is suggested to be 100kΩ with β = 4250 and with accuracy less than 1% error. The NCP15WF104F03RC NTC thermistor from Murata is recommended. When integrated power stage temperature sensor is used for thermal monitoring, the RT3678BE controller senses the temperature reported by TMON pin of integrated power stage. In this application, the relation between VTSEN voltage and the sensed temperature is:

$$Temp.(^{\circ}C) = \frac{V_{TSEN} - 0.6V}{8mV/^{\circ}C}$$

The sensed temperature can be read via SVI3 from the register READ_TEMPERATURE_1 (8Dh), and via I2C from the register TEMP_RPT (23h). The update rate of temperature reporting register is 700μs and the averaging interval is 5.6ms.

System Input Power Monitoring (PSYS)

The RT3678BE provides PSYS function to monitor total system power and reports to the CPU via SVI3 interface.

The PSYS function is illustrated in Figure 5. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the P_{SYS} voltage = 1.6V or 3.2V with maximum I_{PSYS} for 100% system input power. System power telemetry consists of a 10-bit encoding that is mapped to eight user-selectable scales. The user-selectable scales can be set by NVM register P_SYS_SCALE_01h[2:0]. Pulling PSYS pin to VCC and NVM register P_SYS_EN[3] can disable PSYS function.

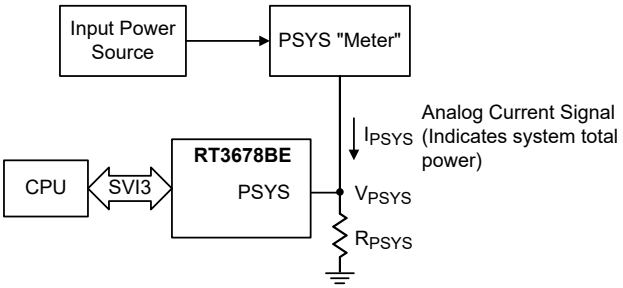


Figure 5. PSYS Function Block Diagram

Zero Load-line and AC-droop

The RT3678BE supports zero load-line applications by setting NVM register EN_0LL_A (25h[3]) for Rail A and EN_0LL_B (65h[3]) for Rail B, and builds in AC-droop feature. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current. The AC-droop can effectively suppress load transient ring-back and control overshoot in zero load-line application. Figure 6 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring-back ΔV2 due to electrical charge integrated in C area.

Figure 7 shows the load transient condition with AC-droop control. When load transient occurs, the controller changes VID to short-term voltage target temporarily.

Short-term voltage target is related to transient loading current ΔICC and can be represented as:

Short-term Voltage Target = VID – ΔICC x RLL x SLL_RATIO

Whether zero load-line is enabled or disabled, the equation of RLL is the same as load-line system. Zero load-line function can be set by NVM register EN_0LL_25h[3] for rail A and EN_0LL_65h[3] for rail B. The detailed application is described in the Load-line Setting section. SLL_RATIO is a ratio of short-term voltage target during AC transient, and it can be set by NVM register SLL_RATIO_A_31h[6:4] for rail A and SLL_RATIO_B_71h[6:4] for rail B. The short-term voltage target returns to VID slowly after a period of time. The short-term voltage target can prevent inductor current from exceeding loading current too much and the ring-back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

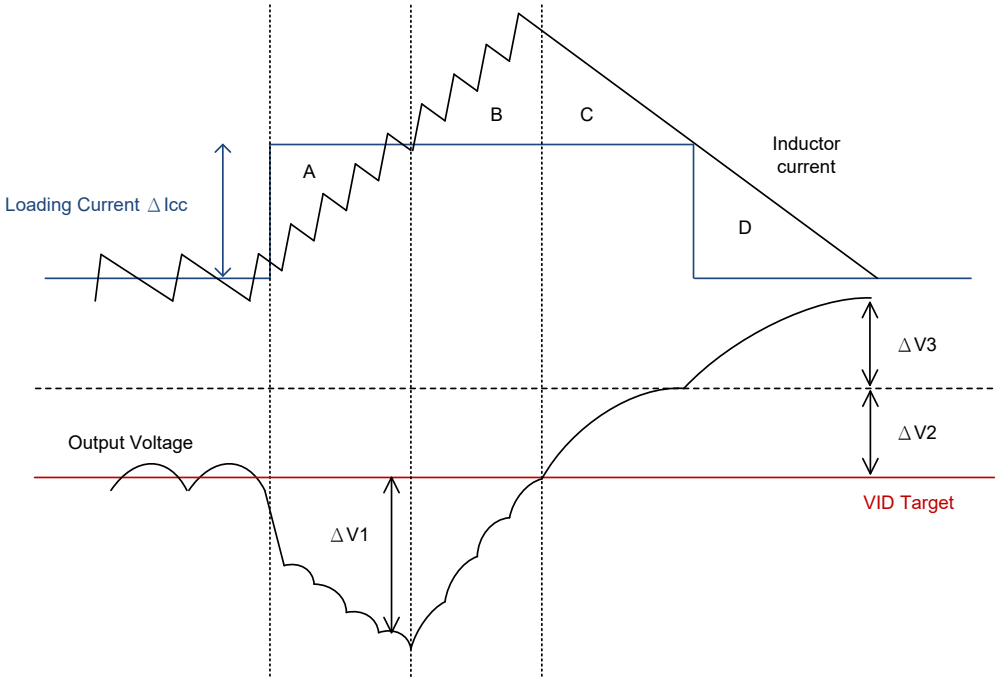


Figure 6. Zero Load-line without AC-droop Control

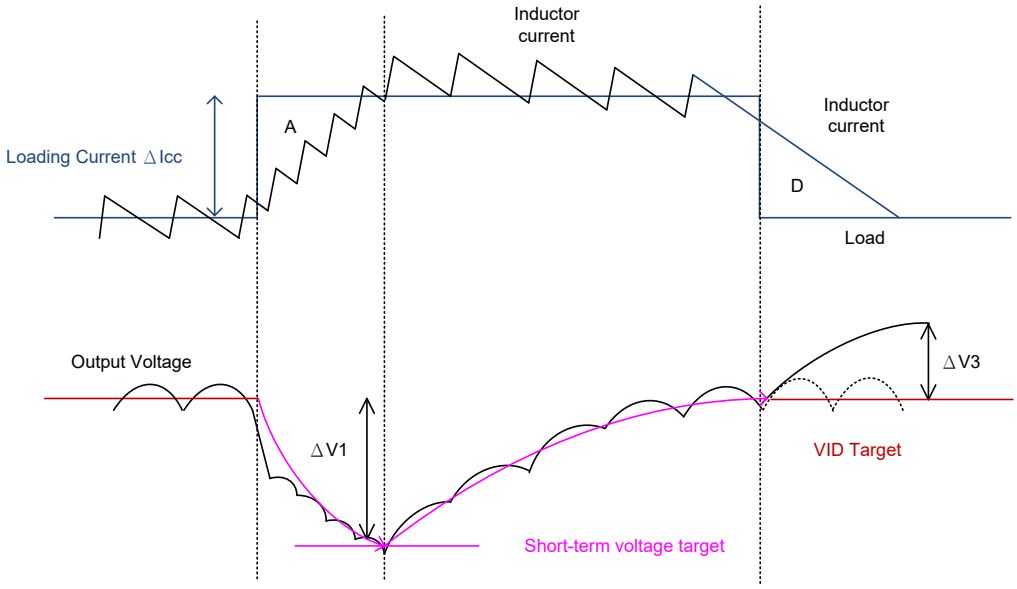


Figure 7. Zero Load-line with AC-droop Control

DCR Current Sense

To achieve higher efficiency, the RT3678BE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 8. An external low-pass filter R_{X1} (R_{X11}+R_{X12}) and C_X reconstruct the current signal. It is necessary to fine-tune R_{X1} (R_{X11}+R_{X12}) and C_X for transient performance and current telemetry. The time constant of R_{X1} x C_X should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS}} = \frac{I_L \times DCR}{R_{CS}}$$

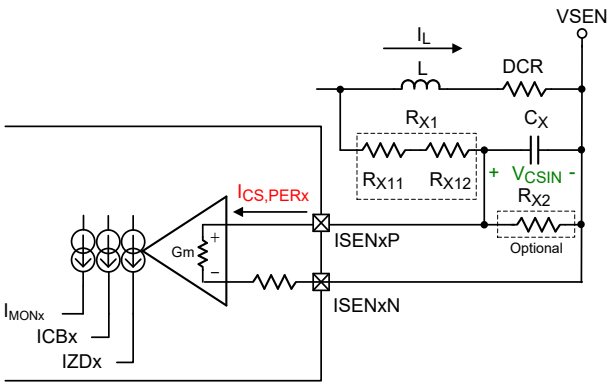


Figure 8. DCR Current Sensing Network of Inductor

Figure 9 shows the waveforms of output voltage according to the time constant of RC network. If R_{X1} x C_X = $\frac{L}{DCR}$, an ideal load transient waveform can be designed. If R_{X1} x C_X > $\frac{L}{DCR}$, VSEN waveform has a sluggish droop during load transient. If R_{X1} x C_X < $\frac{L}{DCR}$, VSEN waveform sags to create an undershoot that might fail the specification and can trigger overcurrent protections (OCP). It is strongly suggested to use two 0603 size resistors connected in series for R_{X1} (R_{X11}+R_{X12}) to enhance the output current telemetry accuracy, and both resistance of R_{X11} and R_{X12} must be the same. The capacitor C_X is suggested to be 0.1μF X7R/0603 to avoid capacitance de-rating at high frequency.

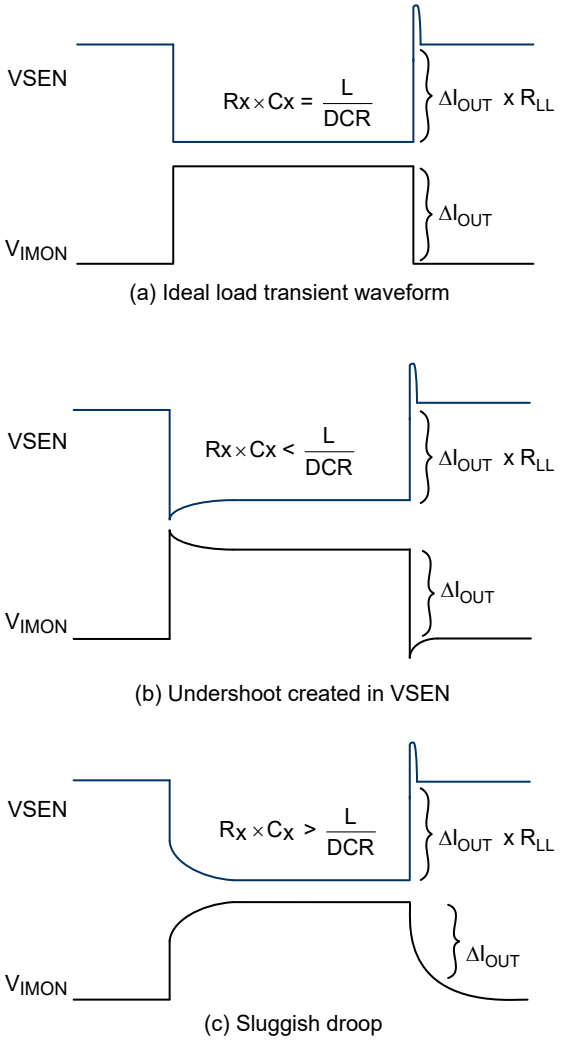


Figure 9. Effects of Different RC Time Constants

R_{X2} in Figure 8 is optional to prevent V_{CSIN} from exceeding the range of current sense amplifier. The time constant of (R_{X1} // R_{X2}) x C_X should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS}} = \frac{I_L \times DCR}{R_{CS}} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero current detection. The mirrored current to IMONx pin is 1.25 times of $I_{CS,PER}$

I_{IMONX} = A_{MIRROR} x $I_{CS,PERx}$, A_{MIRROR} = 1.25

The current sense signal must be routed as differential pair from inductor to the controller on the same PCB layer. Proper differential routing of current sense signal

will provide accurate current telemetry for current balance, load-line regulation and OCP.

The DCR value of inductor increases as the temperature of inductor increases, due to the positive temperature coefficient of the copper windings. To compensate the effect of DCR positive temperature coefficient, conventional current sense method requires an NTC thermistor for each phase current sensing. The RT3678BE adopts a patented total current sense method that requires only one NTC thermistor for thermal compensation. The NTC thermistor is designed within IMON resistor network connected to the IMON pin. It is suggested to place the NTC thermistor close to the inductor of phase 1. The total DCR current sense method is shown in Figure 10. All phase current signals are summed and mirrored to the IMON pin and converted into a voltage signal V_{IMON} by $R_{IMON,EQ}$. The VREF pin provides 0.6V voltage source during normal operation. The relationship between V_{IMON} and inductor current I_{LX} is:

$$V_{IMON} - V_{VREF} = \sum I_{LX} \times \frac{DCR}{1000} \times A_{MIRROR} \times R_{IMON,EQ}$$

$V_{IMON} - V_{VREF}$ is proportional to output current and is used for output current telemetry, load-line control and sum overcurrent protection. $V_{IMON} - V_{VREF}$ is linearly mapped to NVM register I_OUT_SCALE (24h[2:0] for rail A and 64h[2:0] for rail B), which is user selectable. The $R_{IMON,EQ}$ should be designed according to maximum current of I_OUT_SCALE. $V_{IMON} - V_{VREF}$ is 0.4V while sum current equals maximum value of I_OUT_SCALE.

For load-line control, $V_{IMON} - V_{VREF}$ is scaled by NVM register AI_GAIN (25h[2:0] for rail A and 65h[2:0] for rail B). The detailed application is described in the Load-line Setting section.

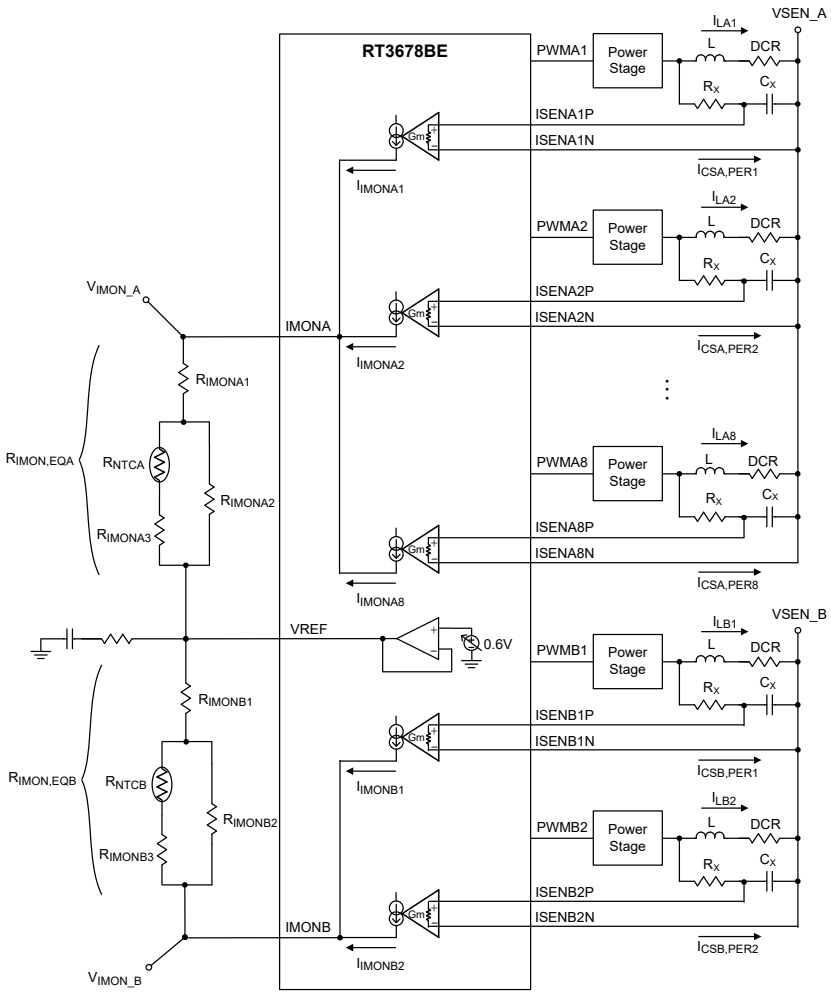


Figure 10. Total DCR Current Sensing

Load-line Setting (R_{LL})

The mechanism of load-line is that the output voltage decreases by an amount proportional to the loading current. The slope between output voltage and loading current is the load-line (R_{LL}) as shown in Figure 11. Figure 12 shows the circuit of voltage loop and current loop for the load-line control. The detailed equation is described as below:

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{CS}} \times \frac{R_{IMON,EQ}}{A_{EAGM}} \times \frac{A_i}{A_V} \times 2.5$$

A_i is the gain of current sense amplifier, and it can be set by NVM register AI_GAIN (25h[2:0] for rail A and 65h[2:0] for rail B). A_{EAGM} is the transconductance ratio of ERROR AMP, and it can be set by NVM register EAGM_GAIN (31h[7] for rail A and 71h[7] for rail B). A_V is the gain of voltage loop compensator, which equals to $\frac{R_{EA2}}{R_{EA1}}$, and is suggested to be 2 to 4.5 for better transient response. Table 6 and 7 show NVM register setting of A_i and A_V.

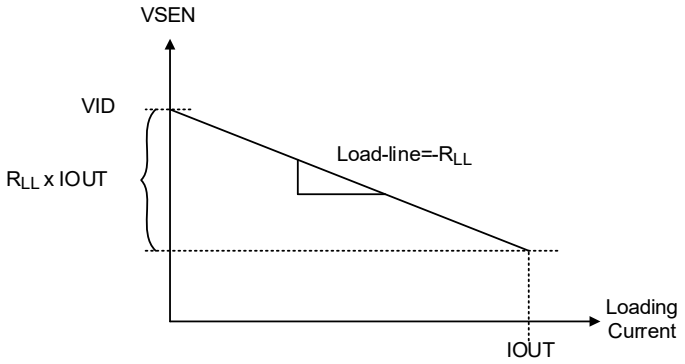


Figure 11. Load-line (Adaptive Voltage Positioning)

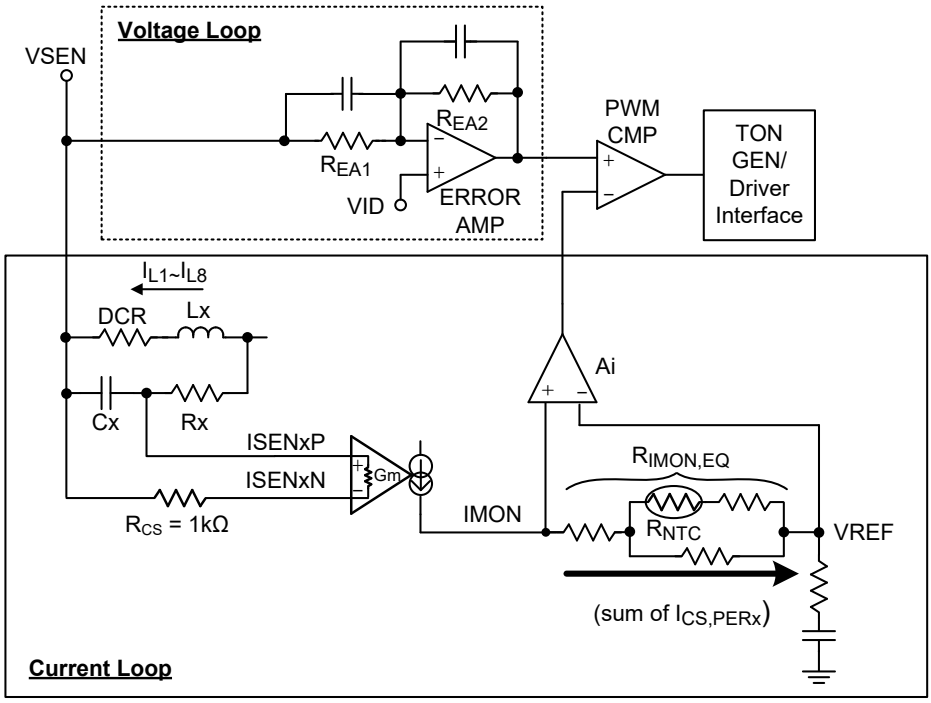


Figure 12. Voltage Loop and Current Loop for Load-line control

Table 6. NVM Configuration of Ai

AI_GAIN_A_25h[2:0] / AI_GAIN_B_65h[2:0]	Current Sense Gain
000	0.25
001	0.5
010	0.75
011	1.00
100	0.125
101	0.375
110	0.625
111	0.875

Table 7. NVM Configuration of AEAGM

EAGM_GAIN_A_31h[7] / EAGM_GAIN_B_71h[7]	A_{EAGM} Gain
0	2/3
1	1

Voltage On-the-Fly (VOTF) Compensation

During VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of VOTF slew rate and output capacitance, as shown in the equation below. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. This extra voltage drop can be seen:

V_{Droop} = VOTF Slew Rate x Output Capacitance x R_{LL}

Where R_{LL} is the load-line slope, mΩ.

This is called droop effect. How the charging current affects VOTF transition is illustrated in Figure 13.

The RT3678BE provides VOTF compensation function as shown in Figure 14. During VOTF, an internal current I_{VOTF_LIFT} sinks from FB pin to generate VOTF compensation, I_{VOTF_LIFT} x R_{EA1}. For different scales of VOTF slew rate, I_{VOTF_LIFT} can be set by NVM register VOTF_LIFT_A_28h[4:0] and VOTF_LIFT_B_68h[4:0]. Compensation magnitude can be adjusted by R_{EA1}. When DAC output reaches the target, inductor current is still high and needs a period of time to settle down to the DC loading current. During the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, VOTF compensation can be less than VOTF Slew Rate x Output Capacitance x R_{LL} (De-rating of capacitance should be considered).

If the output capacitance is too large to be covered by VOTF compensation, adding extra resistor and capacitor in series from FB to GND can also provide similar effect. The ERROR AMP compensation (Resistance and capacitance network among VSEN, FB and COMP) network also affects VOTF behavior. The final setting should be based on actual measurement.

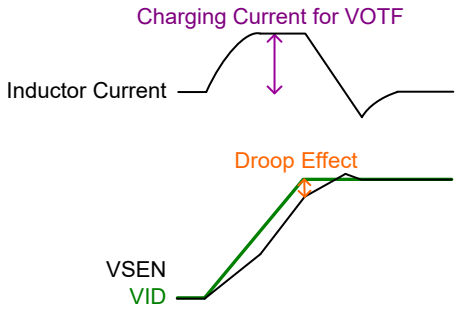


Figure 13. Droop Effect in VOTF Transition

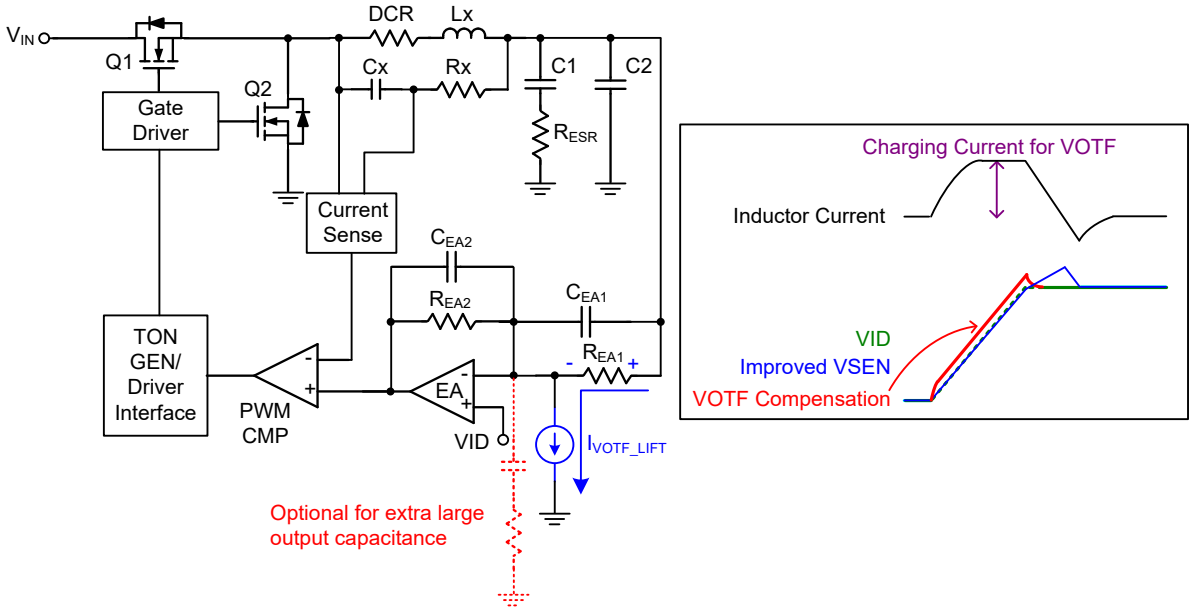


Figure 14. VOTF Compensation

Compensator Design

The compensator of the RT3678BE does not need a complex type III compensator to optimize control loop performance. It can adopt a simple type II compensator (single pole, single zero) in the G-NAVP^{TM} topology to fine-tune ACLL performance. The single pole and single zero compensator is shown in Figure 15. For SVI3 transient specification, it is suggested to adjust compensator according to load transient ring-back level. Refer to the design tool for default compensator values.

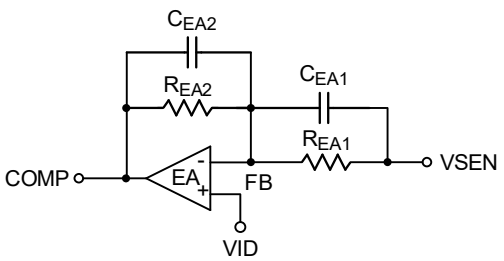


Figure 15. Type II Compensator

Differential Remote Sense

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PCB traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. The related connection is shown in Figure 16. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback. VSEN and RGND must be routed as differential pair all the way from controller to CPU socket without crossing any phase node, gate driver, VIN power delivery path and high-speed signals. They should be well spaced on an internal signal layer between two monolithic ground planes.

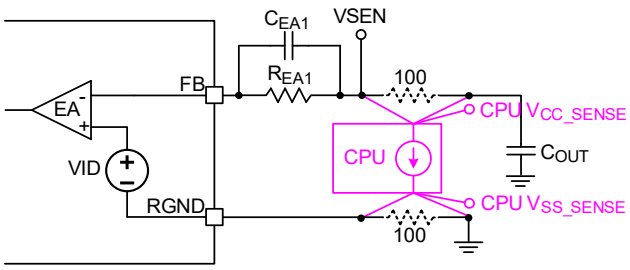


Figure 16. Remote Sensing Circuit

Switching Frequency

The G-NAVP™ (Green Native AVP) topology is a type of current-mode constant on-time control. It generates an adaptive t_{ON} pulse (PWM) based on input voltage for better line regulation. The t_{ON} width is adaptive to VID voltage to achieve constant frequency. The constant switching frequency operation makes thermal estimation and EMI noise reduction easier. The RT3678BE provides a parameter setting of KTON to define t_{ON} width, and KTON can be set by NVM register KTON (27h[4:0] for rail A and 67h[4:0] for rail B). The Table 8 below shows the KTON for t_{ON} width setting. The equations of t_{ON} are listed as below:

$$VID > 0.9V,\ t_{ON} = 2\mu \times \frac{VID}{K_{TON} \times V_{IN}}$$

$$VID \leq 0.9V,\ t_{ON} = 2\mu \times \frac{0.9}{K_{TON} \times V_{IN}}$$

Table 8. NVM Configuration of KTON[4:0]

KTON [4]	KTON
0	KTON = 0.3 + [3:0] x 0.1
1	KTON = 1.2 + [3:0] x 0.1

The switching frequency can be derived from t_{ON} as shown below. The power dissipation in the power stage and driver characteristics are considered.

$$Fsw = \frac{VID + \frac{I_{CC}}{N} \times (DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL})}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}}\right)\right] \times (t_{ON} - t_D + t_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times t_D}$$

VID: VID voltage

VIN: Input voltage

I_{CC}: Loading current

N: Total phase number

$R_{ONHS,max}$: Maximum equivalent high-side $R_{DS(ON)}$

n_{HS}: Number of high-side MOSFETs

$R_{ONLS,max}$: Maximum equivalent low-side $R_{DS(ON)}$

n_{LS}: Number of low-side MOSFETs.

t_D: Sum of the high-side MOSFET delay time and rising time

$t_{ON, VAR}$: On-time variation value

DCR: Inductor DCR

R_{LL}: Load-line setting (Ω)

Quick Response (AQR/Fixed-QR/ABS_QR)

The RT3678BE provides Absolute Quick Response (ABS_QR) and Adaptive Quick Response (AQR)/Fixed Quick Response (Fixed QR) to optimize transient response for zero load-line and load-line system respectively. Table 9 and Table 10 summarizes the settings of quick response in PSI0/PSI3 state.

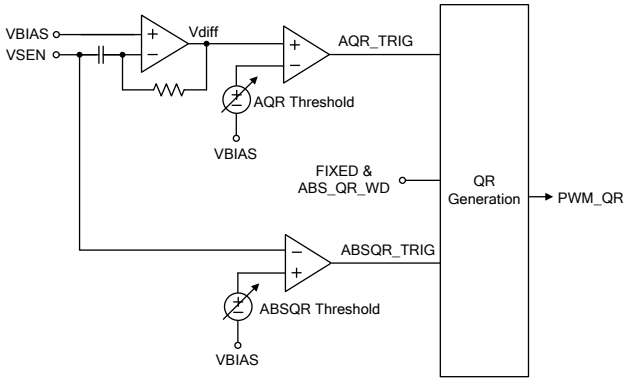


Figure 17. Mechanism of Quick Response

For rail B operating in zero load-line system, the RT3678BE provides Absolute Quick Response (ABS_QR) technique to optimize transient performance and can be set via QR_TRIGGER_SEL (72h[6]). Since the output voltage does not change with loading in zero load-line system, the RT3678BE detects the absolute value of output voltage drop. Figure 18 illustrates the ABS_QR mechanism. When the absolute value of output voltage drops below VID minus ABS_QR threshold, the controller will turn on all PWMs until VSEN climbs up above the threshold. The ABS_QR threshold can be selected via NVM registers ABS_QR_TH_72h[2:0]. The ABS_QR on-time width can be set by FIXED&ABS_QR_WD_6Ah[7:5]. Note that the threshold should be larger than output voltage ripple to avoid triggering ABS_QR mechanism in steady-state.

In load-line system, ABS_QR is not applicable because output voltage decreases as the loading current increases. Instead of ABS_QR, the RT3678BE provides Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR) to optimize transient performance.

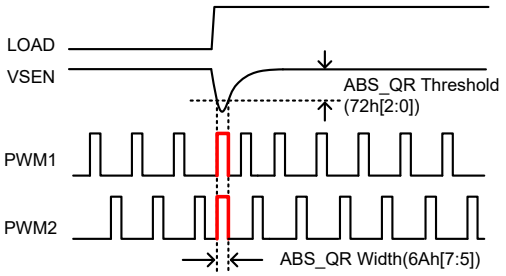


Figure 18. Absolute Quick Response (ABS_QR) in Zero Load-line System (QR_TRIGGER_SEL_72h[6] = 0b: Differential)

Figure 19 and Figure 20 show the mechanisms and differences between AQR and Fixed QR. They can be set by NVM register QR_SEL (30h[5] for rail A and 70h[5] for rail B). In the mechanism of AQR and Fixed-QR, the controller detects the slew rate of output voltage drop. When the slew rate of output voltage drop exceeds the QR threshold, the controller turns on all PWMs until the output derivative drops below QR threshold. Since the current demands in single phase and multi phase are different, the RT3678BE provides each rail two settings of AQR/Fixed QR threshold for multi-phase and single phase operation respectively. For rail A, the QR threshold can be set via NVM registers QR_TH_A (2Ah[4:0]) and QR_TH_1PH_A (2Bh[4:0]); for rail B, the QR threshold can be set via registers QR_TH_B (6Ah[4:0]) and QR_TH_1PH_B (6Bh[4:0]). The t_{ON} width of AQR is adaptive to loading step current. For rail A, the Fixed QR on-time width can be selected via NVM registers FIXED_QR_WD_A (2Ah[6:5]) and FIXED_QR_WD_1PH_A (2Bh[6:5]) for multi-phase and single phase operation respectively. For rail B, the setting of Fixed QR on-time width shares the same register with ABS_QR (FIXED&ABS_QR_WD_6Ah[7:5]). It should be noticed that the threshold of AQR and Fixed QR should be set larger than falling slew rate of output voltage ripple in steady-state and the falling slew rate of overshoot to avoid false triggering. The following equation can initially decide the QR threshold of AQR and Fixed-QR:

$$\text{QR Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$

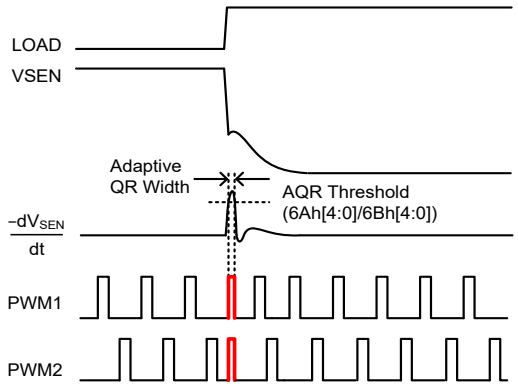


Figure 19. Adaptive Quick Response (AQR)
(QR_TRIGGER_SEL_72h[6] = 1b: Differential)

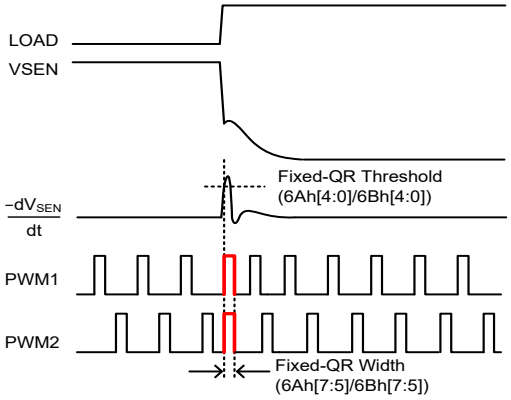


Figure 20. Fixed Quick Response (Fixed-QR)
(QR_TRIGGER_SEL_72h[6] = 1b: Differential)

Table 9. Quick Response in Zero/Non-zero Load-line System

Quick Response	Zero Load-line (EN_0LL = 1b: Enable)	Load-line (EN_0LL = 0b: Disabled)
Adaptive Quick Response (AQR)	Supported	Supported
Fixed Quick Response (Fixed-QR)	Supported	Supported
Absolute Quick Response (ABS_QR)	Supported	Not Supported

Table 10. Summary of Quick Response for Rail A

QR Trigger Mechanism	Differential	
Type	QR_SEL_A_30h[5]/QR_SEL_1PH_A_30h[4]	
	0: Fixed-QR	1: Adaptive-QR
Threshold	QR_TH_A_2A[4:0]/QR_TH_1PH_A_2Bh[4:0]	
QR Width of tON	FIXED_QR_WD_A_2Ah[6:5]/ FIXED_QR_WD_1PH_A_2Bh[6:5]	Adaptive

Table 11. Summary of Quick Response for Rail B

QR Trigger Mechanism	Absolute	Differential	
Trigger Mechanism	QR_TRIGGER_SEL_72h[6] = 0: Absolute(ABS_QR*)	QR_TRIGGER_SEL_72h[6] = 1: Differential(AQR & Fixed-QR)	
Type	QR_SEL_70h[5]	QR_SEL_70h[5]/QR_SEL_1PH_70h[4]	
	0: Fixed-QR	0: Fixed-QR	1: Adaptive-QR
Threshold	ABS_QR_TH_ 72h[2:0]	QR_TH_6Ah[4:0]/ QR_TH_1PH_6Bh[4:0]	
QR Width of tON	FIXED&ABS_QR_ WD_6Ah[7:5]	FIXED&ABS_QR_ WD_6Ah[7:5]	Adaptive

* ABS_QR is only available for rail B with zero load-line system.

Absolute-Overshoot (ABS_OVS)/Anti-Overshoot (ANTI-OVS)

The RT3678BE provides Absolute-Overshoot (ABS_OVS) function and Anti-Overshoot (ANTI-OVS) function to suppress output voltage overshoot for zero load-line and load-line system respectively.

For rail B operating in zero load-line system, the RT3678BE provides Absolute-Overshoot (ABS_OVS) function as shown in Figure 21. Since the output voltage does not change with loading current, the RT3678BE detects the absolute overshoot of output voltage. When output overshoot exceeds ABS_OVS threshold, the controller will force all PWMs in tri-state until zero current is detected or VSEN returns to normal level. The threshold of ABS_OVS can be selected via NVM registers ABSOVS_TH_72h[5:3].

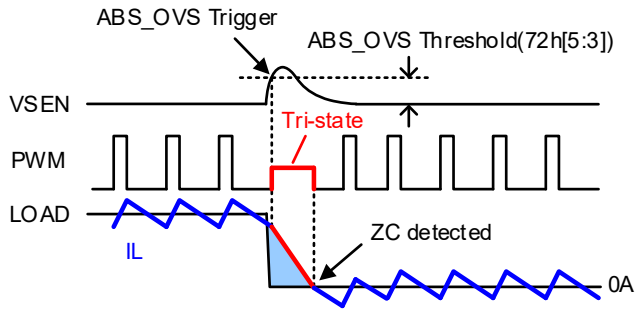


Figure 21. Absolute-Overshoot Function in No Load-Line System

In load-line system, the RT3678BE provides Anti-overshoot (ANTI-OVS) function to suppress output voltage overshoot. The controller detects the internal COMP signal that can vary with voltage loop compensation. The following equation can be used to initially decide the threshold of ANTI-OVS function:

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS Threshold}$$

The final setting should be based on actual Error AMP compensator design and measurement. When output overshoot exceeds the trigger level, the controller will force all PWMs in tri-state until zero current is detected or VSEN returns to normal level. The threshold of ANTI-OVS can be selected via NVM registers ANTI-OVS (28h[7:5] for rail A and 68h[7:5] for rail B).

Overshoot suppression is achieved by turning off both high-side and low-side switches, forcing the inductor current to flow through low-side body diode. The extra forward voltage can accelerate the inductor discharging slope and hence reduce overshoot significantly.

ACLL Performance Enhancement

In single phase configuration, the RT3678BE provides Adaptive Ramp (AR) function to suppress undershoot when load applied. The controller detects internal COMP signal and compares it with steady-state signal. When COMP signal variation exceeds a specified threshold, the controller will force to generate PWM earlier. The threshold of Adaptive Ramp (AR) function can be selected via NVM registers AR_TH_1PH (2Ch[7:5] for rail A and 6Ch[7:5] for rail B). Figure 22 shows UDS behavior in single phase operation. Note that the threshold of AR should be large enough to avoid false triggering in the steady-state. Since the internal COMP signal can vary with ERROR AMP compensator, the final setting should be based on actual Error AMP compensator design and measurement.

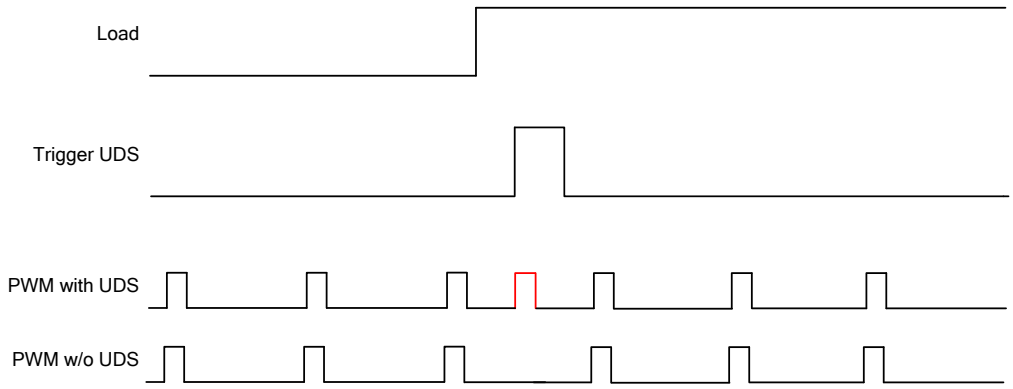


Figure 22. Adaptive Ramp (AR) Function in Single Phase

Smart Phase Management (SPM)

The RT3678BE provides Smart Phase Management (SPM) function to improve light load efficiency for multi-phase operation of each rail. The SPM function can be enabled and disabled via I2C register EN_FORCE_PSI7_12h[1]. As shown in Figure 23, the controller compares the sum current (sensed from VIMON signal) with current threshold SPM_TH_NPH to determine the number of operating N-phase. The threshold of SPM can be set via NVM register SPM_TH_NPH. There is no delay during phase adding. Figure 24 shows the hysteresis of SPM_TH and delay time exit during phase drop. The hysteresis of SPM_TH can be set via NVM register SPM_HYS. When V_{IMON} is lower than (SPM_TH_NPH − SPM_HYS_NPH), the controller goes to (N-1)-phase operation. When the inductor current is lower than zero current detector threshold, the controller automatically enters diode emulation mode (DEM). In addition to the output current comparison, the RT3678BE provides four events to operate in full phase immediately:

(a) During positive VOTF transitions,

(b) During negative VOTF transitions without decay mode,

(c) While the QR functions (AQR/Fixed-QR/ABS_QR) are triggered,

(d) I2C register EN_FORCE_PSI0_12h[0] = 1: Enable.

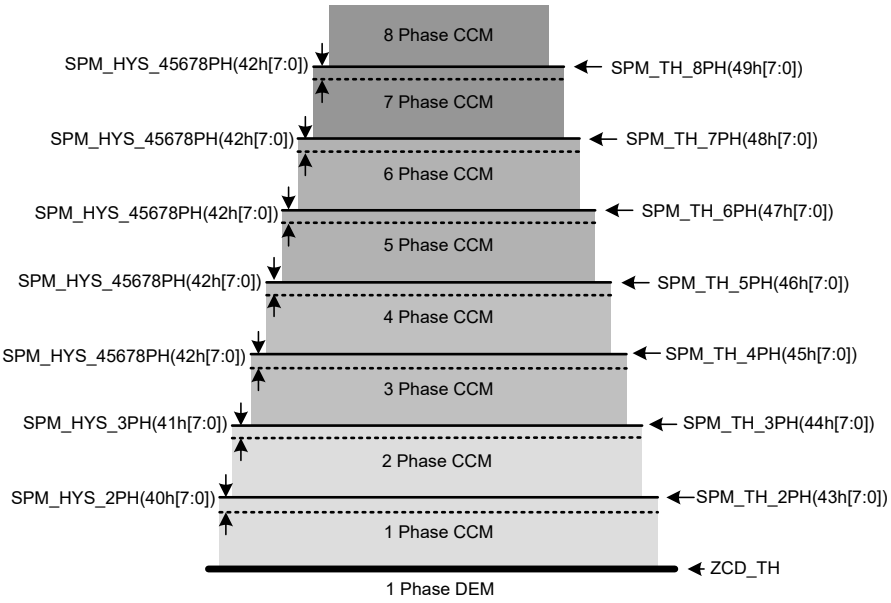


Figure 23-a. Smart Phase Management in 8-Phase for Rail A

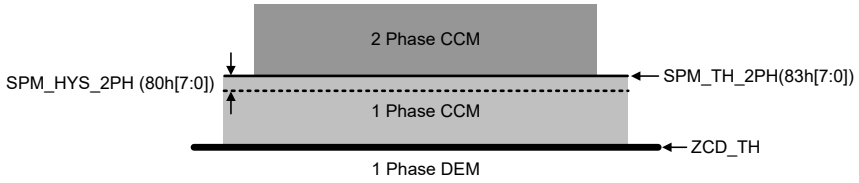


Figure 23-b. Smart Phase Management in 2-Phase for Rail B

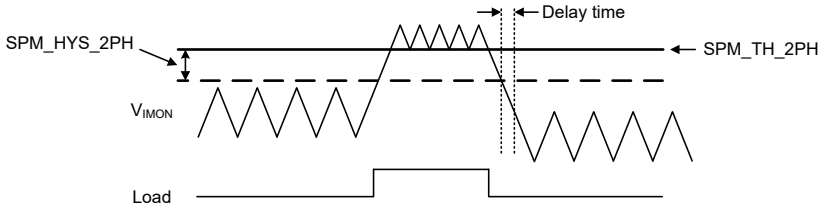


Figure 24. Phase Adding and Shedding

Telemetry for VOUT/IOUT/Temperature

The RT3678BE supports the telemetry function for VOUT, IOUT and temperature.

For VOUT telemetry, the controller continually senses and digitizes the output voltage from differential voltage sense input (VSEN pin and RGND pin), and averages the data to reduce measurement noise. The VOUT data can be read in the I2C register VOUT_RPT[9:0] = {VOUT_RPT_H_25h[1:0], VOUT_RPT_L_24h[7:0]}.

For IOUT telemetry, the controller continually senses the sum current from VIMON signal and averages the data to reduce measurement noise. ($V_{IMON}-V_{VREF}$) is coded by 10-bit ADC and linearly mapped to the output current scale that can be selected via NVM register I_OUT_SCALE_A_24h[2:0] for rail A and I_OUT_SCALE_B_64h[2:0] for rail B. The RT3678BE flexibly provides gain and offset calibrate function about IOUT telemetry, which can be set via NVM register IOUT_CAL_GAIN (4Bh[7:0] for rail A and 8Bh[7:0] for rail B) and IOUT_CAL_OFFSET (4Ah[7:0] for rail A and 8Ah[7:0] for rail B) to calibrate systematic errors related to board layout after PCB assembly. IOUT telemetry data can be read in I^2C register IOUT_RPT[9:0] = {IOUT_RPT_H[1:0], IOUT_RPT_L[7:0]}.

For temperature telemetry, the device continually sense and digitizes the temperature by TSEN pin of each rail, and averages the data to reduce measurement noise. Temperature register is updated every 700μs and the averaging interval is 5.6ms. The filtered temperature can be read in the I2C register TEMP_RPT_23h[7:0].

Undervoltage Lockout (UVLO)

To ensure sufficient power supply for proper operation, the RT3678BE provides VCC undervoltage lockout (UVLO) protection. The controller triggers VCC_UVLO protection if VCC drops below (VCC_POR_R-ΔVCC_POR_F_HYS). The controller will shut down, and all PWMs are in tri-state to turn off both high-side and low-side MOSFETs.

Soft-start Overcurrent Protection (SSOCP)

The RT3678BE provides soft-start overcurrent protection (SSOCP) for each rail while output ramps up from 0V. Figure 25 illustrates the mechanism for SSOCP. When the inductor current exceeds the threshold of SSOCP within 5μs, the controller will turn off both the high-side and low-side MOSFETs immediately, assert OCP_L pin, and assert I^2C register I2C_FAULT_STATUS_1Ah[6]. The SSOCP threshold can be set via NVM register SSOCP_RATIO (24h[6:4] for rail A and 64h[6:4] for rail B). To avoid false triggering, the SSOCP threshold is recommended to be higher than the charging current that approximates to the product of output capacitance and DEFAULT_SLEW_RATE. The SSOCP threshold is defined as:

$$SSOCP\_TH = I\_OUT\_SCALE \times SSOCP\_RATIO$$

After SSOCP event is removed, the controller can be restarted, and the I2C_FAULT_STATUS_1Ah[6] can be cleared by toggling VCC power or PWREN pin.

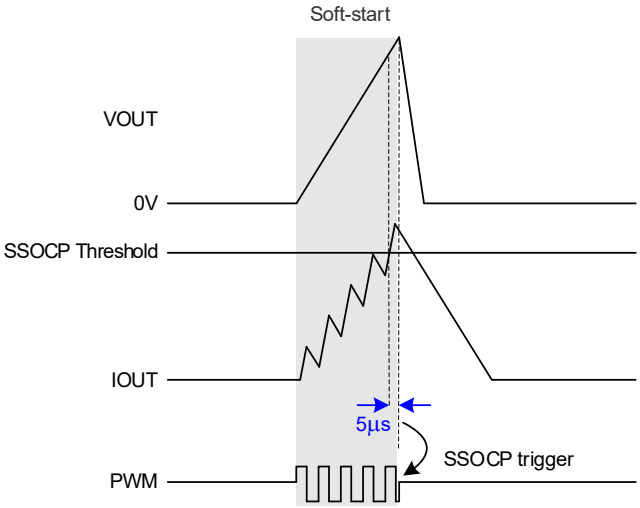


Figure 25. Soft-start Overcurrent Protection Mechanism

Overcurrent Protection (OCP)/Overcurrent Warning (OCP WARN)

The RT3678BE supports two overcurrent protection mechanisms, Overcurrent Protection (OCP) Fault and Overcurrent Warning (OCP WARN). The OCP_L pin is an open-drain output, and an external pull-up resistor is required. Figure 26 illustrates the mechanism for OCP and OCP WARN. When the inductor current exceeds the threshold of OCP WARN, the controller will maintain output regulation, assert OCP_L pin, and assert I2C register I2C_FAULT_STATUS_1Ah[4]. The minimum asserted pulse width of OCP_WARN signal can be set via NVM register OCP_WARN_MIN_PULSE (59h[7:3] for rail A and 99h[7:3] for rail B). The OCP WARN threshold can be set via NVM register OCP_WARN_THRESH (58h[7:0] for rail A and 98h[7:0] for rail B). The OCP warning threshold in PSIx is defined as:

$$I_{OCP\_WARN\_PSI0,1,2,3,7} = \frac{OCP\_WARN\_THRESH[7:0] \times 4 \times I\_OUT\_SCALE}{512A}$$

When the inductor current exceeds the threshold of OCP continuously with a period of OCP delay time, the controller will turn off both the high-side and low-side MOSFETs immediately, de-assert PWRGD, assert OCP_L pin, and assert I2C register I2C_FAULT_STATUS_1Ah[0]. The continuous time that current must exceed OCP_THRESH before triggering fault can be set via NVM register OCP_FAULT_DELAY (59h[2:0] for rail A and 99h[2:0] for rail B). It is recommended that the OCP threshold should be set at the number of active phases multiplied by the current capability of MOSFET. The threshold of OCP can be set via NVM register OCP_THRESH (57h[7:0] for rail A and 97h[7:0] for rail B). The OCP threshold in PSIx is defined as:

$$I_{OCP\_PSI0,1,2,3,7} = OCP\_THRESH[7:0] \times \frac{4 \times I\_OUT\_SCALE}{512A} \times \frac{ACTIVE\_PH}{N}$$

where ACTIVE_PH = active number of phases, N = phase number in PSI0.

After OCP event is removed, the controller can be restarted, and the I2C_FAULT_STATUS_1Ah[0] can be cleared by toggling VCC power or PWREN pin. During VOTF period plus 80μs (After VID settles + 80μs), OCP is masked to avoid trigger.

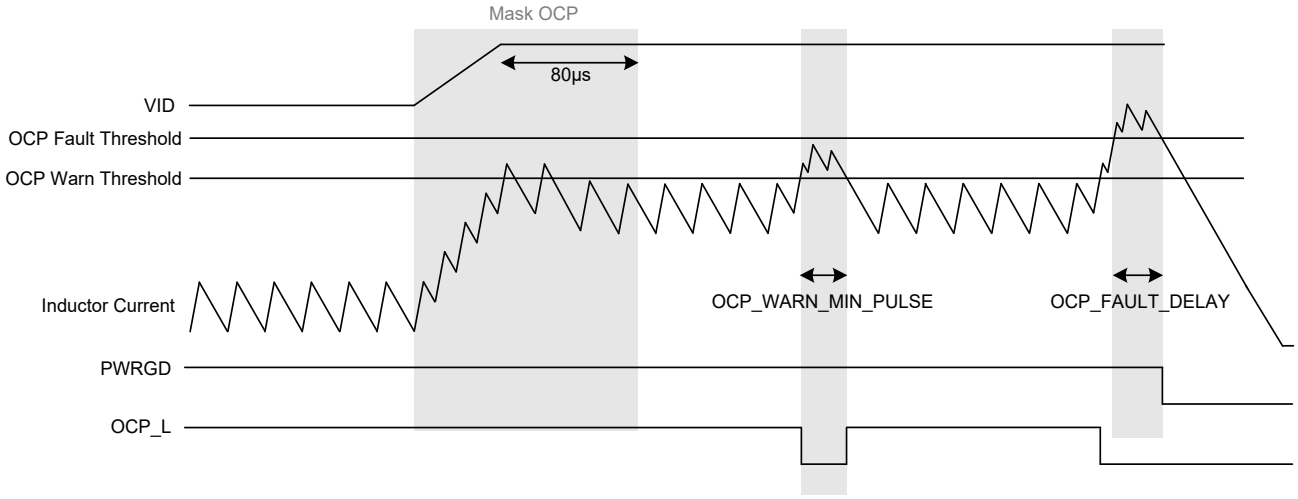


Figure 26. Overcurrent Protection Mechanism

Overvoltage Protection (OVP)

The RT3678BE monitors the output voltage with the VSEN pin for overvoltage detection. The OVP threshold is related to VID condition. Table 12 summarizes the OVP mechanism. The OVP mechanism is illustrated in Figure 27 and Figure 28.

OVP is masked when VID = 0V.

During active regulation, the OVP threshold is VID/VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET, where VID/VID_MAX can be selected via SVI3 register OVP_REF_2Ch[7], OVP_DELTA can be set via SVI3 register OVP_DELTA_2Ch[6:4], VOUT_OFFSET can be set via SVI3 register VOUT_OFFSET_22h[7:0], and I2C_VOUT_OFFSET can set via I2C register I2C_VOUT_OFS_08h[7:0].

During positive/negative VOTF transitions period + 80μs, the OVP threshold is VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET, where VID_MAX can be set via SVI3 register VID_MAX_23h[7:0].

The RT3678BE also provides flexible OVP threshold by I2C register. When I2C_OVP_DELTA_16h[6:4] = 000: I2C_OVP is disabled and the OVP threshold follows SVI3 setting. When I2C_OVP_DELTA_16h[6:4]≠000, I2C_OVP is enabled and the VID/VID_MAX follows I2C setting via I2C register I2C_OVP_REF_16h[7], and the OVP_DELTA follows I2C setting via I2C register I2C_OVP_DELTA_16h[6:4].

When OVP is triggered with 0.8μs filter time, the controller de-asserts PWRGD and forces all PWMs low to turn on low-side power MOSFETs. The PWM remains low until the output voltage is pulled down below OVP_VID. After 60μs from OVP is triggered, VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE.

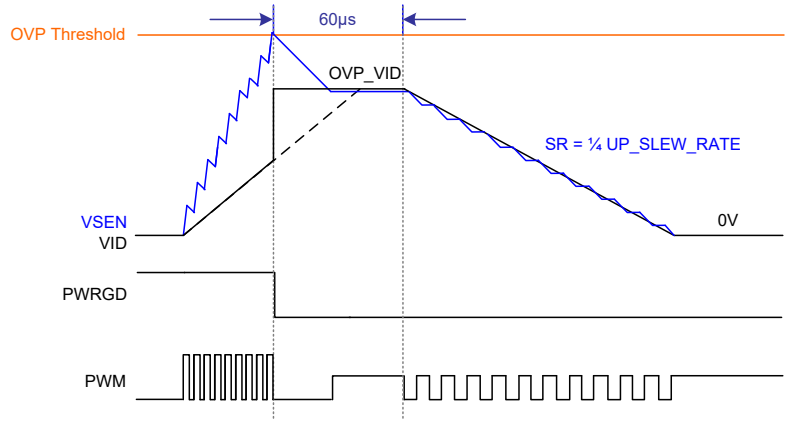


Figure 27. Overvoltage Protection Mechanism during Positive VOTF Transitions

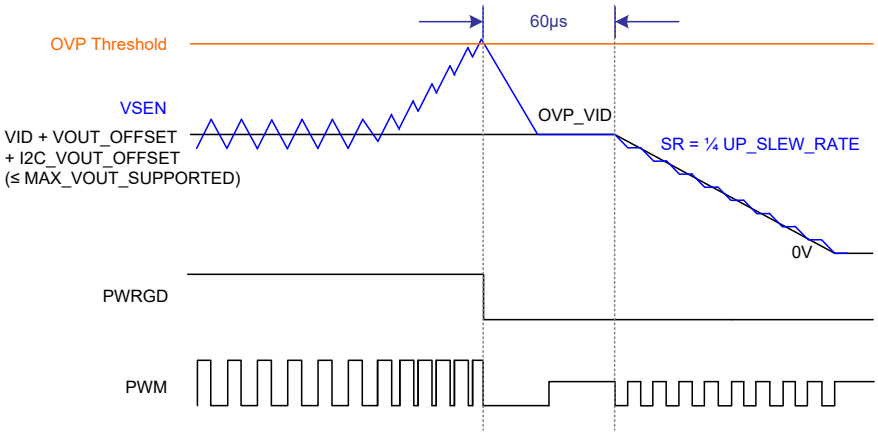


Figure 28. Overvoltage Protection Mechanism during Active Regulation

Table 12. Summary of Overvoltage Protection

Condition	OVP Threshold	Behavior	Protection Reset
VID = 0	OVP is masked.	NA	VCC /PWREN Re-toggled
During VOTF transitions period + 80μs (positive and negative)	OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET **VID_MAX ≠ 0V** OVP_TH = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **VID_MAX = 0V** MAX_VOUT_SUPPORTED is used to calculate OVP threshold. New OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. **VID_MAX ≠ 0V** OVP_VID = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **VID_MAX = 0V** MAX_VOUT_SUPPORTED is used to calculate OVP_VID. OVP_VID = MAX_VOUT_SUPPORTED	
During Active Regulation	**OVP_REF: VID** OVP_TH = VID + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET (VID + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED) **OVP_REF: VID_MAX** OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. **VID_MAX ≠ 0V:** VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED 2. **VID_MAX = 0V:** MAX_VOUT_SUPPORTED is used to calculate OVP threshold. New OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. **OVP_REF: VID** OVP_VID = VID + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED **OVP_REF: VID_MAX** 1. **VID_MAX ≠ 0V:** OVP_VID = VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET ≤ MAX_VOUT_SUPPORTED 2. **VID_MAX = 0V:** MAX_VOUT_SUPPORTED is used to calculate OVP_VID. New OVP_VID = MAX_VOUT_SUPPORTED	
During VOTF transitions period + 80μs in VFIX mode (positive and negative)	**VFIX_EN: Enable** OVP_TH = VFIX_MAX + OVP_DELTA (VFIX_MAX ≤ MAX_VOUT_SUPPORTED)	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID = VFIX_MAX ≤ MAX_VOUT_SUPPORTED	

Continued

Condition	OVP Threshold	Behavior	Protection Reset
During Active Regulation in VFIX mode	**VFIX_EN: Enable** OVP_TH = VFIX + OVP_DELTA (VFIX ≤ VFIX_MAX)	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID = VFIX ≤ VFIX_MAX	VCC /PWREN Re-toggled
Change OVP_TH during VOTF transitions period + 80μs (positive and negative)	**New OVP_TH > Previous OVP_TH** The controller changes new OVP_TH immediately. **New OVP_TH < Previous OVP_TH** After VOTF transitions period + 80μs, the controller changes previous OVP_TH to new OVP_TH.	PWRGD de-assertion. The output voltage is pulled down to OVP_ VID, and VID starts to ramp down to 0V from OVP_VID with 1/4 UP_SLEW_RATE after 60μs. OVP_VID is the same in the four conditions: 1. During VOTF transitions period + 80μs 2. During active regulation 3. During VOTF transitions period + 80μs in VFIX mode 4. During active regulation in VFIX mode	

Undervoltage Protection (UVP)

The RT3678BE monitors the output voltage with the VSEN pin for undervoltage detection. The UVP threshold is related to VID condition. Table 13 summarizes the UVP mechanism.

The UVP mechanism is illustrated in Figure 29. During active regulation, the UVP threshold is VID/VID_MIN - UVP_DELTA + VOUT_OFFSET +I2C_VOUT_OFFSET, where VID/VID_MAX can be selected via SVI3 register UVP_REF_2Ch[3], UVP_DELTA can be set via SVI3 register UVP_DELTA_2Ch[2:0], VOUT_OFFSET can be set via SVI3 register VOUT_OFFSET_22h[7:0], and I2C_VOUT_OFFSET can be set via I2C register I2C_VOUT_OFS_08h[7:0].

UVP is masked during positive/negative VOTF transitions period.

When UVP is triggered with 3.3ms filter time, the controller de-asserts PWRGD and forces all PWMs in tri-state to turn off both high-side and low-side MOSFETs.

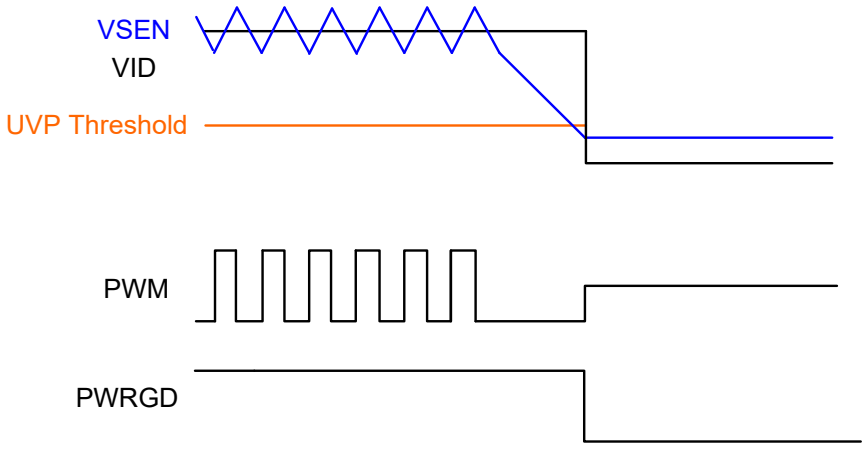


Figure 29. Undervoltage Protection Mechanism during Active Regulation

Table 13. Summary of Undervoltage Protection

Condition	OVP Threshold	Behavior	Protection Reset
VID = 0	UVP is masked.	NA	VCC /PWREN Re-toggled
During VOTF transitions period (positive and negative)	UVP is masked.	NA	
During Active Regulation	**UVP_REF: VID** UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET (MIN_VOUT_SUPPORTED ≤ VID + VOUT_OFFSET + I2C_VOUT_OFFSET) **UVP_REF: VID_MIN** UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET 1. VID_MIN ≠ 0V: MIN_VOUT_SUPPORTED ≤ VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET 2. VID_MIN = 0V: MIN_VOUT_SUPPORTED is used to calculate UVP threshold. New UVP_TH = MIN_VOUT_SUPPORTED - UVP_DELTA	PWRGD de-assertion. All PWMs are in tri-state to turn off both high-side and low-side MOSFETs.	
During VOTF transitions period in VFIX mode (positive and negative)	UVP is masked.	NA	
During Active Regulation in VFIX mode	**VFIX_EN: Enable** UVP_TH = VFIX - UVP_DELTA	PWRGD de-assertion. All PWMs are in tri-state to turn off both high-side and low-side MOSFETs.	

VR-Hot Warning and Over-Temperature Protection (OTP)

The RT3678BE provides VR-Hot Warning and Over-Temperature Protection (OTP) to monitor the temperature from TESN pin of each rail. The VR_HOT# pin is an open-drain output, and an external pull-up resistor is required.

The mechanism of VR-HOT Warning is illustrated in Figure 30. When the sensed temperature is higher than VR-HOT threshold, the controller asserts the VR_HOT bit in the temperature telemetry packet, PWRGD pin keeps high, all PWM signals remain normal regulation, and VR_HOT# pin is asserted to indicate a thermal warning. The VR-HOT threshold can be set via SVI3 register VRHOT_THRESH_2Ah[7:0]. The VR_HOT# can be used to inform the temperature of power stage, and it helps to reduce power consumption when temperature exceeds VR-HOT threshold. VR_HOT# is de-asserted if the VR temperature drops below (VRHOT_THRESH – I2C_VRHOT_HYS). The hysteresis of VR-HOT threshold can be set via I^2C register I2C_VRHOT_HYS_19h[2:0].

The mechanism of OTP is illustrated in Figure 31. When the sensed temperature is higher than OTP threshold, the controller de-asserts PWRGD, asserts the OTP bit in the temperature telemetry packet, and forces all PWMs tri-state to turn off both high-side and low-side MOSFETs. The OTP threshold can be set via SVI3 register OTP_THRESH_2Bh[7:0].

The RT3678BE also provides flexible threshold of VRHOT and OTP by I^2C register. When EN_I2C_VRHOT_16h[1] = 0, the VRHOT threshold follows SVI3 setting. When EN_I2C_VRHOT_16h[1] = 1, the VRHOT threshold follows I^2C setting via I^2C register I2C_VRHOT_TH_18h[7:0]. When EN_I2C_OTP_16h[0] = 0, the OTP threshold follows SVI3 setting. When EN_I2C_OTP_16h[0] = 1, the OTP threshold follows I^2C setting via I^2C register I2C_OTP_TH_17h[7:0].

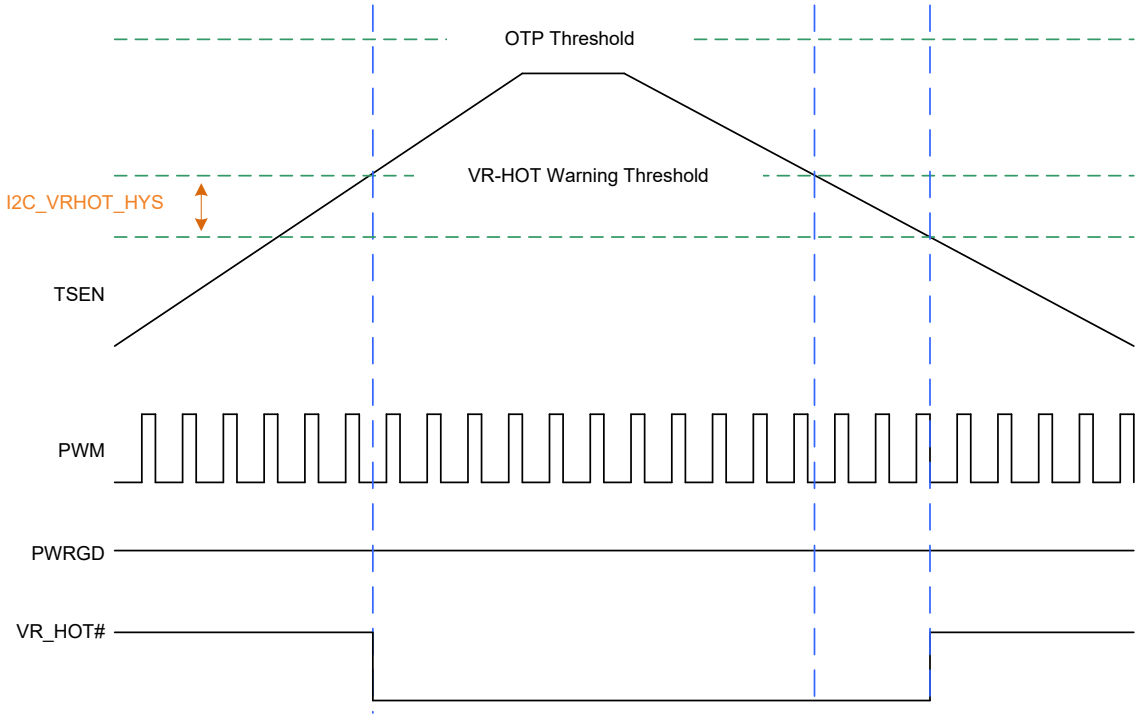


Figure 30. VR-HOT Warning Mechanism

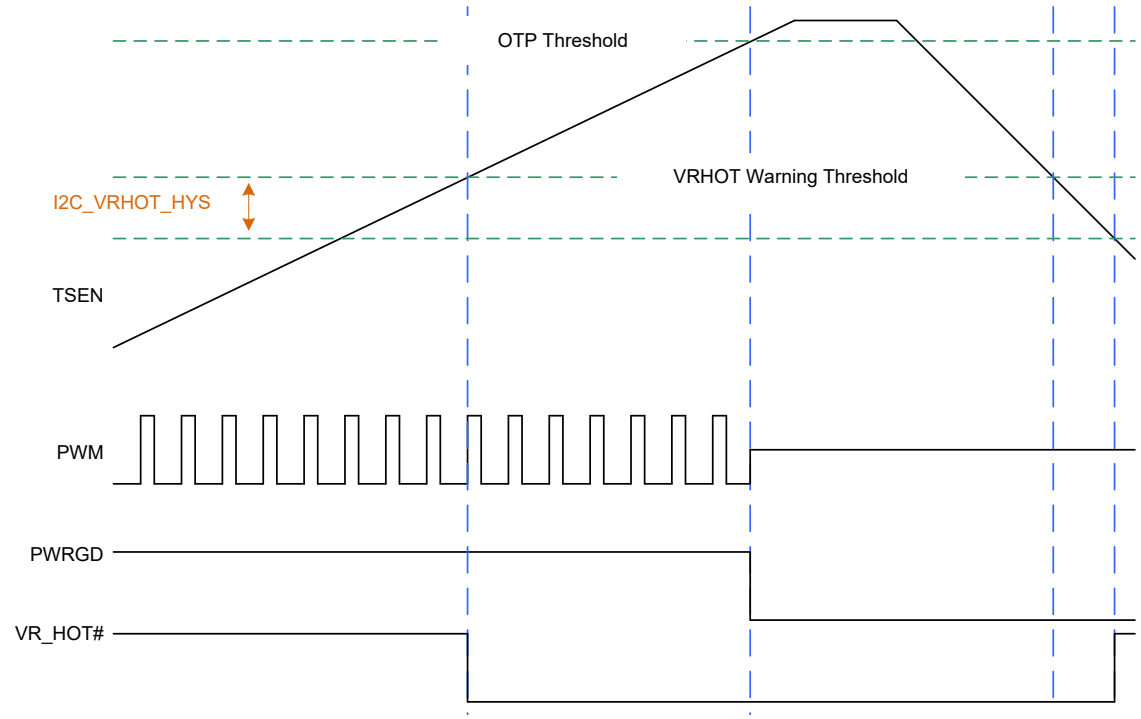


Figure 31. Over-Temperature Protection Mechanism

CRC Failure

NVM loading of the RT3678BE begins after VCC crosses its rising VCC_POR_NVM threshold. When POR_NVM conditions are met, RT3678BE will download NVM into the control registers. The integrity of downloading the configuration from the NVM to the RT3678BE control registers is assured by CRC check. A configuration download CRC failure prevents the controller from leaving the Inactive state and assert I^2C register NVM_PROGRAM_STATUS_ECh[1:0].

Communication Failure

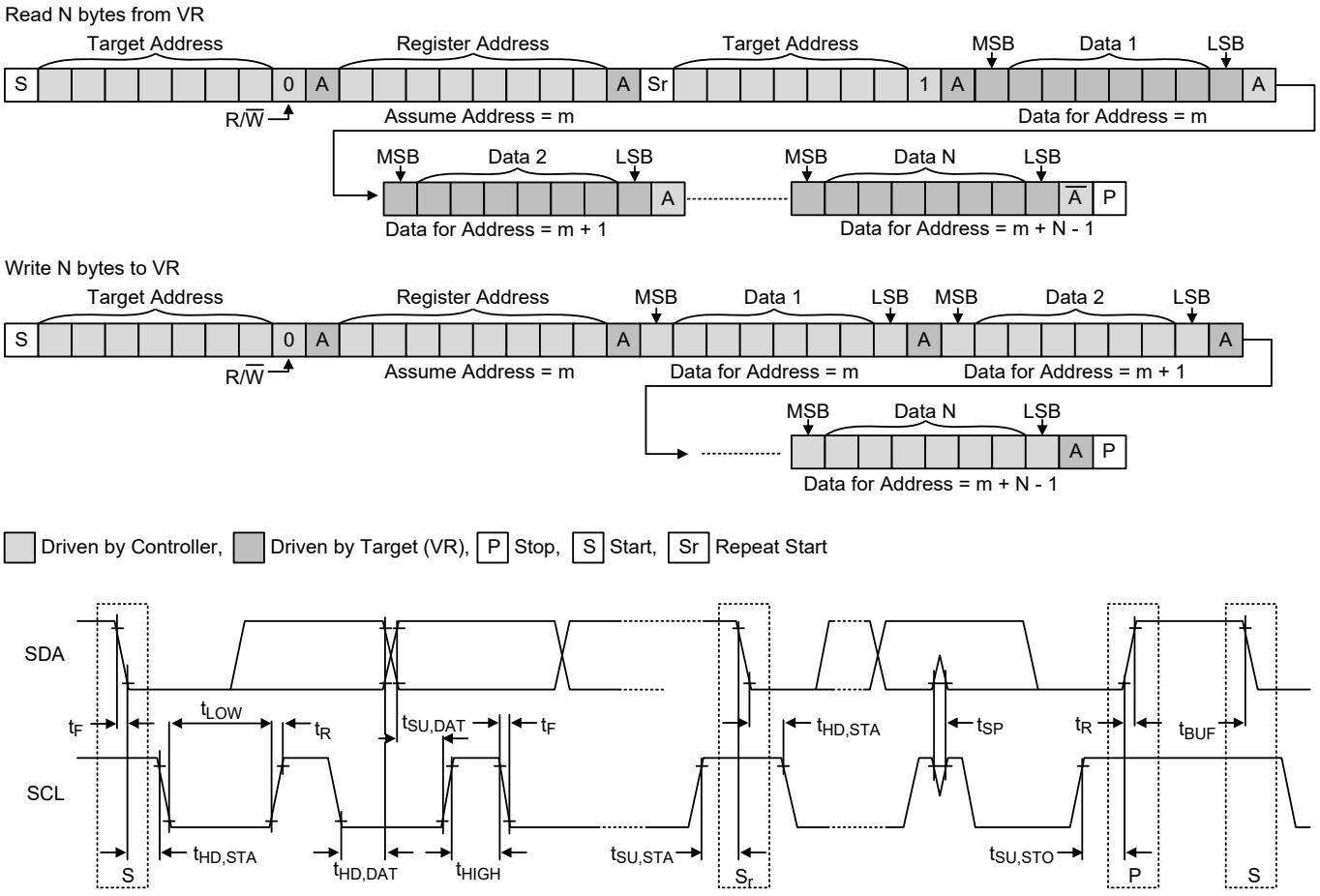
Attempts to access unimplemented commands are detected and reported as communication failures. RT3678BE can recode the SVI3 communication failure through I^2C register SVI3_NACK_STATUS_1Bh. The SVI3_NACK_STATUS command returns one byte of information relating to the SVI3 NACK status: Command before ACK/ Framing Error/ CRC Error/ Undefined Register Command/ Undefined Payload/ Not Executable/ Not Supported.

I²C Interface

The I²C target address (7-bit format) by ADDR pin is summarized in Table 1.

This I²C does not have a stretch function.

The I²C interface supports standard mode (100kbps), and fast mode (400kbps). The write or read bit stream (N>1) is shown below:



General Register Map (Page 03 & 04)

Register Address/NAME		Type	Page	Default Value	NVM	Note
00h	PH1_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH1_CBG = 100%
01h	PH2_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH2_CBG = 100%
02h	PH3_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH3_CBG = 100%
03h	PH4_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH4_CBG = 100%
04h	PH5_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH5_CBG = 100%
05h	PH6_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH6_CBG = 100%
06h	PH7_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH7_CBG = 100%
07h	PH8_CURRENT_BALANCE_GAIN	R/W	Yes	04h	Yes	PH8_CBG = 100%
08h	I2C_VOUT_OFS	R/W	Yes	00h	Yes	I2C_VOUT_OFS = 0mV
09h	VFIX_MAX_L	R/W	Yes	FFh	No	VFIX_MAX = 2.8V
0Ah	VFIX_MAX_H	R/W	Yes	01h	No	
0Bh	EN_VFIX	R/W	Yes	00h	No	EN_VFIX = Disabled
0Ch	VFIX_L	R/W	Yes	97h	Yes	VFIX = 1V
0Dh	VFIX_H	R/W	Yes	00h	Yes	
0Eh	VOFS_BY_IOUT_RPT	R/W	Yes	00h	No	VOFS_BY_IOUT_RPT = 0mV
0Fh	VOFS_BY_IOUT_RPT_TH_L	R/W	Yes	00h	No	VOFS_BY_IOUT_RPT_TH = Disabled
10h	VOFS_BY_IOUT_RPT_TH_H	R/W	Yes	00h	No	
11h	EN_MASK_TIME & VOFS_BY_IOUT_RPT_HYS	R/W	Yes	08h	No	Mask VOFS_BY_IOUT during VOTF+200µs, VOFS_BY_IOUT_RPT_HYS = 12A
12h	EN_PSI	R/W	Yes	00h	Yes	PSI state follows SVI3
13h	I2C_LL_SEL & I2C_LL_ADJ	R/W	Yes	0Ah	No	LL_ADJ follow SVI3, I2C_LL_ADJ = 100%.
14h	EN_PROTECTION	R/W	Yes	7Fh	No	Enable all protections
15h	OCP_WARN_HYS	R/W	Yes	00h	No	OCP_WARN_HYS = 0A
16h	I2C_OVP_REF & I2C_OVP_DELTA & EN_I2C_VRHOT & OTP_TH	R/W	Yes	00h	Yes	OVP_TH, VRHOT_TH and OTP_TH follow SVI3.
17h	I2C_OTP_TH	R/W	Yes	A5h	Yes	I2C_OTP_TH = 125˚C
18h	I2C_VRHOT_TH	R/W	Yes	8Ch	Yes	I2C_VRHOT_TH = 100˚C
19h	I2C_VRHOT_HYS	R/W	Yes	00h	Yes	I2C_VRHOT_HYS = 0˚C
1Ah	I2C_FAULT_STATUS	R	Yes	Current status	No	
1Bh	SVI3_NACK_STATUS	R	Yes	Current status	No	
20h	IOUT_RPT_RATIO	R/W	Yes	00h	No	IOUT_RPT_RATIO = 100%
21h	IOUT_RPT_L	R	Yes	Current status	No	
22h	IOUT_RPT_H	R	Yes	Current status	No	

Register Address/NAME		Type	Page	Default Value	NVM	Note
23h	TEMP_RPT	R	Yes	Current status	No	
24h	VOUT_RPT_L	R	Yes	Current status	No	
25h	VOUT_RPT_H	R	Yes	Current status	No	
26h	P_SYS_RPT_L	R	Yes	Current status	No	
27h	P_SYS_RPT_H	R	Yes	Current status	No	
DD	PRODUCT_ID	R	No	78h	No	RT3678BE
DE	REVISION_CODE	R	No	00h	No	
DF	WDR	R/W	No	03h	Yes	Watchdog-Reset = Enabled, Watchdog-Reset period = 1600ms
ECh	NVM_PROGRAM_STATUS	R	No	Current status	No	
EDh	STORE_RESTORE_CFG	R/W	No	00h	No	
EFh	PAGE	R/W	No	03h	No	EFh=02h: Page 02. Setting registers (Channel Set), EFh=03h: Page 03. General registers for rail A (Channel A), EFh=04h: Page 04. General registers for rail B (Channel B).

Register Address: 00h **Description**: Setting phase 1 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH1_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH1_CBG		[2:0] = 000: 69.2%, [2:0] = 001: 79.2%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (Default). [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08%.				

Register Address: 01h **Description**: Setting phase 2 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH2_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH2_CBG		Please refer to register 00h for detailed description.					

Register Address: 02h **Description**: Setting phase 3 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH3_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH3_CBG		Please refer to register 00h for detailed description.					

Register Address: 03h **Description**: Setting phase 4 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH4_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH4_CBG		Please refer to register 00h for detailed description.					

Register Address: 04h **Description**: Setting phase 5 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH5_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH5_CBG		Please refer to register 00h for detailed description.					

Register Address: 05h **Description**: Setting phase 6 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH6_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH6_CBG		Please refer to register 00h for detailed description.					

Register Address: 06h **Description**: Setting phase 7 current balance gain.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH7_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	PH7_CBG		Please refer to register 00h for detailed description.					

Register Address: 07h
Description: Setting phase 8 current balance gain.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PH8_CURRENT_BALANCE_GAIN							
Default Value	0x04							
Read/Write	R	R	R	R	R	R/W	R/W	R/W

Bits	Name	Description
[7:3]	RESERVED	Reserved bit(s). [7:3] = 00000 (Default).
[2:0]	PH8_CBG	Please refer to register 00h for detailed description.

Register Address: 08h
Description: VOUT offset setting. RT3678BE supports output voltage from 0.25V~2.8V (i.e. 0.25V ≤ VID setting ± SVI3_VOUT_OFFSET ± I2C_VOUT_OFFSET ≤ 2.8V). RT3678BE will slew VOUT to target voltage at the slew rate of 1/4 of SVI3_UP_SLEW_RATE, while the minimum slew rate is limited at 2.5 mV/μs. The VR will return to PSI0 and begin to ramp up when an offset command is received. The VR will return to its original PSI state after the output voltage is within tolerance band. If CPU sends a PSI-changing command, the controller follows the command with VOUT offset remain existing. When CPU sends VID off command, the output voltage is 0V regardless of the value of offset register.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VOUT_OFS							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	I2C_VOUT_OFS	[7]: sign bit (as part of two's complement). [6:0]: 5mV/LSB For example, [7:0] = 00h: 0mV (Default), [7:0] = 01h: 5mV, [7:0] = 7Fh: 635mV, [7:0] = FFh: 5mV, [7:0] = 80h: 640mV.

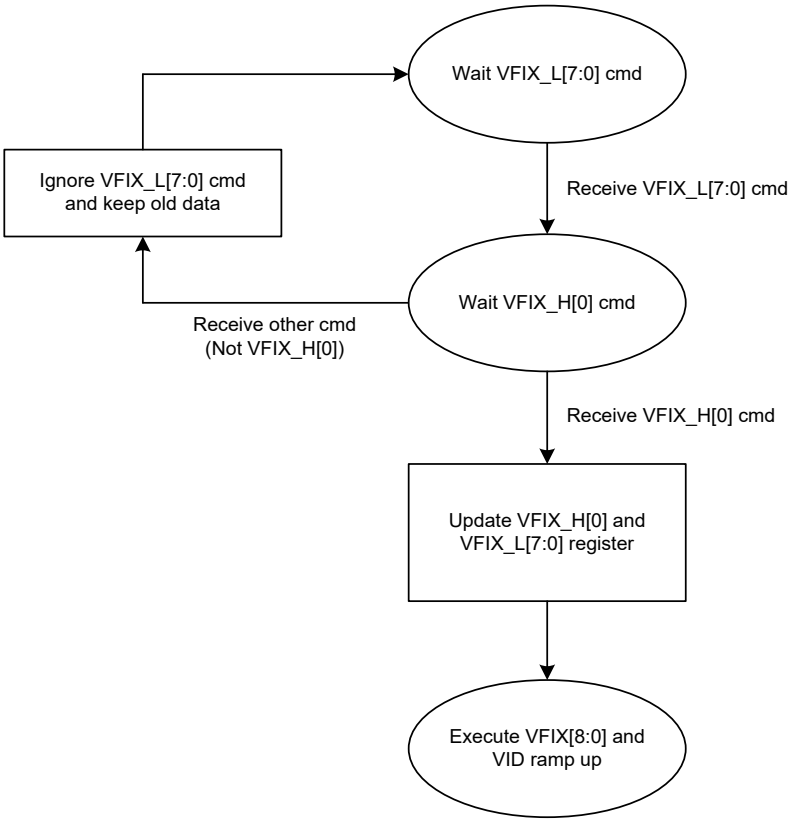
Register Address: 09h
Description: Setting the maximum value of Fixed-VID mode.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_L							
Default Value	0xFF							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VFIX_MAX_L	Default value of VFIX_MAX[8:0] is 1FFh = 2.8V. VFIX_MAX[8:0] = { VFIX_MAX_H[0], VFIX_MAX_L[7:0] }, Please refer to SVI3 Type I Target VID Table. RT3678BE supports output voltage from 0.25V~2.8V. VFIX_MAX will be limited at 2.8V if a value greater than 2.8V is given.

Register Address: 0Ah **Description**: Setting the maximum value of Fixed-VID mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_MAX_H							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	R/W
Bits	**Name**		**Description**					
[7:1]	RESERVED		Reserved bit(s). [7:1] = 0000000 (Default).					
[0]	VFIX_MAX_H		Please refer to the description of VFIX_MAX_L.					

Register Address: 0Bh **Description**: Enable/disable Fixed-VID mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_VFIX							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R/W
Bits	**Name**		**Description**					
[7:1]	RESERVED		Reserved bit(s). [7:1] = 0000000 (Default).					
[0]	EN_VFIX		[0] = 0: Disable Fixed-VID mode (Default), [0] = 1: Enable Fixed-VID mode.					



Register Address: 0Ch
Description: A 9-bit VOUT command for Fixed-VID mode. If Fixed-VID mode is enabled, VR skips all VID and offset commands and responds to PSI-changing command when necessary. When Fixed-VID mode is disabled, VR returns to its original VID and PSI state set by last SVI3 command(s). The VOUT slew rate of Fixed-VID mode entry and exit is 1/4 of SVI3_UP_SLEW_RATE.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_L							
Default Value	0x97							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VFIX_L	Default value of VFIX[8:0] is 097h = 1V. VFIX[8:0] = { VFIX_H[0], VFIX_L[7:0] }. Please refer to SVI3 Type I Target VID Table. VFIX[8:0] command can be set within VFIX_MAX. If VFIX[8:0] command is beyond VFIX_MAX, VOUT will keep the previous VFIX[8:0] command.

Register Address: 0Dh
Description: Please refer to the description of VFIX_L (I^2C register 0x0C).

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VFIX_H							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
[7:1]	RESERVED	Reserved bit(s). [7:1] = 0000000 (Default).
[0]	VFIX_H	Please refer to the description of VFIX_L.

Register Address: 0Eh
Description: Changing VOUT offset dynamically based on IOUT reporting. If IOUT telemetry exceeds the threshold defined in I^2C register 0x0F and 0x10, the offset of VOFS_BY_IOUT_RPT(0x0E) will be added to VOUT automatically without additional communication required.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VOFS_BY_IOUT_RPT	[7]: sign bit (as part of two's complement). [6:0]: 5mV/LSB For example, [7:0] = 00h: 0mV (Default), [7:0] = 01h: 5mV, [7:0] = 7Fh: 635mV, [7:0] = FFh: 5mV, [7:0] = 80h: 640mV.

Register Address: 0Fh
Description: A 10-bit IOUT threshold for changing VOUT offset dynamically. It should be noticed that VOFS_BY_IOUT_RPT_THRESH_L needs to be programmed prior to VOFS_BY_IOUT_RPT_THRESH_H in order to successfully set the IOUT threshold.

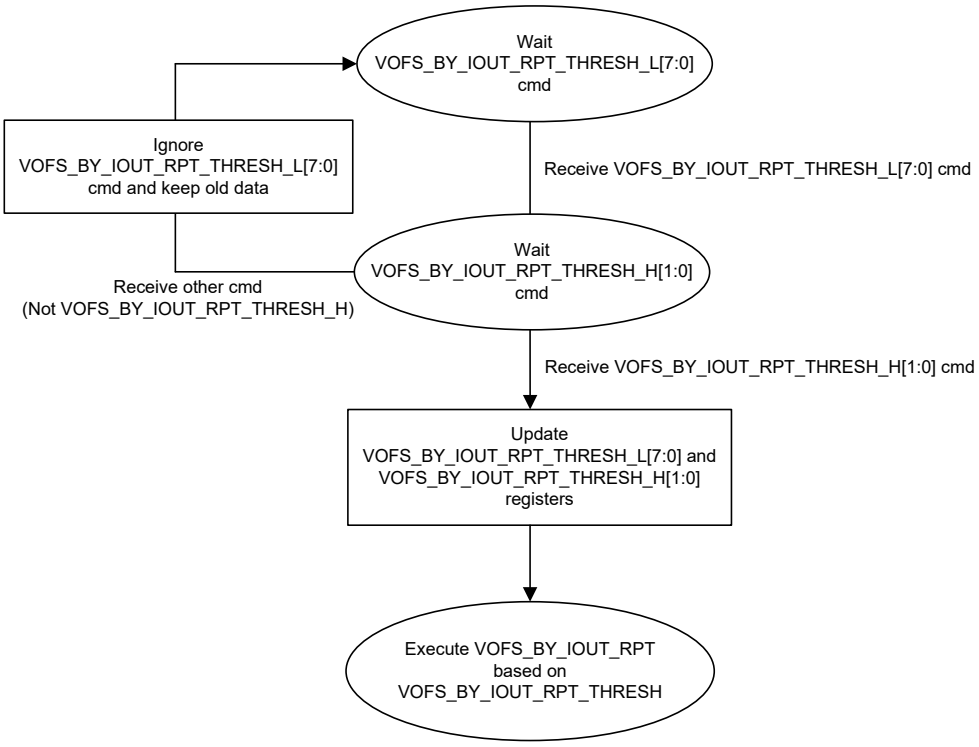
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT_THRESH_L							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	VOFS_BY_IOUT_RPT_THRESH_L	VOFS_BY_IOUT_RPT_THRESH[9:0] = { 0x10[1:0], 0x0F[7:0] }. IOUT_THRESH = VOFS_BY_IOUT_RPT_THRESH[9:0] × I_OUT_SCALE/1023. This function is disabled if VOFS_BY_IOUT_RPT_THRESH[9:0] = 0000h (Default).

Register Address: 10h
Description: Please refer to the description of VOFS_BY_IOUT_RPT_THRESH_L (I^2C register 0x0F).

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOFS_BY_IOUT_RPT_THRESH_H							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s). [7:2] = 0000000 (Default).
[1:0]	VOFS_BY_IOUT_RPT_THRESH_H	Please refer to the description of VOFS_BY_IOUT_RPT_THRESH_L (I^2C register 0x0F).



Register Address: 11h
Description: The function of offsetting VOUT based on IOUT can be masked during VOTF + 200μs to avoid false triggering by capacitor charging current. The hysteresis is also defined to avoid repeatedly entry and exit of VOFS_BY_IOUT_RPT_HYS.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_MASK_TIME & VOFS_BY_IOUT_RPT_HYS							
Default Value	0x08							
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:4]	RESERVED	Reserved bit(s). [7:4] = 0000 (Default).
[3]	EN_MASK_TIME	[3] = 0: Always keep VOFS_BY_IOUT_RPT function. [3] = 1: Mask VOFS_BY_IOUT_RPT during VOTF + 200μs (Default).
[2:0]	VOFS_BY_IOUT_RPT_HYS	[2:0] = 000: 12A (Default) [2:0] = 001: 16A [2:0] = 010: 20A [2:0] = 011: 24A [2:0] = 100: 28A [2:0] = 101: 32A [2:0] = 110: 36A [2:0] = 111: 40A

Register Address: 12h
Description: Set EN_IGNORE_PSI7, EN_FORCE_PSI7, EN_FORCE_PSI0.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PSI							
Default Value	0x00							
Read/Write	R	R	R	R	R	R/W	R/W	R/W

Bits	Name	Description
[7:3]	RESERVED	Reserved bit(s). [7:3] = 00000 (Default).
[2]	EN_IGNORE_PSI7	[2] = 0: Disable, follow SVI3 power states (Default), [1] = 1: Enable, PSI7 ignored. VR will operate in full-phase count when PSI7 command is received. The PSI state register will follow SVI3 specification and ACK PSI-changing commands.
[1]	EN_FORCE_PSI7	[1] = 0: Disable, follow SVI3 power states (Default), [1] = 1: Enable, Force VR to operate in PSI7 and ignore other PSI commands, i.e., the smart phase management (SPM) function is always enabled. The PSI state register will follow SVI3 specification and ACK PSI-changing commands.
[0]	EN_FORCE_PSI0	[0] = 0: Disable, follow SVI3 power states (Default), [0] = 1: Enable, Force VR to operate in PSI0 and ignore other PSI commands, i.e., VR always operates in full-phase count. The PSI state register will follow SVI3 specification and ACK PSI-changing commands.

VR Operation Mode by EN_PSI_12h[2:0]:

EN_IGNORE _PSI7_12h[2]	EN_FORCE _PSI7_12h[1]	EN_FORCE _PSI0_12h[0]	VR Operation Mode
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	Enable	Force PSI0.
Disable	Enable	Disable	Force PSI7.
Disable	Enable	Enable	Force PSI0.
Enable	Disable	Disable	Follow SVI3 power states except PSI7. Operator in full-phase count when PSI7 command is received.
Enable	Disable	Enable	Force PSI0.
Enable	Enable	Disable	Follow SVI3 power states.
Enable	Enable	Enable	Force PSI0.

Register Address: 13h
Description: Setting load-line adjustment and ratio.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_LL_SEL & I2C_LL_ADJ							
Default Value	0x0A							
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7]	I2C_LL_SEL	[7] = 0: LL_ADJ follows SVI3 (Default), [7] = 1: LL_ADJ follows I^2C register.
[6:5]	RESERVED	Reserved bit(s). [6:5] = 100 (Default).
[4:0]	I2C_LL_ADJ	Load-line adjustment relative to nominal load-line. RLL = I2C_LL_ADJ × 10% × Nominal LL 10101b~11111b = invalid (out of range). The default value of I2C_LL_ADJ is 01010b (100% of nominal LL).

Register Address: 14h **Description**: Enable/Disable protection functions.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EN_PROTECTION							
Default Value	0x7F							
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7]	RESERVED		Reserved bit(s).					
[6]	EN_VRHOT		[6] = 0: Disable VRHOT function, [6] = 1: Enable VRHOT function (Default).					
[5]	EN_OTP		[5] = 0: Disable OT protection, [5] = 1: Enable OT protection (Default).					
[4]	EN_OCP_WARN		[4] = 0: Disable OC warning, [4] = 1: Enable OC warning (Default).					
[3]	EN_OCP		[3] = 0: Disable sum OC protection, [3] = 1: Enable sum OC protection (Default).					
[2]	RESERVED		Reserved bit(s). [2] = 1 (Default).					
[1]	EN_UVP		[1] = 0: Disable UV protection, [1] = 1: Enable UV protection (Default).					
[0]	EN_OVP		[0] = 0: Disable OV protection, [0] = 1: Enable OV protection (Default).					

Register Address: 15h **Description**: Setting current hysteresis for OCP warning.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCP_WARN_HYS							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	OCP_WARN_HYS		OCP warning hysteresis. The default value is 00h. OCP_WARN_HYS = [7:0]/384 × I_OUT_SCALE.					

Register Address: 16h **Description**: Setting the control mode for OVP, VRHOT and OTP threshold.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_OVP_REF & I2C_OVP_DELTA & EN_I2C_VRHOT & EN_I2C_OTP							
Default Value	0x00							
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Bits	**Name**		**Description**					
[7]	I2C_OVP_REF		Reference to set overvoltage protection threshold. [7] = 0: VID [7] = 1: VID_MAX					
[6:4]	I2C_OVP_DELTA		Delta value to set overvoltage protection threshold. [6:4] = 000: Disable, follow SVI3 [6:4] = 001: 350mV [6:4] = 010 to 111: 16h[6:4] x 50mV + 350 mV					
[3:2]	RESERVED		Reserved bit(s). [3:2] = 00 (Default).					
[1]	EN_I2C_VRHOT		[1] = 0: VRHOT threshold is controlled by SVI3 (Default), [1] = 1: VRHOT threshold is controlled by I^2C.					
[0]	EN_I2C_OTP		[0] = 0: OTP threshold is controlled by SVI3 (Default), [0] = 1: OTP threshold is controlled by I^2C.					

Register Address: 17h **Description**: Setting OTP threshold in I^2C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_OTP_TH							
Default Value	0xA5							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	I2C_OTP_TH		Over-temperature protection threshold. if EN_I2C_OTP = 1, OTP Threshold = I2C_OTP_TH[7:0] - 40˚C. [7:0] = 00h: Disable, [7:0] = A5h: 125˚C (Default).					

Register Address: 18h **Description**: Setting VRHOT threshold in I^2C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VRHOT_TH							
Default Value	0x8C							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:0]	I2C_VRHOT_TH		Voltage regulator hot warning threshold. if EN_I2C_VRHOT = 1, VRHOT Threshold = I2C_VRHOT_TH [7:0] - 40˚C. [7:0] = 00h: Disable, [7:0] = 8Ch: 100˚C (Default).					

Register Address: 19h **Description**: Setting VRHOT de-assertion hysteresis in I2C control mode.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VRHOT_HYS							
Default Value	0x00							
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Bits	**Name**		**Description**					
[7:3]	RESERVED		Reserved bit(s). [7:3] = 00000 (Default).					
[2:0]	I2C_VRHOT_HYS		[2:0] = 000: No hysteresis (Default), [2:0] = 001: 3°C, [2:0] = 010: 6°C, [2:0] = 011: 9°C, [2:0] = 100: 12°C, [2:0] = 101: 15°C, [2:0] = 110: 18°C, [2:0] = 111: 21°C.					

Register Address: 1Ah **Description**: The I2C_FAULT_STATUS command returns one byte of information relating to the fault status.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_FAULT_STATUS							
Default Value	Current status							
Read/Write	R	R	R/W	R/W	R	R	R	R
Bits	**Name**		**Description**					
[7]	RESERVED		Reserved bit(s). [7] = 0 (Default).					
[6]	SSOCP_FAULT		Output Soft-start Overcurrent Fault.					
[5]	VRHOT		Voltage Regulator Hot Warning. This bit is writeable 1b to clear.					
[4]	OCP_WARN		Output Overcurrent Warning. This bit is writable 1b to clear.					
[3]	OTP_FAULT		Over-temperature Fault					
[2]	UVP_FAULT		Output Undervoltage Fault.					
[1]	OVP_FAULT		Output Overvoltage Fault.					
[0]	OCP_FAULT		Output Overcurrent Fault.					

Register Address: 1Bh
Description: The SVI3_NACK_STATUS command returns one byte of information relating to the SVI3 NACK status.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SVI3_NACK_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:6]	RESERVED	Reserved bit(s).
[5]	Communication Error	Command before ACK
[4]	Communication Error	Framing Error
[3]	Communication Error	CRC Error
[2]	Invalid Command	Undefined Register Command
[1]	Invalid Command	Undefined Payload
[0]	Invalid Command	Not Executable/Not Supported.

Register Address: 20h
Description: Setting output current reporting ratio adjustment.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_RATIO							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s). [7:2] = 000000 (Default).
[1:0]	IOUT_RPT_RATIO	[1:0] = 00: IOUT_RPT_RATIO = 100% (Default), [1:0] = 01: IOUT_RPT_RATIO = 87.5% [1:0] = 10: IOUT_RPT_RATIO = 75% [1:0] = 11: IOUT_RPT_RATIO = 50%

Register Address: 21h
Description: The IOUT_RPT command returns the actual measured output current shown in the least-significant byte of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_L							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	IOUT_RPT_L	IOUT_RPT[9:0] = { IOUT_RPT_H[1:0], IOUT_RPT_L[7:0] } IOUT = IOUT_RPT[9:0] × I_OUT_SCALE /1023.

Register Address: 22h
Description: The IOUT_RPT command returns the actual measured output current shown in the two most-significant bits of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOUT_RPT_H							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s).
[1:0]	IOUT_RPT_H	Please refer to the description of IOUT_RPT_L (I^2C register 0x21).

Register Address: 23h
Description: The TEMP_RPT command returns the actual measured temperature in ˚C shown in the 8-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEMP_RPT							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	TEMP_RPT	Temperature (˚C) = TEMP_RPT[7:0] - 40˚C.

Register Address: 24h
Description: The VOUT_RPT command returns the actual measured output voltage shown in the least-significant byte of the 10-bit.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_L							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	VOUT_RPT_L	VOUT_RPT[9:0] = { VOUT_RPT_H[1:0], VOUT_RPT_L [7:0] } VOUT (V) = VOUT_RPT[9:0] × 5mV.

Register Address: 25h
Description: The VOUT_RPT command returns the actual measured output voltage shown in the two most-significant bits of the 10-bit output voltage reporting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VOUT_RPT_H							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s).
[1:0]	VOUT_RPT_H	Please refer to the description of VOUT_RPT_L (I^2C register 0x24).

Register Address: 26h
Description: The P_SYS_RPT command returns the actual measured system power shown in the two most-significant bits of the 10-bit output voltage reporting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	P_SYS_RPT_L							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	P_SYS_RPT_L	P_SYS_RPT[9:0] = { P_SYS _RPT_H[1:0], P_SYS_RPT_L [7:0] } P_SYS (V) = P_SYS_RPT[9:0] × P_SYS_SCALE/1023.

Register Address: 27h
Description: The P_SYS_RPT command returns the actual measured system power shown in the two most-significant bits of the 10-bit output voltage reporting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	P_SYS_RPT_H							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:2]	RESERVED	Reserved bit(s).
[1:0]	P_SYS_RPT_H	Please refer to the description of P_SYS_RPT_L (I^2C register 0x26).

Register Address: DDh
Description: The PRODUCT_ID is a read-only register that shows the code identifier of RT3678BE.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRODUCT_ID							
Default Value	0x78							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	PRODUCT_ID	[7:0] = 78h (Default).

Register Address: DEh
Description: A read-only shows the unique model code defined by manufacturer.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REVISION_CODE							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:0]	REVISION_CODE	Copy from SVI3 register MODEL_ID[7:0]. Unique model code defined by manufacturer.

Register Address: DFh
Description: Watchdog-reset status, enable/disable watchdog function and setting watchdog-reset period.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	WDR							
Default Value	0x03							
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
[7]	WATCHDOG_STATUS	**Watchdog-Reset Status** [7] = 0: Normal I^2C transmission [7] = 1: SMBus transmission hanging exceeds watchdog-reset period
[6:2]	RESERVED	Reserved bit(s).
[1]	EN_WATCHDOG_RESET	**Enable/Disable watchdog function** [1] = 0: Disable Watchdog-Reset (If I^2C transition hanging exceeds 30ms, VR I^2C interface state machine is reset but all registers keep the latest value.) [1] = 1: Enable Watchdog-Reset (Watchdog period is based on WATCHDOG_RESET_PERIOD[0] setting. When I^2C transmission hanging exceeds the setting, all I^2C registers reset to the default value.) (Default)
[0]	WATCHDOG_RESET_PERIOD	**Watchdog-Reset period** [0] = 0: 800ms [0] = 1: 1600ms (Default)

Register Address: ECh
Description: The NVM_PROGRAM_STATUS command returns one byte of information relating to the NVM program status.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NVM_PROGRAM_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7]	RESTORE_FLAG	Restore process done.
[6]	STORE_FLAG	Store process done.
[5]	STORE_ALLOW	Store process allowed.
[4]	RESTORE_BUSY	NVM restore busy.
[3]	STORE_BUSY	NVM store busy.
[2]	RESERVED	Reserved bit(s).
[1]	CRC_FAILURE_NVM	NVM check fail.
[0]	CRC_FAILURE_NVM_Total	Total NVM check fail.

Register Address: EDh
Description: NVM store and restore command register. A STORE command instructs the device to copy all the contents of the operating memory into corresponding location of non-volatile memory. A RESTORE command instructs the device to copy the entire contents of non-volatile memory into corresponding addresses of operating memory. It is suggested to disable all the outputs of VR before sending STORE and RESTORE commands.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	STORE_RESTORE_CFG							
Default Value	0x00							
Read/Write	W	W	W	W	W	W	W	W

Bits	Name	Description
[7:0]	STORE_RESTORE_CFG	[7:0] = 66h: Restore all storable register settings from NVM, [7:0] = AAh: Store all storable register settings into NVM as new defaults. Except the two instructions mentioned above, all the other combinations are not defined.

Register Address: EFh
Description: The PAGE command provides the ability to configure, control and monitor multiple PWM channels through only one physical address.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PAGE							
Default Value	0x03							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
[7:0]	PAGE	[7:0] = 02h: Page 02. Setting registers (Channel Set), [7:0] = 03h: Page 03. General registers for rail A (Channel A) (Default), [7:0] = 04h: Page 04. General registers for rail B (Channel B), All the other combinations are not defined.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-68L 8x8 package, the thermal resistance, θ_{JA}, is 26.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (26.3°C/W) = 3.8W for a WQFN-68L 8x8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 32 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

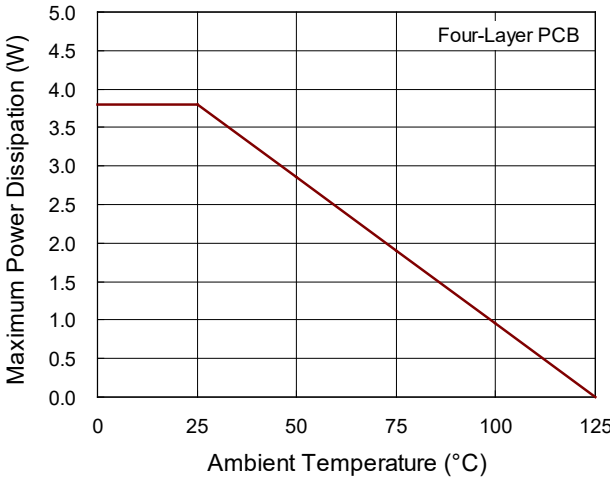
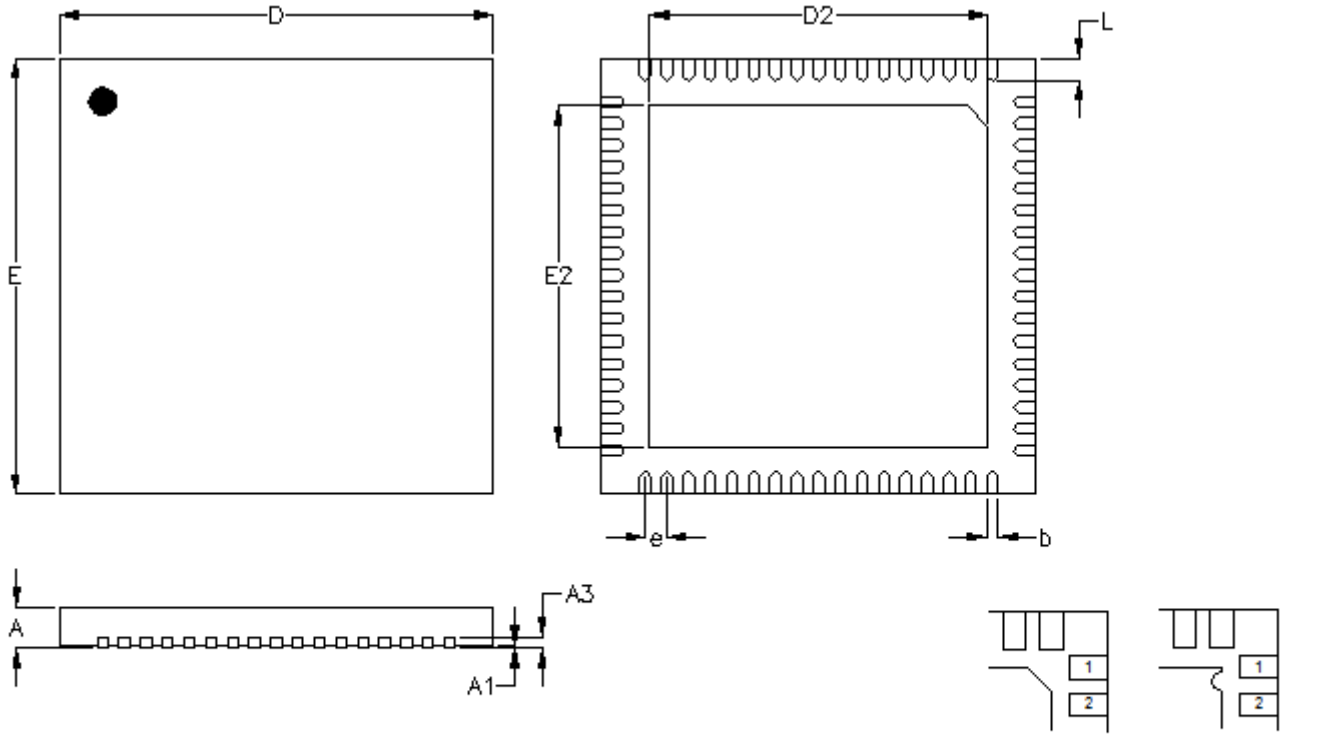


Figure 32. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

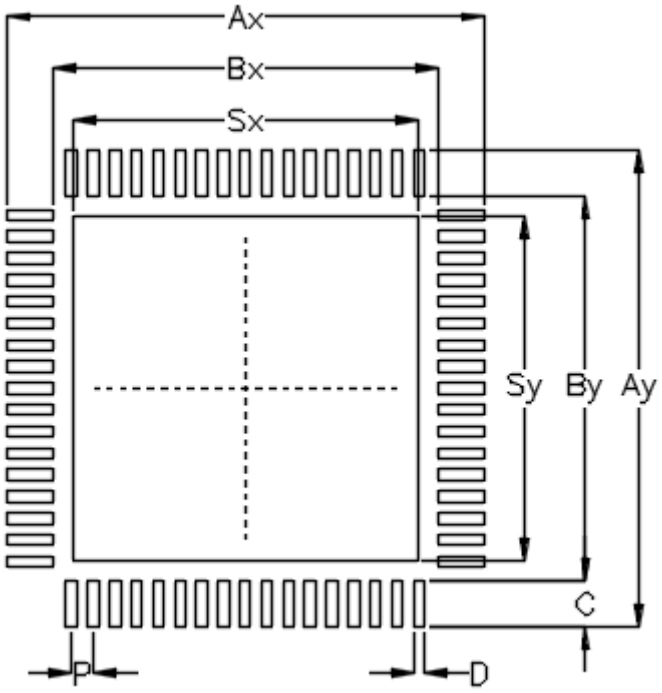
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	7.900	8.100	0.311	0.319
D2	6.200	6.300	0.244	0.248
E	7.900	8.100	0.311	0.319
E2	6.200	6.300	0.244	0.248
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 68L QFN 8x8 Package

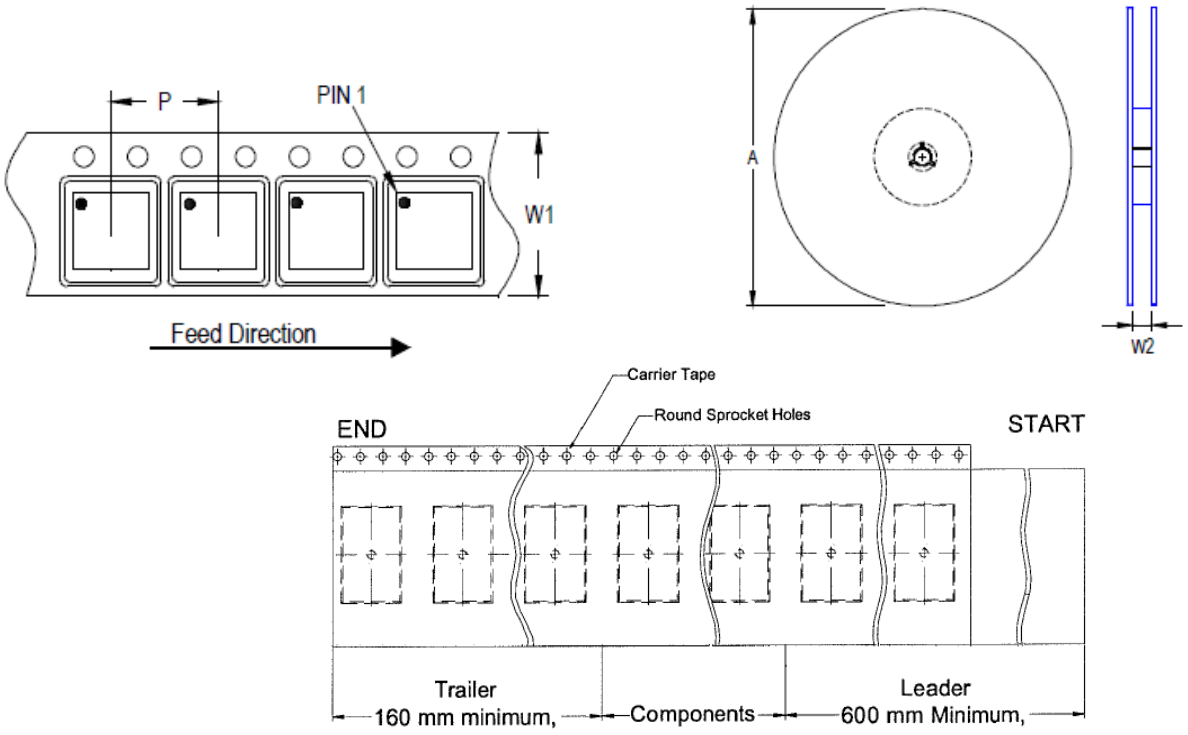
Footprint Information



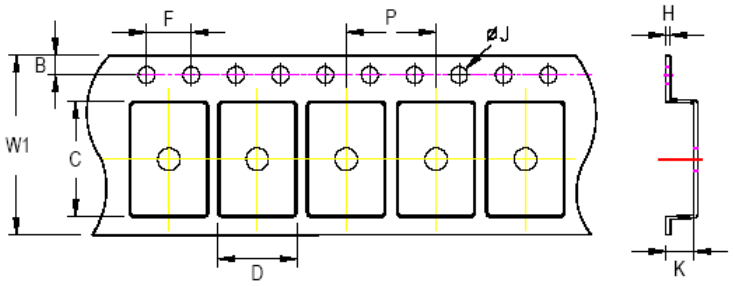
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN8*8-68	68	0.40	8.80	8.80	7.10	7.10	0.85	0.20	6.35	6.35	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 8x8	16	12	330	13	2,500	160	600	16.4/18.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton		
	Size	Units	Item	Weight(kg)	Reels	Units	Item	Boxes	Units
QFN and DFN 8x8	13”	2,500	Box G	1.11	1	2,500	Carton A	6	15,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

Datasheet Revision History

Version	Date	Description	Item
00	2023/3/22	Final	Functional Pin Description on P2 Operation on P7 Electrical Characteristics on P12 Application Information on P21, P23, P25, P26, P27, P29, P30, P35, P36, P37, P55, P57, P68, P73, P79, P83, P85