

## **Dual Output LCD Bias for Smartphones and Tablets**

### **General Description**

The RT4801A is a highly integrated Boost and LDO and inverting charge pump to generate positive and negative output voltage. The output voltages can be adjusted from  $\pm 4V$  to  $\pm 6V$  with 100mV steps by I<sup>2</sup>C interface protocols. With its input voltage range of 2.5V to 5.5V, RT4801A is optimized for products powered by single-cell batteries and symmetrical output currents up to 80mA. The RT4801A is available in the WL-CSP -15B 1.31x2.07 (BSC) package.

### **Ordering Information**

RT4801A-□□□	
□□□	Package Type WSC : WL-CSP-15B 1.31x2.07 (BSC)
□□□	Output Voltage 50 : $\pm 5V$ 60 : $\pm 6V$

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

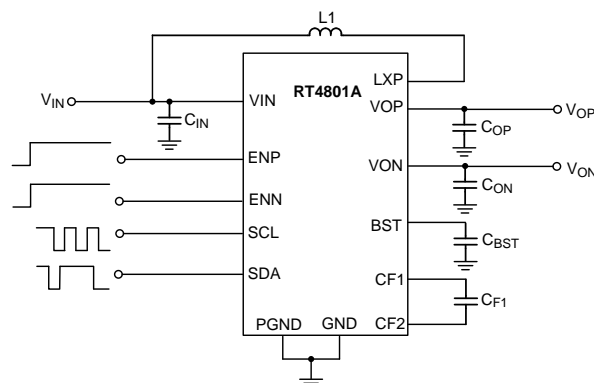
### **Features**

- 2.5V to 5.5V Supply Voltage Range
- Up to 90% Efficiency with Small Magnetics
- Support Up to 80mA Output Current
- Low 1 $\mu$ A Shutdown Current
- Internal Soft-start Function
- Short Circuit Protection Function
- Over-Voltage Protection Function
- Over-Current Protection Function
- Over-Temperature Protection Function
- Elastic Positive and Negative Voltage On/Off Control by ENP/ENN
- Voltage Output from 4V to 6V per 0.1V
- Low Input Noise and EMI
- Output with Programmable Fast Discharge when IC Shutdown
- Adjustable Output Voltage by I<sup>2</sup>C Compatible Interface
- Available in the 15-Ball WL-CSP Package

### **Applications**

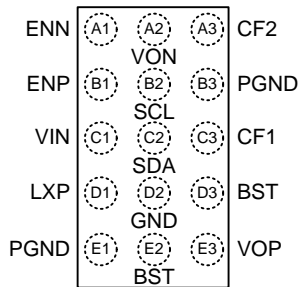
- TFT-LCD Smartphones
- TFT-LCD Tablets
- General Dual Power Supply Applications

## **Simplified Application Circuit**



## Pin Configurations

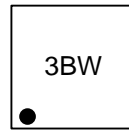
(TOP VIEW)



WL-SP-15B 1.31x2.07 (BSC)

## Marking Information

RT4801AWSC



3B : Product Code  
W : Date Code

## Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	ENN	Enable Control Input for VON.
A2	VON	Negative Terminal Output.
A3	CF2	Negative Charge Pump Flying Capacitor Pin.
B1	ENP	Enable Control Input for VOP.
B2	SCL	Clock of I <sup>2</sup> C.
B3, E1	PGND	Power Ground.
C1	VIN	Power Input.
C2	SDA	Data of I <sup>2</sup> C.
C3	CF1	Negative Charge Pump Flying Capacitor Pin.
D1	LXP	Switching Node of Boost Converter.
D2	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
D3, E2	BST	Output Voltage of Boost Converter.
E3	VOP	Positive Terminal Output.

The block diagram illustrates the internal circuitry of the LDO and I2C interface. Key components include:

- Input and Protection:** VIN is connected to the UVLO (Under Voltage Lockout) block. The LXP and BST pins are connected to the OVP (Over Voltage Protection) block.
- Reference and Control:** A Bandgap Reference provides VREF to the PWM Logic and a GM (General Purpose Comparator). The PWM Logic drives the gate of N1, which is in series with P1. The OCP1 (Over Current Protection) block monitors the current through N1.
- Resistors and Feedback:** RP1 and RP2 are resistors in the feedback path. SCP1 (Short Circuit Protection) is connected to the output VOP.
- I2C Interface:** The I2C block is connected to ENP, ENNO, SCL, SDA, and PGND. It interfaces with the Fast Discharge block and the DAC.
- Charge Pump and Output:** The -1x Charge Pump is connected to the LDO output and the VON pin. The Soft-Start block controls the charge pump. The DAC is connected to the VREF pin and the output of the charge pump.
- Comparator and DAC:** The GM block compares the output voltage to VREF. The DAC is connected to the output of the GM block and the output of the charge pump.

interface. The RT4801A provides Over-Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from damage with abnormal operations. When the EN voltage is logic low for more than 375μs, the IC will be shut down with low input supply current less than 1μA.

**Absolute Maximum Ratings (Note 1)**

- Supply Input Voltage  $V_{IN}$  Pin ----- -0.3V to 6V
- Output Voltage VOP Pins----- -0.3V to 7V
- Output Voltage VON Pins ----- -7V to 0.3V
- Others Pin to GND ----- -0.3V to 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$   
 WL-CSP-15B 1.31x2.07 (BSC) ----- 2W
- Package Thermal Resistance (Note 2)  
 WL-CSP-15B 1.31x2.07 (BSC),  $\theta_{JA}$  ----- 49.8°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)  
 HBM (Human Body Model) ----- 2kV  
 MM (Machine Model) ----- 200V

**Recommended Operating Conditions (Note 4)**

- Supply Input Voltage ----- 2.5V to 5.5V
- Ambient Temperature Range----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

**Electrical Characteristics**

( $V_{IN} = 3.7\text{V}$ ,  $C_{IN} = C_{OP} = C_{F1} = 4.7\mu\text{F}$ ,  $C_{BST} = C_{ON} = 10\mu\text{F}$ ,  $L1 = 2.2\mu\text{H}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Power Supply</b>						
Input Voltage Range	$V_{IN}$		2.5	--	5.5	V
Under Voltage Lockout Threshold Voltage	$V_{UVLO\_H}$	$V_{IN}$ Rising	--	--	2.5	V
	$V_{UVLO\_L}$	$V_{IN}$ Falling	--	--	2.3	
Over-Temperature Protection	$T_{OTP}$	(Note 5)	--	140	--	°C
Over-Temperature Protection Hysteresis	$T_{OTP\_HYST}$	(Note 5)	--	15	--	°C
Shutdown Current	$I_{SHDN}$	$ENP = ENN = 0\text{V}$	--	--	1	$\mu\text{A}$
<b>Boost Converter</b>						
Boost Voltage Range	$V_{BST}$		4.15	--	6.2	V
Peak Current Limit	$I_{OCP}$		--	1	--	A
Boost Switching Frequency	$f_{OSC\_P}$		0.8	1	1.2	MHz
<b>LDO</b>						
Positive Output Voltage Range	$V_{OP}$		4		6	V
Positive Output Voltage Setting Range	$V_{OP\_SET}$	per step	--	100	--	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Output Voltage Accuracy		V <sub>OP_ACC</sub>		−1	--	1	%
Positive Output Current Capability		I <sub>OP_MAX</sub>		80	--	--	mA
Dropout Voltage		V <sub>OP_DROP</sub>	V <sub>BST</sub> = 5.4V, V <sub>OP</sub> = 5.4V, I <sub>OP</sub> = 100mA	--	--	150	mV
Line Regulation		ΔV <sub>LINE_OP</sub>	V <sub>IN</sub> = 2.5 to 5.5V, I <sub>OP</sub> = 40mA	--	2	--	mV
Load Regulation		ΔV <sub>LOAD_OP</sub>	ΔI <sub>OP</sub> = 80mA	--	3	--	%/A
Fast Discharge Resistance		R <sub>DISP</sub>		--	70	--	Ω
Negative Charge Pump							
Negative Output Voltage Range		V <sub>ON</sub>		−4	--	−6	V
Negative Output Voltage Setting Range		V <sub>ON_SET</sub>	per step	--	100	--	mV
Negative Output Voltage Accuracy		V <sub>ON_ACC</sub>		−1	--	1	%
Negative Output Current Capability		I <sub>ON_MAX</sub>		80	--	--	mA
Negative Charge Pump Switching Frequency		f <sub>OSC_N</sub>		0.8	1	1.2	MHz
Line Regulation		ΔV <sub>LINE_ON</sub>	V <sub>IN</sub> = 2.5 to 5.5V, I <sub>ON</sub> = 40mA	--	10	--	mV
Load Regulation		ΔV <sub>LOAD_ON</sub>	ΔI <sub>ON</sub> = 80mA	--	6	--	%/A
Fast Discharge Resistance		R <sub>DISN</sub>		--	20	--	Ω
Logic Input (ENP, ENN, SCL, SDA)							
Input Threshold Voltage	Logic-High	V <sub>IH</sub>	V <sub>IN</sub> = 2.5V to 5.5V	1.2	--	--	V
	Logic-Low	V <sub>IL</sub>	V <sub>IN</sub> = 2.5V to 5.5V	--	--	0.4	
ENP, ENN Pull-down Resistance		R <sub>EN</sub>		--	200	--	kΩ
SDA, SCL Sink Current		I <sub>IH</sub>	V <sub>SDA</sub> , V <sub>SCL</sub> = 3V	--	0.5	--	μA
SDA, SCL Logic Input Voltage	Low-Level	V <sub>SCL_L</sub>		--	--	0.4	V
	High-Level	V <sub>SCL_H</sub>		1.2	--	--	
SCL Clock Frequency		f <sub>CLK</sub>		--	--	400	kHz
Output Fall Time		t <sub>FL2COUT</sub>		--	--	250	ns
Bus Free Time Between Stop/Start		t <sub>BUF</sub>		1.3	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hold Time Start Condition	t <sub>HD,STA</sub>		0.6	--	--	μs
Setup Time for Start Condition	t <sub>SU,STA</sub>		0.6	--	--	μs
SCL Low Time	t <sub>LOW</sub>		1.3	--	--	μs
SCL High Time	t <sub>HIGH</sub>		0.6	--	--	μs
Data Setup Time	t <sub>SU,DAT</sub>		100	--	--	ns
Data Hold Time	t <sub>HD,DAT</sub>		0	--	900	ns
Setup Time for Stop Condition	t <sub>SU,STO</sub>		0.6	--	--	μs

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.**  $T_{OTP}$ ,  $T_{OTP\_HYST}$  are guaranteed by design.

# Typical Application Circuit

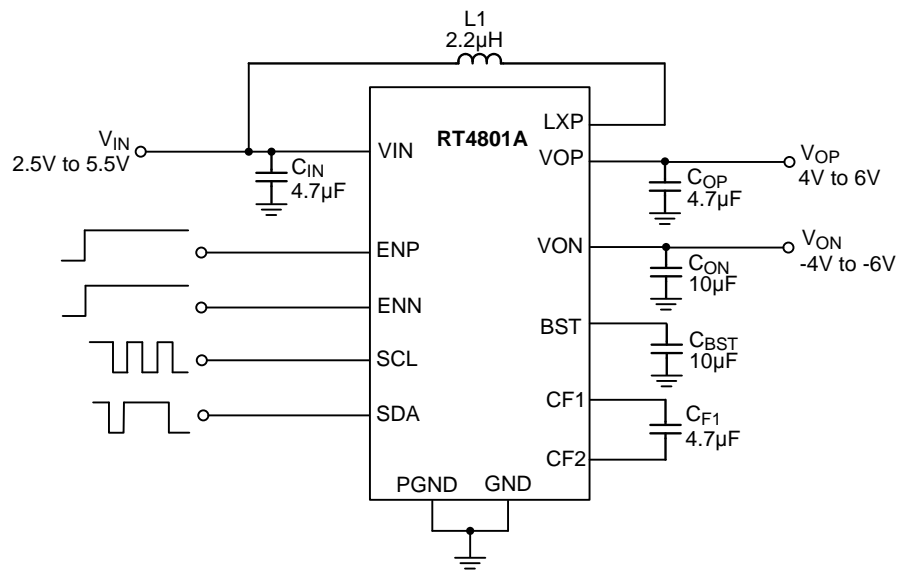
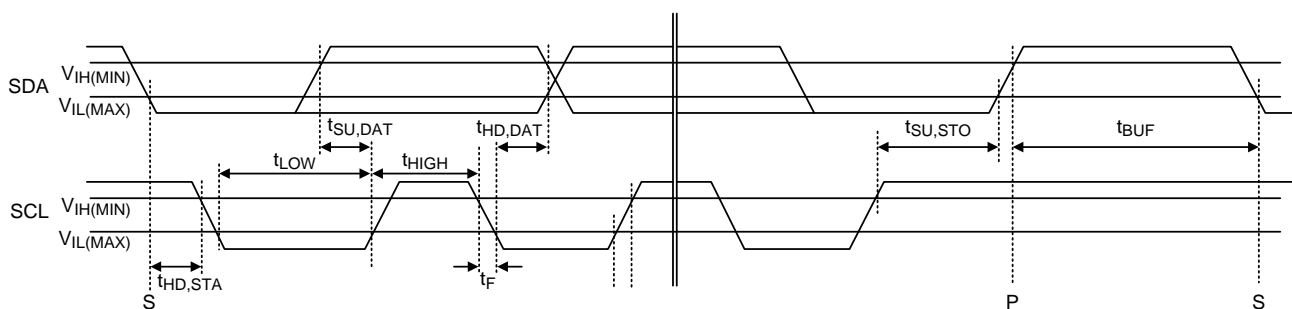


Table 1. Component List of Evaluation Board

Reference	Qty.	Part Number	Description	Package	Supplier
CIN, COP, CF1	1	GRM188R61C475KAAJ	4.7µF/16V/X5R	0603	Murata
CBST, CON	1	GRM188R61C106KAAL	10µF/16V/X5R	0603	Murata
L1	1	1269AS-H-4R7N = P2	2.2µH/130mΩ	2.5mm x 2.0mm x 1.0mm	Toko

I<sup>2</sup>C Interface



## I<sup>2</sup>C Command

### Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
0	1	1	1	1	1	0	R/W

### Write Command

(a) Write single byte of data to Register

Slave Address									Register Address									Data From Master										
Start	0	1	1	1	1	1	0	0	Slave ACK	R7	R6	R5	R4	R3	R2	R1	R0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK	Stop

(b) Write multiple bytes of data to Registers

Slave Address								Register Address n <sub>th</sub>											n <sub>th</sub> Data From Master										
Start	0	1	1	1	1	1	0	0	Slave ACK	R7	R6	R5	R4	R3	R2	R1	R0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK		
										(n + 1) <sub>th</sub> Data From Master											Last Data From Master								
										D7 D6 D5 D4 D3 D2 D1 D0 Slave ACK											D7 D6 D5 D4 D3 D2 D1 D0 Slave ACK Stop								

### Read Command

(a) Read single byte of data from Register

Slave Address								Register Address																	
Start	0	1	1	1	1	1	0	0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK							

Slave Address									Data From Master										
Re-start	0	1	1	1	1	1	0	1	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Master NACK	Stop

(b) Read multiple bytes of data from Registers

Slave Address									Register Address										
Start	0	1	1	1	1	1	0	0	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Slave ACK	

Slave Address									$n^{\text{th}}$ Data From Master											Last Data From Master										
Re-start	0	1	1	1	1	1	0	1	Slave ACK	D7	D6	D5	D4	D3	D2	D1	D0	Master ACK	.....	D7	D6	D5	D4	D3	D2	D1	D0	Master NACK	Stop	

Start : Start command

ACK : Acknowledge = L active

R7 to R0 : Register Address.

D7 to D0 : Write data when WRITE command or read data when READ command

VOP : Register address = 0X00h

Stop : Stop command

VON : Register address = 0X01h

DISP : Register address = 0x03h

DISN : Register address = 0x03h

R/W : Read active (R/W = H) or Write active (R/W = L)

## Registers Map

Table 2. VOP Voltage Selection

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VOP(V)
VOP	00h	00h	Reserved	Reserved	Reserved	0	0	0	0	0	4
VOP	00h	01h	Reserved	Reserved	Reserved	0	0	0	0	1	4.1
VOP	00h	02h	Reserved	Reserved	Reserved	0	0	0	1	0	4.2
VOP	00h	03h	Reserved	Reserved	Reserved	0	0	0	1	1	4.3
VOP	00h	04h	Reserved	Reserved	Reserved	0	0	1	0	0	4.4
VOP	00h	05h	Reserved	Reserved	Reserved	0	0	1	0	1	4.5
VOP	00h	06h	Reserved	Reserved	Reserved	0	0	1	1	0	4.6
VOP	00h	07h	Reserved	Reserved	Reserved	0	0	1	1	1	4.7
VOP	00h	08h	Reserved	Reserved	Reserved	0	1	0	0	0	4.8
VOP	00h	09h	Reserved	Reserved	Reserved	0	1	0	0	1	4.9
VOP	00h	0Ah	Reserved	Reserved	Reserved	0	1	0	1	0	5
VOP	00h	0Bh	Reserved	Reserved	Reserved	0	1	0	1	1	5.1
VOP	00h	0Ch	Reserved	Reserved	Reserved	0	1	1	0	0	5.2
VOP	00h	0Dh	Reserved	Reserved	Reserved	0	1	1	0	1	5.3
VOP	00h	0Eh	Reserved	Reserved	Reserved	0	1	1	1	0	5.4
VOP	00h	0Fh	Reserved	Reserved	Reserved	0	1	1	1	1	5.5
VOP	00h	10h	Reserved	Reserved	Reserved	1	0	0	0	0	5.6
VOP	00h	11h	Reserved	Reserved	Reserved	1	0	0	0	1	5.7
VOP	00h	12h	Reserved	Reserved	Reserved	1	0	0	1	0	5.8
VOP	00h	13h	Reserved	Reserved	Reserved	1	0	0	1	1	5.9
VOP	00h	14h	Reserved	Reserved	Reserved	1	0	1	0	0	6

Table 3. VON Voltage Selection

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON(V)
VON	01h	00h	Reserved	Reserved	Reserved	0	0	0	0	0	-4
VON	01h	01h	Reserved	Reserved	Reserved	0	0	0	0	1	-4.1
VON	01h	02h	Reserved	Reserved	Reserved	0	0	0	1	0	-4.2
VON	01h	03h	Reserved	Reserved	Reserved	0	0	0	1	1	-4.3
VON	01h	04h	Reserved	Reserved	Reserved	0	0	1	0	0	-4.4
VON	01h	05h	Reserved	Reserved	Reserved	0	0	1	0	1	-4.5
VON	01h	06h	Reserved	Reserved	Reserved	0	0	1	1	0	-4.6
VON	01h	07h	Reserved	Reserved	Reserved	0	0	1	1	1	-4.7
VON	01h	08h	Reserved	Reserved	Reserved	0	1	0	0	0	-4.8
VON	01h	09h	Reserved	Reserved	Reserved	0	1	0	0	1	-4.9
VON	01h	0Ah	Reserved	Reserved	Reserved	0	1	0	1	0	-5
VON	01h	0Bh	Reserved	Reserved	Reserved	0	1	0	1	1	-5.1
VON	01h	0Ch	Reserved	Reserved	Reserved	0	1	1	0	0	-5.2

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON(V)
VON	01h	0Dh	Reserved	Reserved	Reserved	0	1	1	0	1	-5.3
VON	01h	0Eh	Reserved	Reserved	Reserved	0	1	1	1	0	-5.4
VON	01h	0Fh	Reserved	Reserved	Reserved	0	1	1	1	1	-5.5
VON	01h	10h	Reserved	Reserved	Reserved	1	0	0	0	0	-5.6
VON	01h	11h	Reserved	Reserved	Reserved	1	0	0	0	1	-5.7
VON	01h	12h	Reserved	Reserved	Reserved	1	0	0	1	0	-5.8
VON	01h	13h	Reserved	Reserved	Reserved	1	0	0	1	1	-5.9
VON	01h	14h	Reserved	Reserved	Reserved	1	0	1	0	0	-6

**Table 4. VOP Active Discharge**

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VOP Discharge
DISP	03h	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0	DISN	W/O
DISP	03h	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	DISN	W

**Table 5. VON Active Discharge**

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VON Discharge
DISN	03h	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DISP	0	W/O
DISN	03h	01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DISP	1	W

The Reserved bits are ignored when written and return either 0 or 1 when read.

**Table 6. Application**

Name	Register Address	DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Application
APPS	03h	00h	Reserved	0	Reserved	Reserved	Reserved	Reserved	DISP	DISN	Tablet
APPS	03h	40h	Reserved	1	Reserved	Reserved	Reserved	Reserved	DISP	DISN	Smartphone

The Reserved bits are ignored when written and return either 0 or 1 when read.

**Factory Default Register Value**

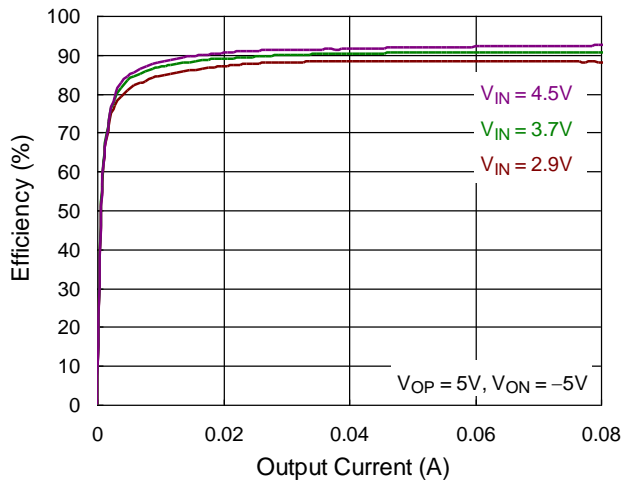
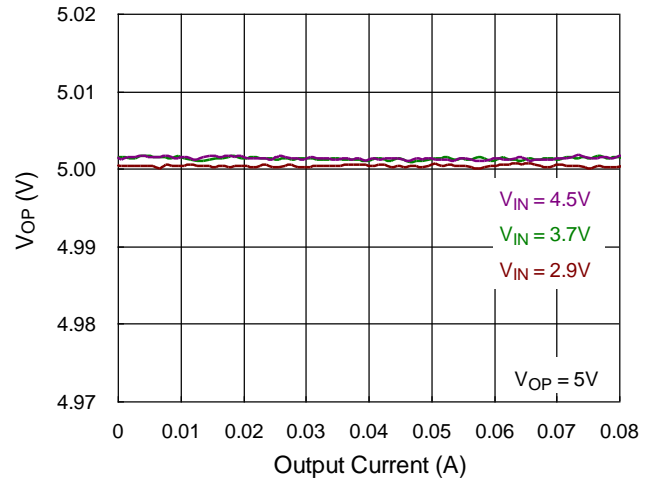
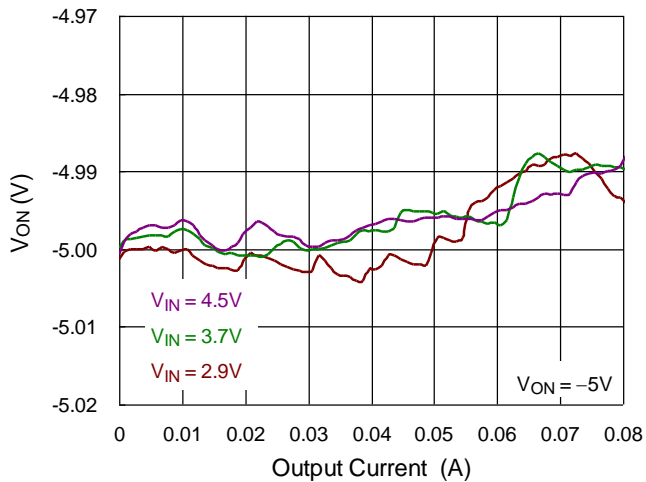
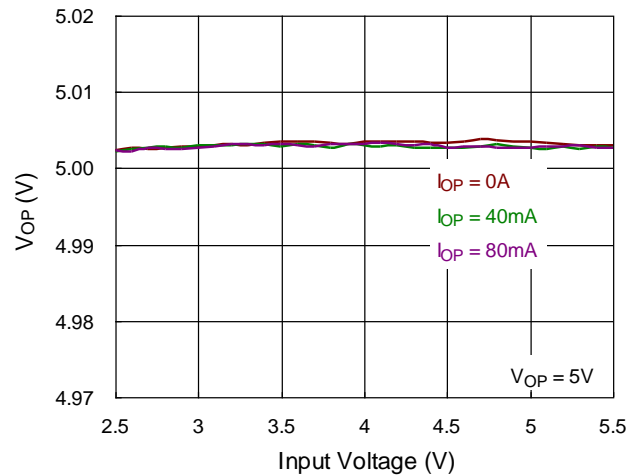
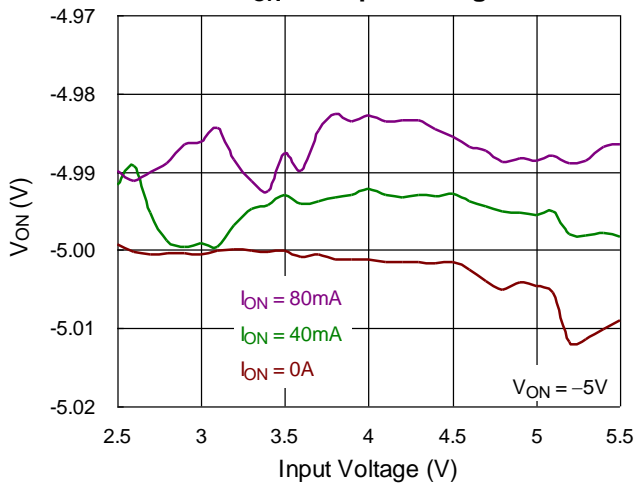
Name	Register Address	DATA
VOP	00h	0Ah / 14h
VON	01h	0Ah / 14h
DISP	03h	43h
DISN	03h	43h
APPS	03h	43h

RT4801A-50WSC default VOP/VON DATA is 0Ah/0Ah.

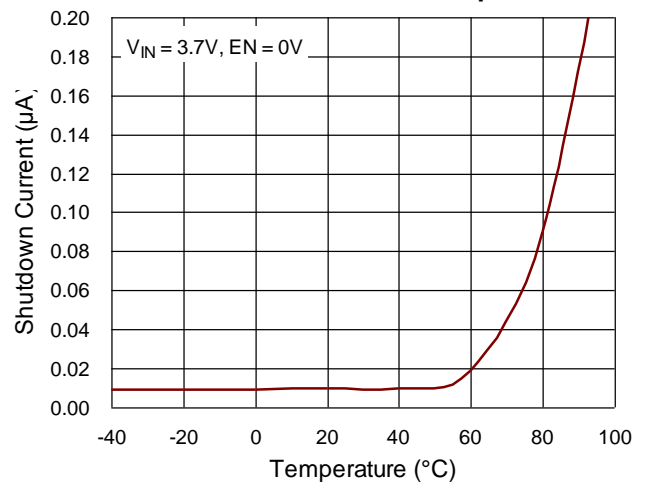
RT4801A-60WSC default VOPN/VON DATA is 14h/14h.

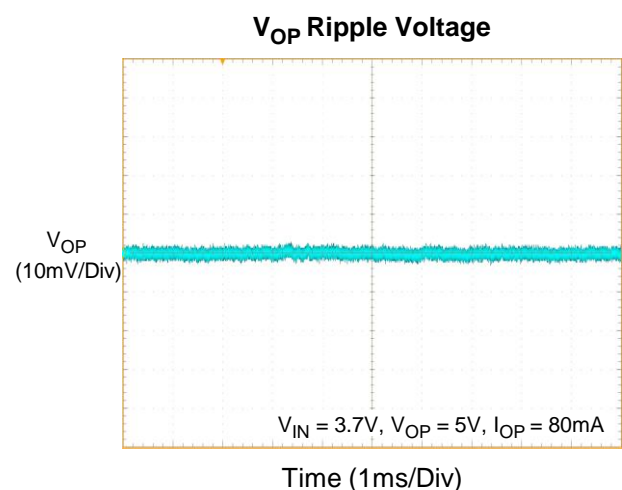
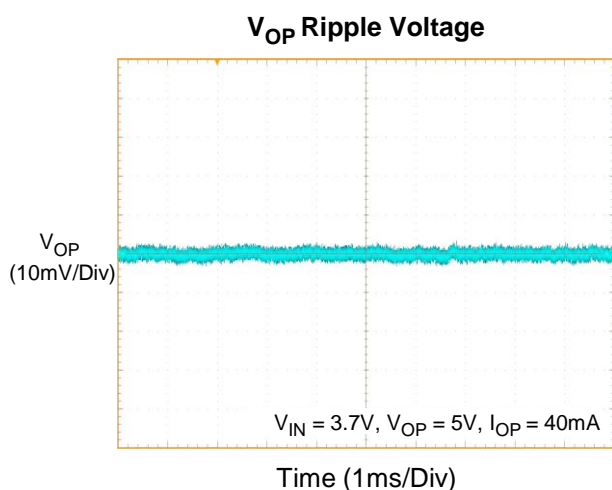
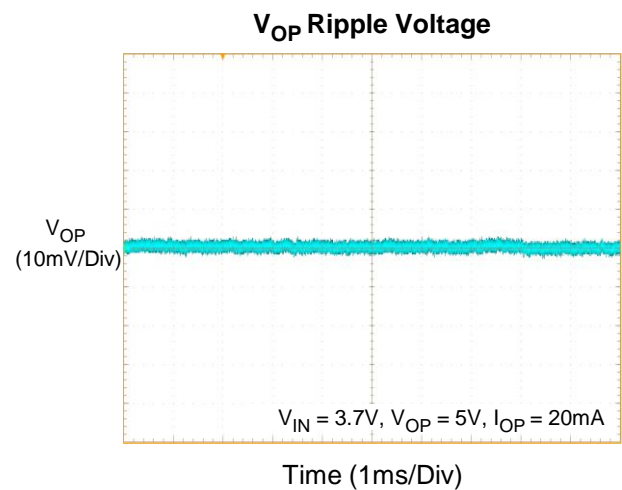
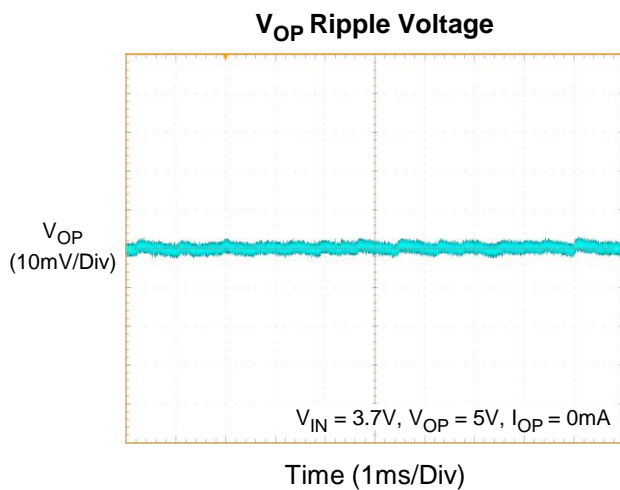
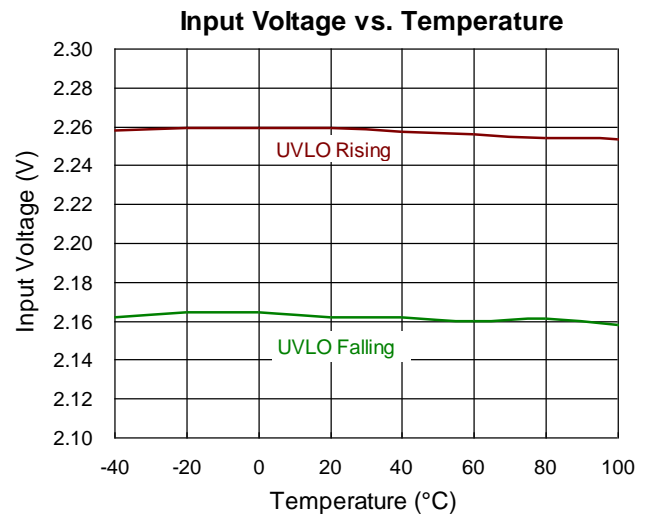
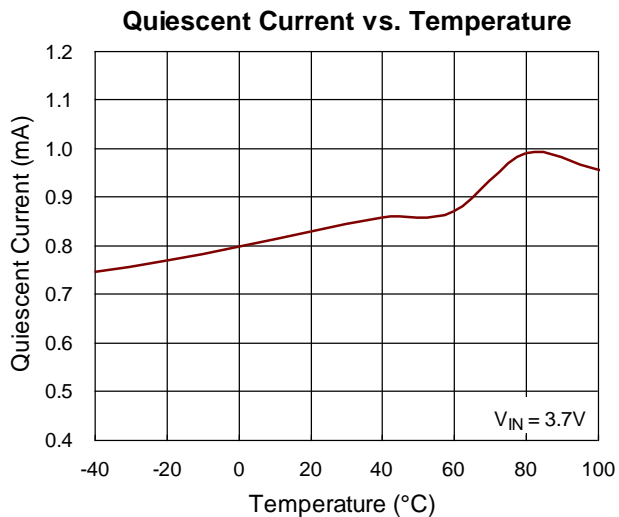
## Typical Operating Characteristics

Efficiency vs. Output Current

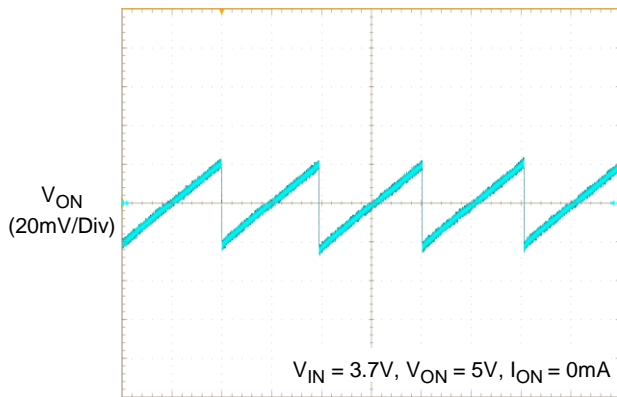
 $V_{OP}$  vs. Output Current $V_{ON}$  vs. Output Current $V_{OP}$  vs. Input Voltage $V_{ON}$  vs. Input Voltage

Shutdown Current vs. Temperature



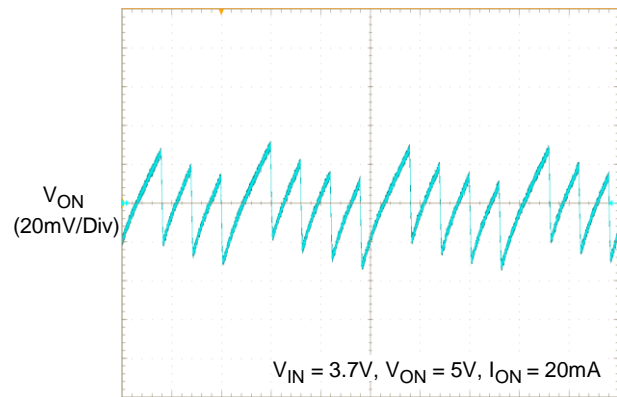


**V<sub>ON</sub> Ripple Voltage**



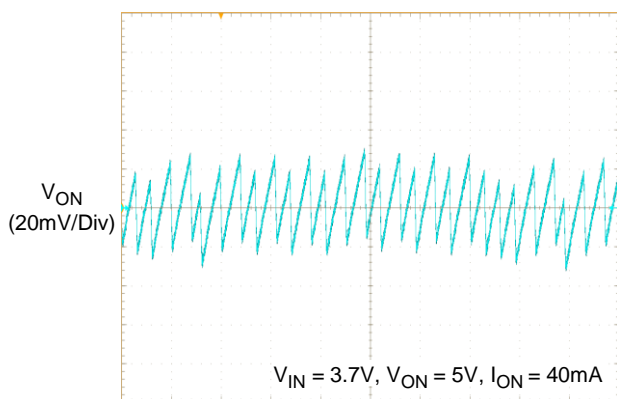
Time (1ms/Div)

**V<sub>ON</sub> Ripple Voltage**



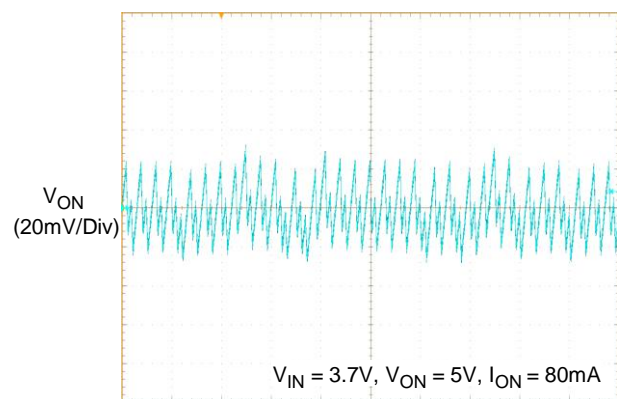
Time (10μs/Div)

**V<sub>ON</sub> Ripple Voltage**



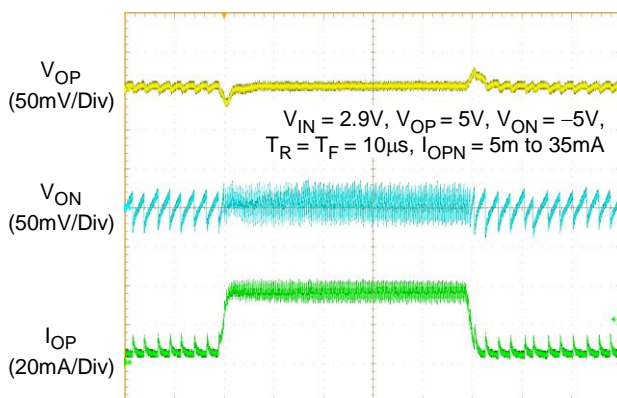
Time (10μs/Div)

**V<sub>ON</sub> Ripple Voltage**



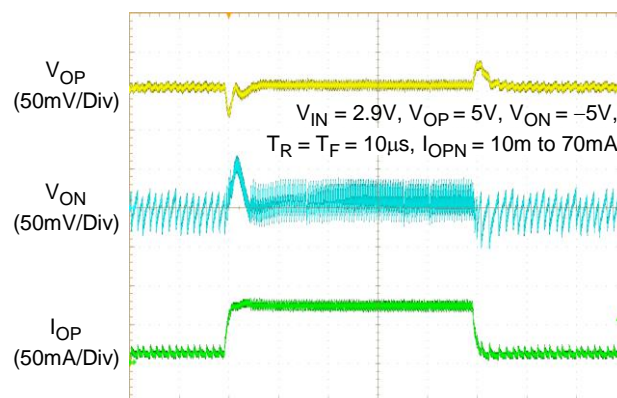
Time (10μs/Div)

**Load Transient**



Time (100μs/Div)

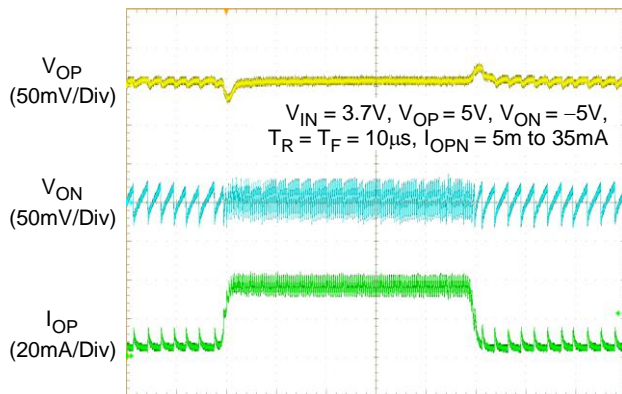
**Load Transient**



Time (100μs/Div)

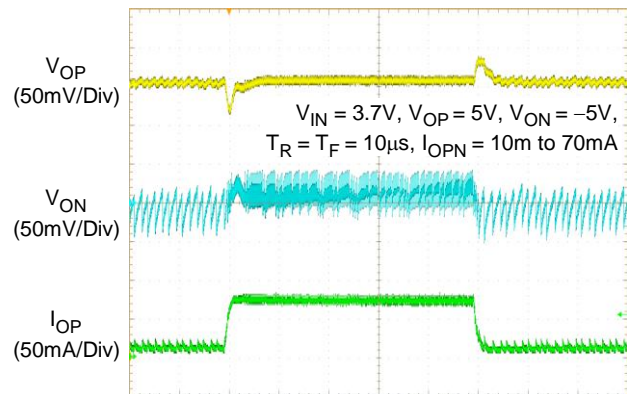


Load Transient



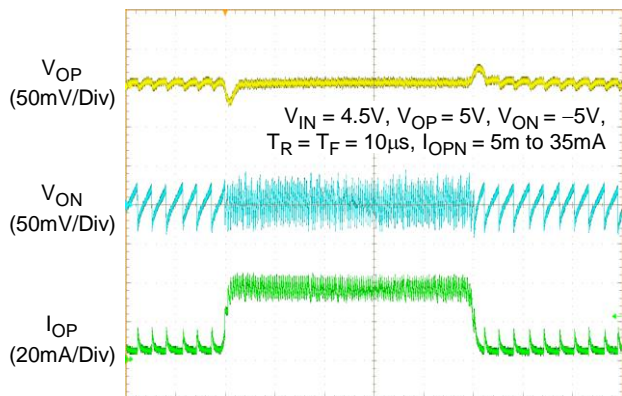
Time (100 $\mu s$ /Div)

Load Transient



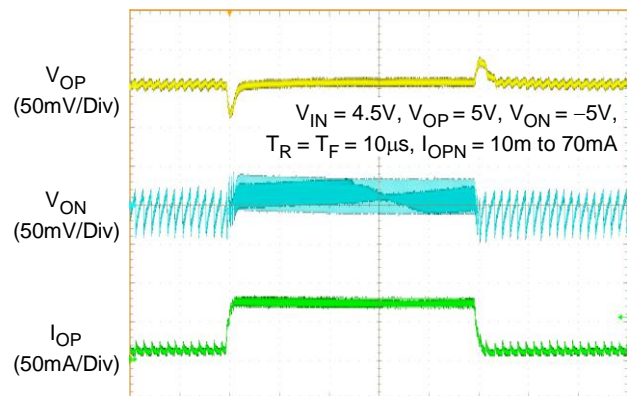
Time (100 $\mu s$ /Div)

Load Transient



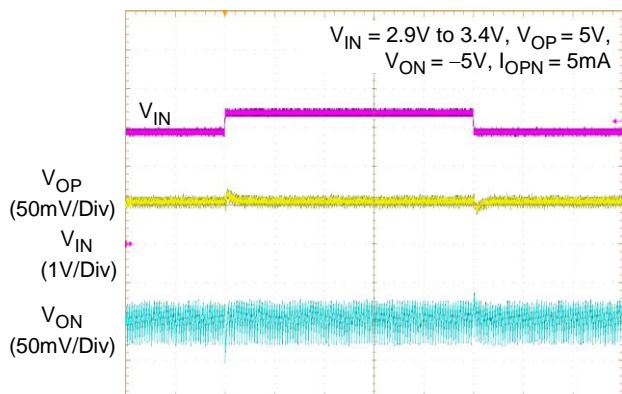
Time (100 $\mu s$ /Div)

Load Transient



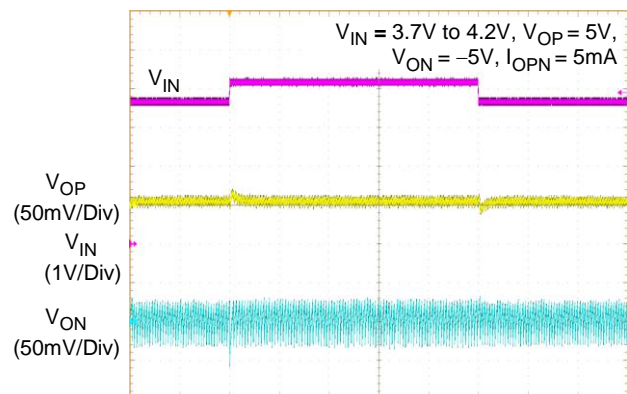
Time (100 $\mu s$ /Div)

Line Transient



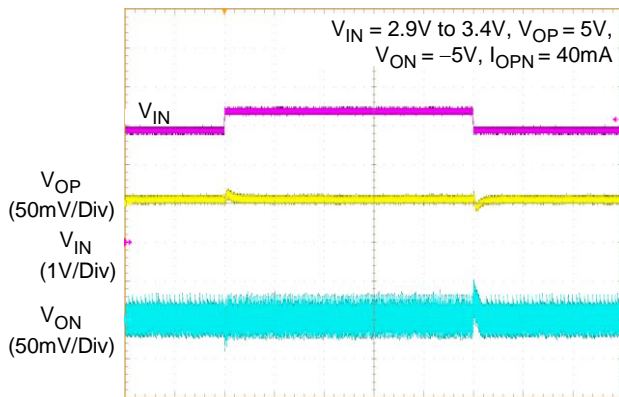
Time (500 $\mu s$ /Div)

Line Transient



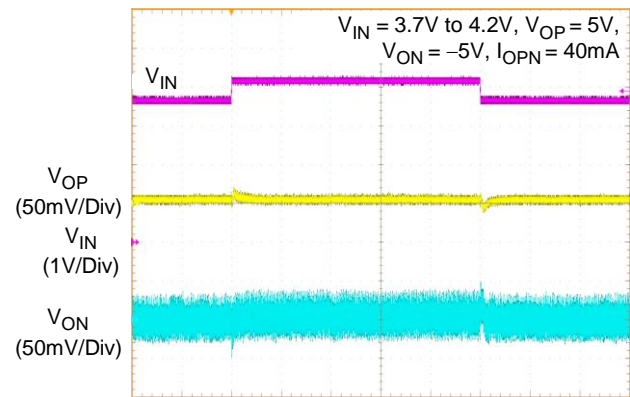
Time (500 $\mu s$ /Div)

### Line Transient



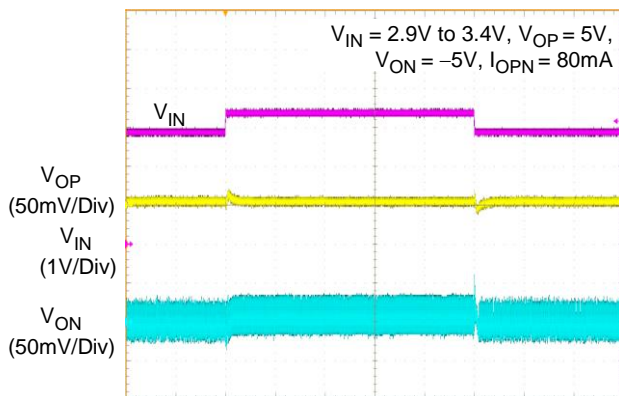
Time (500 $\mu$ s/Div)

### Line Transient



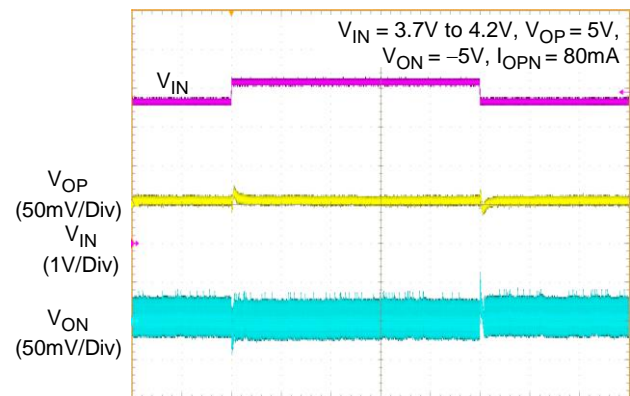
Time (500 $\mu$ s/Div)

### Line Transient



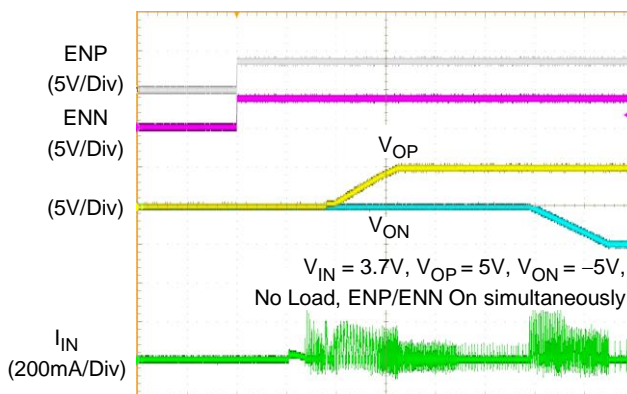
Time (500 $\mu$ s/Div)

### Line Transient



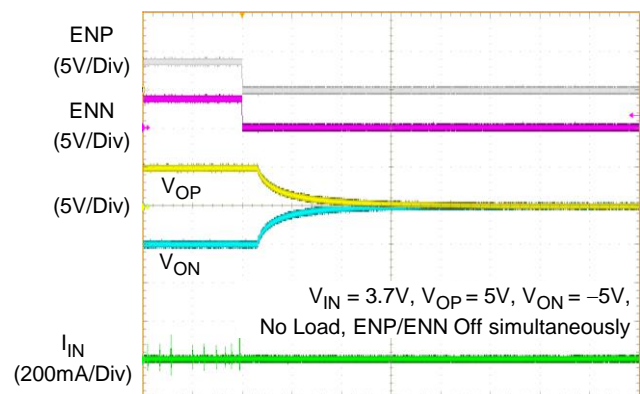
Time (500 $\mu$ s/Div)

### Power On



Time (1ms/Div)

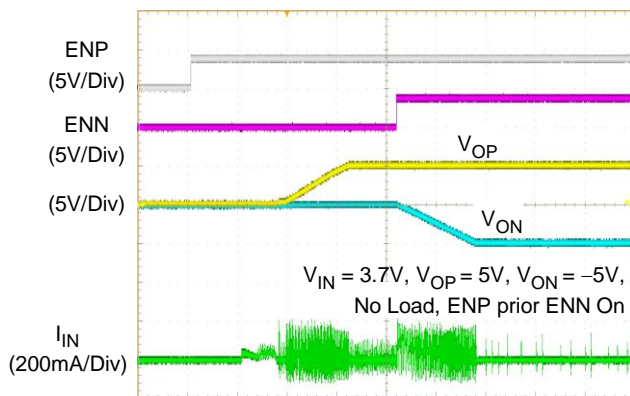
### Power Off



Time (1ms/Div)

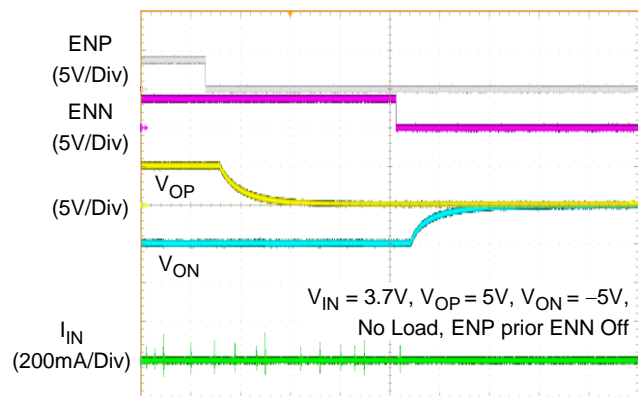


Power On



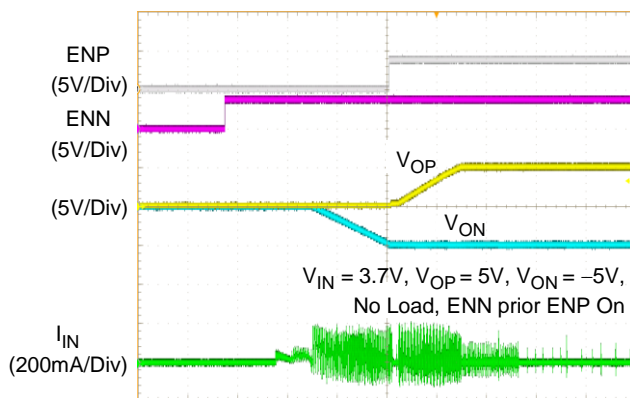
Time (1ms/Div)

Power Off



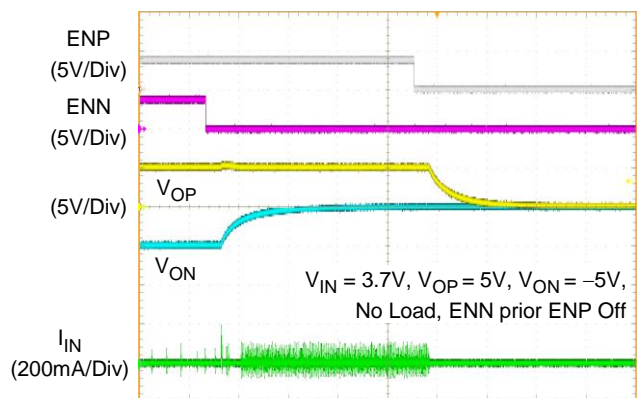
Time (1ms/Div)

Power On



Time (1ms/Div)

Power Off



Time (1ms/Div)

## Application Information

The RT4801A is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltages for LCD panel bias or consumer products. It can support input voltage range from 2.5V to 5.5V and the output current up to 80mA. The V<sub>OP</sub> positive output voltage is generated from the LDO supplied from a synchronous Boost converter, and V<sub>OP</sub> is set at a typical value of 6V. The Boost converter output also drives an inverting charge pump controller to generate V<sub>ON</sub> negative output voltage which is set at a typical value of -6V. Both positive and negative voltages can be programmed by a MCU through the dedicated I<sup>2</sup>C interface and the available voltage range is from ±4V to ±6V with 100mV per step.

### Input Capacitor Selection

Input ceramic capacitor with 4.7μF capacitance is suggested for applications. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their wider voltage and temperature ranges.

### Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where  $\eta$  is the efficiency of the VOP Boost converter,  $I_{IN(MAX)}$  is the maximum input current, and  $\Delta I_L$  is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than  $I_{PEAK}$ .

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where  $f_{OSC}$  is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

### Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating IC performance. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1,  $\Delta V_{OUT1}$  can be evaluated based on the ideal energy equalization. According to the definition of Q, the  $\Delta V_{OUT1}$  value can be calculated as the following equation :

$$Q = I_{OUT} \times D \times \frac{1}{f_{SOC}} = C_{OUT} \times \Delta V_{OUT1}$$

$$\Delta V_{OUT1} = \frac{I_{OUT} \times D}{f_{SOC} \times C_{OUT}}$$

where  $f_{OSC}$  is the switching frequency and D is the duty cycle.

Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{SER} + \frac{I_{OUT} \times D}{f_{OSC} \times C_{OUT}}$$

where  $\Delta V_{ESR} = I_{C_{rms}} \times R_{CESR}$

The output capacitor,  $C_{OUT}$ , should be selected accordingly.

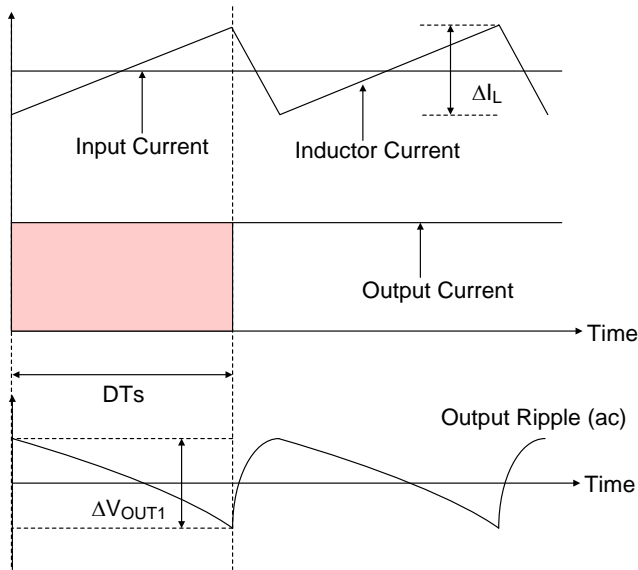


Figure 1. The Output Ripple Voltage without the Contribution of ESR

### Under Voltage Lockout

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down IC operation when input voltage is lower than the specified threshold voltage.

### Soft-Start

The RT4801A employs an internal soft-start feature to avoid high inrush current during start-up. The soft-start function is achieved by clamping the output voltage of the internal error amplifier with another voltage source that is increased slowly from zero to near VIN during the soft-start period.

### Output Voltage Setting

The output voltage can be programmed by a MCU through the dedicated I<sup>2</sup>C interface according to the V<sub>OP</sub>/V<sub>ON</sub> Voltage Selection Table.

### Shutdown Delay and Discharge

When the EN signal is logic low for more than 375μs, the IC function will be shut down. The output V<sub>OP</sub>/V<sub>ON</sub> can be actively discharged to GND via discharge selection bit enabled. In shutdown mode, the input supply current for the IC is less than 1μA.

### Over Current Protection

The RT4801A includes a cycle-by-cycle current limit function which monitors the inductor current during each ON period. The power switch will be forced off to avoid large current damage once the current is over the limit level.

### Short Circuit Protection

The RT4801A has an advanced output short-circuit protection mechanism which prevents the IC from damage by unexpected applications. When the output becomes shorted to ground, and the output voltage is under the limit level with 1ms (typ.) duration, the LCD bias function enters shutdown mode and can only re-start normal operation after triggering the ENP/ENN pin.

### Over Temperature Protection

The RT4801A equips an over temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down LCD bias operation when ambient temperature exceeds 140°C. Once the ambient temperature cools down by approximately 15°C, IC will automatically resume normal operation. To maintain continuous operation, the maximum junction temperature should be prevented from rising above 125°C.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where T<sub>J(MAX)</sub> is the maximum junction temperature, T<sub>A</sub> is the ambient temperature, and θ<sub>JA</sub> is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ<sub>JA</sub>, is layout dependent. For WL-CSP-15B 1.31x2.07 (BSC) package, the thermal resistance, θ<sub>JA</sub>, is 49.8°C/W on a standard JEDEC 51-7 four-layer thermal test board.

The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (49.8^\circ\text{C/W}) = 2\text{W} \text{ for WL-CSP-15B } 1.31 \times 2.07 \text{ (BSC) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(\text{MAX})}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

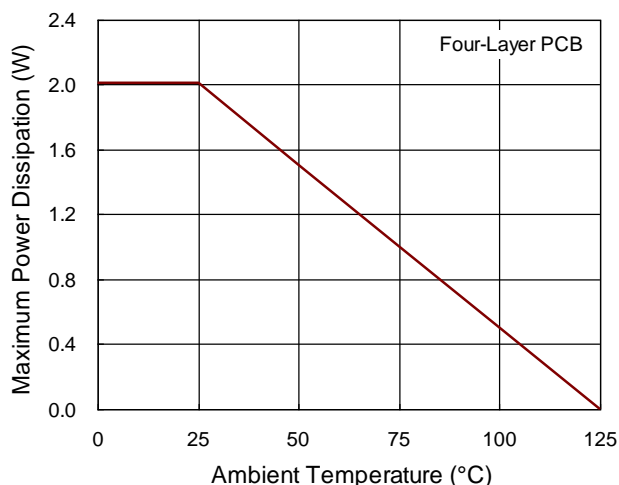


Figure 2. Derating Curve of Maximum Power Dissipation

### Layout Considerations

For the best performance of RT4801A, the following PCB layout guidelines should be strictly followed.

- ▶ For good regulation, place the power components as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- ▶ The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- ▶ The flying capacitor should be placed as close to the CF1/CF2 pin as possible to avoid noise injection.
- ▶ Minimize the size of the LXP node and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LXP or high-current traces.
- ▶ Separate power ground (PGND) and analog ground (GND). Connect the GND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes

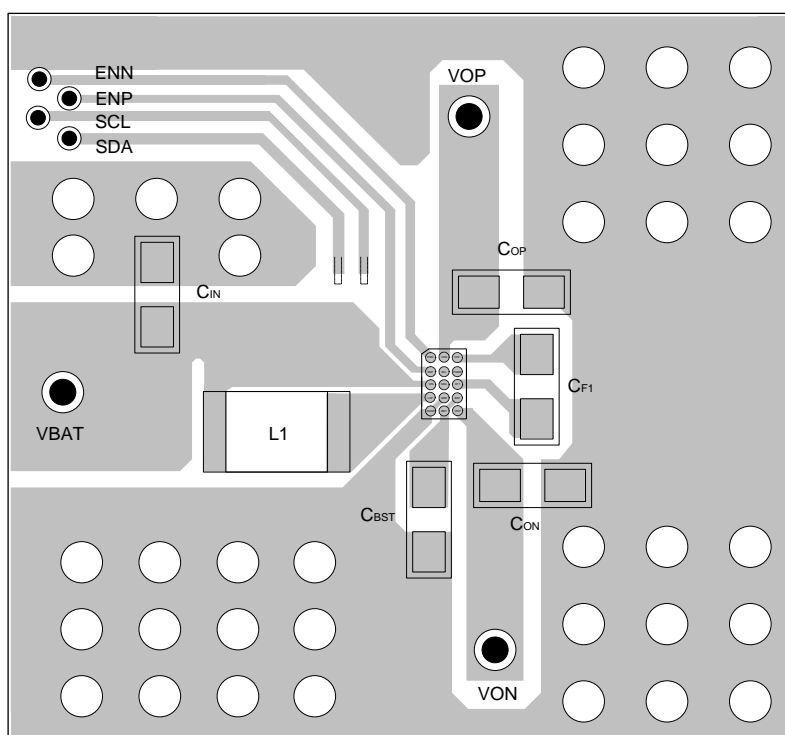
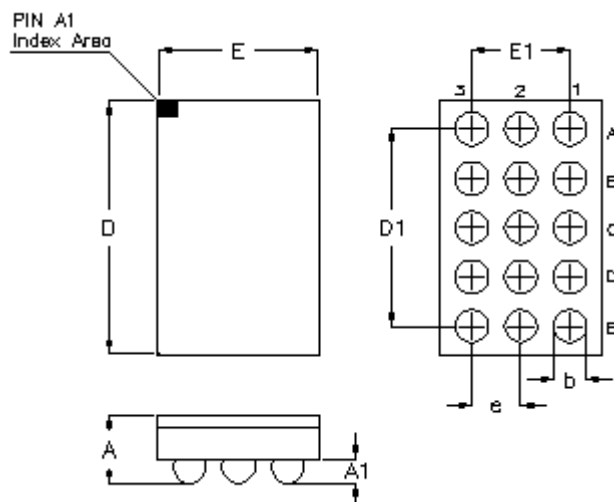


Figure 3. PCB Layout Guide

## **Outline Dimension**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.020	2.120	0.080	0.083
D1	1.600		0.063	
E	1.260	1.360	0.050	0.054
E1	0.800		0.031	
e	0.400		0.016	

### **WL-CSP-15B 1.31x2.07 (BSC)**

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