7+3 Channel DC-DC Converters with RTC and I²C Interface

General Description

RT5035A/B is a highly-integrated DSC Power Management IC that contains 7ch switching DC-DC converters and two generic LDOs, one keep-alive low-quiescent LDO for RTC, one load switch with soft-start control and current limit, a switch with reverse leakage prevention for backup battery, and a Real-Time-Clock (RTC) including time counter and 32768Hz oscillator. The DC-DC converters are one low-voltage Step-Up operated in either Async-PFM or Sync-PWM, one current mode Sync Step-Up/Down (Buck-Boost), four Sync Step-Down, and one Asyn Step-Up for WLED driver. All power MOS are integrated. And compensation networks are built in. RT5035A/B uses I²C interface to set power-on and power-off timing, output voltage, and WLED current and dimming level, and also access RTC time counters and oscillator fine-tuning. RT5035A/B dedicate for CMOS image sensor application by providing one Sync Step-Down, one LDO, and one load switch. The RT5035A/B also provides rich protection functions include Over-Current Protection, Under-Voltage Protection, Over-Voltage Protection, Over-Temperature Protection, and Over-Load Protection. RT5035A/B is available in WQFN-40L 5x5 package.

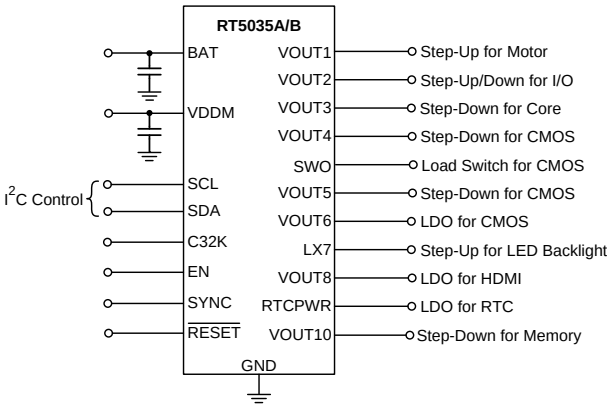
Applications

- Digital Cameras
- Portable Instruments

Features

- **CH1 Sync Step-Up in PWM Mode or Async Step-Up in Pulse Frequency Mode**
- **CH2 Current Mode Sync Step-Up/Down**
- **CH3/CH4/CH5 Current Mode Sync Step-Down**
- **SW4 Load Switch with Soft-Start Inrush Control And Current Limit**
- **CH6 Generic Low Voltage LDO for CMOS Sensor**
- **CH7 WLED Driver in Async Step-Up Mode**
- **Open LED Protection**
- **32 Dimming Levels**
- **CH8 Generic Low Voltage LDO for Multiple Purpose Power Supply**
- **CH9 Keep-Alive Low-Quiescent LDO**
- **CH10 Sync Step-Down or Async Step-down in Pulse Frequency Mode for Memory Standby Mode Application**
- **LV Sync Step-Down DC-DC Converter High Efficiency Up to 95%**
- **100% (Max) Duty Cycle for CH3, CH4, CH5 &CH10**
- **I²C Control Interface to Program Enable, Power On/Off Delay Time, Output Regulated Voltage, WLED Dimming Current**
- **RTC Timer And Oscillator**
- **Fixed 2MHz Switching Frequency for CH1, CH3, CH4, CH5, CH10**
- **Fixed 1MHz Switching Frequency for CH2, CH7**

Simplified Application Circuit



Ordering Information

RT5035A/B □□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- A : Li-ion
  B : 2AA Alkaline

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT5035AGQW

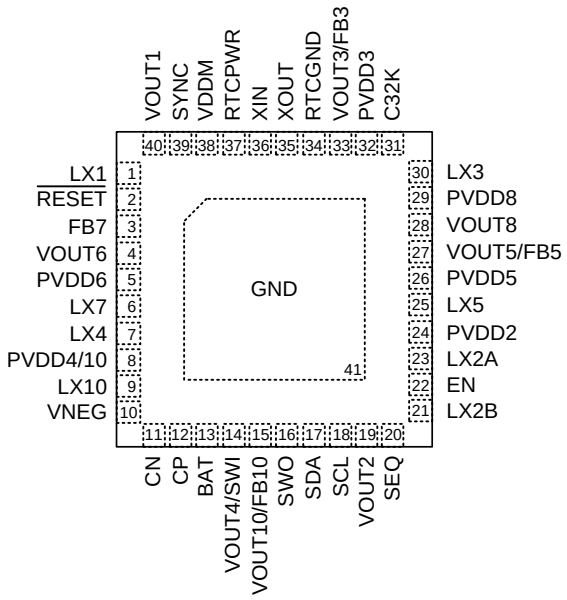
RT5035AGQW : Product Number
YMDNN : Date Code

RT5035BGQW

RT5035BGQW : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

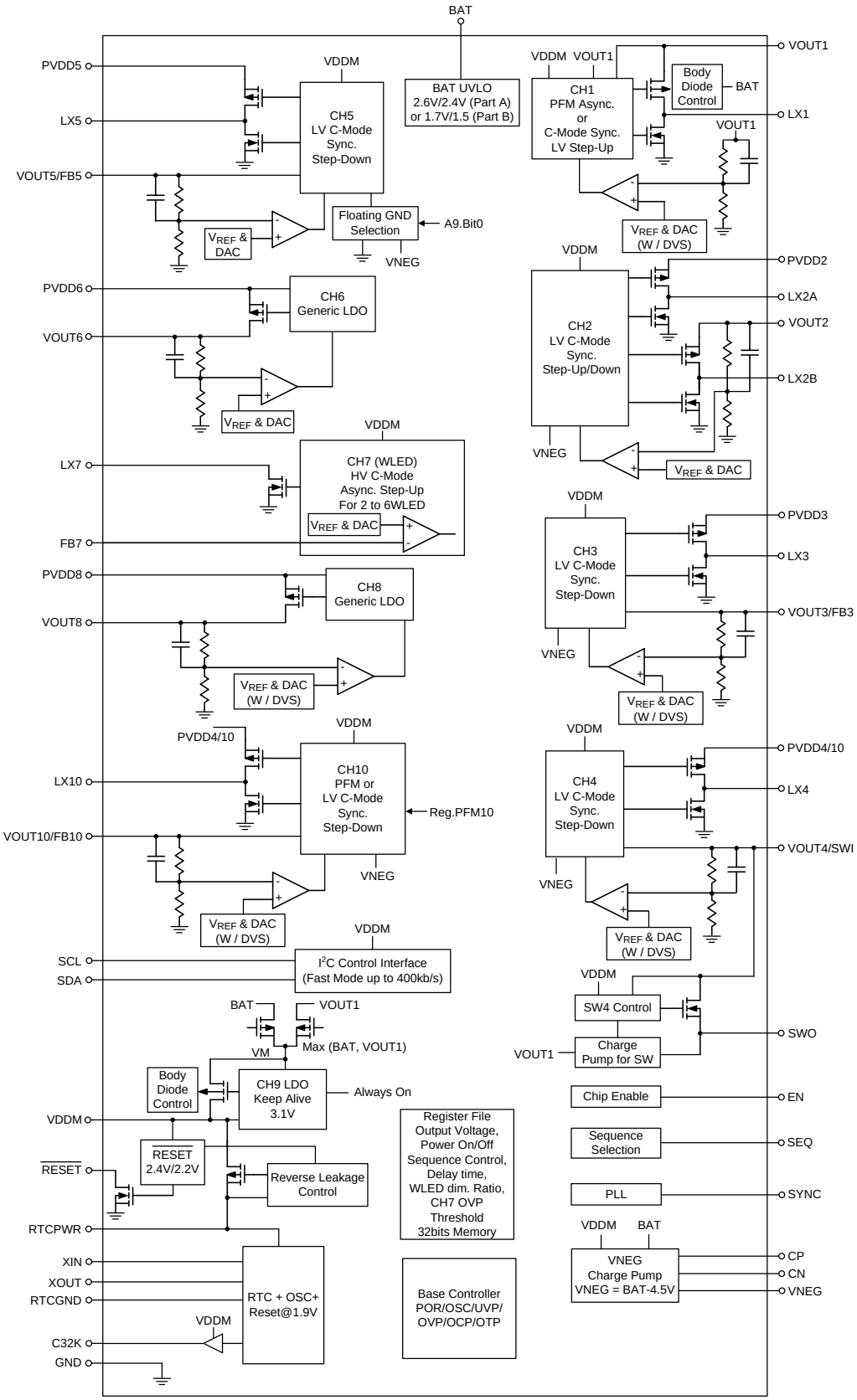
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX1	Switch node of CH1. This pin is in high impedance during shutdown.
2	$\overline{\text{RESET}}$	Open drain output port to assert the status of monitored VDDM voltage.
3	FB7	Feedback input pin for CH7. This pin is in high impedance during shutdown.
4	VOUT6	Regulated output node of CH6 generic LDO. When turning off, RT5035A/B would discharge CH6 output capacitors internally till VOUT6 < 0.1V. This pin is in high impedance during shutdown.
5	PVDD6	Power input of CH6 generic LDO. This pin is in high impedance during shutdown.
6	LX7	Switch node of CH7. This pin is in high impedance during shutdown.
7	LX4	Switch node of CH4. This pin is in high impedance during shutdown.
8	PVDD4/10	Power input pin of CH4 and CH10. This pin is in high impedance during shutdown.

Pin No.	Pin Name	Pin Function
9	LX10	Switch node of CH10. This pin is in high impedance during shutdown.
10	VNEG	Output node of negative charge pump to enhance CH2 (PVDD2 – LX2A), CH3, CH4, CH5, CH10 PMOS driving. The regulated voltage is the higher one between (BAT – 4.5V) and (–BAT). When the negative charge pump is off, VNEG is internally connected to GND. Connect this pin to an external 1μF capacitor.
11	CN	Negative switch node of charge pump. A fly capacitor is needed between pin CP and CN.
12	CP	Positive switch node of charge pump.
13	BAT	Battery power input and sense pin. Recommend that input bypass capacitors are as close as possible to the IC. The IC would sense the voltage of this pin for UVLO and perform body-diode direction control of CH1 PMOS switches. This pin is also the power input pin of negative charge pump circuit for VNEG.
14	VOUT4/SWI	Sense pin for CH4 output voltage and power pin for load switch SW4. When turning off, RT5035A/B would discharge CH4 output capacitors internally till VOUT4 < 0.1V. Recommend that output capacitors are as close to RT5035A/B as possible. This pin is in high impedance during shutdown.
15	VOUT10/FB10	Sense pin of CH10 output voltage. This pin is also the feedback pin for VOUT10 if I^2C is set to use the external resistor. When turning off, the IC discharges CH10 output capacitors internally until VOUT10 < 0.1V. Recommend that output capacitors are as close as possible to the IC. This pin is in high impedance during shutdown.
16	SWO	Power switch output pin of load switch SW4. When turning off, RT5035A/B would discharge SWO output capacitors internally. This pin is in high impedance during shutdown.
17	SDA	Data input and output pin for the I^2C serial port.
18	SCL	Clock input pin for the I^2C serial port.
19	VOUT2	Power output pin for CH2 output voltage. When turning off, RT5035A/B would discharge CH2 output capacitors internally till VOUT2 < 0.1V. I^2C interface power level must be equal to CH2 output voltage. This pin is in high impedance during shutdown.
20	SEQ	Sequence setting pin.
21	LX2B	Switch node B of CH2. This pin is in high impedance during shutdown.
22	EN	Enable input pin to activate the RT5035A/B power on (EN = High) and off. RT5035A/B includes an internal pull-low at EN pin.
23	LX2A	Switch node A of CH2. This pin is in high impedance during shutdown.
24	PVDD2	Power input pin of CH2 and it must connect to the same node as BAT. This pin is in high impedance during shutdown.
25	LX5	Switch node of CH5. This pin is in high impedance during shutdown.
26	PVDD5	Power input pin of CH5. PVDD5 could be separated from BAT. And the logic low level for PMOS is automatically selected. (VNEG or GND) This pin is in high impedance during shutdown.
27	VOUT5/FB5	Sense pin of CH5 Output Voltage. This pin is also the feedback pin for VOUT5 if I^2C is set to use the external resistor. When turning off, the IC discharges CH5 output capacitors internally until VOUT5 < 0.1V. Recommend that output capacitors are as close as possible to the IC. This pin is in high impedance during shutdown.

Pin No.	Pin Name	Pin Function
28	VOUT8	Regulated output node of CH8 generic LDO. When turning off, RT5035A/B would discharge CH8 output capacitors internally till VOUT8 < 0.1V. This pin is in high impedance during shutdown.
29	PVDD8	Power input node of CH8 generic LDO. This pin is in high impedance during shutdown.
30	LX3	Switch node of CH3. This pin is in high impedance during shutdown.
31	C32K	RTC 32768Hz clock output pin. Its rails are VDDM and GND. When $\overline{\text{RESET}}$ goes low, C32K outputs low.
32	PVDD3	Power input pin of CH3 and it must connect to the same node as BAT. This pin is in high impedance during shutdown.
33	VOUT3/FB3	Sense pin of CH3 output voltage. This pin is also the feedback pin for VOUT3 if I^2C is set to use the external resistor. When turning off, the IC discharges CH3 output capacitors internally until VOUT3 < 0.1V. Recommend that output capacitors are as close as possible to the IC. This pin is in high impedance during shutdown.
34	RTCGND	Ground pin for RTC timer counter and oscillator.
35	XOUT	Crystal output. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
36	XIN	Crystal input. This pin's parasitic capacitance should be kept as low as possible. Noise interference should also be avoided.
37	RTCPWR	RTCLDO power pin. Connect this pin to a backup battery
38	VDDM	Regulation voltage output of CH9 keep-alive LDO. It also provides power for all IC control circuit.
39	SYNC	PLL synchronous input pin.
40	VOUT1	Power output and sense pin for CH1 output voltage. Recommend that output capacitors are as close to RT5035A/B as possible. This pin is in high impedance during shutdown.
41 (Exposed Pad)	GND	RT5035A/B power ground and control circuit ground. Exposed PAD should be soldered to PCB and connected to GND.

Functional Block Diagram



Operation

The RT5035A/B is a highly integrated DSC power management IC that contains 7-CH switching DC-DC converters, two generic LDO, one Keep Alive low quiescent LDO, one load switch with soft-start control and current limit, one switch with reverse leakage prevention from backup battery, and a Real-Time Clock (RTC) that includes a time counter and a 32768Hz oscillator.

CH1 : Step-Up DC-DC Converter

CH1 is a step-up converter for motor driver power in DSC system. The converter operates at asynchronous PFM or fixed frequency PWM current mode which can be set by the I^2C interface.

CH2 : Synchronous Step-Up / Down DC-DC

Converter CH2 is a synchronous step-up / down converter for system I/O power. The converter operates at fixed frequency PWM Current Mode.

CH3 : Synchronous Step-Down DC-DC Converter

CH3 is suitable for core power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH3 also can be adjusted output voltage if I^2C is set to use the external resistor.

CH4 : Synchronous Step-Down DC-DC Converter

CH4 is suitable for memory power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network.

CH5 : Synchronous Step-Down DC-DC Converter

The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH5 also can be adjusted output voltage if I^2C is set to use the external resistor.

CH6 : Generic LDO

CH6 is a generic low voltage LDO for multiple purpose power.

CH7 : WLED Driver

CH7 is a WLED driver that can support 6WLED/30mA, and it can setting OVP threshold, dimming current level and power on/off by I^2C interface.

CH8 : Generic LDO

CH8 is a generic low voltage LDO for multiple purpose power.

CH9 : Keep Alive LDO and RTC

The RT5035A/B provides a 3.1V output LDO for all IC control circuits and real time clock.

VNEG Charge Pump

The Charge pump is to increase the Vgs driving of big P-MOSFET in Ch2/3/4/5/10. When BAT < 3.6V and one of Ch2/3/4/5/10 turns on, VNEG charge pump will turn on and start to pump.

Load Switch (SW4)

The Load Switch is equipped with soft-start inrush control and current limit function (SW4).

CH10 : Synchronous Step-Down DC-DC Converter

CH10 is suitable for memory power in DSC system. The converter operates at asynchronous PFM or fixed frequency PWM current mode which can be set by the I^2C interface and it integrated internal MOSFETs, FB resistors and compensation network. The CH10 also can be adjusted output voltage if I^2C is set to use the external resistor.

Absolute Maximum Ratings (Note 1)

- Supply Voltage : BAT, PVDD2, PVDD3, PVDD4/10, PVDD5, PVDD6, PVDD8, SWI ---------- –0.3V to 6V
- Power Switch : LX1,LX2A, LX2B, LX3, LX4, LX5, LX10, CP ---------- –0.3V to 6V
- Power Switch : LX7 ---------- –0.3V to 24V
- Output Node : VOUT1 to VOUT6, SWO, VOUT8, VOUT10, RTCPWR, VDDM ---------- –0.3V to 6V
- Output Node : CN, VNEG ---------- (BAT – 6V) to 0.3V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)

  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W

  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage : BAT ---------- 1.8V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(VDDM = 3.1V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VDDM Over Voltage Protection		V_{DDM} Rising	5.8	6	6.2	V
VDDM Over Voltage Protection Hysteresis			--	0.25	--	V
BAT UVLO High Threshold Voltage (For Li) (Part. A)		V_{BAT} Rising	--	2.6	2.678	V
BAT UVLO Low Threshold Voltage (For Li) (Part. A)			2.328	2.4	--	V
BAT UVLO high Threshold Voltage (For 2AA) (Part. B)		V_{BAT} Rising	--	1.7	1.751	V
BAT UVLO low Threshold Voltage (For 2AA) (Part. B)			1.455	1.5	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Shutdown Supply Current into BAT (Including CH9 keep-alive LDO)	$I_{OFF,BAT}$	EN = 0V, Reg.SHDN_EN1 = 0, Reg.SHDN_EN10 = 0 and VOUT1 = 0V, BAT = 3.3V	--	10	--	μA
Shutdown Supply Current into BAT (Including CH9 keep-alive LDO)	$I_{OFF,BAT}$	EN = 0V, Reg.SHDN_EN1 = 0, Reg.SHDN_EN10 = 1 and VOUT1 = 0V, BAT = 3.3V And CH10 no-switching	--	--	80	μA
Shutdown Supply Current into VOUT1 (Including CH9 keep-alive LDO)	$I_{OFF,VOUT1}$	EN = 0V, Reg.SHDN_EN1 = 1, Reg.SHDN_EN10 = 0 and Ch1 no-switching and VOUT1 = 4.2V, BAT = 3.3V	--	--	80	μA
Shutdown Supply Current into VOUT1 (including CH9 keep-alive LDO)	$I_{OFF,VOUT1}$	EN = 0V, Reg.SHDN_EN1 = 1, Reg.SHDN_EN10 = 1 and Ch1 no-switching and VOUT1 = 4.2V, BAT = 3.3V	--	--	100	μA
CH1 (Sync Step-Up PWM) + CH2 (Sync Step-Up/Down) + CH3 (Sync Step-Down) + CH4 (Sync Step-Down) + CH10 (Sync Step-Down) Supply Current into VDDM	$I_{Q1234,10}$	EN = 3.3V, Reg.SHDN_EN1 = 1, And Non switching.	--	--	1600	μA
CH2 (Sync Step-Up/Down) + CH3 (Sync Step-Down) + CH4 (Sync Step-Down) + CH10 (Sync Step-Down) Supply Current into VDDM	$I_{Q234,10}$	EN = 3.3V, And Non switching.	--	--	1400	μA
CH5 (sync Step-Down) Supply Current into VDDM	I_{Q5}	EN = 3.3V, And Non switching	--	--	400	μA
CH6 (LDO) Supply Current into VDDM	I_{Q6}	EN = 3.3V, And no load.	--	--	100	μA
CH7 (WLED) in Async Step-Up Mode Supply Current into VDDM	I_{Q7bo}	EN = 3.3V, And Non switching	--	--	500	μA
CH8 (LDO) Supply Current into VDDM	I_{Q8}	EN = 3.3V, And no load.	--	--	100	μA
CH10 (sync Step-Down) Supply Current into VDDM	I_{Q10}	EN = 3.3V, And Non switching,	--	--	400	μA
Oscillator						
CH1, 3, 4, 5, 10 Operation Frequency	F_{OSC}	CH1 in PWM mode	1800	2000	2200	kHz
CH2, 7 Operation Frequency	F_{OSC}		900	1000	1100	kHz
CH1 Maximum Duty Cycle (Step-Up)		F_{OSC} = 2000kHz	80	83	86	%
CH2 Maximum Duty Cycle at LX2B		F_{OSC} = 1000kHz	80	83	86	%
CH2 Maximum Duty Cycle at LX2A			--	--	100	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH3 Maximum Duty Cycle (Step-Down)			--	--	100	%
CH4 Maximum Duty Cycle (Step-Down)			--	--	100	%
CH5 Maximum Duty Cycle (Step-Down)			--	--	100	%
CH7 Maximum Duty Cycle (WLED)		Step-Up mode	91	93	97	%
CH10 Maximum Duty Cycle (Step-Down)			--	--	100	%
Feedback and Output Regulation Voltage						
VOUT1 Accuracy		A1.VOUT1 = 0 to 7	–1.5	--	1.5	%
		A1.VOUT1 = 8 to 15	–2	--	2	%
VOUT2, 3, 10 Accuracy		The VOUTx typical values are listed next.	–1.5	--	1.5	%
VOUT4 Accuracy		A2.VOUT4 = 0 to 3 (near 1.8V)	–1.5	--	1.5	%
		A2.VOUT4 = 4 to 7 (near 1.5V)	–2	--	2	%
VOUT5 Accuracy		A2.VOUT5 = 0 to 3	–1.5	--	1.5	%
		A2.VOUT5 = 4 to 7	–2	--	2	%
VOUT6 Accuracy		A3.VOUT6 = 0 to 8	–2	--	2	%
		A3.VOUT6 = 9 to 15	–2	--	2	%
VOUT8 Accuracy		A4.VOUT8 = 0 to 3	–2	--	2	%
		A4.VOUT8 = 4 to 7	–2	--	2	%
Feedback Regulation Voltage @ FB7			0.285	0.3	0.315	V
VDDM Voltage (CH9 LDO Output Regulation)			3.01	3.1	3.19	V
Power Switch Ron and Current Limit						
CH1 On Resistance of MOSFET	$R_{DS(ON)\_1}$	P-MOSFET, VOUT1 = 3.3V	--	150	200	mΩ
		N-MOSFET, VOUT1 = 3.3V	--	100	150	mΩ
CH1 Current Limitation (Step-Up)	I_{LIM_1}		2.5	3.5	4.5	A
CH2 On Resistance of MOSFET	$R_{DS(ON)\_2A}$	P–MOSFET (PVDD2 – LX2A), PVDD2 = VOUT2 = 3.3V	--	100	150	mΩ
		N–MOSFET (LX2A – GND), PVDD2 = VOUT2 = 3.3V	--	200	300	mΩ
CH2 On Resistance of MOSFET	$R_{DS(ON)\_2B}$	P–MOSFET (LX2B – VOUT2), PVDD2 = VOUT2 = 3.3V	--	150	200	mΩ
		N–MOSFET (LX2B – GND), PVDD2 = VOUT2 = 3.3V	--	100	150	mΩ
CH2 Current Limitation	I_{LIM_2}	Both PMOS (PVDD2 – LX2A) and NMOS (LX2B – GND)	2.2	3	4	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH3 On Resistance of MOSFET	$R_{DS(ON)\_3}$	P–MOSFET, PVDD3 = 3.3V	--	200	300	mΩ
		N-MOSFET, PVDD3 = 3.3V	--	150	220	mΩ
CH3 Current Limitation (Step-Down)	I_{LIM_3}		2.2	3	3.8	A
CH4 On Resistance of MOSFET	$R_{DS(ON)\_4}$	P-MOSFET, PVDD4 = 3.3V	--	350	400	mΩ
		N-MOSFET, PVDD4 = 3.3V	--	350	400	mΩ
CH4 Current Limitation (Step-Down)	I_{LIM_4}		1	1.5	2	A
CH5 On Resistance of MOSFET	$R_{DS(ON)\_5}$	P-MOSFET, PVDD5 = 3.3V	--	350	400	mΩ
		N-MOSFET, PVDD5 = 3.3V	--	350	400	mΩ
CH5 Current Limitation (Step-Down)	I_{LIM_5}		1	1.5	2	A
CH7 On Resistance of MOSFET	$R_{DS(ON)\_7}$	N-MOSFET	--	400	500	mΩ
CH7 Current Limitation	I_{LIM_7}	N-MOSFET	0.6	0.8	1	A
CH10 On Resistance of MOSFET	$R_{DS(ON)\_10}$	P-MOSFET, PVDD10 = 3.3V	--	350	400	mΩ
		N-MOSFET, PVDD10 = 3.3V	--	350	400	mΩ
CH10 Current Limitation (Step-Down)	I_{LIM_10}		1	1.5	2	A
SW4 Load Switch						
Supply Voltage of SW4 at SWI	SWI		1.2		3.6	V
SW4 On Resistance of MOSFET	$R_{DS(ON)\_SW4}$	SWI = 1.8V, VOUT1 = 3.6V, I_O = 400mA	--	100	130	mΩ
		SWI = 3.6V, VOUT1 = 5V, I_O = 400mA	--	100	130	mΩ
SW4 Soft-Start Time		From enabled to V_{SWO} = V_{SWI} = 1.8V	--	1.4	--	ms
Current Limit of SW4	I_{LIM_SW4}	SWI = 1.8V	500	900	--	mA
CH6 LDO						
Supply Voltage of Ch6	PVDD6		2.7	--	5.5	V
PSRR+ of Ch6		1kHz, I_O = 10mA, PVDD6 = 3.6V, VOUT6 = 2.7V	--	–60	--	dB
Ch6 Dropout Voltage		VOUT6 = 2.7V, I_O = 100mA	--	50	80	mV
Current Limit of Ch6	I_{LIM_6}	VOUT6 = 2.7V	300	450	600	mA
Control						
CP Pull Down Resistance			70	100	–	kΩ
EN Input High Level Threshold			1.3	--	--	V
EN Input Low Level Threshold			--	--	0.4	V
EN Sink Current			--	1	3	μA
SYNC Input High Level Threshold			1.3	--	--	V
SYNC Input Low Level Threshold			--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYNC Sink Current			--	1	3	μA
Thermal Protection						
Thermal Shutdown	T_{SD}		125	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
VNEG Charge Pump						
Charge Pump Low Threshold to Start	NVst	Monitor BAT falling	3.4	3.6	3.8	V
Charge Pump Hysteresis gap to Stop	ΔNVst		0.1	0.2	0.3	V
(BAT-VNEG) Clamp Level			4.1	4.5	4.9	V
CH8 LDO						
Supply Voltage of Ch8	PVDD8		2.7	--	5.5	V
PSRR+ of Ch8		1kHz, I_O = 10mA, PVDD8 = 3.6V, VOUT8 = 3.4V	--	–60	--	dB
Ch8 Dropout Voltage		VOUT8 = 3.4V, I_O = 100mA	--	40	60	mV
Current Limit of Ch8	I_{LIM_8}	VOUT8 = 3.4V	220	300	380	mA
CH9 Keep-Alive LDO						
Supply Voltage of CH9 at VOUT1 Pin			2.4	--	5.5	V
PSRR+ of CH9		1kHz, I_O = 1mA, V_{DDM} = 3.1V	--	–40	--	dB
CH9 Dropout Voltage		V_{DDM} = 3.1V, I_O = 20mA	--	220	300	mV
Current Limit of RTC LDO	I_{LIM_9}	V_{DDM} = 3.1V	50	100	--	mA
$\overline{\text{RESET}}$ Hysteresis Low		$\overline{\text{RESET}}$ falling	2.15	2.2	--	V
$\overline{\text{RESET}}$ Hysteresis High		$\overline{\text{RESET}}$ rising	--	2.4	2.45	V
$\overline{\text{RESET}}$ Rising Delay Time			--	--	0.5	s
CH9 Quiescent Current		Excluding RTC quiescent current	--	10	--	μA
RTC						
RTC Operation Voltage			1.9	--	3.3	V
RTC Quiescent Current (Including RTC_UVLO, RTC_OSC, and Time Counter)		RTCPWR > UVLO threshold XIN = XOUT = 14pF	--	--	3	μA
		RTCPWR < UVLO threshold	--	--	0.2	μA
RTC Clock			--	32.768	--	kHz
RTC Clock Accuracy		RTCPWR = 1.9V to 3.3V	–10	--	10	ppm
RTC Clock Output High		Pin C32K source Out 0.1mA	VDDM – 0.3	--	--	V
RTC Clock Output Low		Pin C32K sink 0.1mA	--	--	0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RTC Under Voltage Lockout Threshold (UVLO)	V_{RTC_F}	RTCPWR falling	1.8	1.9	2	V
	V_{RTC_R}	RTCPWR rising	V_{RTC_F} + 20m	2.2	2.3	V
RTC OSC Startup Time			--	0.5	1	s
Switch Ron from VDDM to RTCPWR		P-MOSFET, V_{DDM} = 3.1V	--	60	--	Ω
Under-Voltage and Over-Voltage Protection						
CH1 OVP Threshold @ VOUT1			5.6	5.8	6	V
CH2 OVP Threshold @ VOUT2			5.8	6	6.2	V
CH7 OVP Threshold Accuracy @ LX7		Target voltage is the chosen one in A7.OVP7	Target – 1	Target	Target + 1	V
CH1 UVP Threshold @ VOUT1			1.95	2.25	2.55	V
CH2 UVP Threshold @ VOUT2			1.4	1.6	1.8	V
CH3 UVP Threshold @ VOUT3			0.525	0.6	0.675	V
CH4 UVP Threshold @ VOUT4			0.7	0.8	0.9	V
SW4 Load Switch UVP Threshold		VSWI-VSWO	--	0.9	--	V
SW4 Load Switch UVP Threshold		VSWO	--	0.9	--	V
CH5 UVP Threshold @ VOUT5			0.7	0.8	0.9	V
CH6 UVP Threshold @ VOUT6		A3.VOUT6 = 0 to 9	--	1.6	--	V
		A3.VOUT6 = 10 to 15	--	0.8	--	
CH8 UVP Threshold @ VOUT8		Target voltage is the chosen one in A4.VOUT8	--	0.5 x Target	--	V
CH10 UVP Threshold @ VOUT10			0.7	0.8	0.9	V
CH1 Over-Load P threshold (OLP) @ VOUT1		Target voltage is the chosen one in A1.VOUT1	--	Target – 0.6	--	V
CH2 OLP Threshold @ VOUT2		Target voltage is the chosen one in A1.VOUT2	--	Target – 0.4	--	V
CH3 OLP Threshold @ VOUT3		Target voltage is the chosen one in A2.VOUT3	--	Target – 0.15	--	V
CH4 OLP Threshold @ VOUT4		Target voltage is the chosen one in A2.VOUT4	--	Target – 0.2	--	V
CH5 OLP Threshold @ VOUT5		Target voltage is the chosen one in A3.VOUT5	--	Target – 0.2	--	V
CH10 OLP Threshold @ VOUT10		Target voltage is the chosen one in A5.VOUT10	--	Target –0.2	--	V
Protection Delay Time		for OCP and OLP, except OCP of CH2	--	100	--	ms
I^2C						
SDA, SCLK Input High Level Threshold			0.7 x VDDM	--	--	V
SDA, SCLK Input Low Level Threshold			--	--	0.3 x VDDM	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Clock Rate	f_{SCL}	VDDM = 3.1V, VOUT2 = 3.3V	--	--	400	kHz
Hold Time (Repeated) START condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$		0.6	--	--	µs
LOW Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
HIGH Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	µs
Data Set-Up Time	$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		1.3	--	--	µs
Rise Time of both SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of both SDA and SCL Signals	t_F		20	--	300	ns
SDA and SCL Output Low Sink Current	I_{OL}	SDA or SCL voltage = 0.4V	2	--	--	mA
Output Voltage Ramp Rate						
VOUT1 Ramp Rate		VOUT1 = 3.6V to 5.3V	--	1.24	--	V/ms
VOUT2 Ramp Rate		VOUT2 = 0V to 3.25V	--	0.82	--	V/ms
VOUT3 Ramp Rate		VOUT3 = 0V to 1.1V	--	0.33	--	V/ms
VOUT4 Ramp Rate		VOUT4 = 0V to 1.8V	--	0.44	--	V/ms
VOUT5 Ramp Rate		VOUT5 = 0V to 2.2V	--	0.6	--	V/ms
VOUT6 Ramp Rate		VOUT6 = 0V to 2.7V	--	0.84	--	V/ms
VOUT8 Ramp Rate		VOUT8 = 0V to 3.4V	--	0.84	--	V/ms
VOUT10 Ramp Rate		VOUT10 = 0V to 1.35V	--	0.41	--	V/ms
Ramp Rate Accuracy of All the Above			–40	--	+40	%
Enabling Delay Time						
Delay Time Step Resolution		For ENDLY2, 3, 4, 10	1.5	2	2.5	ms
Off Discharge						
VOUT1, 2, 3, 4, 5, 10 Discharge Equivalent Resistance		VDDM = 3.1V and VOUTx = 1V	50	--	--	Ω
SW4 Discharge Equivalent Resistance		VDDM = 3.1V and SWO = 1V	400	--	--	Ω
VOUT6 Discharge Equivalent Resistance		VDDM = 3.1V and VOUT6 = 1V	200	--	--	Ω
VOUT8 Discharge Equivalent Resistance		VDDM = 3.1V and VOUT8 = 1V	200	--	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDM Discharge Equivalent Resistance		VM = 4.2V and VDDM = 1V	200	--	--	Ω
Each Channel Discharge Finish Threshold for Next Channel Starting to Turn Off			0.05	0.1	0.15	V
CH1 Async. PFM						
N-MOSFET On-Time			--	0.5	--	μs
Minimum Off-Time			--	0.5	--	μs
N-MOSFET Current Limit			--	0.8	--	A
VOUT1 Regulation Voltage			3.5	3.6	3.7	V

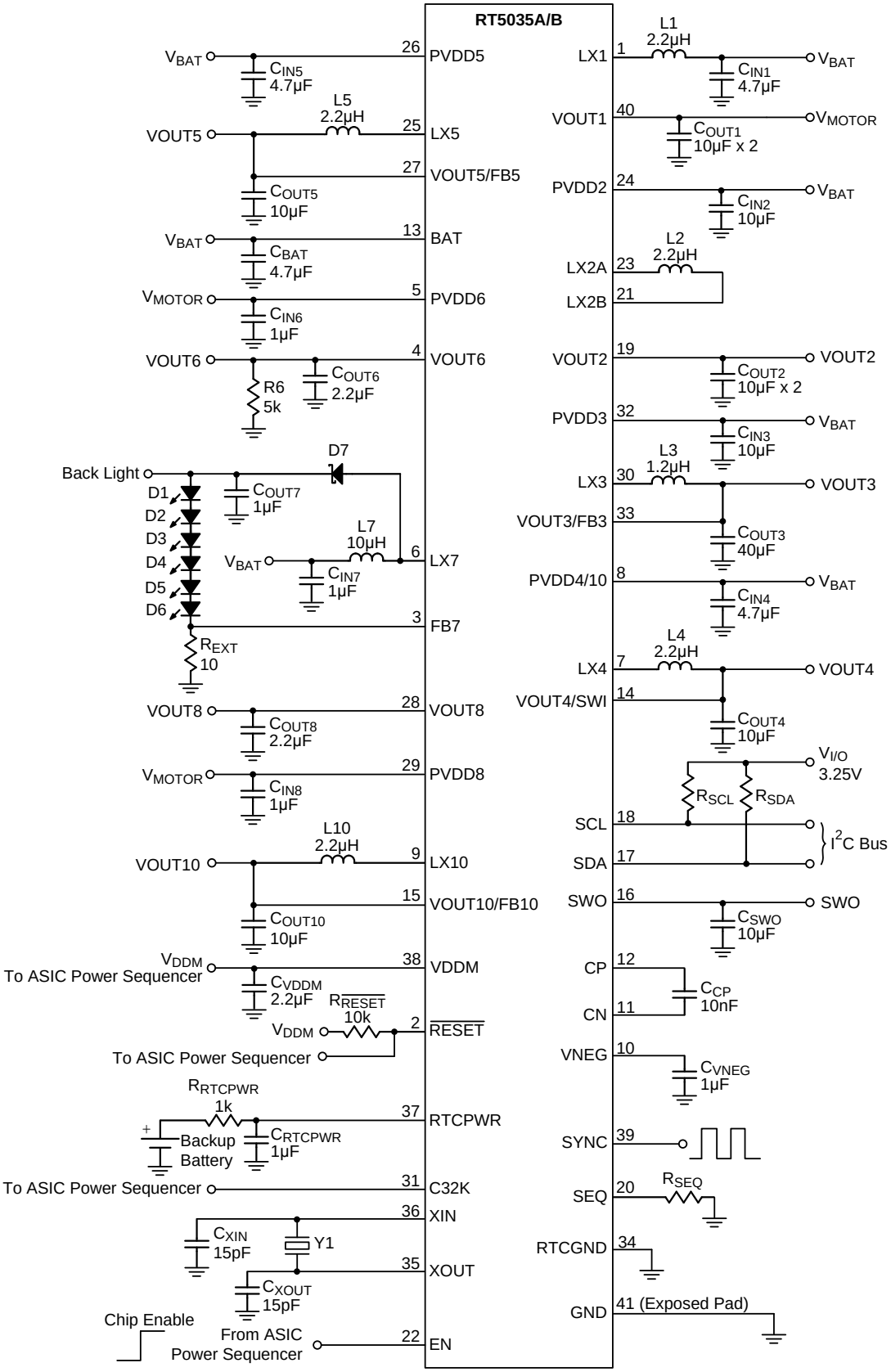
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

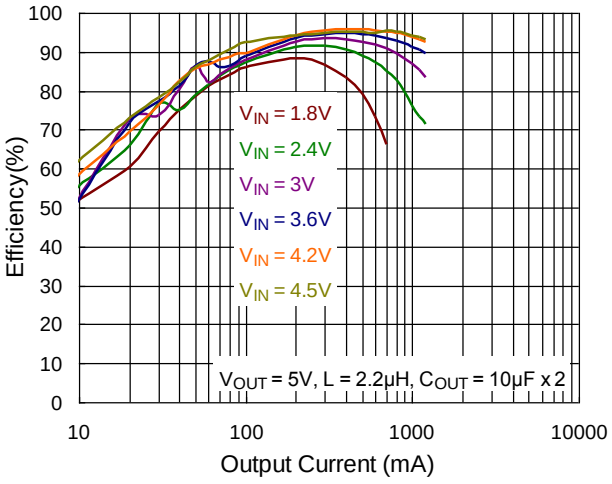
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

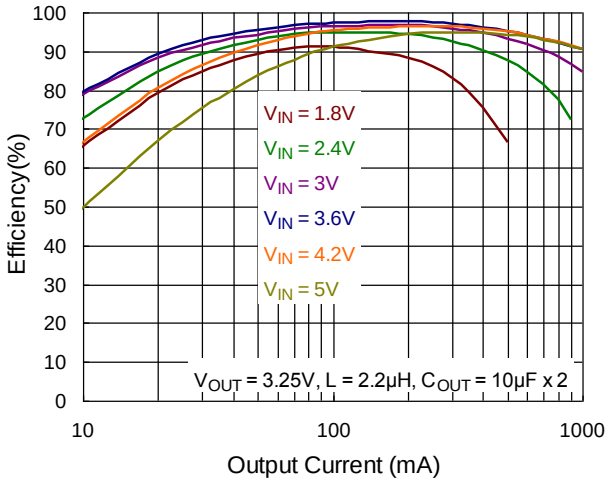


Typical Operating Characteristics

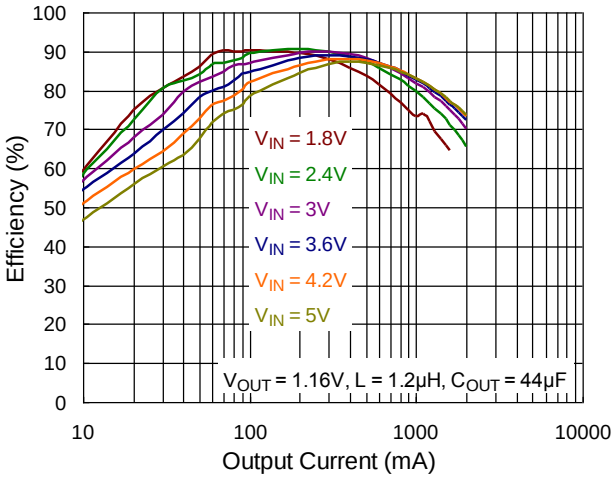
CH1 Boost Efficiency vs. Output Current



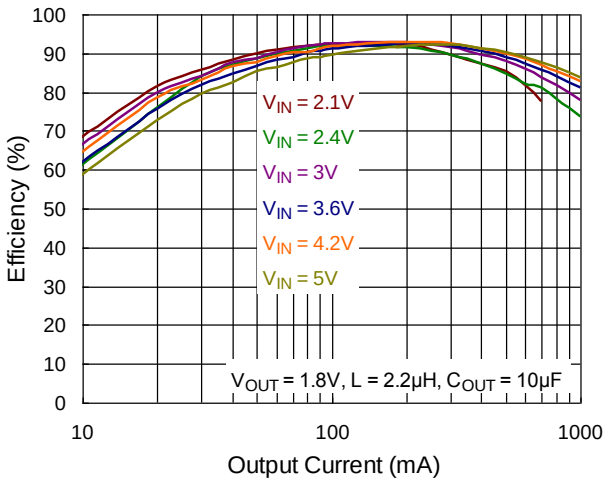
CH2 Buck-Boost Efficiency vs. Output Current



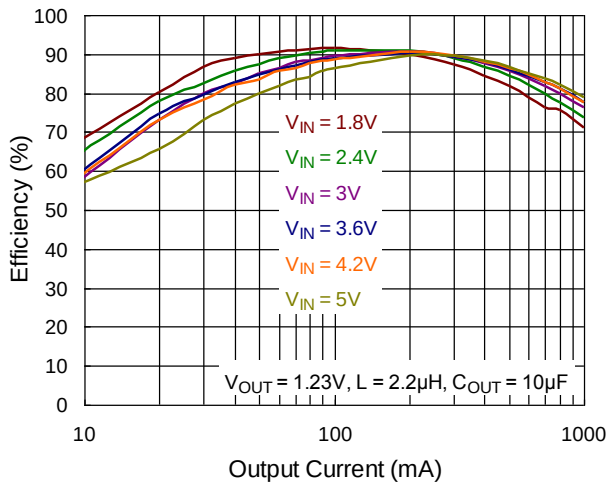
CH3 Buck Efficiency vs. Output Current



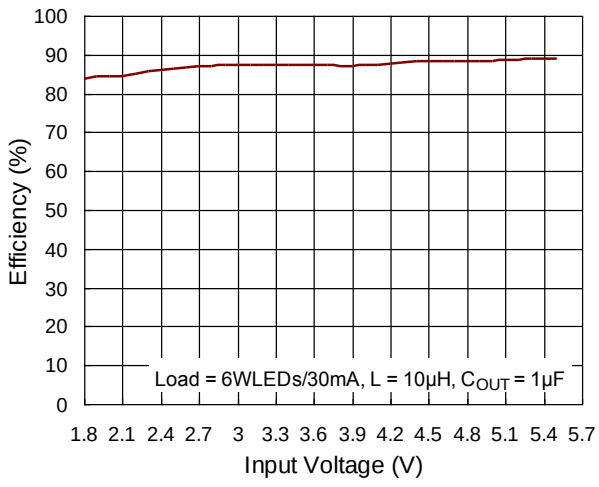
CH4 Buck Efficiency vs. Output Current



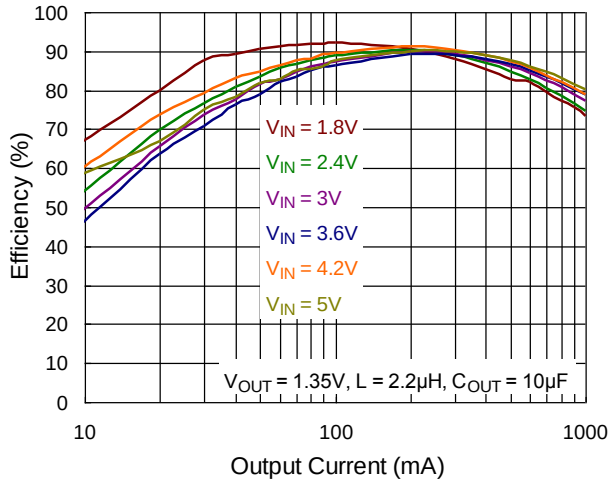
CH5 Buck Efficiency vs. Output Current



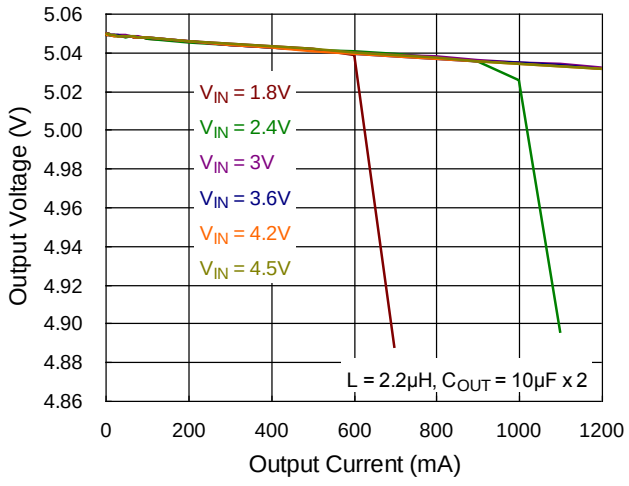
CH7 Efficiency vs. Input Voltage



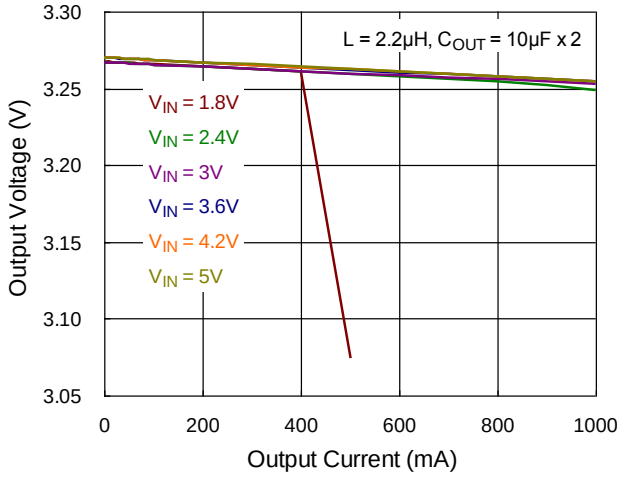
CH10 Buck Efficiency vs. Output Current



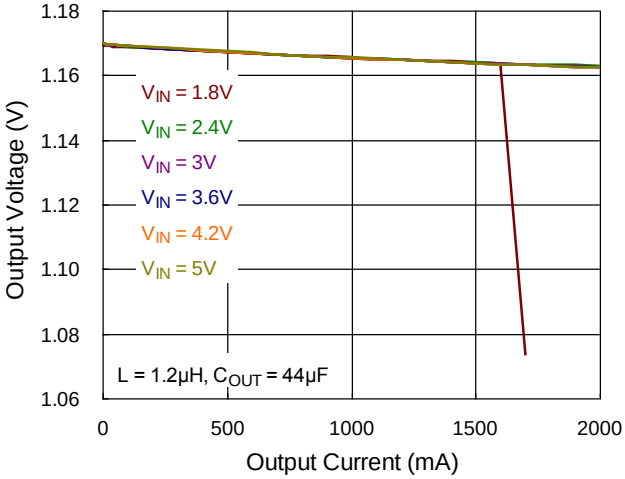
CH1 Boost Output Voltage vs. Output Current



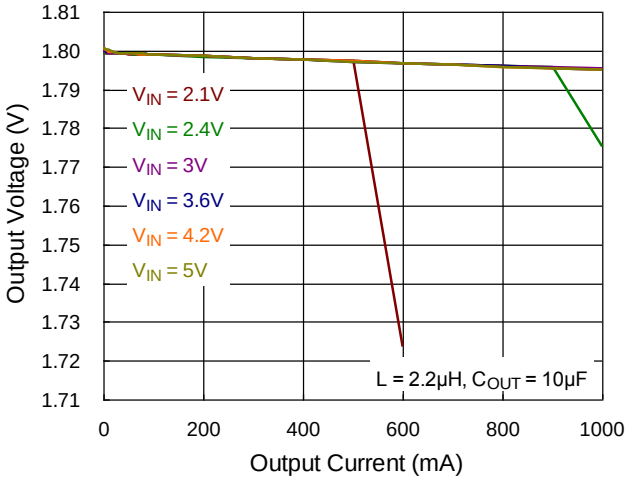
CH2 Buck-Boost Output Voltage vs. Output Current



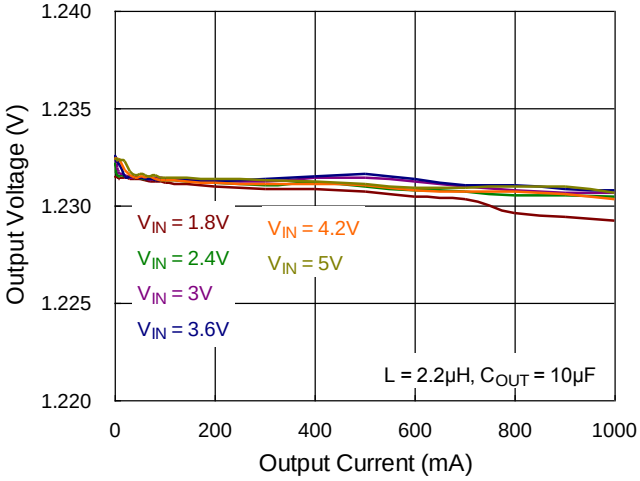
CH3 Buck Output Voltage vs. Output Current



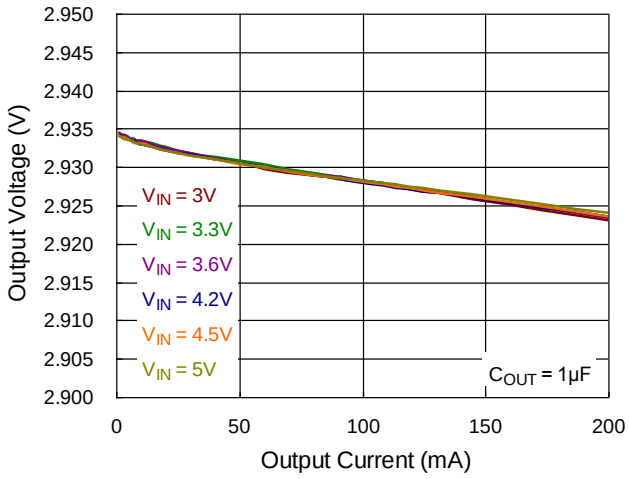
CH4 Buck Output Voltage vs. Output Current



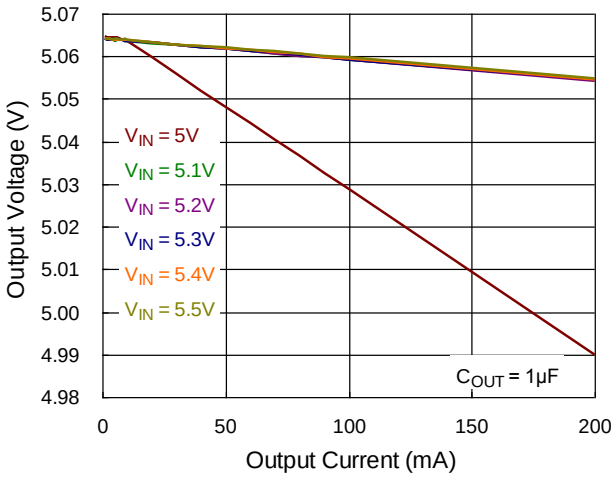
CH5 Buck Output Voltage vs. Output Current



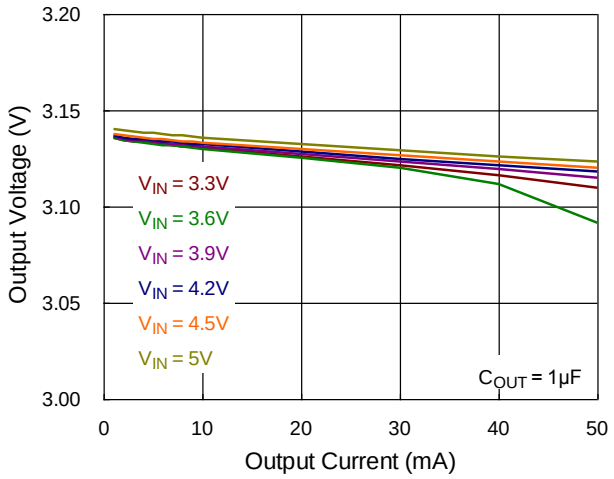
CH6 LDO Output Voltage vs. Output Current



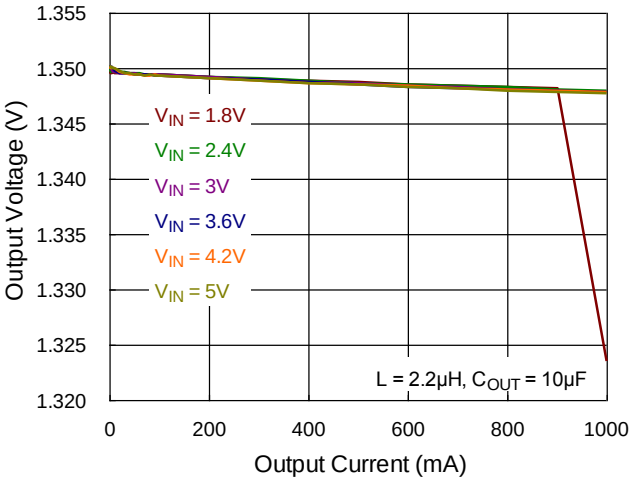
CH8 LDO Output Voltage vs. Output Current



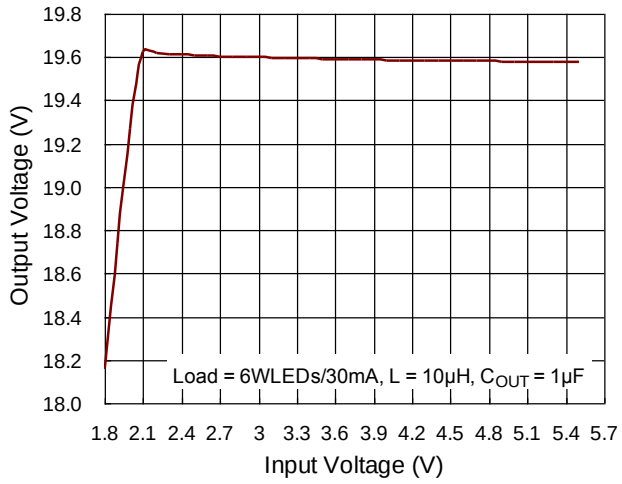
CH9 LDO Output Voltage vs. Output Current



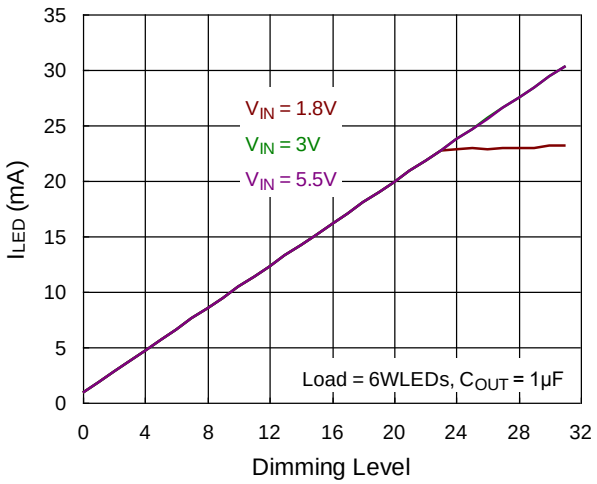
CH10 Buck Output Voltage vs. Output Current



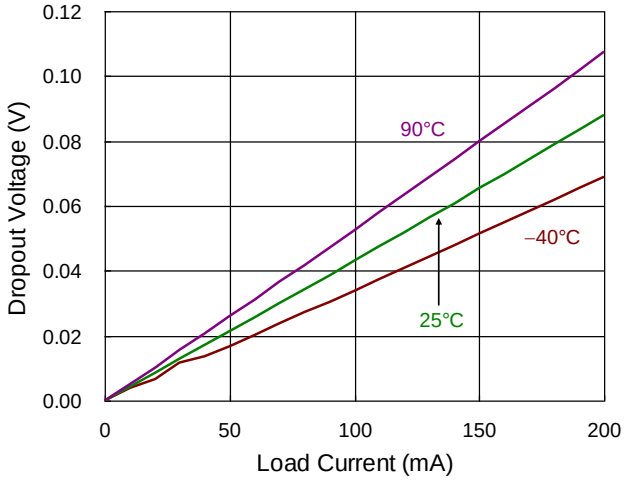
CH7 Output Voltage vs. Input Voltage



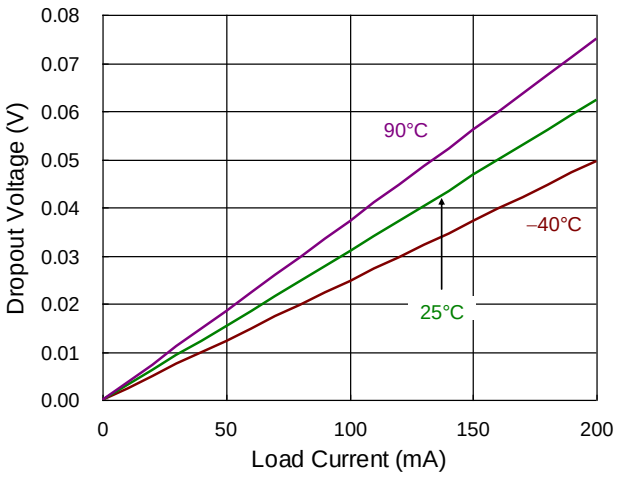
CH7 LED Current vs. Dimming Level



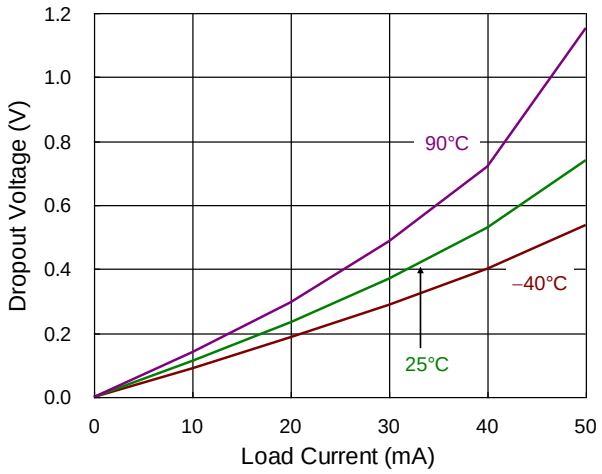
CH6 LDO Dropout Voltage vs. Load Current



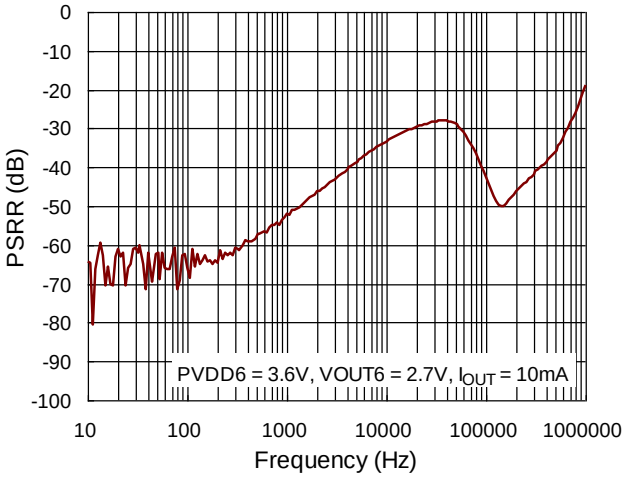
CH8 LDO Dropout Voltage vs. Load Current



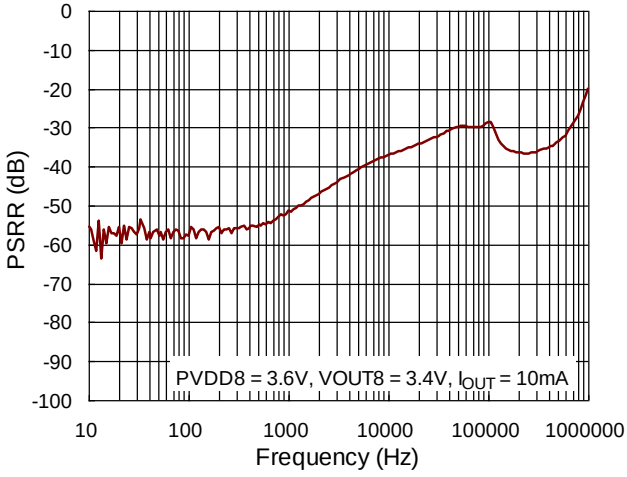
CH9 LDO Dropout Voltage vs. Load Current



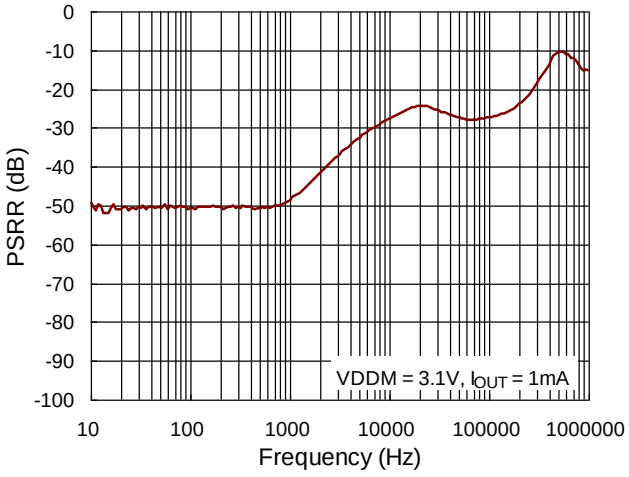
CH6 LDO PSRR



CH8 LDO PSRR



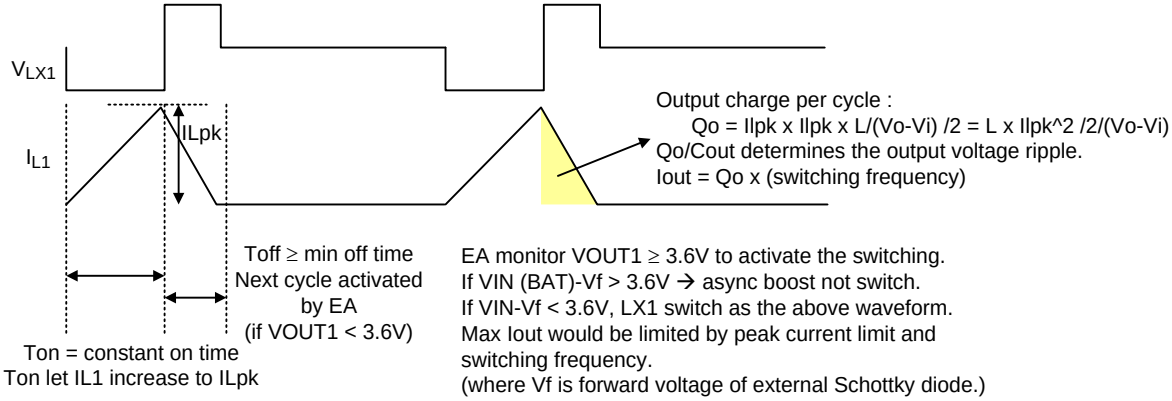
CH9 LDO PSRR



Application Information

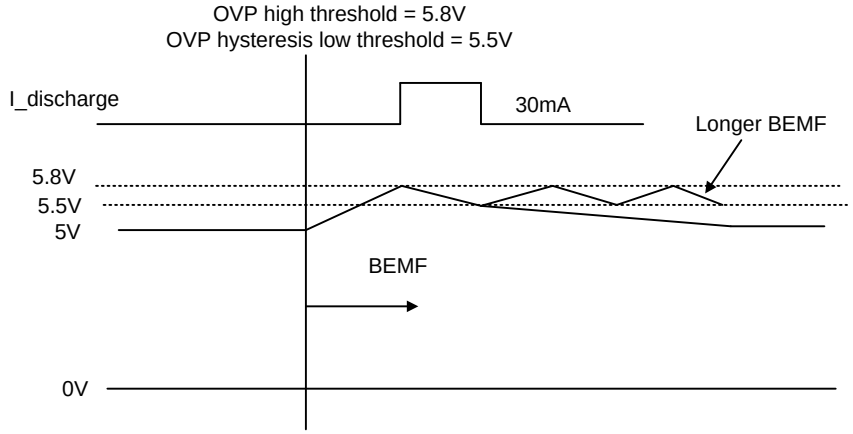
CH1 : Step-Up DC-DC Converter

CH1 is a step-up converter for motor driver power in DSC system. The converter operates at Async PFM or fixed frequency PWM current mode which can be set by I^2C. The converter integrates internal MOSFETs, FB resistors, compensation network and synchronous rectifier for up to 95% efficiency. The output voltage of CH1 is adjustable by the I^2C interface in the range of 3.6V to 5.3V. When CH1 operates at Async. PFM mode, LX1 switches as below waveform :



CH1 OVP Operation

Usually, CH1 suffers BEMF of motor, and OVP would occur abnormally. To eliminate this, the operation of CH1 is as follows. When OVP (5.8V) occurs, CH1 stops switching and CH1 discharges VOUT1 through internal MOS (only for discharge, I~30mA) until OVP hysteresis (5.5V) low threshold. If there is longer BEMF, the charging and discharging period will repeat. PMU itself doesn't shut down immediately, but shuts down when continuous 100mS OVP occurs.



CH2 : Synchronous Step-Up / Down DC-DC Converter

CH2 is a synchronous step-up / down converter for system I/O power. The converter operates at fixed frequency PWM Current Mode. The converter integrates internal MOSFETs, FB resistors, compensation network and synchronous rectifier for up to 95% efficiency. The output voltage of CH2 can be adjusted by the I^2C interface in the range of 2.9V to 3.65V.

VNEG Charge Pump

The Charge pump is to increase the Vgs driving of big PMOS in Ch2/3/4/5/10. When BAT < 3.6V and one of Ch2/3/4/5/10 turns on, VNEG Charge Pump would turn on and start to pump. But when pumping, the BAT threshold to turn off and stop charge pump becomes 3.9V. When pumping, the (BAT – VNEG) voltage would be clamped at 4.5V. But because of charge pumping architecture limitation, most negative level of the VNEG is only (–BAT). Hence, if BAT < 4.5 / 2 = 2.25V, VNEG is limited to (–BAT). When VNEG Charge pump is off, VNEG is connected internally to GND.

CH3 : Synchronous Step-Down DC-DC Converter

CH3 is suitable for core power in DSC system. The converter operates in fixed frequency PWM mode with integrated MOSFETs, FB resistors and compensation network. The CH3 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. The output voltage of CH3 is adjustable by the I^2C interface in the range of 1V to 1.3V. Besides, the CH3 also can be adjusted output voltage if I^2C is set to use the external resistor. The VOUT can be calculated by the equation as below :

$V_{OUT\_CH3} = (1 + R1 / R2) \times V_{FB3}$

Where V_{FB3} is 0.8V typically and suggested value for R1 is 100kΩ to 600kΩ.

CH4 : Synchronous Step-Down DC-DC Converter

CH4 is suitable for digital I/O power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH4 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. The output voltage of CH4 is adjustable by the I^2C interface in the range of 1.35V to 2.14V.

CH5 : Synchronous Step-Down DC-DC Converter

CH5 is suitable for CMOS sensor power in DSC system. The converter operates in fixed frequency PWM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH5 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. The output voltage of CH5 is adjustable by the I^2C interface in the range of 1.2V to 2V or set by external feedback resistors, as expressed in the following equation :

$V_{OUT\_CH5} = (1 + R1 / R2) \times V_{FB5}$

where V_{FB5} is 0.8V typically and suggested value for R1 is 100kΩ to 600kΩ.

CH6 : Generic LDO

CH6 is a generic low voltage LDO for multiple purpose power. The CH6 is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH6 has an ON/OFF control which can be set by I^2C commands. The output voltage of CH6 is adjustable by the I^2C interface in the range of 1.2V to 3V.

CH7 : WLED Driver

CH7 is a WLED driver operates at asynchronous step-up mode with an internal MOSFET and internal compensation. The LED current is defined by FB7 voltage and the external resistor between FB7 and GND. The FB7 regulation voltage can be set in 32 steps from 9.2mV to 300mV, typically, via I^2C interface.

The WLED current can be set by the following equation :

I_{LED} (mA) = [0.3V / R_{EXT}] x (DIM7 + 1) / 32

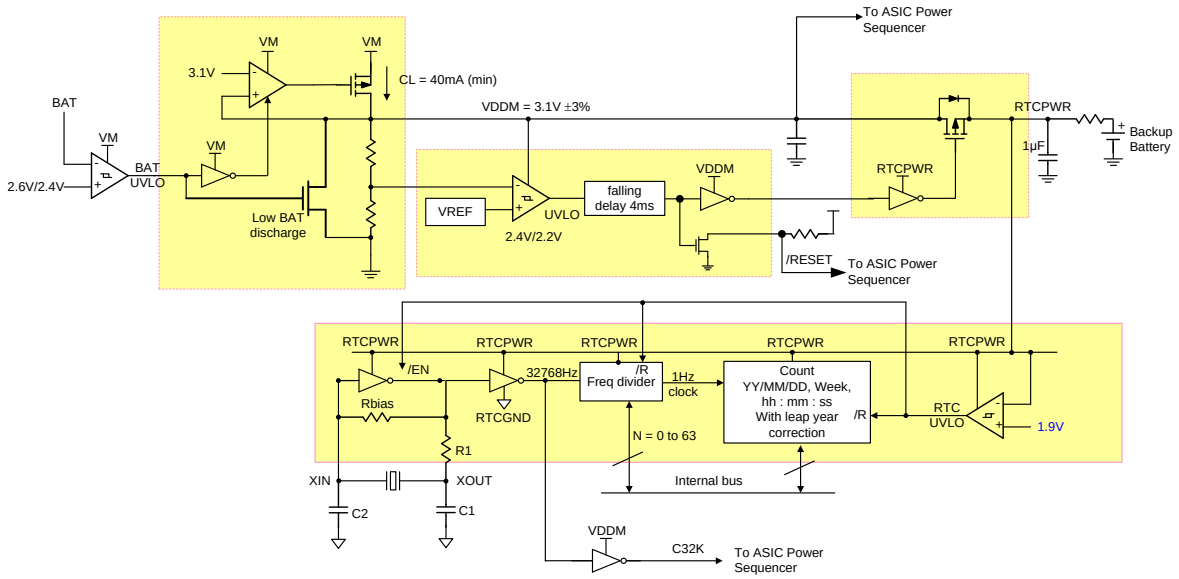
Where R_{EXT} is the current sense resistor from FB7 to GND and (DIM7 + 1) / 32 ratio refers to I^2C control register file. The 0.3V voltage is with ±5% accuracy. The maximum I_{LED} is defined by 0.3V / R_{EXT}.

CH8 : Generic LDO

CH8 is a generic low voltage LDO for multiple purpose power. The CH8 is a linear regulator, designed to be stable over the entire operating load range with the use of external ceramic capacitors. CH8 has an ON/OFF control which can be set by I^2C commands. The output voltage of CH8 is adjustable by the I^2C interface in the range of 1.5V to 5.2V.

CH9 : Keep Alive LDO and RTC Related Function Block

The RT5035A/B provides a 3.1V output LDO for all IC control circuits and real time clock. The LDO features low quiescent current (3μA) and high output voltage accuracy. This LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 1μF to the VDDM pin. The RTCPWR switch avoids back charging from the RTCPWR node into the input node VDDM.



CH10 : Synchronous Step-Down DC-DC Converter

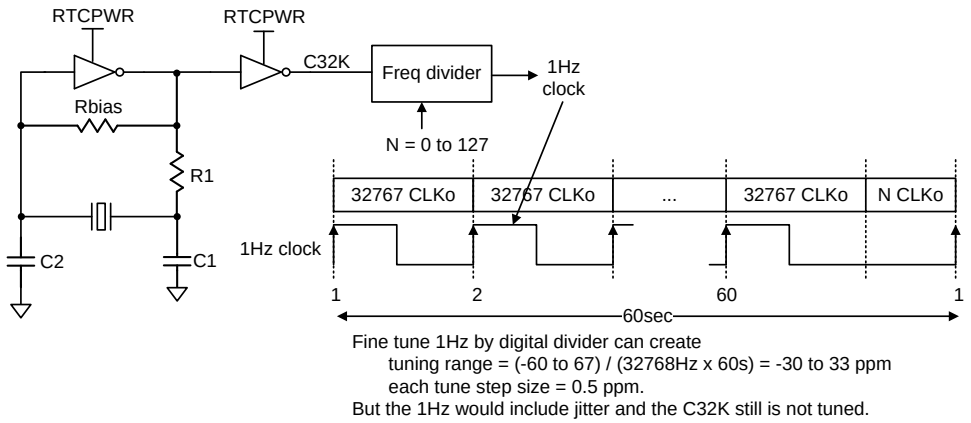
CH10 is suitable for memory power in DSC system. The converter operates in fixed frequency PWM mode or PFM mode with integrated internal MOSFETs, FB resistors and compensation network. The CH10 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. The output voltage of CH10 is adjustable by the I^2C interface in the range of 1.2V to 1.52V or set by external feedback resistors, as expressed in the following equation :

$V_{OUT\_CH10} = (1 + R1 / R2) \times V_{FB10}$

Where V_{FB10} is 0.8V typically and suggested value for R1 is 100kΩ to 600kΩ.

RTC_C32K

The Frequency Divider from 32768Hz to 1Hz would generate the below 1Hz wave that with a little jitter but the 1Hz average frequency can be finely tuned.



Fine tune 1Hz by digital divider can create
tuning range = (-60 to 67) / (32768Hz x 60s) = -30 to 33 ppm
each tune step size = 0.5 ppm.
But the 1Hz would include jitter and the C32K still is not tuned.

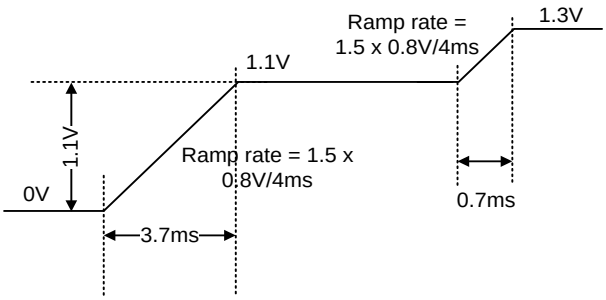
RTC time read/write method :

When reading RTC time via I^{2}C interface, suggest read 6 bytes (address A11 to A16) together and finish reading within 0.5 second to avoid the second carry issue. A16.RTCT_SEC[0] can be used for checking whether second is carried during reading time. When writing RTC time via I^{2}C interface, suggest to write 6 bytes (address A11 to A16) together. A11 is first and then A12, A13, A14, A15, A16. Suggest finishing writing within 0.5 second to avoid second carry issue during writing.

Output Voltage Ramp Rate

For instance, CH3 V_{CORE} output voltage ramp up rate = 1.5 x 0.8V / 4ms = 0.3V/ms. The ramp up/down rate is kept the same for enabling soft-start or dynamic output voltage adjustment.

Each channel has different ramp rate as listed below.



Note :

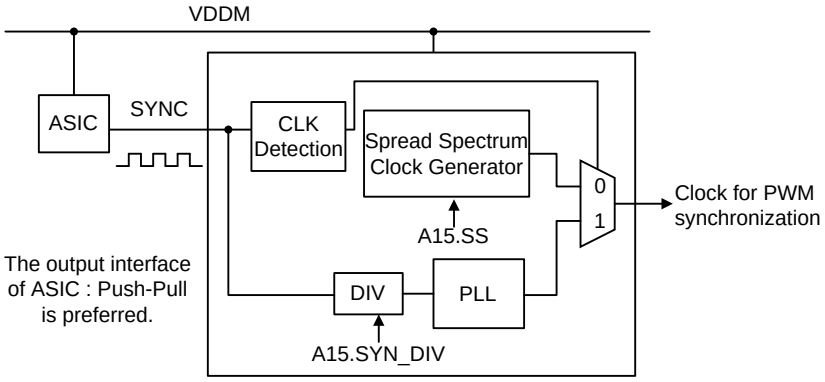
About Dynamic Voltage Scaling, CH1, CH3, CH4, CH8, CH10 output voltage can be changed without inrush and Vout ramping control when they have been turned on (said, dynamically change Vout). CH2, CH5, CH6 are not.

Synchronization and Spread Spectrum

If SYNC remains logic high or low, the spread spectrum clock will act the main clock for PWM. And, spread spectrum function can be turned off by register A15.SS.

If the toggling clock of SYNC is detected, the PLL clock will act the main clock for PWM and the clock of PLL will track its frequency. And the division ratio is decided by A15.SYN_DIV.

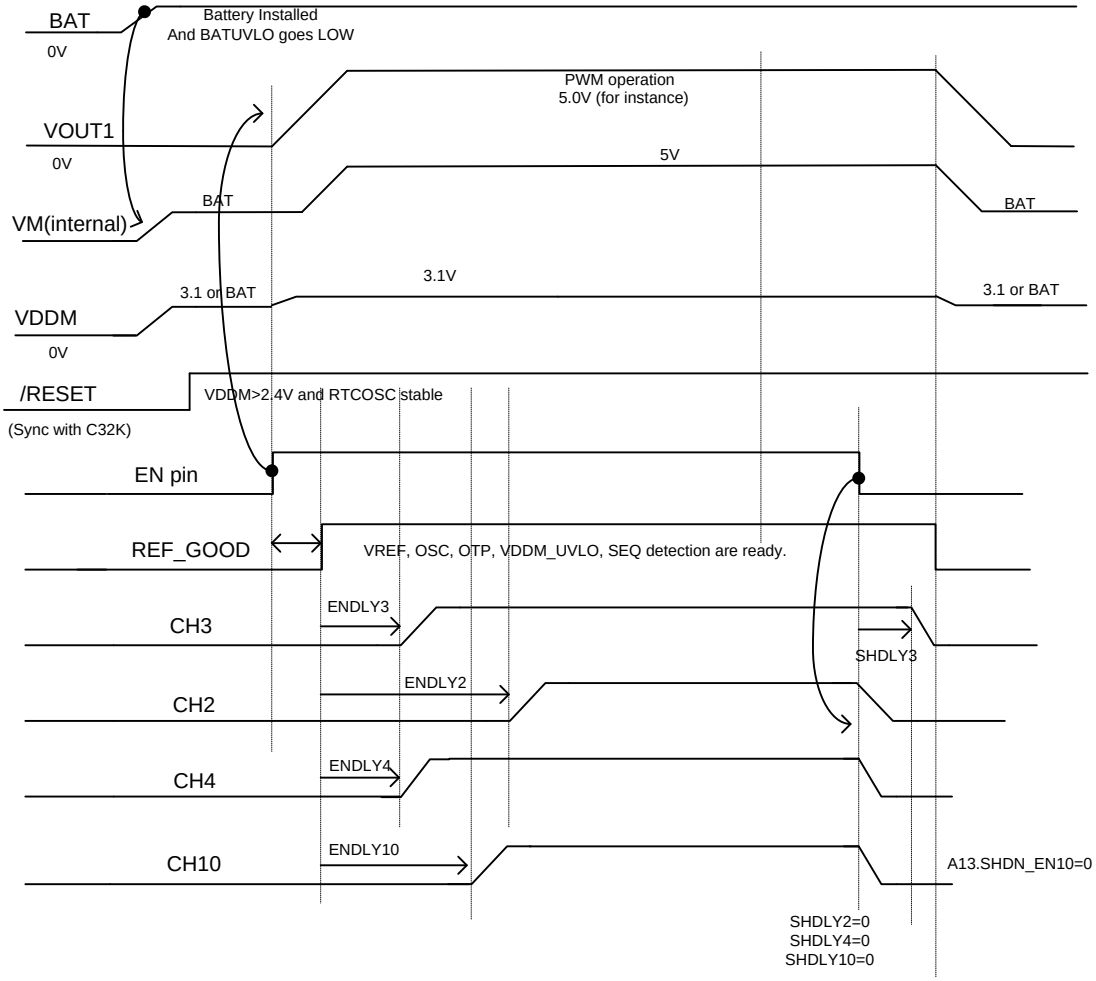
Furthermore, according to the logic high and low level threshold voltage, both 1.8V and 3V logic are compatible. If it isn't used, the SYNC pin must be connected to GND.



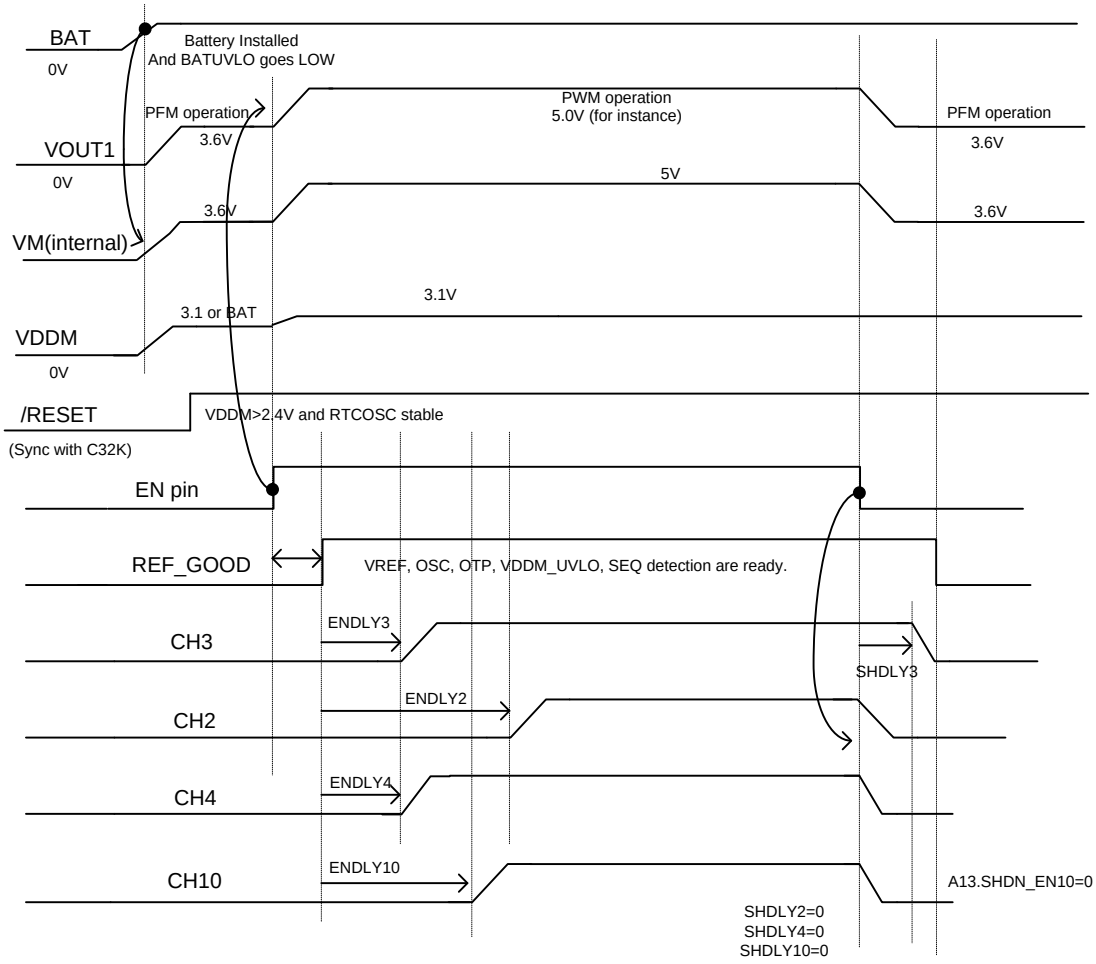
If the clock of SYNC is 12MHz, VDDM is not recommended as pull-up power voltage. Other power domains can be used if they fit the logic high and logic low threshold voltage.

Power On/Off Sequence

Part.A : Li (SHDN_PFM1 = 0)



Part.B : 2AA (SHDN_PFM1 = 1)



CH1 :

For 2AA case, as long as the BAT voltage is higher than UVLO and EN pin = L, CH1 keeps working in PFM mode 3.6V (default SHDN_EN1 = 1). However, when A14.PWM1 = 1, EN pin = H and the VDDM voltage is higher than UVLO, CH1 will switch from PFM mode to PWM mode.

As for Li battery case, to save electricity, when BAT voltage is higher than UVLO and EN pin = L, the CH1 would be off and truly shutdown (default SHDN_EN1 = 0)

CH2/3/4 :

CH2, CH3 and CH4 are both enabled by EN pin and with turn on delay time defined in I^2C register A9 to A10.

CH10 :

CH10 is also equipped PFM operation to reduce operating quiescent current for memory self-refresh application. When EN = H, I^2C registers can be set to ready to get into standby mode. (Set SHDN_EN1 = 1 and SHDN_EN10 = 1)

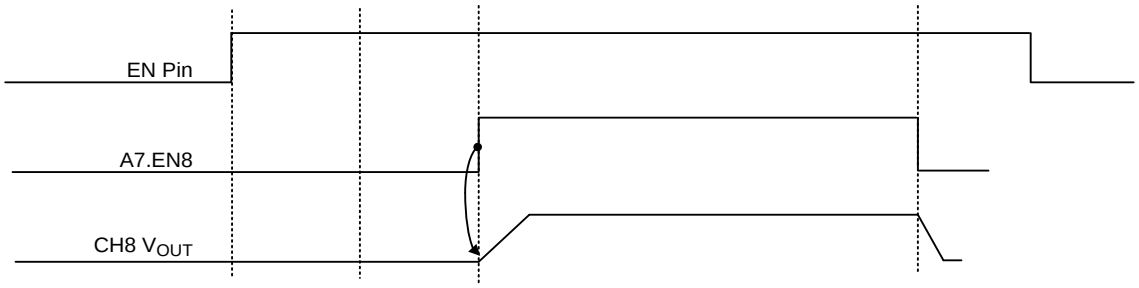
And then EN goes low, IC will get into standby mode with CH1 and CH10 operating in PFM mode.

If BAT > 2.8V is guaranteed, SHDN_EN1 could be 0 to save electricity in standby mode.

As for back to shutdown mode, EN goes high, and to set I²C registers back to shutdown mode (SHDN_EN10 = 0 and SHDN_EN1 = 0 for Li battery. SHDN_EN10 = 0 and SHDN_EN1 keeps 1 for 2AA) and then EN goes low finally.

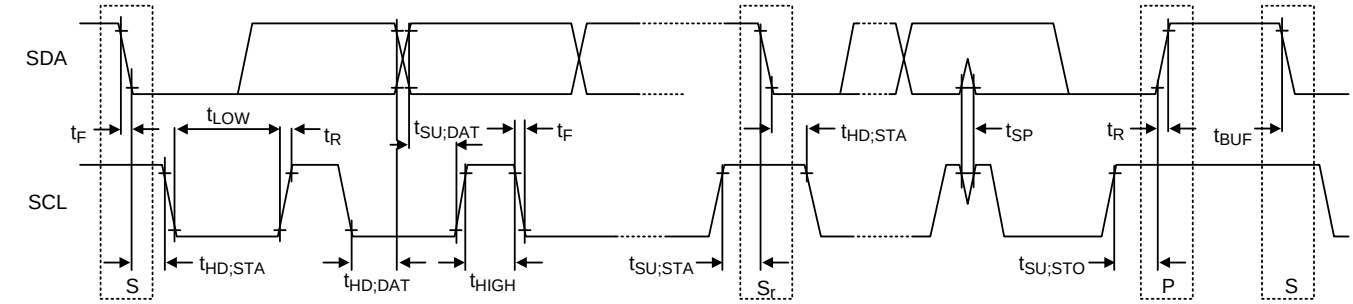
Power Sequence with Delay Time

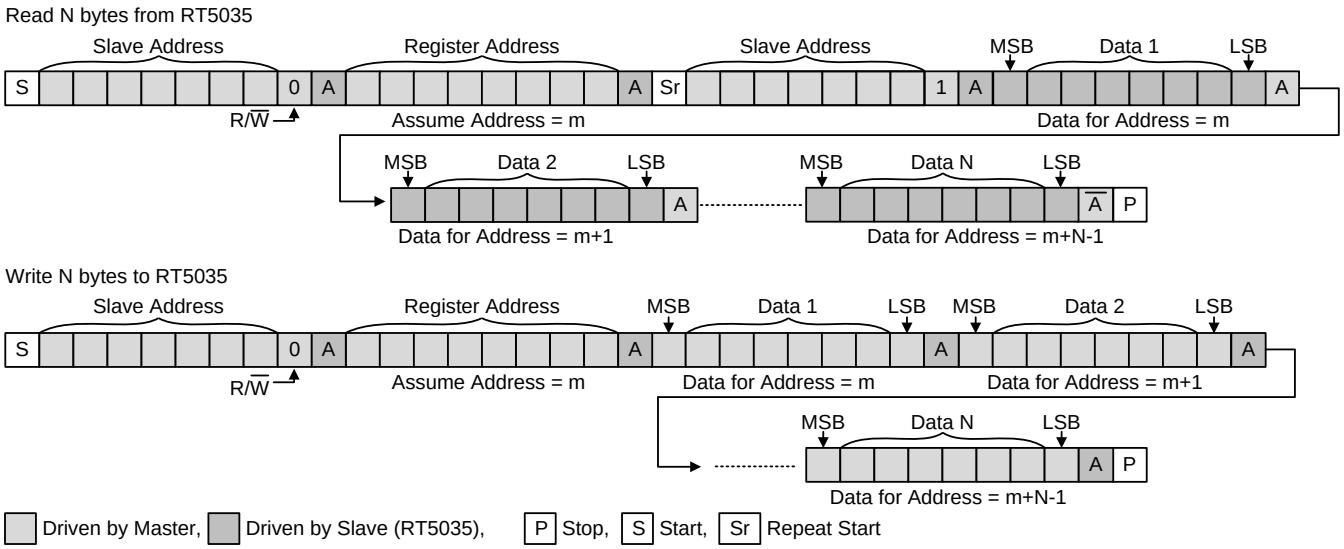
The start point referred by ENDLYx delay time begins when the EN pin goes high. For instance, A14.EN8 = 1, CH8 turns on immediately.



I²C Register Information

The RT5035A/B I²C interface power must be supplied by either VOUT2 or an equal potential node. If $\overline{\text{RESET}}$ = Low, I²C read/write can not function. The RT5035A/B I²C slave address = 0011000 (7bits). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :





I²C Register File

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1	0X01	Meaning	VOUT1				VOUT2			
		Default	1	1	1	1	1	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
VOUT1			Setting of CH1 Output Voltage (Range : 5.3V to 3.6V, Default = 3.6V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	5.3V	0100	4.9V	1000	4.5V	1100	4V
			0001	5.2V	0101	4.8V	1001	4.4V	1101	3.9V
			0010	5.1V	0110	4.7V	1010	4.3V	1110	3.8V
			0011	5V	0111	4.6V	1011	4.2V	1111	3.6V
VOUT2			Setting of CH2 Output Voltage (Range : 3.65V to 2.9V, Default = 3.25V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	3.65V	0100	3.45V	1000	3.25V	1100	3.05V
			0001	3.6V	0101	3.4V	1001	3.2V	1101	3V
			0010	3.55V	0110	3.35V	1010	3.15V	1110	2.95V
			0011	3.5V	0111	3.3V	1011	3.1V	1111	2.9V
Note : If CH1 operate in PFM mode (the bit A14.PWM1 = 0), VOUT1 = 3.6V only										

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A2	0X02	Meaning	VOUT3				VOUT4			
		Default	Decided by SEQ				Decided by SEQ			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
VOUT3			Setting of CH3 Output Voltage (Range : 1.3V to 1V, Default is setting by SEQ)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	1.3V	0100	1.22V	1000	1.14V	1100	1.04V
			0001	1.28V	0101	1.2V	1001	1.12V	1101	1.02V
			0010	1.26V	0110	1.18V	1010	1.1V	1110	1V
			0011	1.24V	0111	1.16V	1011	1.06V	1111	REF
VOUT4			Setting of CH4 Output Voltage (Range : 2.14V to 1.35V, Default is setting by SEQ)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	2.14V	0100	2V	1000	1.84V	1100	1.5 V
			0001	2.1V	0101	1.96V	1001	1.8V	1101	1.46V
			0010	2.06V	0110	1.92V	1010	1.76V	1110	1.39V
			0011	2.04V	0111	1.88V	1011	1.54V	1111	1.35V

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A3	0X03	Meaning	Reserved	VOUT5			VOUT6			
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
VOUT5			Setting of CH5 Output Voltage (Range : 2V to 1.2V, Default = 1.2V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	2V	010	1.5V	100	1.26V	110	1.2V
			001	1.8V	011	1.35V	101	1.23V	111	REF
VOUT6			Setting of CH6 Output Voltage (Range : 3V to 1.2V, Default = 2.7V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	3V	0100	2.6V	1000	2.2V	1100	1.7V
			0001	2.9V	0101	2.5V	1001	2V	1101	1.5V
			0010	2.8V	0110	2.4V	1010	1.9V	1110	1.4V
			0011	2.7V	0111	2.3V	1011	1.8V	1111	1.2V

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A4	0X04	Meaning	VOUT8			DIM7				
		Default	0	1	0	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
VOUT8			Setting of CH8 Output Voltage (Range : 5.2V to 1.5V, Default = 5V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	5.2V	010	5V	100	3.4V	110	3V
			001	5.1V	011	3.5V	101	3.3V	111	1.5V
DIM7			Defines LED current dimming ratio of CH7 The dimming ratio is (DIM7 + 1) / 32. DIM7 define FB7 regulation voltage = 0.3V x (DIM7 + 1) / 32							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A5	0X05	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	VOUT10		
		Default	0	0	0	0	0	by SEQ		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
VOUT10			Setting of CH10 Output Voltage (Range : 1.52V to 1.2V, Default = SEQ Setting)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	1.52V	010	1.37V	100	1.25V	110	1.2V
			001	1.5V	011	1.35V	101	1.22V	111	REF

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A6	0X06	Meaning	Reserved	Reserved	DIS10	DIS5	DIS4	DIS3	Reversed	Reserved
		Default	0	0	0	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
DIS10			1 : CH10 would discharge VOUT10 node when it turns off. 0 : CH10 would not discharge VOUT10 node when it turns off.							
DIS5			1 : CH5 would discharge VOUT5 node when it turns off. 0 : CH5 would not discharge VOUT5 node when it turns off.							
DIS4			1 : CH4 would discharge VOUT4 node when it turns off. 0 : CH4 would not discharge VOUT4 node when it turns off.							
DIS3			1 : CH3 would discharge VOUT3 node when it turns off. 0 : CH3 would not discharge VOUT3 node when it turns off.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A7	0X07	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	OVP7		
		Default	0	0	0	0	0	1	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
OVP7			Setting CH7 OVP threshold at VOUT7 node in Step-Up mode (Range : 8V to 25V, Default = 20V)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			000	8V	010	12V	100	16V	110	20V
			001	10V	011	14V	101	18V	111	25V

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A8	0X08	Meaning	Reserved							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
Reserved										

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A9	0X09	Meaning	ENDLY3				ENDLY2			
		Default	Decided by SEQ				Decided by SEQ			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
ENDLY3			Setting ENDLY3 for CH3 Power on delay time (2ms x ENDLY3).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms
ENDLY2			Setting ENDLY2 for CH2 Power on delay time (2ms x ENDLY2).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A10	0X0A	Meaning	ENDLY10				ENDLY4			
		Default	Decided by SEQ				Decided by SEQ			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
ENDLY10			Setting ENDLY10 for CH10 Power on delay time (2ms x ENDLY10).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms
ENDLY4			Setting ENDLY4 for CH4 Power on delay time (2ms x ENDLY4).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A11	0X0B	Meaning	SHDLY3				SHDLY2			
		Default	Decided by SEQ				Decided by SEQ			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
SHDLY3			Setting SHDLY3 for CH3 Power off delay time (2ms x SHDLY3).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms
SHDLY2			Setting SHDLY2 for CH2 Power off delay time (2ms x SHDLY2).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A12	0X0C	Meaning	SHDLY10				SHDLY4			
		Default	Decided by SEQ				Decided by SEQ			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
SHDLY10			Setting SHDLY10 for CH10 Power on delay time (2ms x SHDLY10).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms
SHDLY4			Setting SHDLY4 for CH4 Power on delay time (2ms x SHDLY4).							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			0000	0ms	0100	8ms	1000	16ms	1100	24ms
			0001	2ms	0101	10ms	1001	18ms	1101	26ms
			0010	4ms	0110	12ms	1010	20ms	1110	28ms
			0011	6ms	0111	14ms	1011	22ms	1111	30ms

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A13	0X0D	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHDN_PFM1	SHDN_PFM10
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
SHDN_PFM1			0 : CH1 is off when EN is low (Part. A default) 1 : CH1 operates at PFM when EN is low (Part. B default)							
SHDN_PFM10			0 : CH10 is off when EN is low 1 : CH 10 operates at PFM when EN is low							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A14	0X0E	Meaning	PWM1	ENSW4	EN4	EN5	EN6	EN7	EN8	PWM10
		Default	1	0	1	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	A	A	A	A	A	A	A	A
PWM1			1 : Means CH1 in Peak-Current Control PWM synchronous rectified operation mode. 0 : Means CH1 in PFM asynchronous rectified operation mode.							
ENSW4			1 : Enable SW4. 0 : Disable SW4							
EN4			1 : Enable CH4 0 : Disable CH4							
EN5			1 : Enable CH5 0 : Disable CH5							
EN6			1 : Enable CH6 0 : Disable CH6							
EN7			1 : Enable CH7 0 : Disable CH7							
EN8			1 : Enable CH8 0 : Disable CH8							
PWM10			1 : Means CH10 in Peak-Current Control PWM synchronous rectified operation mode. 0 : Means CH10 in PFM mode							

Notes :
ENSW4, EN4/5/6/7/8 at A14 : enable (ENx = 1) or disable (ENx = 0) SW4/CH4/5/6/7/8
When EN pin goes high, CHx would turn on (after the delay time ENDLYx) if the bits ENx = 1.
The register byte A14 would be reset when the external EN input pin goes low.

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A15	0X0F	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SS	SYN_DIV
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
SYN_DIV			0: FREQ of RT5035A/B=FREQ of SYNC 1: FREQ of RT5035A/B=FREQ of SYNC/6							
SS			0: Spread spectum OFF 1: Spread spectum ON							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A16	0X10	Meaning	Reserved	Reserved	Reserved	Reserved	DIS9	BAT_UVLO		Reserved
		Default	0	0	0	0	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
DIS9			0: No discharge VDDM when BATUVLO occurs. 1: Discharge VDDM when BATUVLO occurs.							
BAT_UVLO (Li)			BAT UVLO Setting Voltage (Range : 2.4V to 2.7V, Default = 2.6V) (Part. A)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			00	2.4V	01	2.5V	10	2.6V	11	2.7V
BAT_UVLO (2AA)			BAT UVLO Setting Voltage (Range : 1.7V to 2V, Default = 1.7V) (Part. B)							
			Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
			00	1.7V	01	1.8V	10	1.9V	11	2V

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A17	0X11	Meaning	Reserved	RTCAJ						
		Default	0	0	1	1	1	1	0	0
		Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
RTCAJ			Finely tune the RTC time counting frequency by adjusting (RTCAJ − 60) / 2 ppm. Hence, the tuning range is −30ppm to 33ppm.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A18	0X12	Meaning	BUSY	Reversed	RTCT_SEC					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
BUSY			1: RTC is busy and the writing access is not allowed							
RTCT_SEC[5:0]			Stores the SECOND field of RTC time. That is 0 to 59.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A19	0X13	Meaning	Reversed	Reversed	RTCT_MIN					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
RTCT_MIN[5:0]			Stores the MINUTE field of RTC time. That is 0 to 59.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A20	0X14	Meaning	MODE_12H	AM/PM	Reversed	RTCT_HR				
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
MODE_12H/24H			0 = 24H, 1 = 12H							
AM/PM			0 = AM, 1 = PM							
RTCT_HR[4:0]			Stores the HOUR field of RTC time. That is 0 to 23 (24hour format).							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A21	0X15	Meaning	Reversed	Reversed	RTCT_YEAR					
		Default	0	0	0	0	1	1	0	1
		Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
RTCT_YEAR[6:0]			Stores the YEAR field of RTC time. That is 0 to 63. RTCT_YEAR = 0 means the year 2000. Hence, RT5035A/B can count till the year 2063.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A22	0X16	Meaning	RTC MONTH							
		Default	Reversed	Reversed	Reversed	Reversed	RTCT_MON			
		Read/Write	0	0	0	0	0	0	0	1
		Reset Condition	C	C	C	C	C	C	C	C
RTCT_MON [3:0]			Stores the MONTH field of RTC time. That is 1 to 12. RTCT_MON = 1 means January.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A23	0X17	Meaning	RTCT_WEEK			RTCT_DAY				
		Default	1	1	0	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
RTCT_WEK [2:0]			Stores the DAY-of-WEEK field of RTC time. That is 0 to 6. RTCT_WEK = 0 means Sunday. RTCT_WEK = 1 means Monday. RT5035A/B cannot calculate automatically the field based on other fields. (YEAR, MONTH, DATE).							
RTCT_DAY[4:0]			Stores the DATE field of RTC time. That is 1 to 31, depending on the month. RTCT_DAY [4:0] = 1 means 1st day of each month. RT5035A/B supports leap year counting.							

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A24	0X18	Meaning	USER[7:0]							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
A25	0X19	Meaning	USER[15:8]							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
A26	0X1A	Meaning	USER[23:16]							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A27	0X1B	Meaning	USER[31:24]							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
USER[31:0]			USER[31:0] at A24 to A27: Stores user's data. It is like a SARM, which accesses via I^2C.							

Reset Condition

A	External EN pin goes low.
B	A0 to A13 and A15 : Reset when ($\overline{\text{RESET}}$ = L) occurs.
C	A16 to A27: Reset when RTC Reset occurs.

Output Voltage List

I²C Register Value	VOUT1 4bit	VOUT2 4bit	VOUT3 4bit	VOUT4 4bit	VOUT5 3bit	VOUT6 4bit	VOUT8 3bit	VOUT10 3bit
0	5.3	3.65	1.3	2.14	2	3	5.2	1.52
1	5.2	3.6	1.28	2.1	1.8	2.9	5.1	1.5
2	5.1	3.55	1.26	2.06	1.5	2.8	*** 5**	1.37
3	5	3.5	1.24	2.04	1.35	*** 2.7**	3.5	1.35
4	4.9	3.45	1.22	2	1.26	2.6	3.4	1.25
5	4.8	3.4	1.2	1.96	1.23	2.5	3.3	1.22
6	4.7	3.35	1.18	1.92	***1.2**	2.4	3	1.2
7	4.6	3.3	1.16	1.88	REF (0.8)	2.3	1.5	REF (0.8)
8	4.5	*** 3.25**	1.14	1.84		2.2		
9	4.4	3.2	1.12	*** 1.8**		2		
10	4.3	3.15	1.1	1.76		1.9		
11	4.2	3.1	1.06	1.54		1.8		
12	4	3.05	1.04	1.5		1.7		
13	3.9	3	1.02	1.46		1.5		
14	3.8	2.95	1	1.39		1.4		
15	*** 3.6**	2.9	REF (0.8)	1.35		1.2		

* : Default value

VOUT3/4/10 Default Voltage is selected by the SEQ pin and latched at the moment when $\overline{\text{RESET}}$ goes high.

SEQ ID

The SEQ pin pull down resistance R_{SEQ} defines Power on/off Sequence and Default Voltage.

SEQ ID	R_{SEQ} Range (kΩ)	Typical R_{SEQ}(kΩ)	Power on Procedure
SEQ #0	Connect to Power (>0.2V, <AVDD) before EN goes high		Reserved
SEQ #1	80> R_{SEQ} >20	40	Refer Table. SEQ1
SEQ #2	20> R_{SEQ} >5	10	Refer Table. SEQ2
SEQ #3	5> R_{SEQ} >1.25	2.5	Refer Table. SEQ3
SEQ #4	1.25> R_{SEQ} or connect to GND (<0.2V)	0.625 or short to GND	Refer Table. SEQ4
SEQ #5	R_{SEQ} >80 or floating (HZ)	120 or HZ	Refer Table. SEQ5

SEQ1

Register	Item	Code	Value
A2	VOUT3	1101	1.02V
A2	VOUT4	1001	1.8V
A5	VOUT10	111	REF
A9	ENDLY3	0111	14ms
A9	ENDLY2	1011	22ms
A10	ENDLY10	1001	18ms
A10	ENDLY4	1001	18ms
A11	SHDLY3	1010	20ms
A11	SHDLY2	0000	0ms
A12	SHDLY10	0000	0ms
A12	SHDLY4	0000	0ms

SEQ2

Register	Item	Code	Value
A2	VOUT3	1101	1.02V
A2	VOUT4	1001	1.8V
A5	VOUT10	101	1.22V
A9	ENDLY3	0111	14ms
A9	ENDLY2	1001	18ms
A10	ENDLY10	1001	18ms
A10	ENDLY4	1001	18ms
A11	SHDLY3	1010	20ms
A11	SHDLY2	0000	0ms
A12	SHDLY10	0000	0ms
A12	SHDLY4	0000	0ms

SEQ4

Register	Item	Code	Value
A2	VOUT3	1000	1.14V
A2	VOUT4	1001	1.8V
A5	VOUT10	011	1.35V
A9	ENDLY3	0111	14ms
A9	ENDLY2	1001	18ms
A10	ENDLY10	1001	18ms
A10	ENDLY4	1001	18ms
A11	SHDLY3	1010	20ms
A11	SHDLY2	0000	0ms
A12	SHDLY10	0000	0ms
A12	SHDLY4	0000	0ms

SEQ3

Register	Item	Code	Value
A2	VOUT3	1111	REF
A2	VOUT4	1001	1.8V
A5	VOUT10	111	REF
A9	ENDLY3	0111	14ms
A9	ENDLY2	1001	18ms
A10	ENDLY10	1001	18ms
A10	ENDLY4	1001	18ms
A11	SHDLY3	1010	20ms
A11	SHDLY2	0000	0ms
A12	SHDLY10	0000	0ms
A12	SHDLY4	0000	0ms

SEQ5

Register	Item	Code	Value
A2	VOUT3	1101	1.02V
A2	VOUT4	1001	1.8V
A5	VOUT10	011	1.35V
A9	ENDLY3	0111	14ms
A9	ENDLY2	1001	18ms
A10	ENDLY10	1001	18ms
A10	ENDLY4	1001	18ms
A11	SHDLY3	1010	20ms
A11	SHDLY2	0000	0ms
A12	SHDLY10	0000	0ms
A12	SHDLY4	0000	0ms

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.63W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

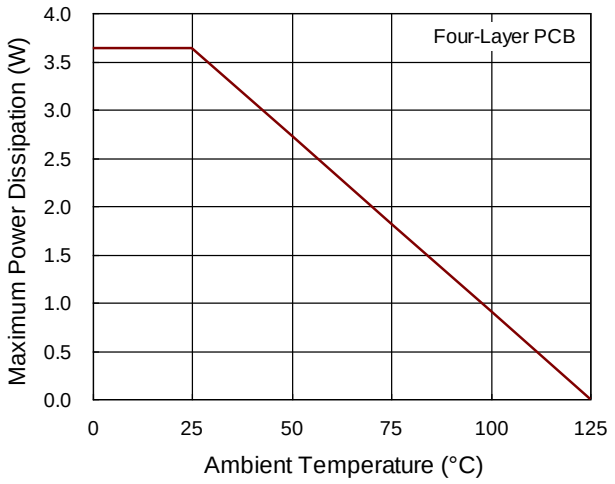


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT5035A/B. Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT5035A/B through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT5035A/B, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.
- For the 32-kHz oscillator to the best performance, observe the following guidelines :
- Place the crystal and its components close to the oscillator side and the oscillator pins.
- Ensure that the ground plane under the oscillator and its components are of good quality.
- Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Use a short connection between the two crystal load capacitors and route the common connection to the oscillator ground reference.

- Place a ceramic capacitor for noise filtering from RTCPWR to RTCGND with short connections.
- Place the C32K (logic output signal) output so that the return ground current runs back to RTCGND. Do not route the trace close to the oscillator input.

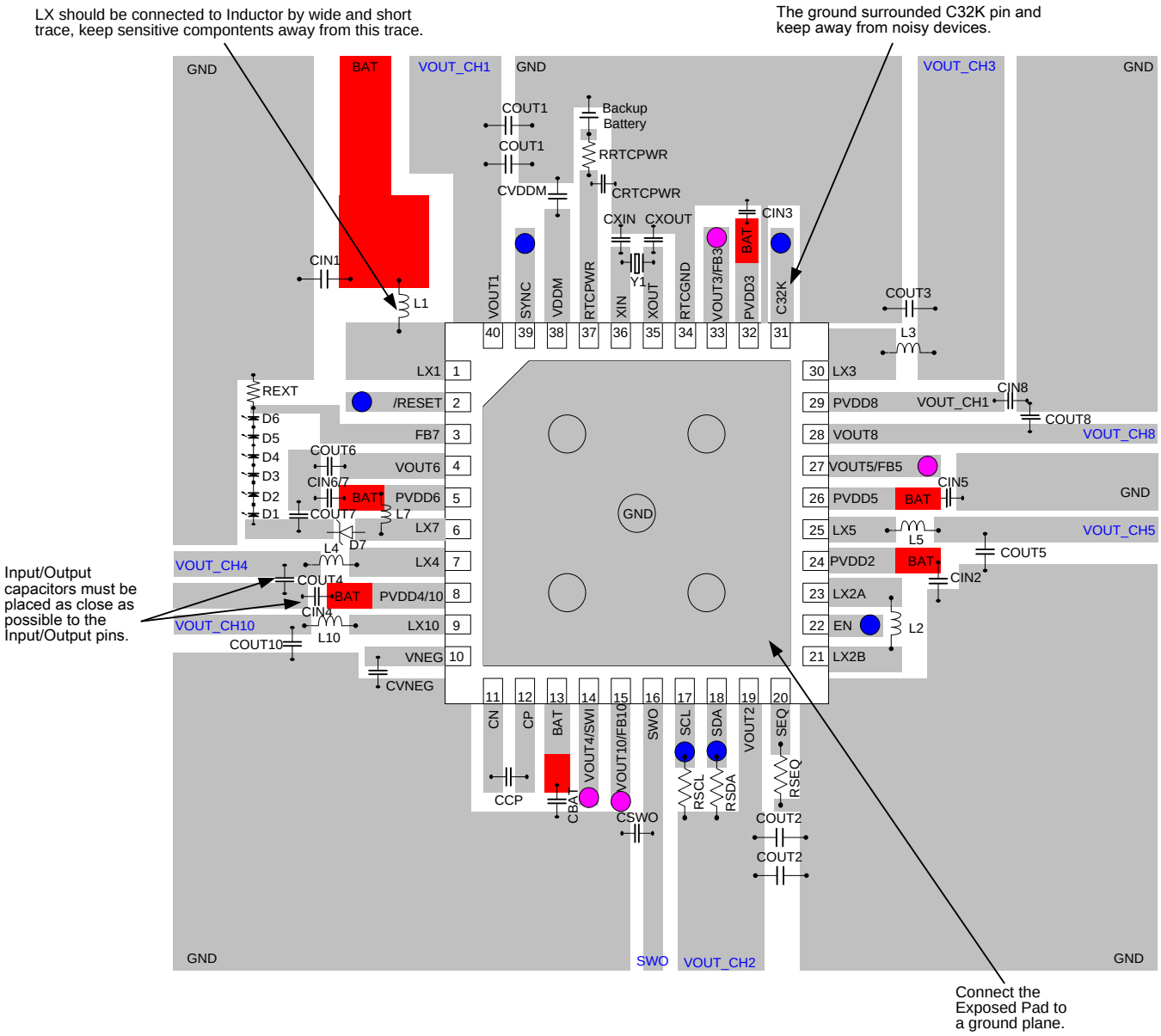


Figure 2. PCB Layout Guide

Max Load of Every Channel

Purpose	RT5035A/B	Current Limit	Max Load	Condition (V_{IN} → V_{OUT})
VDDM and V_{MOTOR}	CH1	3.5A	1200mA	3V → 5V
VI/O	CH2	3A	900mA	3V → 3.3V
VCORE	CH3	3A	2A	3V → 1.1V
VMEM	CH4	1.5A	700mA	3V → 1.8V
CMOS_D	CH5	1.5A	500mA	3V → 2.2V
CMOS_A	CH6	450mA	300mA	3V → 2.7V
Load SW	SW4	900mA	500mA	1.8V → 1.8V
WLED	CH7	0.8A	30mA	6 WLED
Generic LDO	CH8	300mA	200mA	V_{IN} – V_{OUT} > 150mV
Keep-Alive LDO	CH9	100mA	50mA	VIN – VOUT > 300mV
VMEM	CH10	1.5A	700mA	3V → 1.35V

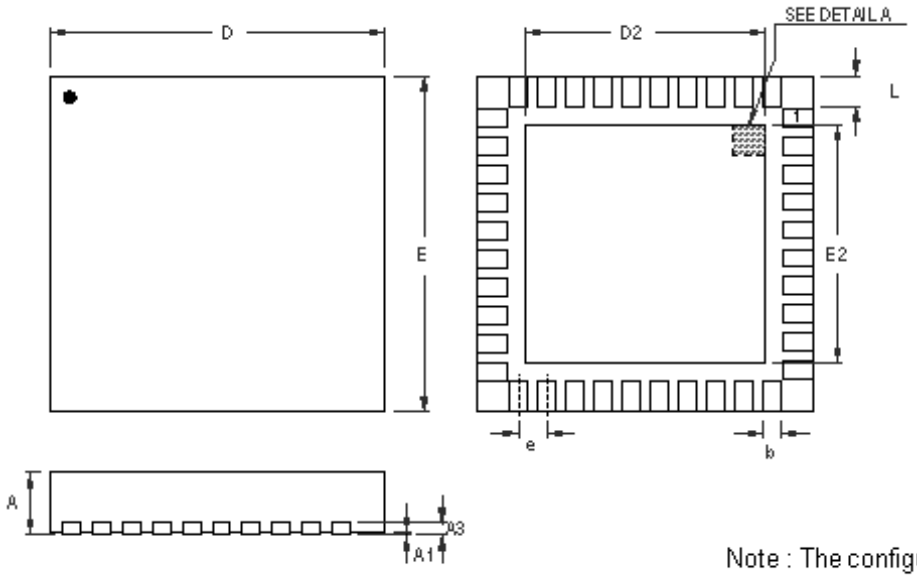
Protection Act

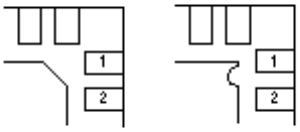
	Protection Type	Threshold (Typical Value)	Delay Time	Protection Method	Reset Method
VDDM	Over Voltage Protection	VDDM > 6V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	Restart if VDDM < 5.8V
BAT	UVLO	V_{BAT} < 2.4V (RT5035A)	No delay	Disable all channels	Restart if V_{BAT} > 2.6V (RT5035A), V_{BAT} > 1.7V (RT5035B)
		V_{BAT} < 1.5V (RT5035B)			
CH1	Current Limit (in PFM)	NMOS current > 0.8A	No delay	Turn off NMOS	Reset after min-off-time finish
	VOUT1 OVP (in PWM)	VOUT1 > 5.8V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	OCP (in PWM)	NMOS current > 3.5A	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT1 UVP (in PWM)	VOUT1< 2.25V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load protection (in PWM)	VOUT1 < target – 0.6V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low

	Protection Type	Threshold (Typical Value)	Delay Time	Protection Method	Reset Method
CH2	OCP	Inductor current > 3A	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT2 OVP	VOUT2 > 6V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT2 UVP	VOUT2 < 1.6V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load Protection	VOUT2 < target – 0.4V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
CH3	OCP	PMOS current > 3A	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT3 UVP	VOUT3 < 0.6V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load Protection	VOUT3 < target – 0.15V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
CH4	OCP	PMOS current > 1.5A	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT4 UVP	VOUT4 < 0.8V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load Protection	VOUT4 < target – 0.2V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
CH5	OCP	PMOS current > 1.5A	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT5 UVP	VOUT5 < 0.8V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load Protection	VOUT5 < target – 0.2V	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
CH6	UVP	A2.VOUT6 = 0 to 9, VOUT6<1.6V A2.VOUT6 = 10 to 15, VOUT6 < 0.8V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Current Limit	PMOS current > 450mA	No delay	Limit PMOS current	Reset by load

	Protection Type	Threshold (Typical Value)	Delay Time	Protection Method	Reset Method
CH7	OCP	NMOS current > 0.8A	100ms	Turn Off whole IC	VDDM power reset or EN = low
	OVP	LX7 > A4.OVP7 threshold	No delay	Turn Off CH7 only	VDDM power reset or EN = low
CH8	UVP	VOUT8 < target x 0.5	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Current Limit	PMOS current > 300mA	No delay	Limit PMOS current	Reset by load
CH9	Current limit	PMOS current > 100mA	No delay	Limit PMOS current	Reset by load
	VDDM UVLO	VDDM < 2.2V	No delay	Turn off whole IC, except CH9 and CH1 in PFM	Restart whole IC if EN = High and VDDM > 2.4V
	$\overline{\text{RESET}}$	VDDM < 2.2V	No delay	$\overline{\text{RESET}}$ goes low	Restart whole IC if EN = High and VDDM > 2.4V
CH10	OCP	PMOS current > 1.5A	100ms	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	VOUT10 UVP	VOUT10 < 0.8V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = low
	Over-Load Protection	VOUT10 < target – 0.2V	100ms	Turn off whole IC, except CH9 and CH1 in PFM	VDDM power reset or EN = low
RTCPWR	UVLO	RTCPWR < 1.9V	No delay	Clear RTC registers	RTCPWR > 2.2V
SW4 Load Switch	UVP	SWO < SWI – 0.9V Or SWO < 0.9V	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	VDDM power reset or EN = L
	Current Limit	NMOS current > 900mA	No delay	Limit N-MOSFET current	Reset by load
Thermal	Thermal Shutdown	Temperature > 160°C	No delay	Turn off whole IC, except CH9 and CH1 in PFM (only for 2AA)	Restart whole IC if EN = High and Temperature < 140°C

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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