TV System Power Management Solution

General Description

The RT5090C integrates 1 channel buck controller, 3 channels high efficiency synchronous buck converters, 1 LDO, I^{2}C Control interface and peripheral logical control.

The RT5090C support mute, AC OFF depop sound and quick setting storage while input power remove. The RT5090C is for 12V to 24V single input system or 12V to 24V + 3.3V standby system. The RT5090C is available in a WQFN-40L 5x5 package.

Ordering Information

RT5090C □□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

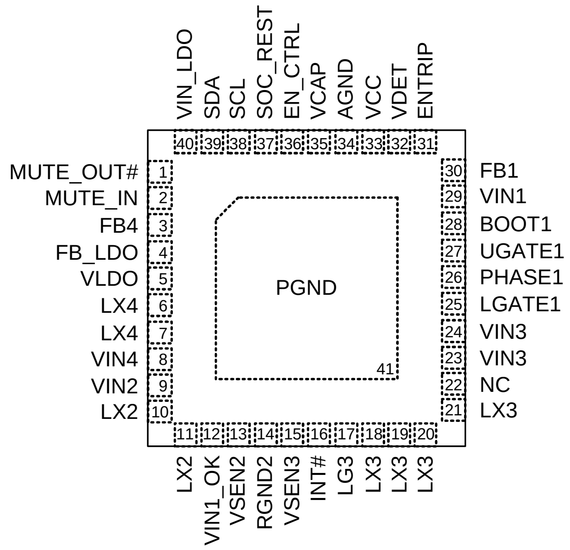
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

Features

- BUCK1
  - 5V Power Controller
  - External MOSFET
  - High Efficiency at Light Load (PSK)
- BUCK2
  - 3A Converter with PSK Mode
  - DVS with 10mV/Step
  - Programmable Output Voltage by I^{2}C, from 0.7V to 1.5V
- BUCK3
  - 6A Converter with PSK Mode
  - Support up to 6A with External Low Side MOSFET
  - DVS with 10mV/Step
  - Programmable Output Voltage by I^{2}C, from 0.7V to 1.5V
- BUCK4
  - 3A Converter with PSK Mode
  - Programmable Output Voltage
- LDO
  - Sourcing up to 0.6A
  - Programmable Output Voltage
- UV Protection : Latch or Hiccup Mode
- OV Protection : Only Latch Mode
- Power Up SOC Reset

Applications

- TV System

Marking Information

RT5090CGQW : Product Number

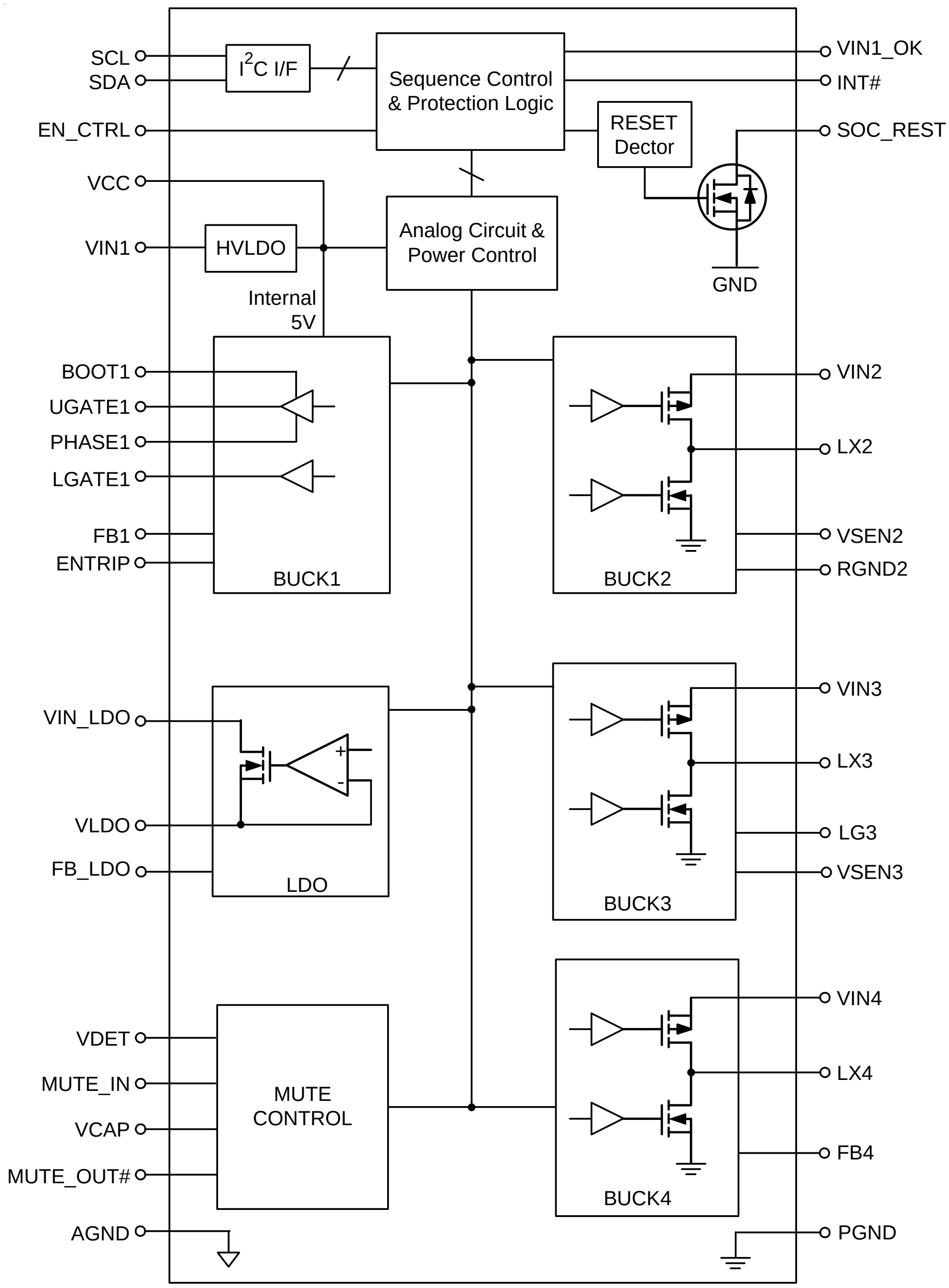
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	MUTE_OUT#	Output signal for mute and depop function.
2	MUTE_IN	Input signal for mute function.
3	FB4	BUCK4 feedback.
4	FB_LDO	LDO feedback.
5	VLDO	LDO output.
6, 7	LX4	Phase node for BUCK4 converter. Connect to inductor.
8	VIN4	Input voltage for BUCK4 converter. Input capacitors as close as possible to VIN4 pin.
9	VIN2	Input voltage for BUCK2 converter. Input capacitors as close as possible to VIN2 pin.
10, 11	LX2	Phase node for BUCK2 converter. Connect to inductor.
12	VIN1_OK	Power OK of input voltage. It is an open-drain output.
13	VSEN2	Remote voltage sense for BUCK2 converter. Connect to the positive side of the load for remote sensing.
14	RGND2	Remote ground sense for BUCK2 converter. Connect to the negative side of the load for remote sensing.
15	VSEN3	Remote voltage sense for BUCK3 converter. Connect to the positive side of the load for remote sensing.
16	INT#	Interrupt output. System information (Thermal, OVP, UVP and PGOOD). Pin is pulled low if an interrupt bit is set. The output goes high after the bit causing the interrupt in register INT has been read and written a 1b to clear the corresponding interrupt bit. The interrupt sources can be masked in register INT, so no interrupt is generated when the corresponding interrupt bit is set.
17	LG3	Low-side driver output. Connect directly to the low-side MOSFET gate for BUCK3 Converter. The MOSFET Ciss need to 500pF above.
18, 19, 20, 21	LX3	Phase node for BUCK3 converter. Connect to inductor.
22	NC	Not connected.
23, 24	VIN3	Input voltage for BUCK3 converter. Input Capacitors as close as possible to VIN3 pin.
25	LGATE1	Low-side driver output. Connect directly to the low-side MOSFET gate for BUCK1 controller.
26	PHASE1	High-side driver return path. Connect to the high-side MOSFET source for BUCK1 controller.
27	UGATE1	High-side driver output. Connect to high-side MOSFET gate for BUCK1 controller.
28	BOOT1	High-side driver supply. This pin supplies the high-side floating driver for BUCK1 controller. Connect through the C_{BOOT} capacitor to the PHASE1 pin.
29	VIN1	Input voltage for internal LDO.
30	FB1	BUCK1 feedback.

Pin No.	Pin Name	Pin Function
31	ENTRIP	BUCK1 enable and current limit setting (CS) input. Connect a resistor to GND to set the threshold for BUCK1 synchronous $R_{DS(ON)}$ sense. The GND to PHASE1 current limit threshold is 1/12th the voltage seen at CS over a 0.515V to 3V range. Leave CS floating or drive it above 4.5V to shutdown BUCK1.
32	VDET	Voltage detection for depop function. Connect to Input Power or Standby Power Ratio Voltage.
33	VCC	Device Power Supply. Internal LDO Supply from VIN1 or External Power Supply. With 4.7μF MLCC to AGND, as close as possible to VCC pin.
34	AGND	Analog ground.
35	VCAP	Connect to capacitor. Hold up capacitors to keep enough energy to supply control logic when remove input power for depop function.
36	EN_CTRL	Enable control. The power on of rails when this pin be pulled high, vice versa. The rails alive or turn-off in sleep mode (DC OFF) can by register 0x08 setting.
37	SOC_REST	Reset signal for SOC.
38	SCL	Clock input for the I^2C interface.
39	SDA	Data line for the I^2C interface.
40	VIN_LDO	Power input for LDO. Input Capacitors as close as possible to VIN_LDO pin.
41 (Exposed Pad)	PGND	Power ground. Connect to GND.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN1 to GND ---------- –0.3V to 29V
- Supply Input Voltage, VIN2,VIN3, VIN4, VIN_LDO, VCC to GND ---------- –0.3V to 6.5V
- BOOT1 to PHASE1 ---------- –0.3V to 6.5V
- PHASE1 to GND
  DC ---------- –0.3V to 29V
  < 100ns ---------- –2V to 36V
- UGATE1 to PHASE1
  DC ---------- –0.3V to 6.5V
  < 100ns ---------- –2V to 7.5V
- LGATE1 to GND
  DC ---------- –0.3V to 6.5V
  < 100ns ---------- –2V to 7.5V
- UGATE1 to GND
  DC ---------- $(V_{PHASE1} – 0.3V)$ to $V_{BOOT1} + 0.3V)$
  < 100ns ---------- $(V_{PHASE1} – 2V)$ to $V_{BOOT1} + 0.3V)$
- Switch Node Voltage, LX2, LX3, LX4 to GND ---------- –0.3V to 6.5V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN1 ---------- 8V to 27V
- Supply Input Voltage, VIN3, VIN4 ---------- 4.5V to 5.5V
- Supply Input Voltage, VCC ---------- 3V to 5.5V
- Supply Input Voltage, VIN2 ---------- 2.7V to 5.5V
- Supply Input Voltage, VIN_LDO ---------- 2.7V to 3.6V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN1} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Supply Voltage	V_{IN1}		8	--	27	V
Supply Current						
Sleep Supply Current	I_Q	V_{CC} = 5V, all rail turn on and buck no switching, measure I(VIN1)	--	1	--	mA
UVLO						
VCC_UVLO Rising Threshold	V_{UVLO_R}	VCC rising	--	2.75	2.9	V
VCC_UVLO Falling Threshold	V_{UVLO_F}	VCC falling	2.45	2.6	--	V
Logic Threshold						
EN_CTRL input High Voltage	V_{EN_H}	Measure EN_CTRL rising	1.2	--	--	V
EN_CTRL input Low Voltage	V_{EN_L}	Measure EN_CTRL falling	--	--	0.4	V
EN_CTRL Input Current	I_{EN_CTRL}	V_{EN_CTRL} = 2V	--	1	5	μA
VIN1_POR Rising Threshold	$V_{VIN1\_POR\_R}$	VIN1 rising	--	7.8	--	V
VIN1_POR Falling Threshold	$V_{VIN1\_POR\_F}$	VIN1 falling	--	7.6	--	V
VIN1_OK Pull Down Capability	$R_{ON\_VIN1\_OK}$	Open drain, measure pull low MOSFET $R_{DS(ON)}$	--	10	--	Ω
SOC_REST Pull Down Capability	$R_{ON\_SOC\_REST}$	Open drain, measure pull low MOSFET $R_{DS(ON)}$	--	10	--	Ω
INT# Pull Down Capability	$R_{ON\_INT\#}$	Open drain, measure pull low MOSFET $R_{DS(ON)}$	--	10	--	Ω
VDET Threshold			0.98	1	1.02	V
Thermal Hot Die						
Thermal HD Threshold	T_{HD}		--	120	--	°C
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
MUTE Function						
MUTE_IN Input High Voltage	$V_{MUTE\_IN\_H}$	Measure $V_{MUTE\_IN\_H}$ rising	1.2	--	--	V
MUTE_IN Input Low Voltage	$V_{MUTE\_IN\_L}$	Measure $V_{MUTE\_IN\_L}$ falling	--	--	0.4	V
MUTE_OUT#	R_{ON_MUTE}	Open drain, measure pull low MOSFET $R_{DS(ON)}$	--	10	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BUCK1						
Supply Current						
Supply Current (Quiescent)		VIN1>VIN1_UVLO, no switching	--	250	--	μA
Reference and Soft-Start						
Output Feedback Voltage	V_{FB}		1.188	1.2	1.212	V
Soft-Star Time	t_{SS}	VOUT soft-start time	--	1	--	ms
Current Limit						
Current Limit Setting Current	I_{CS}		45	50	55	μA
Current Limit Temperature Coefficient			--	4700	--	ppm/°C
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}	Controlled by I^2C 0x03[2:1] = 01h	--	450	--	kHz
Minimum Off-Time	t_{OFF}		150	400	500	ns
Minimum On-Time	t_{ON}		--	350	--	ns
Protections						
OVP Trip Threshold	V_{OVP}		--	120	--	%
OVP Propagation Delay	t_{OVPDLY}		--	5	--	μs
UVP Trip Threshold	V_{UVP}		--	60	--	%
UVP Propagation Delay	t_{UVPDLY}		--	5	--	μs
Zero Current Detection						
Zero Current Crossing Threshold	V_{PHASE_ZC}		–4	--	4	mV
Discharge Resistor						
Discharge Resistance	R_{DISCHG}	Controlled by I^2C 0x09[1:0] = 01h	--	100	--	Ω
Driver On-Resistor						
UGATE1 Driver Source	R_{UGATE1_sr}	V_{BOOT1} - V_{PHASE1} = 5V	--	3	6	Ω
UGATE1 Driver Sink	R_{UGATE1_sk}	V_{BOOT1} - V_{PHASE1} = 5V	--	1	2	Ω
LGATE1 Driver Source	R_{LGATE1_sr}	LGATE1, high state	--	3	6	Ω
LGATE1 Driver Sink	R_{LGATE1_sk}	LGATE1, low state	--	0.7	1.5	Ω
Dead Time	t_{D1_LU}	From LGATE1 falling to UGATE1 rising	--	30	--	ns
	t_{D1_UL}	From UGATE1 falling to LGATE1 rising	--	20	--	ns
Internal Boost Diode Resistance	R_{BOOT}	VCC to BOOT1, I_{BOOT1} = 10mA	--	40	80	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BUCK2						
Supply Voltage						
Supply Voltage	V_{IN2}		2.7	--	5.5	V
Supply Current						
Shutdown Supply Current		V_{EN} = 0V	--	--	3	μA
Quiescent Supply Current		Enable, no switching	--	200	--	μA
Reference and Soft-Start						
Output Voltage Scaling	V_{OUT2}	Controlled by I^2C 0x04[6:0]	0.7	--	1.5	V
Output Voltage	V_{OUT2}	0x04[6:0] = 32h, CCM	1.188	1.2	1.212	V
DC Output Voltage Programmable step	V_{STEP}		--	10	--	mV
Soft-Star Time	t_{SS}	V_{OUT2} soft-start time	--	1	--	ms
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON)\_H}$	V_{IN2} = 5V	--	70	--	mΩ
Switch On Resistance	$R_{DS(ON)\_L}$	V_{IN2} = 5V	--	55	--	mΩ
Current Limit						
Current Limit	I_{OC}	Valley current sense	--	4.5	--	A
DVS Step			--	10	--	mV/μs
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		--	1.5	--	MHz
Minimum Off-Time	t_{OFF}		--	120	--	ns
Protections						
OVP Trip Threshold	V_{OVP_TH}		--	120	--	%
OVP Timer Latch	t_{OVPDLY}		--	10	--	μs
UVP Trip Threshold	V_{UVP_TH}		--	60	--	%
UVP Timer Latch	t_{UVPDLY}		--	10	--	μs
Regulation						
Line Regulation			--	0.5	--	%
Load Regulation		CCM	--	0.5	--	%
Discharge Resistor						
Discharge Resistance	R_{DISCHG}		--	10	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BUCK3						
Supply Voltage						
Supply Voltage	V_{IN3}		4.5	5	5.5	V
Supply Current						
Shutdown Supply Current		V_{EN} = 0V	--	--	3	μA
Quiescent Supply Current		Enable, no switching	--	200	--	μA
Reference and Soft-Start						
Output Voltage Scaling	V_{OUT3}	Controlled by I^2C 0x05[6:0]	0.7	--	1.5	V
Output Voltage	V_{OUT3}	0x05[6:0] = 1Eh, CCM	0.99	1	1.01	V
DC Output Voltage Programmable step	V_{STEP}		--	10	--	mV
Soft-Star Time	t_{SS}	V_{OUT3} Soft-start time	--	1	--	ms
Driver On-Resistor						
LGATE3 Driver Source	R_{LGATE3_sr}	LGATE3, high state	--	3	6	Ω
LGATE3 Driver Sink	R_{LGATE3_sk}	LGATE3, low state	--	1.5	3	Ω
Dead Time	t_{D3_LU}	From LGATE3 falling to UGATE3 rising	--	30	--	ns
	t_{D3_UL}	From UGATE3 falling to LGATE3 rising	--	20	--	ns
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON)\_H}$	V_{IN3} = 5V	--	50	--	mΩ
Switch On Resistance	$R_{DS(ON)\_L}$	V_{IN3} = 5V	--	45	--	mΩ
Current Limit						
Current Limit (External Low Side MOSFET)	I_{OC_EXT}	I_{MAX} = 6A, peak current sense	--	9	--	A
DVS Step			--	10	--	mV/us
Switching Frequency						
Switching Frequency	f_{SW_6A}	6A application	--	1	--	MHz
Protections						
OVP Trip Threshold	V_{OVP_TH}		--	120	--	%
OVP Timer Latch	t_{OVPDLY}		--	10	--	μs
UVP Trip Threshold	V_{UVP_TH}		--	60	--	%
UVP Timer Latch	t_{UVPDLY}		--	10	--	μs
Regulation						
Line Regulation			--	0.5	--	%
Load Regulation		CCM	--	0.5	--	%
Discharge Resistor						
Discharge Resistance	R_{DISCHG}		--	10	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BUCK4						
Supply Voltage						
Supply Voltage	V_{IN4}		4.5	5	5.5	V
Supply Current						
Shutdown Supply Current		V_{EN} = 0V	--	--	3	μA
Quiescent Supply Current		Enable, no switching	--	200	--	μA
Reference and Soft-Start						
Output Voltage Scaling	V_{OUT4}		0.8	--	3.3	V
Output Feedback Voltage	V_{FB4}	CCM	0.588	0.6	0.612	V
Soft-Star Time	t_{SS}	V_{OUT4} soft-start time	--	1	--	ms
$R_{DS(ON)}$						
Switch On Resistance	$R_{DS(ON)\_H}$	V_{IN4} = 5V	--	70	--	mΩ
Switch On Resistance	$R_{DS(ON)\_L}$	V_{IN4} = 5V	--	55	--	mΩ
Current Limit						
Current Limit	I_{OC}	Valley current sense	3	3.6	--	A
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}		--	1	--	MHz
Minimum Off-time	t_{OFF}		--	120	--	ns
Protections						
OVP Trip Threshold	V_{OVP_TH}		--	120	--	%
OVP Timer Latch	t_{OVPDLY}		--	10	--	μs
UVP Trip Threshold	V_{UVP_TH}		--	60	--	%
UVP Timer Latch	t_{UVPDLY}		--	10	--	μs
Regulation						
Line Regulation			--	0.5	--	%
Load Regulation		CCM	--	0.5	--	%
Discharge Resistor						
Discharge Resistance	R_{DISCHG}		--	10	--	Ω

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LDO							
Supply Voltage							
Supply Voltage				2.7	3.3	3.6	V
Supply Current							
Shutdown Supply Current			V_{EN} = 0V	--	--	3	μA
Quiescent Supply Current			Enable	--	100	--	μA
Reference and Soft-Start							
Output Voltage Scaling		V_{OUT_VLDO}		0.8	--	2.5	V
Output Feedback Voltage		V_{FB_LDO}		0.792	0.8	0.808	V
Soft-Star Time		t_{SS}	V_{OUT_VLDO} soft-start time	--	1	--	ms
Dropout Voltage							
Dropout Voltage		V_{DROP}	I_{OUT} = 600mA, V_{IN_LDO} = 5V	--	300	--	mV
Current Limit							
Current Limit		I_{OC}		--	1	--	A
Protections							
OVP Trip Threshold		V_{OVP_TH}		--	120	--	%
OVP Timer Latch		t_{OVPDLY}		--	10	--	μs
UVP Trip Threshold		V_{UVP_TH}		--	60	--	%
UVP Timer Latch		t_{UVPDLY}		--	10	--	μs
Regulation							
Line Regulation				--	1	--	%
Load Regulation				--	1	--	%
Discharge Resistor							
Discharge Resistance		R_{DISCHG}		--	10	--	Ω
SOC_REST							
SOC_REST Lead Time		t_{LEAD}	All rails power good to SOC_REST rising edge lead time	5	6	--	ms
I²C							
SDA, SCL Input Voltage	High-Level			1.2	--	--	V
	Low-Level			--	--	0.4	V
Fast Mode							
SCL Clock Rate		f_{SCL}		--	--	400	kHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated		$t_{HD;STA}$		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	μs
Data Set-Up Time	$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and START Condition	t_{BUF}		1.3	--	--	μs
Rising Time of both SDA and SCL Signals	t_R		20	--	300	ns
Falling Time of both SDA and SCL signals	t_F		20	--	300	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

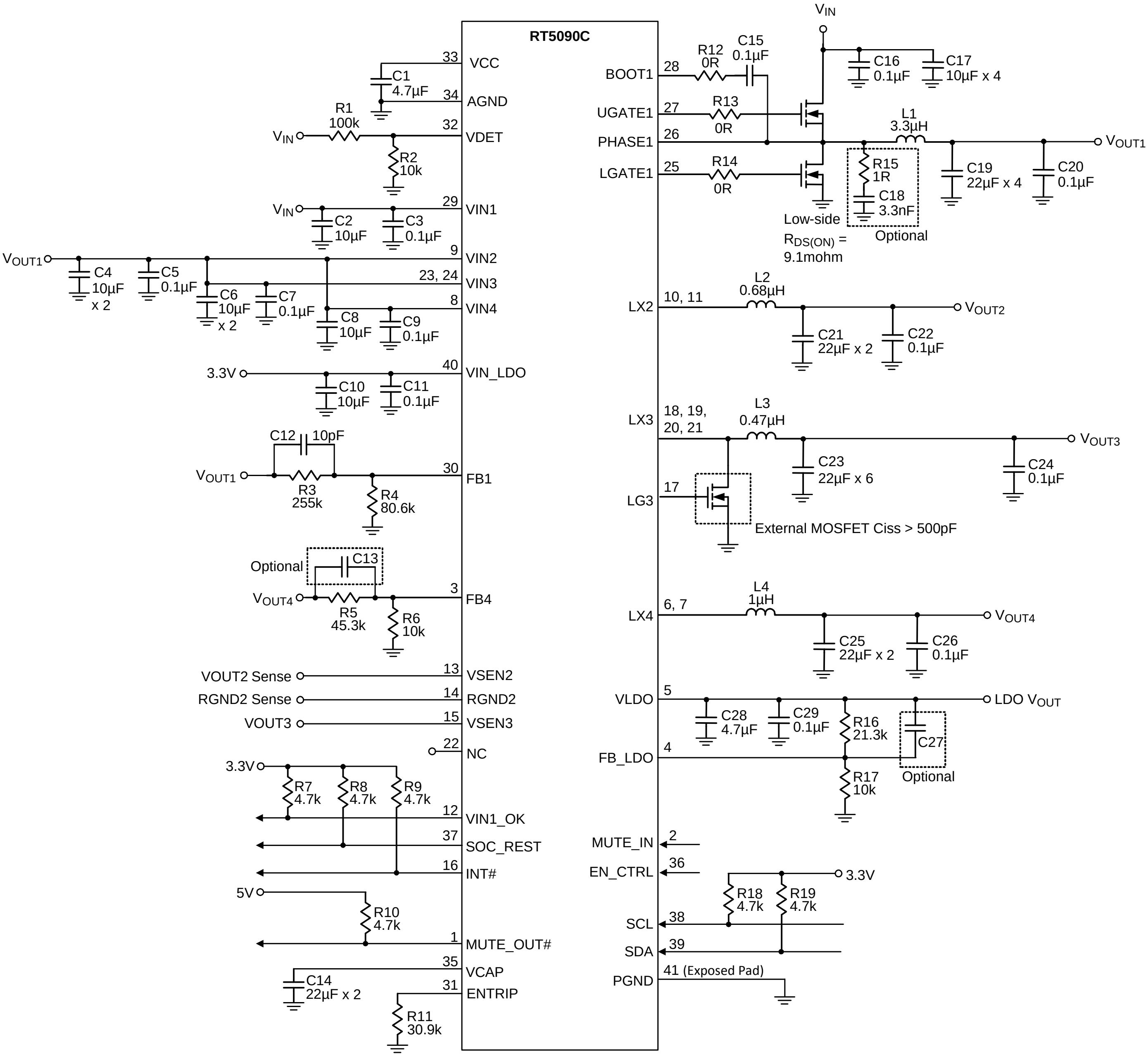


Figure 1. For 24V Single Input Power System

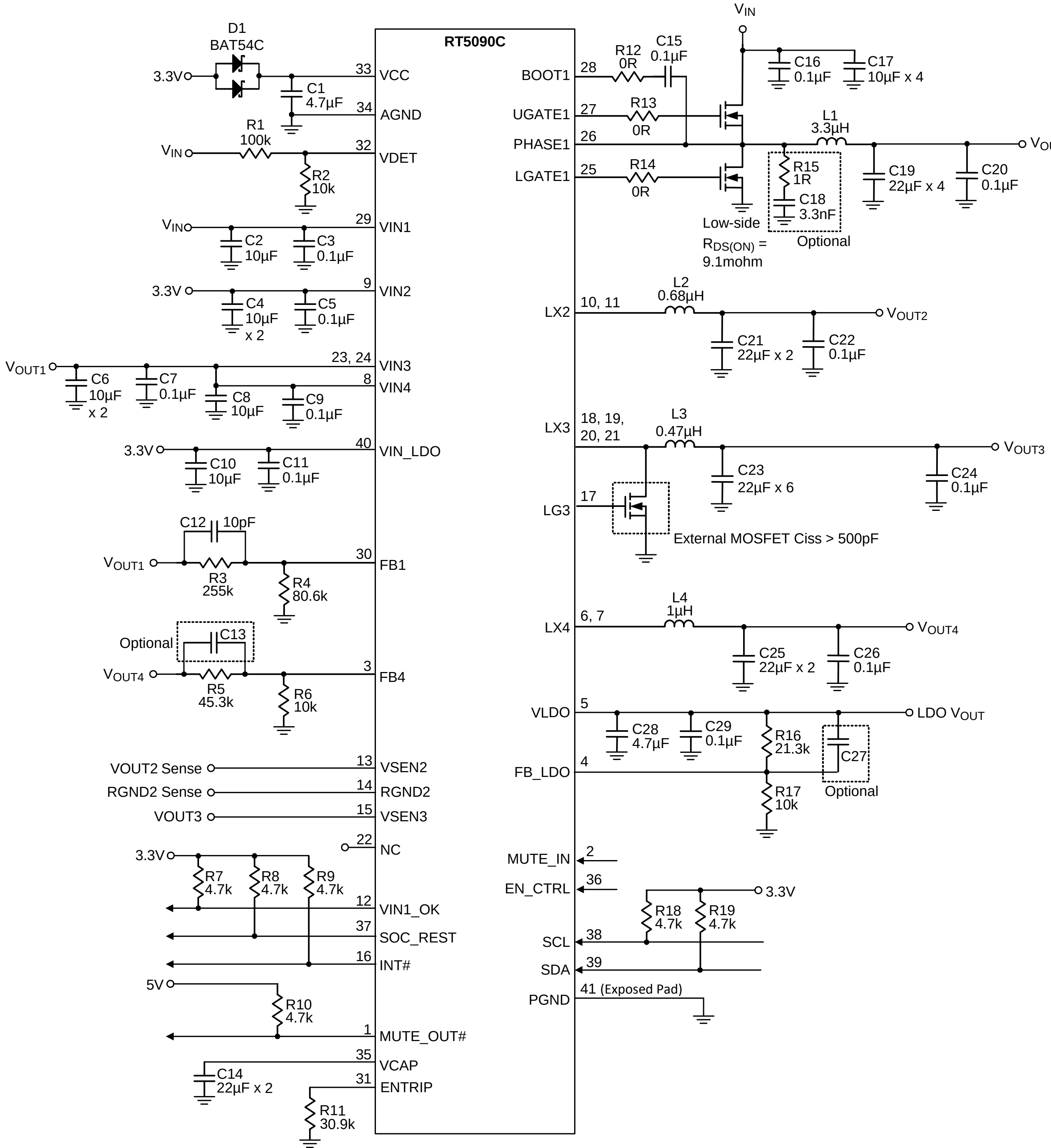
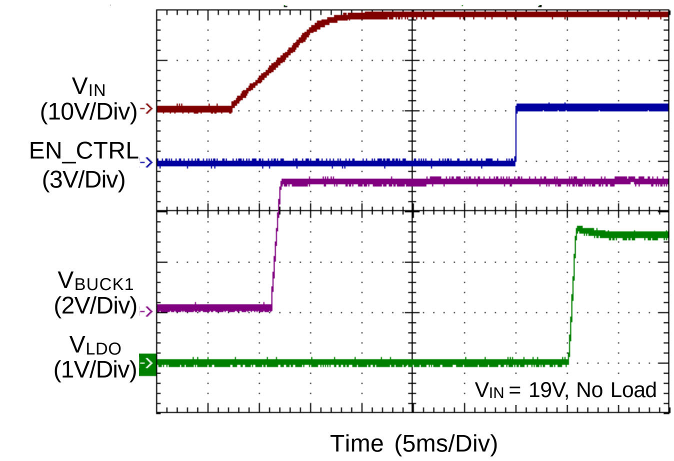


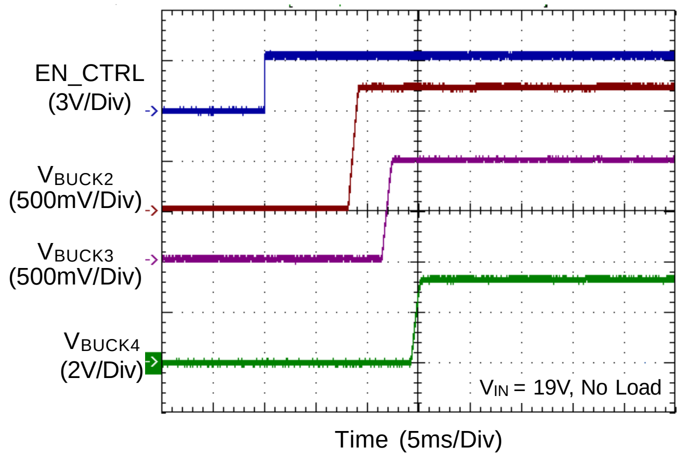
Figure 2. For 12V + 3.3V Standby System

Typical Operating Characteristics

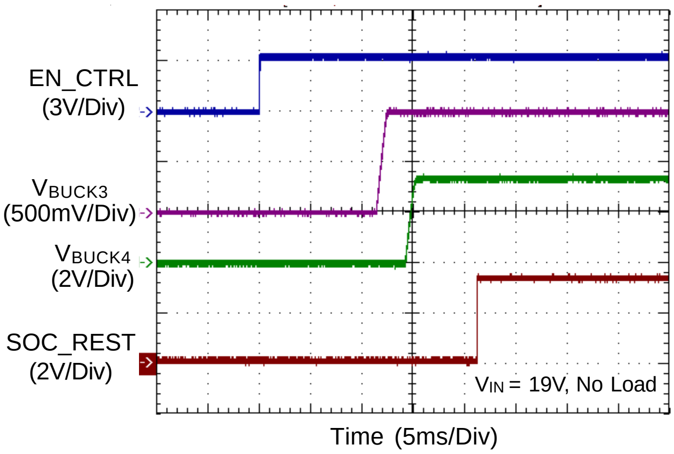
AC ON Sequence 1



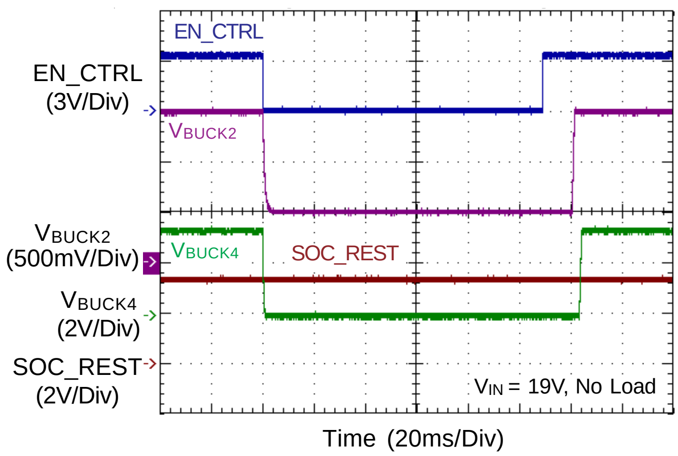
AC ON Sequence 2



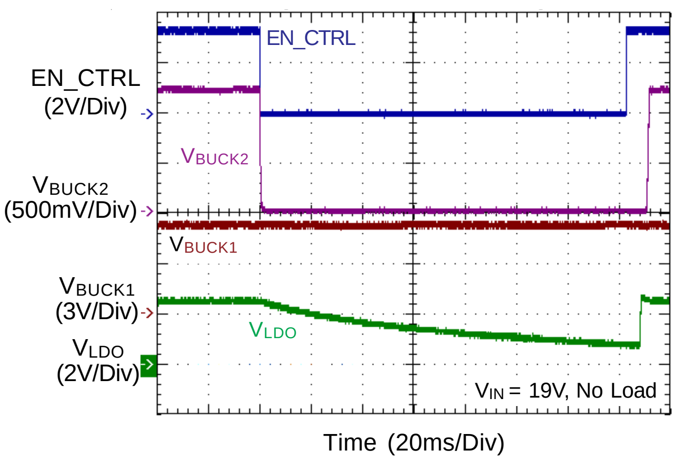
AC ON Sequence 3



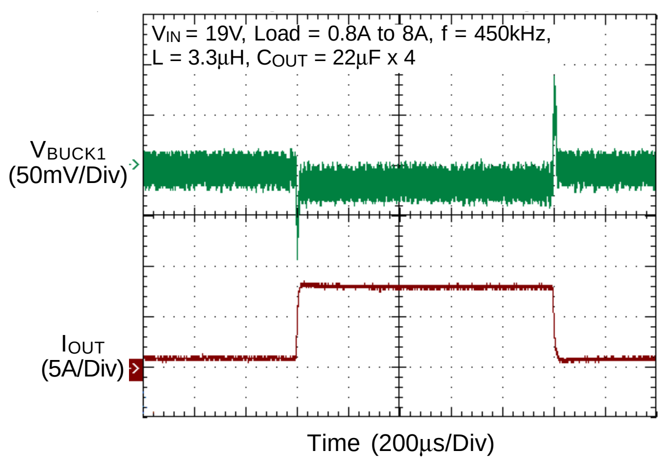
DC ON / OFF



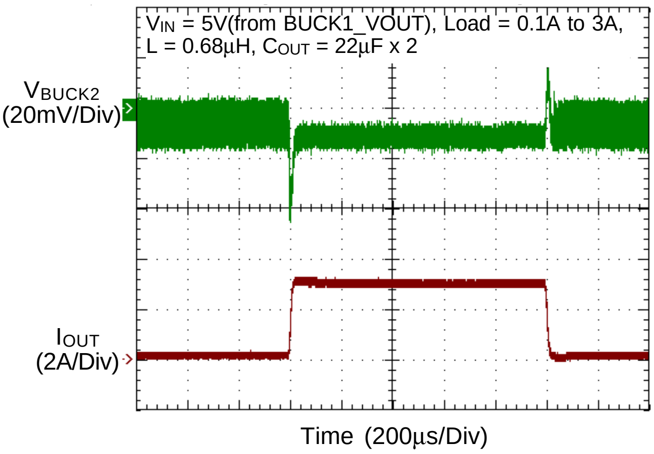
DC ON / OFF



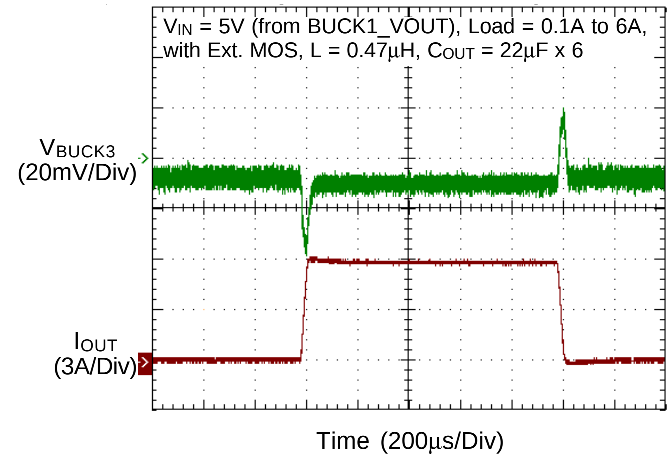
BUCK1 Load Transient



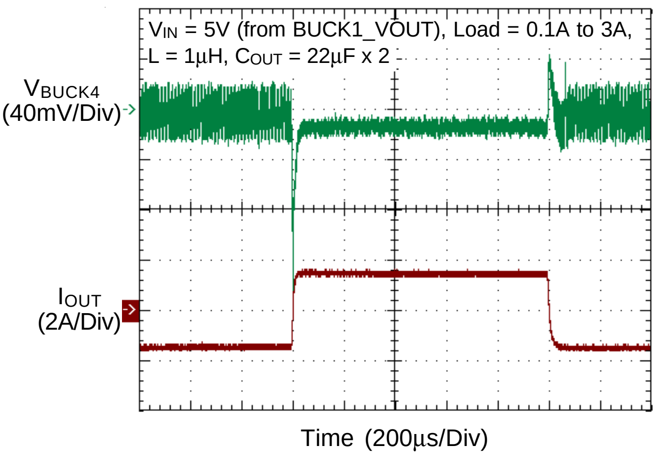
BUCK2 Load Transient



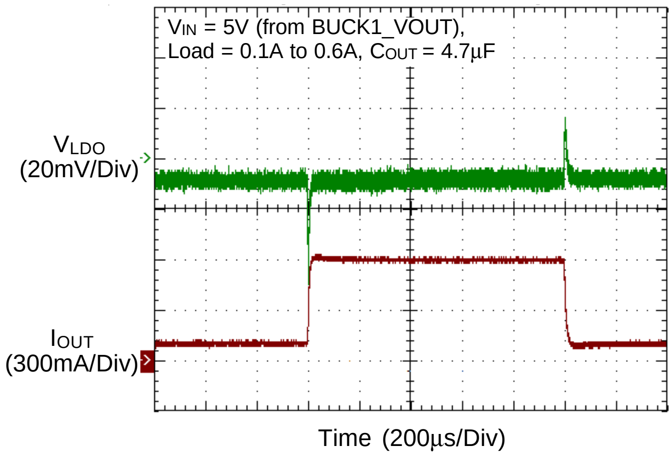
BUCK3 Load Transient



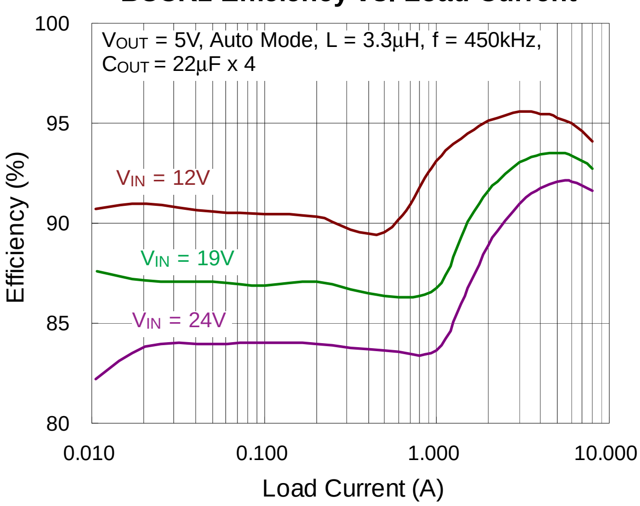
BUCK4 Load Transient



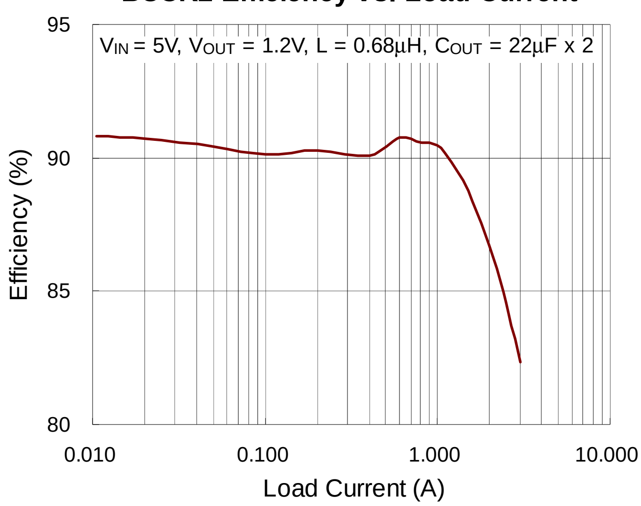
LDO Load Transient

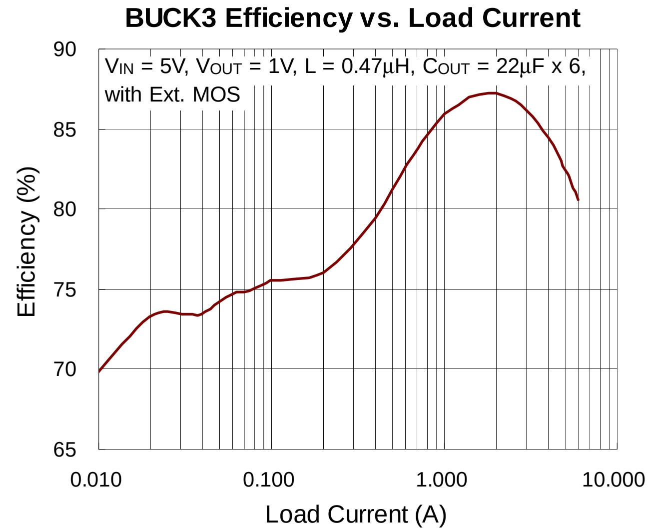


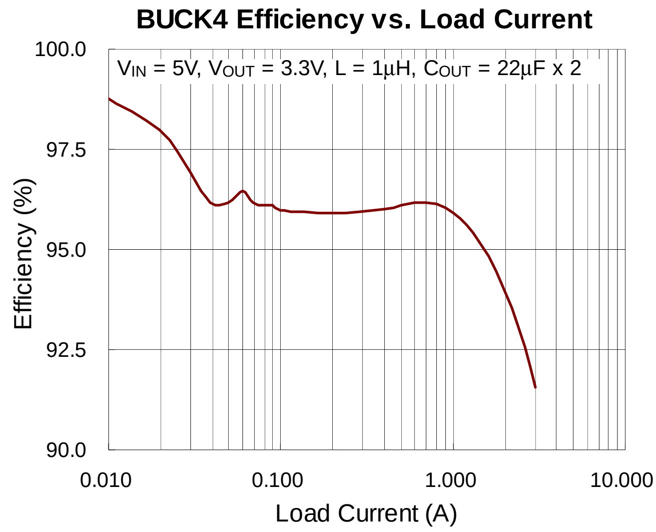
BUCK1 Efficiency vs. Load Current

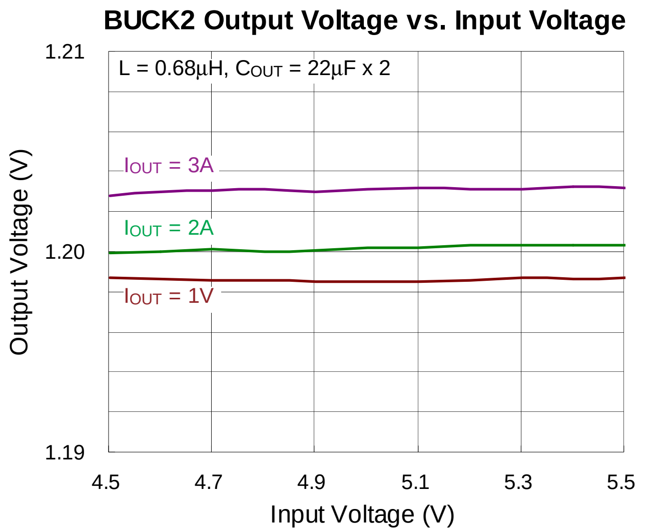


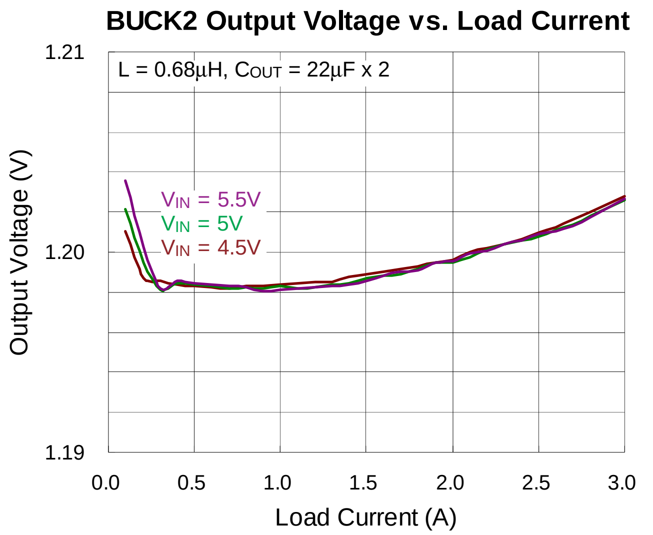
BUCK2 Efficiency vs. Load Current

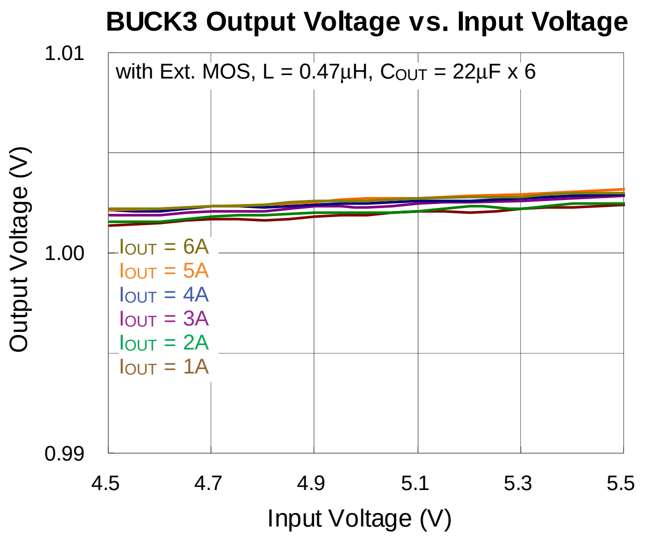


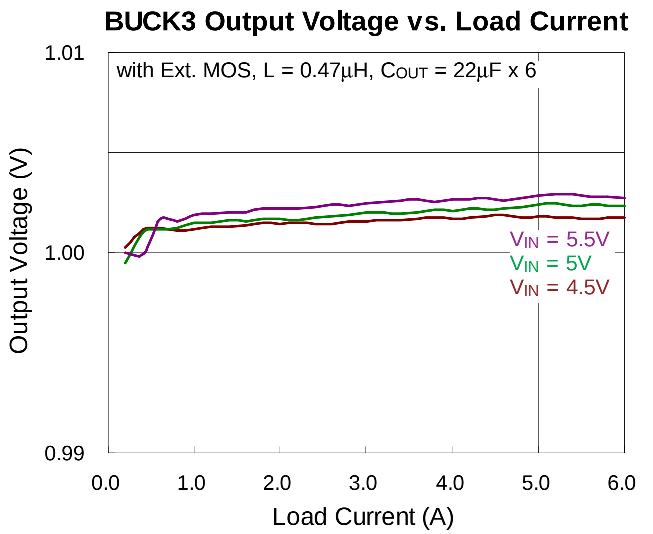

BUCK3 Efficiency vs. Load Current
VIN = 5V, VOUT = 1V, L = 0.47µH, COUT = 22µF x 6, with Ext. MOS
Efficiency (%)
90
85
80
75
70
65
0.010
0.100
1.000
10.000
Load Current (A)

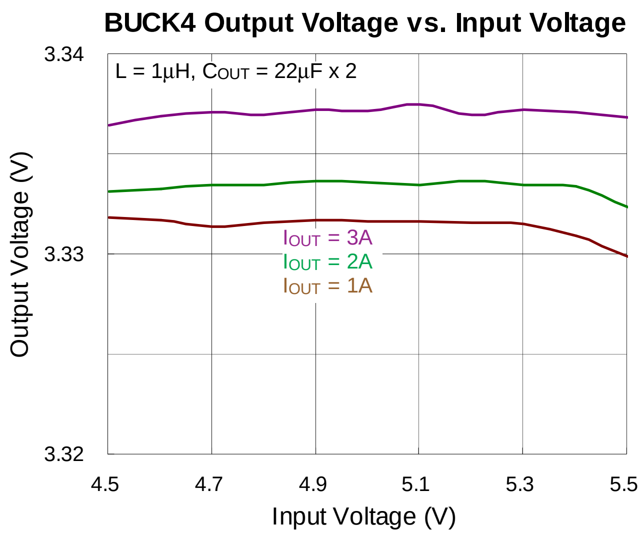

BUCK4 Efficiency vs. Load Current
VIN = 5V, VOUT = 3.3V, L = 1µH, COUT = 22µF x 2
Efficiency (%)
100.0
97.5
95.0
92.5
90.0
0.010
0.100
1.000
10.000
Load Current (A)

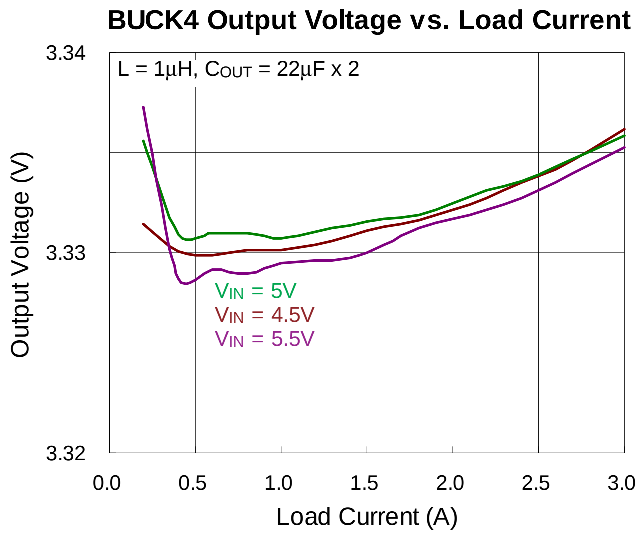

BUCK2 Output Voltage vs. Input Voltage
L = 0.68µH, COUT = 22µF x 2
IOUT = 3A
IOUT = 2A
IOUT = 1V
Output Voltage (V)
1.21
1.20
1.19
4.5
4.7
4.9
5.1
5.3
5.5
Input Voltage (V)

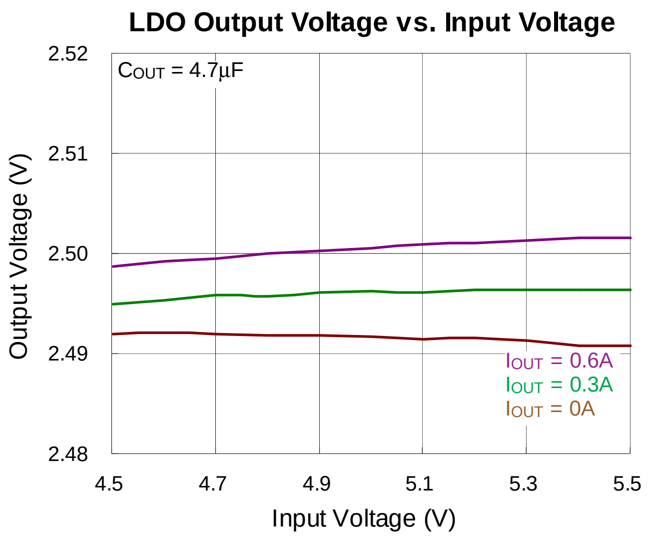

BUCK2 Output Voltage vs. Load Current
L = 0.68µH, COUT = 22µF x 2
VIN = 5.5V
VIN = 5V
VIN = 4.5V
Output Voltage (V)
1.21
1.20
1.19
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Load Current (A)

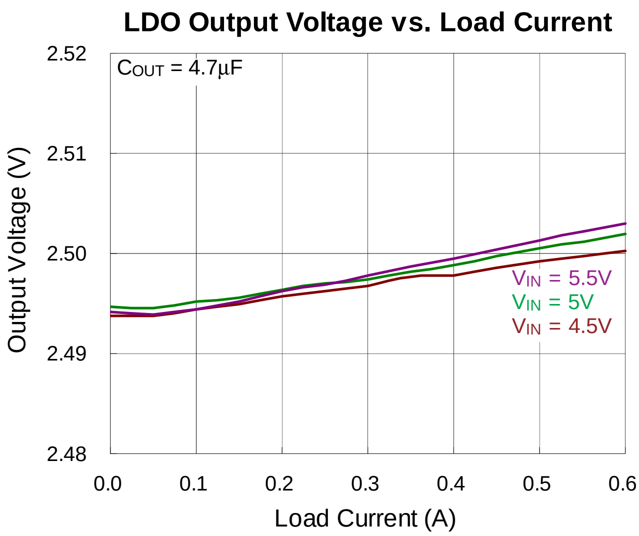

BUCK3 Output Voltage vs. Input Voltage
with Ext. MOS, L = 0.47µH, COUT = 22µF x 6
IOUT = 6A
IOUT = 5A
IOUT = 4A
IOUT = 3A
IOUT = 2A
IOUT = 1A
Output Voltage (V)
1.01
1.00
0.99
4.5
4.7
4.9
5.1
5.3
5.5
Input Voltage (V)


BUCK3 Output Voltage vs. Load Current
with Ext. MOS, L = 0.47µH, COUT = 22µF x 6
VIN = 5.5V
VIN = 5V
VIN = 4.5V
Output Voltage (V)
1.01
1.00
0.99
0.0
1.0
2.0
3.0
4.0
5.0
6.0
Load Current (A)


BUCK4 Output Voltage vs. Input Voltage
L = 1μH, COUT = 22μF x 2
IOUT = 3A
IOUT = 2A
IOUT = 1A
Output Voltage (V)
Input Voltage (V)
3.34
3.33
3.32
4.5
4.7
4.9
5.1
5.3
5.5


BUCK4 Output Voltage vs. Load Current
L = 1μH, COUT = 22μF x 2
VIN = 5V
VIN = 4.5V
VIN = 5.5V
Output Voltage (V)
Load Current (A)
3.34
3.33
3.32
0.0
0.5
1.0
1.5
2.0
2.5
3.0


LDO Output Voltage vs. Input Voltage
COUT = 4.7μF
IOUT = 0.6A
IOUT = 0.3A
IOUT = 0A
Output Voltage (V)
Input Voltage (V)
2.52
2.51
2.50
2.49
2.48
4.5
4.7
4.9
5.1
5.3
5.5

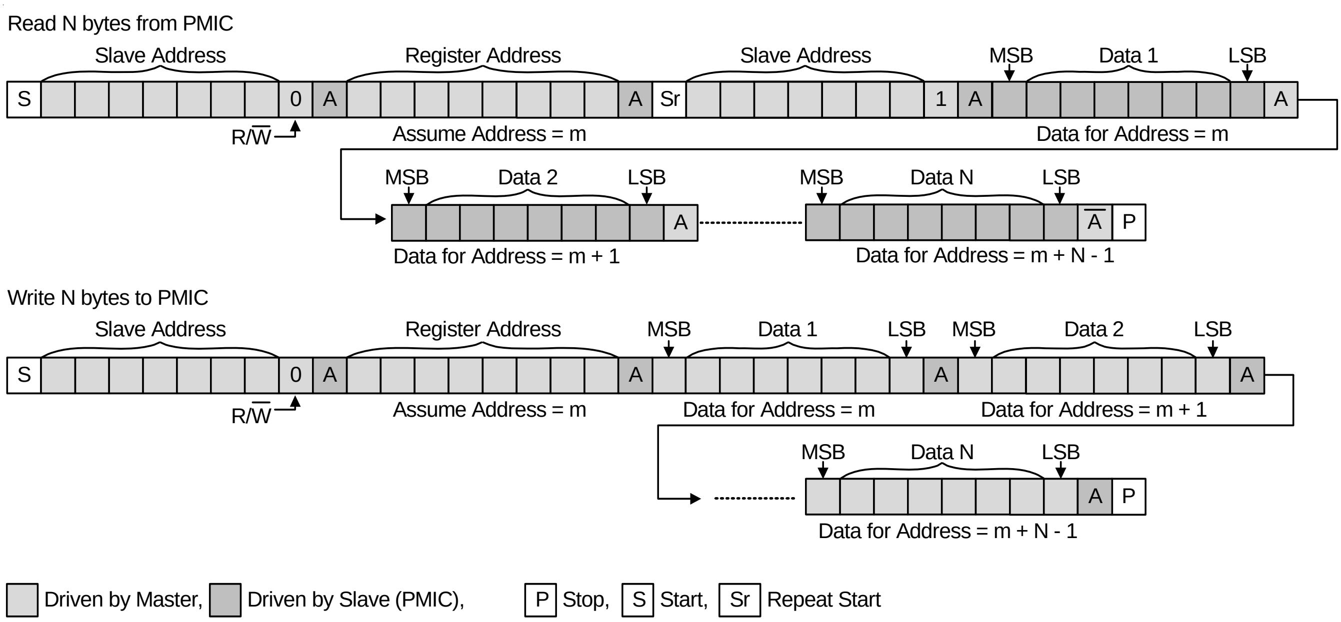

LDO Output Voltage vs. Load Current
COUT = 4.7μF
VIN = 5.5V
VIN = 5V
VIN = 4.5V
Output Voltage (V)
Load Current (A)
2.52
2.51
2.50
2.49
2.48
0.0
0.1
0.2
0.3
0.4
0.5
0.6

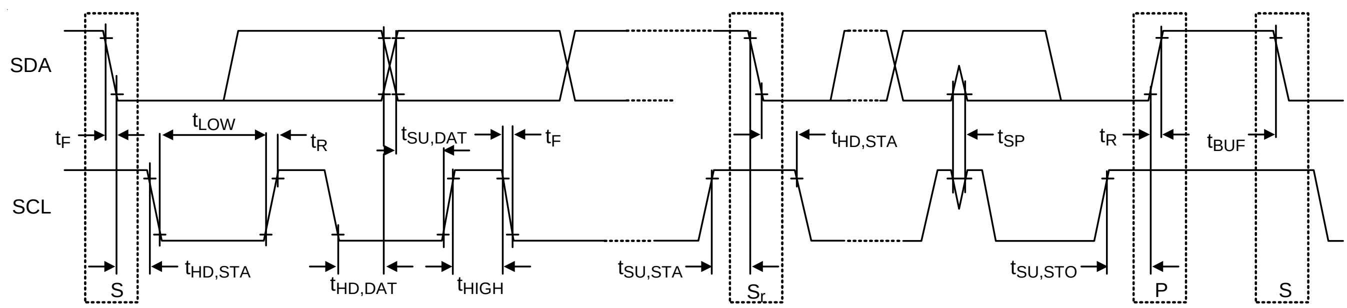
I^2C Interface

The default I^2C slave address = 7' b1100100 (0x64).

This I^2C does not have a stretch function.

I^2C interface support standard slave mode(100 kbps), and fast mode (400kbps). The write or read bit stream (N>1) is shown below :





Register Map

Address Offset	NAME	TYPE	Register Reset
0x00	MANUFACTURE_ID	RO	0x00
0x01	PRODUCT_ID	RO	0x00
0x02	REVISON_NUMBER	RO	0x00
0x03	BUCK1_REG	RW	0x02
0x04	BUCK2_SEL_REG	RW	0x32
0x05	BUCK3_SEL_REG	RW	0x1E
0x06	DCDCTRL0_REG	RW	0x00
0x07	ENABLE_REG	RW	0x00
0x08	DCDCTRL1_REG	RW	0x04
0x09	DISCHARGE	RW	0x1D
0x0A	PROTECTION MODE	RW	0x3E
0x0B	MUTE CONTROL	RW	0x01
0x0F	PGOOD Status	RO	0x00
0X10	OV_INT	RW	0x00
0X11	UV_INT	RW	0x00
0X12	PGOOD_INT	RW	0x00
0X13	HOT_DIE_INT	RW	0x0E
0X14	OV_MASK	RW	0x00
0X15	UV_MASK	RW	0x00
0X16	PGOOD_MASK	RW	0x3E
0X17	HOT_DIE_MASK	RW	0x00
0x2A	VIN1_OK_CTRL_Rail	RW	0x01

Address : 0x00 Description : Manufacturer ID number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MANUFACTURE_ID							
Rest Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	MANUFACTURE_ID		Return the MANUFACTURE_ID number : 0x00					

Address : 0x01 Description : Product ID number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRODUCT_ID							
Rest Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	PRODUCT_ID		Return the PRODUCT_ID number : 0x00					

Address : 0x02 Description : Revision number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	REVISON_NUMBER							
Rest Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	REVISON_NUMBER		Return the REVISON_NUMBER number : 0x00					

Address : 0x03 Description : Switch frequency register for BUCK1 controller.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	BUCK1_REG							
Rest Value	0x02							
Read/Write	R	R	R	R	R	RW	RW	R
Bits	Name		Description					
[7:3]	Reserved		Reserved bits					
[2:1]	FREQ		FREQ[2:1] = 00, 300kHz FREQ[2:1] = 01, 450kHz (Default) FREQ[2:1] = 10, 600kHz FREQ[2:1] = 11, 750kHz					
[0]	Reserved		Reserved bit					

Address : 0x04 Description : Output Voltage setting register for BUCK2 controller.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	BUCK2 SEL_REG							
Rest Value	0x32							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6:0]	SEL_VID		SEL_VID[6:0]=0b000 0000 : 0.7V (Min.) SEL_VID[6:0]=0b101 0000 : 1.50V (Max.) (10mV/step) VOUT2 = SEL_VID[6:0] x 0.01V + 0.7V					

Address : 0x05 Description : Output Voltage setting register for BUCK3 controller.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	BUCK3 SEL_REG							
Rest Value	0x1E							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6:0]	SEL_VID		SEL_VID[6:0]=0b000 0000 : 0.7V (Min.) SEL_VID[6:0]=0b101 0000 : 1.50V (Max.) (10mV/step) VOUT3 = SEL_VID[6:0] x 0.01V + 0.7V					

Address : 0x06 Description : DC-DC Auto/FPWM mode control register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DCDCCTRL0_REG							
Rest Value	0x00							
Read/Write	R	R	R	RW	R	R	RW	R

Bits	Name	Description
[7:5]	Reserved	Reserved bits
[4]	Buck4_ PWM	[4]= 0: Auto mode [4]= 1: Forced PWM mode
[2:3]	Reserved	Reserved bit
[1]	Buck1_PWM	[1]= 0: Auto mode [1]= 1: Forced PWM mode
[0]	Reserved	Reserved bit

Address : 0x07 Description : DC-DC enable/disable mode control register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ENABLE_REG							
Rest Value	0x00							
Read/Write	R	R	RW	RW	RW	RW	RW	R

Bits	Name	Description
[7:6]	Reserved	Reserved bits
[5]	LDO_EN	After each channel soft-start, then value is setting to 1. [5]= 0 : Disable [5]= 1 : Enable
[4]	BUCK4_EN	After each channel soft-start, then value is setting to 1. [4]= 0 : Disable [4]= 1 : Enable
[3]	BUCK 3_EN	After each channel soft-start, then value is setting to 1. [3]= 0 : Disable [3]= 1 : Enable
[2]	BUCK 2_EN	After each channel soft-start, then value is setting to 1. [2]= 0 : Disable [2]= 1 : Enable
[1]	BUCK 1_EN	After each channel soft-start, then value is setting to 1. [1]= 0 : Disable [1]= 1 : Enable
[0]	Reserved	Reserved bit

Address : 0x08 Description : Sleep mode control for DC OFF state register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DCDCCTRL1_REG							
Rest Value	0x04							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7]	Reserved	Reserved bit
[6]	LDO_Alive	[6] = 0 : When Sleep, LDO turn off [6] = 1 : When Sleep, LDO alive
[5]	BUCK4_Alive	[5] = 0 : When Sleep, BUCK4 turn off [5] = 1 : When Sleep, BUCK4 alive
[4]	BUCK3_Alive	[4] = 0 : When Sleep, BUCK3 turn off [4] = 1 : When Sleep, BUCK3 alive
[3]	BUCK2_Alive	[3] = 0 : When Sleep, BUCK2 turn off [3] = 1 : When Sleep, BUCK2 alive
[2]	BUCK1_Alive	[2] = 0 : When Sleep, BUCK1 turn off [2] = 1 : When Sleep, BUCK1 alive
[1]	SLEEP_CTRL(software)	[1] = 0: Exit sleep mode if SLEEP_CTRL = 0 [1]= 1: Enter sleep mode if SLEEP_CTRL = 1
[0]	SLEEP_MODE	[0] = 0: Sleep mode by EN_CTRL (low active) (default) [0] = 1: Sleep mode by software SLEEP register (high active)

Address : 0x09 Description : Discharge register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DISCHARGE							
Rest Value	0x1D							
Read/Write	R	R	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:6]	Reserved	Reserved bits
[5]	LDO_DIS	[5] = 0 : Discharge path disabled [5] = 1 : Discharge path enabled
[4]	BUCK4_ DIS	[4] = 0 : Discharge path disabled [4] = 1 : Discharge path enabled
[3]	BUCK3_ DIS	[3] = 0 : Discharge path disabled [3] = 1 : Discharge path enabled
[2]	BUCK2_ DIS	[2] = 0 : Discharge path disabled [1] = 1 : Discharge path enabled
[1:0]	BUCK1_ DIS	[1:0] = 00 : Hi-Z [1:0] = 01 : 100Ω (default) [1:0] = 10 : 200Ω [1:0] = 11 : 500Ω

Address : 0x0A
Description : UV protection behavior register.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PROTECTION MODE							
Rest Value	0x3E							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_PROTECTION		[5] = 0 : Latch-up [5] = 1 : Hiccup(default)					
[4]	BUCK4_ PROTECTION		[4] = 0 : Latch-up [4] = 1 : Hiccup(default)					
[3]	BUCK3_ PROTECTION		[3] = 0 : Latch-up [3] = 1 : Hiccup(default)					
[2]	BUCK2_ PROTECTION		[2] = 0 : Latch-up [2] = 1 : Hiccup(default)					
[1]	BUCK1_ PROTECTION		[1] = 0 : Latch-up [1] = 1 : Hiccup(default)					
[0]	Reserved		Reserved bit					

Address : 0x0B
Description : Mute control register.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MUTE CONTROL							
Rest Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	MUTE CONTROL		[0]= 0 : Enable mute [0] = 1 : Disable mute					

Address : 0x0F
Description : Power good status register.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PGOOD Status							
Rest Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_PG_ Status		[5] = 0: Not Power Good [5] = 1: Power Good					
[4]	Buck4_ PG_ Status		[4] = 0: Not Power Good [4] = 1: Power Good					
[3]	Buck3_ PG _ Status		[3] = 0: Not Power Good [3] = 1: Power Good					
[2]	Buck2_ PG _ Status		[2] = 0: Not Power Good [2] = 1: Power Good					
[1]	Buck1_ PG _ Status		[1] = 0: Not Power Good [1] = 1: Power Good					
[0]	Reserved		Reserved bit					

Address : 0x10 Description : Over voltage event interrupt register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OV_INT							
Rest Value	0x00							
Read/Write	R	R	RW	RW	RW	RW	RW	R

Bits	Name	Description
[7:6]	Reserved	Reserved bits
[5]	LDO_OV_INT	Interrupt for LDO over voltage event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [5] = 0: Not Over Voltage [5] = 1: Over Voltage
[4]	BUCK4_OV_INT	Interrupt for BUCK4 over voltage event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [4] = 0: Not Over Voltage [4] = 1: Over Voltage
[3]	BUCK3_OV_INT	Interrupt for BUCK3 over voltage event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [3] = 0: Not Over Voltage [3] = 1: Over Voltage
[2]	BUCK2_OV_INT	Interrupt for BUCK2 over voltage event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [2] = 0: Not Over Voltage [2] = 1: Over Voltage
[1]	BUCK1_OV_INT	Interrupt for BUCK1 over voltage event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [1] = 0: Not Over Voltage [1] = 1: Over Voltage
[0]	Reserved	Reserved bits

<table>
<tr><td colspan="9">Address : 0x11
Description : Under voltage event interrupt register.</td></tr>
<tr><td>Bits</td><td>Bit7</td><td>Bit6</td><td>Bit5</td><td>Bit4</td><td>Bit3</td><td>Bit2</td><td>Bit1</td><td>Bit0</td></tr>
<tr><td>Name</td><td colspan="8">UV_INT</td></tr>
<tr><td>Rest Value</td><td colspan="8">0x00</td></tr>
<tr><td>Read/Write</td><td>R</td><td>R</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>R</td></tr>
<tr><td>Bits</td><td colspan="2">Name</td><td colspan="6">Description</td></tr>
<tr><td>[7:6]</td><td colspan="2">Reserved</td><td colspan="6">Reserved bits</td></tr>
<tr><td>[5]</td><td colspan="2">LDO_UV_INT</td><td colspan="6">Interrupt for LDO under voltage event
Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing.
[5] = 0 : Not Under Voltage
[5] = 1 : Under Voltage</td></tr>
<tr><td>[4]</td><td colspan="2">BUCK4_ UV _INT</td><td colspan="6">Interrupt for BUCK4 under voltage event
Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing.
[4] = 0 : Not Under Voltage
[4] = 1 : Under Voltage</td></tr>
<tr><td>[3]</td><td colspan="2">BUCK3_ UV _INT</td><td colspan="6">Interrupt for BUCK3 under voltage event
Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing.
[3] = 0 : Not Under Voltage
[3] = 1 : Under Voltage</td></tr>
<tr><td>[2]</td><td colspan="2">BUCK2_ UV _INT</td><td colspan="6">Interrupt for BUCK2 under voltage event
Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing.
[2] = 0 : Not Under Voltage
[2] = 1 : Under Voltage</td></tr>
<tr><td>[1]</td><td colspan="2">BUCK1_ UV _INT</td><td colspan="6">Interrupt for BUCK1 under voltage event
Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing.
[1] = 0 : Not Under Voltage
[1] = 1 : Under Voltage</td></tr>
<tr><td>[0]</td><td colspan="2">Reserved</td><td colspan="6">Reserved bits</td></tr>
</table>

Address : 0x12 Description : Power good event interrupt register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PGOOD_INT							
Rest Value	0x00							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_PGOOD_INT		Interrupt for LDO power good event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [5] = 0 : Power Good [5] = 1 : Not Power Good					
[4]	BUCK4_PGOOD_INT		Interrupt for BUCK4 power good event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [4] = 0 : Power Good [4] = 1 : Not Power Good					
[3]	BUCK3_PGOOD_INT		Interrupt for BUCK3 power good event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [3] = 0 : Power Good [3] = 1 : Not Power Good					
[2]	BUCK2_PGOOD_INT		Interrupt for BUCK2 power good event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [2] = 0 : Power Good [2] = 1 : Not Power Good					
[1]	BUCK1_PGOOD_INT		Interrupt for BUCK1 power good event Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [1] = 0 : Power Good [1] = 1 : Not Power Good					
[0]	Reserved		Reserved bit					

Address : 0x13 Description : Thermal shutdown event interrupt register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	HOT_DIE_INT							
Rest Value	0x0E							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	THERM_OT_INT		Interrupt for thermal shutdown event (CH2 CH3 CH4 OT Function) Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [5] = 0 : The thermal shutdown threshold is not reached [5] = 1 : The thermal shutdown threshold is reached					
[4]	HOT_DIE_INT		Write a 1b to clear the corresponding interrupt bit. This bit is self-clearing. [4] = 0 : Hot die threshold is not reached [4] = 1 : Hot die threshold is reached					
[3:2]	THERM_HDSEL		[3:2] = 00 : 90°C [3:2] = 01 : 100°C [3:2] = 10 : 110°C [3:2] = 11 : 120°C (default)					
[1]	HOT_DIE _EN		[1] = 0 : Thermal shutdown module is disable [1] = 1 : Thermal shutdown module is enable					
[0]	Reserved		Reserved bit					

Address: 0x14 Description: Mask over voltage event register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OV_MASK							
Rest Value	0x00							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_OV_MASK		[5] = 0: Interrupt generation enabled. [5] = 1: Interrupt generation disabled.					
[4]	BUCK4_OV_MASK		[4] = 0: Interrupt generation enabled. [4] = 1: Interrupt generation disabled.					
[3]	BUCK3_OV_MASK		[3] = 0: Interrupt generation enabled. [3] = 1: Interrupt generation disabled.					
[2]	BUCK2_OV_MASK		[2] = 0: Interrupt generation enabled. [2] = 1: Interrupt generation disabled.					
[1]	BUCK1_OV_MASK		[1] = 0: Interrupt generation enabled. [1] = 1: Interrupt generation disabled.					
[0]	Reserved		Reserved bit					

Address : 0x15 Description : Mask under voltage event register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	UV_MASK							
Rest Value	0x00							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_UV_MASK		[5] = 0 : Interrupt generation enabled. [5] = 1 : Interrupt generation disabled.					
[4]	BUCK4_ UV _MASK		[4] = 0 : Interrupt generation enabled. [4] = 1 : Interrupt generation disabled.					
[3]	BUCK3_ UV _MASK		[3] = 0 : Interrupt generation enabled. [3] = 1 : Interrupt generation disabled.					
[2]	BUCK2_ UV _MASK		[2] = 0 : Interrupt generation enabled. [2] = 1 : Interrupt generation disabled.					
[1]	BUCK1_ UV _MASK		[1] = 0 : Interrupt generation enabled. [1] = 1 : Interrupt generation disabled.					
[0]	Reserved		Reserved bit					

Address : 0x16 Description : Mask power good event register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PGOOD_MASK							
Rest Value	0x3E							
Read/Write	R	R	RW	RW	RW	RW	RW	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5]	LDO_PGOOD_MASK		[5] = 0 : Interrupt generation enabled. [5] = 1 : Interrupt generation disabled.					
[4]	BUCK4_PGOOD_MASK		[4] = 0 : Interrupt generation enabled. [4] = 1 : Interrupt generation disabled.					
[3]	BUCK3_PGOOD_MASK		[3] = 0 : Interrupt generation enabled. [3] = 1 : Interrupt generation disabled.					
[2]	BUCK2_PGOOD_MASK		[2] = 0 : Interrupt generation enabled. [2] = 1 : Interrupt generation disabled.					
[1]	BUCK1_PGOOD_MASK		[1] = 0 : Interrupt generation enabled. [1] = 1 : Interrupt generation disabled.					
[0]	Reserved		Reserved bit					

Address : 0x17 Description : Mask thermal shutdown and hot die event register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	HOT_DIE_MASK							
Rest Value	0x00							
Read/Write	R	R	R	R	R	RW	RW	R

Bits	Name	Description
[7:3]	Reserved	Reserved bits
[2]	THERM_OT_MASK	[2] = 0 : Interrupt generation enabled. [2] = 1 : Interrupt generation disabled.
[1]	HOT_DIE_MASK	[1]= 0 : Interrupt generation enabled. [1] = 1 : Interrupt generation disabled.
[0]	Reserved	Reserved bit

Address : 0x2A Description : Control rails alive and turn off when VIN1_OK go low register. If rail setting to turn off, the rail can re-power on when VIN1_OK and EN_CTRL be pulled high.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VIN1_OK_CTRL_Rail							
Rest Value	0x01							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	Name	Description
[7:5]	Reserved	Reserved bits
[4]	LDO_Alive	[4] = 0 : When VIN1_OK go low, LDO turn off [4] = 1 : When VIN1_OK go low, LDO alive
[3]	Buck4_ Alive	[3] = 0 : When VIN1_OK go low, Buck4 turn off [3] = 1 : When VIN1_OK go low, Buck4 alive
[2]	Buck3_ Alive	[2] = 0 : When VIN1_OK go low, Buck3 turn off [2] = 1 : When VIN1_OK go low, Buck3 alive
[1]	Buck2_ Alive	[1] = 0 : When VIN1_OK go low, Buck2 turn off [1] = 1 : When VIN1_OK go low, Buck2 alive
[0]	Buck1_ Alive	[0] = 0 : When VIN1_OK go low, Buck1 turn off [0] = 1 : When VIN1_OK go low, Buck1 alive

Application Information

Power Sequence

The RT5090C will automatically start power-up-sequence after a valid power is supplied to VIN1 pin and BUCK1 input and then EN_CTRL pin is pulled high for single input power system. 3.3V standby power is supplied to VCC pin and 12V power is supplied to VIN1 pin and BUCK1 input and then EN_CTRL pin is pulled high for system is 12V + 3.3V standby power.

Sleep Mode Control

The sleep mode control by EN_CTRL pin. Enter sleep mode (DC OFF) when EN_CTRL pin is pulled low, exit sleep mode (DC ON) when EN_CTRL pin is pulled high. I^2C register 0x08h for setting each rails alive or turn off state for sleep mode (DC OFF).

SOC_REST Output

All rails are in power good state, then SOC_REST pin is pulled high.

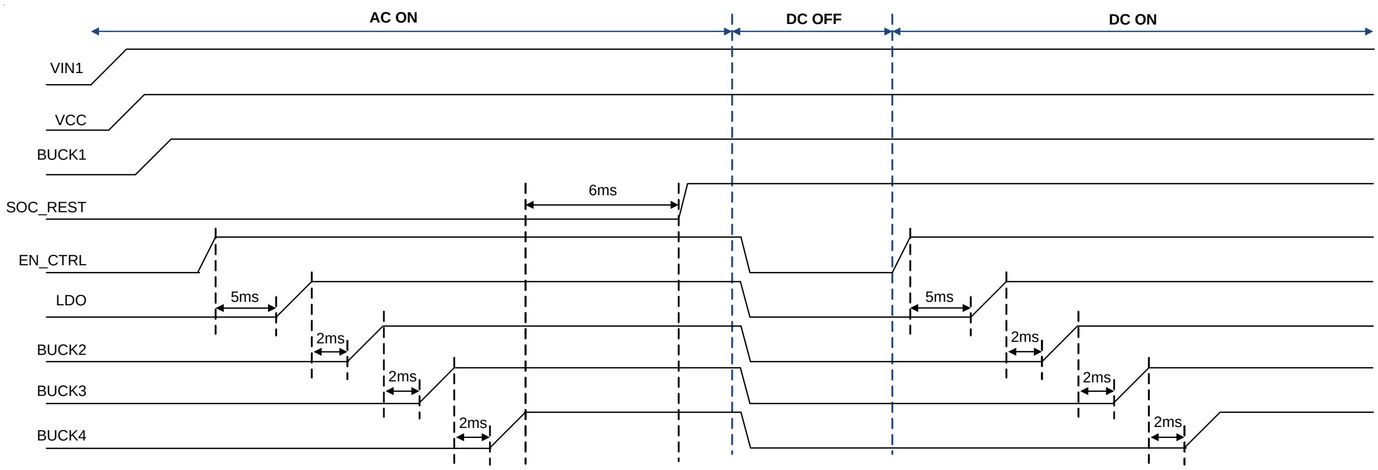


Figure 3. Power ON Sequence

BUCK1

Current Limit Setting (ENTRIP)

The BUCK1 has a cycle-by-cycle current limit control. The current limit circuit employs an unique "Valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE1 is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are functions of the sense resistance, inductor value, input power and output voltage.

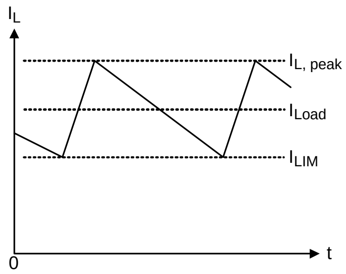


Figure 4. "Valley" Current Limit

The BUCK1 uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIM} resistor between the ENTRIP pin and GND sets the current limit threshold. The resistor R_{ILIM} is connected to a current source from ENTRIP pin, which is typically 50μA at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low side MOSFET equals 1/12 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/12 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor by following equation :

$$V_{ILIM} = (R_{ILIM} \times 50\mu A)/12 = I_{ILIM} \times R_{DS(ON)}$$

$$R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 12 / 50\mu A$$

Carefully observe the PC board layout guidelines to ensures that noise and DC errors do not corrupt the current sense signal at PHASE1 and GND. Mount or place the low side MOSFET close to the IC.

The current limit behavior as Figure 5.

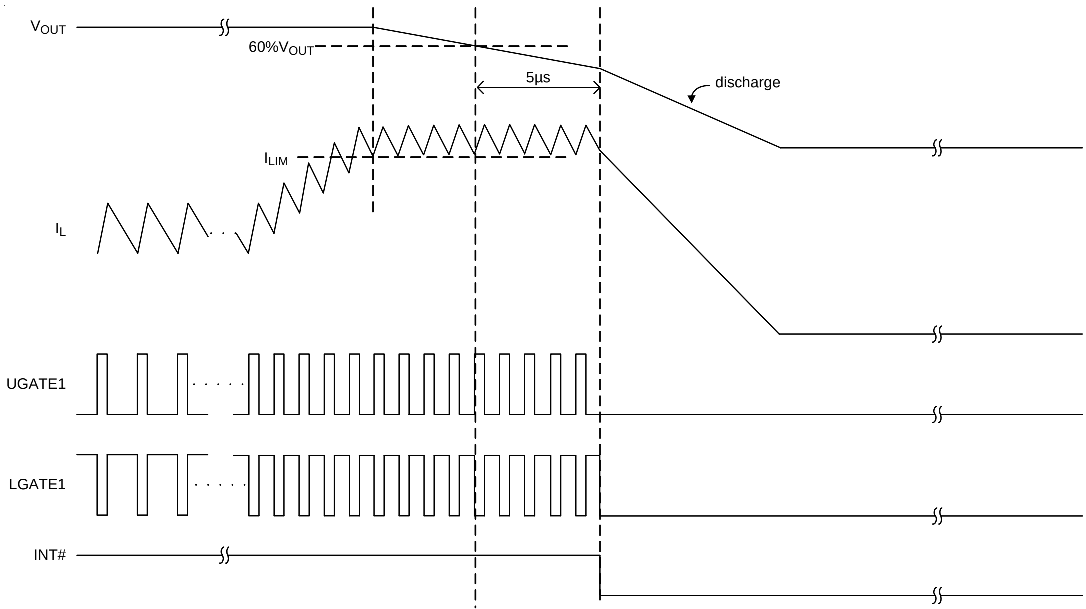


Figure 5. Current Limit Behavior

Over-Voltage Protection (OVP)

The OVP circuit is monitors the output voltage via FB1 pin. When the FB1 voltage exceeds the OVP threshold 120%, OVP is triggered and turns off the high-side MOSFET and turns on the low-side MOSFET. The condition is latched, cycle POR to recover.

The OVP behavior as Figure 6.

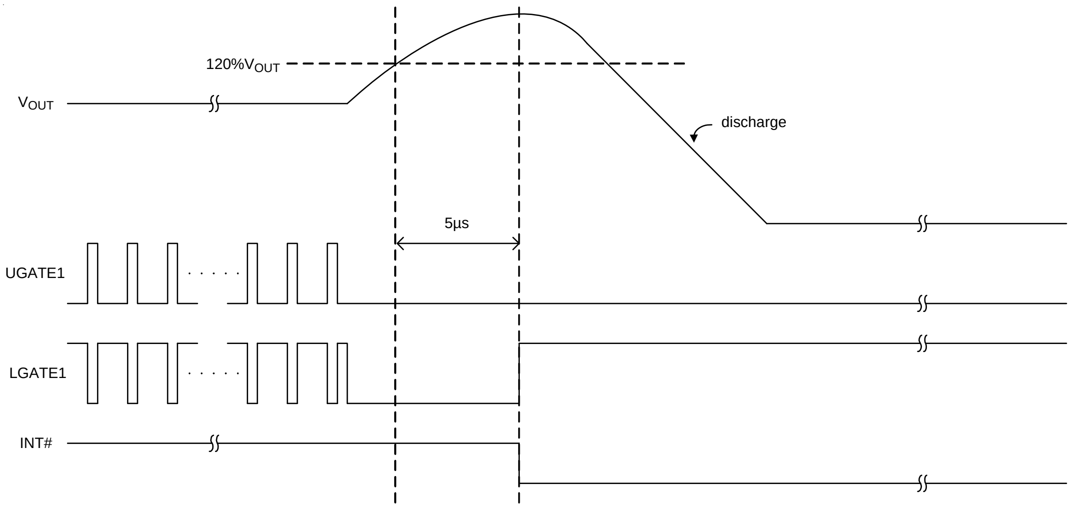


Figure 6. OVP Behavior

Under-Voltage Protection (UVP)

The UVP circuit is monitors the output voltage via FB1 pin. When the FB1 voltage drops below the UVP threshold 60%, UVP is triggered and turns off both the high-side and low-side MOSFET. The condition is hiccup, selection protection behavior by I^2C setting.

The UVP behavior as Figure 7.

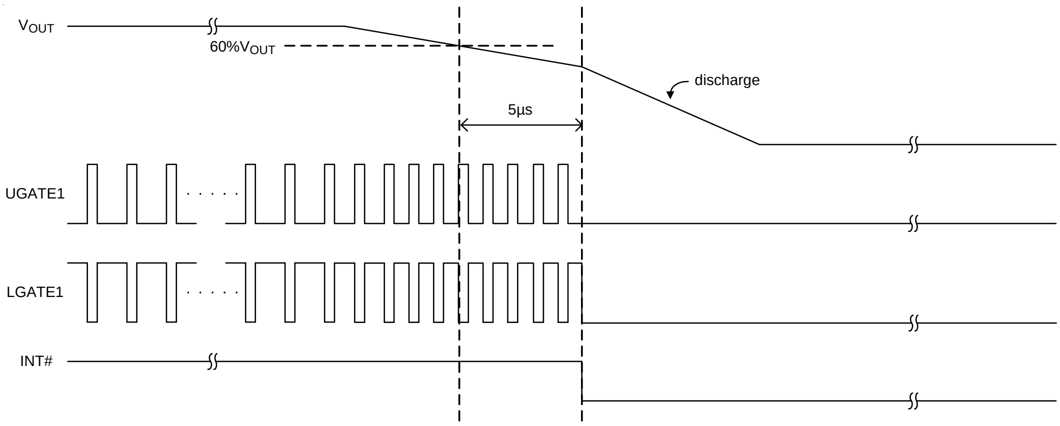


Figure 7. UVP Behavior

Output Voltage Setting (FB1)

Connect a resistor voltage divider at the FB1 pin between V_{OUT1} and GND to adjust the respective output voltage. For example, choose R2 to be approximately 10kΩ, and solve for R1 using the equation:

$$V_{OUT1} = V_{FB1} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FB1} is 1.2V.

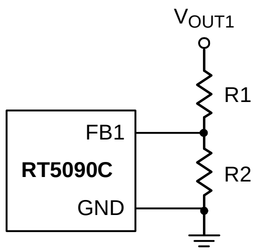


Figure 8. Output Voltage Setting

BUCK2

Over-Voltage Protection (OVP)

The OVP circuit is monitors the output voltage via VSEN2 pin. When the VSEN2 voltage exceeds the OVP threshold 120%, OVP is triggered and turns off both the high-side and low-side MOSFET. The condition is latched and other BUCKx & LDO is disabled, cycle POR to recover.

The OVP behavior as Figure 9.

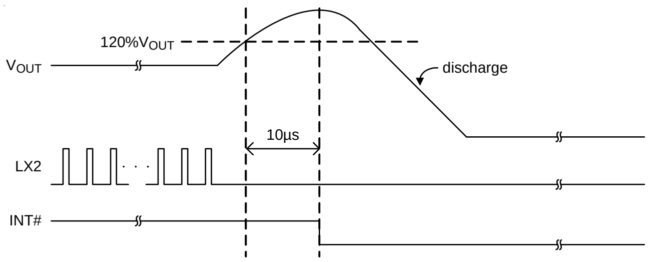


Figure 9. OVP Behavior

Under-Voltage Protection (UVP)

The UVP circuit is monitors the output voltage via VSEN2 pin. When the VSEN2 voltage drops below the UVP threshold 60%, UVP is triggered and turns off both the high-side and low-side MOSFET. The condition is hiccup, selection protection behavior by I^2C setting.

The UVP behavior as Figure 10.

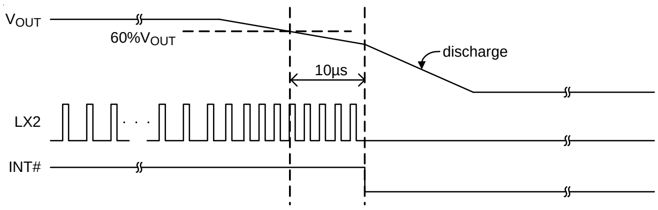


Figure 10. UVP Behavior

Current Limit

The current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level, the IC will stop switching to avoid excessive heat.

The current limit behavior as Figure 11.

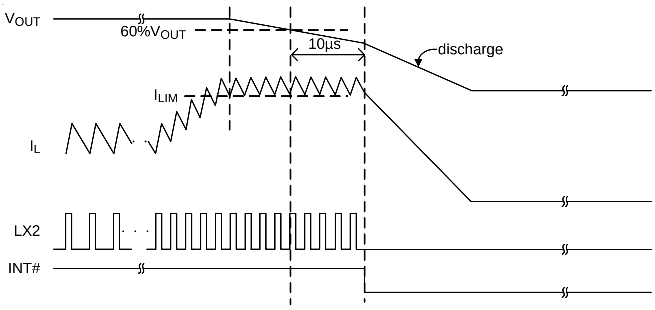


Figure 11. Current Limit Behavior

BUCK3

The BUCK3 with an external low-side MOSFET can support to 6A application. The external MOSFET Ciss need to 500pF above.

Over-Voltage Protection (OVP)

The OVP circuit is monitors the output voltage via VSEN3 pin. When the VSEN3 voltage exceeds the OVP threshold 120%, OVP is triggered and turns off both the high-side and low-side MOSFET. The condition is latched and other BUCKx & LDO is disabled, cycle POR to recover.

The OVP behavior as Figure 12.

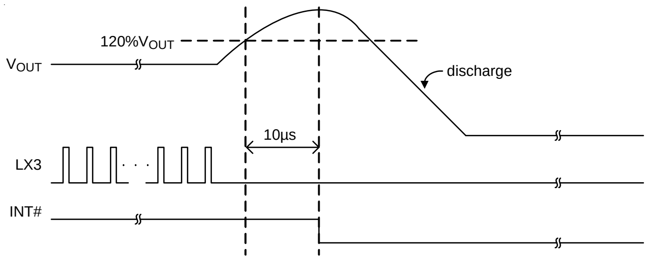


Figure 12. OVP Behavior

Under-Voltage Protection (UVP)

The UVP circuit is monitors the output voltage via VSEN3 pin. When the VSEN3 voltage drops below the UVP threshold 60%, UVP is triggered and turns off both the high-side and low-side MOSFET. The condition is hiccup, selection protection behavior by I^2C setting.

The UVP behavior as Figure 13.

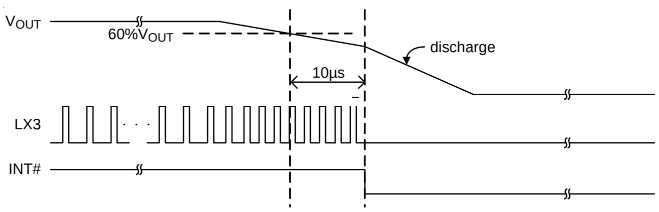


Figure 13. UVP Behavior

Current Limit

The current limit is a cycle-by-cycle “peak” type, measuring the inductor current through the synchronous rectifier during the on-time while the inductor current ramps down. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level, the IC will stop switching to avoid excessive heat.

The current limit behavior as Figure 14.

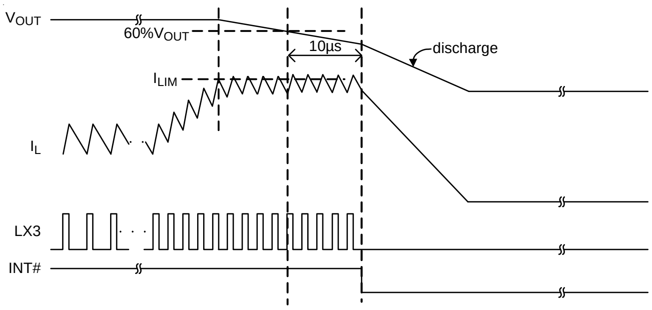


Figure 14. Current Limit Behavior

BUCK4

Over-Voltage Protection (OVP)

The OVP circuit is monitors the output voltage via FB4 pin. When the FB4 voltage exceeds the OVP threshold 120%, OVP is triggered and turns off both the high-side and low-side MOSFET. The condition is latched and other BUCKx & LDO is disabled, cycle POR to recover.

The OVP behavior as Figure 15.

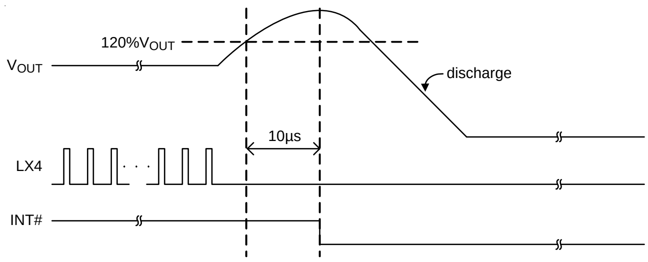


Figure 15. OVP Behavior

Under-Voltage Protection (UVP)

The UVP circuit is monitors the output voltage via FB4 pin. When the FB4 voltage drops below the UVP threshold 60%, UVP is triggered and turns off both the high-side and low-side MOSFET. The condition is hiccup, selection protection behavior by I^2C setting.

The UVP behavior as Figure 16.

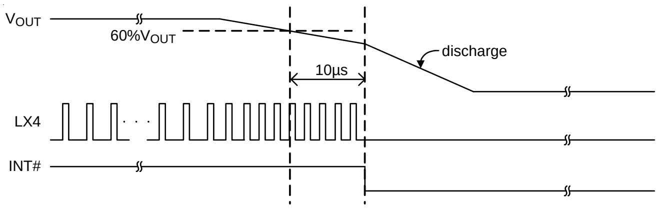


Figure 16. UVP Behavior

Current Limit

The current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the on-time while the inductor current ramps down. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level, the IC will stop switching to avoid excessive heat.

The current limit behavior as Figure 17.

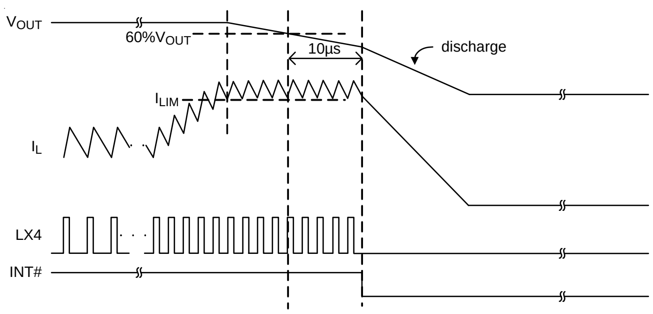


Figure 17. Current Limit Behavior

Output Voltage Setting (FB4)

Connect a resistor voltage divider at the FB4 pin between V_{OUT4} and GND to adjust the respective output voltage. For example, choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUT4} = V_{FB4} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FB4} is 0.6V.

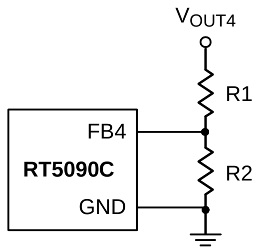


Figure 18. Output Voltage Setting

LDO

Over-Voltage Protection (OVP)

The OVP circuit is monitors the output voltage via FB_LDO pin. When the FB_LDO voltage exceeds the OVP threshold 120%. The condition is latched and other BUCKx is disabled, cycle POR to recover.

The OVP behavior as Figure 19.

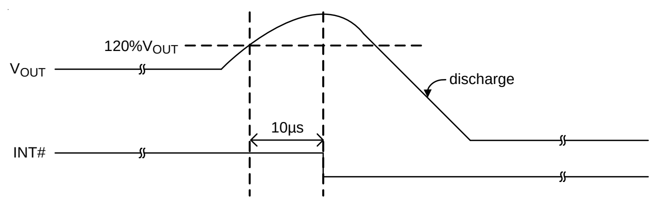


Figure 19. OVP Behavior

Under-Voltage Protection (UVP)

The UVP circuit is monitors the output voltage via FB_LDO pin. When the FB_LDO voltage drops below the UVP threshold 60%. The condition is hiccup, selection protection behavior by I^2C setting.

The UVP behavior as Figure 20.

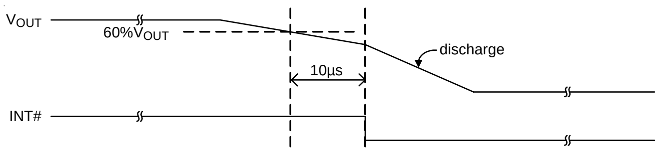


Figure 20. UVP Behavior

Output Voltage Setting (FB_LDO)

Connect a resistor voltage divider at the FB_LDO pin between V_{VLDO} and GND to adjust the respective output voltage. For example, choose R2 to be approximately 10kΩ, and solve for R1 using the equation:

$$V_{VLDO} = V_{FB\_LDO} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FB_LDO} is 0.8V.

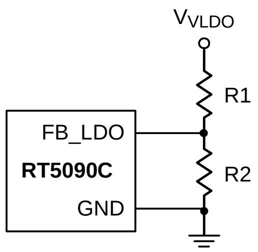


Figure 21. Output Voltage Setting

Mute Function

The mute circuit of the RT5090C for anti-pop sound during AC OFF and mute. The MUTE_OUT# pin is pulled low when the VDET voltage drops below 1V. Connect a resistor voltage divider at the VDET pin between VIN1 and GND to setting power detect point. Connect an enough capacitor at the VCAP pin to provide power for mute control logic circuit.

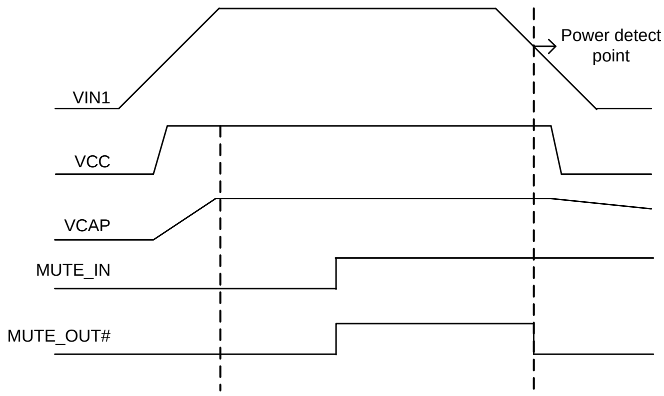


Figure 22. Mute Sequence when AC OFF in 24V Single Input Power System

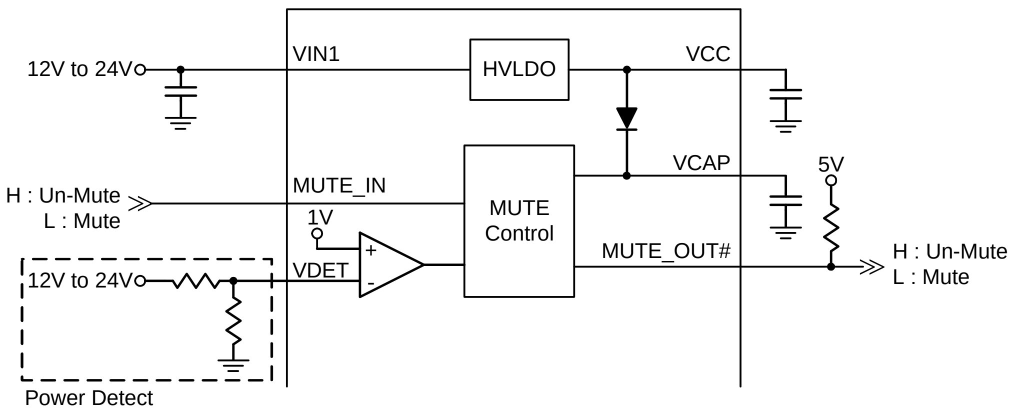


Figure 23. Mute Function Block Diagram

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (27.5°C/W) = 3.63W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 24 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

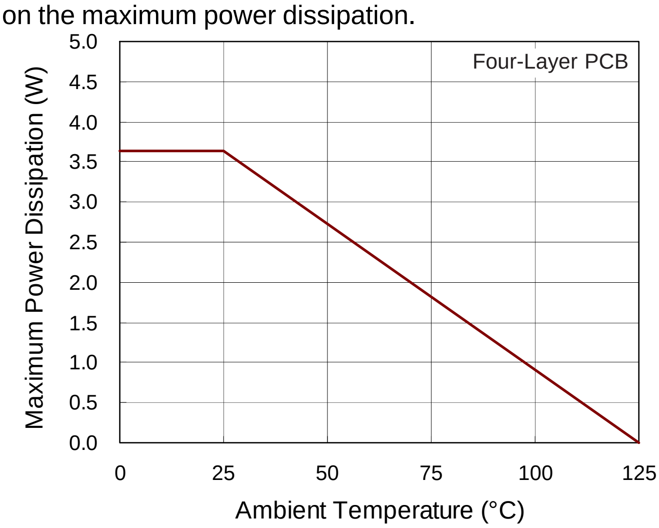


Figure 24. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important of good power supply design. The PCB traces can radiate excessive noise and contribute to converter instability with improper layout. The following layout recommendations will help guide you through a good layout.

- The VINx and VIN_LDO pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The optimum placement is closest to the VINx and VIN_LDO pins of the device.
- The FBx, VSENx and RGND2 pins traces should be routed away from any potential noise source to avoid coupling.
- The LXx trace should be kept on the PCB top layer and free of any vias.
- The PGND should be tied to the PCB ground plane with multiple vias.
- The VCC pin to AGND with a low ESR ceramic bypass capacitor, bypass capacitor should be as close as possible to the VCC pin.
- The AGND pin should not be connected to the PGND on the PCB top layer.
- Route the VSEN2 and RGND2 line from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair.
- Snubber component placement should be on the same layer as the devices, and be kept as close as possible to the phase and GND.

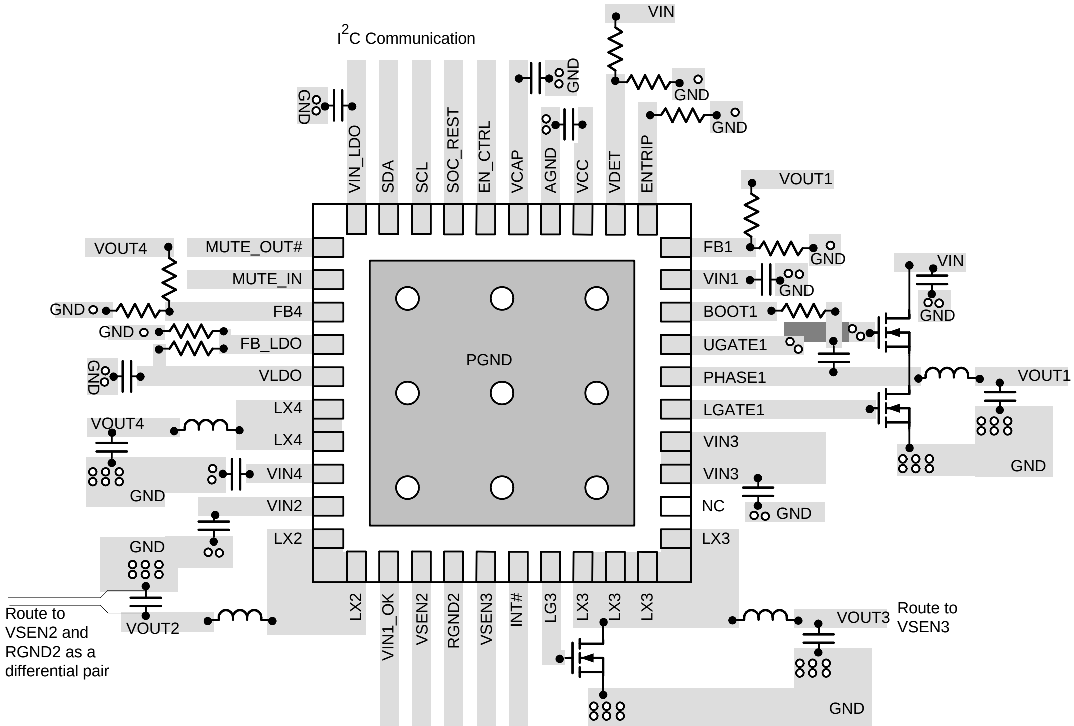
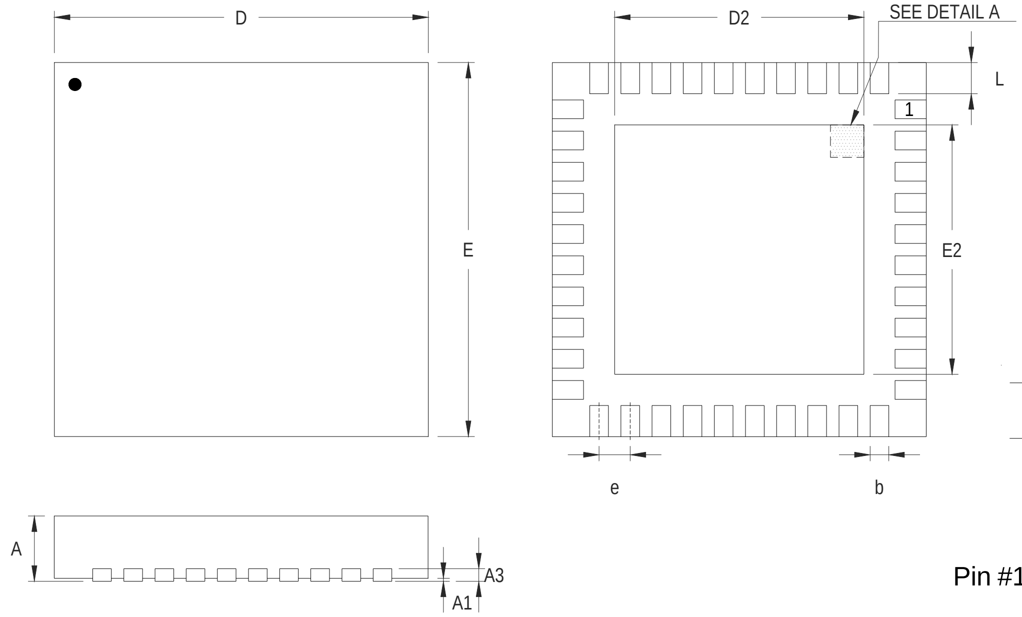
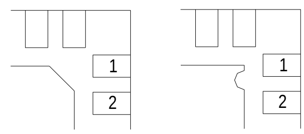


Figure 25. PCB Layout Guide

Outline Dimension





DETAIL A

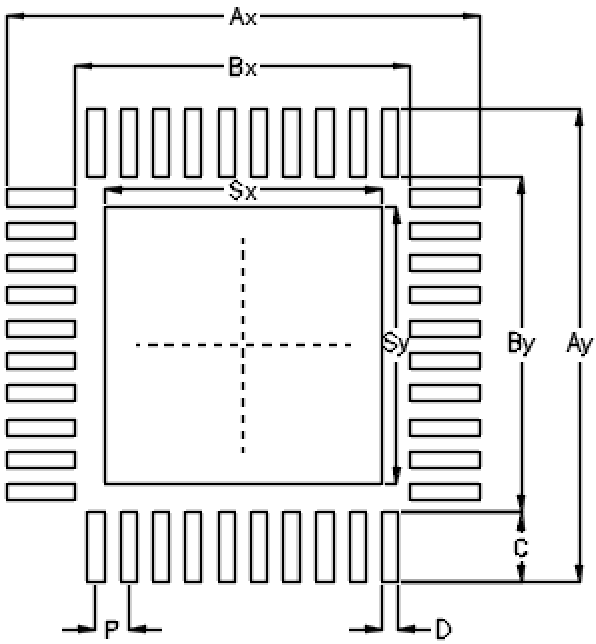
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789