SSD Power Management Total Solution

General Description

The RT5168 is an integrated solution for SSD power management IC. This device provides 5 single Buck voltage regulators (Rail1 to Rail5) and 1 LDO. Among the 5 voltage regulators, the Rail1, Rail2, Rail3 and Rail4 can operate either in single phase mode or dual phase mode. A complete protection mechanism is also embedded for safe power distribution and the corresponding fault events can be recorded by the registers. The RT5168 is available in a UQFN-40L.5x5-FC package. The recommended junction temperature is 0°C to 125°C, and the ambient temperature is 0°C to 85°C.

Ordering Information

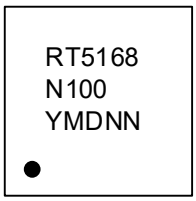
RT5168 □-□□□□

- Packing
  A: Standard
- MTP Version
- Version
- Package Type
  N: UQFN-40L 5x5 (FC) (U-Type)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Marking Information



RT5168N100: Product Code
YMDNN: Date Code

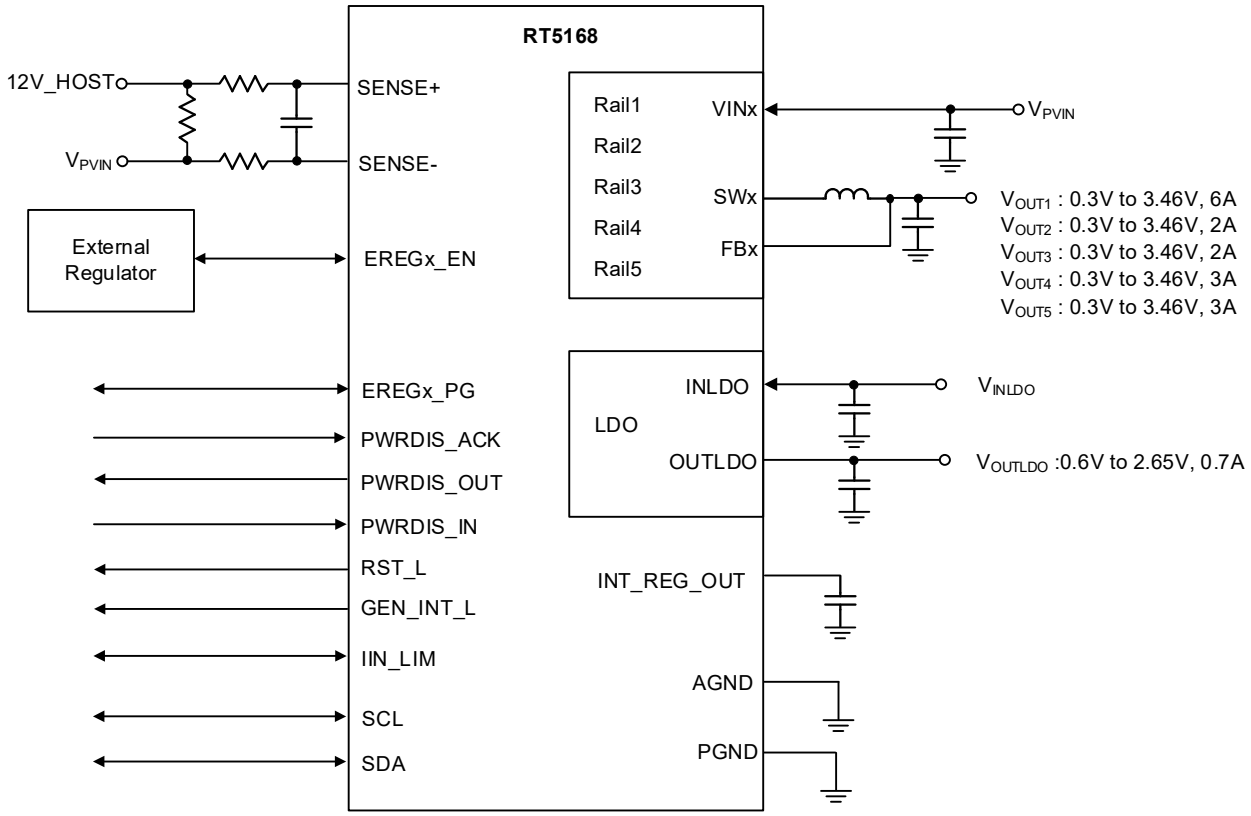
Features

- **Wide Input Supply Range: 4V to 16V**
- **High efficiency for each Buck Converter**
- **Configurable Outputs**
  - **±1% Feedback Voltage Accuracy**
  - **DVID Change for all Bucks via I^2C Interface**
  - **Adjustable Enable Time and Soft-start Time for all VRs.**
  - **Selectable Switching Frequency for Each Buck Rail**
- **Smart Protection Unit Provides Best Protection Shutdown Sequence Control**
- **Dual-Phase DEM Operation Implements Good Light Load Efficiency and Good Transient Response**
- **11 Bits ADC Reporting for V_{IN} and I_{IN}**
- **Non-Volatile Register Configurability**
- **I^2C Interface 400kHz/1MHz**
- **Control and Command Unit**
  - **Power Indication (RST_L) and Interrupt Indication (GEN_INT_L)**
  - **Power Disable Mode**
  - **External Regulator Enable and Power Good Monitoring**
  - **IIN_LIM for OverCurrent Indicator**

Applications

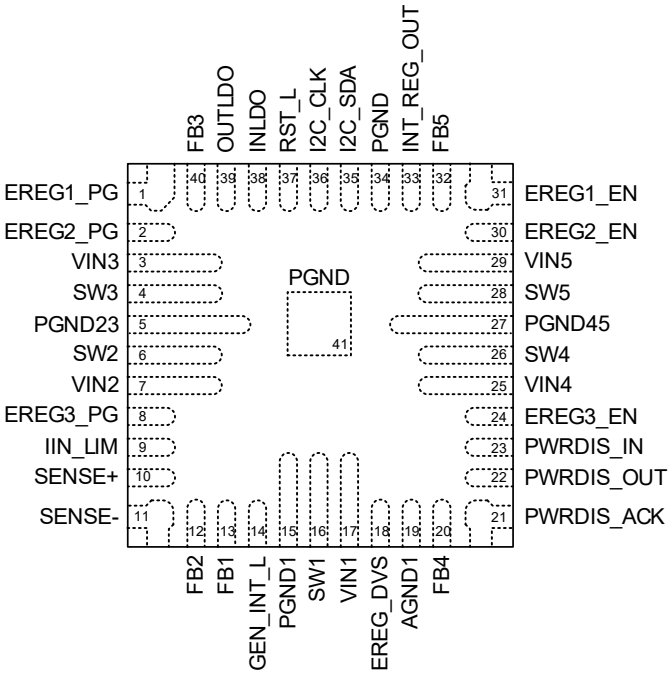
- SSD

Simplified Application Circuit



Pin Configuration

(TOP VIEW)



UQFN-40L 5x5 (FC)

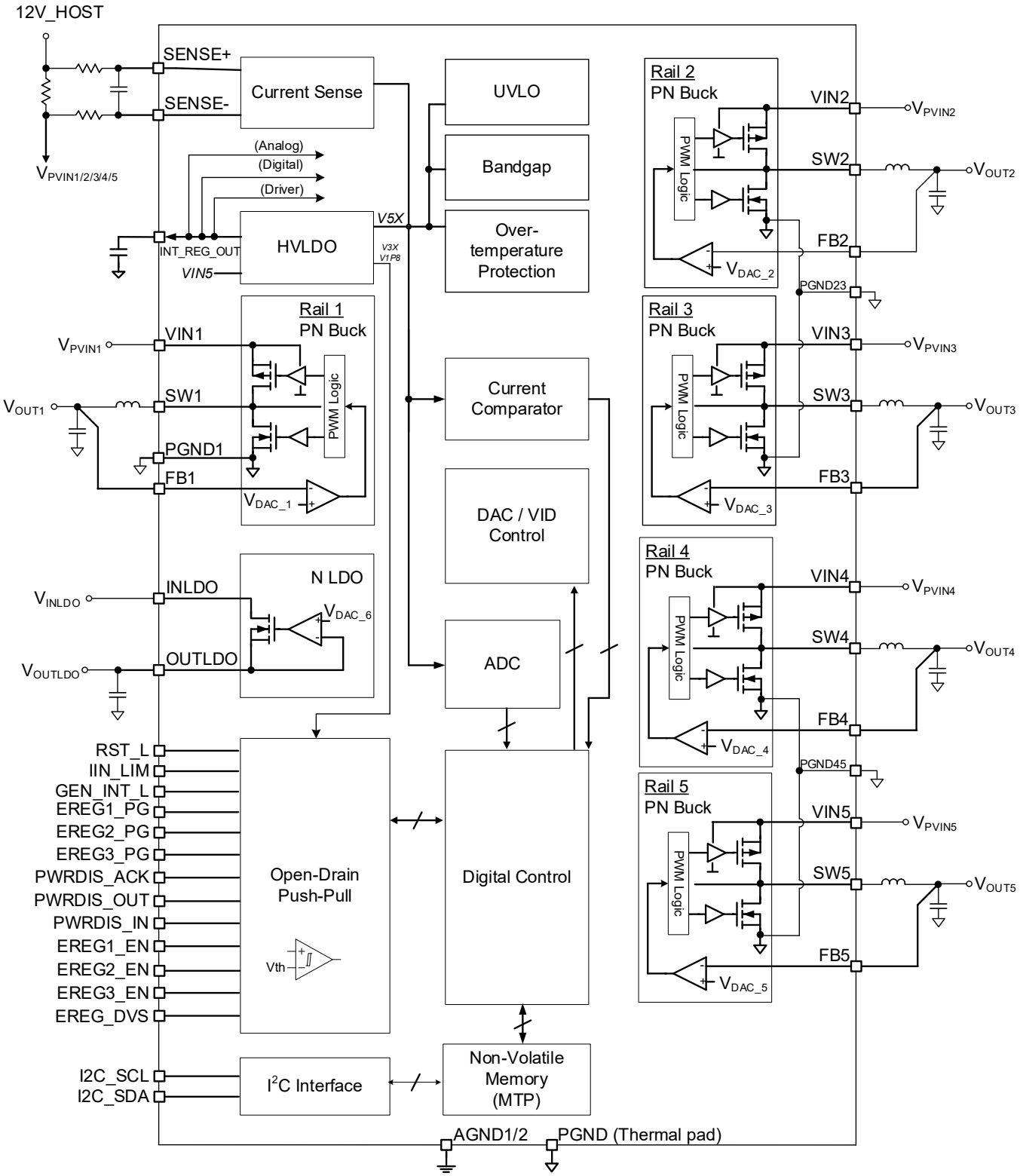
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EREG1_PG	External Regulator 1 power good input. This pin can also be configured as an open-drain output pin by the setting of REG_0x6A[2], and the output high or low are determined by REG_0x18[3]. In open-drain output, the pull-up and pull-down resistors can be determined by REG_0x75[4] to be provided externally or internally. If 0x75[4] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x6A[7:3].
2	EREG2_PG	External Regulator 2 power good input. This pin can also be configured as an open-drain output pin by the setting of REG_0x6B[2], and the output high or low are determined by REG_0x18[2]. In open-drain output, the pull-up and pull-down resistors can be determined by REG_0x75[3] to be provided externally or internally. If 0x75[3] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x6B[7:3].
3	VIN3	Rail3 input supply. It is internally connected to the source terminal of the Rail3 high-side MOSFET. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805) as close as possible from VIN3 pin to PGND23 pin is necessary.
4	SW3	Switch node of the Rail3. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
5	PGND23	Ground return from low-side power MOSFET and driver of Rail2 and Rail3. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND pin are required to minimize the parasitic impedance and thermal resistance.
6	SW2	Switch node of the Rail2. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
7	VIN2	Rail2 input supply. It is internally connected to the source terminal of the Rail2 high-side MOSFET. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805) as close as possible from VIN2 pin to PGND23 pin is necessary.
8	EREG3_PG	External Regulator 3 power good input. This pin can also be configured as an open-drain output pin by the setting of REG_0x6C[2], and the output high or low are determined by REG_0x18[1]. In open-drain output, the pull-up and pull-down resistors can be determined by REG_0x75[2] to be provided externally or internally. If 0x75[2] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x6C[7:3].
9	IIN_LIM	Fault indicator for input overcurrent. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x6E[0] to be provided externally or internally. If 0x6E[0] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x6E[7:3].
10	SENSE+	Input current sense positive node. It is recommended to add an RC filter externally, as shown in Figure 5. The recommended value for R_{filter} is 4.7Ω, and the recommended value for C_{Filter} is 1μF.
11	SENSE-	Input current sense negative node.

Pin No.	Pin Name	Pin Function
12	FB2	Rail2 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power good of Rail2.
13	FB1	Rail1 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power good of Rail1.
14	GEN_INT_L	General interrupt. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x66[0] to be provided externally or internally. If 0x66[0] =0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x66 [7:3].
15	PGND1	Ground return from low-side power MOSFET and driver of Rail1. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND pin are required to minimize the parasitic impedance and thermal resistance.
16	SW1	Switch node of the Rail1. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
17	VIN1	Rail1 input supply. It is internally connected to the source terminal of the Rail1 high-side MOSFET. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805) as close as possible from VIN1 pin to PGND1 pin is necessary.
18	EREG_DVS	EREG_DVS is an open-drain output for external regulator's input requirement. This pin is capable of outputting high, low, and Hi-Z three states. Its Pull-up resistor, Pull-down resistor, output high-level voltage, and output Hi-Z state are determined by REG_0x6D [7:2].
19	AGND1	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
20	FB4	Rail4 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power good of Rail4.
21	PWRDIS_ACK	Power disable ack input. Regarding the functionality and description of this pin, please refer to the section "Power Disable Mode".
22	PWRDIS_OUT	Power disable output. Regarding the functionality and description of this pin, please refer to the section "Power Disable Mode".
23	PWRDIS_IN	Power disable PMIC input. Regarding the functionality and description of this pin, please refer to the section "Power Disable Mode".
24	EREG3_EN	External Rail 2 enable drive. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x75[5] to be provided externally or internally. If 0x75[5] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x69[7:3].
25	VIN4	Rail4 input supply. It is internally connected to the source terminal of the Rail4 high-side MOSFET. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805) as close as possible from VIN4 pin to PGND45 pin is necessary.
26	SW4	Switch node of the Rail4. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
27	PGND45	Ground return from low-side power MOSFET and driver of Rail4 and Rail5. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND45 pin are required to minimize the parasitic impedance and thermal resistance.

Pin No.	Pin Name	Pin Function
28	SW5	Switch node of the Rail5. It is internally connected to the drain terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. Connect this pin to output inductor and keep the sensitive trace and signals away.
29	VIN5	Rail 5 input supply. It is internally connected to the source terminal of the Rail5 high-side MOSFET. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805) as close as possible from VIN pin to PGND45 pin is necessary.
30	EREG2_EN	External Rail 2 enable drive. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x75[6] to be provided externally or internally. If 0x75[6] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x68[7:3].
31	EREG1_EN	External Rail 1 enable drive. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x75[7] to be provided externally or internally. If 0x75[7] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x67[7:3].
32	FB5	Rail5 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power good of Rail5.
33	INT_REG_OUT	Internal LDO output. Used as supply to internal control circuits. **DO NOT** connect to any external loads. Connect a high-quality capacitor (C = 10μF/0603) to ensure system stability.
34	PGND	Power dissipation pad. This pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
35	I2C_SDA	I^2C data pin. This pin is the input and output of serial bus data signal.
36	I2C_CLK	I^2C clock pin. This pin is the input of serial bus clock signal.
37	RST_L	Reset signal from PMIC. It is an open-drain output. The pull-up and pull-down resistors can be determined by REG_0x65 [0] to be provided externally or internally. If 0x65[0] = 0b (resistors provided from internally), the output voltage, pull-up resistor, and pull-down resistor parameters are determined by REG_0x65 [7:3].
38	INLDO	LDO input supply. Connecting the ceramic capacitor (C = 1μF/0402) as close as possible from INLDO pin to PGND pin is necessary.
39	OUTLDO	LDO output. To ensure stability of the LDO, it is recommended to Connecting the ceramic capacitor (C = 22μF/0402)
40	FB3	Rail3 feedback sense for output regulation. It is also used to detect output voltage status for OVP, UVP and Power good of Rail3.
41	PGND	Power dissipation pad. This pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT5168 provides five high-efficiency synchronous buck regulators and one LDO for the power system of SSD.

Buck Converter

The RT5168 incorporates five high-efficiency COT-based mode synchronous buck converters integrated with high-side P-MOSFET and low-side N-MOSFET. It features low output voltage, quick transient response, and low quiescent current. These buck converters also possess all standard protections.

Buck Undervoltage Protection (UVP), Overvoltage Protection (OVP)

The buck rail output voltages are continuous monitored for undervoltage and overvoltage protections.

If the output voltage falls below 80% or 85%(Typ.) of the reference voltage, UVP will be triggered, and both high-side and low-side MOSFETs will be turned off and shut off the rail immediately. The UVP trigger level is defined by REG_0x62.

While output voltage exceeds 115% or 120% (Typ.) of the reference voltage, it triggers OVP, both high-side and low-side MOSFETs turn off and shut off the rail immediately. The OVP trigger level is defined by REG_0x61.

Buck Overcurrent Limiter (OCL)

The current-limited architecture of all buck rails uses valley current detection. When low-side turns on, inductor current is sensed from $R_{DS(ON)}$ of low-side by the internal ZC/OC circuit. If the voltage on low-side $R_{DS(ON)}$ is over V_{OC} (overcurrent voltage), OC circuit forces low-side at turn on status to reduce inductor current and the low-side will not turn off until the inductor current goes low to OC level. Once the inductor current is under OC level, the rail goes back to normal operation. If the controller continues to detect current limited sixteen times every internal clock, it shuts off the rail immediately. Please see the equations below to calculate the current limiting level defined as I_{OUT_OC}. Figure 1 illustrates cycle-by-cycle “valley” current-limiting control.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{OUT\_OC} = I_{L\_Valley} + \frac{\Delta I_L}{2} = I_{L\_Valley} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

Where,

ΔI_L = peak to peak inductor current.

I_{OUT_OC} = average load current when current limitation occurs. I_{L_Valley} = the valley of inductor current when current limitation occurs as defined by REG_0x5C,0x5D.

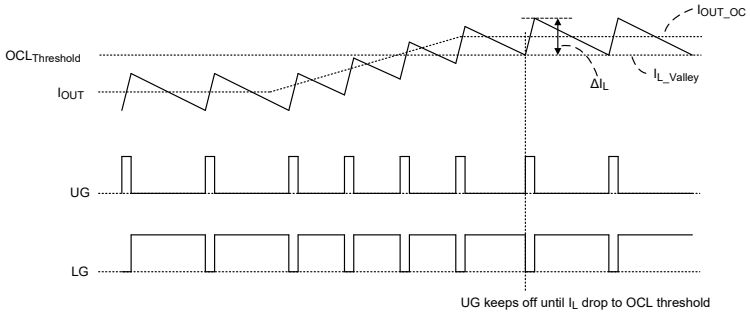


Figure 1. Cycle-by-Cycle “Valley” Current Limiting Control

Linear Dropout Regulator (LDO)

The RT5168 includes one N-MOSFET type linear dropout regulator. The LDO contains independent current limit, overvoltage protection and undervoltage protection circuits to prevent unexpected situations.

When the load current is above the internal current-limit threshold, the current limit circuit adjusts the gate voltage of power stage to limit the output current; if the output load keeps draining current from LDO and the output voltage is lower than 80% or 85% (Typ.) of reference voltage, the UVP is triggered and shuts off LDO immediately.

If the LDO output terminal is abnormally charged and the voltage level is higher than 115% or 120% (Typ.) of the reference voltage, the OVP circuit is triggered and shuts off rails immediately.

Over-Temperature Protection (OTP)

If chip temperature is higher than 125°C, the OTP circuit will shut down all power rails. The PMIC will reboot with power- up sequence after chip temperature cools down and becomes lower than 105°C. The OTP trigger level is defined by REG_0x42[7:6].

External Regulator Enable and Power Good Monitoring

RT5168 supports 3 independent output signals (EREG1_EN, EREG2_EN, EREG3_EN) for external regulator power-on sequence requirement, also with 3 input pins (EREG1_PG, EREG2_PG, EREG3_PG) to monitor the coordinate regulator power status. The maximum waiting time between EREG*_EN and EREG*_PG is 10ms. If EREG*_EN is asserted and waits for over 10ms, and the EREG*_PG is still not asserted, the PMIC will stop the power-on process and shuts down as illustrated in Figure 2.

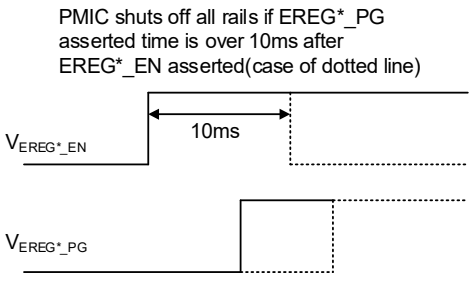


Figure 2. Power-Up Process Interrupted by EREGx_PG Status

External Regulator DVS(EREG_DVS)

EREG_DVS as output pin can buffer out 1.8V/3.3V signal for external regulator's input requirement. Refer to REG_0x6D for detailed setting descriptions.

Power Disable Mode

RT5168 supports power disable function for external input signal flag to shut down the PMIC immediately. It provides PWRDIS_IN as input to accept the shutdown flag, and the PWRDIS_OUT as a buffer output to follow the PWRDIS_IN's flag and assert "High" when entering power disable mode.

Once the PWRDIS_IN accepts the shutdown signal from SOC, the PMIC waits for the AUTO_SHUTDOWN_TIME time up and then shut down all rails immediately.

The PWRDIS_ACK serves as an input to accept the acknowledge signal from SOC; if the ACK signal is asserted before AUTO_SHUTDOWN_TIME time up, the PMIC shuts down all rails immediately as illustrated in Figure 3.

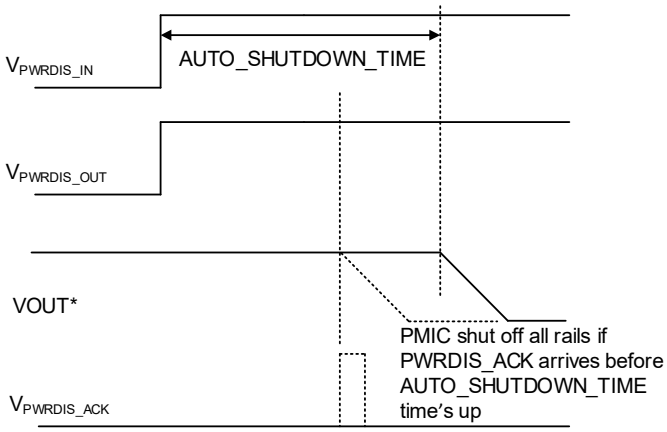


Figure 3. Cases for Entering Power Disable Mode

Power Indication (RST_L) and Interrupt Indication (GEN_INT_L)

RST_L is the indication output pin. When all regulator rails follow the settled sequence power-up successfully, the RST_L asserts "high" after the last rail finishes the power-up procedure.

After power-up procedure completes, for any fault event (refer to REG_0x72 for definition) that triggers protection mechanism, the PMIC shuts down

immediately and RST_L asserts “low”.

The delay time of RST_L is defined by REG_0x41[3:1]. The two cases are illustrated in Figure 4, where the external regulator power-good waiting time of 10ms is counted, and instead PMIC's regulator rail, it is used as the last regulator.

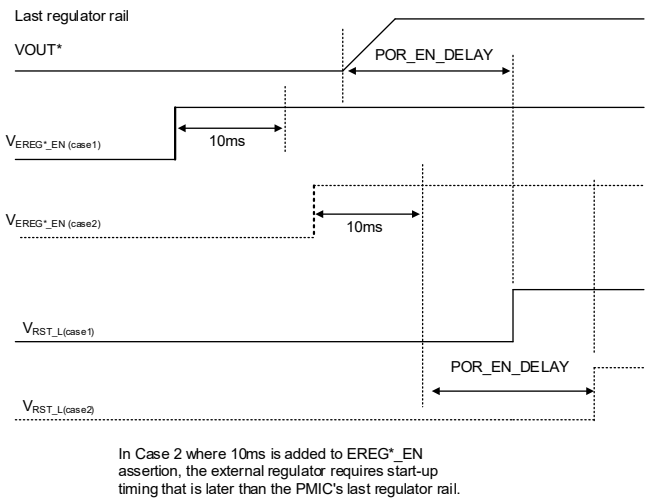


Figure 4. Power-Up Process Completion and RST_L Assertion

GEN_INT_L is output pin to indicate which interrupt event causes PMIC shutdown. It is flexible that the user can choose which event should be included by setting REG_0x71. While interrupt event is detected and causes PMIC shutdown immediately, if this specific interrupt event is included by setting of REG_0x71, GEN_INT_L asserts “low”.

Input Current-Limit Indication (IIN_LIM)

RT5168 integrates ADC function for input power monitoring purpose, the input current sensing voltage “V_{SENSE}” which crosses on “SENSE+ “ and “SENSE- “ pins indicates the input current level.

The IIN_LIM is used to alert the input overcurrent event. When V_{SENSE} is over the defined input overcurrent range, IIN_LIM asserts “high” and the PMIC keeps normal operation. If input current decreases to the level that V_{SENSE} is lower than the overcurrent range, IIN_LIM asserts “low”. See **Input Power Monitoring** section for more detailed description of the pin application.

Protection Mode (Hiccup/Latch-Off)

The RT5168 supports two protection modes when fault events occur, it can be defined by the user with REG_0x41[4].

For Hiccup Mode, when the protection function is triggered, the PMIC will shut down all rails for a period of time and then attempts to recover automatically. It retries a maximum of five times, and then latches the PMIC if the power-up procedure is not completed successfully. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resumes normal operation as soon as the overload or short circuit is removed.

For Latch-Off Mode, when the protection function is triggered, the PMIC shuts down all rails and goes into Latch-Off Mode. Only input re-power on over VIN UV rising threshold restarts the PMIC operation.

Absolute Maximum Ratings (Note 1)

- VINx, SENSE+, SENSE- to AGNDx ---------- –0.3V to 17.5V
- SWx to PGNDx (DC) ---------- –0.3V to 17.5V
- SWx to PGNDx (<100ns) ---------- –6.5V to 25.5V
- PGNDx to AGNDx ---------- –0.3V to 0.3V
- INT_REG_OUT, INLDO, OUTLDO to AGNDx ---------- –0.3V to 6V
- FB_x to AGNDx ---------- –0.3V to 6V
- EREGx_EN, EREGx_PG, EREG_DVS to AGNDx ---------- –0.3V to 6V
- PWRDIS_IN, PWRDIS_OUT, PWRDIS_ACK to AGNDx ---------- –0.3V to 6V
- IIN_LIM, RST_L, GEN_INT_L to AGNDx ---------- –0.3V to 6V
- Junction Temperature ---------- –30°C to 150°C
- Storage Temperature Range ---------- –60°C to 260°C
- Lead Temperature 1.6mm (1/16 inch) from case for 10 seconds ---------- 300°C

ESD Ratings (Note 2)

- ESD Susceptibility

  ESD rating, all pins Human Body Model (HBM) ---------- ±2kV

  ESD rating, all pins Charge Device Model (CDM) ---------- ±500V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 4V to 16V
- Ambient Temperature Range ---------- 0°C to 85°C
- Junction Temperature Range ---------- 0°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		UQFN-40L 5x5 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	25	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	1	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	21.3	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	<1	°C/W

Electrical Characteristics

(VIN1 = VIN2 = VIN3 = VIN4 = VIN5 = 12V, T_A = 25°C , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Supply Input Voltage	VINx	Input voltage range	4	--	16	V
Supply Input Current	I_{Q_VIN}	All VRs OFF, $V_{IN} > V_{INTREGOUT}$	--	220	300	μA
	I_{SBY_VIN}	All VRs OFF, I^2C active	--	1.4	1.8	mA
VIN Undervoltage	V_{IN_UV}	V_{IN_UV} =3.8V, Rising Note: programmable range= 3.8V, 4.3V, 6V, 8V	3.5	3.8	4.1	V
		Falling	--	Rising –0.3	--	V
VIN Overvoltage	V_{IN_OV}	V_{IN_OV} =16V, Rising Note: programmable range: 14V, 15V, 16V, 17V	15.5	16	16.5	V
		Hysteresis, Falling.	--	Rising –0.5	--	V
Thermal Shutdown	Temp_OT	Thermal Shutdown = 145°C, rising threshold Note: Rising, programmable range: 115°C, 125°C, 135°C, 145°C	140	145	150	°C
		Hysteresis	--	20	--	
Current Sense						
CS Accuracy	V_{CS}	$V_{SENSE+} - V_{SENSE-}$ = 60mV	–2	--	2	%
Internal Regulator						
INT_REG_OUT Output Voltage	$V_{INTREGOUT}$	VIN5 = 12V, $0 < I_{INTREGOUT} < 150mA$	4.5	5	5.5	V
INT_REG_OUT UVLO	$V_{INTREGOUT\_UV\_R}$	Rising	3.2	3.5	3.8	V
	$V_{INTREGOUT\_UV\_F}$	Falling	--	2.5	2.8	V
INT_REG_OUT Output Current Limit	$I_{LIM\_INTREGOUT}$	VIN5 = 12V, $0 < V_{INTREGOUT} < 4V$	150	300	450	mA
Buck1 Converter (Rail1)						
Input Voltage Range	V_{IN_1}	Input voltage range	4	12	16	V
Quiescent Current	I_{Q_1}	$V_{FB1} >$ VID, no switching	--	320	450	μA
Output Voltage Range	V_{OUT_1}	V_{FB1} setting range, 1.2V default	0.3	--	3.46	V
VOUT AVS/DVS	V_{OUT_AVS1}	Output Voltage in AVS mode	–15	--	15	%
Regulation Voltage Accuracy	V_{FB_1}	Active Mode, output voltage regulation. VOUT = 1.2V	–1	--	1	%

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Switching frequency	f_{SW_1}	PWM mode	f_{SW} = 0.6MHz	0.51	0.6	0.69	MHz
			f_{SW} = 0.8MHz	0.72	0.8	0.88	
			f_{SW} = 1MHz	0.9	1	1.1	
			f_{SW} = 1.2MHz	1.08	1.2	1.32	
Soft-Start Time	t_{SS_1}	Soft-start time = 2 ms Note: Programmable range: 0.5ms to 10ms		--	2	--	ms
Output Load Transient	AC_{LOAD_1}	V_{IN} = 12V, V_{OUT1} = 1.2V, L = 0.33µH, C_{OUT1} = 22µF x 7, 20% to 80% of I_{MAX} in 1µs		–4	--	4	%
High-Side Switch On- Resistance	$R_{DS(ON)\_H\_1}$	V_{IN1} - V_{SW1} = 0.1V		--	60	110	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L\_1}$	V_{SW1} - V_{PGND1} = 0.1V		--	12.5	20	mΩ
Selectable Bleed Resistance	R_{DIS_1}	Soft-stop discharge = 10 Ω Programmable range: 10Ω, 20Ω, 50Ω, Hi-Z		6	10	14	Ω
Bleed Monitor Comparator	$V_{LOW\_TH\_1}$			--	0.07	0.1	V
Overvoltage Protection	V_{OV_1}	V_{OV_1} = 120%, Rising threshold Note: Programmable range: 110%, 115%, 120%		115	120	125	%
		Hysteresis		--	2.5	--	
Undervoltage Protection	V_{UV_1}	V_{UV_1} = 85%, Falling threshold Programmable range: 90%, 85%, 80%		80	85	90	%
		Hysteresis		--	2.5	--	
OV/UV Deglitch Time	T_{OV/UV_DLY1}	Programmable setting: 5µs (default), Disable deglitch (option)		--	5	--	µs
Overcurrent Limit	I_{LIM_1}	Valley current, 8A setting.		6.4	8	9.6	A
		Valley current, 9A setting.		7.2	9	10.8	
		Programmable range: (7.5A, 8A, 8.5A, 9A)		7.5	--	9	
Overcurrent Protection	OCP_1	Two option for OCP mode: 16 cycle then latch or No latch (continuous current limit)		16	--	N	cycle
DVS SR	DVS_{SR_1}	Programmable range: 0.25, 0.5, 1, 5 (mV/µs)		0.25	--	5	mV/µs
Enable Time	T_{EN_1}	Programmable range: 0ms to 127ms		0	--	127	ms
Buck2/3 Converter (Rail2/3)							
Input Voltage Range	V_{IN_2}, V_{IN_3}	Input voltage range		4	12	16	V
Quiescent Current	I_{Q_2}, I_{Q_3}	V_{FBx} > VID, no switching		--	300	420	µA
Output Voltage Range	V_{OUT_2}, V_{OUT_3}	V_{FBx} setting range, 0.9V/1.8V default		0.3	--	3.46	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VOUT AVS/DVS	V_{OUT_AVS2}, V_{OUT_AVS3}	Output voltage in AVS mode		–15	--	15	%
Regulation Voltage Accuracy	V_{FB_2}	Active Mode, output voltage regulation. VOUT = 0.9V		–1	--	1	%
	V_{FB_3}	Active Mode, output voltage regulation. VOUT = 1.8V		–1	--	1	%
Switching Frequency	f_{SW_2}, f_{SW_3}	PWM mode	f_{SW} = 0.6MHz	0.51	0.6	0.69	MHz
			f_{SW} = 0.8MHz	0.72	0.8	0.88	
			f_{SW} = 1MHz	0.9	1	1.1	
			f_{SW} = 1.2MHz	1.08	1.2	1.32	
Soft-Start Time	t_{SS_2}, t_{SS_3}	Soft-start time = 2 ms Note: Programmable range: 0.5ms to 10ms		--	2	--	ms
Output Load Transient	AC_{LOAD_2},	V_{IN} = 12V, V_{OUT2} = 0.9V, L = 1µH, C_{OUT2} = 22µF x4, 20% to 80% of I_{MAX} in 1µs		–4	--	4	%
	AC_{LOAD_3}	V_{IN} = 12V, V_{OUT3} = 1.8V, L = 1.5µH, C_{OUT2} = 22µF x 4, 20% to 80% of I_{MAX} in 1µs					
High-Side Switch On-Resistance	$R_{DS(ON)\_H\_2}$, $R_{DS(ON)\_H\_3}$	V_{INX} - V_{SWX} = 0.1V		--	160	280	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L\_2}$, $R_{DS(ON)\_L\_3}$	V_{SWX} - V_{PGND23} = 0.1V		--	17	30	mΩ
Selectable Bleed Resistance	R_{DIS_2}, R_{DIS_3}	Soft-stop discharge = 10Ω Note: Programmable range: 10Ω, 20Ω, 50Ω, Hi-Z		6	10	14	Ω
Bleed Monitor Comparator	$V_{LOW\_TH\_2}$, $V_{LOW\_TH\_3}$			--	0.07	0.1	V
Overvoltage Protection	V_{OV_2}, V_{OV_3}	V_{OV_2} = V_{OV_3} = 120%, Rising threshold Note: Programmable range: 110%, 115%, 120%		115	120	125	%
		Hysteresis		--	2.5	--	
Undervoltage Protection	V_{UV_2}, V_{UV_3}	V_{UV_2} = V_{UV_3} = 85%, Falling threshold Note: Programmable range: 90%, 85%, 80%		80	85	90	%
		Hysteresis		--	2.5	--	
OV/UV Deglitch Time	T_{OV/UV_DLY2} T_{OV/UV_DLY3}	Programmable setting: 5µs (default), Disable deglitch(option)		--	5	--	µs
Overcurrent Limit	I_{LIM_2}, I_{LIM_3}	Valley current, 3A setting.		2.1	3	3.9	A
		Programmable range: (2.5A, 3A, 3.5A, 4A)		2.5	--	4	
Overcurrent Protection	OCP_2, OCP_3	Two option for OCP mode: 16 cycle then latch or No latch (continuous current limit)		16	--	N	cycle

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DVS SR	DVS_{SR_2}, DVS_{SR_3}	Programmable range: 0.25, 0.5, 1, 5 (mV/μs)		0.25	--	5	mV/μs
Enable Time	T_{EN_2}, T_{EN_3}	Programmable range: 0ms to 127ms		0	--	127	ms
Buck4/5 Converter(Rail4/5)							
Input Voltage Range	V_{IN_4}, V_{IN5}	Input voltage range		4	12	16	V
Quiescent Current	I_{Q_4}, I_{Q_5}	V_{FBx} > VID, no switching		--	300	420	μA
Output Voltage Range	V_{OUT_4}, V_{OUT_5}	V_{FBx} setting range, 1.05V/0.5V default		0.3	--	3.46	V
VOUT AVS/DVS	V_{OUT_AVS4}, V_{OUT_AVS5}	Output voltage in AVS mode		–15	--	15	%
Regulation Voltage Accuracy	V_{FB_4}	Active Mode, output voltage regulation. VOUT = 0.5V		–1	--	1	%
	V_{FB_5}	Active Mode, output voltage regulation. VOUT = 1.05V		–1	--	1	
Switching Frequency	f_{SW_4}, f_{SW_5}	PWM mode	f_{SW} = 0.6MHz	0.51	0.6	0.69	MHz
			f_{SW} = 0.8MHz	0.72	0.8	0.88	
			f_{SW} = 1MHz	0.9	1	1.1	
			f_{SW} = 1.2MHz	1.08	1.2	1.32	
Soft-Start Time	t_{SS_4}, t_{SS_5}	Soft-start time = 2 ms Note: Programmable range: 0.5ms to 10ms		--	2	--	ms
Output Load Transient	AC_{LOAD_4},	V_{IN} = 12V, V_{OUT4} = 0.5V, L = 0.33μH, C_{OUT4} = 22μF x 7, 20% to 80% of I_{MAX} in 1μs		–4	--	4	%
	AC_{LOAD_5}	V_{IN} = 12V, V_{OUT5} = 1.05V, L = 0.68μH, C_{OUT5} = 22μF x 4, 20% to 80% of I_{MAX} in 1μs					
High-Side Switch On-Resistance	$R_{DS(ON)\_H\_4}$, $R_{DS(ON)\_H\_5}$	V_{INX} - V_{SWX} = 0.1V		--	160	280	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L\_4}$, $R_{DS(ON)\_L\_5}$	V_{SWX} - V_{PGND45} = 0.1V		--	17	30	mΩ
Selectable Bleed Resistance	R_{DIS_4}, R_{DIS_5}	Soft-stop discharge = 10 Ω Note: Programmable range: 10Ω, 20Ω, 50Ω, Hi-Z		6	10	14	Ω
Bleed Monitor Comparator	$V_{LOW\_TH\_4}$, $V_{LOW\_TH\_5}$			--	0.07	0.1	V
Overvoltage Protection	V_{OV_4}, V_{OV_5}	V_{OV_2} = V_{OV_3} = 120%, Rising threshold Note: Programmable range: 110%, 115%, 120%		115	120	125	%
		Hysteresis		--	2.5	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Undervoltage Protection	V_{UV_4}, V_{UV_5}	V_{UV_2} = V_{UV_3} = 85%, Falling threshold. Note: Programmable range: 90%, 85%, 80%	80	85	90	%
		Hysteresis	--	2.5	--	
OV/UV Deglitch Time	T_{OV/UV_DLY4}, T_{OV/UV_DLY5}	Programmable setting: 5μs (default), Disable deglitch(option)	--	5	--	μs
Overcurrent Limit	I_{LIM_4}	Valley current,4A setting.	2.8	4	5.2	A
		Programmable range: (3.5A, 4A, 4.5A, 5A)	3.5	--	5	A
	I_{LIM_5}	Valley current,4A setting.	2.8	4	5.2	A
		Programmable range: (3.5A, 4A, 4.5A)	3.5	--	4.5	
Overcurrent Protection	OCP_4, OCP_5	Two option for OCP mode: 16 cycle then latch or No latch (continuous current limit)	16	--	N	cycle
DVS SR	DVS_{SR_4}, DVS_{SR_5}	Programmable range: [0.25, 0.5, 1, 5 (mV/μs)]	0.25	--	5	mV/μs
Enable Time	T_{EN_4}, T_{EN_5}	Programmable range: (0ms to 127ms [6:0])	0	--	127	ms
LDO Regulator						
Input Voltage Range	V_{INLDO}		1	--	3.6	V
Quiescent Current	I_{Q_LDO}	Light Load Mode	--	--	100	μA
Output Voltage Range	V_{OUT_LDO},	LDO setting range, 1.5V default	0.6	--	2.65	V
Regulation Voltage Accuracy	V_{LDOOUT}	Output voltage regulation. VOUT =1.5V	–1	--	1	%
Load Regulation	V_{LOAD_LDO}		–1	--	1	%
Dropout Voltage	V_{DROP_LDO}	600mA	--	--	200	mV
Soft-Start Time	t_{SS_LDO}	Soft-start time = 2 ms Note: Programmable range: 0.5ms to 10ms	--	2	--	ms
Output Load Transient	AC_{LOAD_LDO}	V_{INLDO} = 1.8V, V_{OUT_LDO} = 1.5V, C_{OUT1} = 10μF, 20% to 80% of I_{MAX} in 1μs	–4	--	4	%
Power Supply Ripple Rejection	PSRR		50	--	--	dB
Selectable Bleed Resistance	R_{DIS_LDO}	Soft-stop discharge	6	10	14	Ω
		Programmable range (11b = high-Z): (10Ω, 20Ω, 50Ω, high-Z [1:0])	10	--	50	
Bleed Monitor Comparator	$V_{LOW\_TH\_LDO}$		--	0.07	0.1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overvoltage Protection	V_{OV_LDO}	V_{OV_LDO} = 120%, Rising threshold Note: Programmable range: 110%, 115%, 120%	115	120	125	%
		Hysteresis	--	2.5	--	
Undervoltage Protection	V_{UV_LDO}	V_{UV_LDO} = 85%, Falling threshold Note: Programmable range: 90%, 85%, 80%	80	85	90	%
		Hysteresis	--	2.5	--	
OV/UV Deglitch Time	T_{OV/UV_DLYLDO}	Programmable setting: 5μs (default), Disable deglitch(option)	--	5	--	μs
Overcurrent Limit	I_{LIM_LDO}	Default 1A setting	1	--	--	A
		Programmable range: 1A, 1.5A	1	--	1.5	
Enable Time	T_{EN_LDO}	Programmable range: 0ms to 127ms	0	--	127	ms
Input Logic Level						
High Level Input Voltage	V_{IH}	V_{DD} = 3.3V	0.625 x V_{DD}	--	--	V
		V_{DD} = 1.8V/1.2V	0.7 x V_{DD}	--	--	
Low Level Input Voltage	V_{IL}	V_{DD} = 3.3V/1.8V/1.2V	--	--	0.3 x V_{DD}	V
Open-Drain						
Output Low Voltage	V_{LOW_OD}	Sink current = 1mA, with 100Ω pull-down resistance.	--	--	0.3	V
Output High Leakage	I_{LEAK_OD}	Pull-up Voltage = 5V	--	--	1	μA
I^2C for High Speed Mode						
High Level Input Voltage of SCL, SDA	VIH	V_{DD} = 1.8V/1.2V	0.7 x V_{DD}			V
Low Level Input Voltage of SCL, SDA	VIL	V_{DD} = 1.8V/1.2V			0.3 x V_{DD}	V
SCL Clock Rate	f_{SCL}		0.1	--	3.4	MHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	160	--	--	ns
Low Period of the SCL Clock	t_{LOW}		160	--	--	ns
High Period of the SCL Clock	t_{HIGH}		60	--	--	ns
Set-UP Time for a Repeated START Condition	$t_{SU;STA}$		60	--	--	ns
Data Hold Time	$t_{HD;DAT}$		0	--	70	ns
Data Set-UP Time	$t_{SU;DAT}$		10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-UP Time for STOP Condition	$t_{SU;STO}$		160	--	--	ns
Rising Time of both SDA and SCL Signals	t_R		10	--	80	ns
Falling Time of both SDA and SCL Signals	t_F		10	--	80	ns
SDA Output Low Sink Current	I_{OL}	SDA Voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} and θ_{JC} are measured or simulated at T_A = 25°C based on the JEDEC 51-7 standard.

Note 5. $\theta_{JA(EVB)}$, and $\Psi_{JC(TOP)}$ are measured on a high effective-thermal-conductivity six-layer test board which is in size of 193mm x 120mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Typical Application Circuit

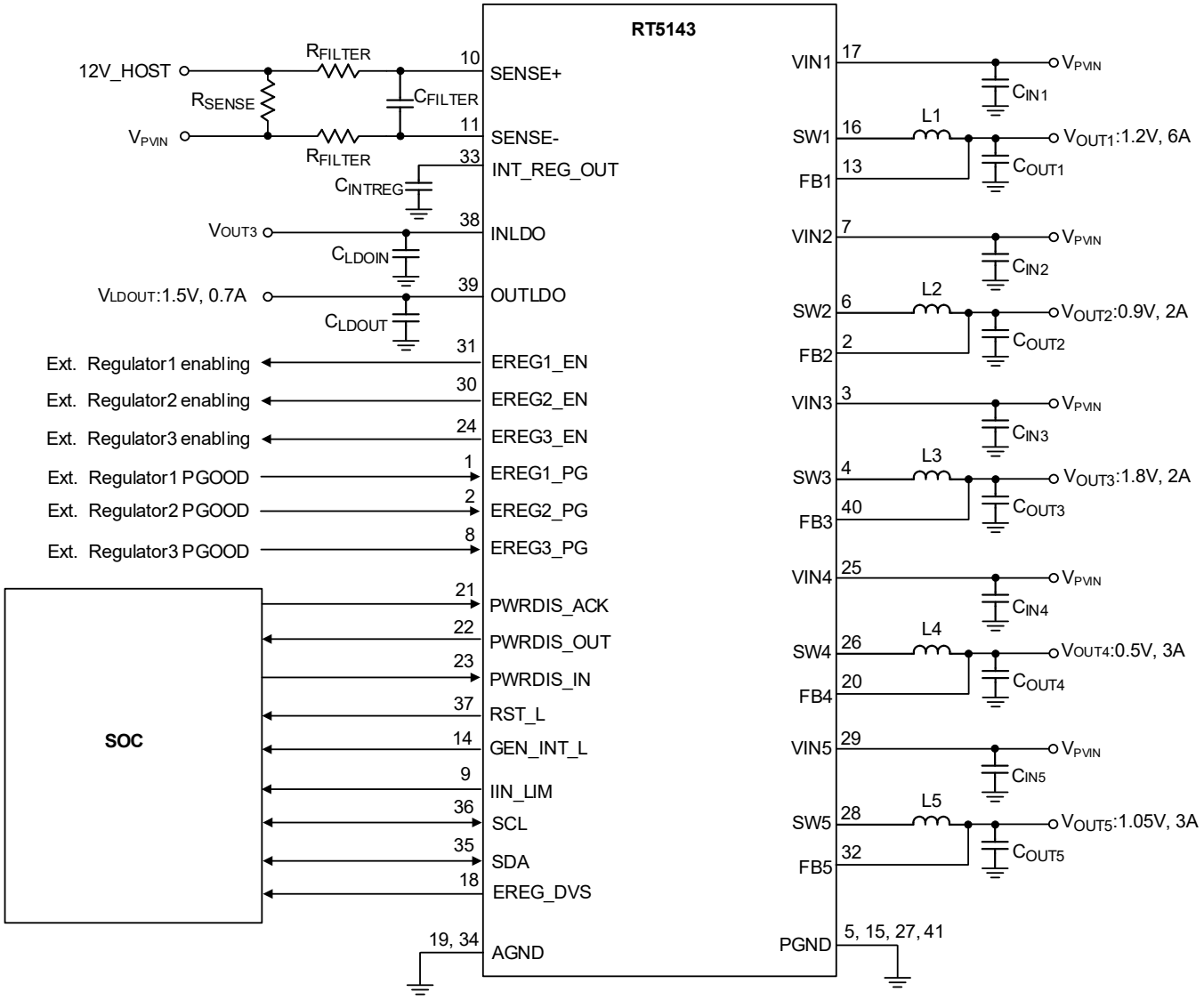


Figure 5. Application Circuit for Buck Normal Mode Operation

Table 1. Suggested Component Values for Each Rail

Rail	VOUT	L	COUT	CIN
RAIL1	1.2V	0.33µH	22µF x 6 to 22µF x 8	10µF to 22µF
RAIL2	0.9V	1µH	22µF x 4 to 22µF x 6	10µF to 22µF
RAIL3	1.8V	1.5µH	22µF x 4 to 22µF x 6	10µF to 22µF
RAIL4	0.5V	0.33µH	22µF x 4 to 22µF x 6	10µF to 22µF
RAIL5	1.05V	0.68µH	22µF x 4 to 22µF x 6	10µF to 22µF
LDO	1.5V	--	10µF	1µF

Table 2. Recommended External Components

Component	Description	Vendor P/N
CIN_BUCK	10μF/25V/X6S/0805	GRM21BC81E106KE51(Murata)
COUT_BUCK	47μF/6.3V/X5R/0603	GRM188R60J476ME15D(Murata)
CLDOIN	1μF/16V/X6S/0402	GRM155C81C105KE11(Murata)
CLDOUT	10μF/6.3V/X6S/0402	GRM155C80J106ME18D(Murata)
L1	0.33μH	HBME041B-R33MSA(Cyntec)
L2	1μH	DFE322520FD-1R0M(Murata)
L3	1.5μH	DFE322520FD-1R5M(Murata)
L4	0.33μH	DFE252012F-R33M(Murata)
L5	0.68μH	DFE322512F-R68M(Murata)

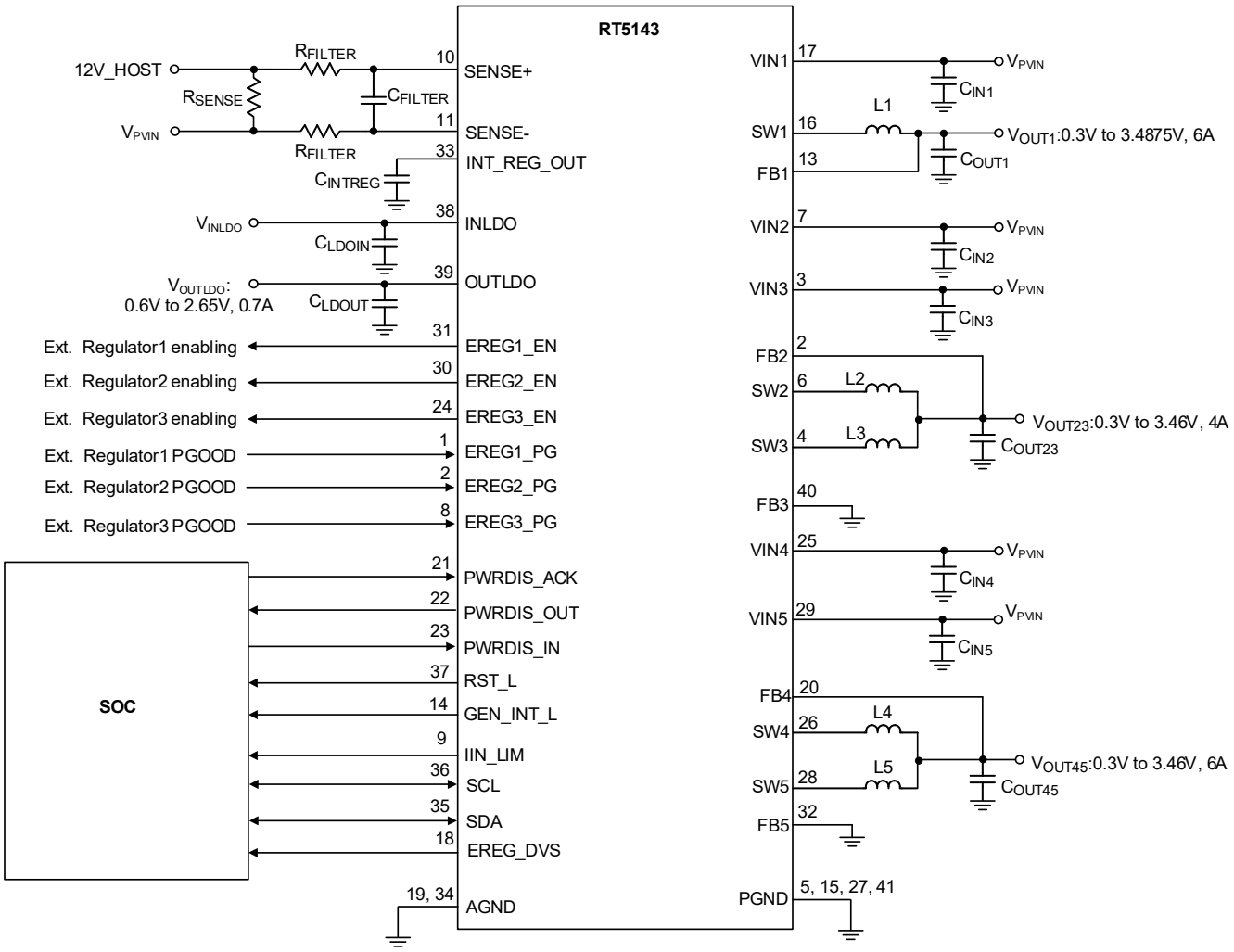
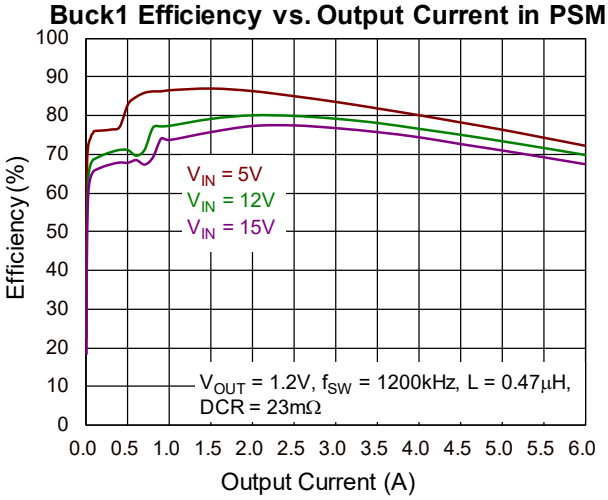


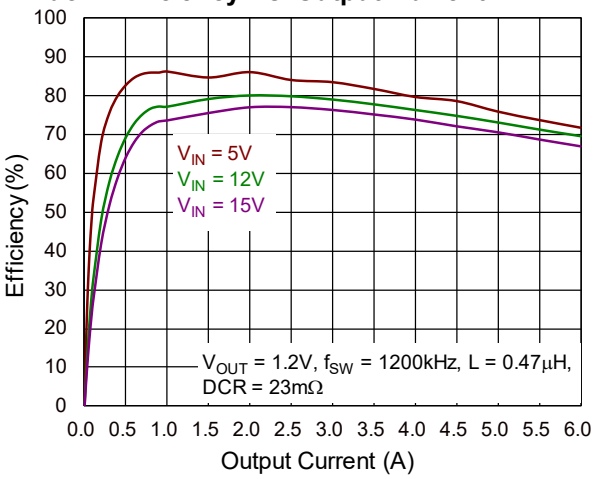
Figure 6. Application Circuit for Buck Dual-Phase Mode Operation

Typical Operating Characteristics

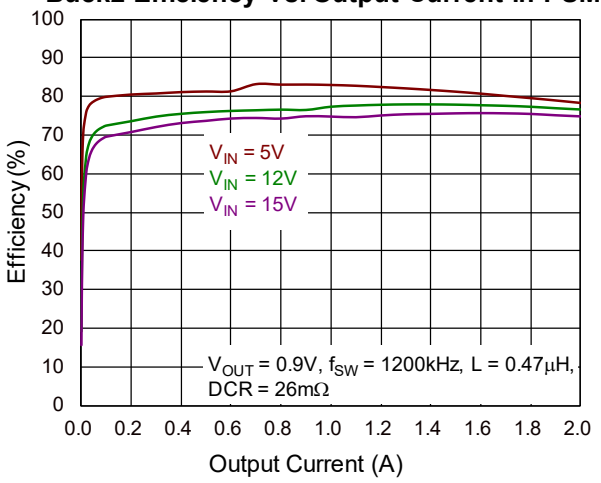
Buck1 Efficiency vs. Output Current in PSM



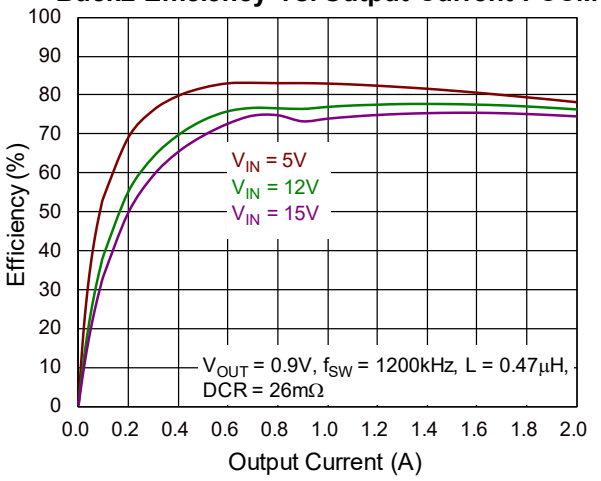
Buck1 Efficiency vs. Output Current in FCCM



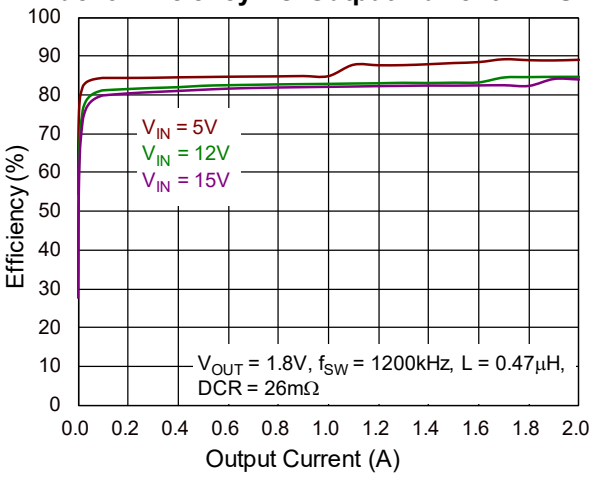
Buck2 Efficiency vs. Output Current in PSM



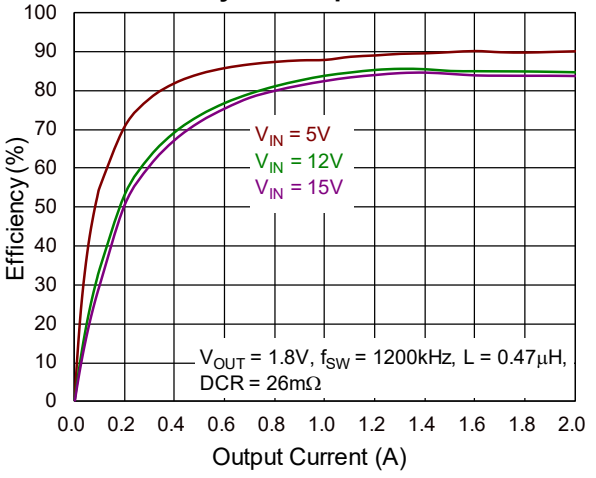
Buck2 Efficiency vs. Output Current FCCM



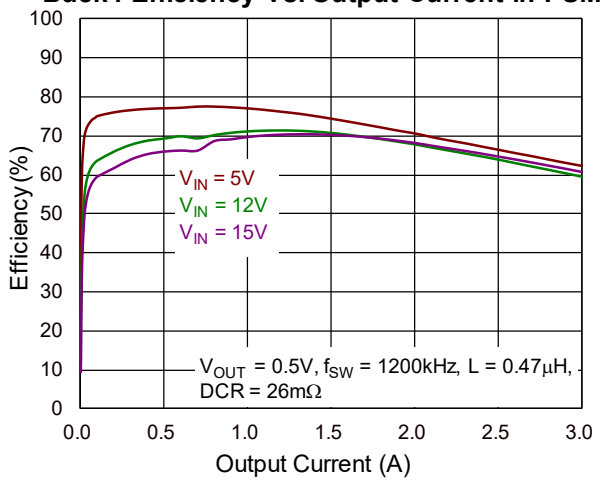
Buck3 Efficiency vs. Output Current in PSM



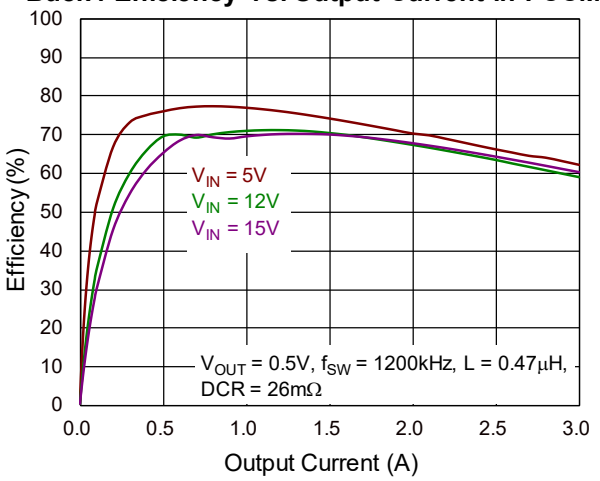
Buck3 Efficiency vs. Output Current in FCCM



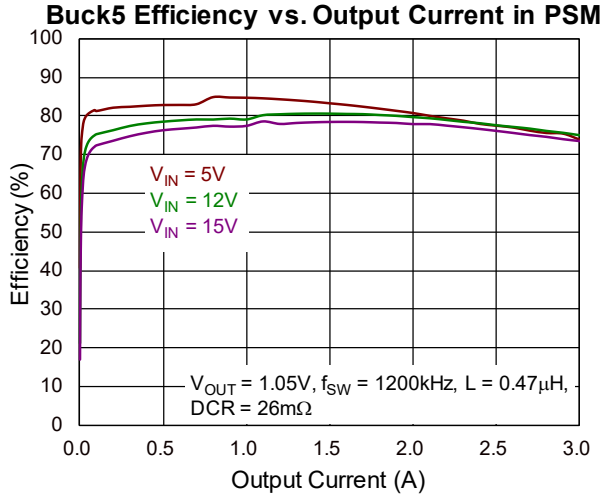
Buck4 Efficiency vs. Output Current in PSM



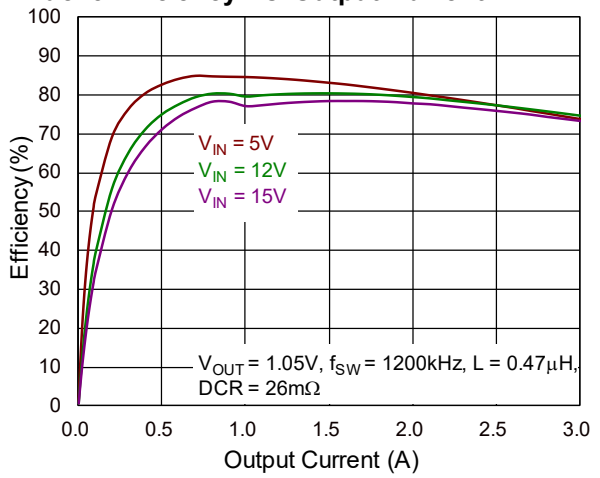
Buck4 Efficiency vs. Output Current in FCCM



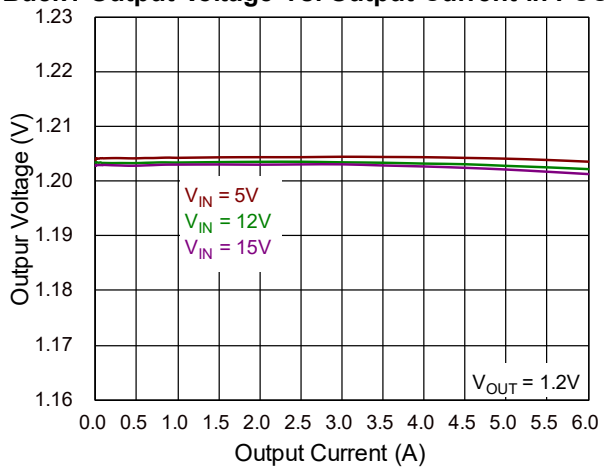
Buck5 Efficiency vs. Output Current in PSM



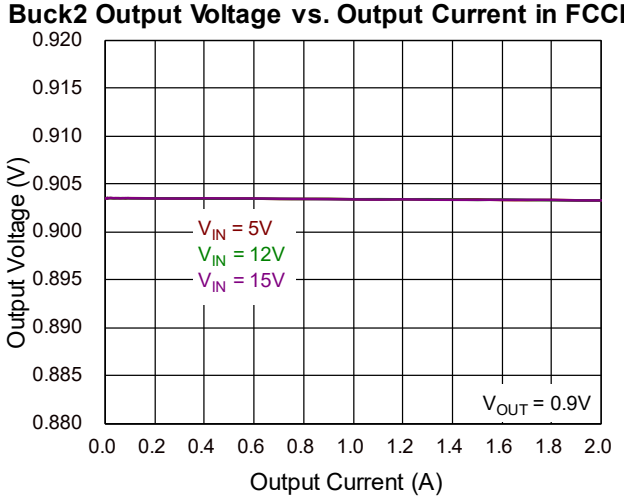
Buck5 Efficiency vs. Output Current in FCCM



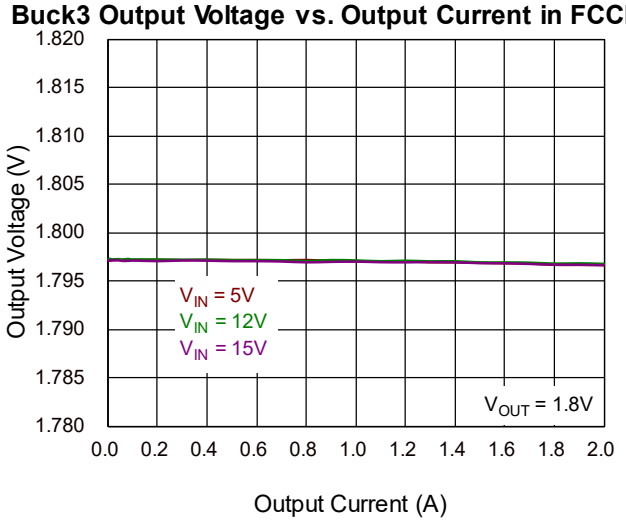
Buck1 Output Voltage vs. Output Current in FCCM



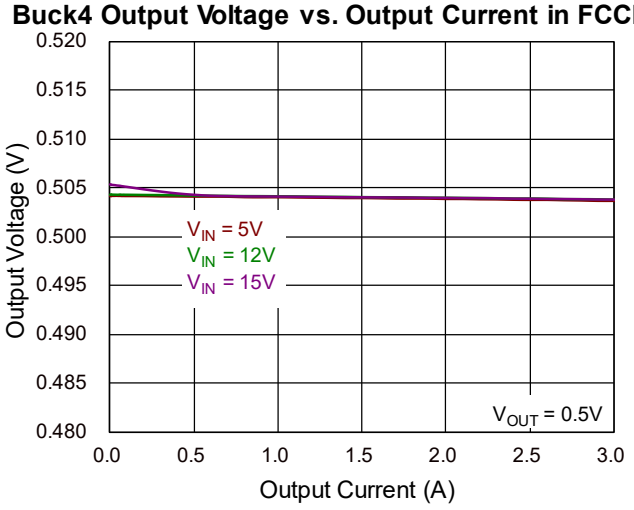
Buck2 Output Voltage vs. Output Current in FCCM



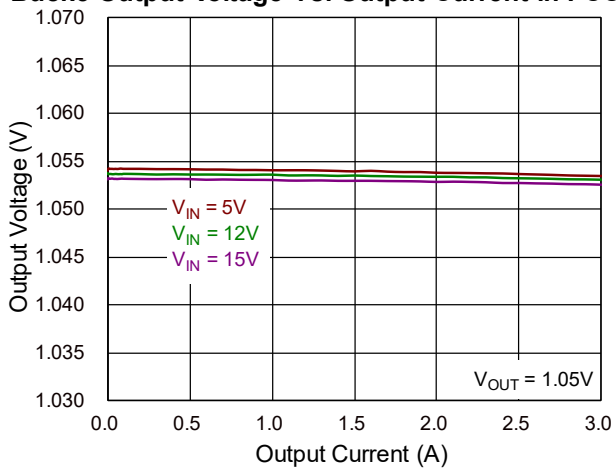
Buck3 Output Voltage vs. Output Current in FCCM



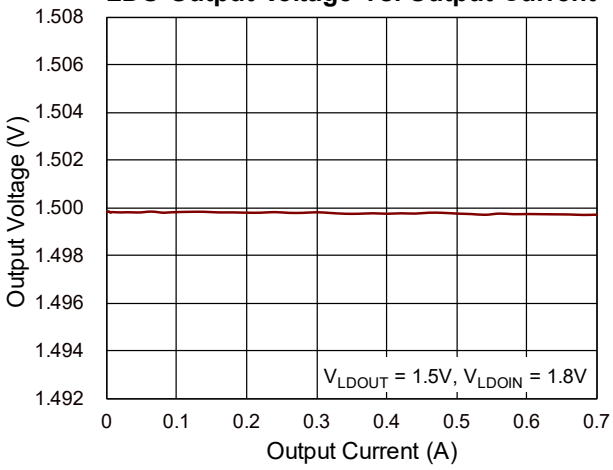
Buck4 Output Voltage vs. Output Current in FCCM



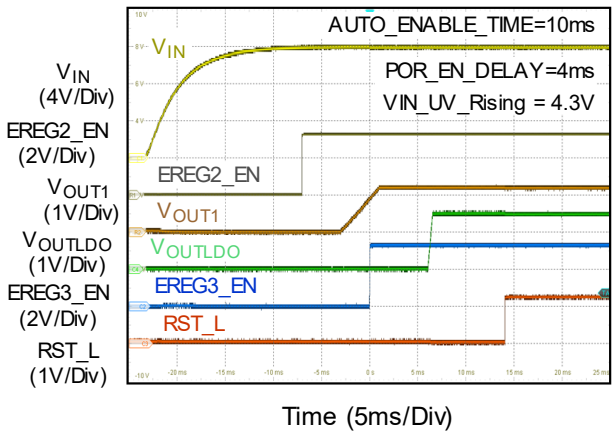
Buck5 Output Voltage vs. Output Current in FCCM



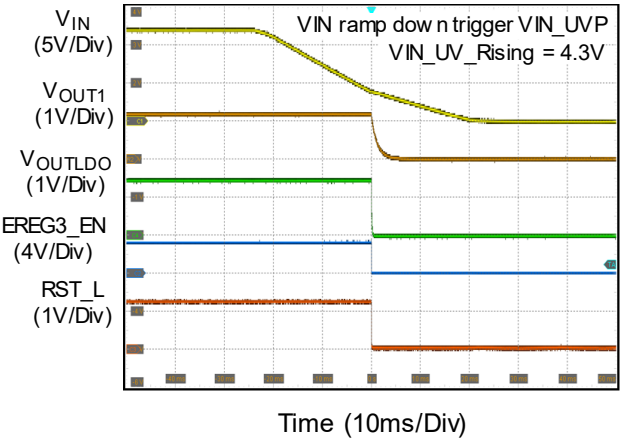
LDO Output Voltage vs. Output Current



Power-On Sequence



Power-Off Sequence



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT5168 provides five synchronous Buck regulators and one LDO for system requirement. This device can communicate with processors through I^2C interface for programming the voltage, monitoring the status. Table 3 lists the power rails provided by RT5168, the basic application circuit is shown in Typical Application Circuit. The output voltage setting is defined by REG_0x56 to 0x5B.

Table 3. Detail of Power Rails

Rail	Type	FB ration	Output Voltage Range	Current Rating
RAIL1	Step-down Buck Converter	100% (Default)	0.3V to 2.1V with 10mV/step	6A
		50%	0.3V to 3.46V with 20mV/step	
RAIL2	Step-down Buck Converter	100% (Default)	0.3V to 2.1V with 10mV/step	2A
		50%	0.3V to 3.46V with 20mV/step	
RAIL3	Step-down Buck Converter	100% (Default)	0.3V to 2.1V with 10mV/step	2A
		50%	0.3V to 3.46V with 20mV/step	
RAIL4	Step-down Buck Converter	100% (Default)	0.3V to 2.1V with 10mV/step	3A
		50%	0.3V to 3.46V with 20mV/step	
RAIL5	Step-down Buck Converter	100% (Default)	0.3V to 2.1V with 10mV/step	3A
		50%	0.3V to 3.46V with 20mV/step	
LDO	Linear Regulator	100%	0.6V to 2.65V with 50mV/step	0.7A

Internal VCC Regulator (INT_REG_OUT)

INT_REG_OUT is the output of internal LDO, this LDO is used to apply power to internal circuits. Putting a capacitor of 10μF for stability. Please do not connect the INT_REG_OUT to provide power to other devices or loads.

LDO Dropout Voltage

The dropout voltage of LDO refers to the required minimum voltage difference which across the INLDO and OUTLDO pins while operating at specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(LDO)}$. Thus the dropout voltage can be defined as (V_{DROP_LDO} = V_{INLDO} – V_{OUTLDO} = $R_{DS(LDO)}$ x I_{RATED}). For normal operation, the suggested LDO operating range is (V_{INLDO} > V_{OUTLDO} + V_{DROP_LDO}) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Rail Power-up and Power-Off

After input power is applied on the PMIC and the internal sequence ready signal [SEQ_READY] asserts, the rail power-up sequence starts as Figure 7 shows below. After a settled delay time AUTO_EN_TIME, the rails follow the settled enable time [EN_TIME_*] to power up respectively.

For buck and LDO rails, users can configure rail soft-start timing by [SOFT_START_TIME_*]. When fault events are detected, all rails power off at the same time and the regulators is discharged by internal impedance load defined by [SOFT_STOP_RDIS_*].

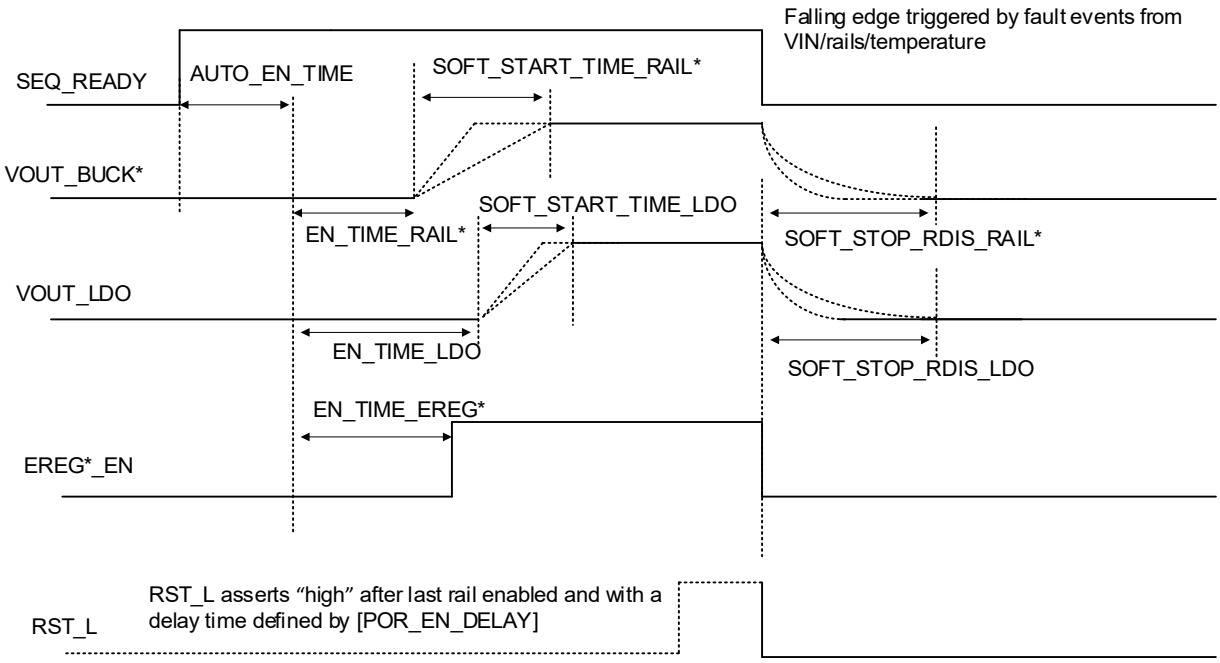


Figure 7. Rail Power-On and Power-Off Procedure

Output Residual Voltage Check

In some cases, rails may have leakage from next stage and with residual charge on output capacitor. To avoid abnormal power-up sequence, the PMIC builds in the output residue check circuit and detects the voltage level on output of each rail. As illustrated in Figure 8, if the voltage level is higher than the checking threshold, the rail will not proceed the power-on process and the PMIC latches when the enable timing is reached.

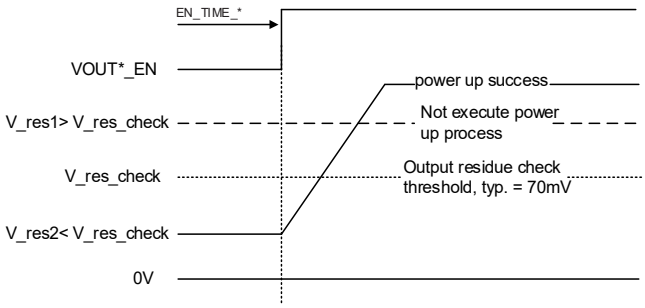


Figure 8. Output Residual Voltage Check During Power-Up Process

Input Power Monitoring

The RT5168 applies an analog to digital converter to reflect the input voltage and current for input power monitoring requirement. The Input voltage sensing point is located on RAIL1's input pin "VIN1". Be aware that layout trace from the host supply to the PMIC input pins should be as short as possible to avoid too much trace loss. The input current sensing voltage "V_{SENSE}" which crosses on "SENSE+ "and "SENSE-" pins indicates the input current level. Choose 10mΩ current sense resistor for general use. The formula of each analog-to-digital converter is shown below.

$$\text{VIN Voltage Sense} = 9.7\text{mV} \times \text{ADC\_code(DEC)}$$

$$\text{VIN Current Sense} = 0.977\text{mV} / \text{RSNS}(10\text{m}\Omega) / \text{ISEN\_GAIN} \times \text{ADC\_code(DEC)}$$

IIN_LIM is of indication purpose to monitor the overcurrent event, users can define the overcurrent-limit threshold by REG_0x73 and 0x74. As Figure 9 illustrates, if input current I_VIN is over the defined overcurrent threshold, the IIN_LIM asserts and the PMIC keeps the operation and will not shut down. The IIN_LIM assertion has "Latch Mode" and "Free Run Mode" for option. For "Latch Mode", after IIN_LIM asserts, the signal keeps "high" consistently even I_VIN is lower than current-limit threshold. While "Free Run Mode" will de-asserts the IIN_LIM once the I_VIN decreases and becomes lower than the configured level.

Additionally, the delta voltage between Sense+ and

Sense- should be smaller than 1.4V/ISEN_GAIN for ADC input common mode range.

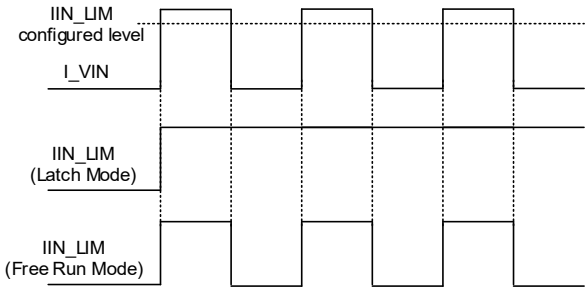


Figure 9. IIN_LIM “Latch Mode” and ”Free Run Mode” Operation

Causes of Initialization

The RT5168 automatically powers up itself only when given a reasonable input power. To know the cause of PMIC re-power up, REG_0x04[7:4] indicates the reason for the most recent initialization. For specific initialization causes, users can check the corresponding registers 0x08, 0x09, 0x0A, 0x0B and 0x0C to find out more detailed information.

- First Power-Up (REG_0x04[7:4] = 0000b) – PMIC first powers up successfully after detecting input V_{IN} > V_{IN_UV} rising threshold
- PWRDIS assertion (REG_0x04[7:4] = 0001b) – PMIC initialized by PWRDIS assertion event
- PMIC initialized by OVP event (REG_0x04[7:4] = 0010b) – Overvoltage Protection detected on VIN or rails
- PMIC initialized by UVP event (REG_0x04[7:4] = 0011b). – Undervoltage Protection detected on VIN or rails
- PMIC initialized by OCP event (REG_0x04[7:4] = 0100b) – Overcurrent Protection detected on VIN or rails
- PMIC initialized by EREG_PG1 timeout event (REG_0x04[7:4] = 0101b) – EREG_PG1 assertion timing out of restricted range.
- PMIC initialized by EREG_PG2 timeout event (REG_0x04[7:4] = 0110b) – EREG_PG2 assertion timing out of restricted range.
- PMIC initialized by EREG_PG3 timeout event (REG_0x04[7:4] = 0111b) – EREG_PG3 assertion timing out of restricted range.
- PMIC initialized by OTP event (REG_0x04[7:4] = 1000b) – Over-Temperature Protection detected.

Buck Dual-Phase Mode Enabling

The RT5168 supports buck rails operating at dual-phase mode for better response and larger load requirement. This function can be enabled by REG_0x45[2:1] if the circuit is settled as illustrated in the Typical Application Circuit, dual phase mode application circuit.

While operating at dual phase mode, “Master” rail setting is followed for dual-phase buck control, and the “Slave” rail setting can be ignored. Table 4 lists the dual-phase buck combinations and control methods.

Table 4. Dual-Phase Buck Combination and Control

Dual phase Buck	Combination	Control	f_{SW_DUAL}	V_{OUT_DUAL}	I_{RATED_DUAL}
Rail23	Rail2	Master	2 x f_{SW2}	V_{OUT2}	4A
	Rail3	Slave			
Rail45	Rail4	Master	2 x f_{SW4}	V_{OUT4}	6A
	Rail5	Slave			

Serial Interface

The RT5168 provides a general-purpose serial interface to control and monitor the configuration registers. The serial interface supports the I^2C protocol 2.1 with standard slave mode (100Kbps), fast mode (400Kbps), and high-speed mode (3.4Mbps). In addition, the PMIC supports four slave addresses to make system able to control maximum four ICs of the RT5168 on the same I^2C bus.

The four slave addresses are 0x68, 0x69, 0x6A and 0x6B and can be configured in the REG_0x43[3:2]. About VDD reference levels of the general-purpose I^2C module, RT5168 provides three voltage levels for selection and it can be set as one of 3.3V, 1.8V and 1.2V by setting the REG_0x43[7:6].

For register write access, it will need write password A5'h on REG_0x03 before change each individual register, the password register will be automatically reset after executing any write command. Below shows the examples for normal register change steps and normal NVM program procedure for reference.

Table 5. Steps for Change Each Individual Register Value

Power on VIN above V_{IN_UV} rising level			
Slave Address	Register	Write Value	Description
0x68	0x03	A5'h	Password key
0x68	0x56	0'h	Change REG_0x56 value as 0'h
0x68	0x03	A5'h	Password key
0x68	0x57	1'h	Change REG_0x57 value as 1'h
Change register value done			

Table 6. Steps for Change Each Individual Register Value and NVM Programing Process

Power on VIN above V_{IN_UV} rising level			
Slave Address	Register	Write Value	Description
0x68	0x03	A5'h	Password key and bypass CRC code
0x68	0x04	08'h	
0x68	0x03	A5'h	Password key and change registers' value. The password needs to be written for each individual register.
0x68	0x56	00'h	
0x68	0x03	A5'h	
0x68	0x57	01'h	
0x68	0x03	A5'h	
0x68	0x58	02'h	
0x68	0x03	A5'h	Test Mode key and write user range NVM procedure.
0x68	0x30	62'h	
0x68	0x31	86'h	
0x68	0x03	A5'h	
0x68	0x33	80'h	
User NVM programing done			

A multiple byte reading over the I²C interface can also be achieved. When performing a multiple byte read, the PMIC will automatically increase to the next address for subsequence byte. While for byte writing, it must write the password [A5'h] on REG_0x03 first, then the interface allows users to write the data on assigned register. Figure 10, Figure 11 and Figure 12 show the I²C-related information.

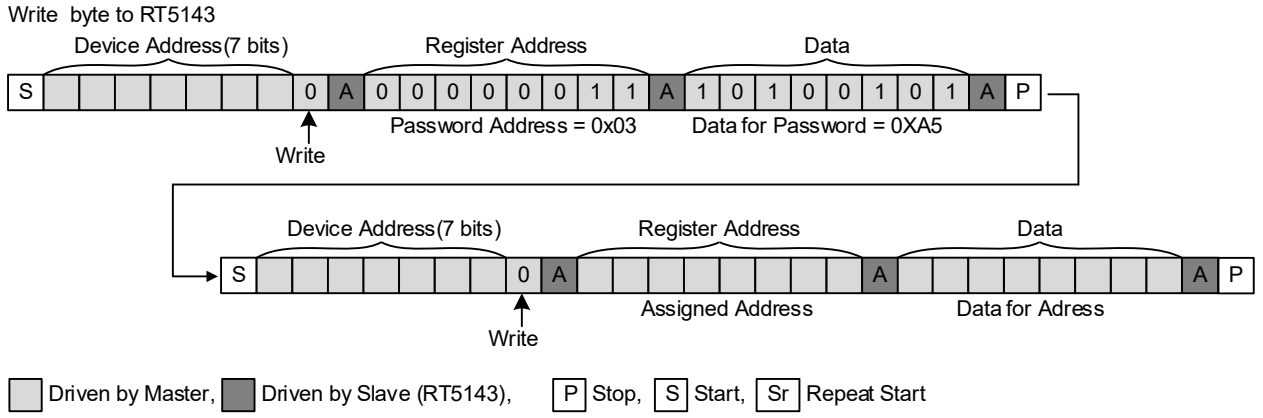


Figure 10. I²C Write Access Byte

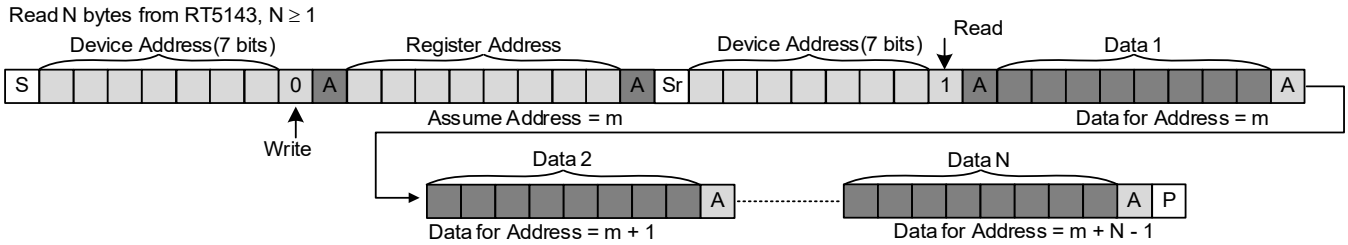


Figure 11. I²C Read Access Multiple Bytes

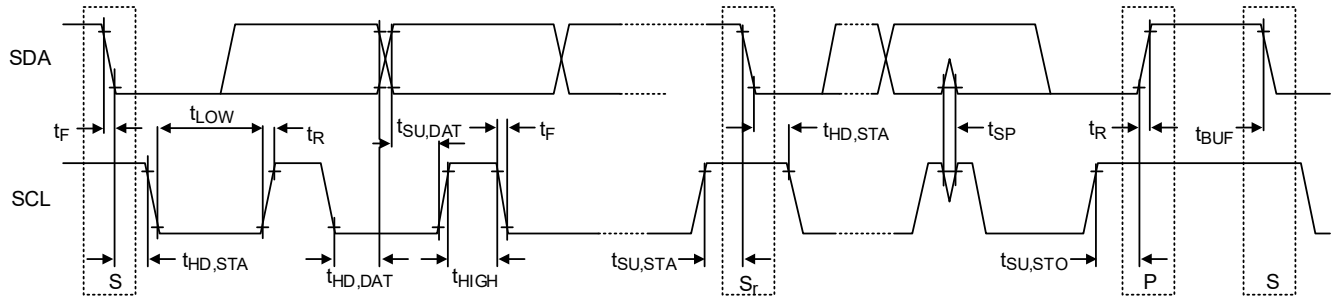


Figure 12. I²C Waveform Information

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a UQFN-40L 5x5 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 21.3°C/W on a standard high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)} = (125°C - 25°C) / (21.3°C/W) = 4.69W$ for a UQFN-40L 5x5 (FC) (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

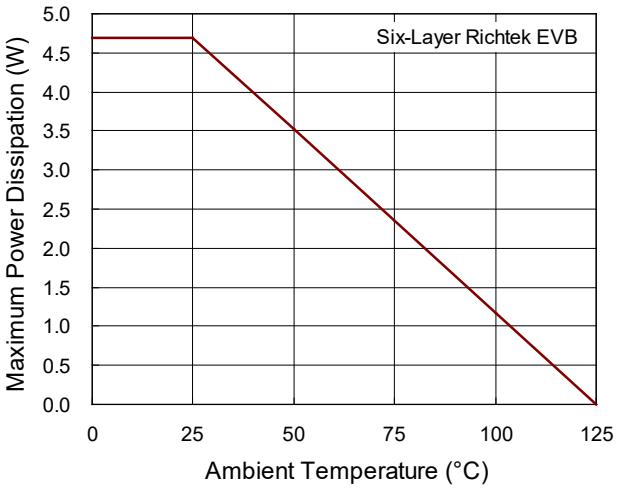


Figure 13. Derating Curve of Maximum Power Dissipation

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RT5168.

- At least four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Input capacitors of bucks should be placed at the back side of the board, the bottom PVIN trace connected to the input pins on top layer through the via.
- Place all the input capacitors as close to input pins as possible and the internal 5V regulator decoupling capacitor, C_{INTREG}, as close to INT_REG_OUT pin as possible.
- Set multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.
- To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RT5168 to additional ground planes within the internal layers or on the bottom side.
- The high frequency switching nodes, SW, should be as small as possible. Keep analog components and

signal away from the SW path.

- The power ground should be close to the IC to minimum the ground current loops. For noise immunity consideration, keep enough isolation between analog return signals and power path by ground plane.
- Connect the feedback sense network behind via of output capacitor.

Below shows two different PCB layout options for reference:

Option 1: Inductor of buck rails placed at the same side with the PMIC, PVIN input caps placed on the back side to the PMIC. This layout method provides the minimized SW path for the efficiency consideration.

Option 2: PVIN input caps placed at the same side with the PMIC, and inductors placed on the back side to the PMIC. Compared with Option 1, it reduces the parasitic inductance and impedance contributed by vias and is with better noise immunity to PVIN source. However, it also requires to set vias near SW pin from top layer to bottom layer. It is suggested to add vias as much as possible to minimize the trace impedance and to meet the required current capacity of each voltage rail.

Layout Reference (Option 1)

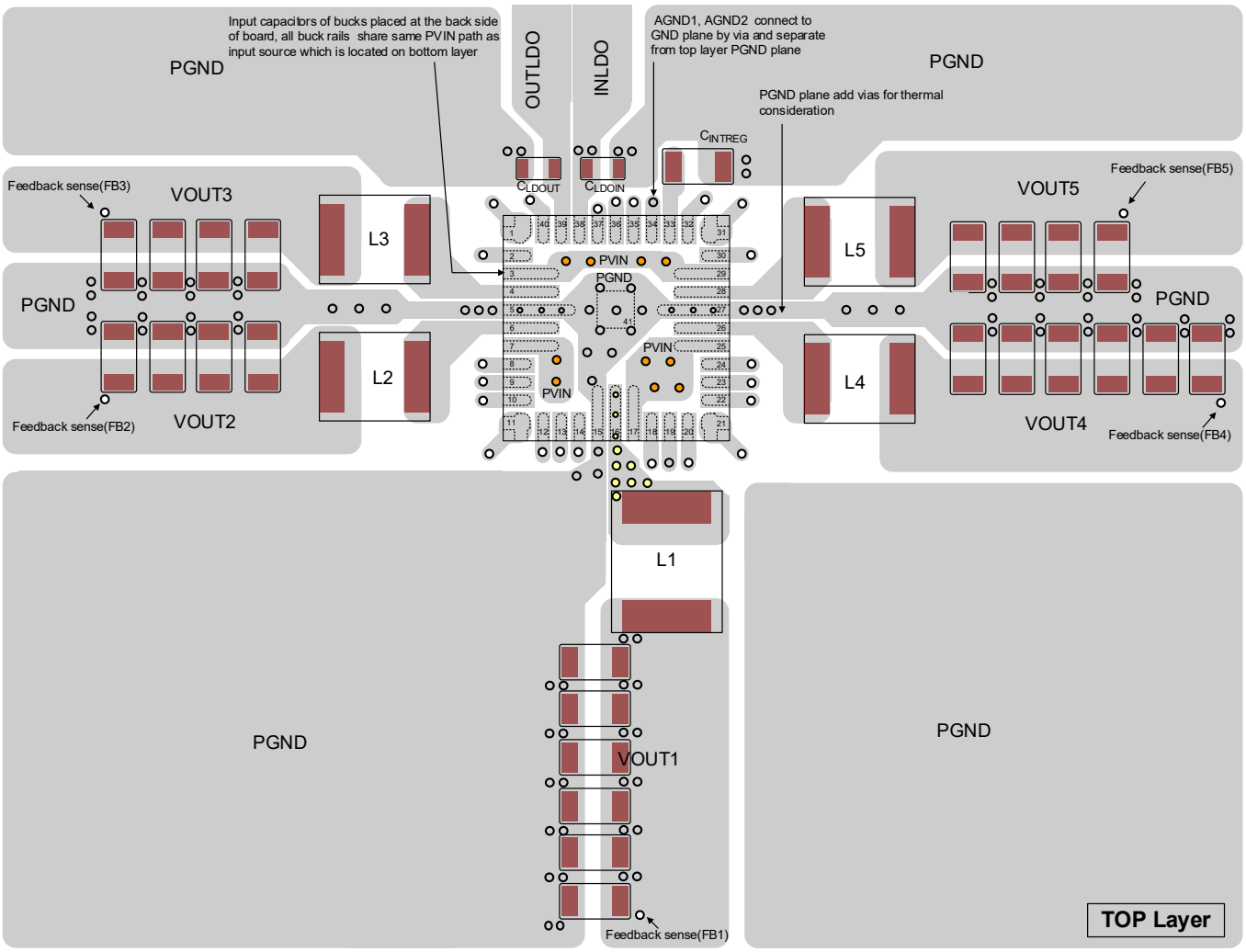


Figure 14. PCB Layout Reference of Option 1 (Top Layer)

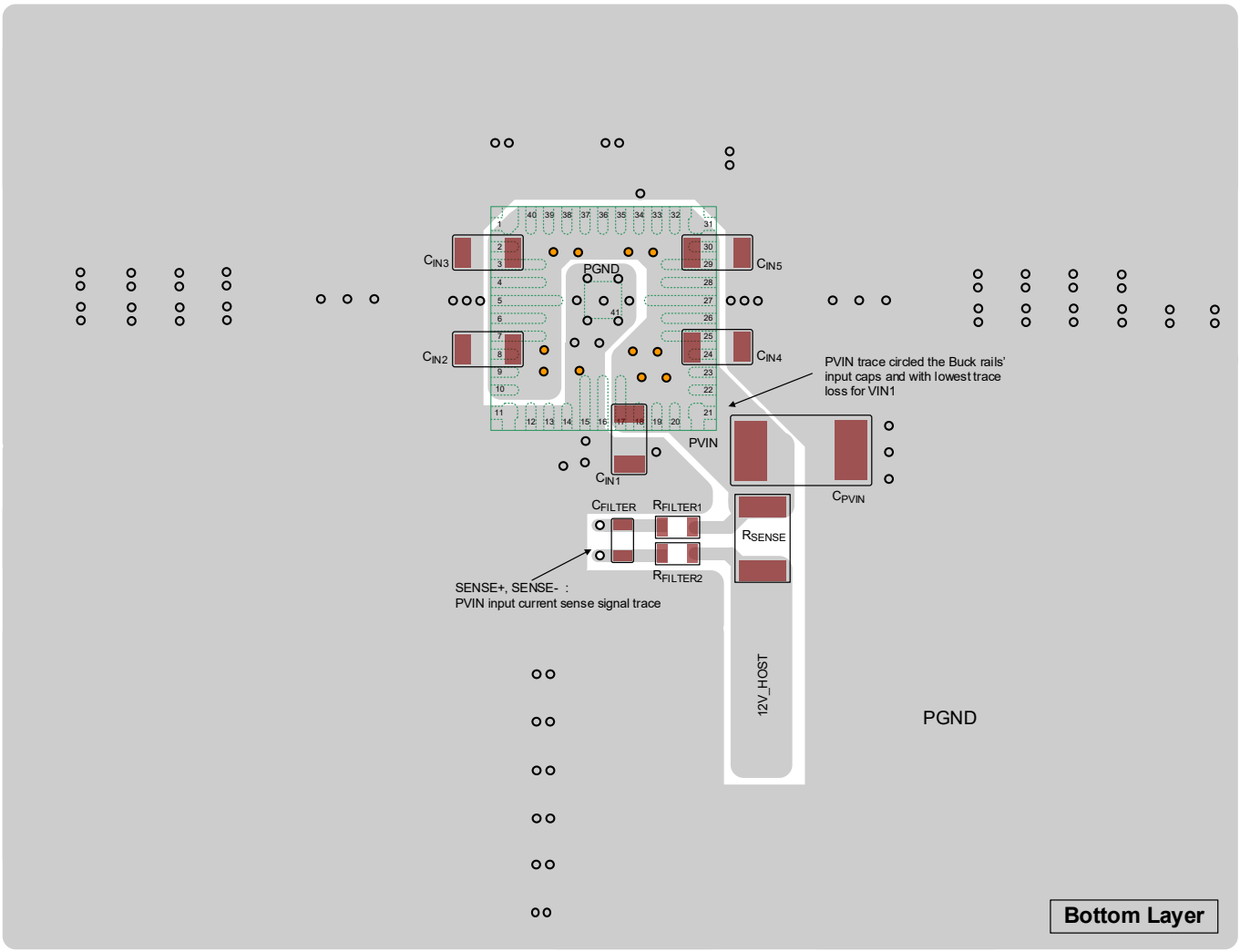


Figure 15. PCB Layout Reference of Option 1 (Bottom Layer, top view)

Layout Reference (Option 2)

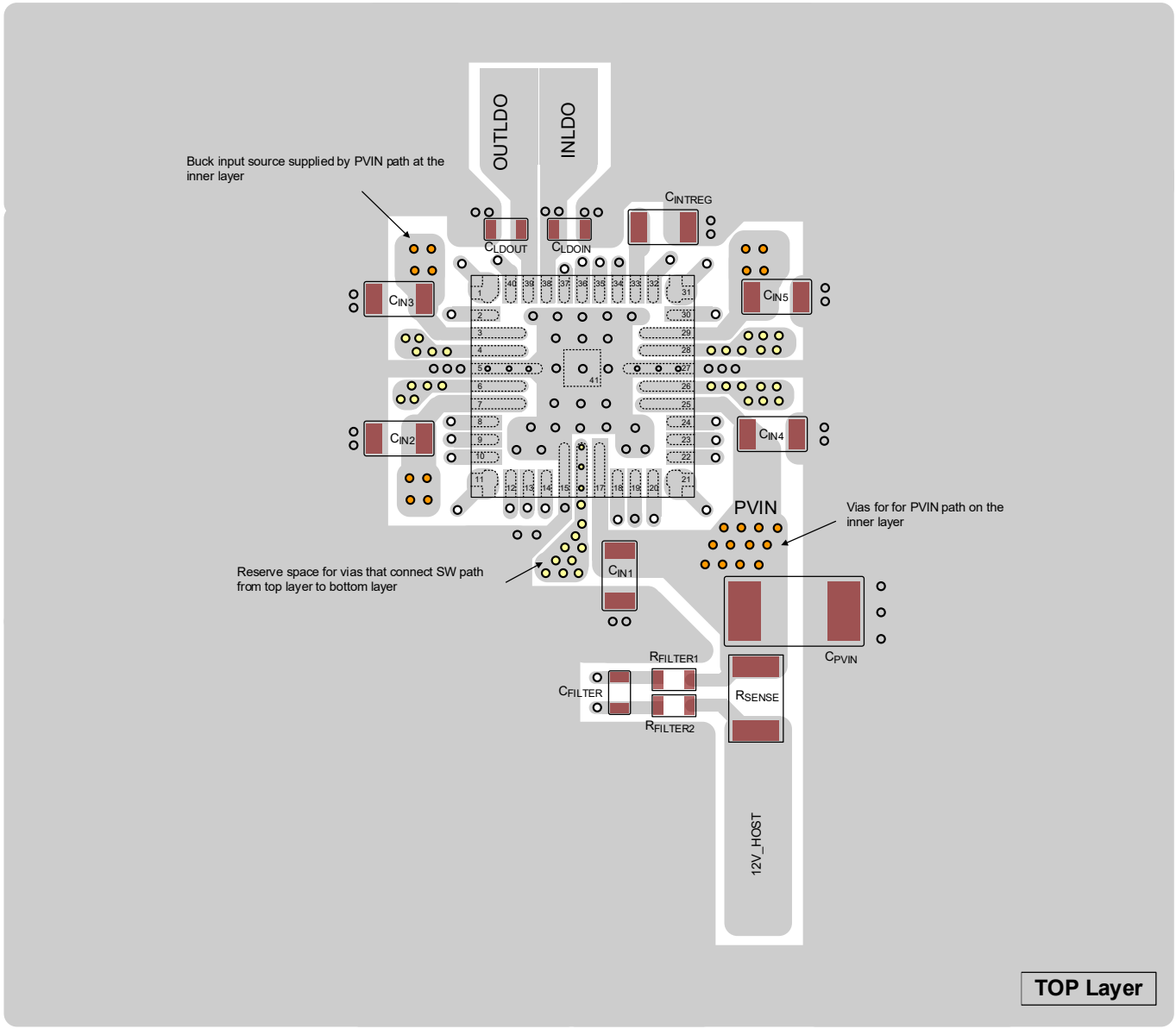


Figure 16. PCB Layout Reference of Option 2 (Top Layer)

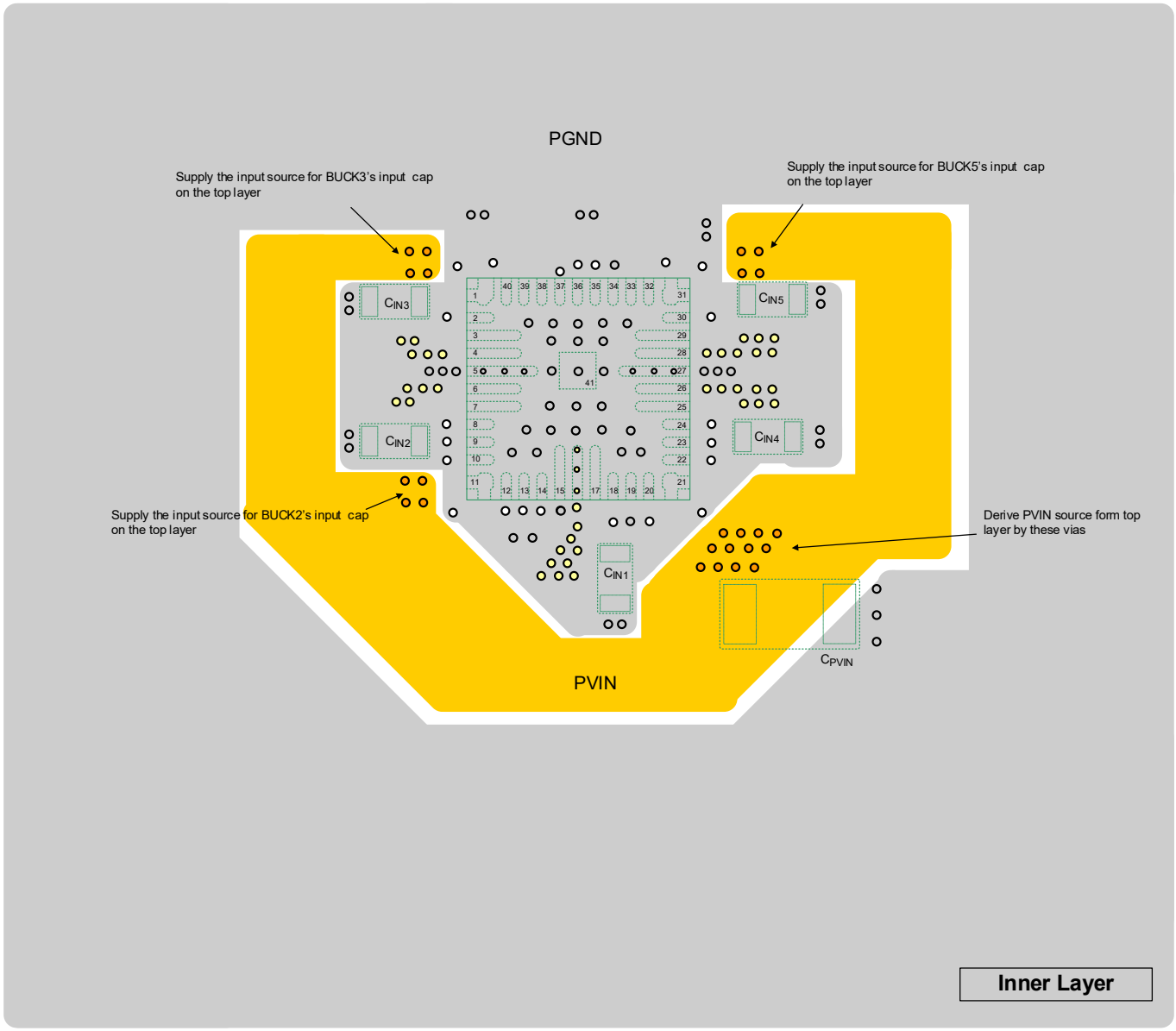


Figure 17. PCB Layout Reference of Option 2 (Inner Layer, top view)

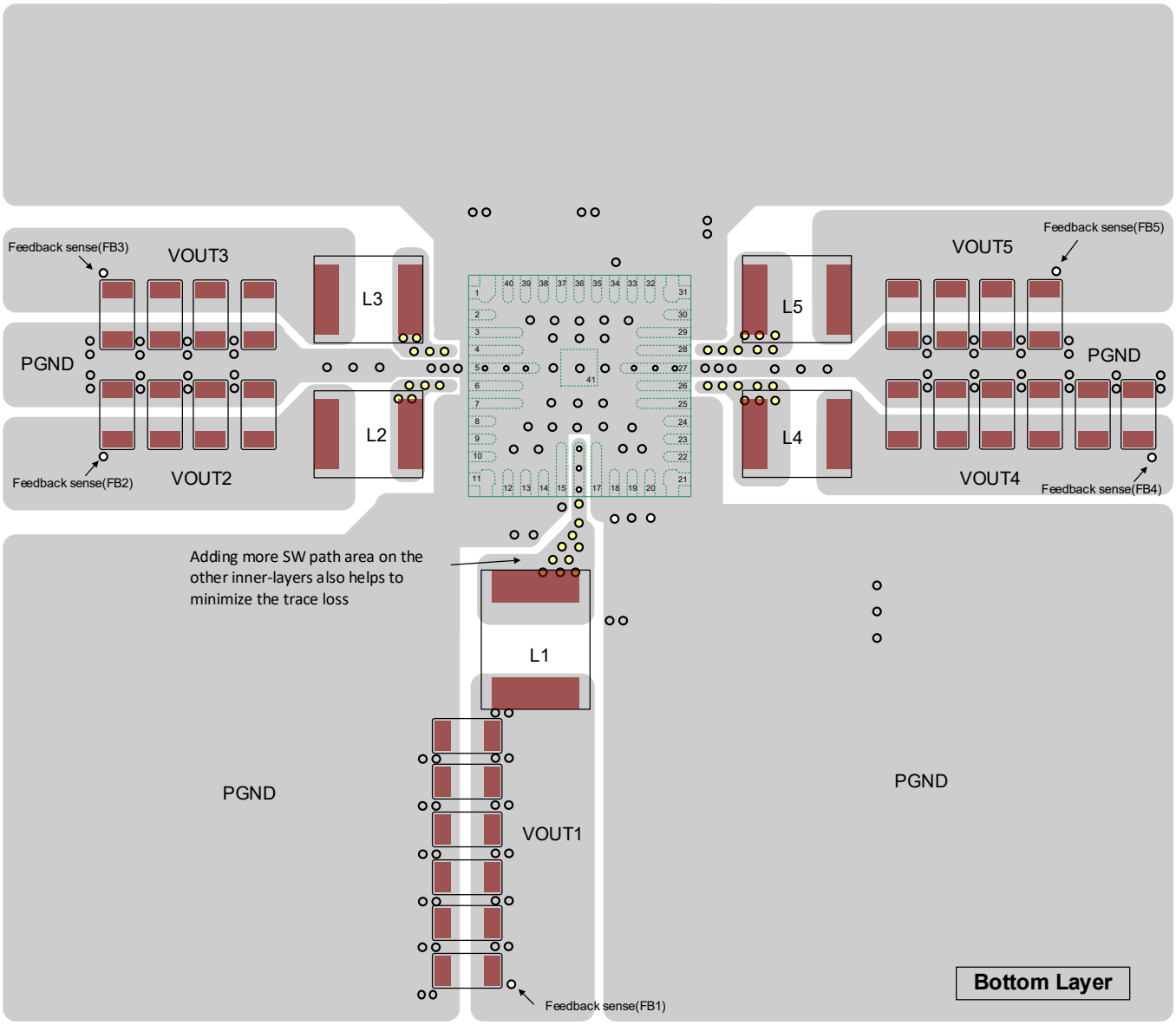


Figure 18. PCB Layout Reference of Option 2 (Bottom Layer, top view)

Register Configuration

The following is a summary of registers. Please see register tables below for more detailed description of their functions. All of the registers are divided into 2 main sections: volatile registers (REG_0x00 to 0x1B), non-volatile registers (REG_0x40 to 0x71). Volatile registers are accessible through I^2C slave bus and are not guaranteed to be valid while input voltage is under VIN UVLO.

Table 7. VENDOR_ID & MTP_REVISION_REG

Address: 0x00 **Description:** This register is used for identifying different NVM settings, future PMICs, etc.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VENDOR_ID		MTP_REVISION					
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:6	VENDOR_ID	Returns the vendor ID. Vendor A =0x1'h Vendor B =0x2'h
5:0	MTP_REVISION	Start with 0x01'h Revision.

Table 8. LOT_SERIAL_ID_REG

Address: 0x01 **Description:** This register is used for identifying Lot Serial ID.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LOT_SERIAL_ID							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	LOT_SERIAL_ID	Returns the lot serial ID. It loads NVM value from REG_0xB1.

Table 9. ASSEMBLY_TIME_CODE_REG

Address: 0x02 **Description:** This register is used for identifying the assembly time.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ASSEMBLY_TIME_CODE							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	ASSEMBLY_TIME_CODE	Returns the assembly time code. It loads NVM value from REG_0xB2.

Table 10. I²C_WRITE_PROTECT_PW_REG

Address: 0x03 **Description:** This register is used for setting password enable access to other registers.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_WRITE_PROTECT_PASSWORD							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:0	I2C_WRITE_PROTECT_PASSWORD	Set A5'h enable access to other registers.

Table 11. INIT_REASON_0_REG

Address: 0x04 **Description:** Indicates the cause for the most recent initialization.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	INIT_REASON				NVM_FAILSAFE_ DISABLE	ERASE_FAULT _NVM	RSVD	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Bits	Name	Description
7:4	INIT_REASON	In situations where the PMIC identifies the cause for the last initialization of the ASIC, the cause will be indicated here. If multi-faults occur at the same time, smaller number has higher priority. 0000b - First power-up 0001b - Initialization from PWRDIS assertion 0010b - Initialization from OVP 0011b - Initialization from UVP 0100b - Initialization from OCP 0101b - Initialization from EREG_PG1 0110b - Initialization from EREG_PG2 0111b - Initialization from EREG_PG3 1000b - Initialization from OTP ... 1111b - Unknown reason
3	NVM_FAILSAFE_DISABLE	Reload Fail-Safe Disable: Debug only (through GUI over I2C) - This bit will disable the fail-safe mechanism to prevent the part from powering up if the NVM bits are not loaded properly. Set to 1b to disable fail-safe mechanism. Set to 1b to enable.
2	ERASE_FAULT_NVM	Set to 1b to erase fault NVM.
1:0	RSVD	Reserved.

Table 12. INIT_REASON_1 _REG

Address: 0x05 **Description:** Indicates whether the signals contribute to the most recent initialization.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	INIT_REASON_VIN	INIT_REASON_Rail1	INIT_REASON_Rail2	INIT_REASON_Rail3	INIT_REASON_Rail4	INIT_REASON_Rail5	INIT_REASON_OUTLDO	RSVD
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
7	INIT_REASON_VIN	Indicates whether the signals contribute to the most recent initialization. 1b = Rail contributes to initialization. 0b = Rail does not contribute to initialization.
6	INIT_REASON_Rail1	
5	INIT_REASON_Rail2	
4	INIT_REASON_Rail3	
3	INIT_REASON_Rail4	
2	INIT_REASON_Rail5	
1	INIT_REASON_OUTLDO	
0	RSVD	Reserved.

Table 13. POWER_GOOD_0 _REG

Address: 0x06 **Description:** Indicates if the selected target is 'power good'.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PGOOD_VIN	PGOOD_Rail1	PGOOD_Rail2	PGOOD_Rail3	PGOOD_Rail4	PGOOD_Rail5	PGOOD_OUTLDO	RSVD
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
7	PGOOD_VIN	Indicates if the selected target is 'power good' 1b = Power good. 0b = Not power good.
6	PGOOD_Rail1	
5	PGOOD_Rail2	
4	PGOOD_Rail3	
3	PGOOD_Rail4	
2	PGOOD_Rail5	
1	PGOOD_OUTLDO	
0	RSVD	Reserved.

Table 14. POWER_GOOD_1 _REG

Address: 0x07
Description: Indicates if the selected target is 'power good'.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					PGOOD_EREG1_PG	PGOOD_EREG2_PG	PGOOD_EREG3_PG
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Bits	Name	Description
7:3	RSVD	Reserved.
2	PGOOD_EREG1_PG	Indicates if the selected target is 'power good' 1b = Power good. 0b = Not power good.
1	PGOOD_EREG2_PG	
0	PGOOD_EREG3_PG	

Table 15. MISC_INT_REG

Address: 0x08
Description: This register indicates miscellaneous interrupts.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP	PWRDIS_ASSERTION	RSVD					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	OTP	Indicates PMIC is shut down by OTP.
6	PWRDIS_ASSERTION	Indicates PMIC is shut down by PWRDIS.
5:0	RSVD	Reserved.

Table 16. OV_INT_REG

Address: 0x09
Description: Interrupt for overvoltage event.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_OV_INT	Rail1_OV_INT	Rail2_OV_INT	Rail3_OV_INT	Rail4_OV_INT	Rail5_OV_INT	OUTLDO_OV_INT	RSVD
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
7	VIN_OV_INT	Indicates if the selected rail is interrupted for overvoltage event 1b = Interrupt for overvoltage event. 0b = Not interrupt for overvoltage event.
6	Rail1_OV_INT	
5	Rail2_OV_INT	
4	Rail3_OV_INT	
3	Rail4_OV_INT	
2	Rail5_OV_INT	
1	OUTLDO_OV_INT	
0	RSVD	Reserved.

Table 17. UV_INT_REG

Address: 0x0A **Description:** Interrupt for undervoltage event.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UV_INT	Rail1_UV_INT	Rail2_UV_INT	Rail3_UV_INT	Rail4_UV_INT	Rail5_UV_INT	OUTLDO_UV_INT	RSVD
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
7	VIN_UV_INT	Indicates if the selected rail is interrupted for undervoltage event 1b = Interrupt for undervoltage event. 0b = Not interrupt for undervoltage event.
6	Rail1_UV_INT	
5	Rail2_UV_INT	
4	Rail3_UV_INT	
3	Rail4_UV_INT	
2	Rail5_UV_INT	
1	OUTLDO_UV_INT	
0	RSVD	Reserved.

Table 18. OCP_INT_REG

Address: 0x0B **Description:** Interrupt for overcurrent protection event.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	Rail1_OCP_INT	Rail2_OCP_INT	Rail3_OCP_INT	Rail4_OCP_INT	Rail5_OCP_INT	RSVD	
Read/Write	R/W	R	R	R	R	R	R	R/W

Bits	Name	Description
7	RSVD	Reserved.
6	Rail1_OCP_INT	Indicates if the selected rail is interrupted for overcurrent protection event 1b = Interrupt for overcurrent protection event 0b = Not interrupt for overcurrent protection event
5	Rail2_OCP_INT	
4	Rail3_OCP_INT	
3	Rail4_OCP_INT	
2	Rail5_OCP_INT	
1:0	RSVD	Reserved.

Table 19. NPG_INT_REG

Address: 0x0C
Description: Interrupt for external PG fail event.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EREG1_PG_INT	EREG2_PG_INT	EREG3_PG_INT	RSVD				
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	EREG1_PG_INT	Indicates if the selected rail is interrupted for PG fail event 1b = Interrupt for PG fail event 0b = Not Interrupt for PG fail event
6	EREG2_PG_INT	
5	EREG3_PG_INT	
4:0	RSVD	Reserved.

Table 20. MISC_CLR_REG

Address: 0x0D
Description: This register clears miscellaneous interrupt indications.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP_CLR	PWRDIS_ASSERTION_CLR	RSVD					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	OTP	Clear miscellaneous interrupt indications.
6	PWRDIS_ASSERTION	
5:0	RSVD	Reserved.

Table 21. OV_CLR_REG

Address: 0x0E
Description: Clear interrupt for overvoltage event.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_OV_CLR	Rail1_OV_CLR	Rail2_OV_CLR	Rail3_OV_CLR	Rail4_OV_CLR	Rail5_OV_CLR	OUTLDO_OV_CLR	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	VIN_OV_CLR	Clear interrupt for overvoltage event.
6	Rail1_OV_CLR	
5	Rail2_OV_CLR	
4	Rail3_OV_CLR	
3	Rail4_OV_CLR	
2	Rail5_OV_CLR	
1	OUTLDO_OV_CLR	
0	RSVD	Reserved.

Table 22. UV_CLR_REG

Address: 0x0F **Description:** Clear interrupt for undervoltage event.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UV_CLR	Rail1_UV_CLR	Rail2_UV_CLR	Rail3_UV_CLR	Rail4_UV_CLR	Rail5_UV_CLR	OUTLDO_UV_CLR	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	VIN_UV_CLR	Clear interrupt for undervoltage event.
6	Rail1_UV_CLR	
5	Rail2_UV_CLR	
4	Rail3_UV_CLR	
3	Rail4_UV_CLR	
2	Rail5_UV_CLR	
1	OUTLDO_UV_CLR	
0	RSVD	Reserved.

Table 23. OCP_CLR_REG

Address: 0x10 **Description:** Clear interrupt for overcurrent protection event.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_OCP_CLR	Rail1_OCP_CLR	Rail2_OCP_CLR	Rail3_OCP_CLR	Rail4_OCP_CLR	Rail5_OCP_CLR	OUTLDO_OCP_CLR	RSVD
Read/Write	R	R	R	R	R	R	R	R/W

Bits	Name	Description
7	VIN	Clear interrupt for overcurrent protection event.
6	Rail1	
5	Rail2	
4	Rail3	
3	Rail4	
2	Rail5	
1	OUTLDO	
0	RSVD	Reserved.

Table 24. NPG_CLR_REG

Address: 0x11 **Description:** Clear interrupt for external PG fail event.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EREG1_PG_CLR	EREG2_PG_CLR	EREG3_PG_CLR	RSVD				
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	EREG1_PG_CLR	Clear interrupt for external PG fail.
6	EREG2_PG_CLR	
5	EREG3_PG_CLR	
4:0	RSVD	Reserved.

Table 25. ADC_IIN_LSB_REG

Address: 0x12 **Description:** Lower eight bits of the ADC results for VIN current measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IIN_LSB							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	IIN_LSB	Clear on read. Lower eight bits of the ADC results for VIN Current measurement. Note: I_{IN} ranges from 0.5A to 1.5A and 0.5A to 6A.

Table 26. ADC_IIN_MSB_REG

Address: 0x13 **Description:** Upper three bits of the ADC results for VIN current measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					IIN_MSB		
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Bits	Name	Description
7:3	RSVD	Reserved.
2:0	IIN_MSB	Clear on read. Upper three bits of the ADC results for VIN Current measurement. Note: I_{IN} ranges from 0.5A to 1.5A and 0.5A to 6A.

Table 27. ADC_VIN_LSB_REG

Address: 0x14 **Description:** Lower eight bits of the ADC results for VIN voltage measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_LSB							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	VIN_LSB	Clear on read. Lower eight bits of the ADC results for VIN voltage measurement. Note: VDC full scale voltage is 16V

Table 28. ADC_VIN_MSB_REG

Address: 0x15 **Description:** Upper three bits of the ADC results for VIN voltage measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					VIN_MSB		
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Bits	Name	Description
7:3	RSVD	Reserved.
2:0	VIN_MSB	Clear on read. Upper three bits of the ADC results for VIN voltage measurement. Note: VDC full scale voltage is 16V

Table 29. ADC_IIN_OFS_REG

Address: 0x16 **Description:** ADC VIN current offset.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IIN_OFFSET							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	IIN_OFFSET	0x16[7] = polarity, 0b for positive offset; 1b is negative. 0x16[6:0] = offset code

Table 30. ADC_VIN_OFS_REG

Address: 0x17 **Description:** ADC VIN voltage offset.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_OFFSET							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VIN_OFFSET	0x17[7] = polarity, 0b for positive offset; 1b is negative. 0x17[6:0] = offset code

Table 31. GPIO_REG_OUT_REG

Address: 0x18 **Description:** GPIO pins buffer output configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG_OUT_PWRDIS_OUT	REG_OUT_EREG1_EN	REG_OUT_EREG2_EN	REG_OUT_EREG3_EN	REG_OUT_EREG1_PG	REG_OUT_EREG2_PG	REG_OUT_EREG3_PG	REG_OUT_EREG_DVS
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	REG_OUT_PWRDIS_OUT	Enable register buffer output function for specific GPIO pin.
6	REG_OUT_EREG1_EN	
5	REG_OUT_EREG2_EN	
4	REG_OUT_EREG3_EN	
3	REG_OUT_EREG1_PG	
2	REG_OUT_EREG2_PG	
1	REG_OUT_EREG3_PG	
0	REG_OUT_EREG_DVS	

Table 32. ADC_IIN_LSB_REALTIME

Address: 0x19 **Description:** Lower eight bits of the real-time ADC results for VIN current measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IIN_LSB_REALTIME							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	IIN_LSB_REALTIME	Clear on read. Real-time ADC_LSB result for IIN.

Table 33. ADC_IIN_MSB_REALTIME

Address: 0x1A **Description:** Upper three bits of the real-time ADC results for VIN current measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					IIN_MSB_REALTIME		
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Bits	Name	Description
7:3	RSVD	Reserved.
2:0	IIN_MSB_REALTIME	Clear on read. Real-time ADC_MSB result for IIN.

Table 34. ADC_VIN_LSB_REALTIME

Address: 0x1B **Description:** Lower eight bits of the real-time ADC results for VIN voltage measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_LSB_REALTIME							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	VIN_LSB_REALTIME	Clear on read. Real-time ADC_LSB result for VIN.

Table 35. ADC_VIN_MSB_REALTIME

Address: 0x1C **Description:** Upper three bits of the real-time ADC results for VIN voltage measurement.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					VIN_MSB_REALTIME		
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R

Bits	Name	Description
7:3	RSVD	Reserved.
2:0	VIN_MSB_REALTIME	Clear on read. Real-time ADC_MSB result for VIN.

Table 36. TESTMODE_UNLOCK_0

Address: 0x30 **Description:** Testmode unlock 0.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TM_KEY_0							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:0	TM_KEY_0	Test mode unlock register. Must be written to first, before TESTMODE_UNLOCK_1. Write 62h as first unlock key. An Invalid key will exit test mode. Write FFh to exit both user and vendor testmode..

Table 37. TESTMODE_UNLOCK_1

Address: 0x31 **Description:** Testmode unlock 1.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TM_KEY_1							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:0	TM_KEY_1	Test mode unlock register. Must be written to after TESTMODE_UNLOCK_0. Write 86h as second unlock key. An Invalid key will exit test mode.

Table 38. TESTMODE_UNLOCK_2

Address: 0x32 **Description:** Testmode unlock 2.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TM_KEY_2							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:0	TM_KEY_2	Write 43h to unlock REG_0x46[2:1].

Table 39. NVM_CTRL (LOCKED)

Address: 0x33 **Description:** NVM control register.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PROGRAM_USER_NVM	PROGRAM_VENDOR_NVM	RELOAD_USER_NVM	RELOAD_VENDOR_NVM	RELOAD_ALL_NVM	RSVD		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	PROGRAM_USER_NVM	Program user NVM.
6	PROGRAM_VENDOR_NVM	Program vendor NVM.
5	RELOAD_USER_NVM	Reload user NVM only.
4	RELOAD_VENDOR_NVM	Reload vendor NVM only.
3	RELOAD_ALL_NVM	Reload all NVM.
2:0	RSVD	Reserved

Table 40. SYSTEM_CFG_0_REG

Address: 0x40 **Description:** This register sets system configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PWRDIS_POLARITY	PWRDIS_IGNORE	VOUT1_RESIDUE_CHK_IGNORE	VOUT2_RESIDUE_CHK_IGNORE	VOUT3_RESIDUE_CHK_IGNORE	VOUT4_RESIDUE_CHK_IGNORE	VOUT5_RESIDUE_CHK_IGNORE	OUTLDO_RESIDUE_CHK_IGNORE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	PWRDIS_POLARITY	Sets polarity for PWRDIS. 0b = Active high (voltage high = disable) 1b = Active low (voltage low = disable)
6	PWRDIS_IGNORE	Set to 1b to ignore PWRDIS pin.
5	VOUT1_RESIDUE_CHK_IGNORE	Set to 1b to ignore specific VOUT<100mV signal.
4	VOUT2_RESIDUE_CHK_IGNORE	
3	VOUT3_RESIDUE_CHK_IGNORE	
2	VOUT4_RESIDUE_CHK_IGNORE	
1	VOUT5_RESIDUE_CHK_IGNORE	
0	OUTLDO_RESIDUE_CHK_IGNORE	

Table 41. SYSTEM_CFG_1_REG

Address: 0x41
Description: This register sets system configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ISEN_GAIN			FAULT_RESPONSE	POR_EN_DELAY			OTP_DISABLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:5	ISEN_GAIN	Set ISEN gain. 000b = 5x 001b = 10x 010b = 15x 011b = 20x 100b = 25x 101b = 30x 110b = 35x 111b = 40x
4	FAULT_RESPONSE	0b = 5 hiccups 1b = latched
3:1	POR_EN_DELAY	Time from last rail finishing its ramp, to RST_L being released. 000b = 0ms 001b = 0.5ms 010b = 1ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
0	OTP_DISABLE	Disable OTP. 0b = Enable Protection. 1b = Disable Protection

Table 42. SYSTEM_CFG_2_REG

Address: 0x42 **Description:** This register sets system configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OTP_THRESHOLD		AUTO_ENABLE_TIME			AUTO_SHUTDOWN_TIME		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7:6	OTP_THRESHOLD	OTP threshold setting, hysteresis is fixed 20°C. 00b = 115°C 01b = 125°C 10b = 135°C 11b = 145°C
5:3	AUTO_ENABLE_TIME	Delay time for SEQUENCE_UP state. Range from 0ms to 10ms. 000b = 50μs 001b = 0.5ms 010b = 1ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
2:0	AUTO_SHUTDOWN_TIME	PWRDIS countdown timer, range from 51.2ms to 10.24s. 000b = 51.2ms 001b = 102.4ms 010b = 307.2ms 011b = 614.4ms 100b = 1.28s 101b = 2.56s 110b = 5.12s 111b = 10.24s

Table 43. COMM_CFG_REG

Address: 0x43
Description: This register sets common configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	I2C_VOLTAGE_MODE		I2C_PULLUP_RESISTANCE		I2C_ADDR		PWRDIS_IN_VOLTAGE	PWRDIS_ACK_VOLTAGE
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bits	Name	Description
7:6	I2C_VOLTAGE_MODE	Sets I2C operating voltage. 00b = low voltage, 1.2V 01b = high voltage, 1.8V 1xb = external pull-up voltage, 3.3V
5:4	I2C_PULLUP_RESISTANCE	Sets internal pull-up resistance, each setting has two levels according to COMM_CFG.I2C_VOLTAGE_MODE. 00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ
3:2	I2C_ADDR	Configure the I2C Slave Address: 00b = 0x68h 01b = 0x69h 10b = 0x6Ah 11b = 0x6Bh
1	PWRDIS_IN_VOLTAGE	0b = 1.8V 1b = 3.3V
0	PWRDIS_ACK_VOLTAGE	0b = 1.2V 1b = 1.8V

Table 44. RAIL_DISABLE _REG

Address: 0x44 **Description:** This register sets rails enable or disable.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DISABLE _RAIL1	DISABLE_ RAIL2	DISABLE _RAIL3	DISABLE _RAIL4	DISABLE _RAIL5	DISABLE _LDO	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	DISABLE_RAIL1	0b = ON 1b = OFF
6	DISABLE_RAIL2	0b = ON 1b = OFF
5	DISABLE_RAIL3	0b = ON 1b = OFF
4	DISABLE_RAIL4	0b = ON 1b = OFF
3	DISABLE_RAIL5	0b = ON 1b = OFF
2	DISABLE_LDO	0b = ON 1b = OFF
1:0	RSVD	Reserved

Table 45. EREG_DISABLE _REG

Address: 0x45 **Description:** This register sets EREGX_EN enable or disable.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DISABLE_ EREG1_EN	DISABLE_ EREG2_EN	DISABLE_ EREG3_EN	RSVD				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	DISABLE_EREG1_EN	Only affect digital output signal, DO_EREG1_EN. 0b = ON 1b = OFF
6	DISABLE_EREG2_EN	Only affect digital output signal, DO_EREG2_EN. 0b = ON 1b = OFF
5	DISABLE_EREG3_EN	Only affect digital output signal, DO_EREG3_EN. 0b = ON 1b = OFF
4:0	RSVD	Reserved.

Table 46. RAIL_MODE_CFG_REG

Address: 0x46
Description: This register is used for rail mode setting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RAIL1_ FCCM	RAIL2_ FCCM	RAIL3_ FCCM	RAIL4_ FCCM	RAIL5_ FCCM	RAIL23_ 2PH_EN	RAIL45_ 2PH_EN	RSVD
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RAIL1_FCCM	Mode selection for rail1. 0b = Auto pulse skipping mode (PSM) 1b = Force pulse width modulation (FCCM)
6	RAIL2_FCCM	Mode selection for rail2. 0b = Auto pulse skipping mode (PSM) 1b = Force pulse width modulation (FCCM)
5	RAIL3_FCCM	Mode selection for rail3. 0b = Auto pulse skipping mode (PSM) 1b = Force pulse width modulation (FCCM)
4	RAIL4_FCCM	Mode selection for rail4. 0b = Auto pulse skipping mode (PSM) 1b = Force pulse width modulation (FCCM)
3	RAIL5_FCCM	Mode selection for rail5. 0b = Auto pulse skipping mode (PSM) 1b = Force pulse width modulation (FCCM)
2	RAIL23_2PH_EN	2-phase enable for rail2 & rail3. LOCKED by TM_KEY_2. 0b = single phase 1b = two phase, should set two rails in the same mode.
1	RAIL45_2PH_EN	2-phase enable for rail4 & rail5. LOCKED by TM_KEY_2. 0b = single phase 1b = two phase, should set two rails in the same mode.
0	RSVD	Reserved.

Table 47. SOFT_START_0_REG

Address: 0x47
Description: This register is used for Rail1 and Rail2 soft-start setting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT_START_TIME_RAIL1			SOFT_START_TIME_RAIL2			RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:5	SOFT_START_TIME_RAIL1	Soft-start setting for Rail1: 000b = 0.5ms 001b = 1ms 010b = 1.5ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
4:2	SOFT_START_TIME_RAIL2	Soft-start setting for Rail2: 000b = 0.5ms 001b = 1ms 010b = 1.5ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
1:0	RSVD	Reserved.

Table 48. SOFT_START_1_REG

Address: 0x48
Description: This register is used for Rail4 and Rail4 soft-start setting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT_START_TIME_RAIL3			SOFT_START_TIME_RAIL4			RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:5	SOFT_START_TIME_RAIL3	Soft-start setting for Rail3: 000b = 0.5ms 001b = 1ms 010b = 1.5ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
4:2	SOFT_START_TIME_RAIL4	Soft-start setting for Rail4: 000b = 0.5ms 001b = 1ms 010b = 1.5ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
1:0	RSVD	Reserved.

Table 49. SOFT_START_2_REG

Address: 0x49
Description: This register is used for Rail5 and LDO soft-start setting.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT_START_TIME_RAIL5			SOFT_START_TIME_LDO		RSVD		
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:5	SOFT_START_TIME_RAIL5	Soft-start setting for Rail5: 000b = 0.5ms 001b = 1ms 010b = 1.5ms 011b = 2ms 100b = 4ms 101b = 6ms 110b = 8ms 111b = 10ms
4:3	SOFT_START_TIME_LDO	Soft-start setting for LDO: 00b = 100μs 01b = 200μs 10b = 500μs 11b = 1ms
2:0	RSVD	Reserved.

Table 50. EN_TIME_RAIL1_REG

Address: 0x4A
Description: This register sets the time from system power good to SEQUENCE_UP-STATE.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_RAIL1						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_RAIL1	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 51. EN_TIME_RAIL2_REG

Address: 0x4B **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_RAIL2						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_RAIL2	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to 127ms Granularity = 1ms

Table 52. EN_TIME_RAIL3_REG

Address: 0x4C **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_RAIL3						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_RAIL3	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 53. EN_TIME_RAIL4_REG

Address: 0x4D **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_RAIL4						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_RAIL4	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 54. EN_TIME_RAIL5_REG

Address: 0x4E **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_RAIL5						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_RAIL5	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 55. EN_TIME_LDO_REG

Address: 0x4F **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_LDO						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_LDO	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 56. EN_TIME_EREG1_REG

Address: 0x50 **Description:** This register sets the time from system power good to SEQUENCE_UP-STATE.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_EREG1						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_EREG1	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to127ms Granularity = 1ms

Table 57. EN_TIME_EREG2_REG

Address: 0x51
Description: This register sets the time from system power good to SEQUENCE_UP-STATE.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_EREG2						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_EREG2	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to 127ms Granularity = 1ms

Table 58. EN_TIME_EREG3_REG

Address: 0x52
Description: This register sets the time from system power good to SEQUENCE_UP-STATE.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	EN_TIME_EREG3						
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved.
6:0	EN_TIME_EREG3	Time from system power good to SEQUENCE_UP-STATE. Range = 0ms to 127ms Granularity = 1ms

Table 59. SOFT_STOP_0_REG

Address: 0x53
Description: This register is used for soft-stop setting for Rail1 to Rail4.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT_STOP_RDIS_RAIL1		SOFT_STOP_RDIS_RAIL2		SOFT_STOP_RDIS_RAIL3		SOFT_STOP_RDIS_RAIL4	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	SOFT_STOP_RDIS_RAIL1	Soft-stop setting for Rail1: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z
5:4	SOFT_STOP_RDIS_RAIL2	Soft-stop setting for Rail2: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z
3:2	SOFT_STOP_RDIS_RAIL3	Soft-stop setting for Rail3: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z
1:0	SOFT_STOP_RDIS_RAIL4	Soft-stop setting for Rail4: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z

Table 60. SOFT_STOP_1_REG

Address: 0x54 **Description:** This register is used for soft-stop setting for Rail5 and LDO.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT_STOP_RDIS_RAIL5		SOFT_STOP_RDIS_LDO		RSVD			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	SOFT_STOP_RDIS_RAIL5	Soft-stop setting for Rail5: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z
5:4	SOFT_STOP_RDIS_LDO	Soft-stop setting for LDO: 00b = 10Ω bleed resistor 01b = 20Ω bleed resistor 10b = 50Ω bleed resistor 11b = High-Z
3:0	RSVD	Reserved

Table 61. ADC_CFG_REG

Address: 0x55 **Description:** ADC configuration register.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ENABLE_IVIN	ENABLE_VIN	AVG_FILTER		IIN_LIM_FREERUN	RSVD		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	ENABLE_IVIN	If disabled, data in ADC_ACCUM* registers will be cleared. Re-write this byte will restart average counter and clear ADC data.
6	ENABLE_VIN	If disabled, data in ADC_ACCUM* registers will be cleared. Re-write this byte will restart average counter and clear ADC data.
5:4	AVG_FILTER	Average filter coefficient for ADC, defined as number of samples. 00b = 1ms 01b = 2ms 10b = 4ms 11b = 5ms
3	IIN_LIM_FREERUN	0b: IIN_LIM latch 1b: IIN_LIM free run
2:0	RSVD	Reserved.

Table 62. VOUT_CFG_RAIL1_REG

Address: 0x56 **Description:** This register is used for Rail1 VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VID_RAIL1							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VID_RAIL1	**Rail1 output voltage:** For REG_0x76[7]=0 (FB_ratio_Rail1 = 100%) 0x56[7:0] = 00000000b: V_{OUT1} = 0.3V 0x56[7:0] = 00000001b: V_{OUT1} = 0.31V … 0x56[7:0] = 10110100b: V_{OUT1} = 2.1V For REG_0x76[7]=1 (FB_ratio_Rail1 = 50%) 0x56[7:0] = 00000000b: V_{OUT1} = 0.3V 0x56[7:0] = 00000001b: V_{OUT1} = 0.32V … 0x56[7:0] = 10011110b: V_{OUT1} = 3.46V

Table 63. VOUT_CFG_RAIL2_REG

Address: 0x57 **Description:** This register is used for Rail2 VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VID_RAIL2							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VID_RAIL2	**Rail2 output voltage:** For REG_0x76[6]=0 (FB_ratio_Rail2 = 100%) 0x57[7:0] = 00000000b: V_{OUT2} = 0.3V 0x57[7:0] = 00000001b: V_{OUT2} = 0.31V … 0x57[7:0] = 10110100b: V_{OUT2} = 2.1V For REG_0x76[6]=1 (FB_ratio_Rail2 = 50%) 0x57[7:0] = 00000000b: V_{OUT2} = 0.3V 0x57[7:0] = 00000001b: V_{OUT2} = 0.32V … 0x57[7:0] = 10011110b: V_{OUT2} = 3.46V

Table 64. VOUT_CFG_RAIL3_REG

Address: 0x58 **Description:** This register is used for Rail3 VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VID_RAIL3							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VID_RAIL3	**Rail3 output voltage:** For REG_0x76[5]=0 (FB_ratio_Rail3 = 100%) 0x57[7:0] = 00000000b: V_{OUT3} = 0.3V 0x57[7:0] = 00000001b: V_{OUT3} = 0.31V … 0x57[7:0] = 10110100b: V_{OUT3} = 2.1V For REG_0x76[5]=1 (FB_ratio_Rail3 = 50%) 0x57[7:0] = 00000000b: V_{OUT3} = 0.3V 0x57[7:0] = 00000001b: V_{OUT3} = 0.32V … 0x57[7:0] = 10011110b: V_{OUT3} = 3.46V

Table 65. VOUT_CFG_RAIL4_REG

Address: 0x59 **Description:** This register is used for Rail4 VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VID_RAIL4							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VID_RAIL4	**Rail4 output voltage:** For REG_0x76[4]=0 (FB_ratio_Rail4 = 100%) 0x57[7:0] = 00000000b: V_{OUT4} = 0.3V 0x57[7:0] = 00000001b: V_{OUT4} = 0.31V … 0x57[7:0] = 10110100b: V_{OUT4} = 2.1V For REG_0x76[4]=1 (FB_ratio_Rail4 = 50%) 0x57[7:0] = 00000000b: V_{OUT4} = 0.3V 0x57[7:0] = 00000001b: V_{OUT4} = 0.32V … 0x57[7:0] = 10011110b: V_{OUT4} = 3.46V

Table 66. VOUT_CFG_RAIL5_REG

Address: 0x5A **Description:** This register is used for Rail5 VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VID_RAIL5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	VID_RAIL5	**Rail5 output voltage:** For REG_0x76[3]=0 (FB_ratio_Rail5 = 100%) 0x57[7:0] = 00000000b: V_{OUT5} = 0.3V 0x57[7:0] = 00000001b: V_{OUT5} = 0.31V … 0x57[7:0] = 10110100b: V_{OUT5} = 2.1V For REG_0x76[3]=1 (FB_ratio_Rail5 = 50%) 0x57[7:0] = 00000000b: V_{OUT5} = 0.3V 0x57[7:0] = 00000001b: V_{OUT5} = 0.32V … 0x57[7:0] = 10011110b: V_{OUT5} = 3.46V

Table 67. VOUT_CFG_LDO_REG

Address: 0x5B **Description:** This register is used for LDO VID range.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD		VID_LDO					
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	RSVD	Reserved.
5:0	VID_LDO	**LDO output supply voltage:** V_{OUTLDO} = 0.6V to 2.65V, 50mV/step. 0x5B[5:0] = 000110b: V_{OUTLDO} = 0.6V 0x5B[5:0] = 000111b: V_{OUTLDO} = 0.65V … 0x5B[5:0] = 101111b: V_{OUTLDO} = 2.65V

Table 68. OC_CFG_0_REG

Address: 0x5C **Description:** This register sets overcurrent limit level of rails.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCL_RAIL1		OCP_N_CYCLES_RAIL1	OCL_RAIL2		OCP_N_CYCLES_RAIL2	OCL_RAIL3	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	OCL_RAIL1	00b = 7.5A 01b = 8A 10b = 8.5A 11b = 9A
5	OCP_N_CYCLES_RAIL1	0b = 16 continuous cycles 1b = Disable OCP
4:3	OCL_RAIL2	00b = 2.5A 01b = 3A 10b = 3.5A 11b = 4A
2	OCP_N_CYCLES_RAIL2	0b = 16 continuous cycles 1b = Disable OCP
1:0	OCL_RAIL3	00b = 2.5A 01b = 3A 10b = 3.5A 11b = 4A

Table 69. OC_CFG_1_REG

Address: 0x5D
Description: This register sets overcurrent limit level of rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCP_N_CYCLES_RAIL3	OCL_RAIL4		OCP_N_CYCLES_RAIL4	OCL_RAIL5		OCP_N_CYCLES_RAIL5	OCL_LDO
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	OCP_N_CYCLES_RAIL3	0b = 16 continuous cycles 1b = Disable OCP
6:5	OCL_RAIL4	00b = 3.5A 01b = 4A 10b = 4.5A 11b = 5A
4	OCP_N_CYCLES_RAIL4	0b = 16 continuous cycles 1b = Disable OCP
3:2	OCL_RAIL5	00b = 3.5A 01b = 4A 10b = 4.5A DO NOT SET TO 11b
1	OCP_N_CYCLES_RAIL5	0b = 16 continuous cycles 1b = Disable OCP
0	OCL_LDO	0b = 1A 1b = 1.5A

Table 70. FSW_DVID_CFG_0_REG

Address: 0x5E
Description: This register sets frequency and DVID slew rate of buck rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSW_RAIL1		DVID_SLEW_RATE_RAIL1		FSW_RAIL2		DVID_SLEW_RATE_RAIL2	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	FSW_RAIL1	00b = 600kHz 01b = 800kHz 10b = 1MHz 11b = 1.2MHz
5:4	DVID_SLEW_RATE_RAIL1	Related with REG_0x76[7] FB ratio setting. If 0x76[7] = 0b(FB_ratio_Rail1 = 100%), 00b = 0.25mV/µs 01b = 0.5mV/µs 10b = 1mV/µs 11b = 5mV/µs If 0x76[7] = 1b(FB_ratio_Rail1 = 50%), 00b = 0.5mV/µs 01b = 1mV/µs 10b = 2mV/µs 11b = 10mV/µs
3:2	FSW_RAIL2	00b = 600kHz 01b = 800kHz 10b = 1MHz 11b = 1.2MHz
1:0	DVID_SLEW_RATE_RAIL2	Related with REG_0x76[6] FB ratio setting. If 0x76[6] = 0b(FB_ratio_Rail2 = 100%) 00b = 0.25mV/µs 01b = 0.5mV/µs 10b = 1mV/µs 11b = 5mV/µs If 0x76[6] = 1b(FB_ratio_Rail2 = 50%) 00b = 0.5mV/µs 01b = 1mV/µs 10b = 2mV/µs 11b = 10mV/µs

Table 71. FSW_DVID_CFG_1_REG

Address: 0x5F
Description: This register sets frequency and DVID slew rate of buck rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSW_RAIL3		DVID_SLEW_RATE_RAIL3		FSW_RAIL4		DVID_SLEW_RATE_RAIL4	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	FSW_RAIL3	00b = 600kHz 01b = 800kHz 10b = 1MHz 11b = 1.2MHz
5:4	DVID_SLEW_RATE_RAIL3	Related with REG_0x76[5] FB ratio setting. If 0x76[5] = 0b(FB_ratio_Rail3 = 100%), 00b = 0.25mV/μs 01b = 0.5mV/μs 10b = 1mV/μs 11b = 5mV/μs If 0x76[5] = 1b(FB_ratio_Rail3 = 50%), 00b = 0.5mV/μs 01b = 1mV/μs 10b = 2mV/μs 11b = 10mV/μs
3:2	FSW_RAIL4	00b = 600kHz 01b = 800kHz 10b = 1MHz 11b = 1.2MHz
1:0	DVID_SLEW_RATE_RAIL4	Related with REG_0x76[4] FB ratio setting. If 0x76[4] = 0b(FB_ratio_Rail4 = 100%) 00b = 0.25mV/μs 01b = 0.5mV/μs 10b = 1mV/μs 11b = 5mV/μs If 0x76[4] = 1b(FB_ratio_Rail4 = 50%) 00b = 0.5mV/μs 01b = 1mV/μs 10b = 2mV/μs 11b = 10mV/μs

Table 72. FSW_DVID_CFG_2_REG

Address: 0x60 **Description:** This register sets frequency and DVID slew rate of buck rails.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSW_RAIL5		DVID_SLEW_RATE_RAIL5		RSVD			
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:6	FSW_RAIL5	00b = 600kHz 01b = 800kHz 10b = 1MHz 11b = 1.2MHz
5:4	DVID_SLEW_RATE_RAIL5	Related with REG_0x76[4] FB ratio setting. If 0x76[3] = 0b(FB_ratio_Rail5 = 100%) 00b = 0.25mV/μs 01b = 0.5mV/μs 10b = 1mV/μs 11b = 5mV/μs If 0x76[3] = 1b(FB_ratio_Rail5 = 50%) 00b = 0.5mV/μs 01b = 1mV/μs 10b = 2mV/μs 11b = 10mV/μs
3:0	RSVD	Reserved.

Table 73. OV_CFG_0_REG

Address: 0x61
Description: This register sets overvoltage level of rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OV_SELECTION_RAIL1	OV_SELECTION_RAIL2	OV_SELECTION_RAIL3	OV_SELECTION_RAIL4	OV_SELECTION_RAIL5	OV_SELECTION_OUTLDO	OV_SELECTION_VIN	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	OV_SELECTION_RAIL1	0b = 110% 1b = 115% Note: If 0x7B[7] = 1b, regardless of whether 0x61[7] = 1b or 0b, the Rail1 overvoltage (OV) level will be set to 120%.
6	OV_SELECTION_RAIL2	0b = 110% 1b = 115% Note: If 0x7B[6] = 1b, regardless of whether 0x61[6] = 1b or 0b, the Rail2 overvoltage (OV) level will be set to 120%.
5	OV_SELECTION_RAIL3	0b = 110% 1b = 115% Note: If 0x7B[5] = 1b, regardless of whether 0x61[5] = 1b or 0b, the Rail3 overvoltage (OV) level will be set to 120%.
4	OV_SELECTION_RAIL4	0b = 110% 1b = 115% Note: If 0x7B[4] = 1b, regardless of whether 0x61[4] = 1b or 0b, the Rail4 overvoltage (OV) level will be set to 120%.
3	OV_SELECTION_RAIL5	0b = 110% 1b = 115% Note: If 0x7B[3] = 1b, regardless of whether 0x61[3] = 1b or 0b, the Rail5 overvoltage (OV) level will be set to 120%.
2	OV_SELECTION_OUTLDO	0b = 110% 1b = 115% Note: If 0x7B[2] = 1b, regardless of whether 0x61[2] = 1b or 0b, the LDO overvoltage (OV) level will be set to 120%.
1:0	OV_SELECTION_VIN	00b = 14V 01b = 15V 10b = 16V 11b = 17V

Table 74. UV_CFG_0_REG

Address: 0x62
Description: This register sets undervoltage level of rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	UV_SELECTION_RAIL1	UV_SELECTION_RAIL2	UV_SELECTION_RAIL3	UV_SELECTION_RAIL4	UV_SELECTION_RAIL5	UV_SELECTION_OUTLDO	UV_SELECTION_VIN	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	UV_SELECTION_RAIL1	0b = 90% 1b = 85% Note: If 0x7C[7] = 1b, regardless of whether 0x61[7] = 1b or 0b, the Rail1 undervoltage (UV) level will be set to 80%.
6	UV_SELECTION_RAIL2	0b = 90% 1b = 85% Note: If 0x7C[6] = 1b, regardless of whether 0x61[6] = 1b or 0b, the Rail2 undervoltage (UV) level will be set to 80%.
5	UV_SELECTION_RAIL3	0b = 90% 1b = 85% Note: If 0x7C[5] = 1b, regardless of whether 0x61[5] = 1b or 0b, the Rail3 undervoltage (UV) level will be set to 80%.
4	UV_SELECTION_RAIL4	0b = 90% 1b = 85% Note: If 0x7C[4] = 1b, regardless of whether 0x61[4] = 1b or 0b, the Rail4 undervoltage (UV) level will be set to 80%.
3	UV_SELECTION_RAIL5	0b = 90% 1b = 85% Note: If 0x7C[3] = 1b, regardless of whether 0x61[3] = 1b or 0b, the Rail5 undervoltage (UV) level will be set to 80%.
2	UV_SELECTION_OUTLDO	0b = 90% 1b = 85% Note: If 0x7C[2] = 1b, regardless of whether 0x61[2] = 1b or 0b, the LDO undervoltage (UV) level will be set to 80%.
1:0	UV_SELECTION_VIN	00b = 3.8V 01b = 4.3V 10b = 6V 11b = 8V

Table 75. DEGLITCH_TIME_CFG_REG

Address: 0x63
Description: This register sets both OVP and UVP deglitch time.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FAULT_DEGLITCH_TIME_VIN	FAULT_DEGLITCH_TIME_OUTLDO	FAULT_DEGLITCH_TIME_RAIL	DEGLITCH_TIME_PWRDIS_IN_ACK	DEGLITCH_TIME_EREG_PG	RSVD		DISABLE_RETRY_TIMER
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	FAULT_DEGLITCH_TIME_VIN	Set deglitch time for both OVP and UVP. 0b = 5μs 1b = 10μs
6	FAULT_DEGLITCH_TIME_OUTLDO	Set deglitch time for both OVP and UVP. 0b = 5μs 1b = Disable digital deglitch
5	FAULT_DEGLITCH_TIME_RAIL	Set deglitch time for rail faults. 0b = 5μs 1b = Disable digital deglitch
4	DEGLITCH_TIME_PWRDIS_IN_ACK	Set deglitch time for PWRDIS_IN and PWRDIS_ACK. 0b = 5μs 1b = 10μs
3	DEGLITCH_TIME_EREG_PG	Set deglitch time for EREG_PGs, only take effect when the pin is programmed as an input pin. 0b = 5μs 1b = 10μs
2:1	RSVD	Reserved
0	DISABLE_RETRY_TIMER	0b = Enable retry time 1b = Disable retry time

Table 76. GPIO_CFG_PWRDIS_OUT_REG

Address: 0x64
Description: This register sets PWRDIS pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_PWRDIS_OUT	PULL_UP_RES_PWRDIS_OUT		PULL_DOWN_RES_PWRDIS_OUT		FUNC_SEL_PWRDIS_OUT	RSVD	OD_EXT_R_PWRDIS_OUT
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_PWRDIS_OUT	0b = 1.2V 1b = 1.8V Note: It is only effective when REG_0x64[4] = 0b
6:5	PULL_UP_RES_PWRDIS_OUT	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x64[4] = 0b
4:3	PULL_DOWN_RES_PWRDIS_OUT	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω
2	FUNC_SEL_PWRDIS_OUT	Function selection. 0b = output pin, buffer out PWRDIS_IN signal. 1b = output pin, buffer out REG_0x18[7]
1	RSVD	
0	OD_EXT_R_PWRDIS_OUT	Open-drain pull-up resistor configuration. 0b = internal resistor 1b = external resistor

Table 77. GPIO_CFG_RST_L_REG

Address: 0x65 **Description:** This register sets RST_L pin configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_RST_L	PULL_UP_RES_RST_L		PULL_DOWN_RES_RST_L		RSVD		OD_EXT_R_RST_L
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_RST_L	0b = 1.2V 1b = 1.8V Note: It is only effective when REG_0x65[0]=0b
6:5	PULL_UP_RES_RST_L	00 = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x65[0]=0b
4:3	PULL_DOWN_RES_RST_L	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω
2:1	RSVD	Reserved.
0	OD_EXT_R_RST_L	Open-drain pull-up resistor configuration. 0b = internal resistor 1b = external resistor

Table 78. GPIO_CFG_GEN_INT_L_REG

Address: 0x66 **Description:** This register sets INT_L pin configuration.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_INT_L	PULL_UP_RES_INT_L		PULL_DOWN_RES_INT_L		RSVD		OD_EXT_R_GEN_INT_L
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_INT_L	0b = 1.2V 1b = 1.8V Note: It is only effective when REG_0x66[0] = 0b
6:5	PULL_UP_RES_INT_L	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x66[0] = 0b
4:3	PULL_DOWN_RES_INT_L	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω

2:1	RSVD	Reserved.
0	OD_EXT_R_GEN_INT_L	Open-drain pull-up resistor configuration. 0b = internal resistor 1b = external resistor

Table 79. GPIO_CFG_EREG1_EN_REG

Address: 0x67
Description: This register sets EREG1_EN pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG1_EN	PULL_UP_RES_EREG1_EN		PULL_DOWN_RES_EREG1_EN		FUNC_SEL_EREG1_EN	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG1_EN	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x75[7] = 0b
6:5	PULL_UP_RES_EREG1_EN	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x75[7] = 0b
4:3	PULL_DOWN_RES_EREG1_EN	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω
2	FUNC_SEL_EREG1_EN	Function selection. 0b = buffer out enable signal for external regulator 1. 1b = buffer out REG_0x18[6]
1:0	RSVD	Reserved.

Table 80. GPIO_CFG_EREG2_EN_REG

Address: 0x68
Description: This register sets EREG2_EN pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG2_EN	PULL_UP_RES_EREG2_EN		PULL_DOWN_RES_EREG2_EN		FUNC_SEL_EREG2_EN	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG2_EN	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x75[6] = 0b
6:5	PULL_UP_RES_EREG2_EN	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x75[6] = 0b
4:3	PULL_DOWN_RES_EREG2_EN	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω
2	FUNC_SEL_EREG2_EN	Function selection. 0b = buffer out enable signal for external regulator 2. 1b = buffer out REG_0x18[5]
1:0	RSVD	Reserved.

Table 81. GPIO_CFG_EREG3_EN_REG

Address: 0x69
Description: This register sets EREG3_EN pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG3_EN	PULL_UP_RES_EREG3_EN		PULL_DOWN_RES_EREG3_EN		FUNC_SEL_EREG3_EN	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG3_EN	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x75[7] = 0b
6:5	PULL_UP_RES_EREG3_EN	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x75[7] = 0b
4:3	PULL_DOWN_RES_EREG3_EN	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω
2	FUNC_SEL_EREG3_EN	Function selection. 0b = buffer out enable signal for external regulator 3. 1b = buffer out REG_0x18[4]
1:0	RSVD	Reserved.

Table 82. GPIO_CFG_EREG1_PG_REG

Address: 0x6A
Description: This register sets EREG1_PG pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG1_PG	PULL_UP_RES_EREG1_PG		PULL_DOWN_RES_EREG1_PG		FUNC_SEL_EREG1_PG	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG1_PG	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x6A[2] = 0b and 0x75[4] =0b
6:5	PULL_UP_RES_EREG1_PG	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x6A[2] = 0b and 0x75[4] =0b
4:3	PULL_DOWN_RES_EREG1_PG	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω Note: It is only effective when REG_0x6A[2] = 0b
2	FUNC_SEL_EREG1_PG	Function selection. 0b = output pin, buffer out REG_0x18[3] 1b = input pin, serve as EREG1's PGOOD signal
1:0	RSVD	Reserved.

Table 83. GPIO_CFG_EREG2_PG_REG

Address: 0x6B
Description: This register sets EREG2_PG pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG2_PG	PULL_UP_RES_EREG2_PG		PULL_DOWN_RES_EREG2_PG		FUNC_SEL_EREG2_PG	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG2_PG	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x6B[2] = 0b and 0x75[3] =0b
6:5	PULL_UP_RES_EREG2_PG	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x6B[2] = 0b and 0x75[3] =0b
4:3	PULL_DOWN_RES_EREG2_PG	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω Note: It is only effective when REG_0x6B[2] = 0b
2	FUNC_SEL_EREG2_PG	Function selection. 0b = output pin, buffer out REG_0x18[2] 1b = input pin, serve as EREG2's PGOOD signal
1:0	RSVD	Reserved.

Table 84. GPIO_CFG_EREG3_PG_REG

Address: 0x6C
Description: This register sets EREG3_PG pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG3_PG	PULL_UP_RES_EREG3_PG		PULL_DOWN_RES_EREG3_PG		FUNC_SEL_EREG3_PG	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG3_PG	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x6C[2] = 0b and 0x75[2] =0b
6:5	PULL_UP_RES_EREG3_PG	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x6C[2] = 0b and 0x75[2] =0b
4:3	PULL_DOWN_RES_EREG3_PG	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω Note: It is only effective when REG_0x6C[2] = 0b
2	FUNC_SEL_EREG3_PG	Function selection. 0b = output pin, buffer out REG_0x18[1] 1b = input pin, serve as EREG3's PGOOD signal
1:0	RSVD	Reserved.

Table 85. GPIO_CFG_EREG_DVS_REG

Address: 0x6D
Description: This register sets EREG_DVS pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_EREG_DVS	PULL_UP_RES_EREG_DVS		PULL_DOWN_RES_EREG_DVS		FUNC_SEL_EREG_DVS	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_EREG_DVS	0b = 1.8V 1b = 3.3V Note: It is only effective when REG_0x6D[2] = 0b and 0x75[1] =0b
6:5	PULL_UP_RES_EREG_DVS	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x6D[2] = 0b and 0x75[1] =0b
4:3	PULL_DOWN_RES_EREG_DVS	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω Note: It is only effective when REG_0x6D[2] = 0b
2	FUNC_SEL_EREG_DVS	Function selection. 0b = buffer out REG_0x18[0] 1b = tri-state (Hi-Z)
1:0	RSVD	Reserved.

Table 86. GPIO_CFG_IIN_LIM_REG

Address: 0x6E
Description: This register sets IIN_LIM pin configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PULL_UP_VOLTAGE_IIN_LIM	PULL_UP_RES_IIN_LIM		PULL_DOWN_RES_IIN_LIM		DO_IIN_LIM_INPIN	RSVD	OD_EXT_R_IIN_LIM
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	PULL_UP_VOLTAGE_IIN_LIM	0b = 1.2V 1b = 1.8V Note: It is only effective when REG_0x6E[2] = 0b and 0x6E[0] = 0b
6:5	PULL_UP_RES_IIN_LIM	00b = 1kΩ 01b = 2kΩ 10b = 3kΩ 11b = 4.7kΩ Note: It is only effective when REG_0x6E[2] = 0b and 0x6E[0] = 0b
4:3	PULL_DOWN_RES_IIN_LIM	00b = 100Ω 01b = 200Ω 10b = 300Ω 11b = 470Ω Note: It is only effective when REG_0x6E[2] = 0b
2	DO_IIN_LIM_INPIN	Set IIN_LIM as output mode or input mode. 0b = output mode, assert high when input overcurrent event detected. 1b = input mode (Hi-Z), no function
1	RSVD	Reserved
0	OD_EXT_R_IIN_LIM	Open-drain pull-up resistor configuration. 0b = internal resistor 1b = external resistor

Table 87. GPIO_WEAK_LOW_CFG_0_REG

Address: 0x6F
Description: This register sets GPIO (as input pin) configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	WEAK_LOW_PWRDIS_IN	WEAK_LOW_PWRDIS_ACK	RSVD					
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	WEAK_LOW_PWRDIS_IN	Only take effect as an input pin. 0b = disable 1b = 1μA to GND
6	WEAK_LOW_PWRDIS_ACK	Only take effect as an input pin. 0b = disable 1b = 1μA to GND
5:0	RSVD	Reserved

Table 88. GPIO_WEAK_LOW_CFG_1_REG

Address: 0x70
Description: This register sets GPIO (as input pin) configuration.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD			WEAK_LOW_EREG1_PG	WEAK_LOW_EREG2_PG	WEAK_LOW_EREG3_PG	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:5	RSVD	Reserved
4	WEAK_LOW_EREG1_PG	Only take effect as an input pin. 0b = disable 1b = 1μA to GND
3	WEAK_LOW_EREG2_PG	Only take effect as an input pin. 0b = disable 1b = 1μA to GND
2	WEAK_LOW_EREG3_PG	Only take effect as an input pin. 0b = disable 1b = 1μA to GND
1:0	RSVD	Reserved

Table 89. GEN_INT_L_EXCLUDE_REG

Address: 0x71
Description: This register sets GPIO exclude indicator.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GEN_EXCLUDE_RAIL_FAULTS	GEN_EXCLUDE_VIN_FAULTS	GEN_EXCLUDE_OUTLDO_FAULTS	GEN_EXCLUDE_EREGx_PG	GEN_EXCLUDE_PMIC_OTP	GEN_EXCLUDE_PWRDIS_ASSERTION	GEN_EXCLUDE_PMIC_RETRY_TIMER	GEN_EXCLUDE_VOUT_RESIDUE_CHK
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	GEN_EXCLUDE_RAIL_FAULTS	GEN_INT_L excludes rails fault. (OV/UV/OCP) 0b = include 1b = exclude
6	GEN_EXCLUDE_VIN_FAULTS	GEN_INT_L excludes VIN fault. (OV/UV) 0b = include 1b = exclude
5	GEN_EXCLUDE_OUTLDO_FAULTS	GEN_INT_L excludes OUTLDO fault. (OV/UV) 0b = include 1b = exclude
4	GEN_EXCLUDE_EREGx_PG	GEN_INT_L excludes EREGx_PG fail. 0b = include 1b = exclude
3	GEN_EXCLUDE_PMIC_OTP	GEN_INT_L excludes PMIC OTP. 0b = include 1b = exclude
2	GEN_EXCLUDE_PWRDIS_ASSERTION	GEN_INT_L excludes PWRDIS_ASSERTION. 0b = include 1b = exclude
1	GEN_EXCLUDE_PMIC_RETRY_TIMER	GEN_INT_L excludes retry timer. 0b = include, de-assert when retry timer is done. 1b = exclude
0	GEN_EXCLUDE_VOUT_RESIDUE_CHK	GEN_INT_L excludes VOUT residue check result. 0b = include, de-assert when VOUT < 100mV during SEQUENCE UP State. 1b = exclude

Table 90. RST_L_EXCLUDE_REG

Address: 0x72 **Description:** This register sets GPIO exclude indicator.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST_EXCLUDE_RAIL_FAULTS	RST_EXCLUDE_VIN_FAULTS	RST_EXCLUDE_OUTLDO_FAULTS	RST_EXCLUDE_EREGx_PG	RST_EXCLUDE_PMIC_OTP	RSVD		
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RST_EXCLUDE_RAIL_FAULTS	RST_L excludes rails fault. (OV/UV/OCP) 0b = include 1b = exclude
6	RST_EXCLUDE_VIN_FAULTS	RST_L excludes VIN fault. (OV/UV) 0b = include 1b = exclude
5	RST_EXCLUDE_OUTLDO_FAULTS	RST_L excludes OUTLDO fault. (OV/UV) 0b = include 1b = exclude
4	RST_EXCLUDE_EREGx_PG	RST_L excludes EREGx_PG fail. 0b = include 1b = exclude
3	RST_EXCLUDE_PMIC_OTP	RST_L excludes PMIC OTP. 0b = include 1b = exclude
2:0	RSVD	Reserved

Table 91. IIN_LIM_CFG_LSB_REG

Address: 0x73 **Description:** Setting for IIN_LIM pin as ADC result indicator.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IIN_LIM_CFG_LSB							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:0	IIN_LIM_CFG_LSB	IIN_LIM asserts high when IIN ADC result is higher than this value. Use it with MSB.

Table 92. IIN_LIM_CFG_MSB_REG

Address: 0x74
Description: Setting for IIN_LIM pin as ADC result indicator.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD					IIN_LIM_CFG_MSB		
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:3	RSVD	Reserved.
2:0	IIN_LIM_CFG_MSB	IIN_LIM asserts high when IIN ADC result is higher than this value. Use it with LSB.

Table 93. GPIO_OD_EXT_R

Address: 0x75
Description: Setting for open-drain pull-up by internal resistor or external resistor.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OD_EXT_R_EREG1_EN	OD_EXT_R_EREG2_EN	OD_EXT_R_EREG3_EN	OD_EXT_R_EREG1_PG	OD_EXT_R_EREG2_PG	OD_EXT_R_EREG3_PG	OD_EXT_R_EREG_DVS	OD_EXT_R_I2C
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	OD_EXT_R_EREG1_EN	Open-drain pull-up resistor configuration. 0b = internal resistor 1b = external resistor
6	OD_EXT_R_EREG2_EN	
5	OD_EXT_R_EREG3_EN	
4	OD_EXT_R_EREG1_PG	
3	OD_EXT_R_EREG2_PG	
2	OD_EXT_R_EREG3_PG	
1	OD_EXT_R_EREG_DVS	
0	OD_EXT_R_I2C	

Table 94. RAIL_FB_RATIO_CFG

Address: 0x76
Description: Setting for the FB resistor divided ratio of rails.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FB_RATIO_RAIL1	FB_RATIO_RAIL2	FB_RATIO_RAIL3	FB_RATIO_RAIL4	FB_RATIO_RAIL5	RSVD		
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	FB_RATIO_RAIL1	LOCKED by TM_KEY_2. 0b: FB=100%*VOUT (0.3V~2.1V, 10mV/step) 1b: FB=50%*VOUT (0.3V~3.46V, 20mV/step)
6	FB_RATIO_RAIL2	
5	FB_RATIO_RAIL3	
4	FB_RATIO_RAIL4	
3	FB_RATIO_RAIL5	
2:0	RSVD	Reserved

Table 95. DISABLE_OV_PROTECTION

Address: 0x77
Description: Setting for OVP disable.

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_OVP_DIS	RAIL1_OVP_DIS	RAIL2_OVP_DIS	RAIL3_OVP_DIS	RAIL4_OVP_DIS	RAIL5_OVP_DIS	OUTLDO_OVP_DIS	RSVD
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	VIN_OVP_DIS	0b: enable OVP 1b: disable OVP
6	RAIL1_OVP_DIS	
5	RAIL2_OVP_DIS	
4	RAIL3_OVP_DIS	
3	RAIL4_OVP_DIS	
2	RAIL5_OVP_DIS	
1	OUTLDO_OVP_DIS	
0	RSVD	Reserved

Table 96. DISABLE_UV_PROTECTION

Address: 0x78 **Description:** Setting for UVP disable.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VIN_UVP_DIS	RAIL1_UVP_DIS	RAIL2_UVP_DIS	RAIL3_UVP_DIS	RAIL4_UVP_DIS	RAIL5_UVP_DIS	OUTLDO_UVP_DIS	RSVD
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	VIN_UVP_DIS	0b: enable UVP 1b: disable UVP
6	RAIL1_UVP_DIS	
5	RAIL2_UVP_DIS	
4	RAIL3_UVP_DIS	
3	RAIL4_UVP_DIS	
2	RAIL5_UVP_DIS	
1	OUTLDO_UVP_DIS	
0	RSVD	Reserved

Table 97. DISABLE_OC_PROTECTION

Address: 0x79 **Description:** Setting for OCL & OCP disable.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RSVD	RAIL1_OC_DIS	RAIL2_OC_DIS	RAIL3_OC_DIS	RAIL4_OC_DIS	RAIL5_OC_DIS	OUTLDO_OC_DIS	RSVD
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	RSVD	Reserved
6	RAIL1_OC_DIS	0b: enable OCL & OCP 1b: disable OCL & OCP
5	RAIL2_OC_DIS	
4	RAIL3_OC_DIS	
3	RAIL4_OC_DIS	
2	RAIL5_OC_DIS	
1	OUTLDO_OC_DIS	
0	RSVD	Reserved

Table 98. DISABLE_NPG_PROTECTION

Address: 0x7A **Description:** Setting for EREG_PG ignoring action.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EREG1_NPG_DIS	EREG2_NPG_DIS	EREG3_NPG_DIS	RSVD				
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	EREG1_NPG_DIS	0b: check EREG_PG 1b: ignore EREG_PG
6	EREG2_NPG_DIS	
5	EREG3_NPG_DIS	
4:0	RSVD	Reserved

Table 99. OV_CFG_1_REG

Address: 0x7B **Description:** This register sets higher overvoltage level of rails.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OV_SELECTION2_RAIL1	OV_SELECTION2_RAIL2	OV_SELECTION2_RAIL3	OV_SELECTION2_RAIL4	OV_SELECTION2_RAIL5	OV_SELECTION2_OUTLDO	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	OV_SELECTION2_RAIL1	0b = follow OV_CFG_0 1b = 120%
6	OV_SELECTION2_RAIL2	
5	OV_SELECTION2_RAIL3	
4	OV_SELECTION2_RAIL4	
3	OV_SELECTION2_RAIL5	
2	OV_SELECTION2_OUTLDO	
1:0	RSVD	Reserved

Table 100. UV_CFG_1_REG

Address: 0x7C **Description:** This register sets lower undervoltage level of rails.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	UV_SELECTION2_RAIL1	UV_SELECTION2_RAIL2	UV_SELECTION2_RAIL3	UV_SELECTION2_RAIL4	UV_SELECTION2_RAIL5	UV_SELECTION2_OUTLDO	RSVD	
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	UV_SELECTION2_RAIL1	0b = follow UV_CFG_0 1b = 80%
6	UV_SELECTION2_RAIL2	
5	UV_SELECTION2_RAIL3	
4	UV_SELECTION2_RAIL4	
3	UV_SELECTION2_RAIL5	
2	UV_SELECTION2_OUTLDO	
1:0	RSVD	Reserved

Table 101. NVM_B1

Address: 0xB1 **Description:** Wafer lot number.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LOT_SERIAL_ID_NVM							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	LOT_SERIAL_ID_NVM	This byte shows the lowest two characters of Lot ID. Example: H6M8’71’-09G5 Lot1(0xB1[7:4]) = 7(0111) , Lot2(0xB1[3:0]) = 1(0001) →0xB1 = 0x71(Hex) = 01110001(BIN)
6		
5		
4		
3		
2		
1		
0		

Table 102. NVM_B2

Address: 0xB2 **Description:** Assembly time code in weeks to indicate when is FT performed.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ASSEMBLY_TIME_CODE_NVM							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	ASSEMBLY_TIME_CODE_NVM	Assembly time code in weeks to indicate when is FT performed.
6		
5		
4		
3		
2		
1		
0		

Table 103. TRIM_ALT_9

Address: 0xAA **Description:** For CP lots/wafer/location.								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CP_LOT_WAFER_LOCATION_0							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	CP_LOT_WAFER_LOCATION_0	Wafer X coordinate. X[7] to X[0]
6		
5		
4		
3		
2		
1		
0		

Table 104. TRIM_ALT_10

Address: 0xAB **Description:** For CP lots/wafer/location								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CP_LOT_WAFER_LOCATION_1							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

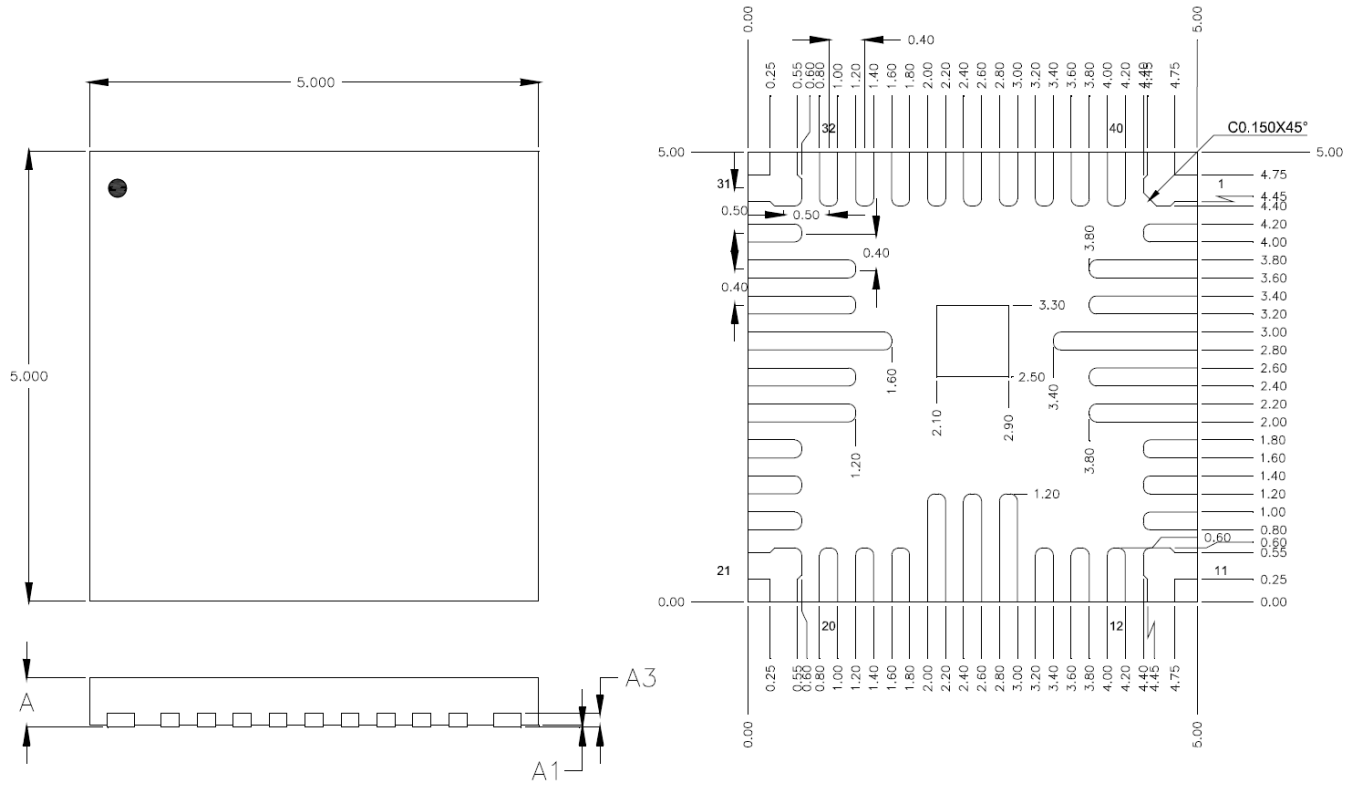
Bits	Name	Description
7	CP_LOT_WAFER_LOCATION_1	Wafer Y coordinate. Y[7] to Y[0]
6		
5		
4		
3		
2		
1		
0		

Table 105. TRIM_ALT_11

Address: 0xAC **Description:** For CP lots/wafer/location								
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CP_LOT_WAFER_LOCATION_2							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7	CP_LOT_WAFER_LOCATION_2	Wafer X coordinate. X[8]
6		Wafer Y coordinate. Y[8]
5		Wafer coordinate. X[9] or Y[9] (option)
4		Wafer Number[4:0]
3		
2		
1		
0		

Outline Dimension

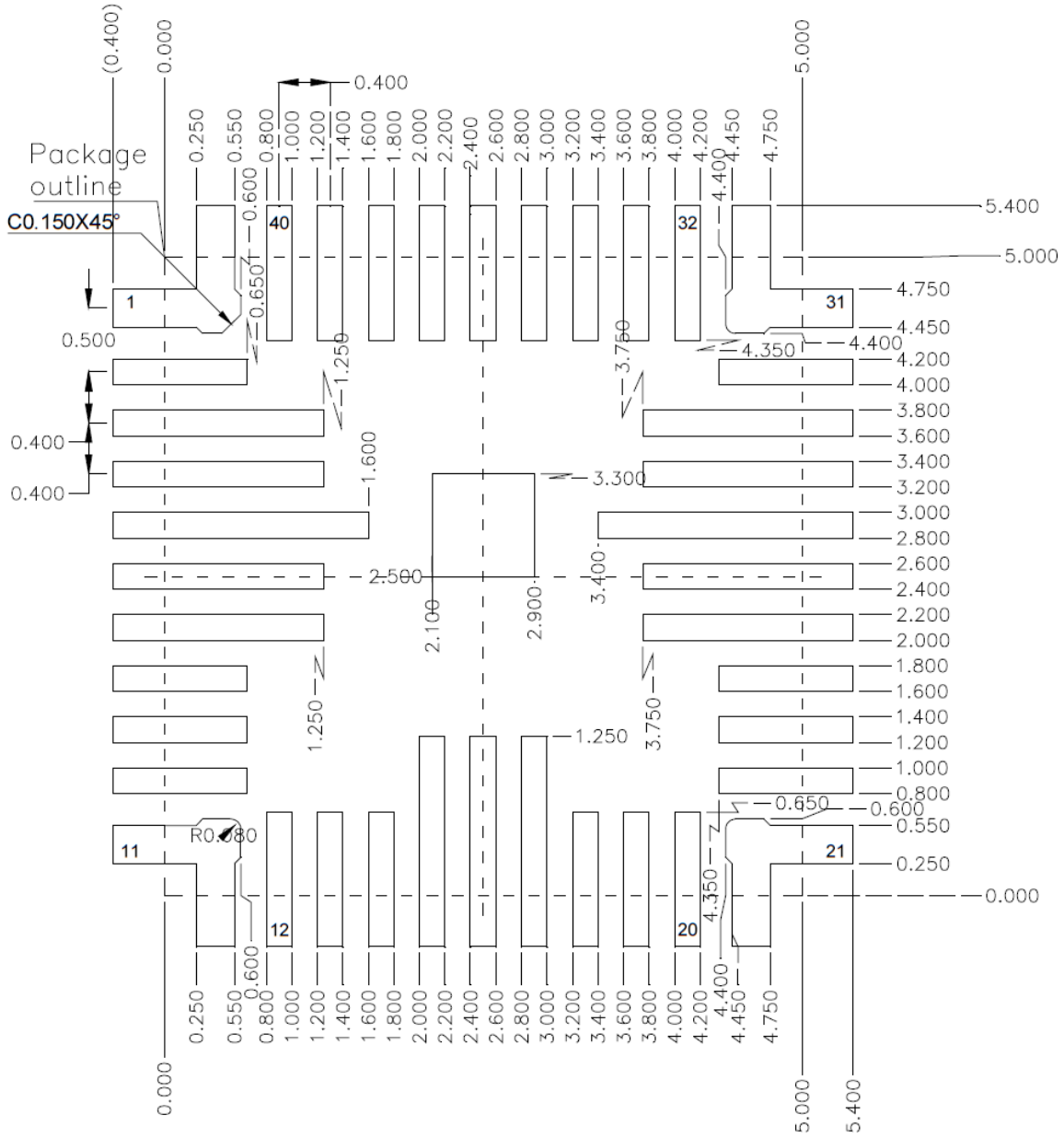


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008

Tolerance
±0.050

U-Type 40L QFN 5x5 Package (FC)

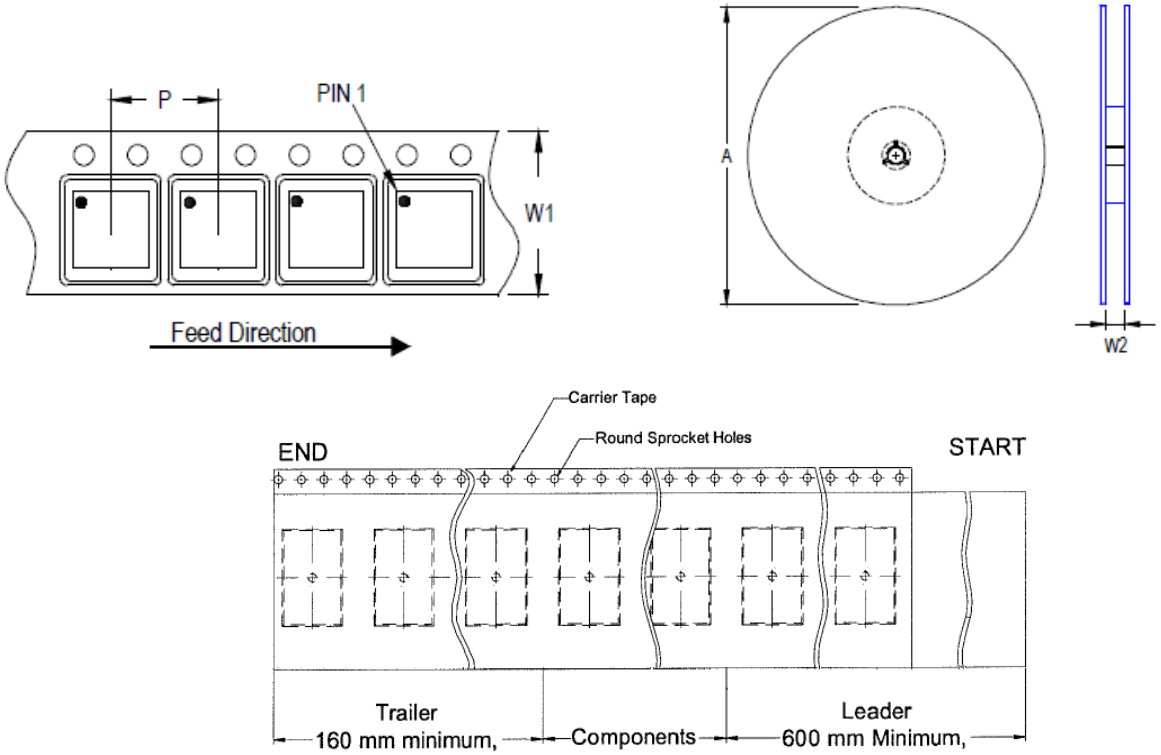
Footprint Information



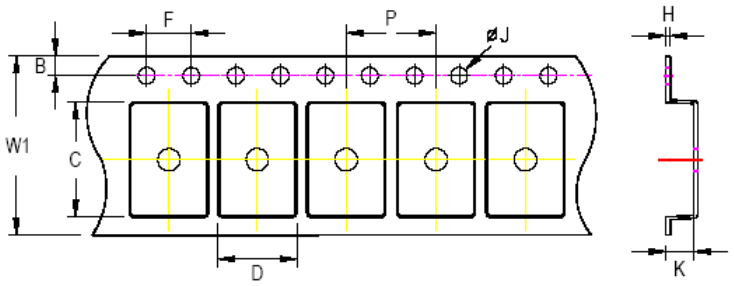
Package	Number of Pin	Tolerance
V/W/U/XQFN5x5-40(FC)	40	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/11/27	Final	