Speaker Amplifier with Speaker Protection

General Description

The RT5508 is a mono BTL class-D amplifier with cutting-edge speaker protection algorithm. Also, a built-in DC-DC step-up converter is used to provide efficient power for class-D amplifier. I^2S interface supports two different audio sources while a pair of auxiliary DATAI/O is used for stereo mode or pass-through application. Chip information including gain, speaker protection output or current sense is able to be monitored via DATAO through proper register setting. Speaker protection provides mechanical / thermal protection with accuracy of 10%/±10°C of rated limit.

Ordering Information

RT5508□□
- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  WSC : WL-CSP-29B 2.87x2.07 (BSC)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

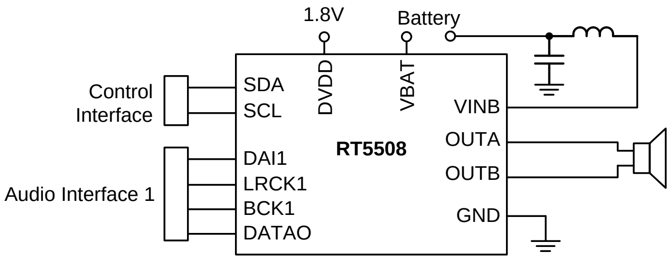
Features

- **Class-D Speaker AMP**
  - **1.6W Output Power @ 5.3V, 8Ω Load, THD < 1%**
  - **0/3/6/9/12/15dB Boost Gain**
  - **20μV Output Noise @ 0dB Gain**
- **Boost Converter**
  - **Adaptive Boost For Speaker, Boost from Battery Supply Up to Programmed Voltage, Max 5.3V**
  - **Power Modes : Adaptive Boost, Fixed Boost, Bypass Mode**
  - **Switching Frequency 2MHz, Maximum Output Current 1A**
  - **Support CCM / DCM Compensation, Feedback ADC**
  - **Digital Part : Voltage Loop in Boost Mode**
- **Digital**
  - **Digital Audio Interface Support I^2S, Left-Justified, Right-Justified**
  - **I^2S Sampling Rate Support up to 48kHz, 24-bit**
  - **Digital Filter, Digital Volume, Multi-Band DRC**
  - **Speaker Protection**
  - **Speaker Amplitude Estimation Accuracy : Error < 10%**
  - **Bl Calibration Function**
  - **Temperature Sensing**
  - **Speaker Temperature Estimation Accuracy : Error < ±10°C**

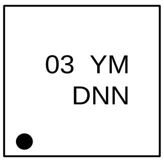
Applications

- Smart Phone
- Tablet

Simplified Application Circuit



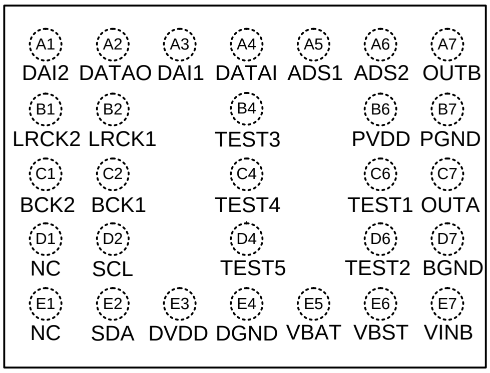
Marking Information



03 : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



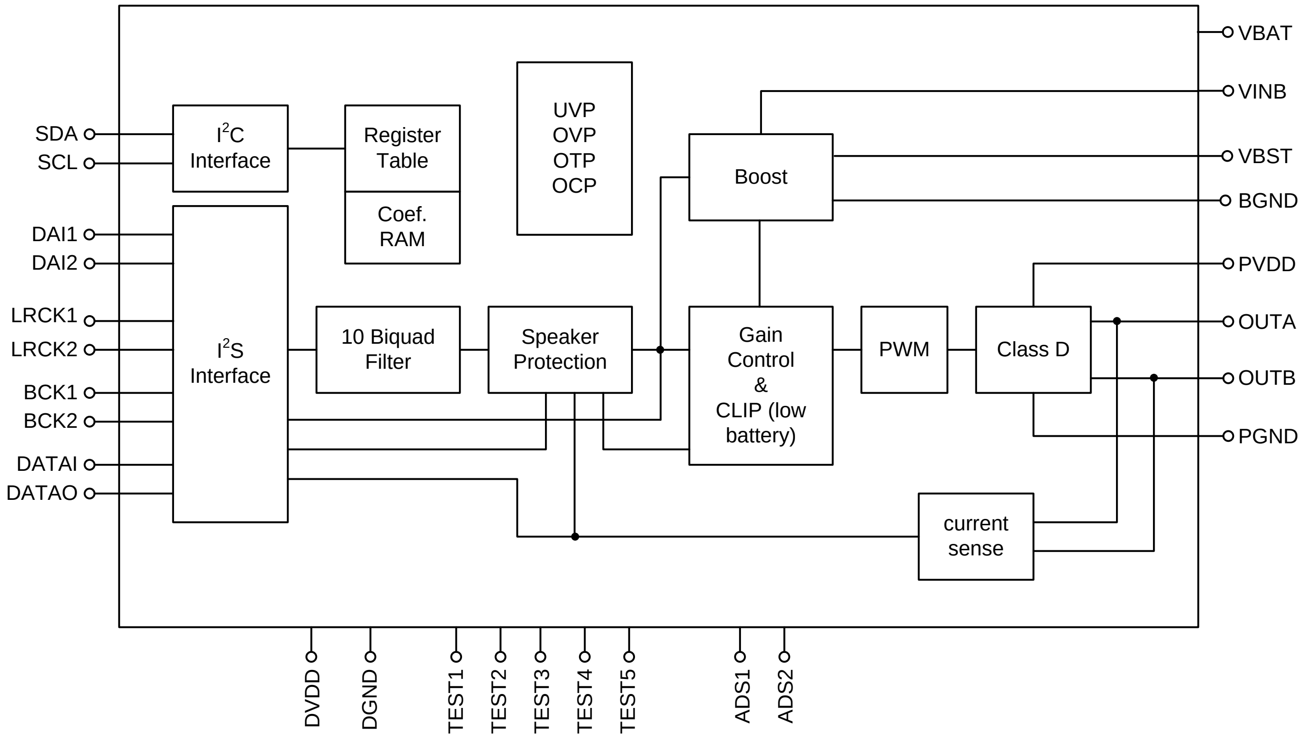
WL-CSP-29B 2.87x2.07 (BSC)

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
A1	DAI2	I	I^2S data input 2.
A2	DATAO	O	I^2S data output.
A3	DAI1	I	I^2S data input 1.
A4	DATAI	I	I^2S Data Input 3.
A5	ADS1	I	Address select 1.
A6	ADS2	I	Address select 2.
A7	OUTB	O	Class-d inverting output.
B1	LRCK2	I	I^2S word select 2.
B2	LRCK1	I	I^2S word select 1.
B4	TEST3	I	Test purpose, connect to PCB ground.
B6	PVDD	P	Class-D supply voltage.
B7	PGND	G	Class-D supply ground.
C1	BCK2	I	I^2S bit clock 2.
C2	BCK1	I	I^2S bit clock 1.
C4	TEST4	I	Test purpose, connect to PCB ground.
C6	TEST1	I	Test purpose, connect to VBST.
C7	OUTA	O	Class-D non-inverting output.
D1, E1	NC		No internal connection.
D2	SCL	I	I^2C clock.
D4	TEST5	I	Test purpose, connect to PCB ground.
D6	TEST2	I	Test purpose, connect to VBST.
D7	BGND	G	Boosted ground.
E2	SDA	I/O	I^2C data.
E3	DVDD	P	Digital / Analog supply voltage.
E4	DGND	G	Digital / Analog ground.

Pin No.	Pin Name	Type	Pin Function
E5	VBAT	I	Battery supply sense input.
E6	VBST	O	Boosted supply voltage.
E7	VINB	P	Boost converter input.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VBAT, VBST, VINB, PVDD -- –0.3 to 6V
- DVDD -- –0.3 to 2.5V
- LRCK, BCK, DATA I/O --- –0.3 to (DVDD + 0.3V)
- SCL, SDA -- –0.3 to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-29B 2.87x2.07 (BSC) -- 3W
- Package Thermal Resistance (Note 2)

  WL-CSP-29B 2.87x2.07 (BSC), θ_{JA} --- 33.3°C/W
- Lead Temperature (Soldering, 10 sec.) --- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range --- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) --- 2kV

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range --- –40°C to 85°C
- Junction Temperature Range -- –40°C to 125°C

Electrical Characteristics

(VBAT = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
Speaker Amp Supply Voltage	PVDD		2.7	3.6	5.5	V
Battery Supply Voltage	V_{BAT}		2.7	3.6	5.3	V
Boost Converter Input Voltage	V_{INB}		2.7	--	5.3	V
Shutdown Current (VBAT)	I_{SD_VBAT}	VBAT = 2.7 to 5.3V, DVDD = 1.8V	--	2	5	μA
		VBAT = 2.7 to 5.3V, DVDD = 0V	--	1	2	
Shutdown Current (DVDD)	I_{SD_DVDD}	VBAT = 2.7 to 5.3V, DVDD = 1.8V	--	10	20	μA
Offset Voltage	Vos	PVDD = 2.7 to 5.3V	--	1	--	mV
DAC to Stereo Speaker Amplifier						
Signal to Noise Ratio	SNR	PVDD = 5.3V, THD+N < 1%, DA Gain = 12dB, A-Weighting	--	96	--	dB
Noise level	Vn	DA Gain = 0dB, A-Weighting	--	20	--	μV
		DA Gain = 12dB, A-Weighting	--	60	--	
Total Harmonic Distortion + Noise	THD+N	1kHz, Po = 350mW, 8Ω, load	--	–65	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Output Power	Po	1kHz, PVDD = 3.6V, 8Ω load, 1%THD+N	--	0.65	--	W
		1kHz, PVDD = 5.3V, 8Ω load, 1%THD+N	1.5	1.6	--	W
Power Supply Rejection Ratio	PSRR	217Hz ripple = 200mVpp, Boost active	--	–80	--	dB
Quiescent Current (VBAT)	I_{Q_VBAT}	Normal operation, Speaker protection Bypassed	--	2	--	mA
Quiescent Current (DVDD)	I_{Q_DVDD}	Normal operation, Speaker protection Bypassed	--	12	--	mA
Efficiency	η	Output efficiency, 1kHz, Boost active	--	80	--	%
Over-Temperature Protection	OTP		130	--	150	°C
Over-Current Protection	OCP		1.5	--	--	A
The Recovery Time of SC			--	200	--	ms
Under-Voltage Protection	UVP		2.2	2.4	--	V
I2C Interface Electrical Characteristics (Note 5)						
SDA, SCL Input Threshold	V_{IH}		0.7 x DVDD	--	--	V
	V_{IL}		--	--	0.3 x DVDD	V
Pull-Down Current	I_{FO2}		--	2	--	μA
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.6	--	--	μs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.6	--	--	μs
Stop Condition Time	$t_{SU,STD}$		0.6	--	--	μs
Data Hold Time	$t_{HD,DAT}$ (OUT)		225	--	--	ns
Input Data Hold Time	$t_{HD,DAT}$ (IN)		0	--	900	ns
Data Setup Time	$t_{SU,DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	μs
Clock High Period	t_{HIGH}		0.6	--	--	μs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	50	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I^2S Interface Electrical Characteristics (Note 5)						
High-level Input Voltage	V_{IH}		0.7x DVDD	--	--	V
Low-level Input Voltage	V_{IL}		--	--	0.3x DVDD	V
Setup Time, LRCK to SCLK Rising Edge	t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge	t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge	t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge	t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCLK	t_r		--	--	8	ns

Note 1. Continuously stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

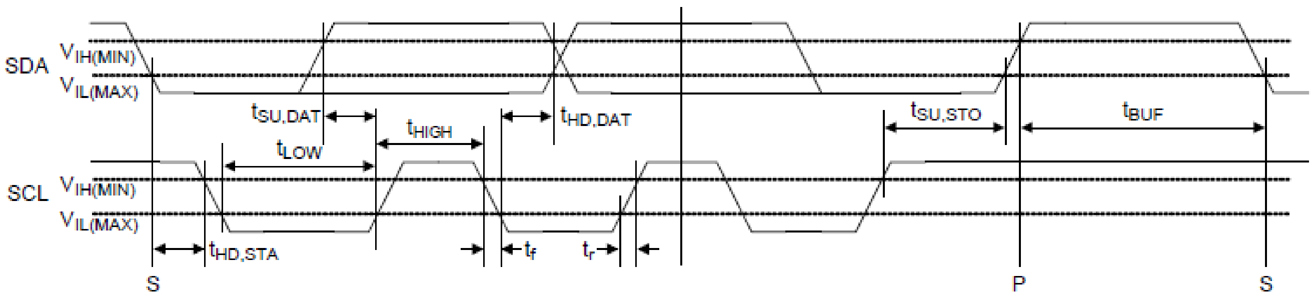


Figure 1. I^2C Interface Trimming Diagram

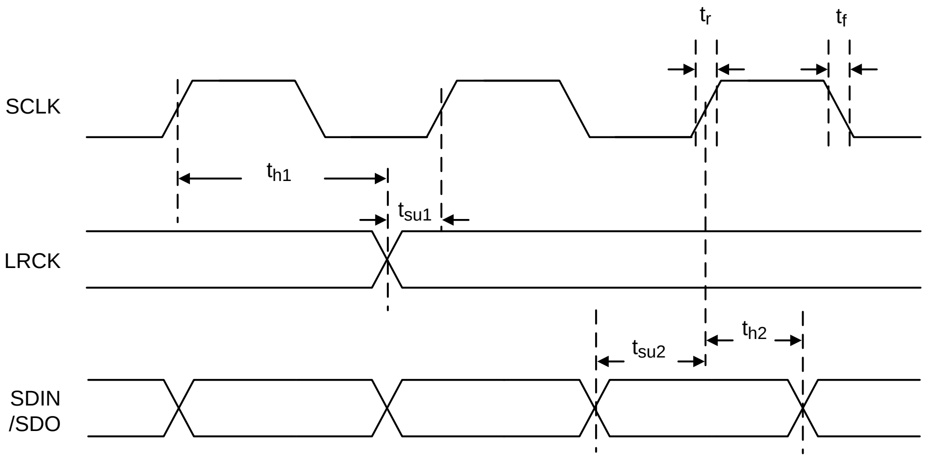


Figure 2. Timing diagram of Slave mode I^2S Interface

Typical Application Circuit

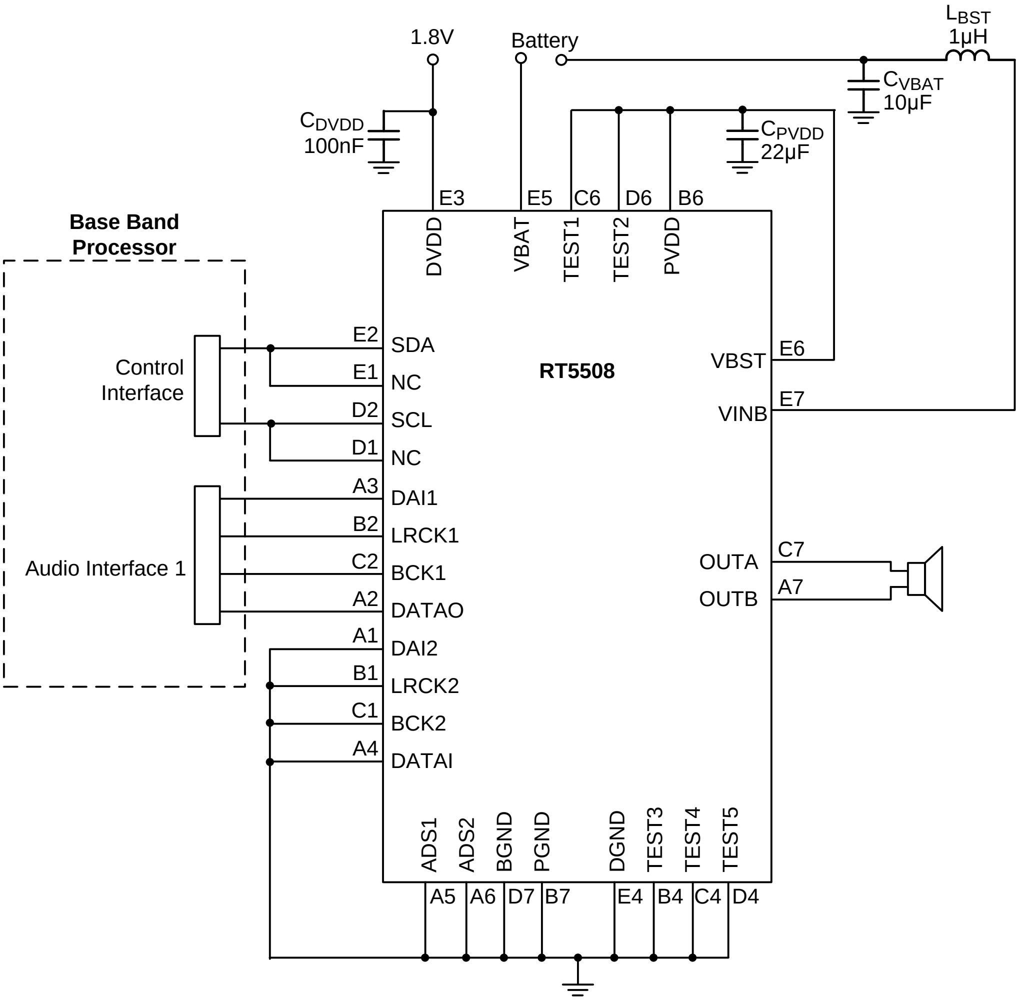


Figure 3. Mono Mode Application Circuit

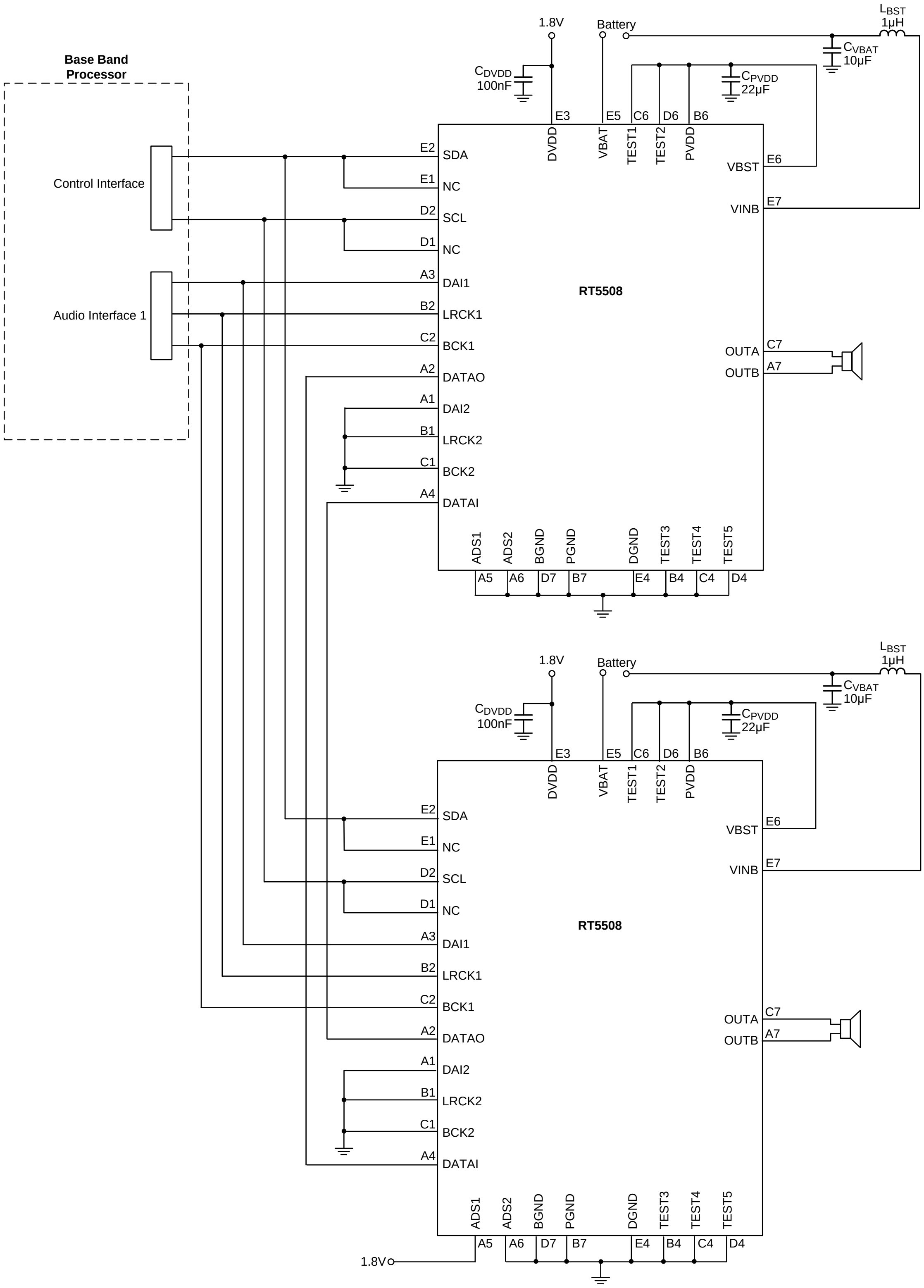
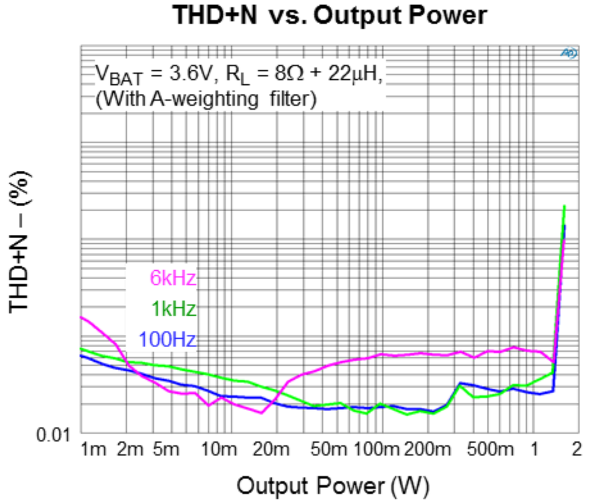
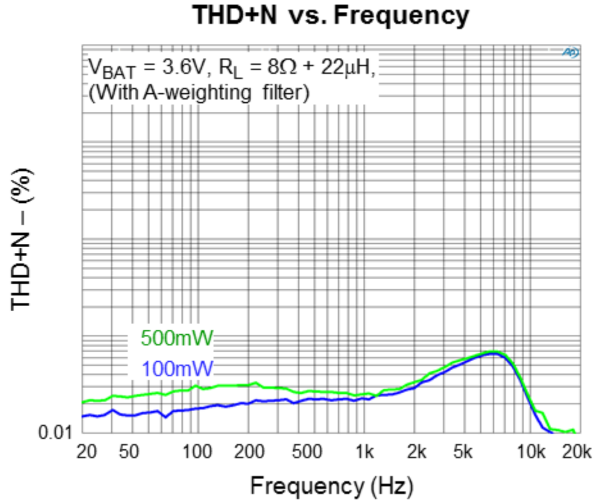
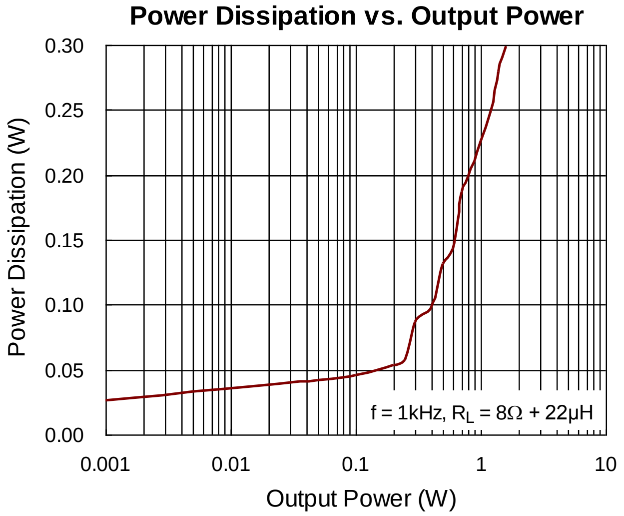


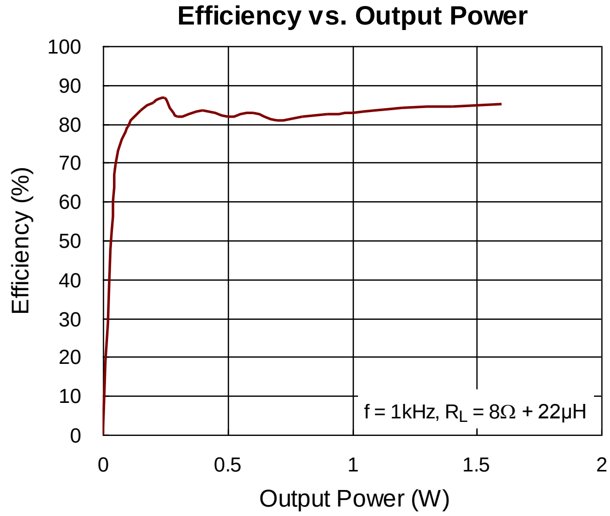
Figure 4. Stereo Mode Application Circuit

Typical Operating Characteristics









I²C Interface

Device Addressing

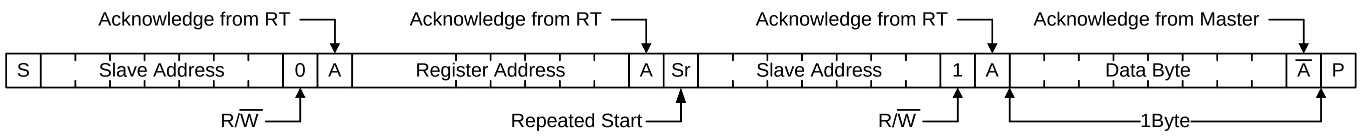
RT5508 Support I²C Control interface. The default device address is accessed via Pin ADS1 and ADS2. (see Table 1.) Four separate address are supported for stereo mode application. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively. The generic address is independent of pins ADS1 and ADS2.

Table 1. Address Selection Via Pins ADS1 and ADS2

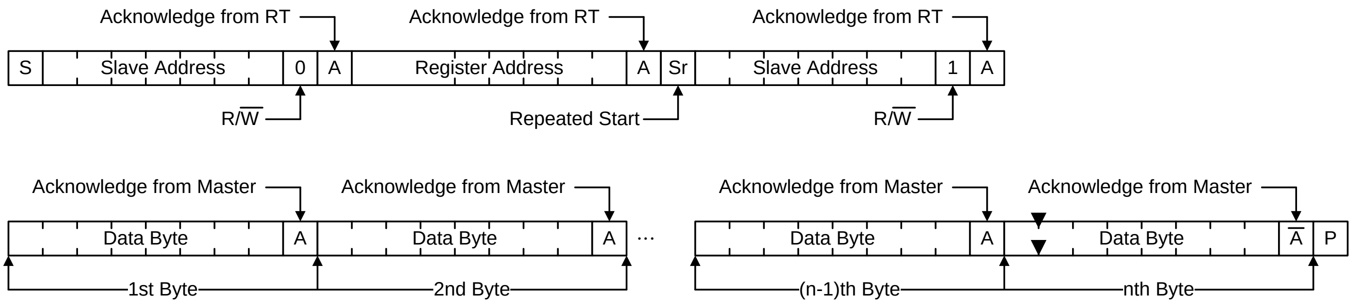
ADS2 Pin (V)	ADS1 Pin (V)	Address	Function (bit 0)
0	0	0110100x	0: write 1:read
0	DVDD	0110101x	0: write 1:read
DVDD	0	0110110x	0: write 1:read
DVDD	DVDD	0110111x	0: write 1:read

Read Function

Reading One Indexed Byte of Data from RT (With 1-Byte)

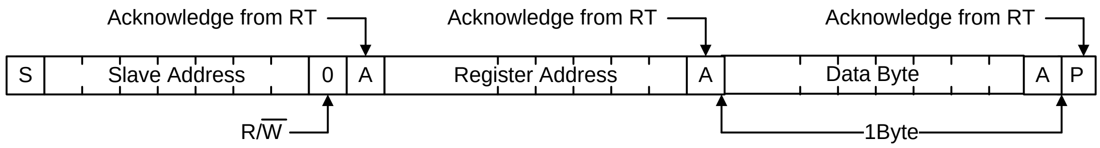


Reading n Indexed Words of Data from RT (With N-Byte)

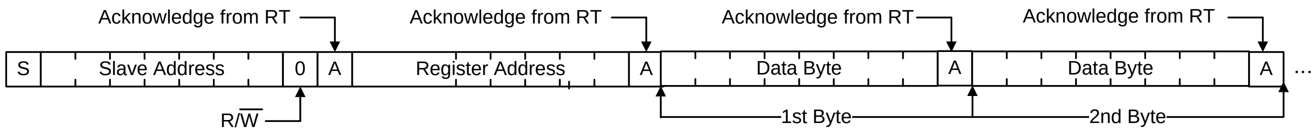


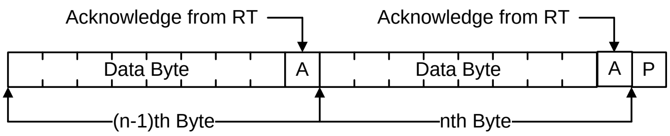
Write Function

Writing One Byte of Data to RT (With 1-Byte)



Writing n Byte of Data to RT (With N-Byte)





Operation Mode Modes

The RT5508 can operate in six different modes which are power-down/suspend/operating/mute/off/fault. Internal functional block operational status in different mode is depicted in Figure 5.

Mode / Blk	PWDN	SUSP	OP	MUTE	OFF	FAULT
PLL	×	○	○	○	○	○
I2C	○	○	○	○	○	○
I2S	×	△	○	○	○	○
SPK	×	△	○	○	○	○
AMP	×	△	○	△	⊠	⊠

○ : Normal operation

△ : Operational with zero input

⊠ : Output floating

× : Power down

Figure 5. Operation Mode

Power-Down mode (PWDN = 1)

When PWDN is set to 1, chip will enter power-down mode.

In power-down mode, power consumption is minimum and PWM outputs are floating.

I^2C remains awake in power-down mode.

If PWDN is set to 1, I^2S is also disabled.

Suspend mode (BCK/LRCK Invalid)

When BCK/LRCK is invalid, chip will enter suspend mode.

In suspend mode, most of the data path are off, and PWM outputs are floating.

I^2C remains awake in power-down mode.

PLL keeps awake used to monitor BCK/LRCK on I2S bus to see if they are correct.

Operating mode (PWDN = 0, SPKE = 1, SPKM = 0, AMPE = 1)

Operating mode is selected via PWDN/SPKE/SPKM/AMPE at register 0xXX. One of I2S interface (DATA1/DATA2) is selected as the audio source. In operating mode, the frequency of LRCK should be the same as I2SFS.

Mute mode (PWDN = 0, SPKE = 1, SPKM = 1, AMPE = 1)

Soft muting is used to prevent pop noise and is implemented in the speaker protection block when SPKE set to logic 1. Ramp up/down in exponential scale are implemented when switching between muted and unmuted mode.

Off mode (PWDN = 0, SPKE = 1, AMPE = 0)

The outputs of class-D are floating and chip is biased in off mode.

Soft mute can be executed if AMPDS at register 0xXX equals to 1 before chip enters off mode.

Fault Mode

Chip enters fault mode when an error event of physical protection mechanisms occurs (OCP/OVP/UVP/OTP).

The outputs of class-D are floating in Fault mode. The system exits from Fault mode after the protection event released for a checking cycle of about 200ms.

Mode Transition

The state machine of mode transition is shown in Figure 6. “Mute” mode is not shown in this figure since it can be considered as the sub-mode of the normal Operating mode, only with zero input signal.

The “Off” mode is usually used only in the power down sequence, and is depicted in the next sub-clause.

After power on, the control bit will always be reset to PWDN mode.

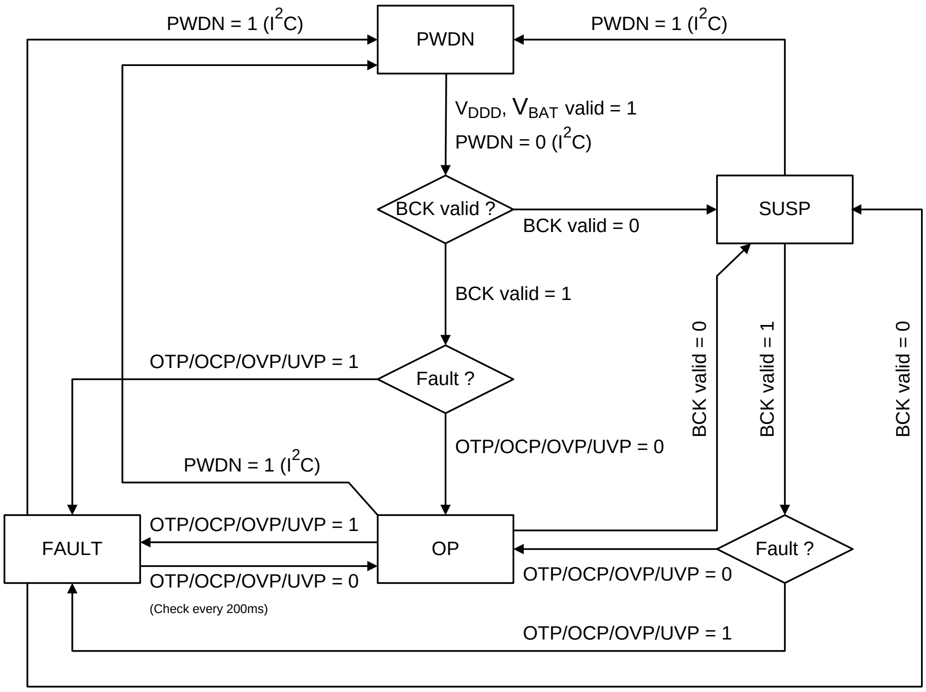


Figure 6. Mode Transition

Power ON Sequence

The power on sequence is shown in Figure 7. After power is valid, two groups of control signals should be set, without specific order requirement between these two groups :

1. I^{2}C : PWDN, AMPE should be programmed. These three bits can be programmed by single command since they are at the same byte address.

2. I^{2}C : I2SDIS, I2SFORMAT, I2SRATE set for reference clock selection for PLL.

I^{2}S : BCK should be valid on the specified interface.

If the PWDN is set to 0 before the BCK valid, it will go to SUSP mode automatically. The output of amplifier will be valid after entering OP mode, signal ramp up will always be implemented when the mode transits from PWDN or SUSP mode to OP mode.

Power OFF Sequence

The power off sequence is shown in Figure 8. PWDN mode should be set before the power supplies disconnected. To avoid pop or click, the amplifier should be turned off by setting AMPE = 0 before power down. Soft muting will also be enabled automatically if AMPDS bit is set to 1, which further ensures a pop-free procedure.

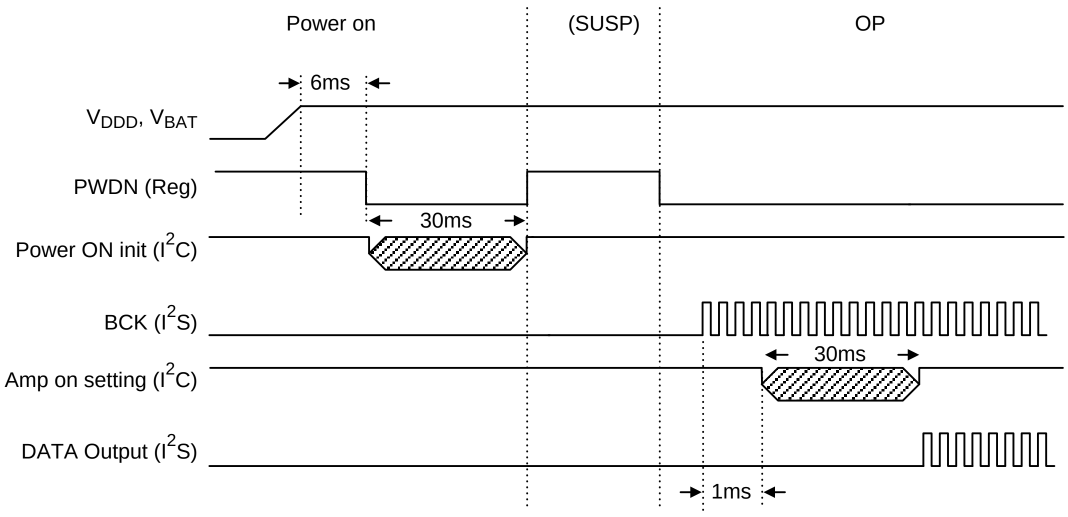


Figure 7. Power ON Sequence

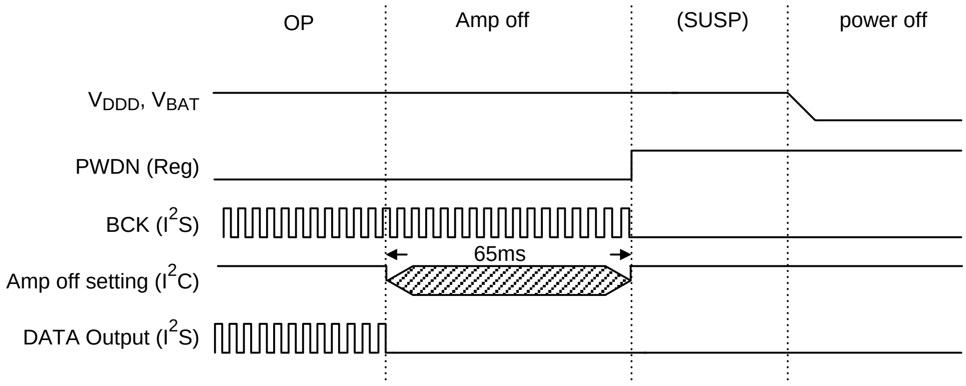


Figure 8. Power OFF Sequence

I^{2}S Mode Change without PWDN

Suspend mode is detected if the clock source from I^{2}S is not valid according to the value of I2SFORMAT/I2SRATE. In this case, soft muting is implemented before entering suspend mode. In the opposite situation, if the clock source from I^{2}S is detected valid again, signal ramp up is implemented at the start after it enters the operating mode.

The above procedure is shown in Figure 9.

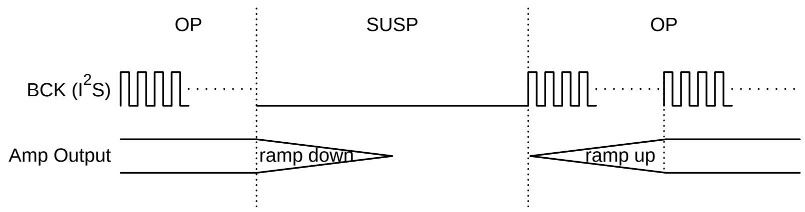


Figure 9. I^{2}S Mode Change without PWDN

Data (I^2S) Interface

Data Format

The I^2S formats supported by the RT5508 are listed below :

Interface	Data Format	BCK Frequency
I^2S Standard	up to 16-bit	32fs
I^2S Standard	up to 24-bit	48fs
I^2S Standard	up to 24-bit	64fs
MSB-justified	up to 16-bit	32fs
MSB-justified	up to 24-bit	48fs
MSB-justified	up to 24-bit	64fs
LSB-justified(16-bit)	16-bit	32fs
LSB-justified(16-bit)	16-bit	48fs
LSB-justified(16-bit)	16-bit	64fs
LSB-justified(20-bit)	20-bit	48fs
LSB-justified(20-bit)	20-bit	64fs
LSB-justified(24-bit)	24-bit	48fs
LSB-justified(24-bit)	24-bit	64fs

fs : 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz

I^2S Sampling Rate

I^2S can support sampling rate of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz. As shown in Figure 10, the sampling rate conversion block is applied to convert the data to internal working sampling rate, that is 44.1kHz or 48KHz. In stereo mode, the gain between two paths can be passed through each other.

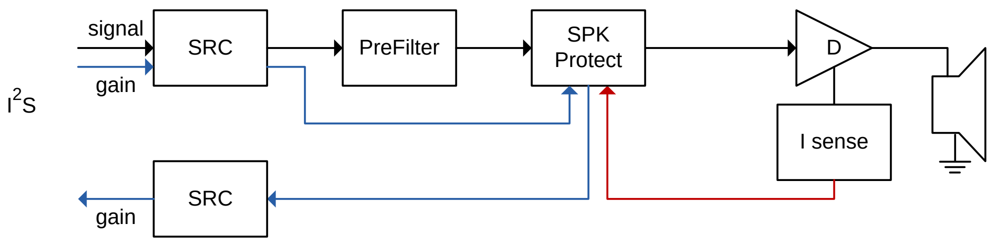


Figure 10. Sampling Rate

Setting I2SFORMAT/I2SRATE

I^2S data format and fs can be set by I2SFOMAT and I2SRATE at register 0x04 to 0x05.

RT5508 should be configured to power down or suspend mode before changing I2SFORMAT/ I2SRATE.

Input Path

I^2S input interface is shown in Figure 11. An internal mux select for two audio sources are supported. DATAI is used to provide stereo or pass-through application and uses BCK1/2, LRCK1/2 as its clock and word select signal. The active I^2S input is selected by I2SDIS and I2SCHS at register 0x06. After selecting I^2S input source, I2SLRS can be used to decide which channel (left, right or mixed) is sent to bi-quads.

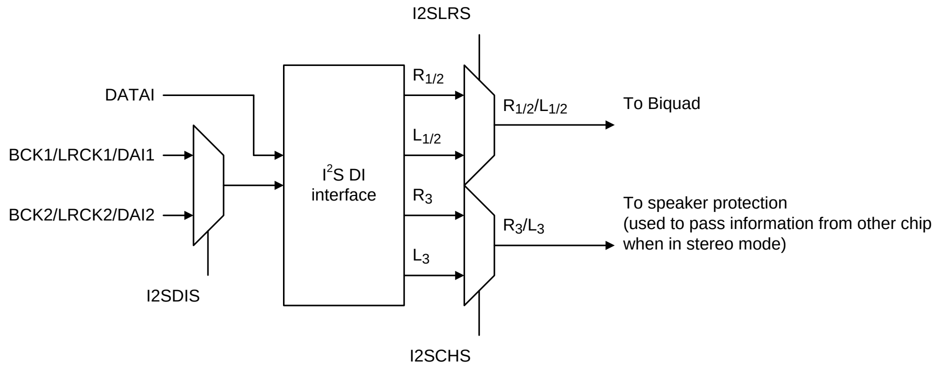


Figure 11. I^2S Input Mux

Output Path

DATAO can output different data via I2SDOS/I2SDOR /I2SDOL at register 0x07 to 0x08. It can also be disabled via I2SDOE at register 0x08. DATAO uses BCK1/2 as its reference clock to transmit desired data. LRCK1/2 is referred when I2SDOS/I2SDOE is switched to output I2SDOR/I2SDOL.

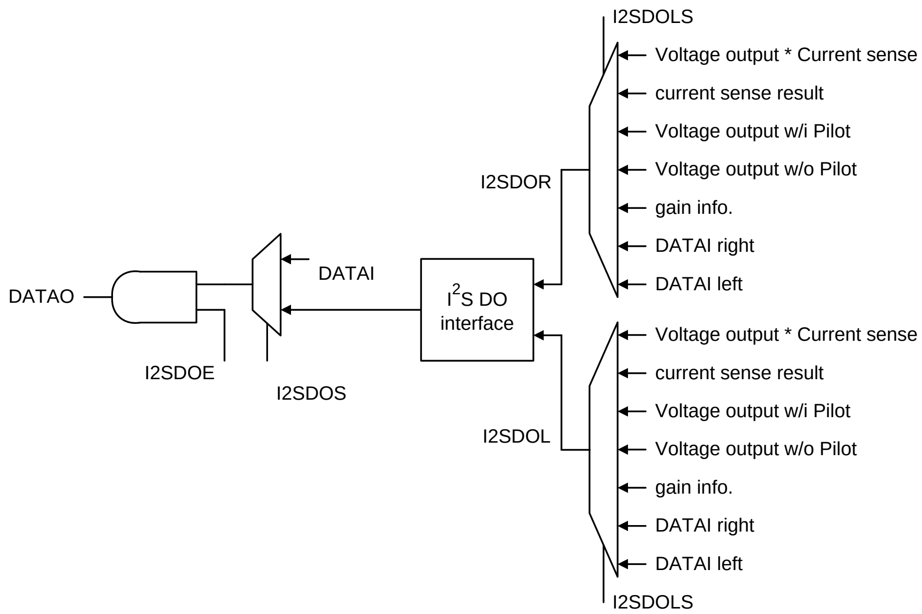


Figure 12. I^2S Output Mux

Sampling Rate Delay

The SRC introduces delay with respect to different I^{2}S sampling rates, which is shown in Table 2.

Table. 2Sampling Rate Conversion Delay

I^{2}S sampling rate	Delay	Absolute Delay
fs = 8k	29/fs	3.6ms
fs = 11.025k	28/fs	2.5ms
fs = 12k	28/fs	2.3ms
fs = 16k	29/fs	1.8ms
fs = 22.05k	26/fs	1.2ms
fs = 24k	26/fs	1.1ms
fs = 32k	29/fs	0.9ms
fs = 44.1k	0/fs	0ms
fs = 48k	0/fs	0ms

The I^{2}S signals at different sampling rate are all up-sampled to 48ksps or 44.1ksps before DSP processing or pass-through to PWM + class D amplifier. The data path delay is dominated by the group delay of SRC, the look-ahead delay of gain limiter, and some minor delay in SPK protection algorithm (<0.5ms).

For example: the worst case loopback delay of I^{2}S may be about 16ms (3.6*2+8+0.5) if fs = 8k and look-ahead delay = 8ms.

Signal Processing Path

After sampling rate conversion, the signal is processed by two sub-functions as shown in Figure 13. The pre-filters are some audio effect related functions, and the SPK protection block is the core function for speaker protection.

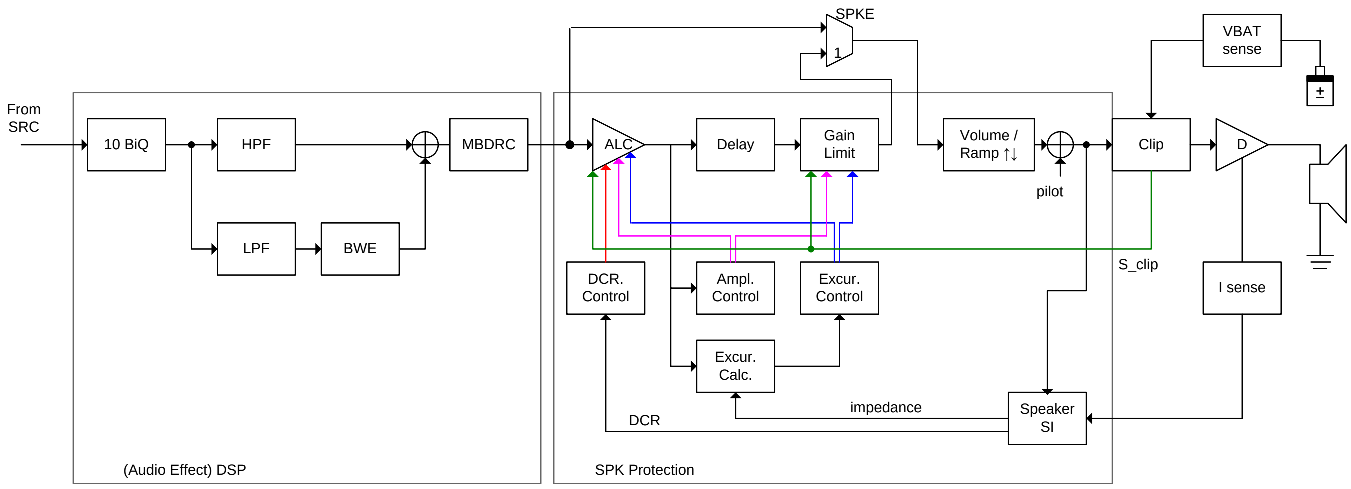


Figure 13. Signal Processing Path

Pass-through Mode

There is pass-through mode for debug or application use.

SPKE = 0 viewed as DSP through mode, where the signal is processed by DSP then passed through volume and amplifier.

Set SPKE = 1 to the normal mode, all functions are turned on regardless of the setting of DSPE.

Pilot is always disabled if SPKE = 0.

Audio Effect DSP Functions

10-BiQuad

After channel selection, there are 10 fully programmable bi-quad filters implemented for user-specified frequency response. The coefficients are 24-bit 2's complement numbers, which are set by I^2C interface.

Band-Split & BWE

Dedicated HPF/LPF with programmable corner frequency are equipped after 10-Biquad filters, both are implemented by selectable 1st or 2nd order Butterworth filter.

LPF is only needed when optional BWE is enabled. The BWE block generate harmonic terms to recover the suppressed of low-frequency signal that is not efficiently conveyed on small loudspeaker.

All the HPF/LPF/BWE functions can be bypassed.

Dynamic Range Control (DRC)

DRC is a specific feature to automatically adjust the volume gain corresponds to different input signal. With DRC function, the output dynamic range is under controlled from input amplitude is unknown or varies over a wide range. The RT5508 provide two thresholds as dynamic range compression (DRC_TH0) and extension (DRC_TH1). For the application of compression and extension, the slope ratio can be programmed as R0 and R1, respectively.

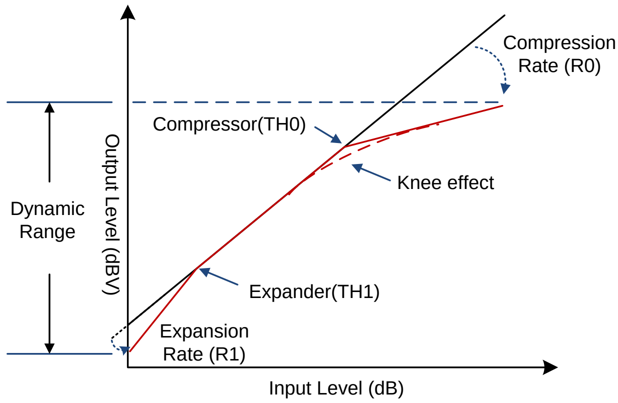


Figure 14. Dynamic Range Control

DRC function is composed of several parts as following Figure. The input signal passes through the programmable Energy Filter (DRC_AE). The Filter structure is shown in Figure 14. The time constant of each filter can be determined by below equation :

$$t_{window} = \frac{-1}{f_S \ln(1 - ae)}$$

Then, the filtered signal is compared with the given compression threshold. After the comparison between Input signal amplitude and threshold, the Attack Rate (DRC_AA) determines how quickly the DRC gain decreases when the signal amplitude is high. The Decay Rate (DRC_AD) determines how quickly the DRC gain increases when the signal amplitude is low.

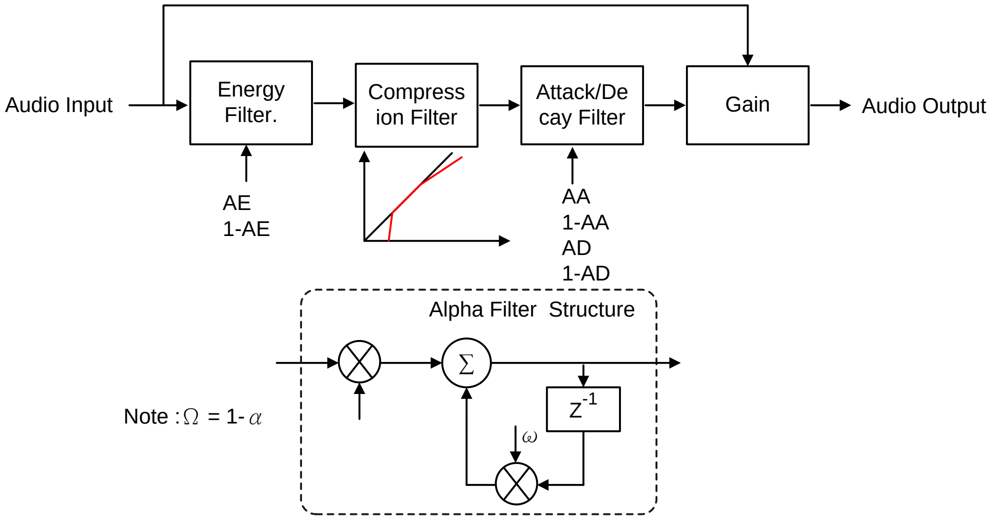


Figure 15. DRC Structure and Signal Processing Path

Speaker Protection Functions

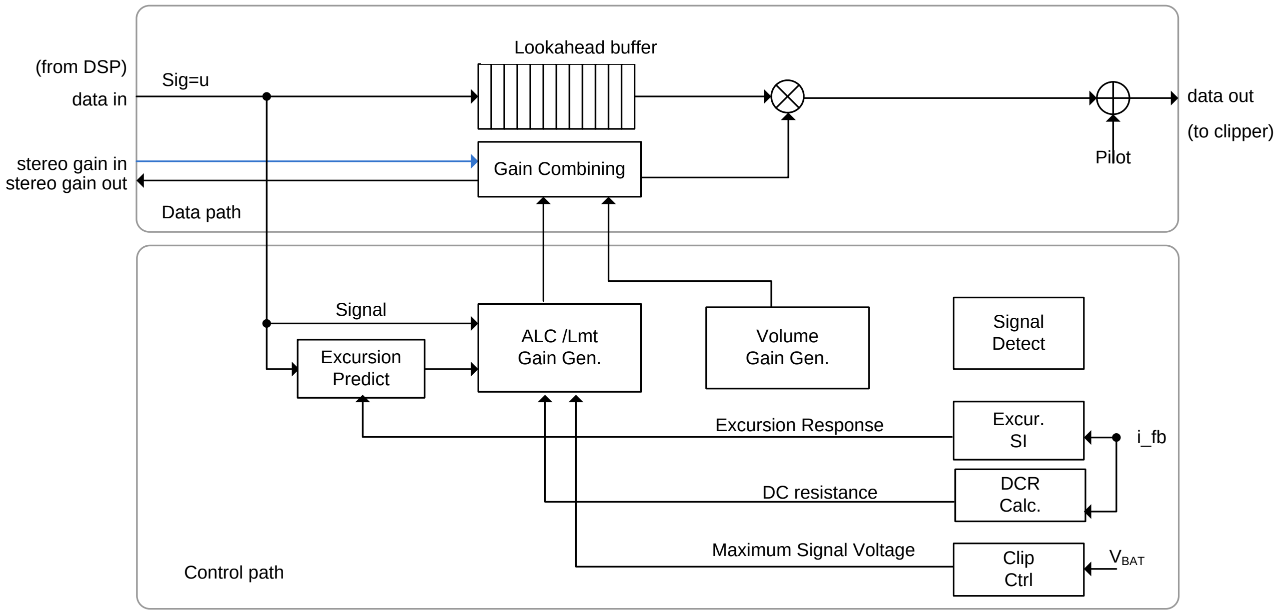


Figure 16. Block Diagram of SPK Protection Function

The following sub-clauses explain the function of each sub-block.

Look-Ahead Delay Buffer

Look-ahead delay can be programed from 0 up to 480 samples, which is up to 10ms at 48k sampling rate. This delay should contain stereo gain synchronization delay.

Gain Processing on the Data Path

The level control, limiting for protection, and the volume control are implemented by multiplying the signal on the data path, with the gain generated from the control path.

Pilot

The pilot signal, with constant magnitude (30mV) is added at the last stage of data path. The frequency of pilot is fixed fp = 50Hz.

The pilot is disabled at PWDN/SUSPD/Off/Fault/Mute mode.

A register control bit can be configured to set if the pilot is also turned off in Silence mode. If yes, then the pilot should be turn off after signal power below threshold for SilenceResetTime. This bit also defines if the DC resistance is monitored or not in Silence mode.

Except for Fault mode, the pilot always turned on or turned off at zero cross level. In worst case the pilot turn-off latency will be 11.6ms.

Signal Detector

The signal activity is detected when the input signal level is above a user defined threshold. The detection window can be specified to be 5ms/10ms/20ms.

Another long time constant: SilenceRestTime is used to ensure the silence happen and set the ALC to its initial gain.

Parameters :

sThresAct : silence or active threshold (0 to −90dBFS, -6dB step)

SilenceResetTime : the time to reset ALC gain to initial value (0 to 15 seconds)

Peak Detector

The peak detector monitors the peak of the signal magnitude and the estimated excursion. The algorithm is describe as following equation, with attack time can be specified as 0ms/1ms/2ms/4ms and release time can be specified by (1-RT) represented in 16-bit 2's complement format.

$$xPeak(n) = (1-AT) \times xPeak(n-1) + AT \times |x(n)|$$

$$xPeak(n) = (1-RT) \times xPeak(n-1)$$

for

$$|x(n)| > xPeak(n-1)$$

$$|x(n)| \leq xPeak(n-1)$$

Automatic Level Control (ALC)

The core of ALC gain control is depicted in Figure 15. The gain is checked and adjusted every ALC_period, which is specified by UpDoubleTime and DnHalfTime registers. These two register bit fields has physical meaning which mapped to approximately ±6dB per second. They can be specified from 1/16 to 15.9375 seconds with resolution of 1/16s.

The internal logic implements ALC_period by a counter expired every 16*UpDoubleTime or 16*DnHalfTime when the gain is going up/dn respectively. Depend on the clock base of I^2S, the nominal of ±6dB per second for double/half the gain is actually approximately by:

44.1k : 20*log10((4097/4096)^(48000/16)) = 6.36dB; 20*log10((4095/4096)^(48000/16)) = -6.36dB

48k : 20*log10((4097/4096)^(44100/16)) = 5.84dB; 20*log10((4095/4096)^(44100/16)) = -5.84dB

The Parameters for ALC Control :

sThresALC[7:0] : Threshold of signal, specified by 0 to1. 1 corresponds to the maximum allowable signal specified by clipper module.

xThresALC[7:0] : Threshold of excursion, specified by 0~1. 1 corresponds to the maximum allowable excursion.

sThresALC and xThresALC are 8-bit unsigned number representing the value 1/128~1, 0x80 is normalized to 1.

UpDoubleTime[7:0] : gain double time = UpDoubleTime /16 (seconds)

DnHalfTime[7:0] : gain half time = DnHalfTime /16

(seconds)

InitUpDoubleTime[7:0] : gain double time used for signal just detected from silence mode.

UpDoubleTime, DnHalfTime, InitUpDoubleTime and InitDnHalfTime are unsigned 8-bit number representing the value 1/16~15.9375, 0x10 is normalized to 1.

ALCInitGain[2:0] : ALC initial gain when signal is detected from silence mode. 0 ~ 21dB, 3dB step.

ALCMaxGain[2:0] : ALC maximum allowable gain. 0 ~ 21dB, 3dB step.

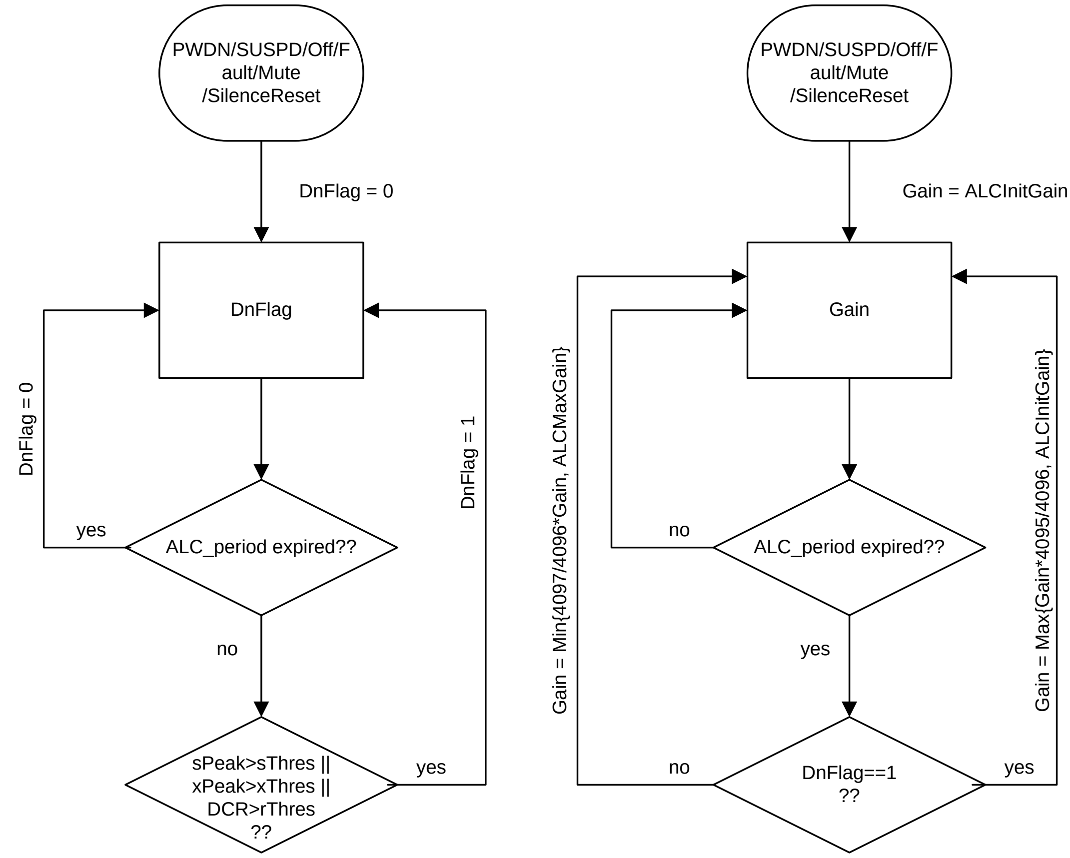


Figure 17. Gain Generation for ALC

Gain Limiter

The signal and excursion is limited to ensure the signal is not clipped, and the excursion never growth over the maximum allowable value.

The gain required to limit the signal and excursion are calculated by :

$$G_{Lmt} = \min\left\{\frac{sThres}{sPeak}, \frac{xThres}{xPeak}, 1\right\}$$

The parameters for Limiter control :

sThresLmt : Threshold of signal, specified by 0 to 1. 1 corresponds to the maximum allowable signal specified by clipper module.

xThresLmt : Threshold of excursion, specified by 0 to 1. 1 corresponds to the maximum allowable excursion.

xThresLmtDamage : Threshold of excursion when either resistance or excursion damage is detected.

DC Resistance Control Loop

DC Resistance Measurement

Metal coil resistance is highly linear dependent on the temperature, for example the scale factor is +0.393%/C for copper. The coil resistance is online monitored by the speaker protection algorithm. The update is disabled at PWDN/SUSPD/Off/Fault/Mute mode. A register bit can be set to define if the DC resistance is monitored or not in Silence mode.

The parameters for Coil Resistance :

- RNML : Nominal resistance of coil (Ω)
- RApp : The application resistance between amplifier and the loudspeaker, normalized to RNML. The application resistance is assumed to be constant through all time.

PI Control Loop :

- The parameters for PI-control loop:
- RMaxExcess : The maximum tolerable resistance growth ratio. 8-bit unsigned number representing the value 1/256 to 255/256
- PdictWeight : The weighting of prediction
- Kp: proportional gain of PI-controller
- KiKpRatio : ratio of Ki/Kp

This value of rMaxExcess should be set correctly considering the material dependent scale factor and the ambient temperature when the resistance calibration procedure is activated.

Excursion Control Loop

Speaker (Impedance) Identification

IIR with 2nd to 5th order can be chosen in this implementation. 3rd order is generally sufficient for the mobile devices, and 5th order is reserved for the case when vented-box is implemented. The impedance coefficients update is disabled at PWDN/SUSPD/Off /Fault/Mute mode or when the input signal power is below the threshold of the signal detector (Silence mode).

The parameters for impedance identification

- SglEn : enable the adaptation in single-tone case
- SIBlocks : block size to average coefficient update vector
- SIOrd : order of IIR filter
- InitImpIDMu : step size to update coefficient in initial stage
- ImpIDMU : step size in normal stage

Excursion Prediction

The excursion is predicted by integrating the back emf, which is induced by the coil movement and direct proportional to its velocity scaled by the Bl factor.

Resistance Calibration :

A measurement of resistance is activated by register control, after this procedure, the initial value of DCR is saved to One-Time-Program (OTP) memory.

The command/status for DC Resistance Calibration :

- DCRCalEn : Trigger the automatic DCR calibration procedure once
- InitDCR : Calibrated DC resistance value

Bl Calibration

Bl factor $\phi(0)$ can be calibrated to check if the preset coefficient is adequate.

The command/status for Bl Calibration :

- BlCalEn : Trigger the automatic Bl calibration procedure once
- InitBlFactor : Calibrated Bl factor

Speaker Damage Detection

In two cases the loudspeaker is considered as damaged :

1. The DCR deviates for a scale above predefined value.

2. The Resonant deviates for a scale above or below predefined value.

The parameters for Damage detection :

- rMaxDamage : Threshold of resistor growth, specified by 0 to 1, represents the ratio with respect to the value of initial calibrated resistor. “0” is a special setting that disables this function.
- fScaleDamage : The boundary for resonant frequency drift vs. the preset resonant frequency. 0~1,
- fRes x fScaleDamage > fRes0 or fRes < fRes0 x fScaleDamage will trigger the damage event.
- DamgeRecoveryTime : The time (seconds) to recovery from damaged situations. “0” is a special

setting that disables this function.

This value of rMaxDamage should be set correctly considering the material dependent scale factor and the ambient temperature when the resistance calibration procedure is activated.

Volume Control

The volume control can be set from –127.5dB to 0dB, with step = 0.5dB. The control timing is illustrated as in Figure . When a new gain is set by I^2C, the hardware will change from the original setting in step of 0.5dB/ΔT, where ΔT is the step size with the following options :

ΔT = 4, 8, 16, 32, 64 samples, or ΔT = 0 stands for no ramping up / down is applied.

When mute mode is set by I^2C or detected by hardware, the volume setting is overruled, but the original gain setting is kept in hardware, allows to be recovered to the original state.

Volume control can be bypassed by register.

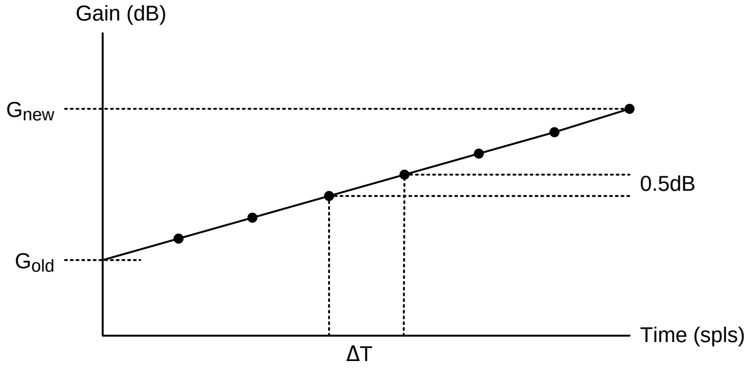


Figure 18. Volume Control Timing Graph

Clip Control

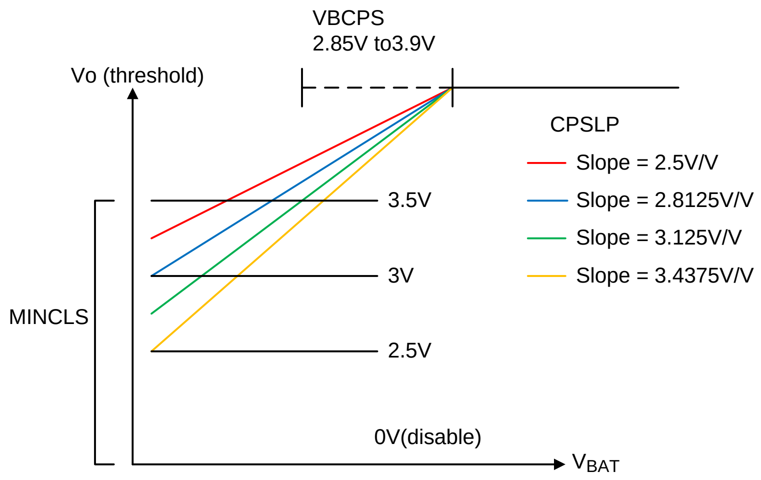


Figure 19. Clipping Threshold

Clip control is used to reduce current consumption when VBAT is low. It is defined by three parameters, VBCPS, CPSLP and MINCLS. The clip threshold is shown in Figure.

The voltage sent to class-D is clipped when VBAT is lower than clip point (2.85V to 3.9V) which is set by VBCPS. The slope of clip threshold (Vo/VBAT) can be set by CPSLP from 2.5V/V to 3.4375V/V. A VO stop point (0, 2.5V, 3V, 3.5V) for clip threshold can be set via MINCLS. The output voltage drop will stops at this point. The clip threshold is calculated through following equation :

$ClipThres = 5-(VBCPS-V_{BAT}) \times CPSLP$ for clip threshold $\geqq$ MINCLS

$ClipThres = MINCLS$ for clip threshold $\leqq$ MINCLS

After clip is done, a threshold is passed to speaker protection. Combined with speaker protection algorithm, a gain reduced procedure will be activated by speaker protection block and output signal is reduced to prevent clip. The detail function is shown below, the dropping rate of threshold can be set via CLIPDR at register 0x0B :

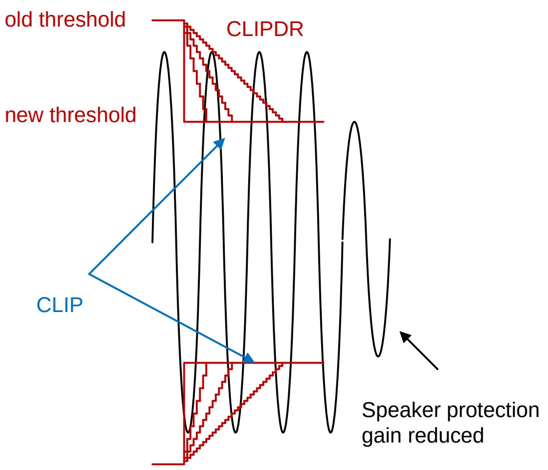


Figure 20. Clipper Gain Step Down

The threshold is normalized to 1 is passed to speaker protection which equals to :

$$ClipThres\ (normalized) = \frac{5 - (VBCPS - V_{BAT}) \times CPSLP}{5}$$

ClipThres (normalized) equals to 1 if signal is small and never reaches to the threshold. When signal is large and is clipped by this threshold, ClipThres (normalized) will be sent to speaker protection block.

If battery voltage returns to a hysteresis level, ClipThres will increase by a rate of CLIPRR to a certain level which is defined by VBCPS, CPSLP and VBAT. As ClipThres increases, speaker protection will also increase its gain to let the signal return to its original level. The battery voltage hysteresis can bet set via BVHYS at register 0x0B.

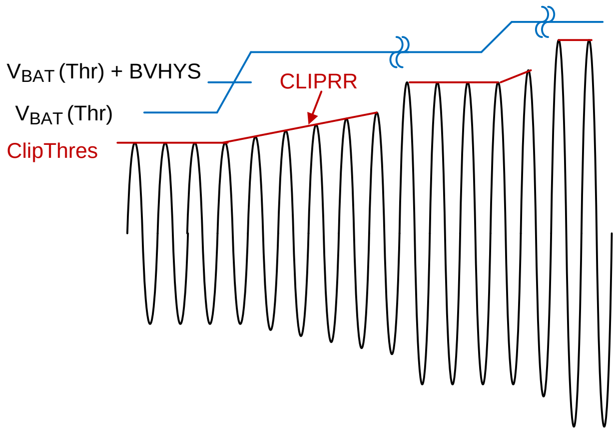


Figure 21. Clipper Gain Step Up

Boost Converter

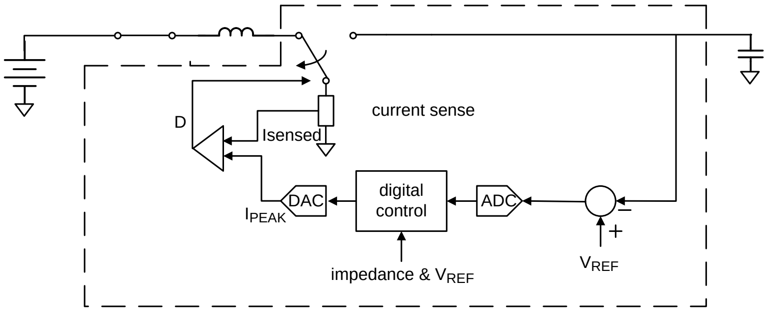


Figure 22. Boost converter schematic

A built-in boost converter is used to adjust class-D supply voltage. This converter could be operated in 4 different modes which are :

Disable Mode, in this case class-D is powered externally, boost converter is off.

Battery Mode, VBST = VBAT, boost converter is powered, but MOS is switched to OFF state at all times.

Fixed Mode, VBST = VBSTPG, VBAT is boosted to a certain value.

Adaptive Mode, VBST depends on the level of signal

The boost mode can be selected via BBMODE at register 0x14.

When boost converter is powered and in Boost/Adaptive mode, it tries to regulate the output voltage VBST to a desired value. The switching frequency f_{SW} is 2.048MHz (for fs = 8/12/16/24/32 kHz)/1.8816MHz (for fs = 11.025/22.05/44.1kHz).

The digital control logic inside this converter collects V_{REF}/load/Vo information and then output a I_{PEAK} value to general a proper D value which makes Vo equals V_{REF}. When in adaptive mode, boost converter can be used to generate required class-D power supply according to VBAT, TH1/TH2/TH3, THT1/THT2/THT3 and TOT where TH1/2/3, THT1/2/3 and TOT is at register 0x10 to 0x13.The detail function is shown below :

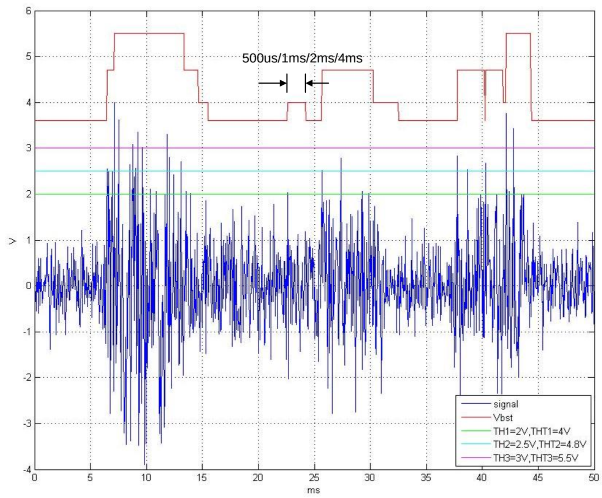


Figure 23. Illustration for Adaptive Boost Mode

TOT can be set to 500us/1ms/2ms/4ms :

```
if ( signal >= THx )
tot_cntx = 1;
elseif ( tot_cntx == TOT )
tot_cntx = 0;
elseif ( tot_cntx ~= 0 )
tot_cntx = tot_cntx+1;
else
tot_cntx = tot_cntx;                    (x:1/2/3)
if ( tot_cnt3 > 0 )
vbst = THT3;
elseif ( tot_cnt2 > 0 )
vbst = THT2;
elseif( tot_cnt1 > 0)
vbst = THT1;
else
vbst = VBAT;
```

Register Definition

Address Mapping

Registers Description

ADDR	Byte	Bits	R/W	Name	Description	Default
0x00	1	7:0	R	CHIP_ID[7:0]	Chip Revision ID	
0x01	1	7	R	BCK_CLOCK_STABLE	BCK rate stable	0
		6	R	PLL_LOCK	PLL is locked to BCK or LRCK 0 : Unlocked 1 : Locked	0
		5	R	BAT_UV	Battery voltage under threshold; analog signal 0 : Normal 1 : Under threshold	0
		4	R	AMP_OV	Class-D amplifier supply voltage (VDDP) over threshold; analog signal 0 : Normal 1 : Over threshold	0
		3	R	AMP_OC	Class-D amplifier output current over threshold; analog signal 0 : Normal 1 : Over threshold	0
		2	R	OT_FLAG	Class-D amplifier temperature over threshold; analog signal 0 : Normal 1 : Over threshold	0
		1	R	BST_OC	Boost converter current over threshold; 0 : Normal; 1 : Over threshold	0
		0	R	OT_FLAG_PULSE	Reserved	0
0x02		7:2	-	Reserved	-	
		1	WC	flagResDmg	Resistance exceeds the predefined value	1'b0
		0	WC	flagFreqDmg	Resonant frequency out of range	1'b0

ADDR	Byte	Bits	R/W	Name	Description	Default
0x03	1	7:6	-	Reserved	-	
		5	R/W	D_EN_TRIWAVE	Enable triangle wave generator	1
		4	R/W	AMPDS	Soft off mode enable 0 : Enter soft mode before off mode 1 : enter off mode directly	0
		3	R/W	AMPE	Class D Enable 0 : Disable Class D 1 : Enable Class D	0
		2	R/W	SPKM	Speaker protection mute 0 : Disable speaker protection mute 1 : Enable speaker protection mute	0
		1	R/W	SPKE	Speaker protection block enable 0 : Disable speaker protection 1 : Enable speaker protection	0
		0	R/W	PWDN	Chip power down control 0 : Chip enable 1 : Chip power down	1
0x04	1	7:5	-	Reserved	-	
		4	R/W	DSP_MODE_SEL	0 : DSP_MODE_A 1 : DSP_MODE_B	0
		3:2	R/W	AUD_FMT[1:0]	00 : I^2S 01 : Left Justify 10 : Right Justify 11 : DSP Mode	0
		1:0	R/W	AUD_BITS[1:0]	00 : 24 Bits 01 : 20 Bits 10 : 18 Bits 11 : 16 Bits	0
0x05	1	7	R	BCK_VALID	BCK stable and match with BCK_MODE setting	0
		6	R/W	BCK_MODE_DET_EN	Check BCK_VALID to enable audio path 0 : without check BCK_VALID 1 : check BCK_VALID	0
		4:3	R/W	BCK_MODE[1:0]	BCK Mode Select 00 : 32fs 01 : 48fs Others : 64fs	2'b10
		2:0	R/W	SR_MODE[1:0]	Sampling Rate Select 000 : 8K 001 : 12K/11.025K 010 : 16K 011 : 24K/22.05K 100 : 32K 101 : 48K/44.1K 110 : 96K/88.2K 111 : 192K/176.4K	3'b101

ADDR	Byte	Bits	R/W	Name	Description	Default
0x06	1	7:4	-	Reserved	-	
		3:2	R/W	I2SLRS	Biquad input selection 00 : left channel 01 : (left+right)/2 10 : right channel 11 : Reserved	2'b01
		1	R/W	I2SCHS	I^2S interface DATAI channel selection 0 : from DATAI left channel 1 : from DATAI right channel	0
		0	R/W	I2SDIS	I^2S interface 1/2 selection 0 : from I^2S interface 1 1 : from I^2S interface 2	0
0x07	1	7:4	R/W	I2SDORS	DATAO right channel output selection (DATA.R format: Q0.23) 0x0 : DATAI left = DATAO.R 0x1 : DATAI right = DATAO.R 0x2 : gain information = DATAO.R 0x3 : voltage output w/o pilot = DATAO.R * 16 0x4 : voltage output w/I pilot = DATAO.R 0x5 : corrent sense result = DATAO.R 0x6 : (voltage output w/I pilot)*current sense = DATAO.R * 16 0x7 : FDRC_DATA_OUT = DATAO.R 0x8 : SPK_DATA_OUT = DATAO.R 0x9 : est. current (for excursion est.) = DATAO.R 0xa : estimated current error = DATAO.R 0xb : rx_pilot = DATAO.R 0xc : estimated excursion = DATAO.R * 16 0xd : estimated Resistor = DATAO.R * 16 0xe : input signal behind notch filters = DATAO.R 0xf : excursion peak = DATAO.R * 16	4'h5

ADDR	Byte	Bits	R/W	Name	Description	Default
		3:0	R/W	I2SDOLS	DATAO left channel output selection (DATA.L format: Q0.23) 0x0 : DATAI3 left = DATAO.L 0x1 : DATAI3 right = DATAO.L 0x2 : gain information = DATAO.L 0x3 : voltage output w/o pilot = DATAO.L * 16 0x4 : voltage output w/I pilot = DATAO.L 0x5 : corrent sense result = DATAO.L 0x6 : (voltage output w/I pilot)*current sense = DATAO.L * 16 0x7 : EQ_DATA_OUT = DATAO.L 0x8 : DAC_DATA_IN = DATAO.L 0x9 : voltage input for excursion estimation = DATAO.L 0xa : est. current (for sys. identification) = DATAO.L 0xb : estimated velocity = DATAO.L * 16 0xc : digital maximum allowable absolute data = DATAO.L 0xd : side channel gain = DATAO.L 0xe : voltage from spkfb = DATAO.L 0xf : speaker protection input data = DATAO.L	4'h4
0x08	1	7:2	-	Reserved	-	
		1	R/W	I2SDOS	DATAO pass through selection 0 : DATAO is from I2SDOR/L 1 : DATAO is from DATAI3	0
		0	R/W	I2SDOE	DATAO output enable 0 : Disable 1 : Enable	0
0x09	1	7	-	Reserved	-	
		6	R/W	STRSYNC	Gain Synchronize in stereo mode 0 : Don't sync 1 : Sync to use minimum gain from two channels	0
		5	R/W	LMTEN	Limiter Enable 0 : Disabe 1 : Enable	0
		4	R/W	ALCEN	ALC gain Control enable 0 : Disable 1 : Enable	0
		3	R/W	MBDRCEN	Multi-Band DRC Enable 0 : Disable 1 : Enable	0
		2	R/W	BWEEN	LPF+BWE enable 0 : Disable, output zero at lower branch 1 : Enable	0
		1	R/W	HPFEN	HPF enable 0 : Bypass at upper branch 1 : Enable	0
		0	R/W	BQEN	10 Band BQ Enable 0 : ByPass 10 band BQ 1 : Enable 10 band BQ	0

ADDR	Byte	Bits	R/W	Name	Description	Default
0x10	1	7:3	-	Reserved	-	0
		2:0	R/W	VBCPS	Clip threshold setting 000 : 4.0V 001 : 3.75V 010 : 3.6V 011 : 3.45V 100 : 3.3V 101 : 3.15V 110 : 3V 111 : 2.85V	0
0x11	1	7	R/W	CLPE	Clip enable	0
		6	-	Reserved	-	
		5:4	R/W	BVHYS	Battery voltage recovery hysteresis 00 : battery voltage + 0.05 01 : battery voltage + 0.1 10 : battery voltage + 0.15 11 : battery voltage + 0.2	0
		3:2	R/W	CLIPRR	Rate of Vo threshold recover when Vbat return 00 : increase by 1/8 of orignal Vo per 1s 01 : increase by 1/8 of orignal Vo per 1.5s 10 : increase by 1/8 of orignal Vo per 2s 11 : increase by 1/8 of orignal Vo per 2.5s	0
		1:0	R/W	CLIPDR	Rate of Vo threshold drop when Vbat is low 00 : 1/16 of orginal per sample 01 : 1/8 of orginal Vo 10 : 1/4 of orginal Vo 11 : 1 step to target	0
0x12	2	15:10	-	Reserved	-	
		9:0	R/W	CPSLP	Clip slope setting : For example 3Vo/VBAT CPSLP = 3/DtoA GAIN(DAC+CLASS-D)	0
0x13	2	15:0	R/W	VOMIN	Minimum Clip threshold converted from (V) For example, minimum clip threshold is 2.5V, then VO_MIN = 2.5V / DtoA GAIN(DAC+CLASS-D) 16’b0 : no minimum	0
0x14	2	15:0	R/W	SIGMAX	Digital maximum allowable absolute data : SIG_MAX = max absolute voltage (V) / DtoA GAIN(DAC+CLASS-D) This value should be less than 1	16’h4000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x16	1	7:6	R/W	IDAC3_R	IDAC3 resolution (μA) : 00 : 0.05/16 01 : 0.1/16 10 : 0.15/16 11 : 0.2/16	2’b01
		5:4	-	Reserved	-	
		3:2	R/W	KP_GAIN	Kp parameter gain : 00 : 0.5x 01 : 1x 10 : 2x 11 : 4x	2’b01
		1:0	R/W	KI_GAIN	Ki parameter gain : 00 : 0.5x 01 : 1x 10 : 2x 11 : 4x	2’b01
0x1B	1	7:0	R/W	VBAT_GAIN	Mapping VBAT 1LSB to real value (1LSB = 1/1024V) : Ex. VBAT 1LSB = 5mV VBAT_GAIN = 0.005/(1/1024) * 32 =	8’h7E
0x1E	1	7:2	R/W	IPEAK_LOW	ipeak low limit	6’hA
		1:0	R/W	BST_MODE	Boost mode : 00 : disable 01 : battery 10 : fixed 11 : adaptive	2’b0

ADDR	Byte	Bits	R/W	Name	Description	Default
0x1F	1	7:4	R/W	BST_THT1	0000 : Disabled 0001 : 3.1 V 0010 : 3.3 V 0011 : 3.5 V 0100 : 3.7 V 0101 : 3.9 V 0110 : 4.1 V 0111 : 4.3 V 1000 : 4.5 V 1001 : 4.7 V 1010 : 4.9 V 1011 : 5.1 V 1100 : 5.3 V Others : Rsvd	4’b0000
		3:0	R/W	BST_TH1	0000 : disabled 0001 : 1.5 V 0010 : 1.7 V 0011 : 1.9 V 0100 :2.1 V 0101 : 2.3 V 0110 : 2.5 V 0111 : 2.7 V 1000 : 2.9 V 1001 : 3.1 V 1010 : 3.3 V 1011 : 3.5 V 1100 : 3.7 V 1101 : 3.9 V Others : Rsvd	4’b0000
0x20	1	7:4	R/W	BST_THT2	Same definition as BST_THT1	4’b0000
		3:0	R/W	BST_TH2	Same definition as BST_TH1	4’b0000
0x21	1	7:4	R/W	BST_THT3	Same definition as BST_THT1	4’b0000
		3:0	R/W	BST_TH3	Same definition as BST_TH1	4’b0000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x22	1	7	R/W	EN_AMP_OCP_LATCH	1 : Enable amplifier OCP latch	0
		6:4	R/W	AUDIO_IN2_SEL	audio_in2 delay selection : 000 : No delay 001 : 0.5μs 010 : 1.0μs 011 : 1.5μs 100 : 2.0μs 101 : 2.5μs Others : Rsvd	3'b000
		3:2	R/W	SLEW_RATE	VBST slew rate when using adaptive mode : 00 : 2.5mV/μs 01 : 5mV/μs 10 : 20mV/μs 11 : 10mV/μs	2'b01
		1:0	R/W	BST_TOT	Level timeout time : 00 : 500μs 01 : 1ms 10 : 2ms 11 : 4ms	2'b01
0x23	1	7:0	R/W	SIG_GAIN	Signal path gain : SIG_GAIN = DA gain * other analog gain * 10	8'h69
0x24	1	7	R/W	D_VBB_7P5V_EN	Enable to slow the gate driver slew rate for 7.5V operation	0
		6	R/W	D_FCCM	Force boost operate in CCM mode	1
		5	R/W	D_DCM_EN	DCM enable : 0 : Disable 1 : Enable	1'b0
		4	R/W	PSM_EN	PSM enable : 0 : Disable 1 : Enable	1'b0
		3:2	-	Reserved	-	-
		1:0	R/W	PSM_THR2	PSM VREF threshold : 00 : 10mV 01 : 20mV 10 : 30mV 11 : 40mV	2'b01
0x25	1	7	R/W	BST_FORCE_FSW3X	Force boost switching frequency from 2MHz to 6MHz	0
		6	R/W	BST_AUTO_FSW3X	Auto detect to make boost switching frequency from 2MHz to 6MHz	0
		5:0	R/W	PSM_THR1	PSM IPEAK value setting : When 6-bit IDAC1 < PSM_THR1, PSM mode is enabled if PSM_EN and DCM_EN is on. The actual IPEAK is calculated as following: IPEAK ~ (IDAC1(6-bit) * 0.625e-3 *12.2 * 50 /6.1) – (slope_comp * (1-VBAT * effi / VBST))	6'b0

ADDR	Byte	Bits	R/W	Name	Description	Default
0x26	1	7	R	D_OCP	Latch OC flag if EN_AMP_OCP_LATCH = 1 and cd_ocp_prot_en = 0	
		6:4	-	Reserved	-	
		3	R	OC_EV	OC event happens	
		2	R	OT_EV	OT event happens	
		1	R/W	OCP_EN	Over-current protection enable: 0 : Disable 1 : Enable	1'b0
		0	R/W	OTP_EN	Over-temperature protection enable: 0 : Disable 1 : Enable	1'b0
0x2A	1	7	R/W	OTPPRG_EN	OTP memory programming enable 0 : Disable 1 : Enable	1'b0
		6:0	-	Reserved	-	
0x2B	1	7:6	-	Reserved	-	
		5:0	R/W	CC_MAX	IDAC1 peak value	6'b0
0x2C	1	7:6	-	Reserved	-	
		5:0	R/W	OCP_CURR	IDAC1 6-bit ocp enable level	6'b0
0x30	1	7:4	R/W	SilenceRestTime	Silence reset time: 0 to 15 seconds	4'b0001
		3:0	R/W	sThresAct	Signal Active threshold: 0 to –90dB (sThresAct * -6dB)	4'b1010
0x31	1	7:6	-	Reserved	-	
		5:4	R/W	acqTimeSel	00 : 0.5s 01 : 1s 10 : 2s 11 : 4s	2'b01
		3:2	R/W	SigDectWin	Signal Detection Window 00 : 5ms 01 : 10ms 10 : 20ms 11 : 40ms	2'b10
		1:0	R/W	SToneRatio	Single Tone Ratio (To regard as single tone case) 00 : 2 01 : 4 10 : 8 11 : 16	2'b00

ADDR	Byte	Bits	R/W	Name	Description	Default
0x32	2	15:14	-	Reserved	-	
		13:9	R/W	delayGain[4:0]	The gain delay which is used to synchronize left channel and right channel	5'h00
		8:0	R/W	tDelay	Look-ahead delay samples The behavior is undefined if tDelay = 0	9'h64
0x33	1	7:2	-	Reserved	-	
		1:0	R/W	tAttackSel	Attack Time Selection : 00 : 0ms 01 : 0.1ms 10 : 0.2ms 11 : 0.3ms	2'b10
0x34	2	15:0	R/W	tRelease	Release Time constant (1-RT)	16'h7fce
0x35	2	15:0	R/W	tHoldRelease	Hold Release Time constant (1-RT)^tDelay	16'h6dd3
0x38	1	7:0	R/W	sThresLmt	Signal threshold for gain limiter 0 to 255/128, 0x80 normalized to 1	8'h80
0x39	1	7:0	R/W	xThresLmt	Excurstion threshold for gain limiter 0 to 255/128, 0x80 normalized to 1	8'h80
0x3A	1	7:0	R/W	sThresALC	Signal threshold for automatic gain controller 0 to 255/128, 0x80 normalized to 1	8'h40
0x3B	1	7:0	R/W	xThresALC	Excursion threshold for automatic gain controller 0 to 255/128, 0x80 normalized to 1	8'h40
0x3C	1	7:0	R/W	InitUpDoubleTime	Gain up double time for initial active 1/16 to 15.9375, 0x10 normalized to 1	8'h04
0x3D	1	7:0	R/W	UpDoubleTime	Gain up double time 1/16 to 15.9375, 0x10 normalized to 1	8'h10
0x3E	1	7:0	R/W	DnHalfTime	Gain down half time 1/16 to 15.9375, 0x10 normalized to 1	8'h40
0x3F	1	7	-	Reserved	-	
		6:4	R/W	ALCMaxGain	ALC maximum gain 0 to 21dB (ALCMaxGain * 3dB)	3'b111
		3	-	Reserved	-	
		2:0	R/W	ALCInitGain	ALC initial gain 0 to 21dB (ALCInitGain * 3dB)	3'b000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x40	1	7	-	Reserved	-	
		6:5	R/W	spsTh4Si	Scalable power stage threshold select for system identification	2'b11
		4	R/W	SglEn	Adaptation enabled in single-tone case 0 : disable 1 : enable	0
		3:2	R/W	SIBlocks	Adaptation blocks 00 : 8 01 : 16 10 : 32 11 : 64	2'b00
		1:0	R/W	SIOrd	Filter order 00 : 2 01 : 3 10 : 4 11 : 5	2'b01
0x41	1	7:0	R/W	InitImpIDMu	Initial adaptation step size 1/128 to 255/128	8'h04
0x42	1	7:0	R/W	ImpIDMu	Normal adaptation step size 1/2048 to 255/2048	8'h02
0x43	1	7:0	R/W	gPilot	Gain of pilot (in digital domain) 1/4096 to 255/4096 (gPilot*1/16); gPilot = 1/256 to 255/256	8'h11
0x44	1	7:2	R/W	TRXdelay[5:0]		0
		1	R/W	slPilotEN	Pilot enable in silence mode	0
		0	R/W	PilotEN	Pilot enable	0
0x45	1	7	-	Reserved	-	
		6:4	R/W	PilotScale	Scale-up factor = 2^PilotScale to scale up the output of HPF to extract the pilot	0
		3	R/W	iSenseInv	inverse the sign of the current sensing data	0
		2:0	R/W	iSenseScale	Scale-up factor = 2^iSenseScale to let CRx/CTx in the range of [1, 2) at calibration phase	0
0x46	3	23:0	R/W	iSenseGain	Gain of current sense loop, normalized to 32Ω Read/Write to OTP if SenseGPGMEN = 1 Read/Write to local register if SenseGPGMEN = 0	24'h800000
0x47	3	23:0	R/W	Rapp	Application resistance, normalized to 32Ω	0
0x48	1	7:0	R/W	rMaxExcess	Maximum allowable DCR growth ratio 1/256 to 255/256	0
0x49	2	15:11	-	Reserved	-	
		10:8	R/W	PdictWeightExp	PdictWeight = PdictWeightMant * 2^PdictWeightExp PdictWeightExp = 0 to 7	3'h7
		7:0	R/W	PdictWeightMant	1/128 to 255/128, 0x80 normalized to 1	8'h80

ADDR	Byte	Bits	R/W	Name	Description	Default
0x4A	2	15:10	-	Reserved	-	
		9:8	R/W	KpExp	Kp = KpMant * 2^KpExp KpExp = 0 to 3	2'h3
		7:0	R/W	KpMant	1/128 to 255/128, 0x80 normalized to 1	8'h80
0x4B	1	7:0	R/W	KiKpRatio	The ratio of Ki/Kp 1/256 to 255/256	8'h3
0x4C	1	7:0	R/W	InitDCRIDMu	Initial adaptation step size 1/256 to 255/256	8'h40
0x4D	1	7:0	R/W	DCRIDMu	Normal adaptation step size 1/1024 ~ 255/1024	8'h04
0x4E	3	23:0	R/W	CalibDCR	Factory calibrated DC resistor Read/Write to OTP if DCRPGEN = 1 Read/Write to local register if DCRPGEN = 0	24'h800000
0x4F	2	15:0	R/W	CalibBL	Factory calibrated BL factor Read/Write to OTP if BLPGEN = 1 Read/Write to local register if BLPGEN = 0 CalibBL = reg[0x4f] / 2^15	16'h4000
0x50	1	7	R/W	CalibEn	Trigger the calibration to start; self-cleared	0
		6	R/W	BGVMSK	BGV mask : select the internal used BGV to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		5	R/W	VBATGAINMSK	VBAT GAIN mask : select the internal used VBAT GAIN to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		4	R/W	VTEMPMSK	VTEMP GAIN mask : select the internal used VTEMP GAIN to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		3	R/W	DCRMSK	DCR mask : select the internal used CalibDRC to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		2	R/W	BLMSK	Bl Factor mask : select the internal used CalibBL to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		1	R/W	SGMSK	Sense Gain mask : select the internal used iSenseGain to be from OTP or from register setting. 0 : from OTP 1 : from Register	0
		0	R	CalibRDY	The calibration output is ready for software reading	0

ADDR	Byte	Bits	R/W	Name	Description	Default
0x51	2	15:0	R/W	CalibReq	Calibration frequency = round (2*f_Hz /fs*65536); fs = 48000	0
0x52	2	15:0	R/W	GalibGain	Gain of the signal, ranged in [0,1), bit[15] is sign-bit and should be 0 for positive value	0
0x53	4	31:0	R	CalibOut0	Output #1 of calibration data	
0x54	4	31:0	R	CalibOut1	Output #2 of calibration data	
0x55	1	7:0	R/W	xThresLmtDamage	Excursion threshold for gain limiter when damage mode is detected 1/128 to 1, 0x80 normalized to 1	8'h1a
0x56	1	7:0	R/W	rMaxDamage	Maximum allowable DCR growth ratio to regard coil as damaged 1/256 to 255/256	8'hcd
0x57	1	7:0	R/W	fScaleDamge	If the value of SetResFreq/GetResFreq or GetResFreq/SetResFreq is less than this factor, then the diaphragm is regarded as damaged fScaleDamge represents : 1/256 to 255/256	8'h80
0x58	1	7:4	-	Reserved	-	
		3:0	R/W	RecoveryTime	The time to exit the damage mode after the RMAXDMGE or FSCALDMGE criteria is no longer violated. Range for 0 to 15s	0
0x59	2	15:0	R/W	SetResFreq	Preset resonant frequency for damage detection SetResFreq = round(2*fres /fs*65536); fs = 48000	16'h889
0x5A	2	15:0	R	GetResFreq	Estimated resonant frequency fres (Hz) = GetResFreq/65536 *fs/2	
0x5B	1	7:3	-	Reserved	-	
		2:0	R/W	VOLCTRL	Ramp control when new volume setting is different from old setting : 000: No ramp up/down 001 : 0.5dB per 4 samples 010 : 0.5dB per 8 samples 011 : 0.5dB per 16 samples 100 : 0.5dB per 32 samples 101 : 0.5dB per 64 samples Others : reserved	3'b001
0x5C	1	7:0	R/W	VOLUME	Volume, downward 0 to −127.5dB in −0.5dB step	0
0x5D	4	31:0	R	CalibOutX	Output #2 of calibration X data	
0x5E	4	31:0	R	CalibOutY	Output #2 of calibration Y data	
0x60	20	159:128	R/W	bq_1_b0	u[31:26], b0[25:0]	32'h00000000
		127:96	R/W	bq_1_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_1_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_1_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_1_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x61	20	159:128	R/W	bq_2_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_2_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_2_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_2_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x62	20	159:128	R/W	bq_3_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_3_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_3_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_3_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_3_a2	u[31:26], a2[25:0]	32'h00000000
0x63	20	159:128	R/W	bq_4_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_4_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_4_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_4_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_4_a2	u[31:26], a2[25:0]	32'h00000000
0x64	20	159:128	R/W	bq_5_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_5_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_5_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_5_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_5_a2	u[31:26], a2[25:0]	32'h00000000
0x65	20	159:128	R/W	bq_6_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_6_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_6_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_6_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_6_a2	u[31:26], a2[25:0]	32'h00000000
0x66	20	159:128	R/W	bq_7_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_7_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_7_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_7_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_7_a2	u[31:26], a2[25:0]	32'h00000000
0x67	20	159:128	R/W	bq_8_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_8_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_8_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_8_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_8_a2	u[31:26], a2[25:0]	32'h00000000
0x68	20	159:128	R/W	bq_9_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_9_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_9_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_9_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_9_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x69	20	159:128	R/W	bq_10_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_10_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_10_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_10_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_10_a2	u[31:26], a2[25:0]	32'h00000000
0x6A	20	159:128	R/W	VB_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_1_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_1_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x6B	20	159:128	R/W	VB_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_2_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_2_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x6C	20	159:128	R/W	VB_bq_3_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_3_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_3_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_3_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_3_a2	u[31:26], a2[25:0]	32'h00000000
0x6D	20	159:128	R/W	VB_bq_4_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_4_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_4_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_4_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_4_a2	u[31:26], a2[25:0]	32'h00000000
0x6E	20	159:128	R/W	VB_bq_5_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_5_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_5_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_5_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_5_a2	u[31:26], a2[25:0]	32'h00000000
0x6F	20	159:128	R/W	VB_bq_6_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_6_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_6_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_6_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_6_a2	u[31:26], a2[25:0]	32'h00000000
0x70	20	159:128	R/W	VB_bq_7_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_7_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_7_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_7_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_7_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x71	20	159:128	R/W	VB_bq_8_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_8_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_8_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_8_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_8_a2	u[31:26], a2[25:0]	32'h00000000
0x72	20	159:128	R/W	VB_bq_9_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	VB_bq_9_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	VB_bq_9_b1	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	VB_bq_9_b1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	VB_bq_9_a2	u[31:26], a2[25:0]	32'h00000000
0x73	24	191:160	R/W	VB_fcn_a0	u[31:26], a0[25:0]	32'h00800000
		159:128	R/W	VB_fcn_a1	u[31:26], a1[25:0]	32'h00000000
		127:96	R/W	VB_fcn_a2	u[31:26], a2[25:0]	32'h00000000
		95:64	R/W	VB_fcn_b0	u[31:26], b0[25:0]	32'h00800000
		63:32	R/W	VB_fcn_b1	u[31:26],b1[25:0]	32'h00000000
		31:0	R/W	VB_fcn_b2	u[31:26], b2[25:0]	32'h00000000
0x74	4	31:0	R/W	VB_GAIN_1[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x75	4	31:0	R/W	VB_GAIN_2[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x76	4	31:0	R/W	VB_GAIN_3[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x77	4	31:0	R/W	VB_GAIN_4[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x78	4	31:0	R/W	VB_GAIN_5[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x79	4	31:0	R/W	VB_GAIN_6[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x7A	4	31:0	R/W	VB_GAIN_7[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x7B	4	31:0	R/W	VB_GAIN_8[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x7C	4	31:0	R/W	VB_GAIN_9[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x7D	4	31:0	R/W	VB_GAIN_10[25:0]	u[31:26], gain1[25:0]	32'h00800000
0x7F	1	7:0	R/W	BW_COEFF[7:0]		8'h30

Analog Block Register

ADDR	Byte	Bits	R/W	Name	Description	Default
0x80	1	7	R/W	SW_RESET	1 : Software Reset	0
		0	-	Reserved	-	0
0x81	1	7:5	R/W	D_SPK_BOOST[2:0]	Class D gain control [000:110] = 0 to 15db/3db	3'b100
		4:0	R/W	D_SPKLPF_VOL[4:0]	PGA Feedback Gain control RF [0000~1111] = −31db to 0db/1db	4'b10111
0x82	1	1:0	R/W	D_PGA_SPKPGA_VOL[1:0]	PGA Input Gain control 00 = −6db 01 = −3db 10 = 0db 11 = 3db	2'b11
0x86	1	7	R/W	D_VMID_EN	VMID enable (AVDD/2)	0
		6	R/W	D_VMID_FAST	VMID quick charge	0
		5:4	R/W	D_ITH_OCP_BB[1:0]	Over-current threshold level of boost converter	2'b01
		3:0	R/W	D_IR_RAMP[3:0]	slop compensation select option	4'b1000
0x88	1	7	R/W	D_CS_EN	Current sense enable 1 = enable 0 disable	0
		6:5	R/W	D_CS_SEL[1:0]	CK_CS_CHP frequence selection 00 : 256K 01 : 128K 10 : 64K 11 : 32KHz	2'b00
		4:0	-	Reserved	-	
0x8A	1	7	R/W	D_BUF_EN	SPK_DAC buffer and CS_ADC buffer enable	0
		6	R/W	D_BIAS_EN	Analog V2I bias enable	0
		5	R/W	D_IMADC_DCHP_EN	IMADC chopper enable	0
		4	R/W	D_IMADC_EN	IMADC enable (Vbattery,temp and current DAC sense)	0
		3	R/W	D_IM_GAIN_SEL	IMADC PREAMP gain setting 1: X10, 0 : X5	0
		2:0	R/W	D_IPTAT_VAR[2:0]	IPTAT current select (8.0μA to 12.67μA) 011:10μA with 1.66μA delta	3'b011
0x8B	2	15:0	R/W	vbat_data[15:0]	read mode : read vbat_data value from vbt_sens write mode : when 0xC8 vbat_data_tst_en is set to 1, vbat_data is from this register	16'h0000
0x8C	2	15:0	R/W	vtherm_data[15:0]	read mode : read vtherm_data value from vbt_sens write mode : when 0xC8 vtherm_data_tst_en is set to 1, vtherm_data is from this register	16'h0000

ADDR	Byte	Bits	R/W	Name	Description	Default
0x8D	1	7:6	R/W	D_IB_CMP_OVP[1:0]	OVP option selection Delta = 3.125% 00 : 5.8V 01 : 6.0V 10 : 6.2V 11 : 6.4V	2'b01
		5	R/W	vbt_sense_auto_en	battery/temperature auto sense enable : 1 : enable battery/temperature auto sense 0 : disable	1'b0
		4:2	R/W	vbt_sense_time_sel[2:0]	battery/temperature sense period : 000 : sense every 16ms 001 : sense every 32ms 010 : sense every 64ms 011 : sense every 128ms 100 : sense every 256ms 101 : sense every 512ms 110 : sense every 1024ms 111 : sense every 2048ms	3'b0
		1:0	R/W	vbt_sense_clk_sel[1:0]	battery/temperature sense ADC clock frequency selection : 00 : 384KHz 01 : 192KHz 10 : 96KHz 11 : 48KHz	2'b0
0x90	1	7	R/W	D_CK_POR_EN	POR internal clcok generator enable	1
		6	R/W	D_DAC_CHP_EN	HP DAC Chopper enable	0
		5:4	R/W	D_IB_ADC_BUF[1:0]	Bias current option for ADC buffer ,01 = 50%, 10 = 100%, 11 = 150%	2'b01
		3	R/W	D_VBG_SEL_VREF	Bandgap Internal LDO reference select	1
		2:0	R/W	D_OTP_TSEL[2:0]	OTP threhold select,Option range = 98 to 182, Step = 13 to 10,Default = 138 (011)	3'b011
0x94	1	7	R/W	D_VBG_Double_SEL	Pre-LDO and Quick-Charge turn-on period during bandgap start-up, 0 : 2mSec/3mSec, 1 : 4mSec/6mSec	0
		6	R/W	D_VBG_EN	Bandgap enable	0
		5	R/W	DAC_CLK_INV	1 : Invert DAC clock	0
		4	R/W	DITH_EN	1 : Enable DAC SDM dither	0
		3:2	R/W	DITH_PWR[1:0]	Dither power option	2'b00
		1:0	R/W	SDM_SEL[1:0]	SDM type select 00: 3 level typ 1 01 : 3 level typ 2 10 : 2 level	2'b00

ADDR	Byte	Bits	R/W	Name	Description	Default
0x95	1	7	-	Reserved	-	
		6	R/W	DAC_SEL	1 : RHP_DAC_EN only, 0 : RHP_DAC_EN + LHP_DAC_EN	0
		5	R/W	ADC_HPF_EN	ADC high-pass filter enable	0
		4	R/W	ADC_CLK_INV	Only for FPGA. Invert the ADC_CLK port	0
		3	R/W	D_OTP_TM_EN	OTP test mode enable, change OTP Threshold level to 0 degree around	0
		2:0	-	Reserved	-	2'b00
0x96	1	7	R/W	ovp_prot_en	OVP protection enable : 1 : enable ovp protection 0 : disable	0
		6	R/W	uvp_prot_en	UVP protection eenable : 1 : enable uvp protection 0 : disable	0
		5	R/W	cd_ocp_prot_en	Class-D OCP protection enable : 1 : enable class-d ocp protection 0 : disable	0
		4:1	R/W	gpwm_lv_reg[3:0]	Digital GPWM setting for triangle Vp-p, 0000 : 0.5Vpp to 1111 : 1.1Vpp@30mVpp	4'h0
		0	R/W	gpwm_lv_source	digital GPWM setting source : 0 : from digital state machine 1 : from register 0x96[4:1]	0
0x97	1	0	R/W	PLL_FREERUN	1 : PLL free run mode	1'b1
0x9a	1	7	R/W	bypass_vsettle	Enable to bypass vref_settle for internal dcm_en	1
		6	R/W	bypass_il0	Enable to bypass iL0 for internal dcm_en	1
		5:4	R/W	PLL_BW_RATIO	Kp / Ki ratio : 2'b00 -> Kp = 1; Ki = 1/8 2'b00 -> Kp = 1; Ki = 1/16 2'b00 -> Kp = 1; Ki = 1/32 2'b00 -> Kp = 1; Ki = 1/64	2'b01
		3	R/W	PLL_DZONE_MODE	dead-zone mode: 1 : accumlate Kp path, larger BW. 0 : skip Ki path, smaller BW.	1'b1
		2	R/W	PLL_NDSM_MODE	DSM order for fractional-N mode 0 : 1st order 1 : 2nd order	1'b1
		1:0	R/W	PLL_REF_DIV[1:0]	Input reference frequency divided ratio 2'b00 -> FREF 2'b01 -> FREF/2 2'b10 -> FREF/4 2'b11 -> FREF/8	2'b00

ADDR	Byte	Bits	R/W	Name	Description	Default
0x9b	1	7:1	-	Reserved	-	
0x9c	4	31:29	-	Reserved	-	
		28:16	R/W	PLL_N_I	PLL frequency disivor, integer part. {PLL_N_I, PLL_N_F} is a unsigned number in u13.16 format, which specifies the ratio of nominal system clock (to 24MHz) over reference clock frequency.	13'h0008
		15:0	R/W	PLL_N_F	PLL frequency disivor, fractional part.	16'h0000
0x9F	1	7	-	Reserved	-	0
		6	R/W	I2S_LOSS_DET_EN	1 :Enable LRCK/BCK loss check	0
		5	R/W	I2C_TIME_OUT_SEL	1 : Reset Chip if I^2C timeout and Cheh function enable	0
		4	R/W	I2C_TIME_OUT	1 : Enable I^2C time out check	0
		3	R	BCK_LOSS	1 : BCK loss	0
		2	R	LRCK_LOSS	1 : LRCK loss	0
		1	R	OCPN_FLAG	CLASS-D output stage low-side OC flag	0
		0	R	OCPP_FLAG	CLASS-D output stage high-side OC flag	0

ADDR	Byte	Bits	R/W	Name	Description	Default
0xA2	1	7:6	-	Reserved	-	
		4:0	R/W	spk_rpt_sel[4:0]	0x00 : Limiter gain = spk_rpt * 16 0x01 : ALC gain = spk_rpt * 16 0x02 : Gain information = spk_rpt 0x03 : Voltage output w/o pilot = spk_rpt * 16 0x04 : Voltage output w/I pilot = spk_rpt 0x05 : Corrent sense result = spk_rpt 0x06 : (voltage output w/I pilot) * current sense = spk_rpt * 16 0x07 : ATC gain = spk_rpt * 16 0x08 : Voltage delay = spk_rpt * 16 0x09 : Estimated current = spk_rpt * 16 0x0a : Estimated current error = spk_rpt * 16 0x0b: Estimated velocity = spk_rpt * 16 0x0c: Estimated excursion = spk_rpt * 16 0x0d: Estimated Resistor = spk_rpt * 16 0x0e: Input signal peak = spk_rpt * 16 0x0f : Excursion peak = spk_rpt * 16 0x10 : phi1 = spk_rpt * 16π 0x11 : phi2 = spk_rpt * 16π 0x12 : phi3 = spk_rpt * 16π 0x13 : phi4 = spk_rpt * 16π 0x14 : phi5 = spk_rpt * 16π 0x15 : adaptive b0 = spk_rpt * 16 0x16 : adaptive b1 = spk_rpt * 16 0x17 : adaptive b2 = spk_rpt * 16 0x18 : adaptive b3 = spk_rpt * 16 0x19 : adaptive b4 = spk_rpt * 16 0x1a : adaptive b5 = spk_rpt * 16 0x1b : tx_data = spk_rpt 0x1c : rx_pilot = spk_rpt 0x1d : tx_pilot = spk_rpt 0x1e : Digital maximum allowable absolute data = spk_rpt * 16 0x1f : single_tone = spk_rpt[23] active = spk_rpt[22] silence = spk_rpt[21] dmgRes = spk_rpt[20] dmgFreq = spk_rpt[19] damage = spk_rpt[18] acq = spk_rpt[17] spkE = spk_rpt[16] cntr10ms = spk_rpt[8:0]	5'h02
0xA3	3	23:0	R	spk_rpt[23:0]		

ADDR	Byte	Bits	R/W	Name	Description	Default
0xA4	3	23:0	R/W	nDelay[23:0]	The delay added to the output voltage of SPKFB for synchronization. nDelay = reg[0xa4] / 2^21 The range is [-2, 3) with 21 fractional bits.	0
0xA5	3	23:0	R/W	res[23:0]	The initial value of the parameter which is propotional to the resistance. Resistance = reg[0xa5] / 2^23 The range is [0, 2) with 23 fractional bits.	24'h800000
0xA6	3	23:0	R/W	phi1[23:0]	The initial value of the radians for the adaptive filter. The radians π/2 is normalized to 1/2, and the range is [-0.5, 0.5] with 23 fractional bits. Phi1 = reg[a6] / 2^23 * pi	24'hC4266F
0xA7	3	23:0	R/W	phi2[23:0]		24'h345F58
0xA8	3	23:0	R/W	phi3[23:0]		24'hFE21CB
0xA9	3	23:0	R/W	phi4[23:0]		24'h000000
0xAA	3	23:0	R/W	phi5[23:0]		24'h000000
0xAB	3	23:0	R/W	Adptive_b0[23:0]	The initial value of the expansion coefficient for the adaptive filter. The range is [-2, 2) with 22 fractional bits. B0 = reg[ab] / 2^22	24'h10221
0xAC	3	23:0	R/W	Adptive_b1[23:0]		24'hF1EBC8
0xAD	3	23:0	R/W	Adptive_b2[23:0]		24'h33BD58
0xAE	3	23:0	R/W	Adptive_b3[23:0]		24'h309E9
0xAF	3	23:0	R/W	Adptive_b4[23:0]		24'h000000
0xB0	3	23:0	R/W	Adptive_b5[23:0]		24'h000000
0xB3	1	7:5	-	Reserved	-	
		4:3	R/W	selMinAtc	The minimum value of the ATC gain 0 : 1/16 1 : 1/8 2 : 1/4 3 : 1/2	2'b0
		2	R/W	disMinAtc	Disable the minimum limitation of the ATC gain	1'b0
		1	R/W	D_VBG_PLDO_ON		1'b0
		0	R/W	R_AD_DITH_EN	Current sense ADC dither enable	1'b0
0xB4	1	7	R/W	OTP_PLL_LOCK_IGNORE	Access MTP memory without PLL lock	0
		6:4	-	Reserved	-	
		3	R/W	TDM_EN	I^{2}S TDM enable bit	0
		2	R/W	TDM_ADC_SEL	I^{2}S ADC TDM slot selection	0
		1	R/W	TDM_DAC_SEL	I^{2}S DAC TDM slot selection	0
		0	R/W	dcrEstInSilMod	Do DCR estimation when act signal is not logic 0	0

ADDR	Byte	Bits	R/W	Name	Description	Default
0xB5	1	7	R/W	D_SPK_VREF_OCP_SEL	OCP protection threshold level 0 : 1.8A 1 : 2.4A	0
		6	R/W	D_SPK_OCP_ANA_EN	OCP protection sequence for discharge enable	1
		5:2	R/W	D_IB_DAC	See the bit 1 of reg[0xB5].	0
		1	R/W	MODE_IB_DAC	reg[0xB5] instead of the data from OTP memory	0
		0	R/W	D_VBG_BUF_EN_ECO	Used for VBST trim	0
0xC0	1	7	R/W	otp_access_en	Enable otp access	4'h0
		6	-	Reserved	-	
		5	R	otp_pon_rdy	OTP power on auto load ready	1'b0
		4:3	R/W	otp_byte_num[1:0]	otp access byte number 00: 1byte, 01: 2bytes, 10: 3bytes, 11: 4bytes	2'b00
		2	R/W	otp_wr	0 : read, 1 : write	1'b0
		1:0	R/W	otp_acmr[1:0]	00 : normal read/write 01 : accelerated program mode 10 : margin-1 read mode 11 : margin-2 read mode	2'b00
0xC1	2	15:11	-	Reserved	-	
		10:0	R/W	otp_init_addr[10:0]	otp access address	11'h0
0xC2	4	31:24	R/W	otp_din3[7:0]/otp_dout3[7:0]	Write mode : otp_din0~3 is written into OTP memory Read mode : OTP memory data is put into otp_dout0~3	8'b0
		23:16	R/W	otp_din2[7:0]/otp_dout2[7:0]		8'b0
		15:8	R/W	otp_din1[7:0]/otp_dout1[7:0]		8'b0
		7:0	R/W	otp_din0[7:0]/otp_dout0[7:0]		8'b0
0xC3	1	7:5	-	Reserved	-	0
		4:0	R/W	D_VBG_TRIM[4:0]	Trim bits of BandGap	5'h10
0xC4	2	15:0	R/W	VTEMP_TRIM[15:0]	Calibration Result of VTEMP	0
0xC5	2	15:0	R/W	TCOEFF[15:0]	TC for iSense resistance	0
0xCF	1	7:0	R/W	DRC_MIN_GAIN[7:0]		8'hFF
0xD0	1	7:4	-	Reserved	-	2'b00
		3:0	R/W	DRC_SET_SEL[3:0]	0000 : DRC1 0001 : DRC2 0010 : DRC3 0011 : DRC4 0100 : DRC5 Other : no define	4'h0

ADDR	Byte	Bits	R/W	Name	Description	Default
0xD1	16	127:122	-	Reserved	-	
		121:96	R/W	DRC_AE	DRC_AE[25:0]	26'h0800000
		95:90	-	Reserved	-	
		89:64	R/W	DRC_1_AE	DRC_1_AE[25:0]	26'h0000000
		63:58	-	Reserved	-	
		57:32	R/W	DRC_AA	DRC_AA[25:0]	26'h0800000
		31:26	-	Reserved	-	
		25:0	R/W	DRC_AD	DRC_AD[25:0]	26'h0800000
0xD2	7	55	R/W	DRC_RMS	0 : RMS 1 : Peak	0
		54:52	R/W	DRC_KNEE[2:0]		3'b000
		51:50	-	Reserved	-	
		49:40	R/W	DRC_TH0[9:0]	1. 0 to −127dB, 0.125dB per step 2. 10'h000 is 0dB 3. Value definiton is 7.3	10'h000
		39:34	-	Reserved	-	
		33:24	R/W	DRC_TH1[9:0]	1. 0 to −127dB, 0.125dB per step 2. 10'h000 is 0dB	10'h000
		23:16	R/W	DRC_OFF[7:0]	1. +24dB to −24dB 2. 0.25dB per step 3. Value definiton is 6.2, MSB is sign bit.	8'h00
		15:13	-	Reserved	-	
		12:8	R/W	DRC_R0[4:0]	1. 0 to 1 2. 5'h10 is 1	5'h10
		7	-	Reserved	-	
		6:0	R/W	DRC_R1[6:0]	1. 1 to 8 2. 7'h10 is 1	7'h10
0xD3	20	159:128	R/W	bq_1_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_1_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_1_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_1_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0xD4	20	159:128	R/W	bq_2_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_2_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_2_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_2_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0xD5	20	159:128	R/W	bq_3_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_3_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_3_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_3_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_3_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte	Bits	R/W	Name	Description	Default
0xD6	20	159:128	R/W	bq_4_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_4_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_4_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_4_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_4_a2	u[31:26], a2[25:0]	32'h00000000
0xD7	20	159:128	R/W	bq_5_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_5_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_5_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_5_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_5_a2	u[31:26], a2[25:0]	32'h00000000
0xD8	20	159:128	R/W	bq_6_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_6_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_6_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_6_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_6_a2	u[31:26], a2[25:0]	32'h00000000
0xD9	20	159:128	R/W	bq_7_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_7_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_7_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_7_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_7_a2	u[31:26], a2[25:0]	32'h00000000
0xDA	20	159:128	R/W	bq_8_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_8_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_8_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_8_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_8_a2	u[31:26], a2[25:0]	32'h00000000
0xDB	20	159:128	R/W	bq_9_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_9_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_9_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_9_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_9_a2	u[31:26], a2[25:0]	32'h00000000
0xDC	20	159:128	R/W	bq_10_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_10_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_10_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_10_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_10_a2	u[31:26], a2[25:0]	32'h00000000
0xDD	20	159:128	R/W	bq_11_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_11_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_11_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_11_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_11_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte	Bits	R/W	Name	Description	Default
0xDE	20	159:128	R/W	bq_12_b0	u[31:26], b0[25:0]	32'h00800000
		127:96	R/W	bq_12_b1	u[31:26], b1[25:0]	32'h00000000
		95:64	R/W	bq_12_b2	u[31:26], b2[25:0]	32'h00000000
		63:32	R/W	bq_12_a1	u[31:26], a1[25:0]	32'h00000000
		31:0	R/W	bq_12_a2	u[31:26], a2[25:0]	32'h00000000
0xDF	2	15	R/W	DC_CUT_FILTER_DIS	1 : Disable DC-Cut filter	0
		14	R/W	H_BAND_BYPASS	1 : Bypass High band DRC	0
		13	R/W	M_BAND_BYPASS	1 : Bypass Middle band DRC	0
		12	R/W	L_BAND_BYPASS	1 : Bypass Low band DRC	0
		11:10	-	Reserved	-	
		9	R/W	SideChain_2_ON	1 : Enable sidchain for low band DRC	0
		8	R/W	SideChain_1_ON	1 : Enable sidchain for Middle band DRC	0
		7:5	-	Reserved	-	0
		4	R/W	DRC5_EN	1 : DRC5 enable	0
		3	R/W	DRC4_EN	1 : DRC4 enable	0
		2	R/W	DRC3_EN	1 : DRC3 enable	0
		1	R/W	DRC2_EN	1 : DRC2 enable	0
		0	R/W	DRC1_EN	1 : DRC1 enable	0
0xF4	1	7	R/W	FDRC_CK_EN	1 : Enable FDRC block clock	1
		6	R/W	BOOST_CK_EN	1 : Enable BOOST block clock	1
		5	R/W	ADC_CK_EN	1 : Enable ADC block clock	1
		4	R/W	DAC_CK_EN	1 : Enable DAC block clock	1
		3	R/W	SSRC_CK_EN	1 : Enable SSRC block clock	1
		2	R/W	DSP_CK_EN	1 : Enable DSP block clock	1
		1	R/W	SPK_CK_EN	1 : Enable SPK Protection block clock	1
		0	R/W	ANA_CK_EN	1 : Enable Analog block clock	1
0xF5	1	7:2	-	Reserved	-	6'h00
		1	R/W	SAFE_GUARD_CK_EN	1 : Enable SAFE Guard block clock	1
		0	R/W	CAL_CK_EN	1 : Enable Cal block clock	1

Application Information

Inductor Selection

The recommended value of inductor for DC-to-DC boost converter applications is 1μH. Small size and better efficiency are the major concerns for portable devices, such as the RT5508 used for mobile phone. The inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency. The minimum effective inductance should be higher than 0.7μH.

The maximum current of inductor is highly depends on the speaker impedance which determines the output current of the boost converter. The inductor saturation current rating should be considered to cover the inductor peak current which can be approximated by the following equation :

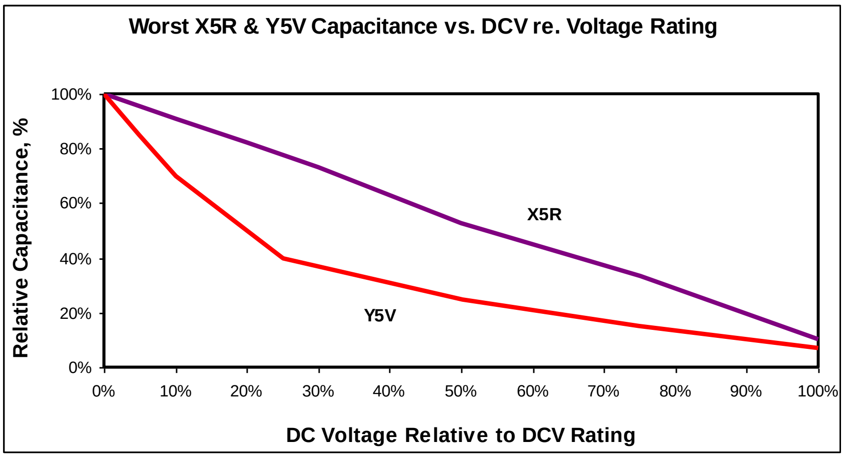
$$I_{L\_max} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}$$

Following is the inductor selection reference for typical speaker impedances with 10% tolerance and 95% efficient.

R_L (Ω)	I_{OUT} (A)	$I_{L(max)}$ (A)	Manufacturer	Part Number
8	1.14	1.43	Murata	MDT2520-CN1ROM
6	1.52	1.81	Coilcraft	PFL2512-102MEB
4	2.28	2.57	Coilcraft	LPS4012-102NLB

Capacitor Selection

For low ripple voltage, ceramic capacitors with low ESR are recommended. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. X5R and X7R types are suitable because of their wide voltage range and good operating temperature characteristics. The capacitance value decreases over the DC-biasing voltage range (30% to 70% decrease) as following figure. Consequently, the nominal DC rating of the capacitor should be close to twice the maximum application voltage value. When select capacitor, please notice the DC bias characteristics. The RT5508 minimum effective C_{VBST} capacitance should be higher than 6μF.



The output ripple can be determined as following equation :

$$\Delta V_{OUT} = \frac{D \times I_{OUT} \times T_S}{\eta \times C_{OUT}} + \left(\frac{I_{OUT}}{1\text{-}D} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}\right) \times r_{C\_esr}$$

For the application of the RT5508 to boost VBAT to 5.3V, a 10μF for input capacitor, an 22μF for boost capacitor and a 100nF for DVDD decoupling capacitor are recommended.

R_L (Ω)	Value (μF)	Manufacturer	Part Number	Description	Size/Height (mm)
8	10 (2pcs)	Murata	GRM188R61E106M	X5R/15%/25V	0603/0.8
8	22	Murata	GRM219R61C226ME15	X5R/15%/16V	0805/0.85
6	10 (2pcs)	Murata	GRM188R61E106M	X5R/15%/25V	0603/0.8
6	22	Murata	GRM219R61C226ME15	X5R/15%/16V	0805/0.85

Filter Free Operation and Ferrite Bead Filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. Typically, impedance rises over 150Ω before 30MHz to provide at least −20dB decade is minimum requirement (such as TDK : MPZ1608S221A). In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

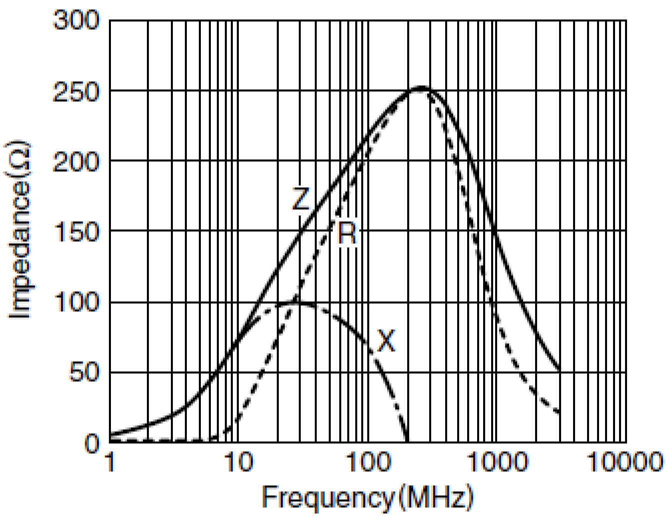


Figure 24

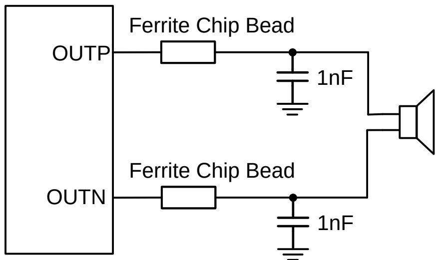


Figure 25

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For WL-CSP-29B 2.87x2.07 (BSC) package, the thermal resistance, θ_{JA}, is 33.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (33.5°C/W) = 3W for a WL-CSP-29B 2.87x2.07 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 26 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

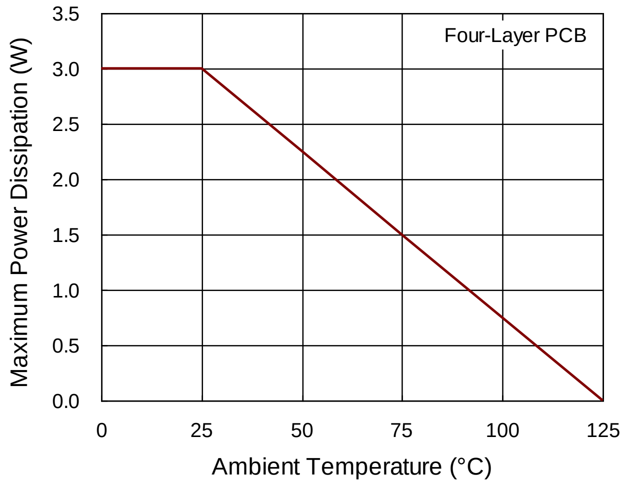


Figure 26. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RT5508, the below PCB Layout guidelines must be strictly followed.

Place the decoupling capacitors as close as possible to the DVDD pins. For achieving a good quality.

The traces of OUTA and OUTB should be kept equal width and length respectively. The Bead+C should be placed close to chip for better EMI performance. The power trace of boost inductor is suggested to placed on the external layers for higher current capability. For the case of speaker impedance equal to 8Ω, trace width greater than 60mil is recommended. The speaker output trace width should be greater than 40mil and total length from chip to connector do not longer than 1cm to minimize the power loss on the PCB trace.

The via numbers determine the current capability. Typically, the boost converter trace need four via to handle the current requirement around 2A.

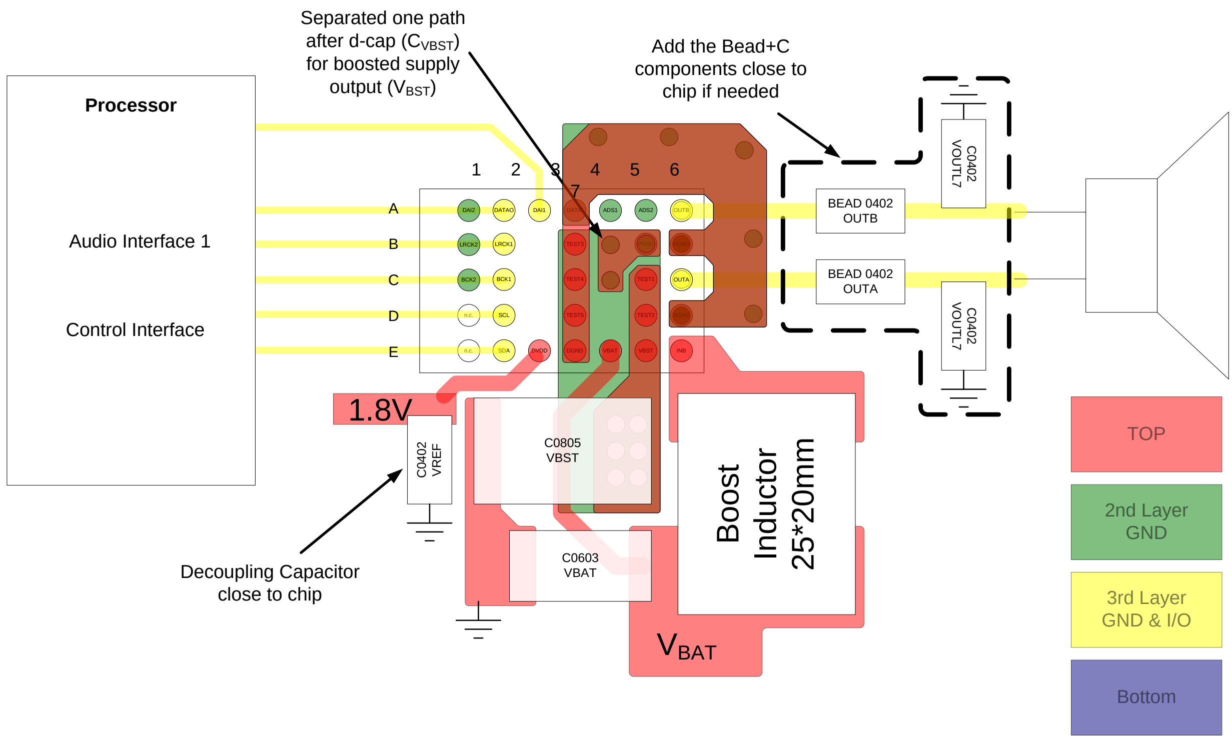
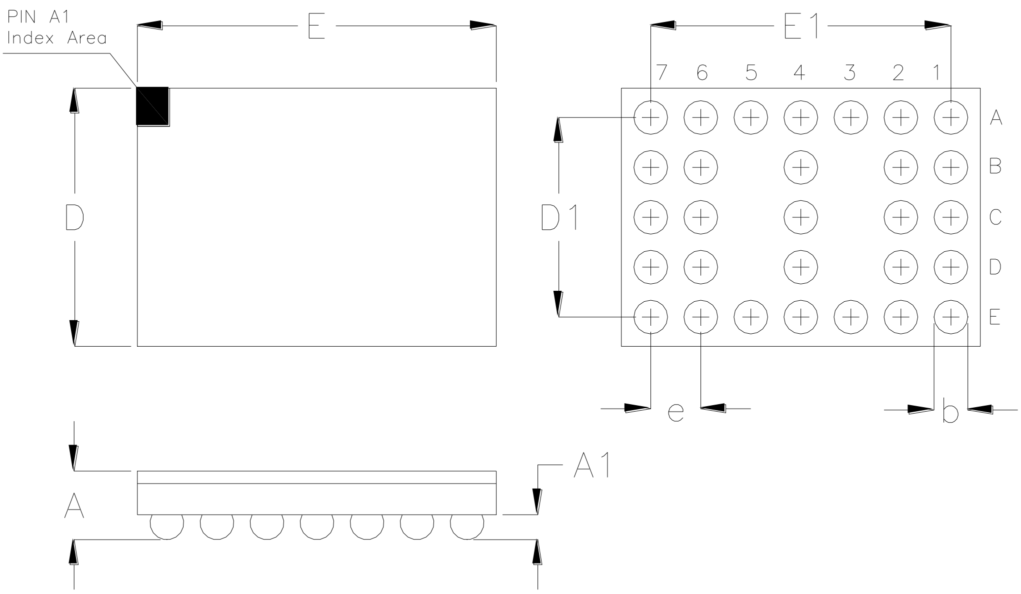


Figure 27. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.020	2.120	0.080	0.083
D1	1.600		0.063	
E	2.820	2.920	0.111	0.115
E1	2.400		0.094	
e	0.400		0.016	

29B WL-CSP 2.87x2.07 Package (BSC)

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