Audio Amplifier with IV Sense

General Description

The RT5512B is a boosted class-D amplifier with V/I sensing. A built-in DC-DC step-up converter is used to provide efficient power for class-D amplifier with multi-level class-H operation. The digital audio interface supports I^2S, left-justified, right-justified and TDM format for audio in with a data out used for chip information like voltage sense and current sense, which are able to be monitored via DATAO pin through proper register setting.

Applications

- Smart Phone, Tablet

Ordering Information

RT5512B□

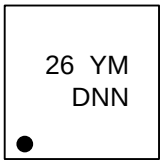
Package Type
WSC : WL-CSP-36B 2.57x2.57 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

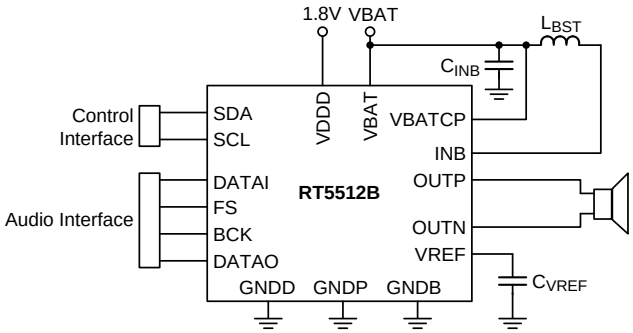


26 : Product Code
YMDNN : Date Code

Features

- **Class-D Speaker AMP**
  - **7W Output Power @ 12V, 8Ω load, THD+N < 1%**
  - **0 to 23dB Analog Gain**
  - **10μV Output Noise @ 18dB Gain**
  - **Add DRE to Reduce Output Noise**
  - **Min. R_L = 3.2Ω, Max. R_L = 38Ω**
- **Boost Converter**
  - **Adaptive Boost for Speaker, Boost from Battery Supply Up to Programmed Voltage, Max. 12.5V**
  - **Switching Frequency 2MHz**
  - **Accurate Input Current Limit**
  - **Analog Part : Feedback ADC, Current Sense, Slope Compensation**
  - **Digital Part : Voltage Loop and End-Point Prediction in Boost Mode**
- **V/I Sensing**
- **Digital**
  - **Digital Audio Interface Support I^2S, Left-Justified, Right-Justified, TDM**
  - **Flexible Interrupt Controller**
  - **Clip Control (Battery Safeguard) to Prevent Drawing Larger Current from Battery when Low VBAT**
  - **Volume Control**
- **RoHS Compliant and Halogen Free**

Simplified Application Circuit



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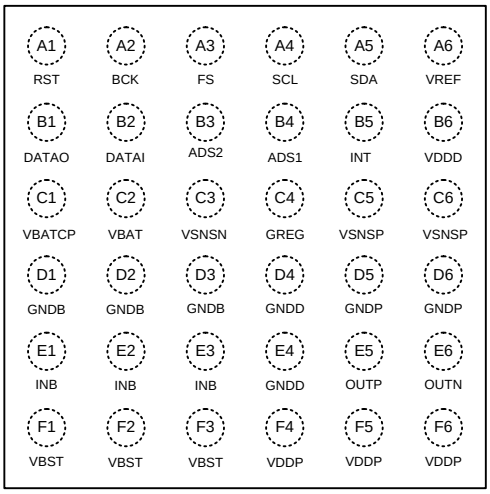
Pin Configuration

(TOP VIEW)



WL-CSP-36B 2.57x2.57 (BSC)

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
A1	RST	I	Hardware reset input, low active. Normally keep high level, go low level for hardware reset.
A2	BCK	I	I^2S interface bit clock data input.
A3	FS	I	I^2S interface word select data input.
A4	SCL	I	I^2C interface clock input, open drain structure. An external pull-up resistor 4.7kΩ is required.
A5	SDA	I/O	I^2C interface data input, open drain structure. An external pull-up resistor 4.7kΩ is required.
A6	VREF	I/O	Reference voltage output. An external capacitor 1μF is required.
B1	DATAO	O	I^2S interface digital audio data output.
B2	DATAI	I	I^2S interface digital audio data input.
B3	ADS2	I	Address select input 2, the RT5512B will latch the level of ADS2 once 768μs after the edge of RST pin goes from high to low or after I^2C write software reset for address select function.
B4	ADS1	I	Address select input 1.
B5	INT	O	Interrupt output, this pin is open-drain output.
B6	VDDD	P	Digital / analog supply voltage. An external capacitor 1μF is required.
C1	VBATCP	P	Battery supply voltage for charge pump.
C2	VBAT	P	Battery supply voltage. Connect 3V to 5.5V battery supply. An external capacitor 1μF is required.
C3	VSNSN	I	Voltage sense negative input.
C4	GREG	P	Gate driver supply voltage.

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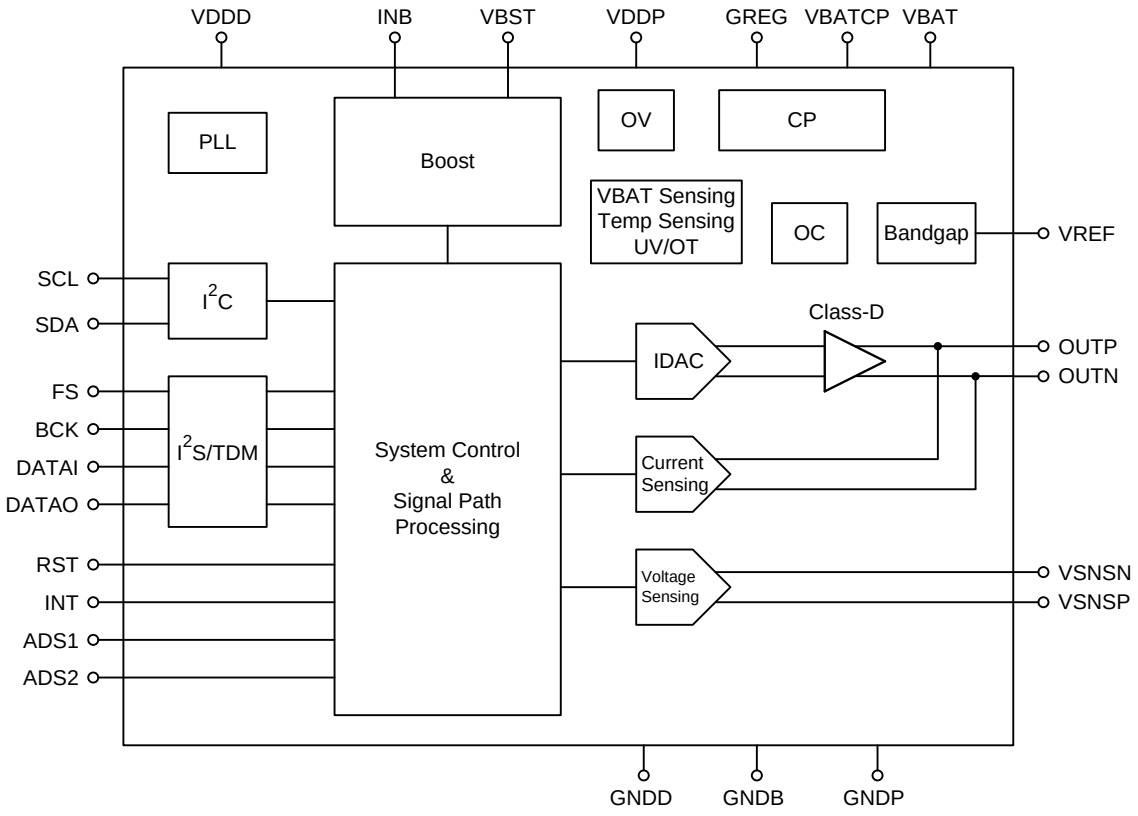
Pin No.	Pin Name	Type	Pin Function
C5, C6	VSNSP	I	Voltage sense positive input.
D1, D2, D3	GNDB	G	Boost converter ground.
D4, E4	GNDD	G	Digital ground.
D5, D6	GNDP	G	Ground for class-D amplifier.
E1, E2, E3	INB	P	Boost converter switch input node.
E5	OUTP	O	Class-D non-inverting output.
E6	OUTN	O	Class-D inverting output.
F1, F2, F3	VBST	P	Boost converter output voltage.
F4, F5, F6	VDDP	P	Class-D supply voltage. Voltage is provided by VBST pin. An external capacitor 30μF is required.

Functional Block Diagram



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Operation

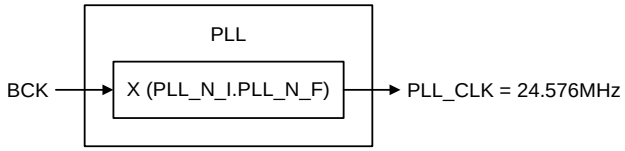
Class-D Audio Amplifier

The RT5512B is a 12V boosted class-D audio amplifier capable of delivering up to 7Wrms output power into an 8Ω speaker at a supply voltage of 3.8V. The audio amplifier features low noise (10μVrms). Signal gains are configurable through analog (IDAC_GAIN_SEL[4:0] 0 to 23dB, 1dB/step) and digital (VOLUME[7:0] 12 to −115.5dB, −0.5dB/step) circuits. Over-current protection with threshold of 3A is also implemented in the high efficiency bridge-tied-load (BTL) devices to provide additional protection alongside the current limit of boost converter. The 3-level PWM scheme supports filter-less speaker drive.

PLL

The on-chip PLL generates the 24.576MHz clock as the internal operating clock source. The PLL uses the BCK of I^2S interface as the reference clock and the programmability of the PLL allows the support of various sample rate of audio data, like 8k / 11.025k / 12k / 16k / 22.05k / 24k / 32k / 44.1k / 48k / 88.2k / 96kHz. Combining PLL_N_I and PLL_N_F forms an unsigned number in u13.16 format, which specifies the ratio of 24.576MHz clock over the reference clock, BCK.

$$PLL\_CLK = BCK \times (PLL\_N\_I + \frac{PLL\_N\_F}{2^{16}})$$



Over-Voltage Protection

The over-voltage (OV) protection can detect the over voltage fault on charge pump. The fault on the charge pump which cause VDDP in the range of 15.3V to 16.1V triggers the OV flag to the digital control system and disable the analog blocks by 200ms. After 200ms cooling time, the OV protection detects the voltage again to determinate if the OV event is finished.

Over-Current Protection

The over-current protection can detect the over-current fault on class-D. The fault on the class-D which causes a large current over 3A triggers the OC flag to the digital control system and disables the analog blocks by 200ms. After 200ms cooling time, the OC protection detects the current again to determinate if the OC event is finished.

Under-Voltage Protection

The under voltage protection can detect the under voltage fault on power supply VBAT. The UV flag is triggered when VBAT is lower than 2.3V, then digital control system disables the analog blocks by 200ms. After 200ms cooling time, the UV protection detects the voltage again to determinate if the UV event is finished.

Over-Temperature Protection

The over-temperature protection can detect the over-temperature fault on the chip. The OT protection is triggered when temperature sensed by Temp sense is higher than 160°C then the digital control system disables the analog blocks by 200ms. After 200ms cooling time, the OT protection detects the temperature again to determinate if the OT event is finished with the hysteresis threshold 130°C.

VBAT Sense

The VBAT sense monitors the battery voltage between the range from 2V to 6.375V with 10-bit resolution, the output is shown in the register “0x48 VBAT” with the equation battery voltage (V) = VBAT code (DEC) / 160.

Temp. Sensing

Temperature sense monitors the temperature of the chip with the range between −40°C to 175°C with 9 -bit resolution, the output is shown in the register 0x47 “VPTAT” with the equation code (DEC) = temperature (K) = temperature (°C) + 273.

Charge Pump

In order for the class-D amplifier to operate normally, the RT5512B has a charge pump inside. It would provide one high voltage source for class-D amplifier. Charge pump need an external capacitor around 10nF to stabilize the output voltage.

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Absolute Maximum Ratings (Note 1)

- VBST, VDDP ---------- –0.3 to 17V
- OUTP, OUTN, VSNSN, VSNSP, INB ---------- –0.3V to 17V
- VBAT, VBATCP ---------- –0.3V to 6V
- VDDD, VREF ---------- –0.3V to 2.5V
- FS, BCK, DATAI, DATAO, ADS1, ADS2, RST ---------- –0.3V to (VDDD + 0.3V)
- SCL, SDA, INT ---------- –0.3V to 6V
- GREG ---------- –0.3V to 22V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-36B 2.57x2.57 (BSC) ---------- 3.08W
- Package Thermal Resistance (Note 2)

  WL-CSP-36B 2.57x2.57 (BSC), θ_{JA} ---------- 32.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(Test condition : VBAT = VINB = 3.8V, VDDD = 1.8V, T_A = 25°C, load = 8Ω + 22μH, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System						
Digital Supply Voltage	VDDD		1.71	1.8	1.98	V
Battery Supply Voltage	V_{BAT}		3.0	3.8	5.5	V
Iq, Boost in Battery Mode DRE Mode, Reduced Bias (Note 5)	IQ_VBAT	VBAT and INB	--	6	--	mA
	IQ_VDDD	Analog part (VDDD = 1.8V)	--	5	--	mA
		Digital part (VDDD = 1.8V)	--	6.2	--	
ISD on VBAT	ISD_VBAT	V_{BAT} = 3.8V, VDDD = 1.8V	--	--	1	μA
ISD on VDDD	ISD_VDDD	V_{BAT} = 3.8V, VDDD = 1.8V	--	4	20	μA
ILEAK in Shipping Mode	I_{LEAK}	V_{BAT} = 4.2V, VDDD = 0V	--	--	1	μA

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System Efficiency	η	Po = 0.5W, including DC to DC converter, 1kHz audio signal	--	84	--	%
		Po = 1W, including DC to DC converter, 1kHz audio signal	--	86	--	
		Po = 0.5W, including DC to DC converter, 100Hz audio signal	--	85	--	
		Po = 1W, including DC to DC converter, 100Hz audio signal	--	87	--	
VDDP OVP	OVP_{VDDP}	VDDP rising	15.3	--	16.1	V
		Hysteresis (falling)	0.5	--	1.5	
Over-Temperature Protection	OTP	Temperature rising	150	160	170	°C
		Hysteresis (falling)	--	30	--	
Under-Voltage Protection	UVP	V_{BAT} falling	2.1	2.3	2.4	V
		Hysteresis (rising)	--	0.15	--	
Boost						
Boost Output Voltage	VBST		--	12	12.5	V
VBST Accuracy	ΔVBST		–0.1	--	0.1	V
Boost Voltage Step		Adjustable by register	--	0.1	--	V
Boost Switching Frequency	f_{SW}	CCM and DCM	--	2	--	MHz
		PSM	50	--	--	kHz
Inductor Current Limit	I_{lim}	Programmable by I^2C	4	--	7	A
Inductor Current Limit Accuracy		I_{lim} = 6A	–10	--	10	%
Class-D						
Maximum Output Power	Po	1kHz, VDDP = 12V, 8Ω load, 1% THD+N	7	--	--	W
		1kHz, VDDP = 12V, 32Ω load, 1% THD+N	1.7	--	--	
Full-Scale Output Voltage		Gain = 0dB	0.95	1	1.05	Vrms
		Gain = 18dB	7.6	8	8.4	
Output Gain	Gain range		0	--	23	dB
	Gain step		--	1	--	dB
	Gain error		--	--	0.5	dB
Output Offset Voltage	Vos	Gain = 18dB, A-weighting	--	1	3	mV
Output Noise	Vn	Class-D gain = 18dB, A-weighting	--	10	--	μV
		In DRE mode, class-D gain = 0 to 23dB, A-weighting	--	10	--	
Signal to Noise Ratio	SNR	VDDP = 12V, THD+N < 1%, A-weighting	--	117	--	dB
Dynamic Range	DR	–60dBFS, 1kHz signal	110	--	--	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	1kHz, Po = 0.5W, 8Ω load	--	–70	--	dB
		1kHz, Po = 1W, 8Ω load	--	–65	--	
Power Supply Rejection Ratio	$PSRR_{VDDP}$	217Hz, VDDP ripple = 200mVpp	70	90	--	dB
	$PSRR_{VBAT}$	217Hz, VBAT ripple = 200mVpp	70	90	--	dB
Class-D OCP			2.5	3	3.5	A
Output DC Protection		Trigger level, configurable by I^2C	0.5	1	2	V
		Trigger time, configurable by I^2C	100	500	1000	ms
Capacitive Load			--	--	1	nF
Current Sense						
Resolution			--	16	--	Bits
Accuracy		0.9A IPEAK, Freq = 20 to 20kHz	--	--	±1	%
Current Sense Gain Linearity		f = 1kHz from 7.3mAp to 1.3Ap (–45dBFS to 0dBFS), max. to min. gain	--	--	±2	%
		f = 1kHz from 1.3mAp to 7.3mAp (–60dBFS to –45dBFS), max. to min. gain	--	--	±3	%
Signal to Noise Ratio	SNR		--	60	--	dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, Po = 3W	--	–45	--	dB
Current Sense Full Scale		peak current which will give full scale digital output	–3	--	3	A
Path Delay Difference		Delay difference between V/I	--	--	1	μs
Voltage Sense						
Resolution			--	16	--	Bits
Accuracy		12V peak voltage, Freq = 20 to 20kHz	--	--	±1	%
Voltage Sense Gain Linearity		f = 1kHz from 60mVp to 10.6Vp (–45dBFS to 0dBFS)	--	--	±2	%
		f = 1kHz from 10.6mVp to 60mVp (–60dBFS to –45dBFS)	--	--	±3	%
Signal to Noise Ratio	SNR	A-weighting	--	80	--	dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, Po = 3W	--	–65	--	dB
Voltage Sense Full Scale			–16	--	16	V
Path Delay Difference		Delay difference between V/I	--	--	1	μs

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Battery Sense						
Resolution			--	10	--	Bits
Voltage Resolution			--	6.25	--	mV
Full Scale Input Voltage			--	6.375	--	V
Accuracy		V_{BAT} = 3.8V	–50	--	50	mV
I^2C Interface Electrical Characteristics (Note 6)						
SDA, SCL Input Threshold	V_{IH}		0.7 x VDDD	--	--	V
	V_{IL}		--	--	0.3 x VDDD	
Pull-Down Current	I_{FO2}		--	2	--	µA
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.6	--	--	µs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.6	--	--	µs
Stop Condition Time	$t_{SU,STD}$		0.6	--	--	µs
Data Hold Time	$t_{HD,DAT (OUT)}$		225	--	--	ns
Input Data Hold Time	$t_{HD,DAT (IN)}$		0	--	900	ns
Data Setup Time	$t_{SU,DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	µs
Clock High Period	t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	50	ns
I^2S Interface Electrical Characteristics (Note 6)						
High-Level Input Voltage	V_{IH}		0.7 x VDDD	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.3 x VDDD	V
Setup Time, FS to BCK Rising Edge	t_{su1}		10	--	--	ns
Hold Time, FS from BCK Rising Edge	t_{h1}		10	--	--	ns
Setup Time, DATAI to BCK Rising Edge	t_{su2}		10	--	--	ns
Hold Time, DATAI from BCK Rising Edge	t_{h2}		10	--	--	ns
Rise/fall Time for BCK/LRCLK	t_r		--	--	8	ns

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Note 1. Continuously stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 6. Guaranteed by design.

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Typical Application Circuit

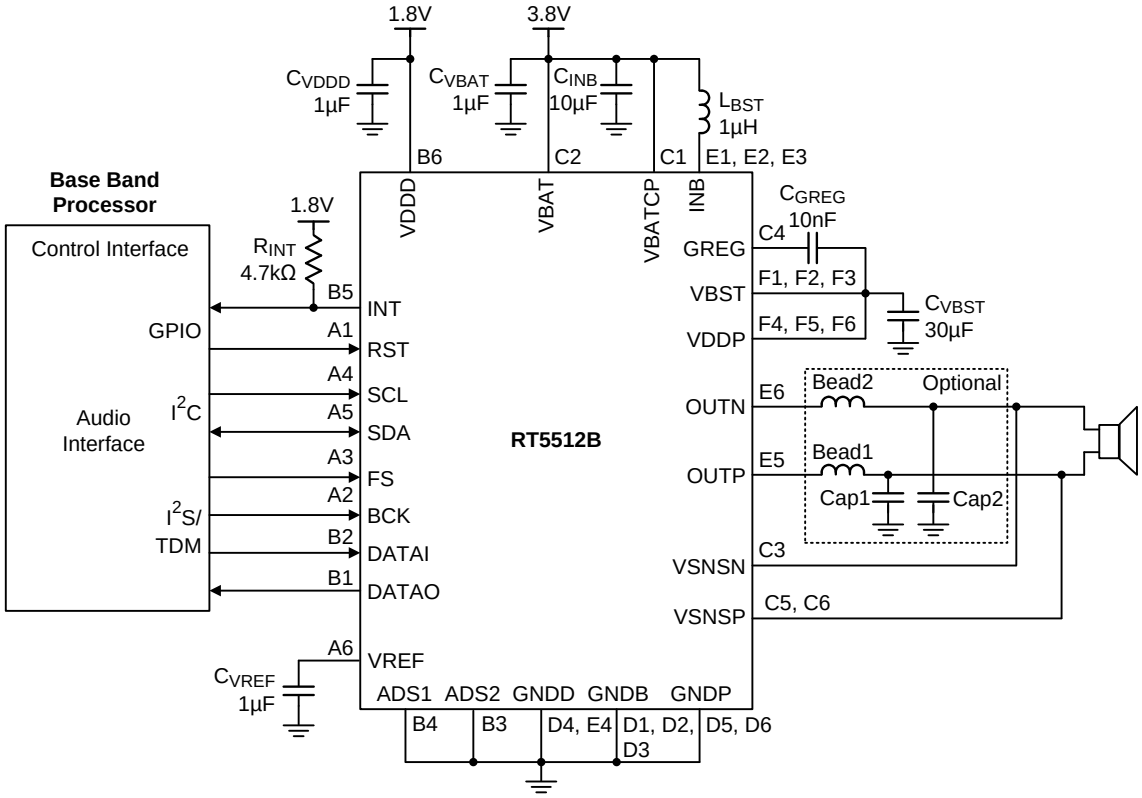

Table 1. Recommended Components Information

Reference	Part Number	Description	Package	Manufacturer
C_{INB}	GRM155R61A106ME11D	10µF, 10V, X5R	0402	murata
C_{VREF}, C_{VBAT}, C_{VDDD}	GRM033R60J105MEA2D	1µF, 6.3V, X5R	0201	murata
C_{GREG}	GRM155R71H103KA88	10nF, 50V, X7R	0402	murata
C_{VBST}	GRM188R61E106MA73D	10µF, 25V, X5R, 3pcs	0603	murata
L_{BST}	CIGT252010TM1R0MLE	1µH, 5.5A, 23mΩ, ±20%	2.5x2x1mm	Samsung
R_{INT}	RTT02472JTH	1/16W, 5%, 4.7kΩ	0402	RALEC
Bead1, Bead2	LQW15CN77NJ10D	77nH, 5%, 1.1A, 90mΩ,	0402	murata
Cap1, Cap2	GRM1555C1H151JA01	150pF, 50V, C0G	0402	murata

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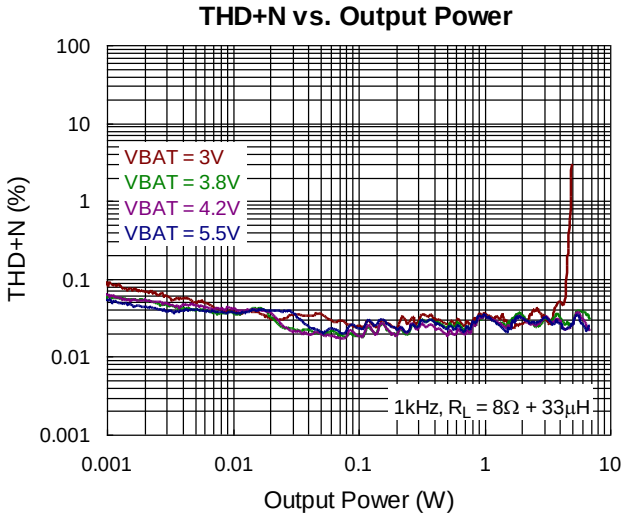
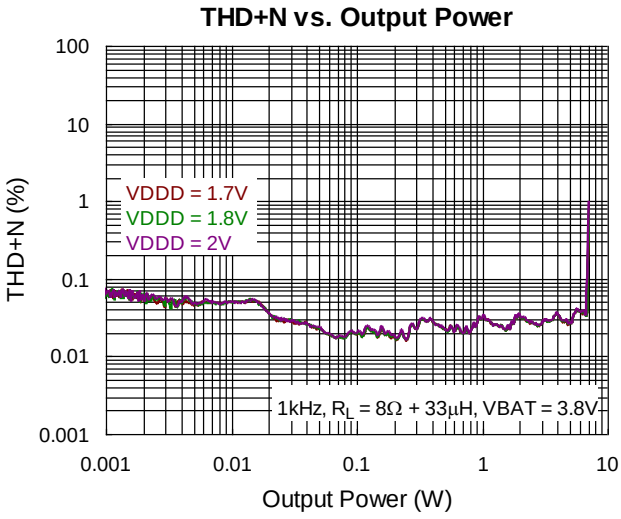
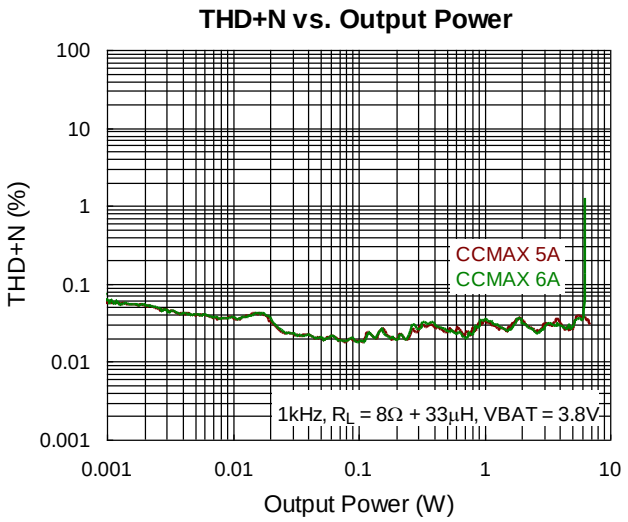
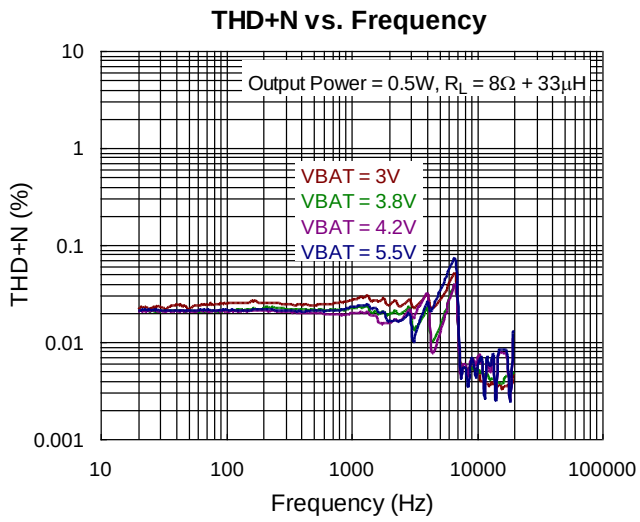
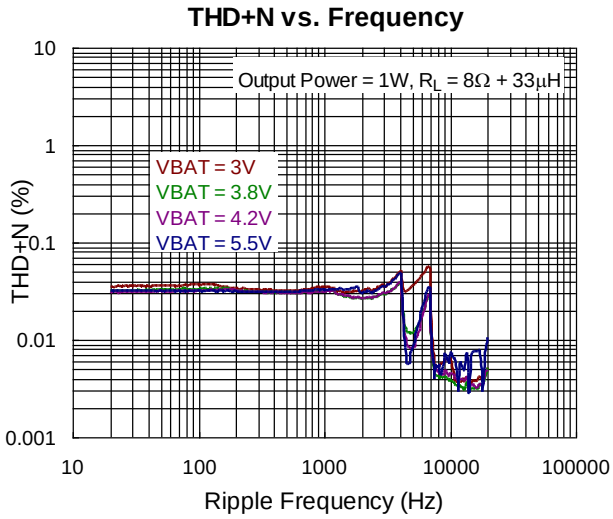
Typical Operating Characteristics

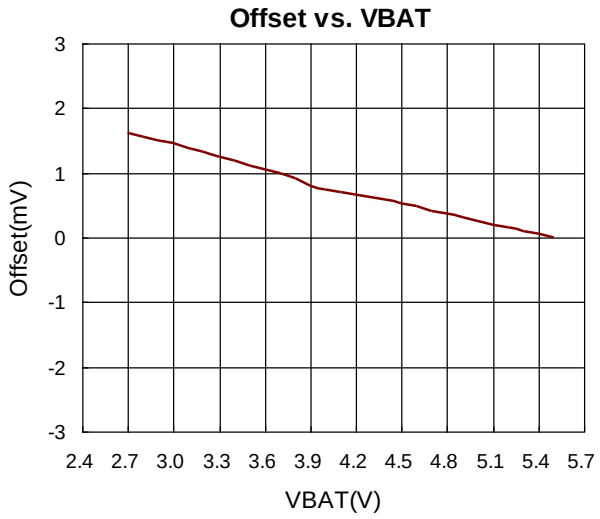












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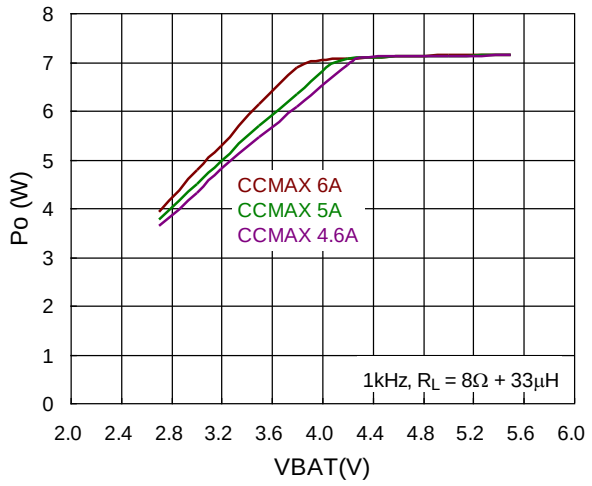
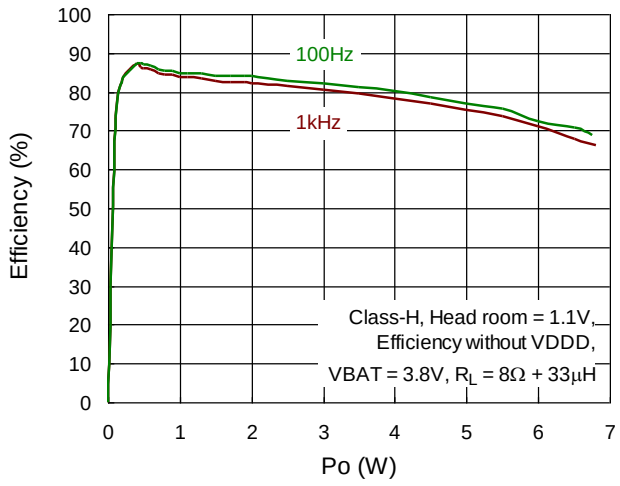
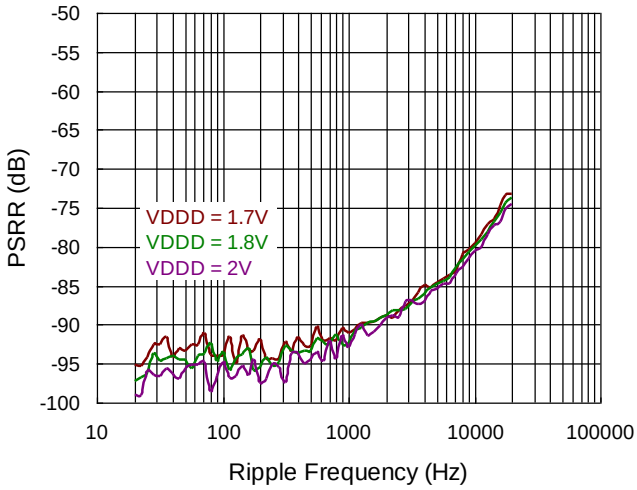
Output Power vs. VBAT



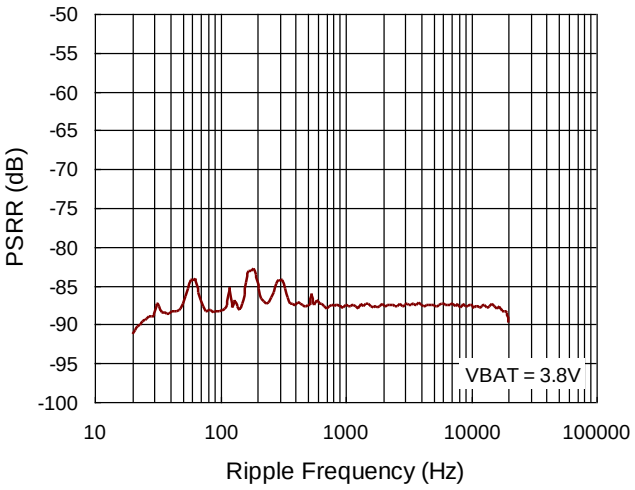
Efficiency vs. Output Power



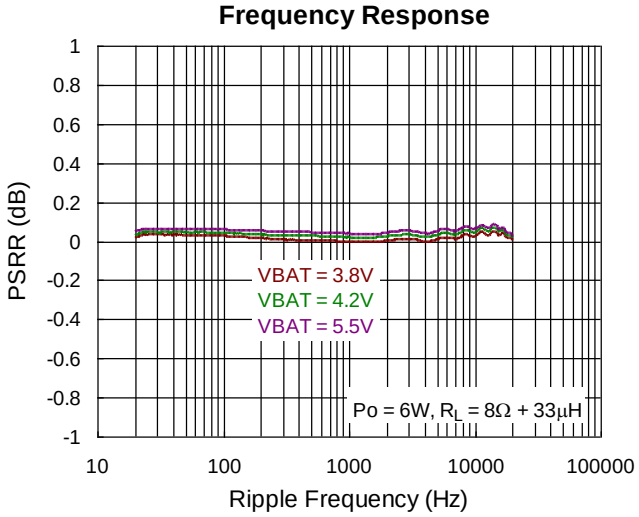
VDDD PSRR



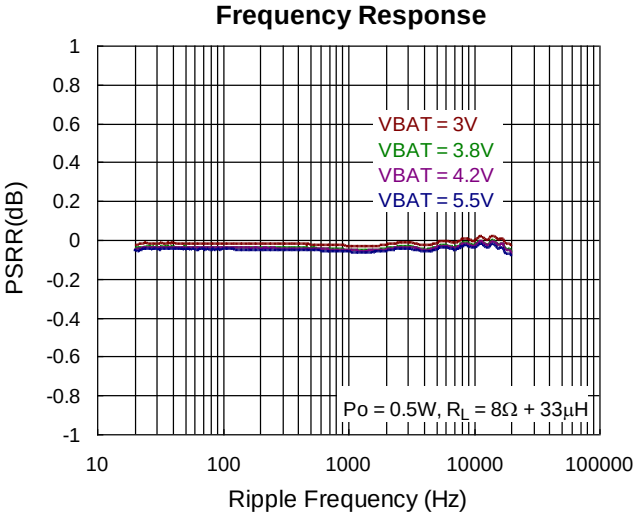
VBAT PSRR



Frequency Response



Frequency Response



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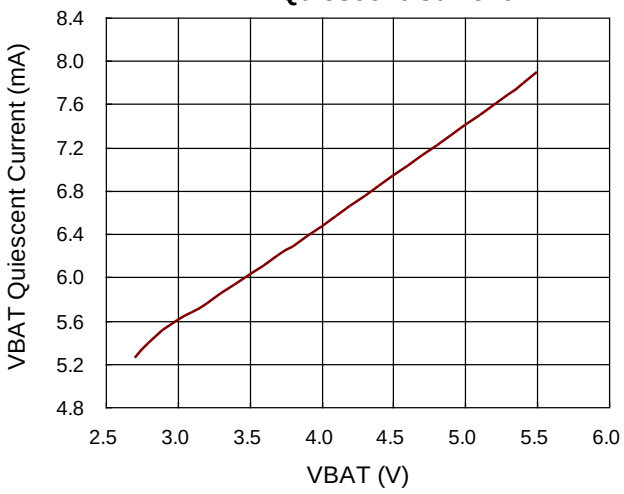
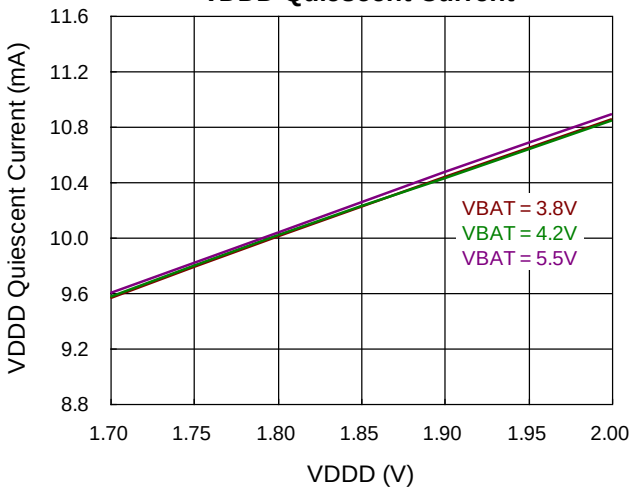
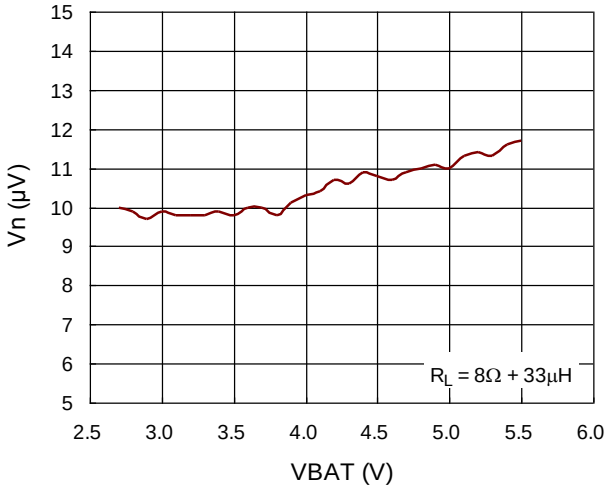
VBAT Quiescent Current



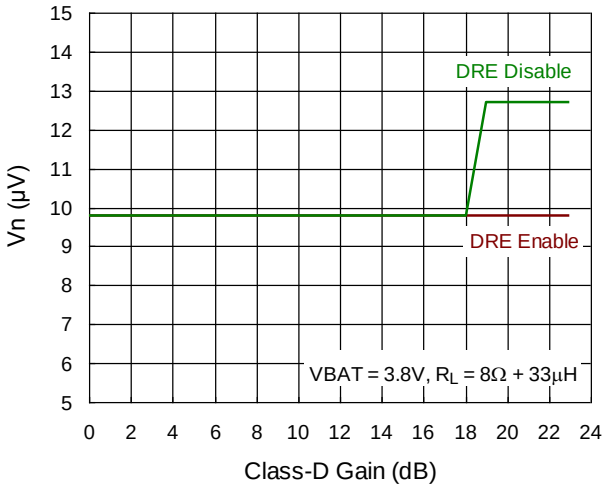
VDDD Quiescent Current



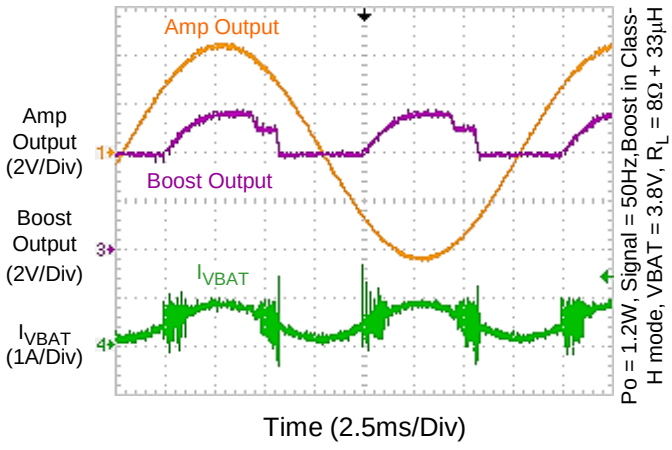
Vn vs. VBAT



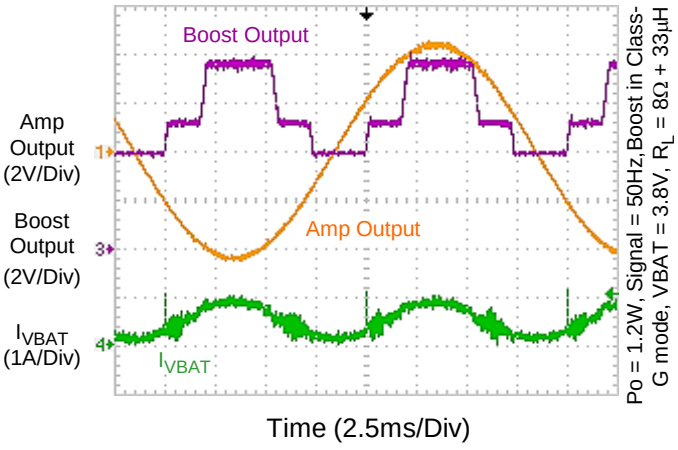
Vn vs. Class-D Gain



Boost Change Mode Behavior



Boost Change Mode Behavior



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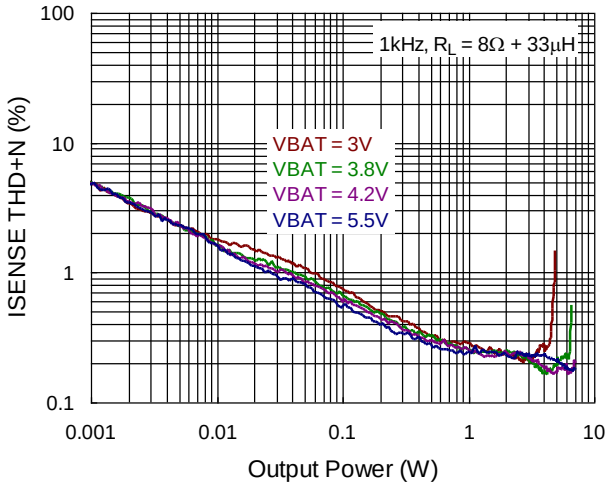
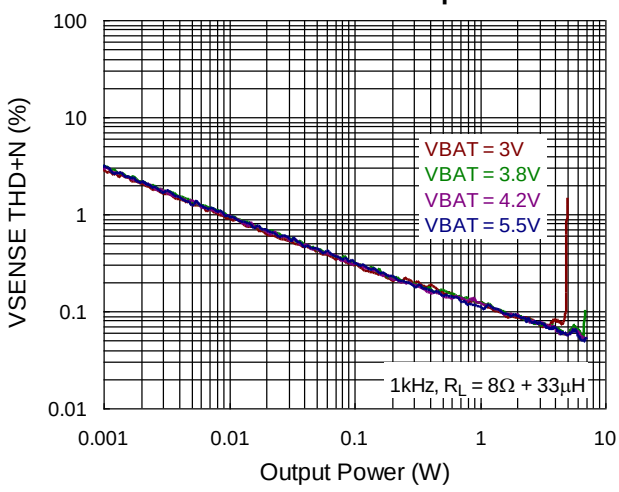
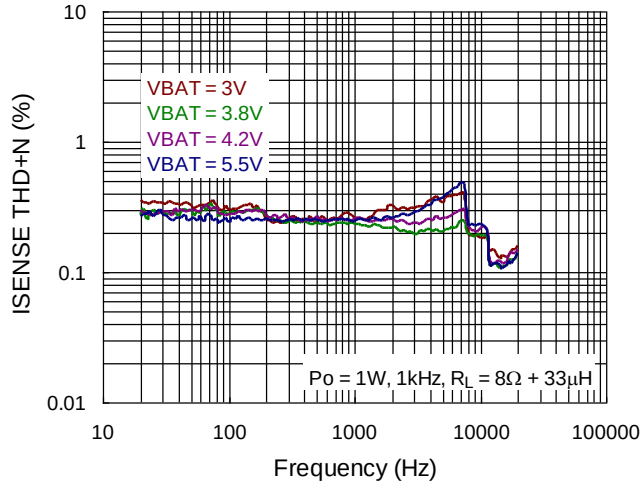
ISENSE THD+N vs. Output Power



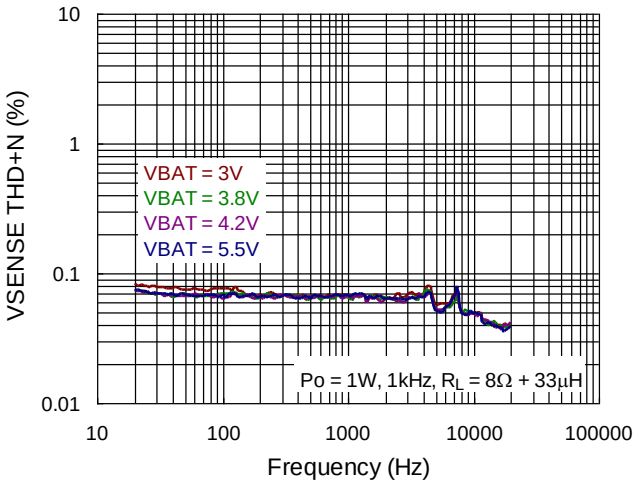
VSENSE THD+N vs. Output Power



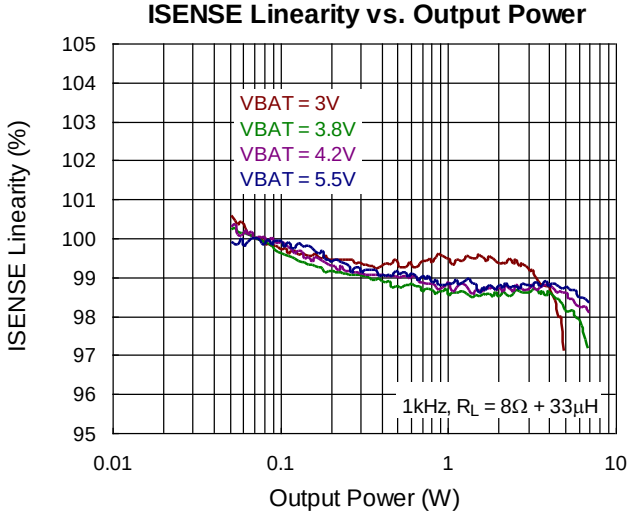
ISENSE THD+N vs. Frequency



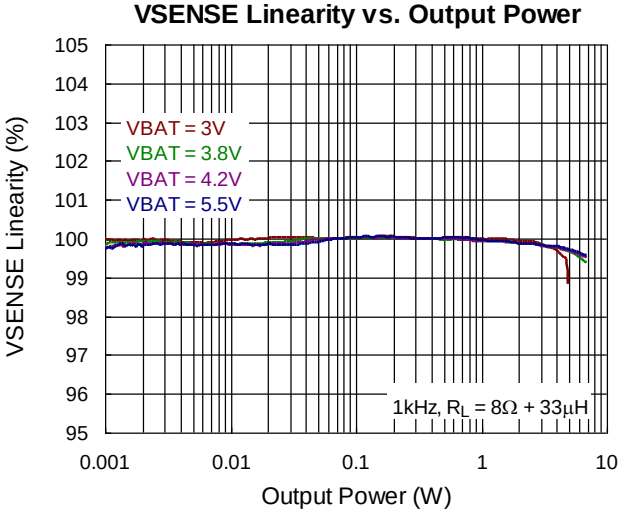
VSENSE THD+N vs. Frequency



ISENSE Linearity vs. Output Power



VSENSE Linearity vs. Output Power



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I²C Interface

Device Addressing

The RT5512B supports I²C control interface. The default device address is accessed via pin ADS1 and ADS2, see Table 2. Address selection via pins ADS1 and ADS2 four separate address are supported for stereo mode application. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively. The generic address is independent of pins ADS1 and ADS2. Note that the RT5512B always monitors the level of ADS1 to change its I²C ID, but the RT5512B will latch the level of ADS2 once 768μs after the edge of RST pin goes from low to high or after I²C write software reset.

Table 2. Address Selection Via Pins ADS1 and ADS2

ADS2 Pin (V)	ADS1 Pin (V)	Address	Function (bit 0)
0	0	1011100x (5CH)	0 : write, 1 : read
0	VDDD	1011101x (5DH)	0 : write, 1 : read
VDDD	0	1011110x (5EH)	0 : write, 1 : read
VDDD	VDDD	1011111x (5FH)	0 : write, 1 : read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
1	0	1	1	1	ADS2	ADS1	Bit 0 = LSB

I²C bus wiring is very simple. Only two signal lines SDA (Serial Data Line, Data or address signal) and SCL (Serial Clock Line, Clock signal) are used to perform serial communication between integrated circuits in the system.

The corresponding I²C communication pins in the RT5512B are SDA and SCL.

Typical I²C format is (Start)-[Slave Address]-[Register Address]-[Data]-(Stop). After writing the slave address first, it needs to be written again to specify the register address for reading and writing. The start and stop conditions of I²C are determined by the SDA transition state, while SCL is at logic high level. When SCL is high, the SDA transition from high to low is Start condition. Otherwise, SDA transition from low to high is Stop condition. The I²C Bus protocol stipulates that in addition to the start signal and the stop signal, all signal transmissions are fixed in groups of 8 bits (1 Byte), and the MSB is sent first. After each group (8 bits) signal is sent, the sender needs to read an ACK bit (acknowledged) that the receiver responds. ACK low indicates that the data has been received. ACK is an important basis for judging whether the communication between Master/Slave is normal. For valid I²C data read or write, SDA must keep the signal stable and can't change state when SCL is high in order to correctly read (latch) the data. SDA only allows transitions when SCL is low level.

The serial interface also supports single-byte and multiple-byte read/write function. Please refer to the next paragraph for the RT5512B Read/Write function description.

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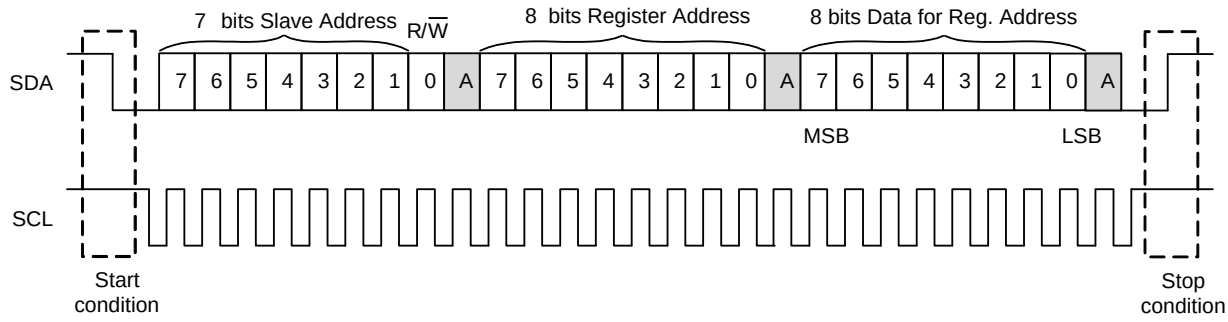

Figure 1. Typical I²C Format

Read and Write Function

The RT5512B single-byte data-read function format is shown in Figure 2.

Data transfer is initiated when the master device transmits a start condition: SDA is pulled low while SCL stays high, followed by the slave address. The data is sampled when SCL rises for the first bit. The read/write bit is set to 0 to declare the RT5512B address byte to be read. After slave device address and the read/write bit, the RT5512B device responds an acknowledge bit. In second step, the master device sends the RT5512B internal memory address to be read and the RT5512B responds with an acknowledge bit. Then the master device sends start condition again followed by setting the RT5512B device address and read/write bit to 1, and the RT5512B device responds an acknowledge bit. (Setting the read/write bit to 1 represents read internal memory address data.)

The RT5512B sends out data from the register to read. After receiving register data, the master device replies no-acknowledge bit (SDA go high) to indicate that it has not continued to read the data. Then master device sends stop condition (when SDA is pulled high while SCL is high) to complete the single-byte data reading function.

About read multiple data byte, the format is the same as reading a single data byte, and the only difference is the data byte amount sent form slave device. The master device replies with an acknowledge bit after receiving each data byte. After the RT5512B sends the last data byte, the master device replies no-acknowledge bit and transmits a stop condition.

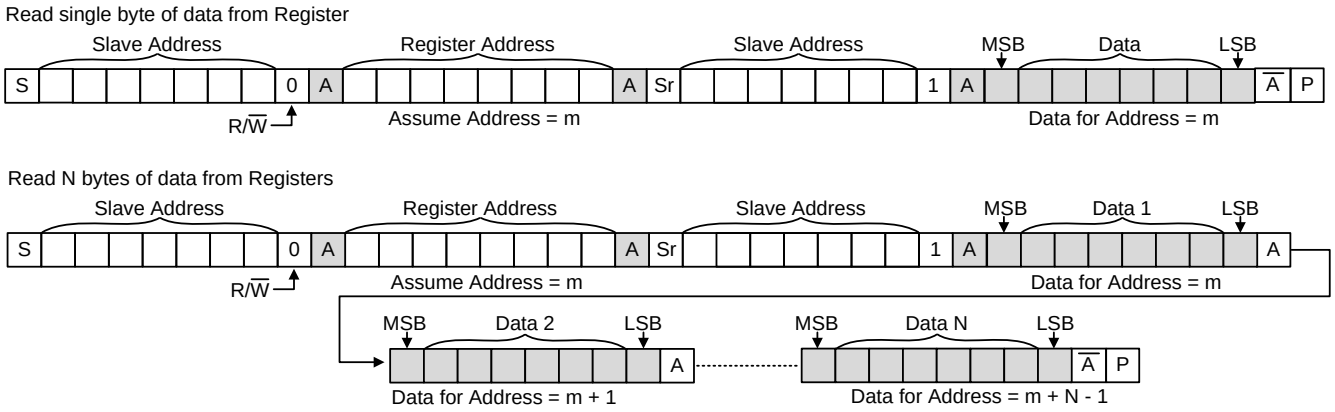

Figure 2. Single-byte and Multiple-byte I²C Read Format

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The RT5512B single-byte data-write function format is shown in Figure 3.

Data transfer is initiated when the master device transmit a start condition: SDA is pulled low while SCL stays high, followed by the slave address. The data is sampled when SCL rises for the first bit. The read/write bit is set to 0 to declare the RT5512B address byte to be write. After slave device address and the read/write bit, the RT5512B device responds an acknowledge bit. In second step, the master device sends the RT5512B internal memory address to be written and the RT5512B responds with an acknowledge bit. Then master device sends out data to write in RT5512B internal memory address. After receiving register data, the RT5512B replies an acknowledge bit to indicate that the data is received. Then master device sends stop condition (when SDA is pulled high while SCL is high) to complete the single-byte data write function.

About write multiple data byte, the format is the same as write a single data byte, and the only difference is the data byte amount sent form master device. The slave device replies with an acknowledge bit after receiving each data byte. After the RT5512B receives the last data byte, the RT5512B replies an acknowledged bit and master device transmits a stop condition.

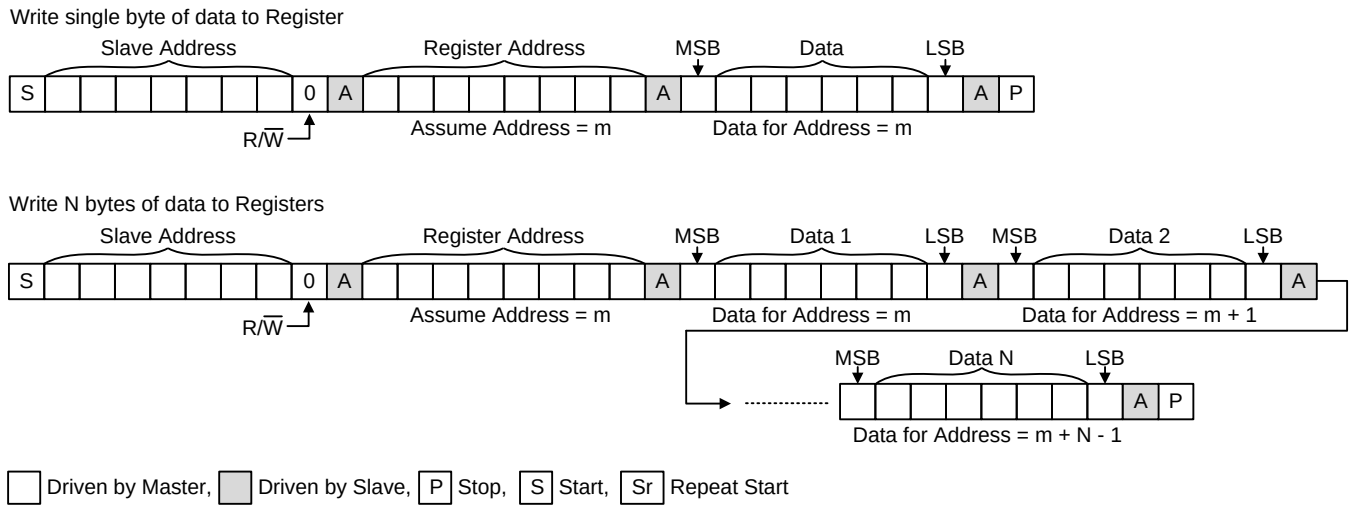

Figure 3. Single-byte and Multiple-byte I²C Write Format

I²C Waveform Information

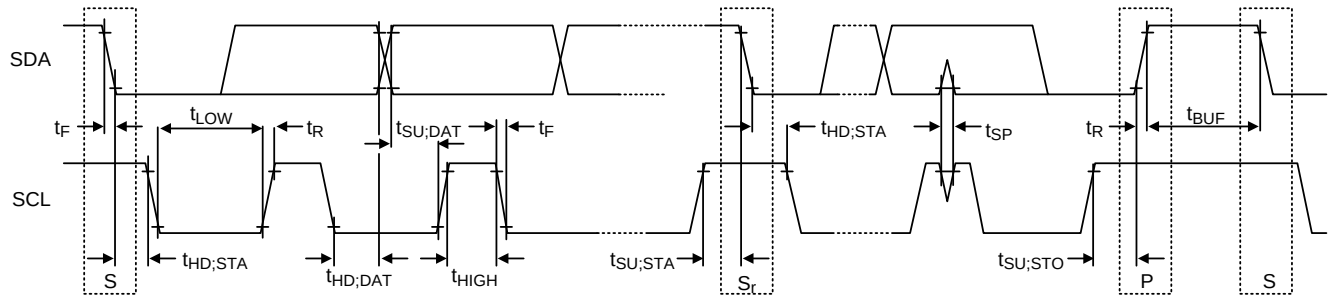

Figure 4. Timing Diagram of I²C Interface

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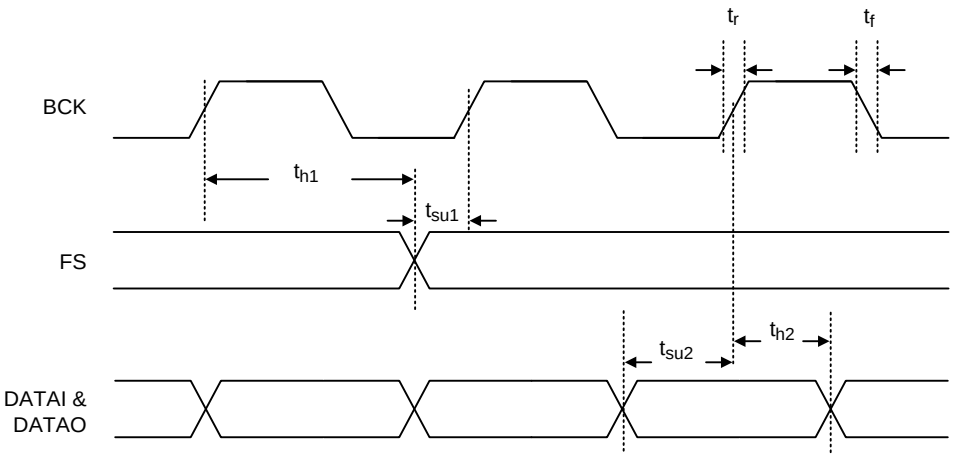

Figure 5. Timing Diagram of Slave Mode I^2S Interface

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Operation Mode Modes

The RT5512B can operate in four different mode which are power-down/suspend/operating/fault. Internal functional block operational status in different mode is depicted in Figure 6.

Mode / Blk	PWDN	SUSP	OP	FAULT
PLL	✕	○	○	○
I²C	○	○	○	○
I²S	✕	✕	○	○
AMP	✕	✕	○	✕

○ : Normal operation

✕ : Power down

Figure 6. Operation Mode

Mode	Condition	Description
Power-down	PWDN = 1	1. When PWDN set to 1, chip will enter power-down mode. 2. Power consumption is minimum and PWM outputs are floating. 3. I^2C bus remains awake. 4. I^2S path is disable.
Suspend	BCK/SR invalid	1. Chip will enter suspend mode. 2. Most of the data path are off, and PWM outputs are floating. 3. I^2C bus remains awake. 4. PLL keeps in free-run mode and CK1M is used to monitor BCK/SR on I^2S bus to see if they are correct.
Operating	BCK & SR valid PWDN = 0 AMPE = 1	1. If set PWDN/AMPE at register 0x03 as condition, chip will enter operating mode when BCK and sampling rate are valid.
Fault	OV/OT/OC/UV = 1	1. Chip enters fault mode when an error event of physical protection mechanisms occurs (OCP/OVP/UVP/OTP). 2. The boost and AMP are OFF. 3. The system exits from Fault mode after the protection event released for a checking cycle of about 200ms.

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Mode Transition

The state machine of mode transition is shown in Figure 7. After power on, the control bit will always be reset to PWDN mode.

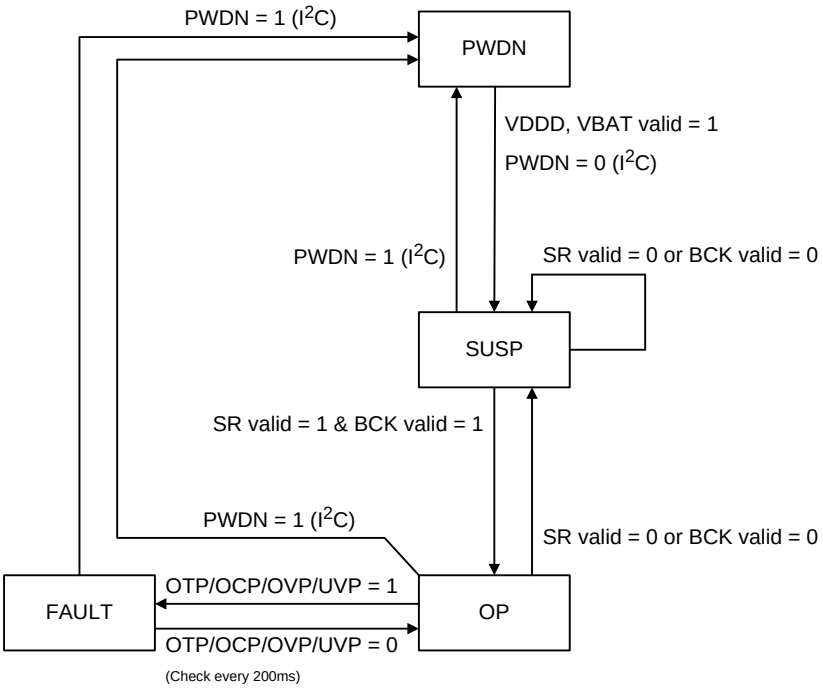

Figure 7. Mode Transition

Power ON/OFF Sequence

The power on sequence is shown in Figure 8. After power is valid, two groups of control signals should be set, without specific order requirement between these two groups:

I^2C : PWDN, AMPE should be programmed. These three bits can be programmed by single command since they are at the same byte address.

I^2S : BCK should be valid on the specified interface.

If the PWDN is set to 0 before the BCK valid, it will go to SUSP mode automatically. The output of amplifier will be valid after entering OP mode, signal ramp up will always be implemented when the mode transits from PWDN or SUSP mode to OP mode.

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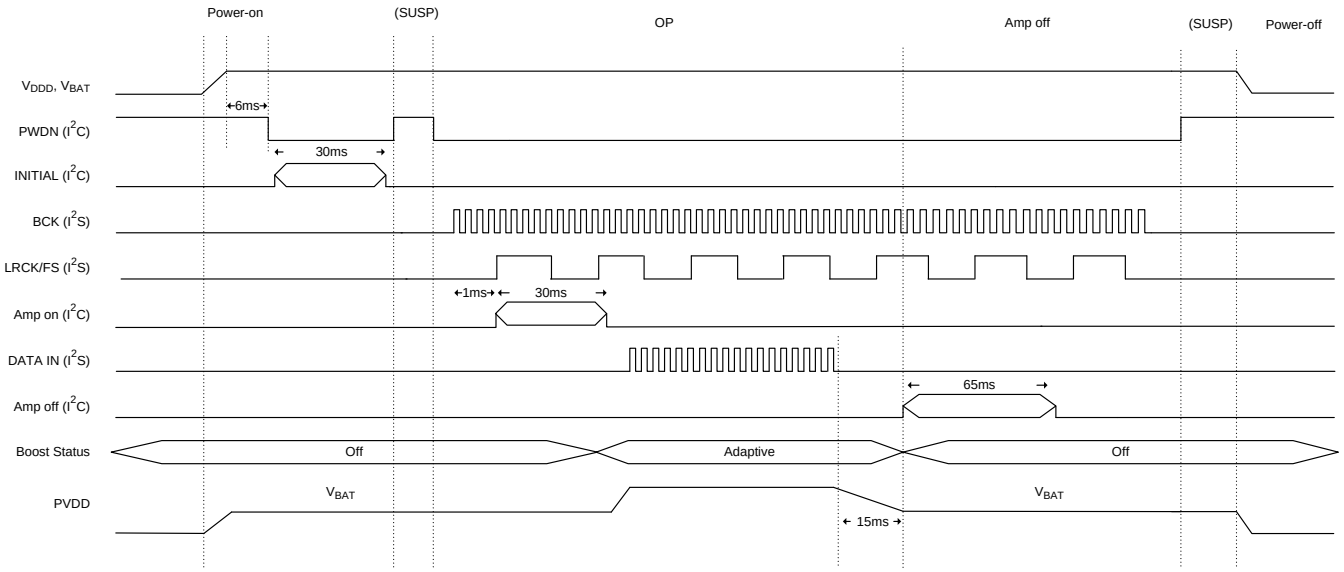

Figure 8. Power-ON/OFF Sequence

I²S Mode Change without PWDN

When I²S mode change, like BCK and FS frequency relationship, the chip will not be shut down. If the clock source from I²S changes, I²S invalid is detected. In this case, soft muting is implemented before entering Amp off situation. In the opposite situation, if the clock source from I²S is detected valid again, signal ramp up is implemented at the start after it enters the operating mode.

The above procedure is shown in Figure 9 and ramp is setting by register 0x28 bit[2:0].

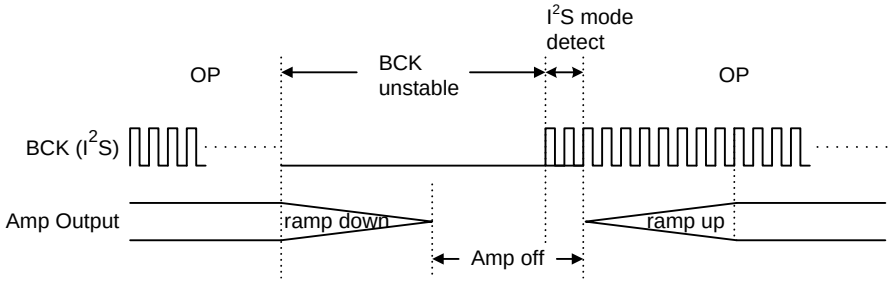

Figure 9. I²S Mode Change without PWDN

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Table 3. Ramp Control Setting

Register	Bits	Bits Name	Description
0x28	2:0	VOLCTRL	Ramp control when new volume setting is different from old setting : 000 : No ramp up/down (default) 001 : 0.5dB per sample 010 : 0.5dB per 2 samples 011 : 0.5dB per 4 samples 100 : 0.5dB per 8 samples 101 : 0.5dB per 16 samples 110 : 0.5dB per 32 samples 111 : 0.5dB per 64 samples

Data (I^2S) Interface

Data Format

The I^2S formats supported by the RT5512B are listed below :

Interface	Data Format	BCK Frequency
I^2S Standard	up to 16-bit	32fs
I^2S Standard	up to 24-bit	64fs
Left-justified	up to 16-bit	32fs
Left-justified	up to 24-bit	64fs
Right-justified (16-bit)	16-bit	32fs
Right-justified (16-bit)	16-bit	64fs
Right-justified (18-bit)	18-bit	64fs
Right-justified (20-bit)	20-bit	64fs
Right-justified (24-bit)	24-bit	64fs
TDM 8-slot	64-bit	64fs
TDM 16-slot	128-bit	128fs
TDM 32-slot	256-bit	256fs

fs : 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz

Note :

TDM 32-slot BCK Frequency 256fs formats does not support 88.2kHz and 96kHz.

I^2S Sampling Rate

I^2S can support rate 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz.

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Output Path

DATAO can output different data format by configuring I2SDOLS and I2SDORS at register 0x12. In TDM mode, the DATAO will be kept hi-z if the bit is beyond the range indicated by TDM_TX_LOC and TDM_TX_LEN at register 0x14. DATAO uses BCK as the reference clock to transmit selected data. The FS is treated as channel select for I^2S mode and frame synchronizer in TDM mode.

The Digital Audio interface supports I^2S and TDM formats at various sample rates from 8kHz to 96kHz. The interface is compliant with all I^2S interface configurations and supports a wide range of TDM interface configurations (up to 16-channel at fs = 48kHz). And the LSB and MSB must be supported. The signal name is defined as :

1. I-SENSE : The Current sense signal.
2. V-SENSE : The Voltage sense for speaker output signal.
3. D-SENSE : The data is only for testing
4. B-SENSE : The Voltage sense for battery.

When only one smart PA is connected, I^2S bus is recommend. At this situation, signal sequence should be I-SENSE and V-SENSE. Each signal is in 16-bit Format. I^2S L/R channel data signal is in 24-bit Format. The register have to set 0x12 bit'[5:3] = 1, 0x12 bit'[2:0] = 6 for receive I-SENSE, V-SENSE data from DATAO.

The sequence is shown as below :

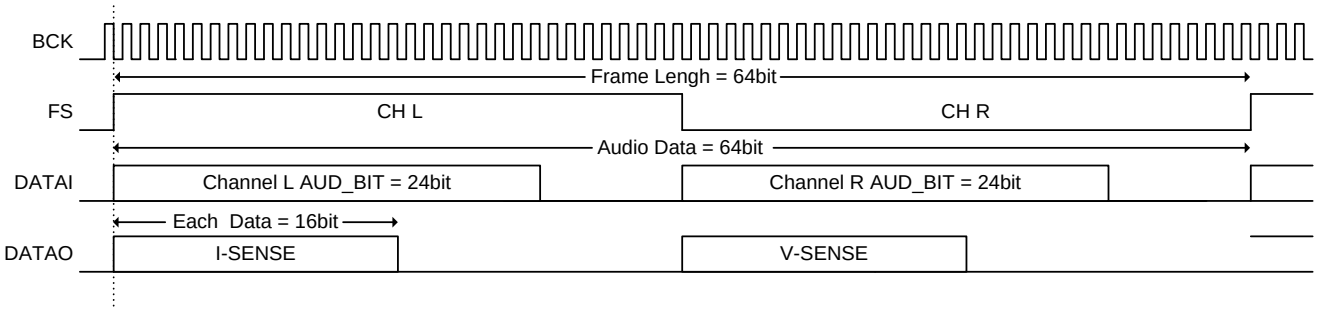

Figure 10. Only One Smart PA I^2S Left-Justified Format (Data = 24bit)

When two smart PA is connected and the I^2S is used. The DATAI signal is only 16bit available for each channel.

The sequence is shown as below :

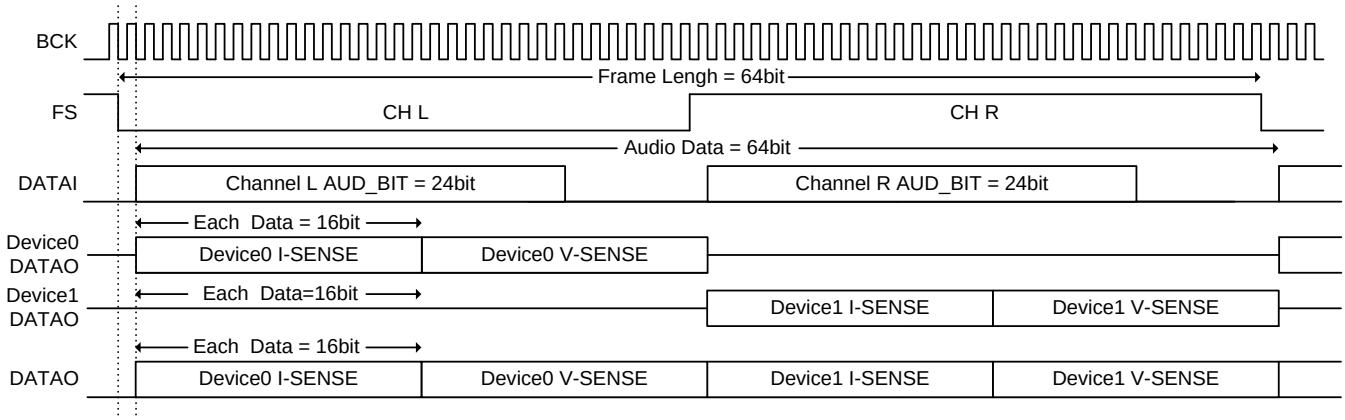

Figure 11. Two Smart PA I^2S Standard Format

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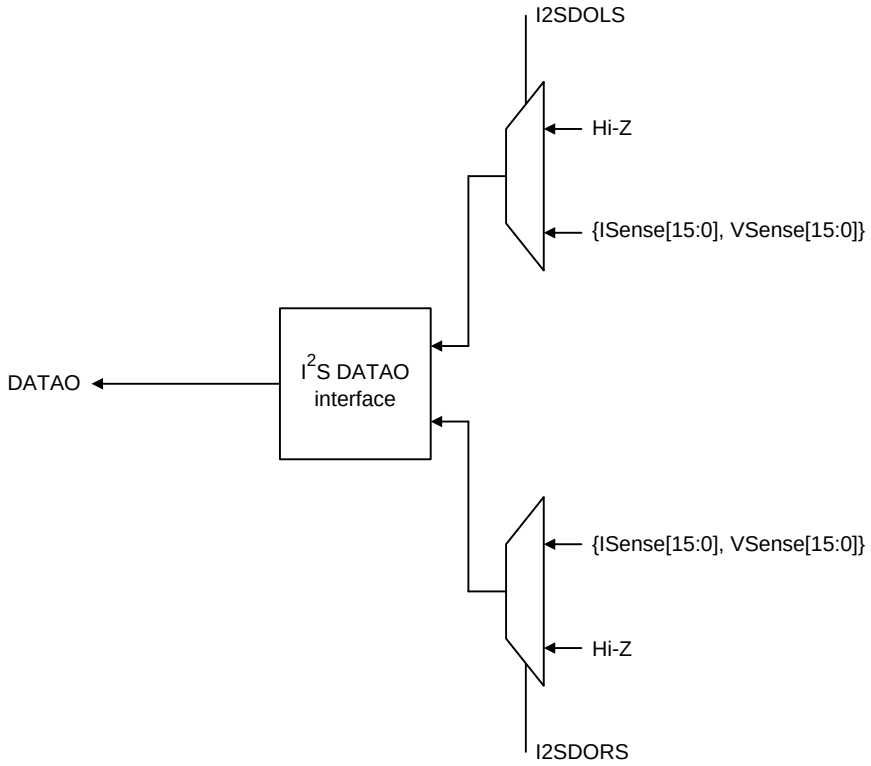

Figure 12. I²S Output Mux

TX Data Structuring in I²S Mode (Stereo)

I2SDOLS I2SDORS	Left Channel		Right Channel	
	bit 0-15	bit 16-31	bit 0-15	bit 16-31
010	Hi-Z		I-Sense[15:0]	V-Sense[15:0]
011	I-Sense[15:0]	V-Sense[15:0]	Hi-Z	
Others	Reserved		Reserved	

TX Data Structuring in I²S Mode (Mono)

I2SDOLS	Left Channel	
	bit 0-15	bit 16-31
001	I-Sense[15:0]	Reserved[15:0]

I2SDORS	Right Channel	
	bit 0-15	bit 16-31
110	V-Sense[15:0]	Reserved[15:0]

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When four smart PA is connected and TDM mode is used, the frame length should set to 128bit. The DATAI signal is only 24bit available for each channel.

The sequence is shown as below :

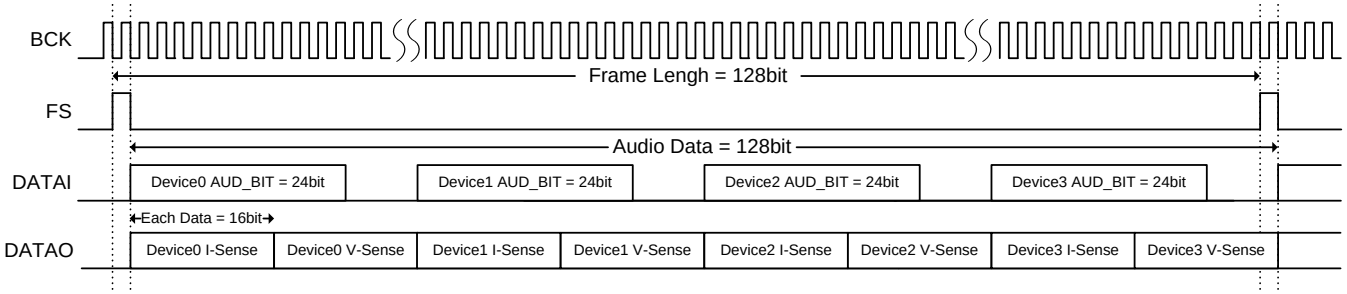

Figure 13. Four Smart PA TDM Standard Format

TX Data Structuring in TDM Mode

The RT5512B can transmit I-Sense[15:0], V-Sense[15:0], D-Sense[15:0], B-Sense[15:0], speaker protect gain[15:0], Vtherm[8:0], R_IF[7:0] and DAC_BIQ to I^2S DATAO in TDM mode. The TDM_TX_LOC register indicates the starting slot to put the data stream on DATAO pin. The sequence of data stream in TDM mode is {I-Sense[15:0], V-Sense[15:0], D-Sense[15:0], B-Sense[15:0]} and MSB-first. The TDM_TX_LEN whose unit is byte (slot) determines how many bytes will be transmitted, from MSB to the end of (TDM_TX_LEN)th slot. The rest of slots outside of the transmitted data stream shall be keep Hi-Z.

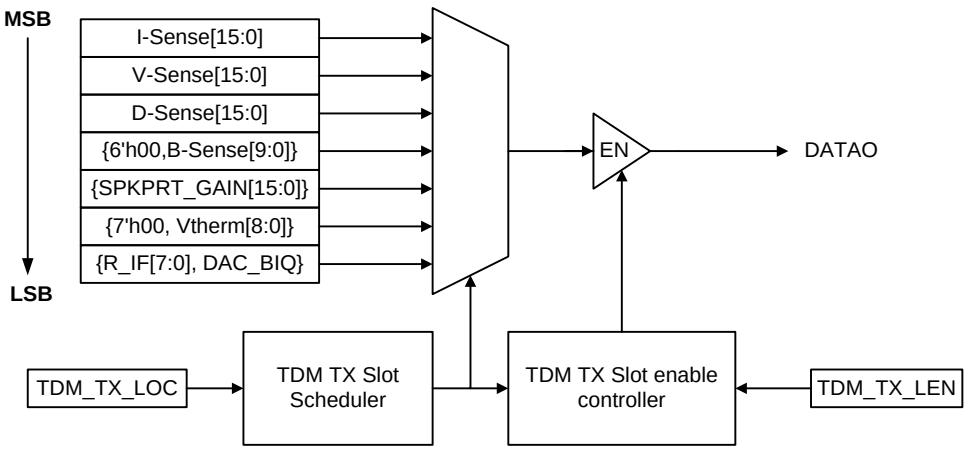

Figure 14. TX Data Structuring in TDM Mode

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RX Data in TDM Mode

The data in the TDM stream that is allocated for assignment to the internal data registers is extracted using the TDM_RX_LOC and TDM_RX_LEN controls at register 0x13. Data is extracted MSB-first, starting at the TDM_RX_LOC location and placing it into its respective internal data register. This process continues until TDM_RX_LEN bits are extracted from the TDM stream or another data extraction begins.

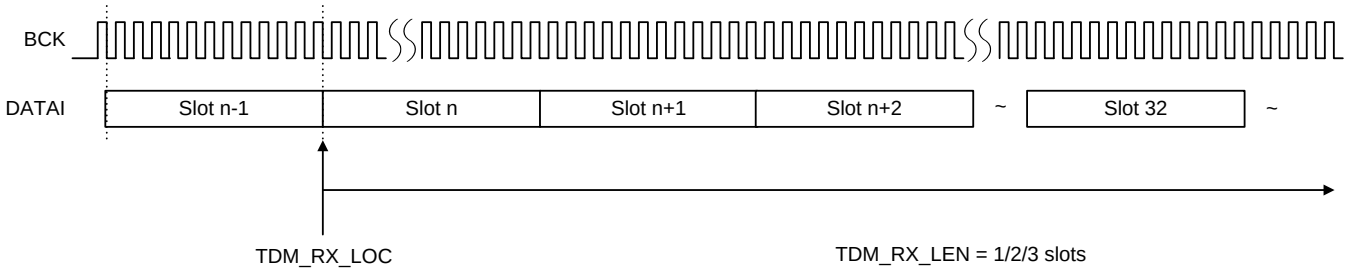

Figure 15. RX Data structuring in TDM Mode

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Application Information

Boost Mode and Signal Tracking Behavior

The RT5512B can automatically enables the boost converter if necessary. The boost converter behavior can be configured in class-H or class-G. Please refer to below table to set the behavior :

Register	Bits	Bits Name	Description
0x40	8	CLASS_H_EN	0 : Boost class-G 1 : Boost class-H (default)

Boost converter in class-H can keeps tracking the speaker output signal and adjusts the boost output voltage just above what is needed, namely the head room.

0x41 bit [11:6] BST_THT1 is used as the head room setting and the head room formula is 1.1V + (BST_THT1 (DEC) x 0.2(V)). The minimum head room is 1.1V.

The boost converter maximum output can be limited in 12.5V by register 0x41 bit[3:0]

Register	Bits	Bits Name	Description
0x41	11:6	BST_THT1	Class-H : Head room for output signal = 1.1V + (BST_THT1 x 0.2V), Head room = 1.7V (default) e.g. 000000 : 1.1V, 000100 : 1.9V
	5:0	BST_TH1	Class-H : Set the maximum of VBST = 9.5V + (BST_TH1[3:0] x 0.2V), the maximum of VBST = 12.5V (default) e.g. BST_TH1[3:0] = 1100, the maximum of VBST = 11.9V

When the speaker output signal go low, the boost converter output voltage will not fall immediately, and it will remain. After the hold time period, speaker signal does not become larger again, the boost converter output voltage start to drop. If the speaker signal increase during the hold time, the boost converter output voltage will not drop. The hold time can be adjusted by the register 0x40 bit[7:6]. In order to supply voltage to class-D amp in time, the slew rate of boost converter output going up is no limit. When speaker signal go low, the boost output voltage is going down. It slew rate is adjusted by the register 0x40 bit[5:4]. About boost converter hold time and slew rate, please refer to the Table 4.

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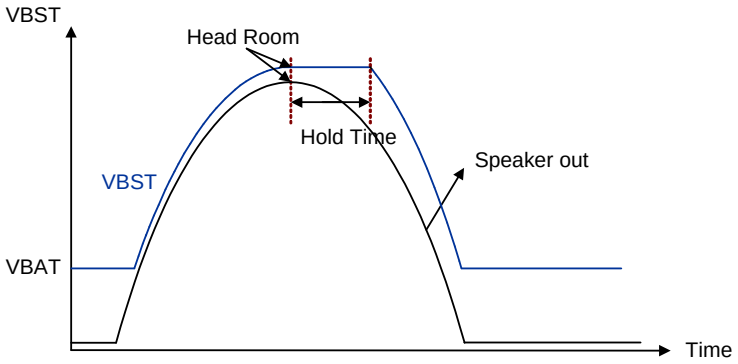

Figure 16. Boost Class-H Behavior

Table 4. Boost Class-H Slew Rate

Register	Bits	Bits Name	Description
0x40	7:6	BST_TOT	Level timeout time in adaptive mode : 00 : 500μs 01 : 1ms (default) 10 : 2ms 11 : 4ms
	5:4	SLEW_RATE	when in boost mode-H, the rate of signal going down is limited by SLEW_RATE 00 : 0.75mV/μs 01 : 1.5mV/μs (default) 10 : 3.0mV/μs 11 : 6.0mV/μs

The RT5512B I^2S input signal is converted and processed by the DAC to a speaker output with a delay time of approximately 100μs. The boost algorithm calculates the voltage of the speaker output signal from I^2S to directly control the boost converter output voltage. This means that the boost output voltage is 100μs faster than the speaker output signal. This ensures that the speaker output signal gets enough voltage level from boost converter.

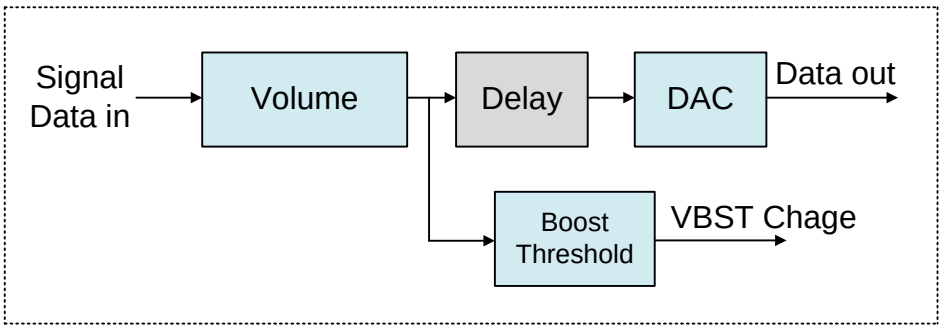

Figure 17. DAC and Processing Time in Class-H

The RT5512B boost converter has three modes of operation in class-G : battery mode, fixed mode and adaptive mode. The operating mode is usually set to adaptive mode for optimum efficiency. Please refer to below table to set the operating mode :

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Table 5. Boost Mode Selection

Register	Bits	Bits Name	Description
0x40	1:0	BST MODE	00 : Disable (default) 01 : Battery mode 10 : Fixed mode 11 : Adaptive mode

Note : when select Boost mode, please set 0x40 bit8 = 0 for boost class-G

According to the I^{2}S input signal change, the RT5512B boost class-G algorithm can determine the voltage required by the speaker output signal to achieve the best efficiency.

The boost algorithm calculates the voltage of the speaker output signal and compares it with the threshold voltage of the boost converter change mode to determine whether the boost converter output voltage needs to be changed. The boost converter has up to three output voltage configurations that can be set by the user.

When the boost converter is configured in adaptive mode, the speaker output signal is lower than threshold 4 voltage. The boost converter is bypassed and supplied directly to the load by the battery. When the speaker output signal is higher than threshold 4 voltage, boost converter enable and the boost output is set to target 4 voltage. This is for the speaker output signal to have a margin and avoid the phenomenon of clipping. In the same way, when the speaker output signal is higher than threshold 3 voltage, boost converter enables and the boost output is set to target 3 voltage. The boost converter has a maximum configurable voltage of 12.5V.

When estimating the voltage drop of the output signal, the Boost algorithm is compared to the threshold voltage to determine whether to change the output voltage of the boost converter.

When the Boost algorithm determines that the speaker output signal is lower than the threshold 1 voltage, the boost converter output voltage has a hold time of 500μs to maintain the original output voltage to ensure that the signal becomes larger again. After the hold time, the boost converter reduces the output voltage to the target 2 voltage. In the same way, the speaker output signal is below the threshold 4 voltage. After the hold time, the boost converter reduces the output voltage and is configured to bypass, supplying the load energy directly from the battery.

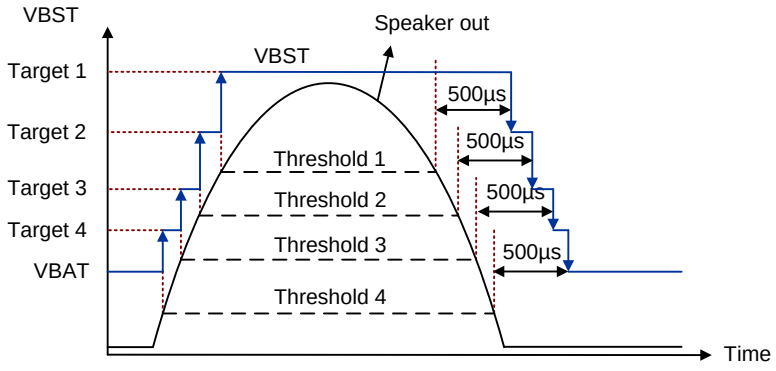

Figure 18. Boost adaptive Mode Behavior

The RT5512B I^{2}S input signal is converted and processed by the DAC to a speaker output with a delay time of approximately 430μs. The boost algorithm calculates the voltage of the speaker output signal from I^{2}S to directly control the boost converter output voltage. This means that the boost output voltage is 430μs faster than the speaker output signal. This ensures that the speaker output signal gets enough voltage level from boost converter.

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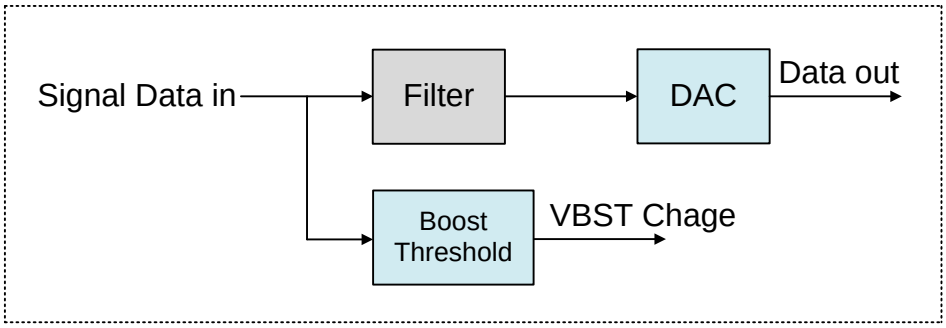

Figure 19. DAC and Processing Time in Class-G

Boost output voltage and change mode threshold register are shown in below table. BST_TH indicates the threshold at which the boost converter changes the output voltage, and BST_THT indicates the target voltage to be outputted by the boost converter.

Table 6. Boost Output Voltage and Change Mode Threshold

Register	Bits	Bits Name	Description
0x41	11:6	BST_THT1	Class-G : VBST target in fixed mode or highest VBST target in adaptive mode 000000 : Disabled 000001 to 110000: 2.9V + (BST_THT1 x 0.2 V) e.g. 000001 : 3.1V, 100001 : 9.5V 000011 : 3.5V (default) 110001 to 111111 : Reserved Class-H : Head room for output signal = 1.1V + (BST_THT1 x 0.2V), Head room = 1.7V (default) e.g. 000000 : 1.1V, 000100 : 1.9V
	5:0	BST_TH1	Class-G : Boost threshold for BST_THT1 000000 : Disabled 000001 to 110001: 1.3V + (BST_TH1 x 0.2 V) e.g. 000001 : 1.5V, 100001 : 7.9V 101111 : 10.7V (default) 110010 to 111111 : Reserved Class-H : Set the maximum of VBST = 9.5V + (BST_TH1[3:0] x 0.2V), the maximum of VBST = 12.5V (default) e.g. BST_TH1[3:0] = 1100, the maximum of VBST = 11.9V

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Register	Bits	Bits Name	Description
0x42	11:6	BST_THT2	Middle VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT2 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V (default) 110001 to 111111 : Reserved
	5:0	BST_TH2	Boost threshold for BST_THT2 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH2 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 011011 : 6.7V (default) 110001 to 111111 : Reserved
0x43	11:6	BST_THT3	Lower VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT3 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V, 010111 : 7.5V (default) 110001 to 111111 : Reserved
	5:0	BST_TH3	Boost threshold for BST_THT3 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH3 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 001111 : 4.3V (default) 110001 to 111111 : Reserved
0x44	11:6	BST_THT4	Lowest VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT4 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V, 001011 : 5.1V (default) 110001 to 111111 : Reserved
	5:0	BST_TH4	Boost threshold for BST_THT4 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH4 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 000111 : 2.7V (default) 110001 to 111111 : Reserved

Boost Current Limit

The RT5512B boost converter has a configurable current limit function. The default current limit is 6A. This setting can meet the application of RL = 8Ω and output 7W. This limit value can be set lower according to the selected inductor. Please refer to Table 7 to set the required limit value. If the CC_MAX set value is small, the output power will be limited. The CC_MAX value from 00000000 to 01100111 and 10011001 to 11111111 are not allowed for use.

Table 7. Boost Mode Selection

Register	Bits	Bits Name	Description
0x45	7:0	CC_MAX	01101000 : 4A 01111000 : 5A 10001000 : 6A (default) 10011000 : 7A CC_MAX resolution is 62.5mA/per code.

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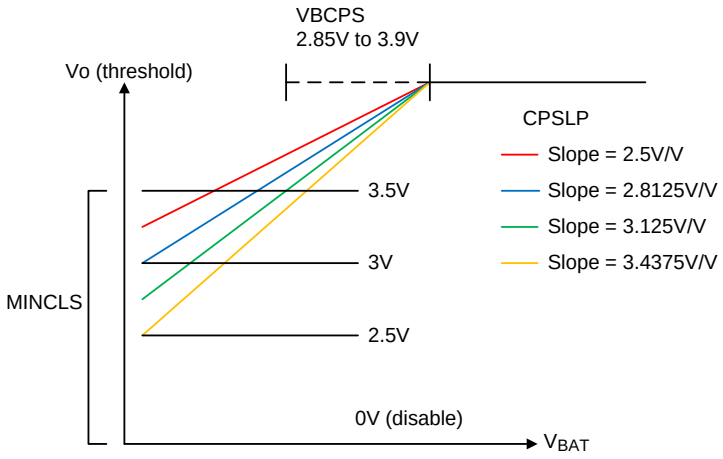
Clip Control

Clip control is used to reduce current consumption when VBAT is low. It is defined by three parameters, VBCPS, CPSLP and MINCLS. The clip threshold is shown in below figure.

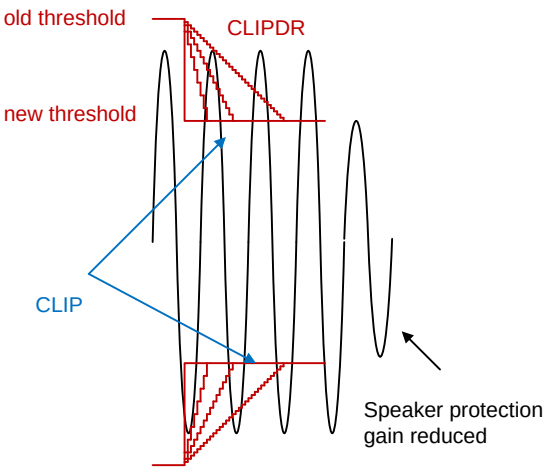


The slope of clip threshold (Vo/VBAT) can be set by CPSLP from 2.5V/V to 3.4375V/V. A Vo stop point (0, 2.5V, 3V or 3.5V) for clip threshold can be set via MINCLS. The output voltage drop will stops at this point. The clip threshold is calculated through following equation :

ClipThres = SIGMAX - (VBCPS - VBAT) x CPSLP for clip threshold ≥ MINCLS

ClipThres = MINCLS for clip threshold ≤ MINCLS

The detail function is shown below, the dropping rate of threshold can be set via CLIPDR register.



If battery voltage returns to a hysteresis level, ClipThres will increase by a rate of CLIPRR to a certain level which is defined by VBCPS, CPSLP and VBAT. The battery voltage hysteresis can be set via BVHYS register.

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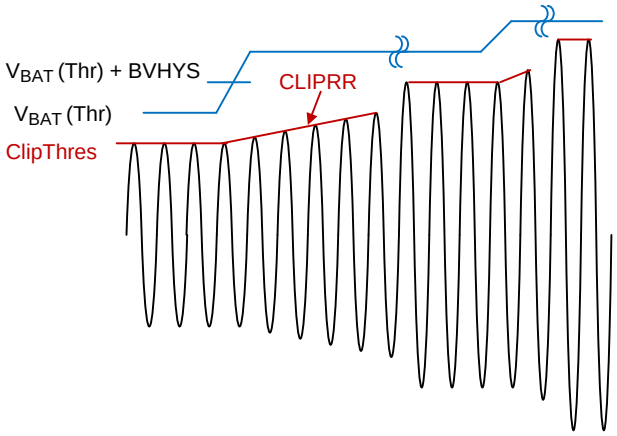
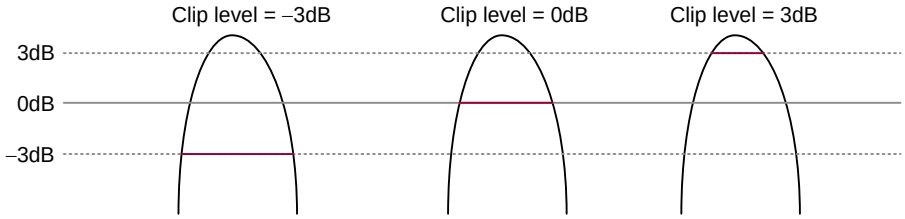


Hard Clipping

When Hard clip enable (Register 0x24 bit 8), if the digital signal is larger than HARD_CLIP_TH, the signal will be clamped to HARD_CLIP_TH.



DRE

In the signal path, the noise floor of SPK output is related to the analog gain. If decreasing the analog gain, the noise floor decreases, and vice versa. However, increasing the digital gain will not affect the noise floor. To help eliminating unwanted low level noise caused by analog circuit when incoming signal is below a certain threshold, a DRE technique is used. The DRE, Dynamic Range Expansion, stands for expanding the dynamic range of a signal. Any signal before entering analog circuit below the threshold is expanded by the specified ratio, and also the analog end is compressed by the inverse of this ratio.

The function block is depicted as below. DRE controller will monitor the signal and check if it is smaller than the threshold. If the signal is continuously smaller than the threshold for a certain time, the digital gain will be raised to current analog gain and the analog gain will be reduced to 0dB to keep the overall path gain unchanged.

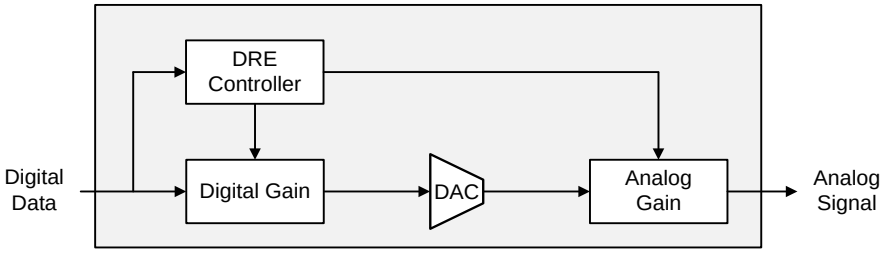


Figure 20. DRE Function Block

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There are some parameters necessary to be configured before enabling DRE. The Threshold, (0x69), is the trigger point to enter or leave DRE. Before entering DRE, the Hold Time, (0x68[2:1]), is the time before starting to find zero cross point when signal < Threshold is triggered. In Zero crossing stage, the Hold Time is also used to timeout this stage if no zero cross is detected. The Coarse delay, (0x6E[4:0]), is used to delay the gain-changing time of digital and analog end after finding zero cross stage. The gain-changing time for digital (0x6A[9:0], 0x6B[9:0]), and analog (0x6C[9:0], 0x6D[9:0]), can be both fine-tuned to compensate the path delay from digital end to analog end. During DRE, if any signal is detected as larger than Threshold, it is going to leaving DRE after zero cross point is detected or Hold Time is expired. Also, the Coarse delay, Analog fine delay and Digital fine delay are applied to compensate the path delay between digital end and analog end.

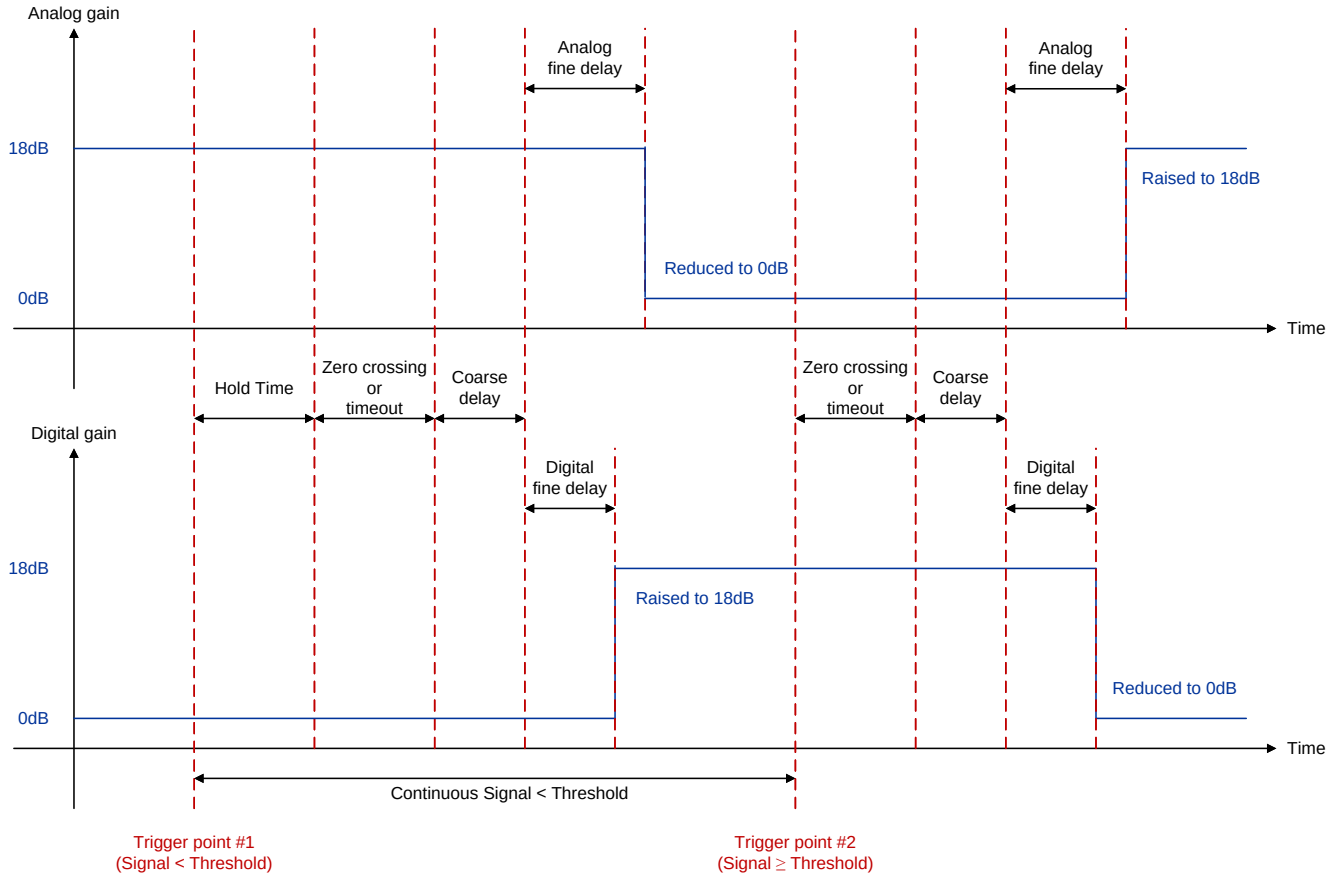

Figure 21. DRE Function Sequence

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V/I Sensing

The RT5512B has built-in voltage and current sensing to monitor speaker behavior in real time. The VSNSN and VSNSP pins are speaker voltage sensing application and it should be connected after ferrite bead filter. In addition to getting the output voltage on speaker, the V-Sense connections can eliminate output trace and ferrite bead filter resistance IR drop between output pin to V-Sense terminal. The voltage sense monitors the speaker load voltage signal via an amplifier and an A/D converter. The current sense monitors the speaker load current with a small resistor, this signal via an amplifier and an A/D converter. Both signal output are pin DATAO. Set 0XB6 bit'[13] = 1, bit'[11] = 1, bit'[10] = 0 for RT5512B V/I sensing application.

This feature can be set to disable in the register 0XB6 bit'[13], 0XB6 bit'[11:10] to reduce the quiescent current. Please refer to Table 8.

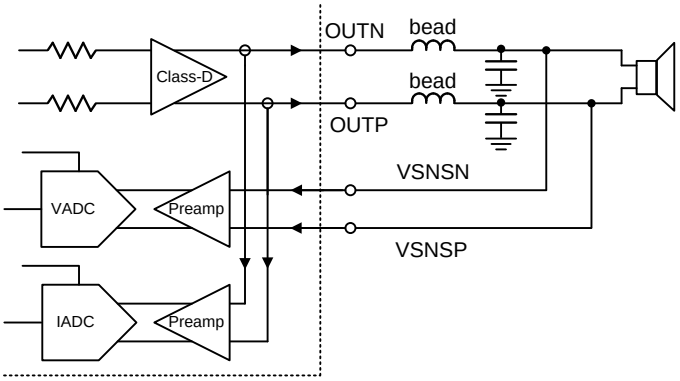

Figure 22. Voltage and Current Setting Monitor Structure

Table 8. V/I Sense Control

Register	Bits	Bits Name	Description
0xB6	13	D_CS_EN	0 = Disable current sense 1 = Enable current sense
	11	D_VS_EN	0 = Disable voltage sense 1 = Enable voltage sense
	10	D_VS_BIAS	0 = Half voltage sense bias current 1 = Max. voltage sense bias current

Users can use the algorithm and the RT5512B to reach speaker protection. If the system has a speaker protection algorithm, the voltage and current sensing data can be used to achieve speaker excursion and temperature protection. Regarding the temperature protection of the speaker, the speaker resistance can be estimated by voltage and current sensing data, and the temperature of the speaker is calculated from the temperature coefficient of resistance of the coil material. Current sensing data obtains the current variation to estimate the speaker excursion.

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Table 9. V/I Sense Data

Register	Bits	Bits Name	Description
0x12	5:3	I2SDOLS	DATAO left channel output selection 000 : {DAC_BIQ[23:0], 8'h0} 001 : {ISENSE[15:0], VSENSE[15:0]} (default) 010 : {[Hi-Z[31:0]} 011 : {ISENSE[15:0], VSENSE[15:0]} 100 : {DC_CUT_DATA[25:0], 6'h0} 101 : {SAFE_DATA_OUT[19:0], 12'h0} 110 : {DF_DATA_OUT[21:0], 10'h0} 111 : {DF_DATA_OUT_HC[21:0], 10'h0}
	2:0	I2SDORS	DATAO right channel output selection 000 : {DC_CUT_DATA[25:0], 8'h0} 001 : {DSENSE[15:0], BSENSE[9:0], 6'd0} (default) 010 : {ISENSE[15:0], VSENSE[15:0]} 011 : {[Hi-Z[31:0]} 100 : {SAFE_DATA_OUT[19:0], 12'h0} 101 : {DF_DATA_OUT[21:0], 10'h0} 110 : {VSENSE[15:0], BSENSE[9:0], 6'd0} 111 : {DF_DATA_OUT_IN[21:0], 10'h0}

Boost Capacitor Selection

In real cell phone the RT5512B VBAT power from battery, the trace is not shortest and battery provide to other device on phone mother board. On VBAT pin predictable has current peak drop and voltage ripple. In order to reduce the ripple from battery and boost convertor input voltage is stable all loading. Place a 10μF ceramic capacitor close to VBAT pin and inductor. For cell phone application, ceramic capacitor has small size and low ESR, choose X5R or X7R temperature characteristic to keep capacitance in higher temperature.

When select capacitor, have to ensure the DC bias characteristics in component datasheet, it will show the capacitance reduction percentage from rating. Suggest to choose capacitor voltage rating at least 2x the maximum DC voltage application range to avoid capacitance reduction. For the application of the RT5512B to boost VBST to 12V, a 10μF for input capacitor, a 1μF for VDDD decoupling capacitor are recommended.

Boost output capacitor is important for supply Class-D amplifier VDDP power. This capacitor can reduce boost output voltage ripple and keep the boost output voltage stable. If output capacitance dropped to low, the supply power VDDP for class-D amplifier will too low and get worst performance.

The output ripple can be determined as following equation:

$$\Delta V_{OUT} = \frac{D \times I_{OUT} \times T_S}{\eta \times C_{OUT}} + \left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}\right) \times r_{C\_esr}$$

Boost capacitor connect to BST is important for stability. The C_{VBST} capacitance is changed by DC bias. When select capacitor, please notice the DC bias characteristics. The RT5512B minimum recommended C_{VBST} capacitance is C_{VBST} capacitance is 4.5μF for output power 7W.

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Boost Inductor Selection

Small size and better efficiency are the major concerns for portable devices, such as the RT5512B used for mobile phone. The inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency.

The maximum current of inductor is highly depends on the speaker impedance which determines the output current of the boost converter. The inductor saturation current rating should be considered to cover the inductor peak current which can be approximated by the following equation :

$$I_{L\_max} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} + \frac{V_{IN} \times D \times T_S}{2 \times L_{Boost}}$$

Following is the inductor selection reference. The recommend typical inductance is 1μH for the RT5512B boost convertor. Select inductor must consideration saturation current and DC resistance specifications. Since inductance rating reduced dependent on inductor current increase, please refer to the inductance decrease current and temperature rise current in inductor datasheet. Therefore, please note the input current limit, don't let the inductor into saturation state. For system efficiency, suggest choosing a low DC resistance component.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8L 2x3 package, the thermal resistance, θ_{JA}, is 32.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (32.4°C/W) = 3.08W for a WL-CSP-36B 2.57x2.57 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 23 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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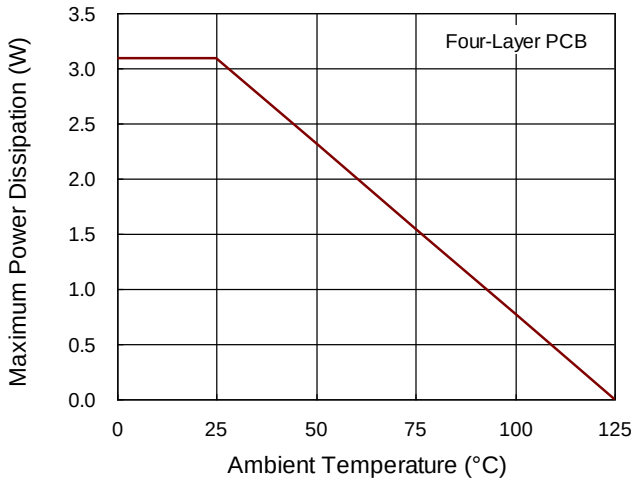

Figure 23. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT5512B, suggested external components placement and PCB routing as Figure 24.

For best performance of the RT5512B, the below PCB layout guidelines including the below items must be strictly followed.

- VBAT connect to INB through the boost inductor. Place the inductor as close as possible to the chip with 80mil width at least. The shorter and wider trace provides lower parasitic inductance and resistance for achieving better efficient. VBAT pin only consumes few micro amperes for internal analog circuit, so the trace with 6mil width is enough for VBAT of the RT5512B. The VBAT capacitor handling high noisy current for boost circuit, please connect to GNDB and GNDP first for shorten the current path and minimize the influence to digital circuit.
- Place the filter capacitor as close as possible to the VBST pin, then use shortest trace to link the capacitors and the trace width is 60mil at least. Use more vias to connect to main ground to reduce parasitic inductance and resistance.
- Connect VDDP to the VBST filter capacitor from an independent path to make sure the voltage feed into VDDP is well filtered. The shortest path may bypass the filter capacitor so that causes higher voltage ripple than expected on VDDP.
- For achieving good audio quality, place the ground connection of decoupling capacitors (VDDD caps) should be linked to GNDD first before going to main ground, identically the VREF decoupling capacitor ground connection should be linked to GNDD first before going to main ground. The trace width of VDDD and VREF are 6mil at least.
- Separating three ground plane (GNDP, GNDB and GNDD) to isolate the noisy ground from other sensitive grounds and routing the shortest path for high current return from Power/Boost ground plane before connected to main ground to make sure the digital and analog circuit gets a sufficient clean ground before influence by noisy high current path.

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- The traces of OUTP and OUTN should be kept equal width and length respectively and when use the ferrite bead filter, should be placed close to chip for better EMI performance.

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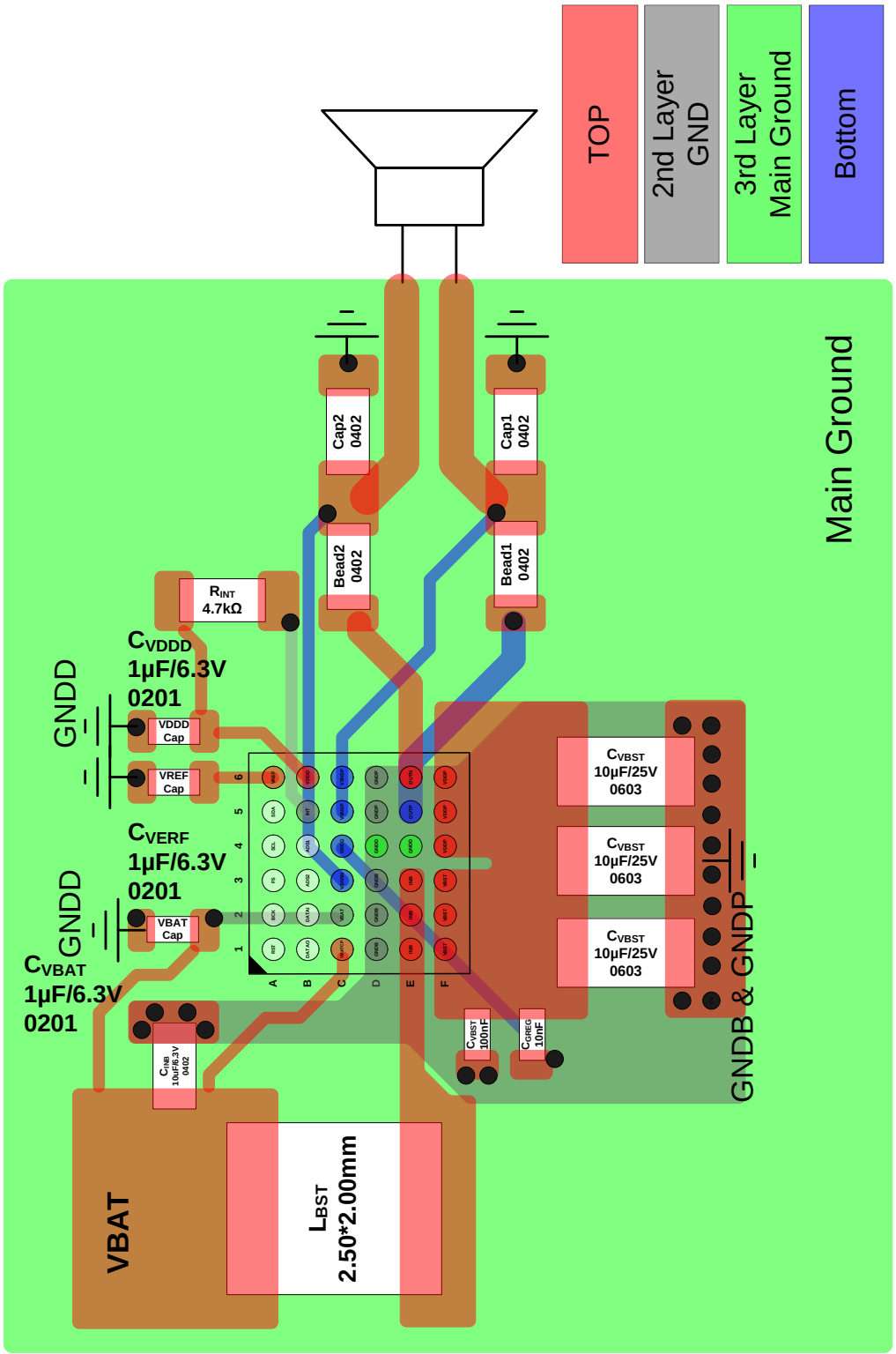
For achieving good accuracy for speaker protection, route separate trace from VSNSN and VSNSP to SPK side.



Note : C_{VBST} 100nF is optional.

Figure 24. Suggested the RT5512B PCB Layout for 4 Layers

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Register Table

Registers Description

Address	Byte	Bits	Bits Name	Default	Type	Description
0x00	2	15:12	Reserved	0000	R	Reserved
		11:8	DEVICE_ID	0000	R/W	Device ID
		7:0	CHIP_ID[7:0]	00000000	R	Chip Revision ID 00 : First version 01 : 2nd version 02 : 3rd version …
0x01	2	15:5	Reserved	00000000000	R	Reserved
		4	PLL_LOCK	0	R	0 : PLL is locked to BCK (default) 1 : PLL is unlocked to BCK
		3	BCK_CLOCK_ STABLE	0	R	0 : BCK rate stable (default) 1 : BCK rate unstable
		2	BCK_VALID	0	R	0 : BCK stable and match with BCK_MODE setting (default) 1 : BCK unstable and miss match with BCK_MODE setting
		1	BCK_LOSS	0	R	0 : BCK no loss (default) 1 : BCK loss
		0	FS_LOSS	0	R	0 : FS no loss (default) 1 : FS loss
0x02	2	15:8	Reserved	00000000	R	Reserved
		7:6	CK2M_PHASE	00	R/W	Phase selection of 2.048MHz clock, this clock will be aligned to FS. 00 : 0° (default) 01 : 90° 10 : 180° 11 : 270°
		5	SAFE_GUARD_ CK_EN	1	R/W	0 : Disable SAFE_GUARD block clock 1 : Enable SAFE_GUARD block clock (default)
		4	BOOST_CK_EN	1	R/W	0 : Disable BOOST block clock 1 : Enable BOOST block clock (default)
		3	IS_ADC_CK_EN	1	R/W	0 : Disable IS_ADC block clock 1 : Enable IS_ADC block clock (default)
		2	VS_ADC_CK_EN	1	R/W	0 : Disable VS_ADC block clock 1 : Enable VS_ADC block clock (default)
		1	DAC_CK_EN	1	R/W	0 : Disable DAC block clock 1 : Enable DAC block clock (default)
		0	ANA_CK_EN	1	R/W	0 : Disable Analog block clock 1 : Enable Analog block clock (default)

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x03	2	15:8	Reserved	00000000	R	Reserved
		7	SW_RESET	0	R/W	0 : Chip doesn't Software reset (default) 1 : Chip reset by Software reset
		6:4	Reserved	000	R	Reserved
		3	AMPDS	0	R/W	Soft off mode enable 0 : Enter soft mode before off mode (enable ramp control) (default) 1 : Enter off mode directly (disable ramp control)
		2	AMPE	0	R/W	Class D enable 0 : Disable Class D (default) 1 : Enable Class D
		1	SPKM	0	R/W	0 : Unmute (default) 1 : Force speaker mute (with ramp control)
		0	PWDN	1	R/W	Chip power down control 0 : Chip enable 1 : Chip power down (default)
0x05	2	15:8	Reserved	00000000	R	Reserved
		7	Reserved	0	R	Reserved
		6	IF_BCK_STABLE	0	RC	BCK un-stable interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, BCK un-stable
		5	IF_PLL_LOCK	0	RC	PLL unlock interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, PLL unlock
		4	IF_UV	0	RC	Under-voltage interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		3	IF_OV	0	RC	Over-voltage interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		2	IF_OCP	0	RC	AMP NMOS or PMOS over-current interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		1	IF_BST_OC	0	RC	Boost over-current interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
		0	IF_OT	0	RC	Over-temperature interrupt flag 0 : Chip operating mode (default) 1 : Interrupt flag = 1, protection occurs
0x06	2	15:8	Reserved	00000000	R	Reserved
		7:0	CRC8	00000000	R/W	I^2C write data checksum

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x09	2	15:6	Reserved	0000000000	R	Reserved
		5	D_UVP_FLAG	0	R	Battery voltage under threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		4	D_OVP_FLAG	0	R	Class-D amplifier supply voltage (VDDP) over threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		3	OCPP_FLAG	0	R	Class-D output stage high-side OC flag 0 : Normal (default) 1 : Over threshold, protection occurs
		2	OCPN_FLAG	0	R	Class-D output stage low-side OC flag 0 : Normal (default) 1 : Over threshold, protection occurs
		1	D_OCP_FLAG	0	R	Boost Converter current over threshold 0 : Normal (default) 1 : Over threshold, protection occurs
		0	D_OTP_FLAG	0	R	Class-D amplifier temperature over threshold 0 : Normal (default) 1 : Over threshold, protection occurs
0x10	2	15:8	Reserved	00000000	R	Reserved
		7:6	AUD_BIT	00	R/W	00 : 24bits (default) 01 : 20bits 10 : 18bits 11 : 16bits
		5:3	BCK_MODE	010	R/W	If MODE_DET_EN = 1, the detected BCK mode is read out If MODE_DET_EN = 0, the BCK_MODE is written to indicate the BCK mode 000 : 32fs 001 : 48fs 010 : 64fs (default) 011 : 96fs 100 : 128fs 101 : 256fs Others : Not support
		2:0	SR_MODE	011	R/W	If MODE_DET_EN = 1, the detected SR is read out If MODE_DET_EN = 0, the SR_MODE is written to indicate the sampling rate 000 : 32k 001 : Not support 010 : 96k/88.2k 011 : 48k/44.1k (default) 100 : 16k 101 : 24k/22.05k 110 : 8k 111 : 12k/11.025k

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x11	2	15:8	Reserved	00000000	R	Reserved
		7	I2S_LOSS_DET_EN	1	R/W	0 : Disable BCK/FS LOSS auto-detect 1 : Enable BCK/FS LOSS auto-detect (default)
		6	BCK_STABLE_CHK_EN	1	R/W	0 : Disable BCK stable and valid check 1 : Enable BCK stable and valid check (default)
		5	MODE_DET_EN	1	R/W	0 : Disable sampling rate auto-detect and write SR_MODE/BCK_MODE to indicate the sampling rate and BCK mode 1 : Enable SR & BCK mode auto-detect and read SR_MODE/BCK_MODE will return the detection result (default)
		4	DSP_MODE_SEL	0	R/W	0 : DSP mode A (default) 1 : DSP mode B
		3	TDM_OFFSET	0	R/W	The number of bits between the frame sync signal transitioning and data being driven on the data line 0 : The first data can be sampled at the first BCK rising edge after FSYNC rising edge (default) 1 : The first data can be sampled at the second BCK rising edge after FSYNC rising edge
		2:0	AUD_FMT	000	R/W	000 : I^2S (default) 001 : Left justify mode 010 : Right justify mode 011 : DSP mode 100 : 8 TDM slots (slot #0 to slot #7) 101 : 16 TDM slots (slot #0 to slot #15) 110 : 32 TDM slots (slot #0 to slot #31) 111 : Reserved

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x12	2	15:8	Reserved	00000000	R	Reserved
		7:6	I2SLRS	00	R/W	Audio input selection 00 : Left channel (default) 01 : (Left + Right)/2 10 : Right channel 11 : Reserved
		5:3	I2SDOLS	001	R/W	DATAO left channel output selection 000 : {DAC_BIQ[23:0], 8'h0} 001 : {ISENSE[15:0], VSENSE[15:0]} (default) 010 : {[Hi-Z[31:0]} 011 : {ISENSE[15:0], VSENSE[15:0]} 100 : {DC_CUT_DATA[25:0], 6'h0} 101 : {SAFE_DATA_OUT[19:0], 12'h0} 110 : {DF_DATA_OUT[21:0], 10'h0} 111 : {DF_DATA_OUT_HC[21:0], 10'h0}
		2:0	I2SDORS	001	R/W	DATAO right channel output selection 000 : {DC_CUT_DATA[25:0], 8'h0} 001 : {DSENSE[15:0], BSENSE[9:0], 6'd0} (default) 010 : {ISENSE[15:0], VSENSE[15:0]} 011 : {[Hi-Z[31:0]} 100 : {SAFE_DATA_OUT[19:0], 12'h0} 101 : {DF_DATA_OUT[21:0], 10'h0} 110 : {VSENSE[15:0], BSENSE[9:0], 6'd0} 111 : {DF_DATA_OUT_IN[21:0], 10'h0}
0x13	2	15:8	Reserved	00000000	R	Reserved
		7:6	TDM_RX_LEN	10	R/W	RX length control 00 : 1 slot (8bits) 01 : 2 slot (16bits) 10 : 3 slot (24bits) (default) 11 : Reserved
		5	Reserved	0	R	Reserved
		4:0	TDM_RX_LOC	00000	R/W	RX location control, indicate which slot the data MSB is loaded in 00000 : Slot 0 (default) 00001 to 11110 : Slot 1 to Slow30 11111 : Slot 31

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x14	2	15:13	Reserved	000	R	Reserved
		12:8	TDM_TX_LEN	00000	R/W	TX length control, indicate how many bytes should be transmitted from slot TDM_TX_LOC 00000 : TX disable (default) 00001 : TX length 1 slots 00010 : TX length 2 slots 00001 to 10000 : TX length 1 to 16 slots Others : Reserved
		7	TDM_TEST_EN	0	R/W	0 : TDM TX debug data test mode disable (default) 1 : TDM TX debug data test mode enable
		6:5	Reserved	00	R	Reserved
		4:0	TDM_TX_LOC	00000	R/W	TX location control, indicate which slot the data MSB is loaded in 00000 : Slot 0 (default) 00001 to 11110 : Slot 1 to Slow30 11111 : Slot 31
0x15	2	15:10	Reserved	000000	R	Reserved
		9:4	AUD_WL	011000	R/W	Audio interface word length. Valid range : 16bit to 32bit 010000 : 16bit 011000 : 24bit (default) 100000 : 32bit 000000 to 001111 : Reserved 100001 to 111111 : Reserved
		3:0	Reserved	0000	R	Reserved
0x16	2	15:3	Reserved	13'h0000	R	Reserved
		2	HPF_VS_EN	1	R/W	0 : Disable HPF for voltage sense 1 : Enable HPF for voltage sense (default)
		1	HPF_IS_EN	1	R/W	0 : Disable HPF for current sense 1 : Enable HPF for current sense (default)
		0	HPF_AUD_IN_EN	1	R/W	0 : Disable HPF for audio in 1 : Enable HPF for audio in (default)
0x24	2	15:9	Reserved	0000000	R	Reserved
		8	HARD_CLIP_EN	1	R/W	0 : Disable hard clipping 1 : Enable hard clipping (default)
		7:0	HARD_CLIP_TH	00000000	R/W	Hard clip threshold if HARD_CLIP_EN = 1 Downward, 12 to –115.5dB in 0.5dB step, (default 00000000 = 12dB) e.g. 00000001 = 11.5dB Equation : Hard Clip threshold = (HARD_CLIP_TH (DEC) x –0.5dB) + 12dB

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x28	2	15:3	Reserved	13'h0000	R	Reserved
		2:0	VOLCTRL	000	R/W	Ramp control when new volume setting is different from old setting : 000 : No ramp up/down (default) 001 : 0.5dB per sample 010 : 0.5dB per 2 samples 011 : 0.5dB per 4 samples 100 : 0.5dB per 8 samples 101 : 0.5dB per 16 samples 110 : 0.5dB per 32 samples 111 : 0.5dB per 64 samples
0x29	2	15:8	Reserved	00000000	R	Reserved
		7:0	VOLUME	00011000	R/W	Volume, downward 12 to −115.5dB in −0.5dB step, (default 00011000 = 0dB) e.g. 00000000 = 12dB Equation : Digital volume = (VOLUME (DEC) x −0.5dB) + 12dB
0x30	2	15:4	Reserved	12'h000	R	Reserved
		3:1	VBCPS	001	R/W	Clip threshold setting 000 : 3.9V 001 : 3.75V (default) 010 : 3.6V 011 : 3.45V 100 : 3.3V 101 : 3.15V 110 : 3V 111 : 2.85V
		0	CLPE	1	R/W	0 : Disable clip 1 : Enable clip (default)

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x31	2	15:14	CLIPRR	00	R/W	Rate of V_O threshold recover when V_{BAT} return 00 : Increase by 1/8 of original Vo per 1s (default) 01 : Increase by 1/1024 of original Vo per 5ms 10 : Increase by 1/4096 of original Vo per 5ms 11 : Increase by 1/8192 of original Vo per 5ms
		13:12	CLIPDR	00	R/W	Rate of V_O threshold drop when V_{BAT} is low 00 : 1/1024 of original Vo per sample (default) 01 : 1/256 of original Vo per sample 10 : 1/16 of original Vo per sample 11 : 1 step to target
		11:10	BVHYS	00	R/W	Battery voltage recovery hysteresis 00 : Battery voltage + 0.05 (default) 01 : Battery voltage + 0.1 10 : Battery voltage + 0.15 11 : Battery voltage + 0.2
		9:0	CPSLP	1000000000	R/W	Clip slope setting : For example, set clip slope = 12, signal path gain = 11.1 CPSLP value (DEC) = Clip slope × 256 / Signal path gain CPSLP value (Bin) = 0100010100 CPSLP value (Bin) =1000000000 (default), the clip slope is 22.2.
0x32	2	15:0	VOMIN	16'h1DDD	R/W	Minimum Clip threshold converted from (V) For example, set minimum clip threshold = 2.85V, signal path gain = 11.1 VOMIN (DEC) = 2.85 × 32768 / Signal path gain VOMIN (HEX) = 20DD Set VOMIN = 1DDD (default), signal path gain = 11.1, minimum clip threshold = 2.59V. 16’b0 : No minimum

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x40	2	15:12	Reserved	0000	R	Reserved
		11	EQU_SAMP_DOWN_PEAK_EN	1	R/W	0 : Disable EQU_SAMP_DOWN_PEAK function 1 : Enable to decrease signal peak by slew rate when 2 adjacent samples are equal in class-H mode when hold time is expired (default)
		10	max_audio_in12_en	1	R/W	0 : Audio_in1 = audio_in1 1 : Audio_in1 = max (audio_in1, audio_in2) (default)
		9	SLEW_LIMIT_EN	1	R/W	0 : Slew limit disable for boost class-H 1 : Slew limit enable for boost class-H (default) (Slew limit refers to SLEW_RATE)
		8	CLASS_H_EN	1	R/W	0 : Boost class-G 1 : Boost class-H (default)
		7:6	BST_TOT	01	R/W	0 : Disable EQU_SAMP_DOWN_PEAK function 1 : Enable to decrease signal peak by slew rate when 2 adjacent samples are equal in class-H mode when hold time is expired (default)
		5:4	SLEW_RATE	01	R/W	When in boost mode -G, the up/down slew rate is 00: 2.5mV/μs 01: 5mV/μs (default) 10: 10mV/μs 11: 20mV/μs When in boost mode-H, the rate of signal peak going up is no limit, but going down to current signal is limited by SLEW_RATE 00 : 0.75mV/μs 01 : 1.5mV/μs (default) 10 : 3.0mV/μs 11 : 6.0mV/μs
		3	PSM_EN	1	R/W	0 : Disable PSM 1 : Enable PSM (default)
		2	DCM_EN	1	R/W	0 : Disable DCM 1 : Enable DCM (default)
		1:0	BST_MODE	00	R/W	Boost mode 00 : Disable (default) 01 : Battery 10 : Fixed 11 : Adaptive

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x41	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT1	000011	R/W	Class-G : VBST target in fixed mode or highest VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT1 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V 000011 : 3.5V (default) 110001 to 111111 : Reserved Class-H : Head room for output signal = 1.1V + (BST_THT1 x 0.2V), Head room = 1.7V (default) e.g. 000000 : 1.1V, 000100 : 1.9V
		5:0	BST_TH1	101111	R/W	Class-G : Boost threshold for BST_THT1 000000 : Disabled 000001 to 110001 : 1.3V + (BST_TH1 x 0.2 V) e.g. 000001 : 1.5V, 100001 : 7.9V 101111 : 10.7V (default) 110010 to 111111 : Reserved Class-H : Set the maximum of VBST = 9.5V + (BST_TH1[3:0] x 0.2V), the maximum of VBST = 12.5V (default) e.g. BST_TH1[3:0] = 1100, the maximum of VBST = 11.9V
0x42	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT2	100001	R/W	Middle VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT2 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V (default) 110001 to 111111 : Reserved
		5:0	BST_TH2	011011	R/W	Boost threshold for BST_THT2 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH2 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 011011: 6.7V (default) 110001 to 111111 : Reserved

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x43	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT3	010111	R/W	Lower VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT3 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V, 010111 : 7.5V (default) 110001 to 111111 : Reserved
		5:0	BST_TH3	001111	R/W	Boost threshold for BST_THT3 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH3 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 001111 : 4.3V (default) 110001 to 111111 : Reserved
0x44	2	15:12	Reserved	0000	R	Reserved
		11:6	BST_THT4	001011	R/W	Lowest VBST target in adaptive mode 000000 : Disabled 000001 to 110000 : 2.9V + (BST_THT4 x 0.2V) e.g. 000001 : 3.1V, 100001 : 9.5V, 001011 : 5.1V (default) 110001 to 111111 : Reserved
		5:0	BST_TH4	000111	R/W	Boost threshold for BST_THT4 000000 : Disabled 000001 to 110000 : 1.3V + (BST_TH4 x 0.2V) e.g. 000001 : 1.5V, 100001 : 7.9V 000111 : 2.7V (default) 110001 to 111111 : Reserved
0x45	2	7:0	CC_MAX	10001000	R/W	01101000 : 4A 01111000 : 5A 10001000 : 6A (default) 10011000 : 7A CC_MAX resolution is 62.5mA/per code.

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x46	2	15:7	Reserved	000000000	R	Reserved
		6	OTP_MODE	0	R/W	0 : Digital OTP to trigger auto-recovery (default) 1 : Analog OTP flag to trigger auto-recovery
		5	BST_OCP_MODE	1	R/W	0 : Boost digital OCP if OCP_PROT_EN = 1 1 : Boost Analog OCP for limit PWM duty (without OCP) (default)
		4	AMP_OCP_PROT_EN	1	R/W	0 : Disable speaker OCP protection 1 : Enable speaker OCP protection (default)
		3	OVP_PROT_EN	1	R/W	0 : Disable OVP protection 1 : Enable OVP protection (default)
		2	UVP_PROT_EN	1	R/W	0 : Disable UVP protection 1 : Enable UVP protection (default)
		1	BST_OCP_PROT_EN	1	R/W	0 : Disable boost OCP protection 1 : Enable boost OCP protection (default)
		0	OTP_PROT_EN	1	R/W	0 : Disable OTP protection 1 : Enable OTP protection (default)
0x47	2	15:9	Reserved	0000000	R	Reserved
		8:0	VPTAT_code	0	R	VPTAT code (DEC) = Chip temperature (°C) + 273°C e.g. VPTAT code = 100101010, VPTAT code (DEC) = 298, chip temperature = 25°C
0x48	2	15:10	Reserved	000000	R	Reserved
		9:0	VBAT_code	0	R	Battery voltage (V) = VBAT code (DEC) / 160 e.g. 1010000000 = 640 (DEC), Battery voltage = 640 / 160 = 4V
0x68	2	15:5	Reserved	00000000000	R	Reserved
		4	timeout_disable	0	R/W	0 : Enter DRE if timeout to find zero crossing (default) 1 : Not enter DRE if timeout to find zero crossing
		3	dre_method_sel	0	R/W	0 : Enter DRE at zero crossing (default) 1 : Enter DRE if signal < threshold
		2:1	DRE_HOLD_SEL	10	R/W	Hold time before entering DRE 00 : 16ms 01 : 32ms 10 : 64ms (default) 11 : 128ms
		0	DRE_EN	1	R/W	0 : Disable DRE 1 : Enable DRE (default)

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Address	Byte	Bits	Bits Name	Default	Type	Description
0x69	2	15:8	Reserved	00000000	R	Reserved
		7:0	DRE_THDMODE	01000000	R/W	Threshold = 20log (DRE_THDMODE (DEC) × 2 ^ (-11)), DRE_THDMODE = −30.1dB (default)
0x6A	2	15:10	Reserved	000000	R	Reserved
		9:0	D_FINE_RISING	0000000000	R/W	Fine tune the enter time of digital dre (= D_FINE_RISING(DEC) /12M)= 0s (default)
0x6B	2	15:10	Reserved	000000	R	Reserved
		9:0	D_FINE_FALLING	0000000000	R/W	Fine tune the leave time of digital dre (= D_FINE_FALLING(DEC) /12M) = 0s (default)
0x6C	2	15:10	Reserved	000000	R	Reserved
		9:0	A_FINE_RISING	0000000000	R/W	Fine tune the enter time of analog dre (= A_FINE_RISING(DEC) /12M) = 0s (default)
0x6D	2	15:10	Reserved	000000	R	Reserved
		9:0	A_FINE_FALLING	0000000000	R/W	Fine tune the leave time of analog dre (= A_FINE_FALLING (DEC)/12M) = 0s (default)
0x74	2	15:8	Reserved	00000000	R	Reserved
		7	DC_FLAG	0	R	0 : The DC condition is not occur (default) 1 : Indicate the DC condition is detected. It will be automatically clear when AMP is enabled.
		6:5	Reserved	00	R	Reserved
		4	DC_PROT_EN	0	R/W	0 : Disable DC protect (default) 1 : Enable DC protect
		3:2	DC_TIME_SEL	00	R/W	If the DC voltage > DC_TH for DC_TIME, the DC condition is detected and DC_FLAG = 1 00 : 100ms (default) 01 : 500ms 10 : 1000ms 11 : 1000ms
		1:0	DC_TH_SEL	00	R/W	DC threshold 00 : 0.5V (default) 01 : 1.0V 10 : 2.0V 11 : 2.0V
0xA6	2	9:8	D_SET_VDDP_OV	00	R/W	VDDP over-voltage threshold setting (rising) 00 : 16.6V (default) 01 : 15.7V 10 : 14.8V 11 : 14.1V

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Address	Byte	Bits	Bits Name	Default	Type	Description
0xB6	2	15:14	Reserved	11	R	Reserved
		13	D_CS_EN	1	R/W	0 : Disable current sense 1 : Enable current sense (default)
		12	D_CSVS_REFBUF_EN	1	R/W	Current / Voltage reference buffer 0 : Disable 1 : Enable (default)
		11	D_VS_EN	1	R/W	0 : Disable voltage sense 1 : Enable voltage sense (default)
		10	D_VS_BIAS	1	R/W	0 : Half voltage sense bias current 1 : Max. voltage sense bias current (default)
		9:5	Reserved	11111	R	Reserved
		4:0	IDAC_GAIN_SEL [4:0]	10010	R/W	Gain range 0dB to 23dB 00000 : 0dB 00001 : 1dB … 10010 : 18dB (default) 10111 : 23dB Others : Reserved

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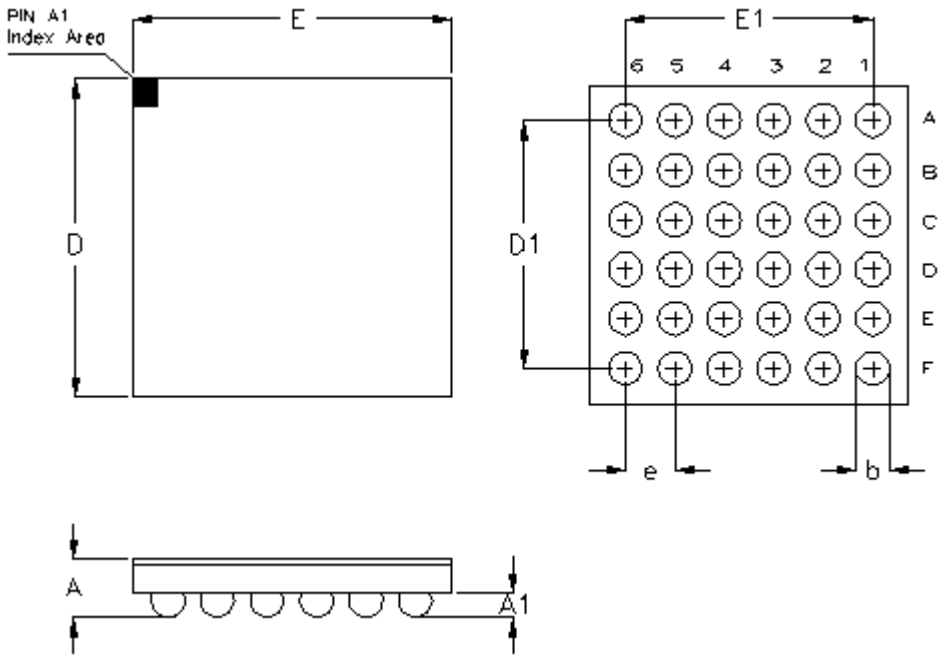
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.420	0.520	0.017	0.020
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.530	2.610	0.100	0.103
D1	2.000		0.079	
E	2.530	2.610	0.100	0.103
E1	2.000		0.079	
e	0.400		0.016	

36B WL-CSP 2.57x2.57 Package (BSC)

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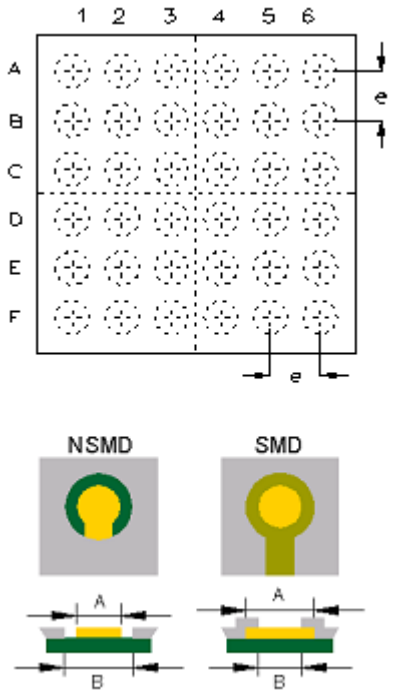
Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.57*2.57-36(BSC)	36	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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