2.4MHz 1A Step-Down Converter with I²C Interface

General Description

The RT5721 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface capable of operating up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the RT5721 is capable of delivering 1A continuously at over 80% efficiency, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 45μA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed- frequency control, operating at 2.4MHz. In the Shutdown Mode, the supply current drops below 1μA, reducing power consumption. The PFM Mode can be disabled if fixed frequency is desired. The RT5721 is available in a small WL-CSP-11B 1.31x1.62 (BSC).

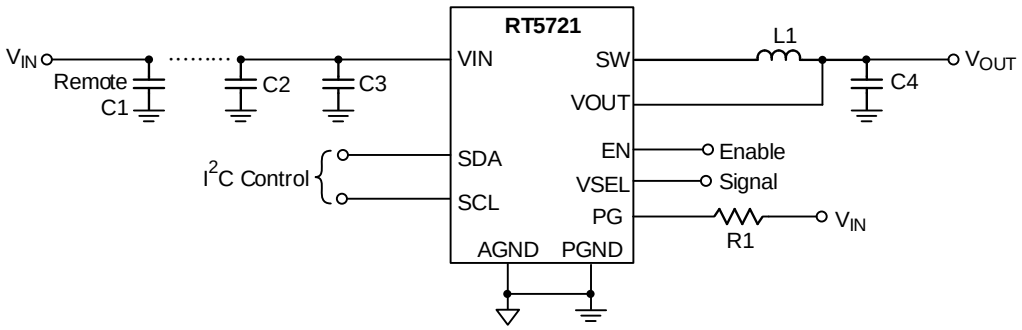
Features

- **Steady 2.4MHz Switching Frequency**
- **Fast Load Transient**
- **Continuous Output Current Capability: 1A**
- **2.5V to 5.5V Input Voltage Range**
- **Digitally Programmable Output Voltage**
  - **0.3V to 1.3V Programmable Slew Rate for Voltage Transitions**
- **I²C-Compatible Interface Up to 3.4MHz**
- **PFM Mode for High Efficiency in Light Load**
- **Quiescent Current in PFM Mode: 45μA (Typical)**
- **Input Undervoltage Lockout (UVLO)**
- **Thermal Shutdown and Overload Protection**
- **Power Good Indicator**

Applications

- **Application, Graphic, and DSP Processors**
  - **ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, etc.**
- **Hard Disk Drives, LPDDR3, LPDDR4**
- **Tablets, Netbooks, Ultra-Mobile PCs**
- **Smart Phones**
- **Gaming Devices**

Simplified Application Circuit



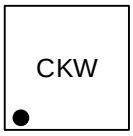
Ordering Information

Product	Power-Up Defaults		EN Delay Time	Package Type
	VSEL0	VSEL1		
RT5721AP-A	0.9V	0.8V	0ms	WL-CSP-11B 1.31x1.62 (BSC)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

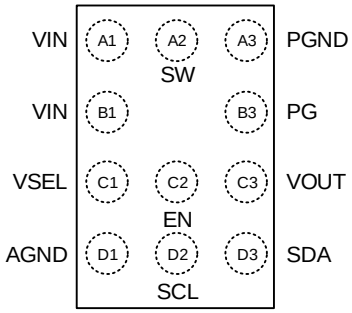
Marking Information



CK: Product Code
W: Date Code

Pin Configuration

(TOP VIEW)



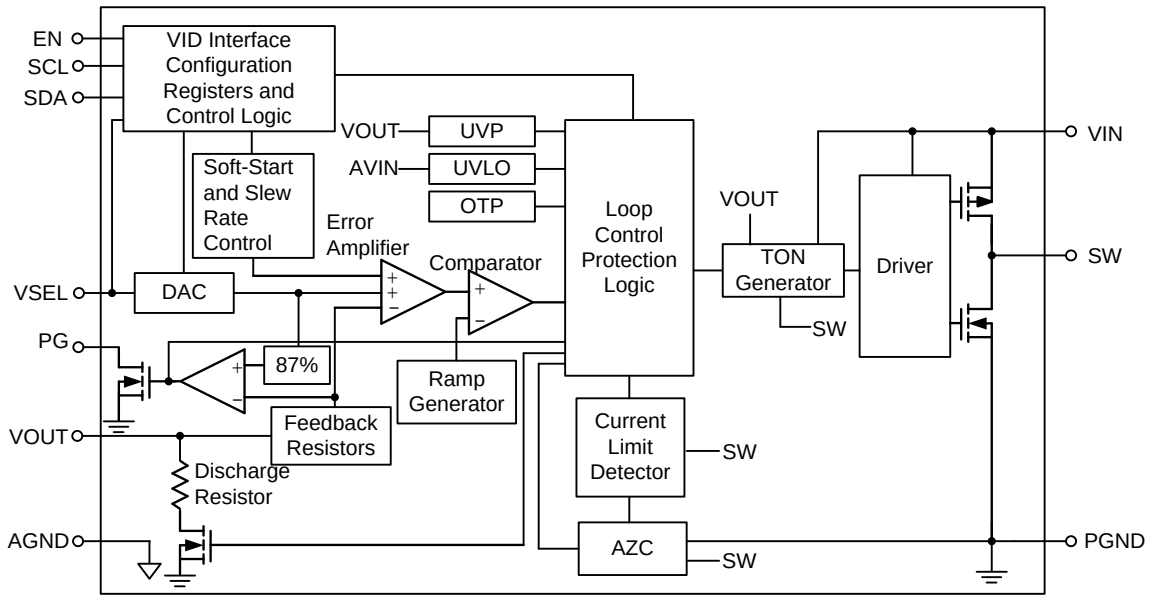
WL-CSP-11B 1.31x 1.62 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B1	VIN	Power input voltage. Connect to the input power source. Connect to CIN with minimal path.
A2	SW	Switching node. Connect to the inductor.
A3	PGND	Power ground. The low-side MOSFET is referenced to this pin. CIN and COUT should be returned with a minimal path to these pins.
B3	PG	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. After soft-startup, PG is pulled up when the FB voltage is within 87% (typ.). The PG status is low while EN is disabled. Note that when VIN is lower than 2.32V (typ.), the PG pin will keep low to indicate the power is not ready.
C1	VSEL	Voltage select. When this pin is low, VOUT is set by the VSEL0 register. When this pin is high, VOUT is set by the VSEL1 register. Polarity of this pin in conjunction with the mode bits in the Control register 02h will select Forced PWM or Auto PFM/PWM mode of operation.
C2	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode, and will reset all registers to the default value.
C3	VOUT	VOUT. Output voltage sense through this pin. Connect to output capacitor.
D1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.

Pin No.	Pin Name	Pin Function
D2	SCL	I^2C serial clock.
D3	SDA	I^2C serial data.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 7V
- Switch Node Voltage ---------- –0.3V to 7.3V
  <50ns ---------- –5V to 8.5V
- Other I/O Pins Voltages ---------- –0.3V to 7.3V
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WL-CSP-11B 1.31x1.62 (BSC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	49.9	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	2.1	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	65.4	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.1	°C/W

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Quiescent Current PWM		I_{Q_PWM}	I_{LOAD} = 0, mode Bit = 1 (Forced PWM)	--	15	--	mA
Operating Quiescent Current PFM		I_{Q_PFM}	I_{LOAD} = 0	--	45	--	μA
H/W Shutdown Supply Current		$I_{SHDN\_H/W}$	EN = GND	--	0.1	3	μA
S/W Shutdown Supply Current		$I_{SHDN\_S/W}$	EN = V_{IN}, 0x06[1:0] = 2'b00, 2.5V ≤ V_{IN} ≤ 5.5V	--	2	12	μA
Undervoltage Lockout Threshold		V_{UVLO}	V_{IN} rising	--	2.32	2.45	V
Undervoltage Lockout Hysteresis		ΔV_{UVLO}		--	350	--	mV
High-Side Switch-On Resistance		$R_{DS(ON)\_H}$	V_{IN} = 5V	--	60	--	mΩ
Low-Side Switch-On Resistance		$R_{DS(ON)\_L}$	V_{IN} = 5V	--	34	--	mΩ
Enable Threshold Voltage	Logic-High	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V	0.74	0.9	1.06	V
	Logic-Low	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V	0.64	0.8	0.92	
Enable Input Bias Current		I_{EN}	EN Pin tied to GND or VIN	--	0.01	1	μA
VOUT DC Accuracy			2.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} from minimum to maximum, $I_{OUT(DC)}$ = 0A to 1A, Auto PFM/PWM (Note 6)	–3	--	5	%
			2.5V ≤ V_{IN} ≤ 5.5V, V_{OUT} from minimum to maximum, $I_{OUT(DC)}$ = 0A to 1A, Forced PWM (Note 6)	–1.5	--	1.5	%
Load Regulation		ΔV_{LOAD}	$I_{OUT(DC)}$ = 0.5A to 1A (Note 6)	--	0.1	--	%/A
Line Regulation		ΔV_{LINE}	2.5V ≤ V_{IN} ≤ 5.5V, $I_{OUT(DC)}$ = 1A (Note 6)	--	0.2	--	%/V
Transient Load Response		AC_{LOAD}	I_{LOAD} step 0.01A to 1A, t_R = t_F = 500ns, V_{OUT} = 1.125V (Note 6)	--	±45	--	mV
Transient Load Response		AC_{LOAD}	I_{LOAD} step 0.01A to 0.8A, t_R = t_F = 1μs, L = 0.33μH, C_{OUT} = 22μF x 2 (Note 5)	--	45	--	mV
Line Transient		V_{LINE}	V_{IN} = 3V to 3.6V, t_R = t_F = 10μs, I_{OUT} = 100mA, Forced PWM mode (Note 6)	--	±40	--	mV
High-Side MOSFET Peak Current Limit		I_{LIM_P}		--	3.15	--	A
Low-Side MOSFET Valley Current Limit		I_{LIM_V}		--	1.67	--	A
Thermal Shutdown		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	15	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency	f_{SW}		2100	2400	2700	kHz
Minimum Off-Time	t_{OFF_MIN}		--	170	--	ns
DAC Resolution		(Note5)	--	8	--	bits
DAC Differential Nonlinearity		(Note5)	--	--	0.5	LSB
Power Good						
Power Good Threshold	V_{TH_PGLH}	V_{OUT} rising, PGOOD from low to high	--	87	--	% of V_{REF}
	V_{TH_PGHL}	V_{OUT} falling, PGOOD from high to low	--	77	--	
Power Good Falling Delay Time			--	3	--	μs
I^2C Interface (The I^2C interface will not work until the RESET# goes high) (Note 5)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
SDA, SCL Input Voltage — High Level			1.2	--	--	V
SDA, SCL Input Voltage — Low Level			--	--	0.4	V
SCL Clock Rate	f_{SCL}	Fast mode	--	--	400	kHz
		Fast plus mode	--	--	1	MHz
		High speed mode, load 100pF max	--	--	3.4	MHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	μs
		High speed mode	0.16			μs
Low Period of the SCL Clock	t_{LOW}	Fast mode	1.3	--	--	μs
		Fast plus mode	0.5	--	--	μs
		High speed mode	0.16			μs
High Period of the SCL Clock	t_{HIGH}	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	μs
		High speed mode	0.06			μs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	μs
		High speed mode	0.01			μs
Data Hold Time	$t_{HD;DAT}$	Fast mode	0	--	--	μs
		Fast plus mode	0	--	--	μs
		High speed mode	0	--	--	μs
Data Set-Up Time	$t_{SU;DAT}$	Fast mode	100	--	--	ns
		Fast plus mode	50	--	--	ns
		High speed mode	10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-Up Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	μs
		High speed mode	0.16	--	--	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	Fast mode	1.3	--	--	μs
		Fast plus mode	0.5	--	--	μs
Rising Time of both SDA and SCL Signals	t_R	Fast mode	20	--	300	ns
		Fast plus mode	--	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
Falling Time of both SDA and SCL Signals	t_F	Fast mode	20×(VDD/5.5V)	--	300	ns
		Fast plus mode	20×(VDD/5.5V)	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
Falling Time of both SDA and SCL Signals	t_F	Fast mode	20×(VDD/5.5V)	--	300	ns
		Fast plus mode	20×(VDD/5.5V)	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm, furthermore, all layers with 1 oz. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. Guaranteed by design.

Typical Application Circuit

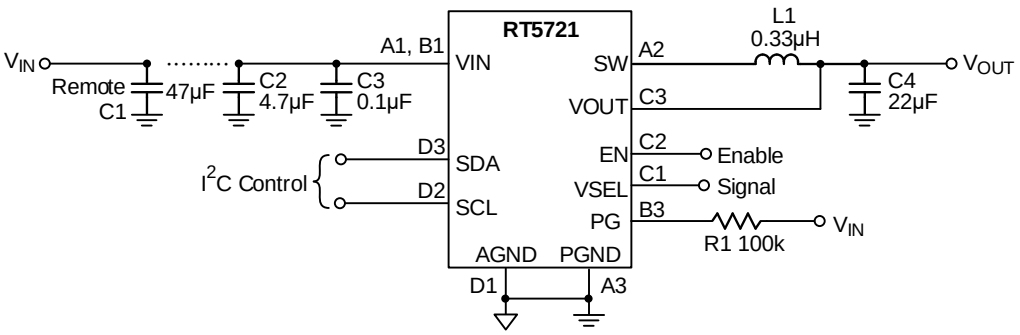


Table 1. Recommended External Components for 1A Maximum Load Current

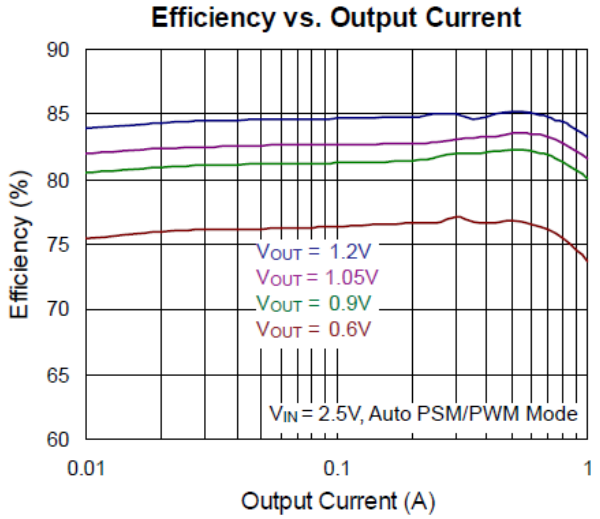
Component	Description	Vendor P/N
L1	330nH, 2016 case size	DFE201610E-R33M=P2 (Murata)
		HMMQ20161T-33MDR (Cyntec)
C2	4.7µF, 10V, X5R, 0402	ZRB15XR61A475ME01D (Murata)
C3(1)	100nF, 6.3V, X5R, 0201	GRM033R60J104KE19D (Murata)
C4	22µF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
		C1608X5R0J226M080AC (TDK)

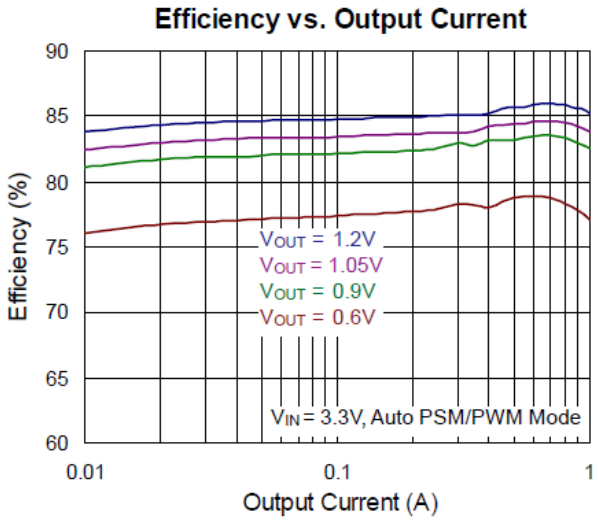
Note:

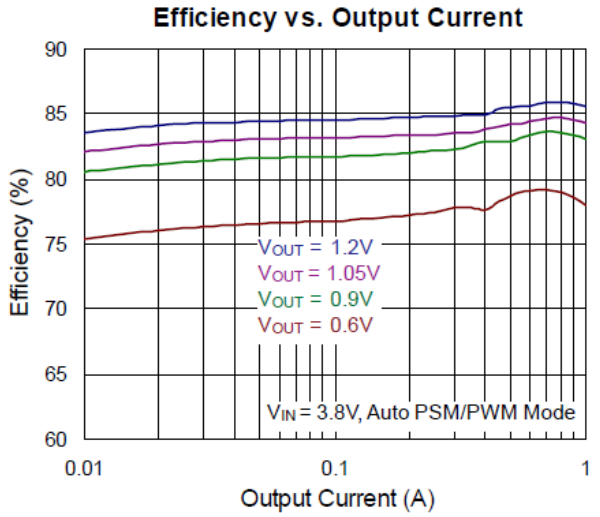
1. The decoupling capacitor C3 is recommended to reduce any high frequency component on VIN bus.
2. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

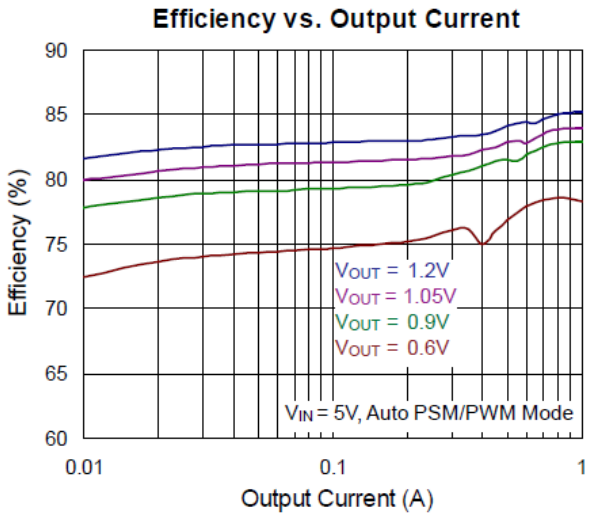
Typical Operating Characteristics

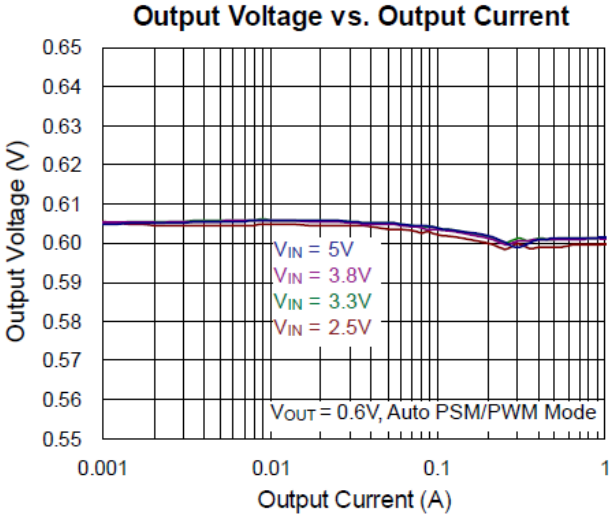
Unless otherwise specified, Auto PFM/PWM mode, T_A = 25°C; circuit and components according to typical application circuit and Table 2.

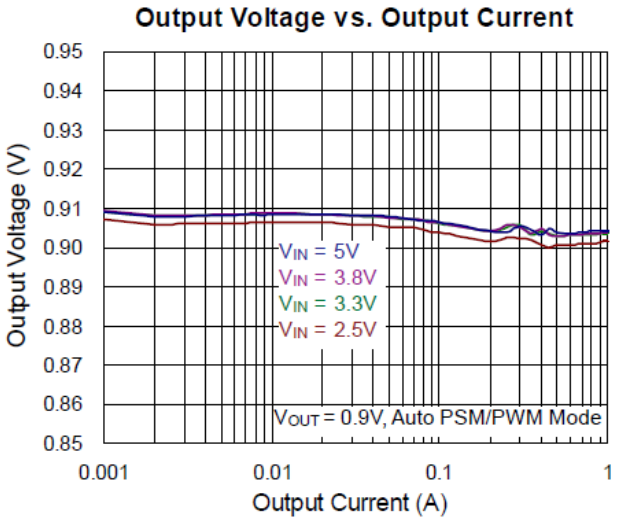




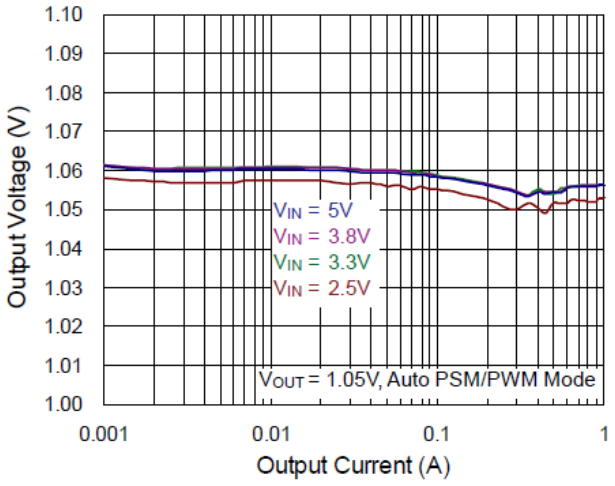




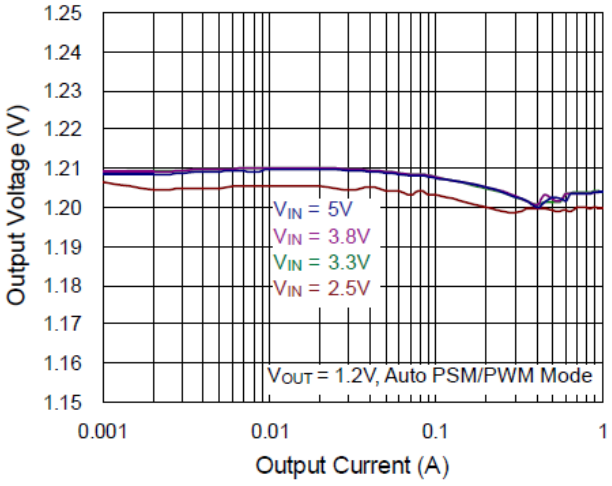




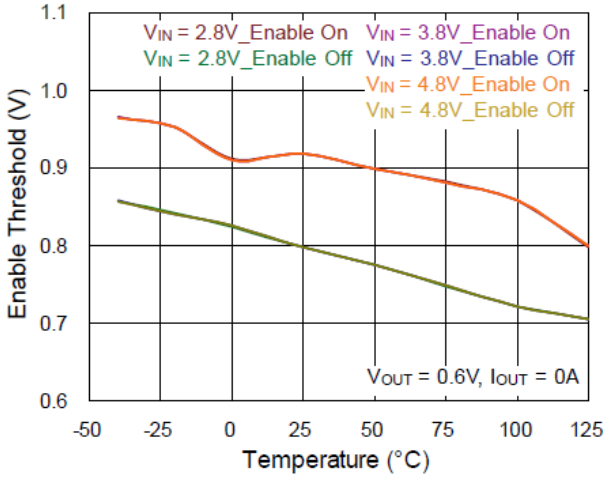
Output Voltage vs. Output Current



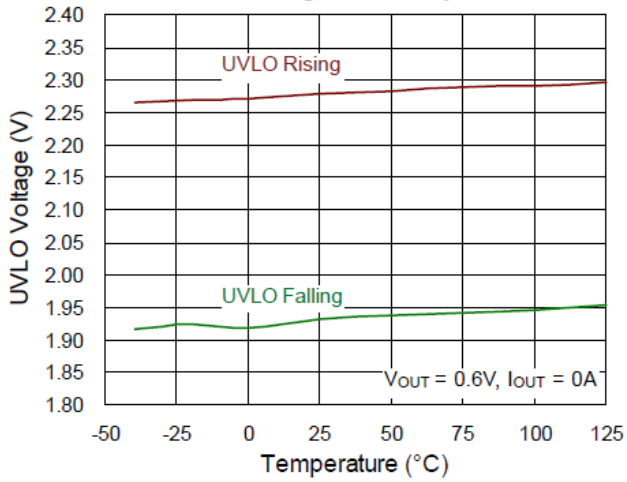
Output Voltage vs. Output Current



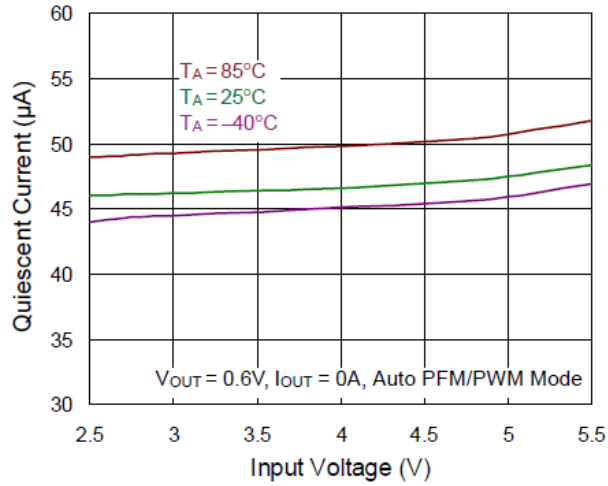
Enable Threshold vs. Temperature



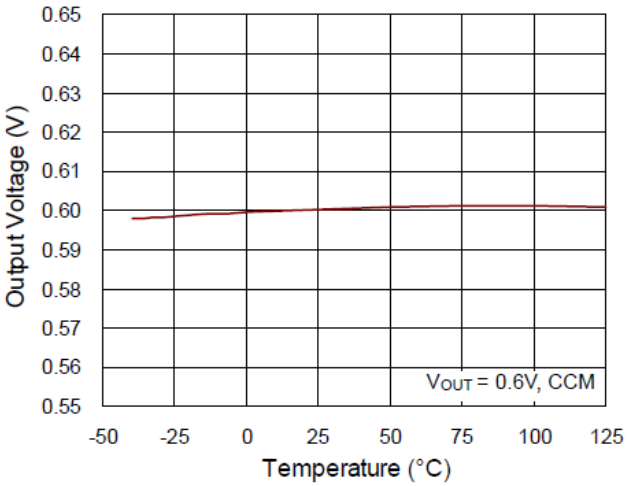
UVLO Voltage vs. Temperature



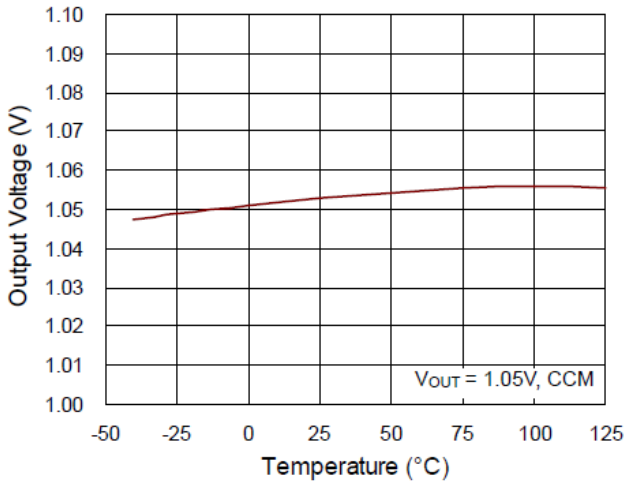
Quiescent Current vs. Input Voltage



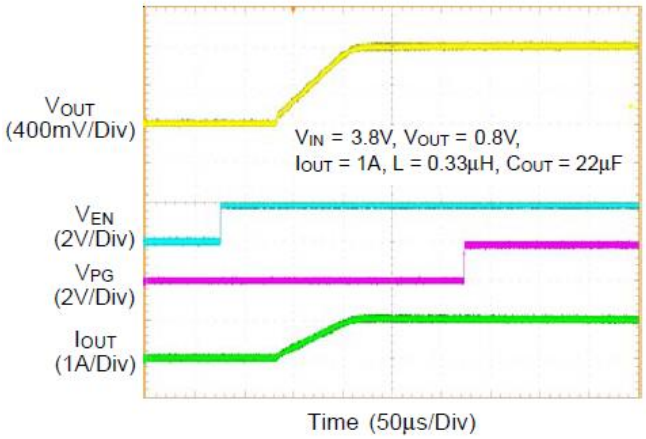
Output Voltage vs. Temperature



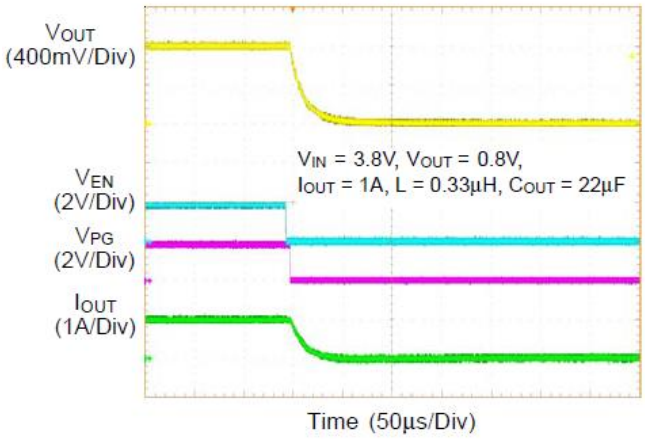
Output Voltage vs. Temperature



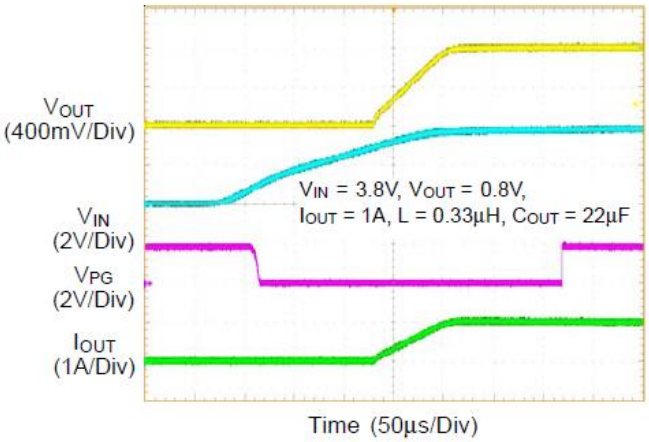
Power On from EN



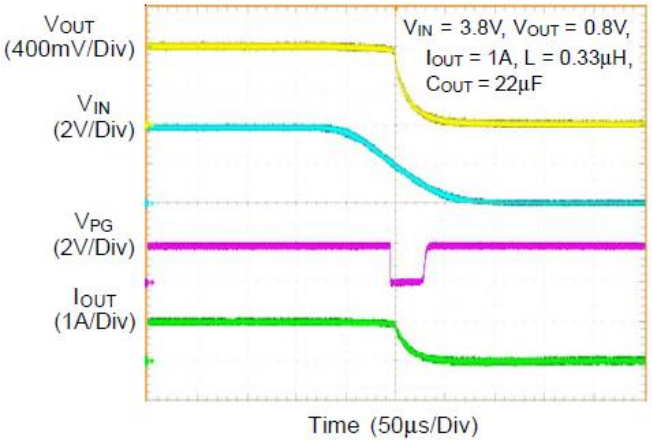
Power Off from EN



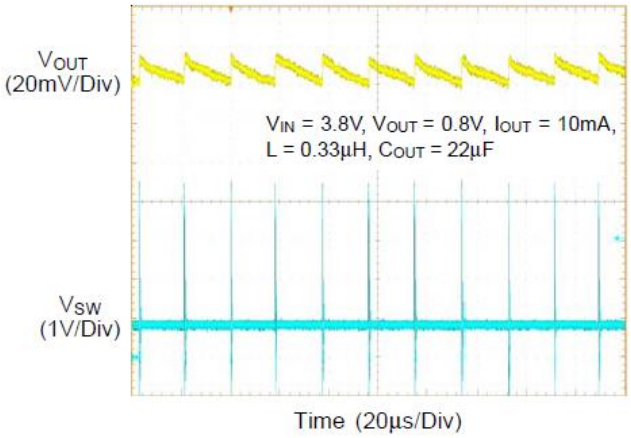
Power On from VIN



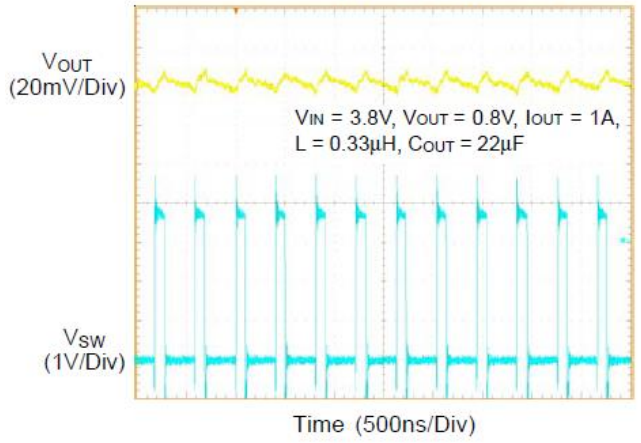
Power Off from VIN



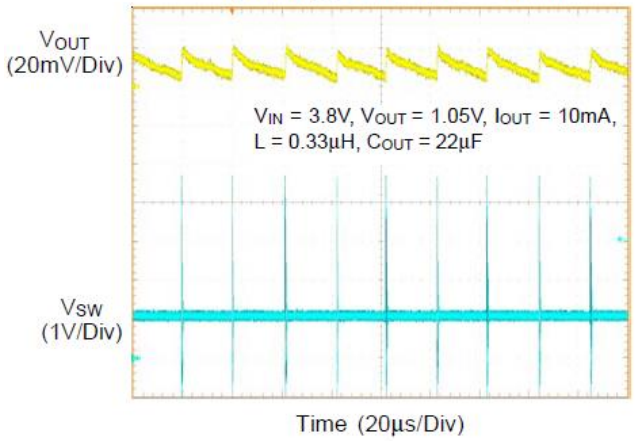
Output Ripple as I_{OUT} = 10mA



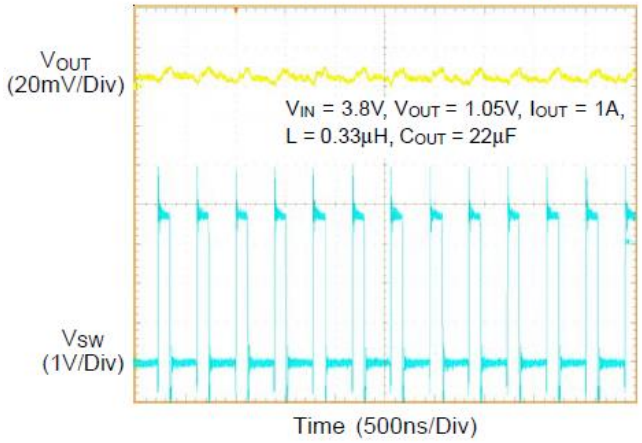
Output Ripple as I_{OUT} = 1A



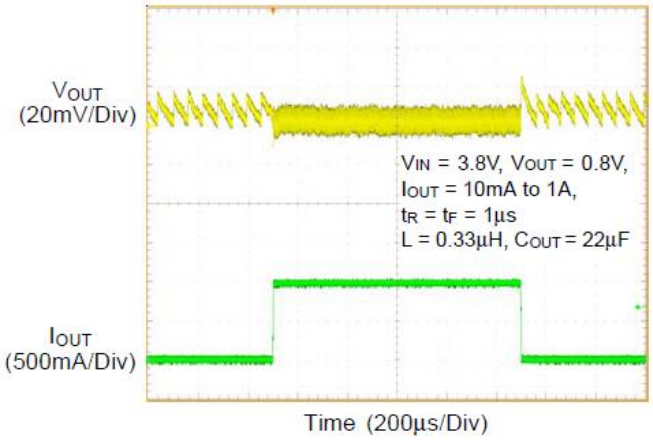
Output Ripple as I_{OUT} = 10mA



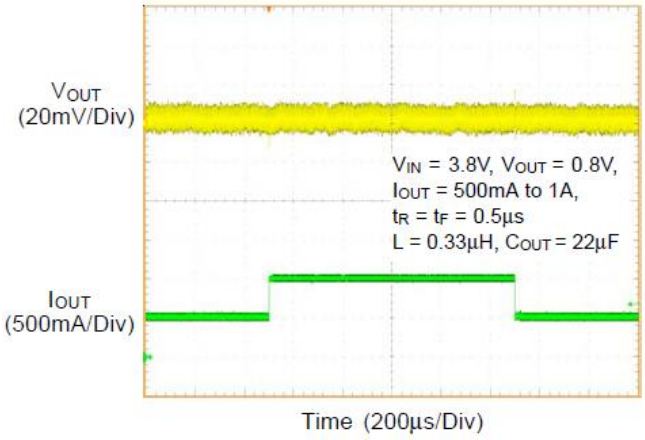
Output Ripple as I_{OUT} = 1A



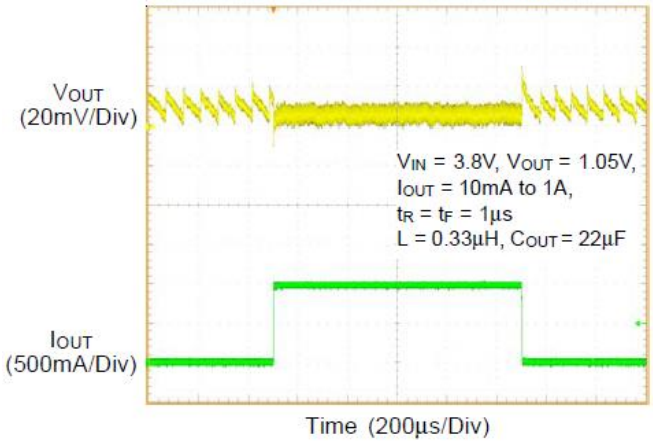
Load Transient Response



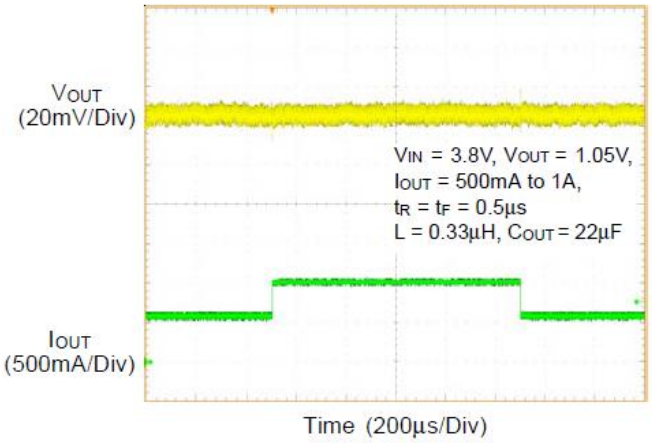
Load Transient Response



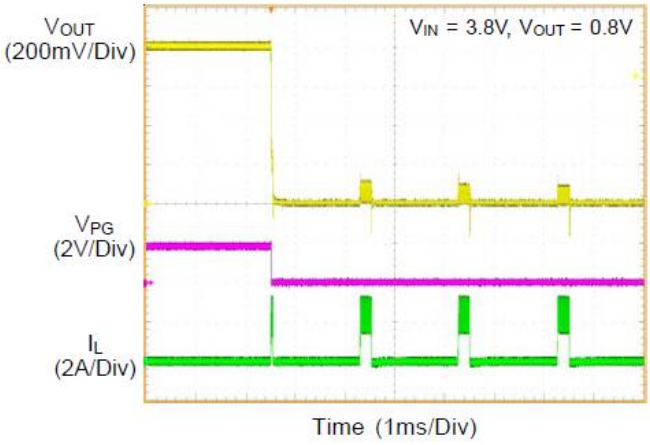
Load Transient Response



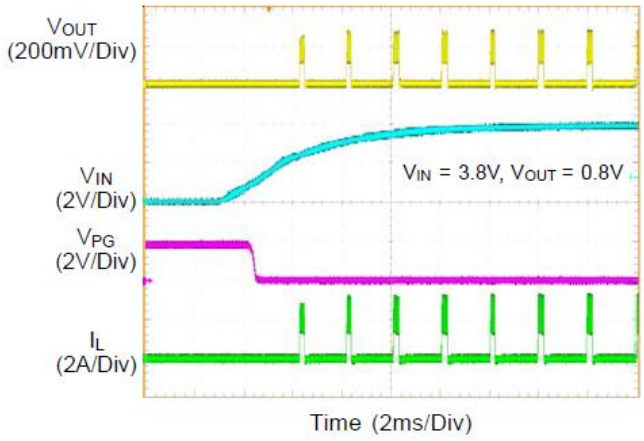
Load Transient Response



Over-Current Protection



Short-Circuit before Power On



Operation

The RT5721 is a low voltage synchronous step-down converter that supports input voltage ranging from 2.5V to 5.5V and the output current can be up to 1A. The RT5721 uses ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is cleared and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allows the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominal 2.4MHz.

Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decrease to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to get better efficiency.

Undervoltage Protection (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VCC is high enough to reach the high threshold voltage of UVLO, the step-down converter softly starts or pre-biases to its regulated output voltage. When the VIN decreases to its low threshold (160mV hysteresis), the device will shut down.

Power Good Indication Pin

The RT5721 features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to VOUT or an external voltage below 5.5V. When VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft- start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{OUT}. If V_{OUT} rises above a power-good high threshold (V_{TH_PGLH}) (typically 87% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. Moreover, when VIN is above UVLO and device is powered on through EN pin, the PG pin will assert high within 300μs as soon as the V_{EN} is above logic-high threshold; in other words, the PG delay time is around 300μs from EN asserts to logic-high. When V_{OUT} falls below the power-good low threshold (V_{TH_PGHL}) (typically 77% of the reference voltage), the PG pin will be pulled low after a certain delay (3μs, typically). Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull down device (11Ω, typically) will pull the PG pin low. The power good indication profile is shown in Table 1. Note that when VIN is lower than 2.32V (typically), the PG pin will keep low to indicate the power is not ready.

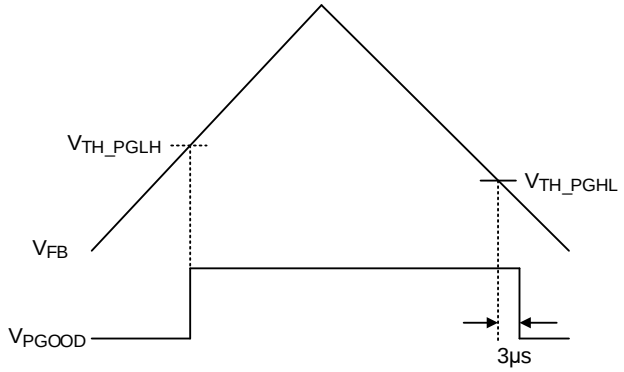


Figure 1. The Logic of PG

Table 2. PG Pin Status

Conditions		PG Pin
Enable	$V_{EN} > V_{EN\_H}$, $V_{FB} > V_{TH\_PGLH}$	High Impedance
	$V_{EN} > V_{EN\_H}$, $V_{FB} < V_{TH\_PGHL}$	Low
Shutdown	$V_{EN} < V_{EN\_L}$	Low
OTP	$T_J > T_{SD}$	Low

Overcurrent Protection (OCP)

When the output voltage of the RT5721 is lower than 59% of the reference voltage after soft-start, the UVP is triggered.

The RT5721 senses the current signal when high-side and low-side MOSFET turns on. As a result, the OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next pulse and turns on low-side switch until inductor drops below the valley current limit, and then turns on high-side again to maintain output voltage and supports loading current to output before triggering UVP.

If the OCP condition keeps and the load current is larger than the current which converter can provide, the output voltage will decrease and drop below UVP threshold, and the converter will keep switching for 16 consecutive cycles before entering hiccup operation. The converter latches off 1.7ms when the output voltage is still lower than UVP threshold, and the soft-start sequence begins again after latching off time.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time can be programming by I^2C.

Over-Temperature Protection (OTP)

The RT5721 has over-temperature protection. When the device triggers the OTP, the device shuts down.

Overvoltage Behavior (OV)

The RT5721 provides a natural overvoltage protection function to prevent damage behavior during heavy load released scenario.

When device is set at auto PFM/PWM operation, the high-side and low-side MOSFET will automatically turn off immediately as long as output voltage rises above internal reference target. When the output voltage goes below the target, the internal comparator will trigger on-time controller to resume switching behavior to maintain excellent regulation.

When device is configured as FCCM operation mode, the high-side and low-side MOSFET will continuously switch to regulate the output voltage back to target setting.

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The basic RT5721 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher VIN and decreases with higher inductance, as shown in the equation below:

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance.

To optimize the loop stability, 0.33μH is strongly recommended. Suppose the higher inductance is chosen, the transient performance may become worse; in the opposite situation, the lower inductance causes larger ripple, and there is a risk of reaching negative overcurrent protection during VID down.

Input and Output Capacitor Selection

An input capacitor, CIN, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at VIN = 2V_{OUT}, where $I_{RMS} = I_{OUT(MAX)}/2$.

This simple worst-case condition is commonly used for design.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right]$$

where f_{SW} is the switching frequency and ΔI_L is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement.

Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Nevertheless, high value, low cost ceramic capacitors

are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

I²C Interface Function

The RT5721 can be managed by I²C interface to select VOUT voltage level, Dynamic Voltage Scaling (DVS) slew rate, Auto PFM/PSM or Forced PWM mode, and so on.

The register of each function can be found from the following register map, which also explains how to use these functions.

VOUT Selection

The RT5721 has programmable VOUT from 0.3V to 1300mV with 5mV resolution.

The output voltage can be set by NSELx register bit and the output voltage is given by the following equation:

V_{OUT} = 0.3V + NSELx x 5mV

For example:

if NSELx = 0111100 (60 decimal), then

V_{OUT} = 0.3 + 60 x 5mV

= 0.3 + 0.3 = 0.6V.

The RT5721 also has external VSEL pin to select NSEL1(0X01) or NSEL0(0X00). Pulling VSEL to high is for VSEL1 and pulling VSEL to low is for VSEL0.

Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

Enable and Soft-Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I2C cannot be written to or read until input voltage is above the UVLO. The registers are reset when the EN pin is LOW or during a Power On Reset (POR).

Once the EN pin is high, VOUT will ramp up at the chosen soft-start slew rate programmed in the CONTROL2 register SS_SR bit.

Discharge Function

In the CONTROL1 register, setting the DISCHG bit to 1 can make VOUT discharge by internal resistor when the converter shuts down. If the DISCHG bit is set to 0, VOUT will decrease depending on the loading. When EN pin is set to low, the RT5721 turns on 11Ω discharge resistor by default.

Slew Rate Setting

The RT5721 can control slew rate as VOUT changes between two voltage levels for both up and down.

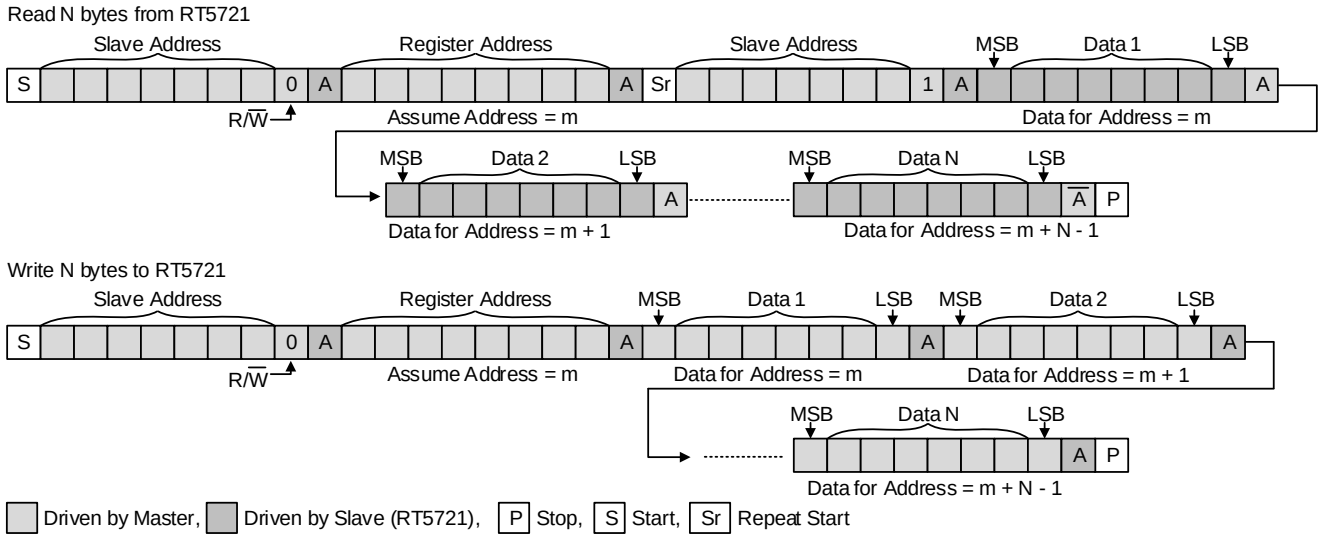
The UP_SR bits in the CONTROL1 register control up-speed, whereas the DN_SR bits in the CONTROL2 register control down-speed. The default DVS up slew rate is 12mV/μs and DVS down slew rate is 3mV/μs.

Forced PWM Mode

The MODE_VSEL0 and MODE_VSEL1 bits in CONTROL1 register can determine the operation mode of the converter. Set 1 for Forced PWM operation and set 0 for auto PSM/PWM operation. Note that, MODE_VSEL0 is activated only when pulling VSEL pin to low, and only set VSEL pin to high for VSEL1 so that the setting of MODE_VSEL1 can be activated.

During dynamic voltage scaling from high setting of output voltage to low setting, the RT5721 makes transient in Forced PWM mode, and output voltage will decrease quickly.

The RT5721 all series IC are able to support fast mode I^{2}C interface (bit rate 400kb/s). For example, the RT5721A default I^{2}C slave address is 7'b1010000. The write or read bit stream (N ≥1) is shown below:



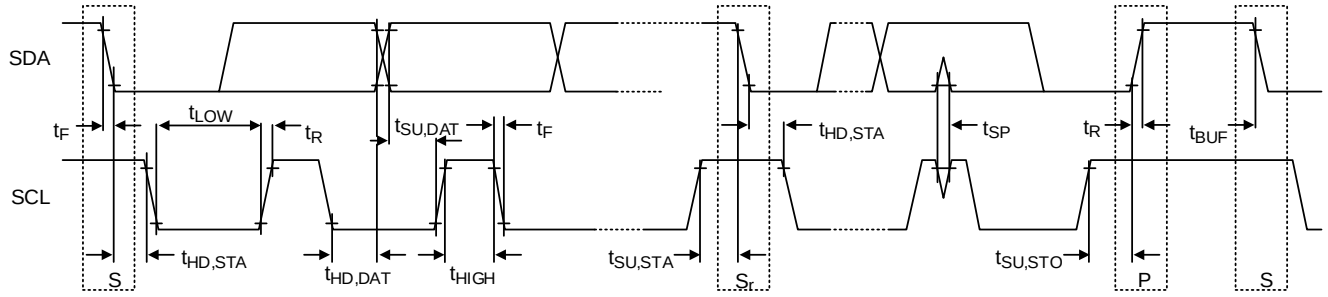


Figure 2. I^{2}C Read and Write Stream and Timing Diagram

The RT5721 also supports High-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 3 and Figure 4 show detailed transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

- START condition (S)
- 8-bit master code (00001xxx)
- not-acknowledge bit ($\overline{A}$)

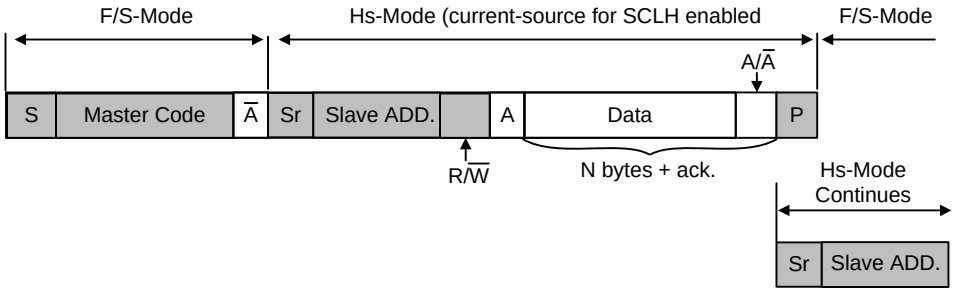


Figure 3. Data Transfer Format in Hs-mode

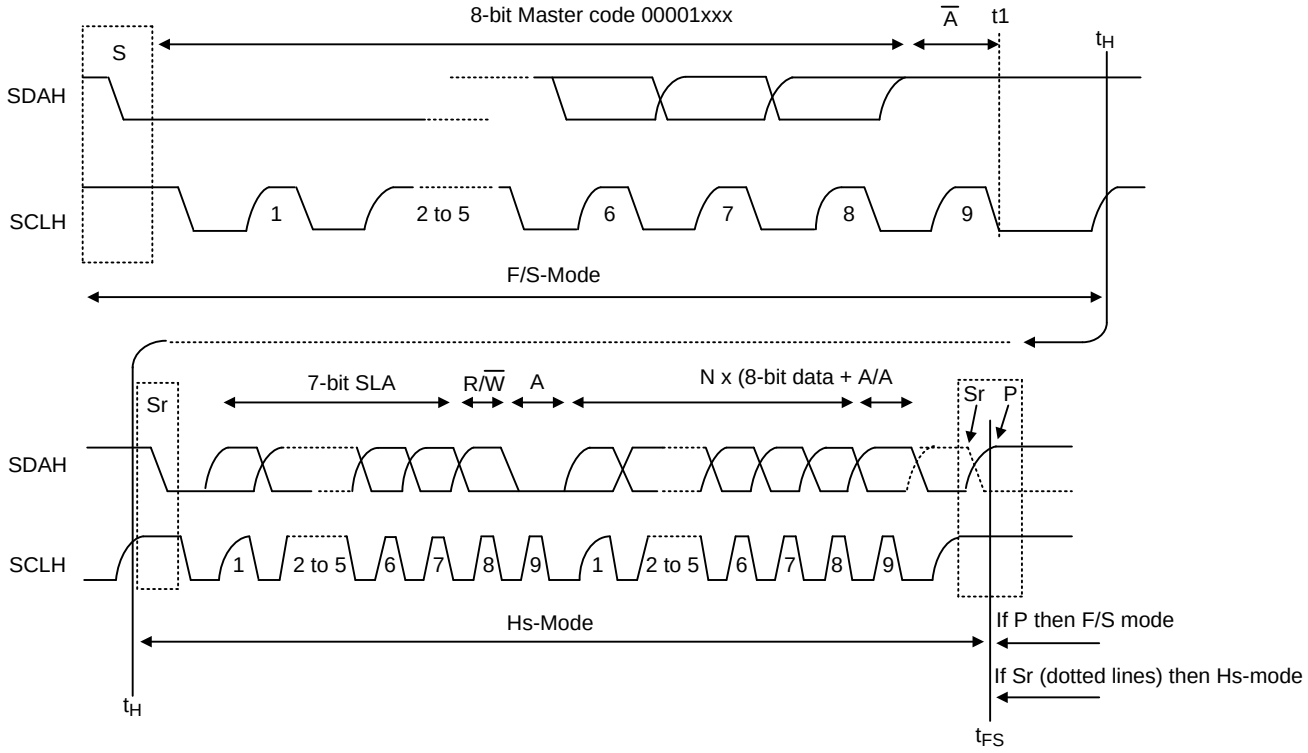


Figure 4. A Complete Hs-mode Transfer

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WL-CSP-11B 1.31x1.62 (BSC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 65.4°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°)/(65.4°C/W) = 1.53W for a WL-CSP-11B 1.31x1.62 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

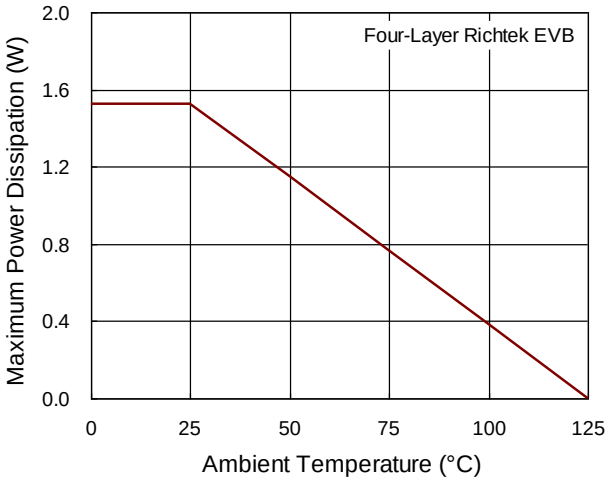


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT5721, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to IC to minimize the power loop area. A typical 0.1μF decoupling capacitor is recommended to reduce power loop area and any high frequency component on VIN.
- SW node is with high frequency voltage swing, so the SW node area should be kept small.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.

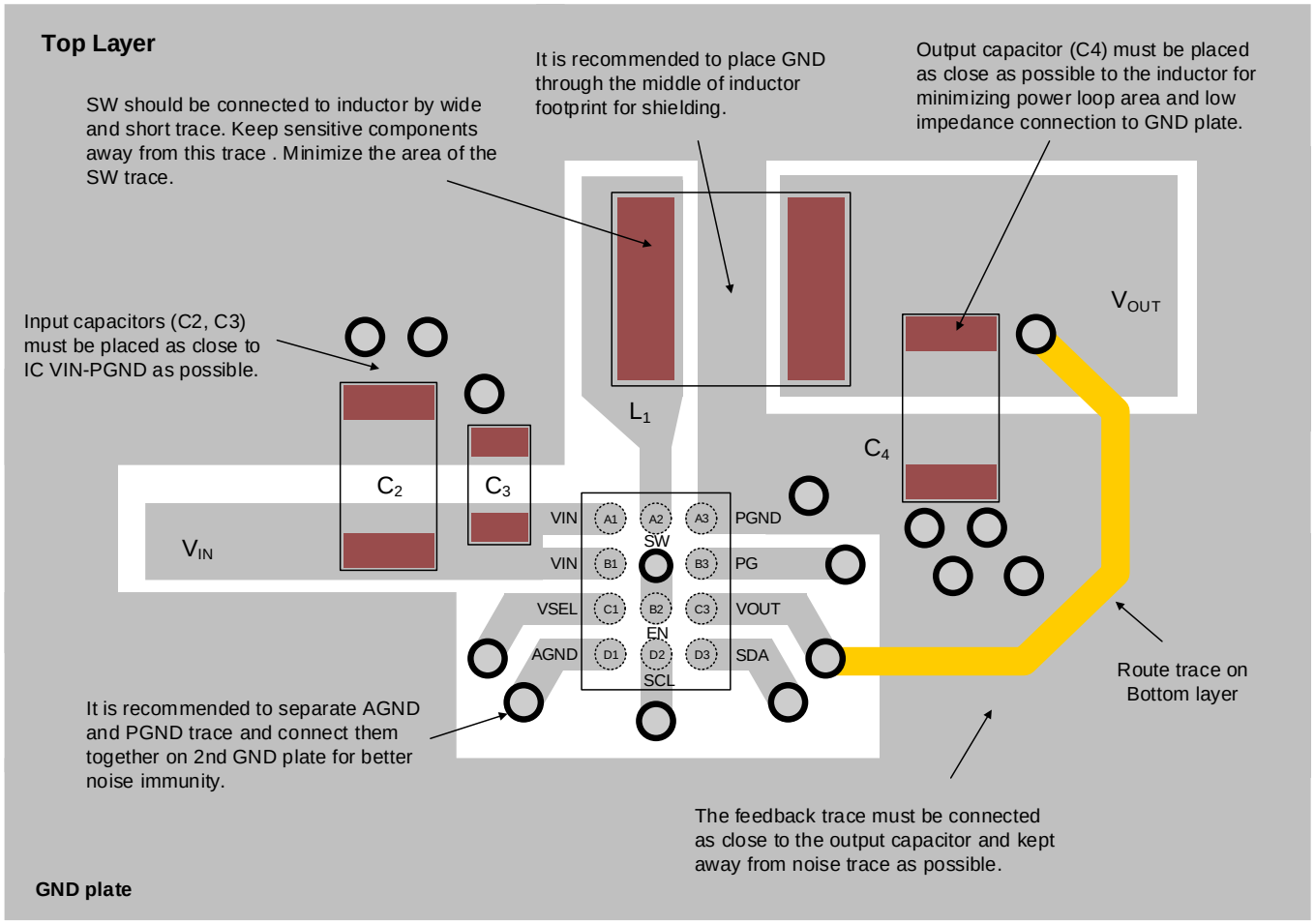


Figure 6. PCB Layout Guide

Functional Register Description

Table 3. Register Map

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x00	NSEL0	VSEL0								0x78	RW
0x01	NSEL1	VSEL1								0x64	RW
0x02	CONTROL1	DISCHG	UP_SR[2:0]			Reserved	SW_RESET	MODE_VSEL1	MODE_VSEL0	0x90	R/W
0x03	ID1	VENDOR_ID			Reserved	DIE_ID				0x00	R
0x04	ID2	Reserved				DIE_REV				0x00	R
0x05	MONITOR	PGOOD	UVLO	Reserved	POS	NEG	RESET_STAT	OT	BUCK_STATUS	0x00	R
0x06	CONTROL2	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_VSEL1	EN_VSEL0	0x63	R/W
0x08	CONTROL4	Reserved		DIS_DLY[5:0]						0x00	R/W

Table 4. VSEL0

Address: 0x00 **Description:** Setting of VSEL0 voltage								
Bit	7	6	5	4	3	2	1	0
Field	VSEL0							
Default (RT5721A)	0	1	1	1	1	0	0	0
Type	R/W							

Bit	Name	Description
7:0	NSEL0	VID Table satisfy : SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 00000000 : 0.3V 5mV step for 0.3V to 1.3V

Table 5. VSEL1

Address: 0x01 **Description:** Setting of VSEL1 voltage								
Bit	7	6	5	4	3	2	1	0
Field	VSEL1							
Default (RT5721A)	0	1	1	0	0	1	0	0
Type	R/W							

Bit	Name	Description
7:0	NSEL1	VID Table satisfy : SEL[7:0] = 1100100 0: V_{OUT} = 1.3V … SEL[7:0] = 00000000 : 0.3V 5mV step for 0.3V to 1.3V

Table 6. CONTROL1

Address: 0x02 **Description:** Control1 setting								
Bit	7	6	5	4	3	2	1	0
Field	DISCHG	UP_SR			Reserved	SW_ RESET	MODE_ VSEL1	MODE_ VSEL0
Default (RT5721A)	1	0	0	1	0	0	0	0
Type	R/W	R/W			R/W		R/W	

Bit	Name	Description
7	DISCHG	0 : Discharge path disabled
		1 : Discharge path enabled
6:4	UP_SR[2:0]	DVS Speed for UP DVS 000 = 24mV step/μs 001 = 12mV step/μs 010 = 6mV step/μs 011 = 3mV step/μs 100 = 1.5mV step/μs 101 = 0.75mV step/μs 110 = 0.375mV step/μs 111 = 0.1875mV step/μs
3	SW_RESET	write 1 to reset, always read 0
2	MODE_VSEL1	0 : Auto
		1 : Continuous mode
1	MODE_VSEL0	0 : Auto
		1 : Continuous mode

Table 7. ID1

Address: 0x03 **Description:** Search Vendor_ID and DIE_ID								
Bit	7	6	5	4	3	2	1	0
Field	VENDOR_ID[2:0]			Reserved	DIE_ID[3:0]			
Default	0	0	0	0	0	0	0	0
Type	R			R	R			

Bit	Name	Description
7:5	VENDOR_ID	Vendor_ID
4	Reserved	Reserved bits
3:0	DIE_ID	DIE_ID

Table 8. ID2

Address: 0x04 **Description:** Search Revision_ID								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				DIE_REV			
Default	0	0	0	0	0	0	0	0
Type	R				R			

Bit	Name	Description
7:4	Reserved	Reserved bits
3:0	DIE_REV	Revision_ID

Table 9. MONITOR

Address: 0x05 **Description:** Monitoring the IC status								
Bit	7	6	5	4	3	2	1	0
Field	PGOOD	UVLO	Reserved	POS	NEG	RESET_ STAT	OT	BUCK_ STATUS
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7	PGOOD	1 : Buck is enabled and soft-start is completed.
6	UVLO	1 : Signifies the V_{IN} is less than the UVLO threshold.
5	Reserved	Reserved bits
4	POS	1 : Signifies a positive voltage transition is in progress
3	NEG	1 : Signifies a negative voltage transition is in progress
2	RESET_STAT	1 : Indicates that a register reset was performed.
1	OT	1 : Signifies the thermal shutdown is active.
0	BUCK_STATUS	1 : Buck enabled; 0 : buck disabled.

Table 10. CONTROL2

Address: 0x06 **Description:** Control2 setting								
Bit	7	6	5	4	3	2	1	0
Field	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_ VSEL0
Default	0	1	1	0	0	0	1	1
Type	R/W			R	R/W		R/W	R/W

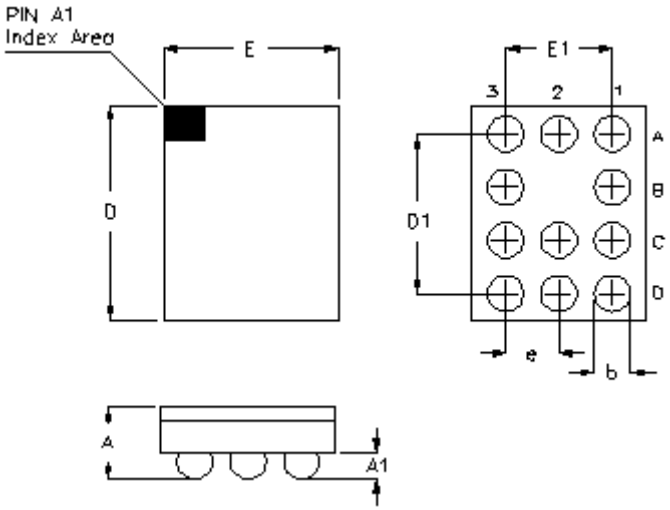
Bit	Name	Description
7:5	DN_SR[2:0]	DVS speed for DN DVS 000 = 24mV step/μs 001 = 12mV step/μs 010 = 6mV step/μs 011 = 3mV step/μs 100 = 1.5mV step/μs 101 = 0.75mV step/μs 110 = 0.375mV step/μs 111 = 0.1875mV step/μs
4	Reserved	Reserved bits
3:2	SS_SR[1:0]	DVS speed for soft-start DVS 00 = 10mV step/μs 01 = 5mV step/μs 10 = 2.5mV step/μs 11 = 1.25mV step/μs
1	EN_VSEL1	0 : Disable 1 : Enable
0	EN_VSEL0	0 : Disable 1 : Enable

Table 11. CONTROL4

Address: 0x08 **Description:** Control4 setting								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		DIS_DLY[5:0]					
Default	0	0	0	0	0	0	0	0
Type	R		R/W					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	DIS_DLY	Delay applied upon disable (ms) 000000b = 0ms – 111111b = 63ms (steps of 1ms)

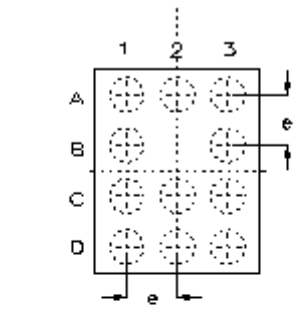
Outline Dimension

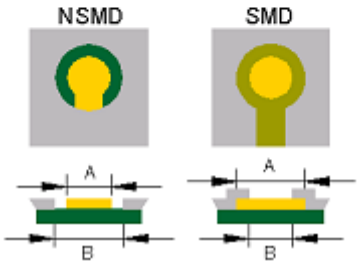


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min.	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.580	1.660	0.062	0.065
D1	1.200		0.047	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

11B WL-CSP 1.31x1.62 Package (BSC)

Footprint Information

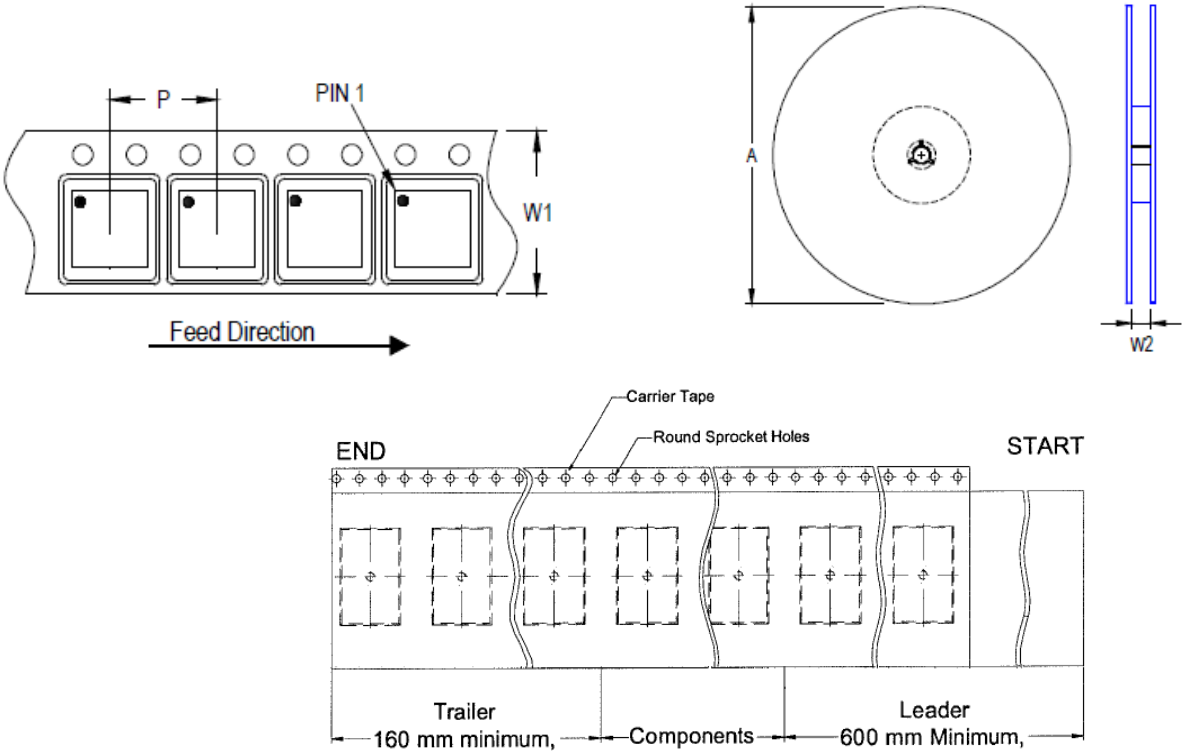




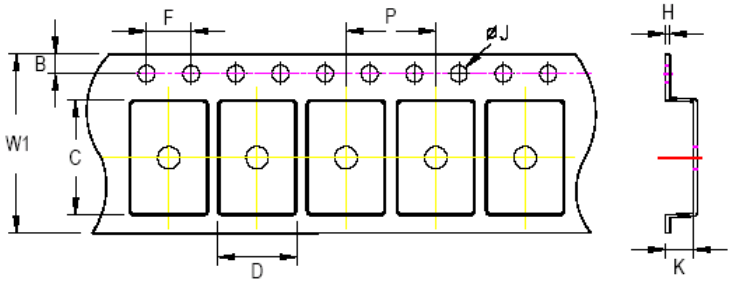
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31x1.62-11(BSC)	11	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.31x1.62	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 1.31x1.62	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/11/22	Final	