2.4MHz 3.5A Step-Down Converter with I²C Interface

General Description

The RT5733 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface and is capable of operating up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the RT5733 is capable of delivering continuous 3.5A, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the external component counts. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in power-save mode with a typical quiescent current of 45μA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed frequency control, operating at 2.4MHz. In shutdown mode, the supply current is typically 0.1μA, and is excellent in reducing power consumption. The PFM mode can be disabled if the fixed frequency is desired. The RT5733 is available in both WQFN-20L 3.5x3.5 and WL-CSP-15B 1.31x2.02 (BSC) package.

Features

- **Programmable Output Voltage Range**
  - **0.27V to 1.4V, 6.25mV/bit**
- **Programmable Slew Rate for Voltage Transitions**
- **Steady 2.4MHz Switching Frequency**
- **Fast Load Transient**
- **Continuous Output Current Capability: 3.5A**
- **2.5V to 5.5V Input Voltage Range**
- **Digitally Programmable Output Voltage**
- **I²C-Compatible Interface Up to 3.4Mbps**
- **PFM Mode for High Efficiency at Light Load**
- **Quiescent Current in PFM Mode: 45μA (Typical)**
- **Input Undervoltage Lockout (UVLO)**
- **Thermal Shutdown and Overload Protection**
- **Power Good Indicator**

Applications

- Application, Graphic, and DSP Processors
- ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, etc.
- Hard Disk Drives, LPDDR3, LPDDR4, LPDDR5
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Phones
- Gaming Devices

Ordering Information

Part No.	Power-Up Defaults		EN Delay Time	Slave Address	Package Type	Lead Plating System
	VSEL0	VSEL1				
RT5733AGQW	0.5V	0.9V	0ms	0x50	WQFN-20L 3.5x3.5	G: Green (Halogen Free and Pb Free)
RT5733AWSC	0.5V	0.9V	0ms	0x50	WL-CSP-15B 1.31x 2.02	--

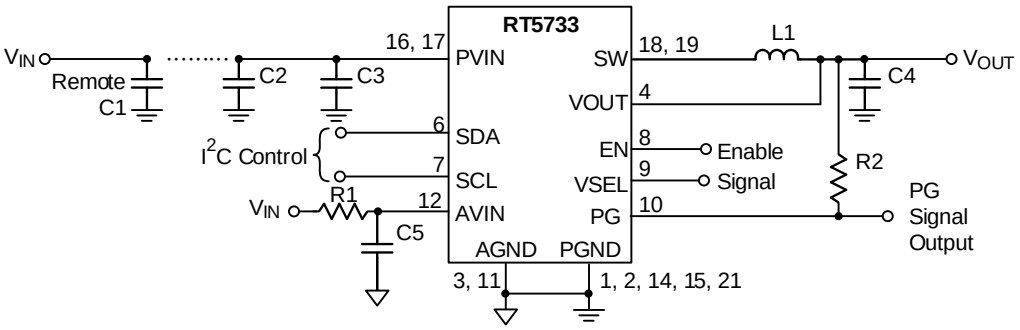
Note:

Richtek products are:

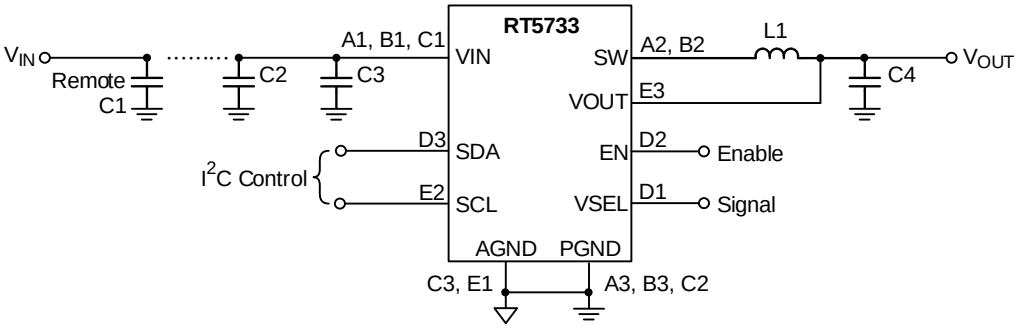
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit

For WQFN-20L 3.5x3.5 package

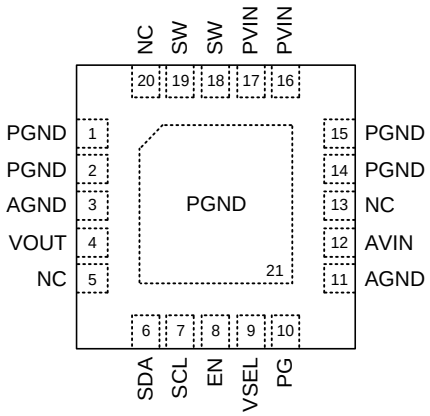


For WL-CSP-15B 1.31x2.02 (BSC) package

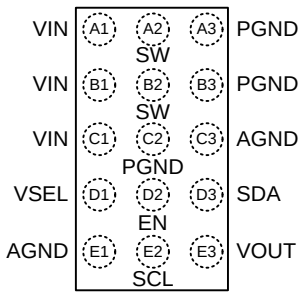


Pin Configuration

(TOP VIEW)



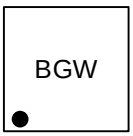
WQFN-20L 3.5x3.5



WL-CSP-15B 1.31x 2.02 (BSC)

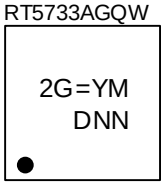
Marking Information

RT5733AWSC



BG : Product Code
W : Date Code

RT5733AGQW



2G= : Product Code
YMDNN : Date Code

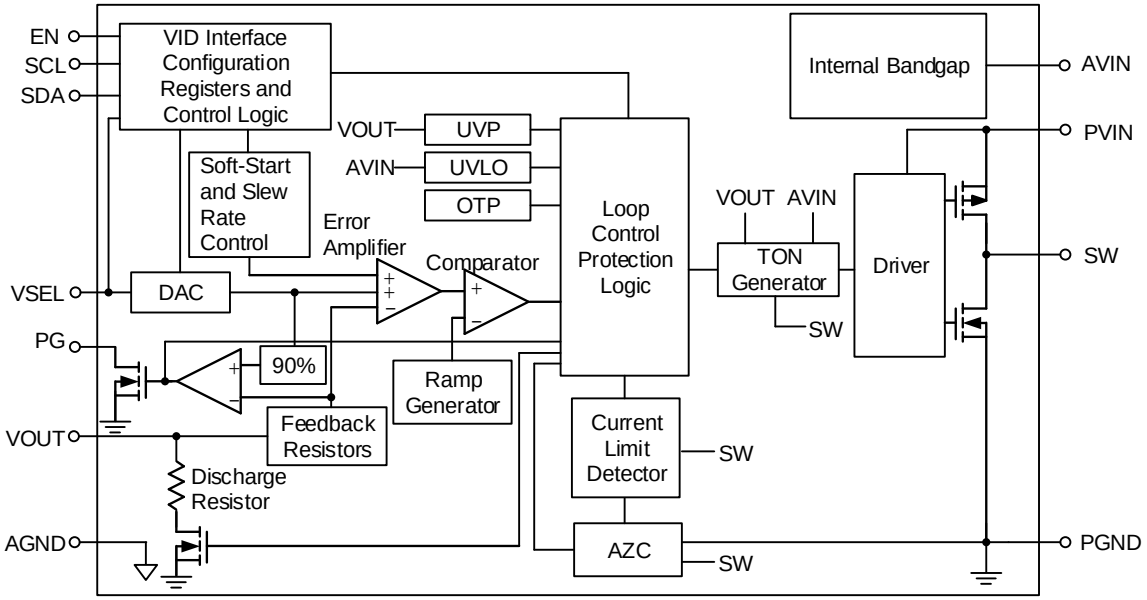
Functional Pin Description

Pin No.		Pin Name	Pin Function
WQFN-20L 3.5x3.5	WL-CSP-15B 1.31x 2.02 (BSC)		
1, 2, 14, 15, 21 (Exposed Pad)	A3, B3, C2	PGND	Power ground. The low-side MOSFET is referenced to this pin. The CIN and COUT should be returned with a minimal path to these pins. The exposed pad is internally connected with PGND and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.
3, 11	C3, E1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
4	E3	VOUT	Output feedback sense pin. Output voltage sense through this pin. Connect to output capacitor.
5, 13, 20	--	NC	No internal connection.
6	D3	SDA	I^2C serial data.
7	E2	SCL	I^2C serial clock.
8	D2	EN	Enable control input. A logic-high enables the converter. A logic-low forces the device into shutdown mode, and all registers will reset to default values.
9	D1	VSEL	Output voltage and operation mode selection pin. When this pin is low, VOUT is set by the VSEL0 register. When this pin is high, VOUT is set by the VSEL1 register. Except the output voltage setting, operation mode can also be configured and selected by the VSEL pin; for example, when 0x02 Bit1 & Bit0 are equal to 0, then VSEL0 = Auto PFM/PWM mode, and VSEL1 = Auto PFM/PWM mode. Please refer to the I^2C register map for more details.
10	--	PG	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. After soft-startup, PG is pulled up when the FB voltage is within 90% (typ.). The PG status is low while EN is disabled. Note that when VIN is lower than 2.32V (typ.), the PG pin will keep low to indicate the power is not ready.

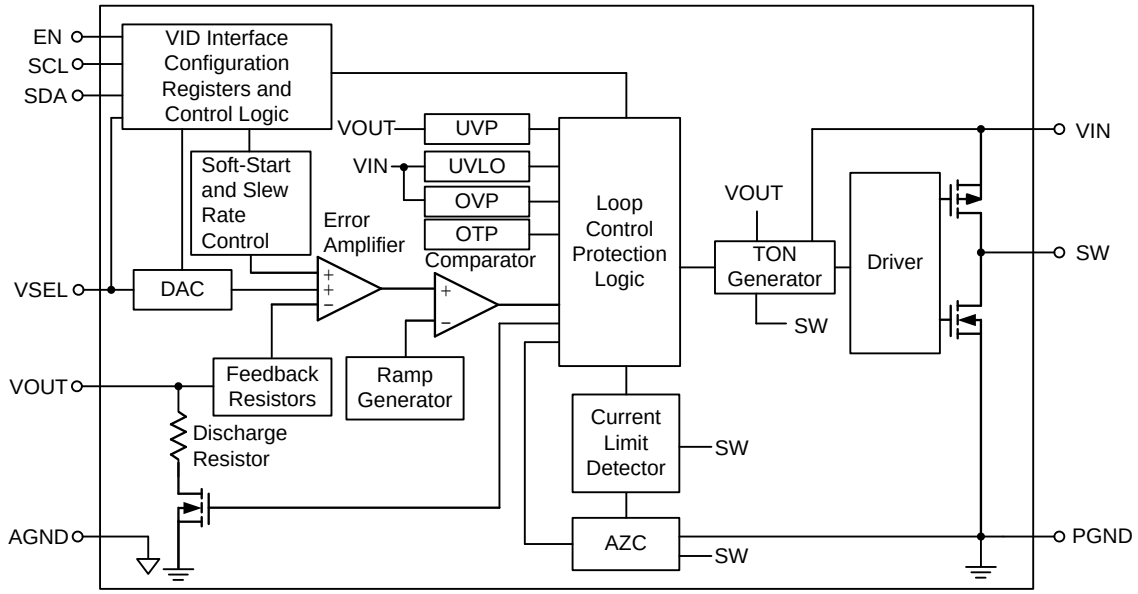
Pin No.		Pin Name	Pin Function
WQFN-20L 3.5x3.5	WL-CSP-15B 1.31x 2.02 (BSC)		
12	--	AVIN	Power supply input for internal circuit. Decouple with a 2.2μF, X5R ceramic capacitor from AVIN to AGND for normal operation.
16, 17	A1, B1, C1	PVIN	Power input voltage. Connect to the input power source. Connect to CIN with minimal path.
18, 19	A2, B2	SW	Switching node. Connect to the inductor.

Functional Block Diagram

For WQFN-20L 3.5x3.5 package



For WL-CSP-15B 1.31x 2.02 (BSC) package



Operation

The RT5733 is a low voltage synchronous step-down converter that can support input voltage ranging from 2.5V to 5.5V, and the output current can be up to 3.5A. The RT5733 uses ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is cleared and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off, the synchronous rectifier is turned on, and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching times and allows the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominal 2.4MHz.

Undervoltage Protection (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VCC is high enough to reach the high threshold voltage of UVLO, the step-down converter softly starts or pre-biases to its regulated output voltage. When the VIN decreases to its low threshold (350mV hysteresis), the device will shut down.

Power GOOD (Register, 0x05 bit7)

When the output voltage is higher than PGOOD rising threshold (90% of its setting voltage), the PGOOD flag is high.

Power Good Indication Pin (only parts with PG pin)

The RT5733 features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull up PG with a resistor to V_{OUT} or an external voltage below 5.5V. When VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft-start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{OUT}. If V_{OUT} rises above a power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. Moreover, when V_{IN} is above UVLO and device is powered on through the EN pin, the PG pin will assert high within 300μs as soon as the V_{EN} is above logic-high threshold; in other words, the PG delay time is around 300μs from EN asserts to logic-high.

When V_{OUT} falls below the power-good low threshold (V_{TH_PGHL}) (typically 80% of the reference voltage), the PG pin will be pulled low after a certain delay (3μs, typically). Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device (11Ω, typically) will pull the PG pin low. Note that when Vin is lower than 2.32V, the PG pin will keep low to indicate the power is not ready.

Output Undervoltage Protection (UVP) and Overcurrent Protection (OCP)

When the output voltage of the RT5733 is lower than 59% of the reference voltage after soft-start, the UVP is triggered.

The RT5733 senses the current signal when high-side and low-side MOSFETs turn on. As a result, the OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next pulse and turns on low-side switch

until inductor drops below the valley current limit, and then turns on high-side again to maintain output voltage and supports loading current to output before triggering UVP.

If the OCP condition keeps and the load current is larger than the current that the converter can provide, the output voltage will decrease and drop below UVP threshold, and the converter will keep switching for 16 consecutive cycles before it enters hiccup operation. The converter latches off 1.7ms when the output voltage is still lower than UVP threshold, and the soft-start sequence begins again after latching off time.

Note that, there is sensing propagation delay time before triggering OCP; hence, the OCP may take a few cycles to occur when the inductor current is near OCP threshold. If the output voltage drops slowly before entering hiccup operation, the converter will extend the high-side switch on-time and turns on low-side switch for only minimum off-time to provide large load current and catch up with the output voltage before detecting peak current limit OCP.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time can be programmed by I^2C.

Over-Temperature Protection (OTP)

The RT5733 has over-temperature protection. When the device triggers the OTP, the device shuts down immediately, and will soft-start again when the junction temperature is below the recovery threshold.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVIN, AVIN ---------- 0.3V to 7V
- SW Pin Switch Voltage, SW ---------- –1V to 7.3V
  <50ns ---------- –5V to 8.5V
- Other I/O Pin Voltages ---------- –0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings

- ESD Susceptibility (Note 2)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, PVIN ---------- 2.5V to 5.5V
- Supply Input Voltage, AVIN ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WQFN-20L 3.5x3.5	WL-CSP-15B 1.31x2.02	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	28.6	42	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	55.6	0.2	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.3	9.5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	43.2	49.9	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	5.4	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.8	27.7	°C/W

Electrical Characteristics

(V_{IN} = V_{AVIN} = V_{PVIN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Quiescent Current PWM		I_{Q_PWM}	I_{LOAD} = 0, mode Bit = 1 (Forced PWM) (Note 6)	--	15	--	mA
Operating Quiescent Current PFM		I_{Q_PFM}	I_{LOAD} = 0A	--	45	--	μA
Operating Low Power Mode Quiescent Current PFM		$I_{Q\_PFM\_LPM}$	I_{LOAD} = 0A and Enable LPM	--	36	--	μA
H/W Shutdown Supply Current		$I_{SHDN\_H/W}$	EN = GND	--	0.1	3	μA
S/W Shutdown Supply Current		$I_{SHDN\_S/W}$	EN = V_{IN}, BUCK_ENx = 0, 2.5V ≤ V_{IN} ≤ 5.5V	--	2	12	μA
Undervoltage Lockout Threshold		V_{UVLO}	VIN rising	--	2.32	2.45	V
Undervoltage Lockout Hysteresis		ΔV_{UVLO}		--	350	--	mV
$R_{DS(ON)}$ of P-MOSFET		$R_{DS(ON)\_P}$	V_{IN} = 5V	--	30	--	mΩ
$R_{DS(ON)}$ of N-MOSFET		$R_{DS(ON)\_L}$	V_{IN} = 5V	--	17	--	mΩ
Input Voltage	Logic-High	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V	1.1	--	--	V
	Logic-Low	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V	--	--	0.4	
EN Input Bias Current		I_{EN}	EN input tied to GND or V_{IN}	--	0.01	1	μA
V_{OUT} DC Accuracy			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Auto PFM/PWM (Note 6)	--	--	3	%
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Auto PFM/PWM (Note 6)	–18	--	18	mV
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Forced PWM (Note 6)	–2	--	2	%
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Forced PWM (Note 6)	–12	--	12	mV
Load Regulation		ΔV_{LOAD}	$I_{OUT(DC)}$ = 1 to 3A (Note 6)	--	0.1	--	%/A
Line Regulation		ΔV_{LINE}	2.5V ≤ V_{IN} ≤ 5.5V, $I_{OUT(DC)}$ = 1.5A (Note 6)	--	0.2	--	%/V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transient Load Response	AC_{LOAD}	I_{LOAD} step 0.01A to 1.5A, $t_R = t_F$ = 500ns, V_{OUT} = 1.125V (Note 6)	--	±45	--	mV
		I_{LOAD} step 0.1A to 1.8A, $t_R = t_F$ = 1μs, V_{IN} = 3.8V, V_{OUT} = 0.9V (Note 6)	--	±56	--	
		I_{LOAD} step 0.01A to 0.8A, $t_R = t_F$ = 1μs, L = 0.33μH, C_{OUT} = 22μF x 2 (Note 6)	--	45	--	
Line Transient	V_{LINE}	V_{IN} = 3V to 3.6V, $t_R = t_F$ = 10μs, I_{OUT} = 100mA, Forced PWM mode (Note 6)	--	±40	--	mV
P-MOSFET Peak Current Limit	I_{LIM_P}		5	5.5	6	A
Valley Current Limit			3.5	4	4.5	A
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	°C
Input OVP Shutdown	V_{SDHD_OVPrth}	Rising threshold	--	6.15	--	V
Input OVP Shutdown	V_{SDHD_OVPfth}	Falling threshold	5.5	5.73	--	V
Switching Frequency	f_{SW}	V_{OUT} = Default RT5733AGQW: 0.5V RT5733AWSC: 0.5V	2100	2400	2700	kHz
Minimum Off-Time	t_{OFF_MIN}		--	170	--	ns
DAC Resolution		(Note 6)	--	8	--	bits
DAC Differential Nonlinearity		(Note 6)	--	--	0.5	LSB
I^2C Interface (Note 6)						
SDA, SCL Input Voltage	High Level		1.2	--	--	V
	Low Level		--	--	0.4	
SCL Clock Rate	f_{SCL}	Fast mode	--	--	400	kHz
		Fast plus mode	--	--	1	MHz
		High speed mode, load 100pF max	--	--	3.4	MHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	
		High speed mode	0.16			
Low Period of the SCL Clock	t_{LOW}	Fast mode	1.3	--	--	μs
		Fast plus mode	0.5	--	--	
		High speed mode	0.16			
High Period of the SCL Clock	t_{HIGH}	Fast mode	0.6	--	--	μs
		Fast plus mode	0.26	--	--	
		High speed mode	0.06			

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
		High speed mode	0.01			
Data Hold Time	$t_{HD;DAT}$	Fast mode	0	--	--	µs
		Fast plus mode	0	--	--	
		High speed mode	0	--	--	
Data Set-Up Time	$t_{SU;DAT}$	Fast mode	100	--	--	ns
		Fast plus mode	50	--	--	
		High speed mode	10	--	--	
Set-Up Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	--	--	µs
		Fast plus mode	0.26	--	--	
		High speed mode	0.16	--	--	
Bus Free Time between a STOP and START Condition	t_{BUF}	Fast mode	1.3	--	--	µs
		Fast plus mode	0.5	--	--	
Rising Time of both SDA and SCL Signals	t_R	Fast mode	20	--	300	ns
		Fast plus mode	--	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
Falling Time of both SDA and SCL Signals	t_F	Fast mode	20 x (V_{DD}/5.5V)	--	300	ns
		Fast plus mode	20 x (V_{DD}/5.5V)	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. Guaranteed by design.

Typical Application Circuit

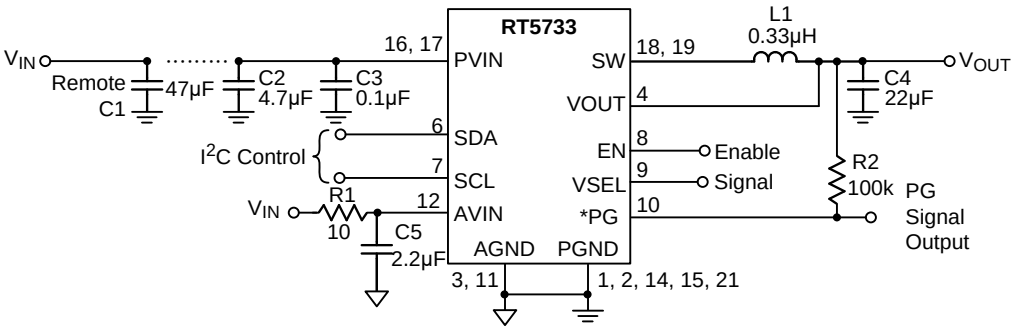


Figure 1. RT5733 WQFN-20L 3.5x3.5 Package Typical Application Circuit

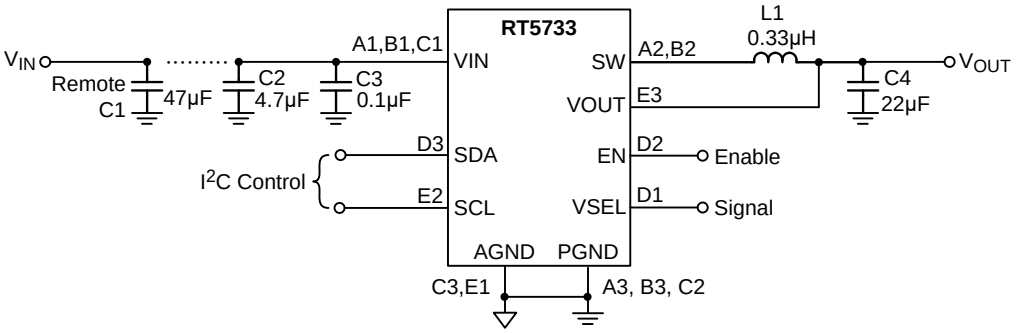


Figure 2. RT5733 WL-CSP-15B 1.31x 2.02 (BSC) Package Typical Application Circuit

Table 1. Recommended External Components for 3.5A Maximum Load Current

Component	Description	Vendor P/N
L1	330nH, case size	DFE201610E-R33M=P2 (Murata)
	470nH, case size	DFE201610E-R47M=P2 (Murata)
C2	4.7µF, 10V, X5R, 0402	GRM155R61A475MEAA (Murata)
C3(1)	100nF, 6.3V, X5R, 0201	GRM033R60J104KE19D (Murata)
C4	22µF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
		C1608X5R0J226M080AC (TDK)

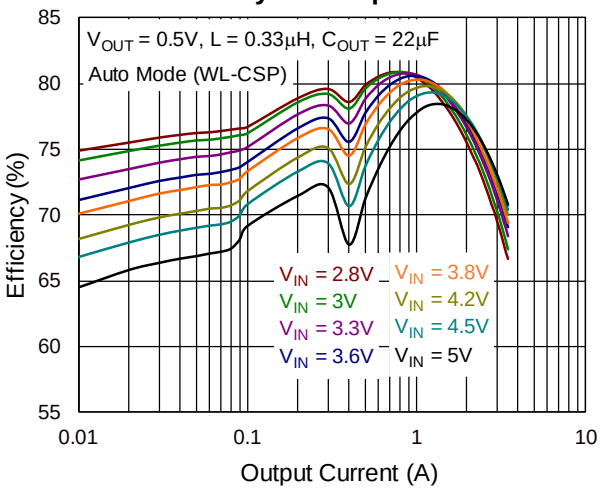
Note:

(1) The decouple capacitor C3 is recommended to reduce any high frequency component on VIN bus. C3 is optional and used to filter any high frequency component on VIN bus.

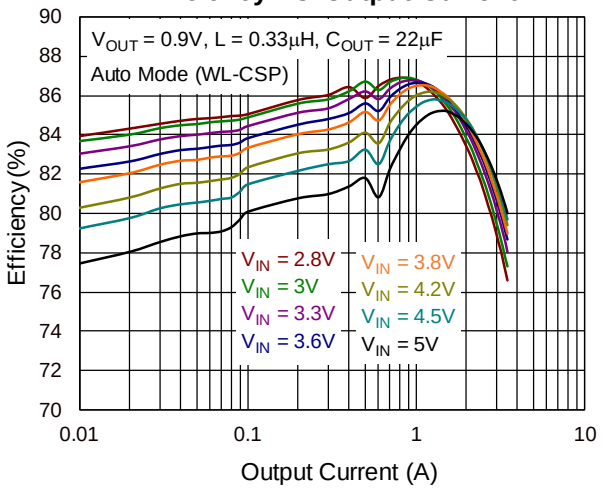
(2) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Typical Operating Characteristics

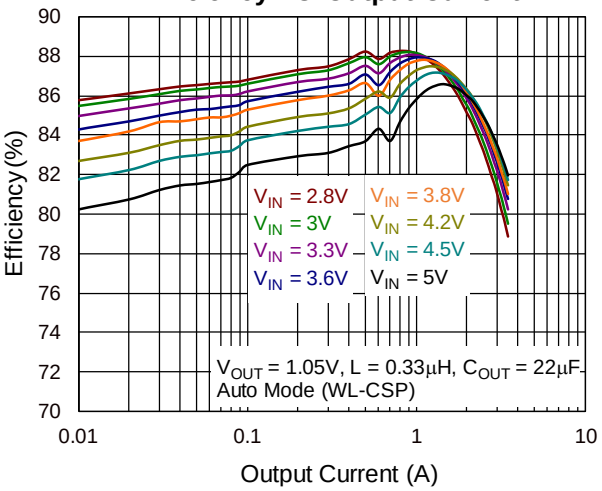
Efficiency vs. Output Current



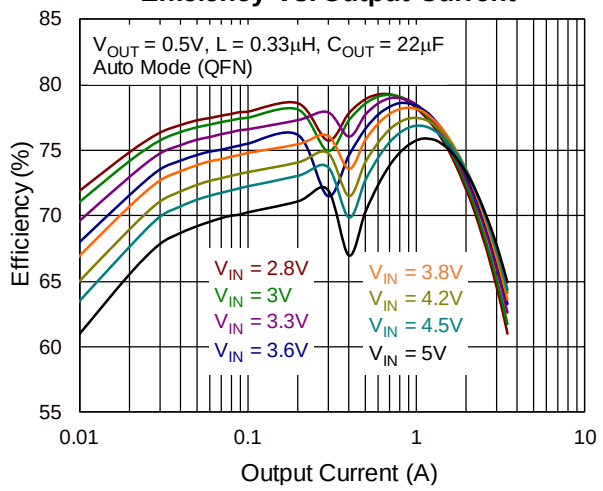
Efficiency vs. Output Current



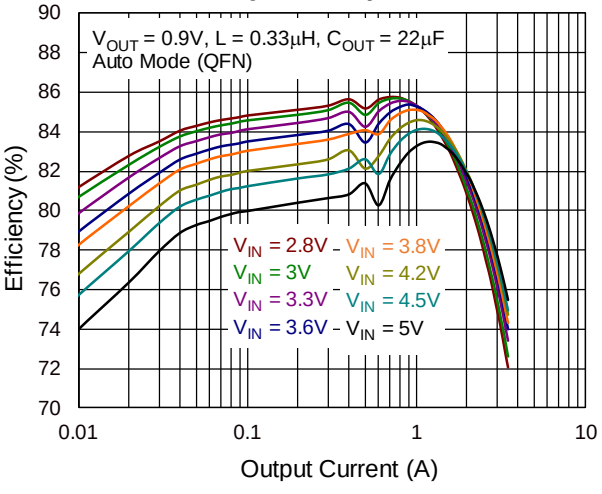
Efficiency vs. Output Current



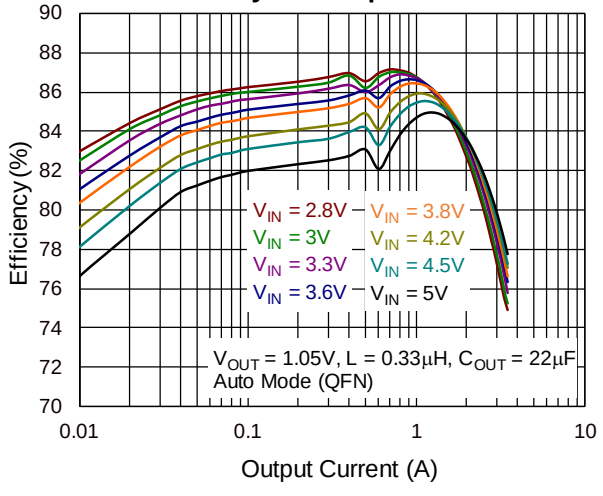
Efficiency vs. Output Current

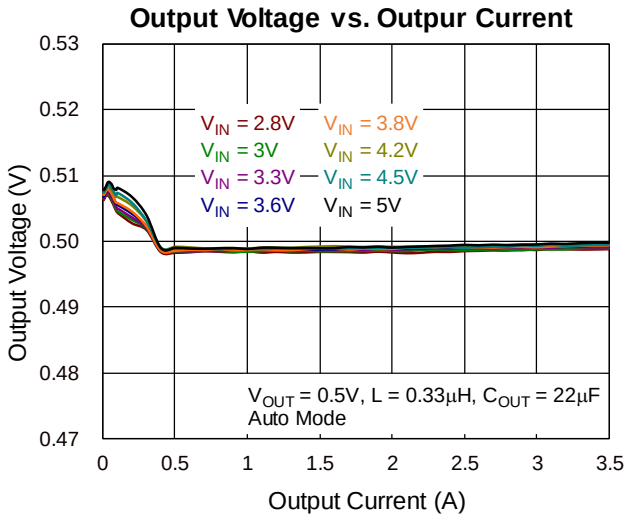


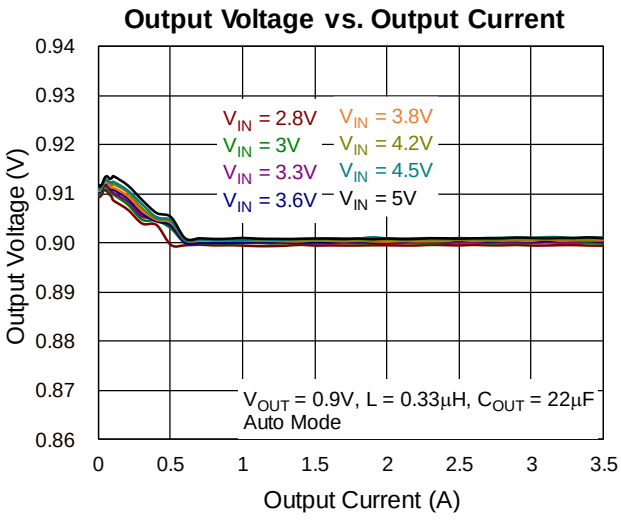
Efficiency vs. Output Current

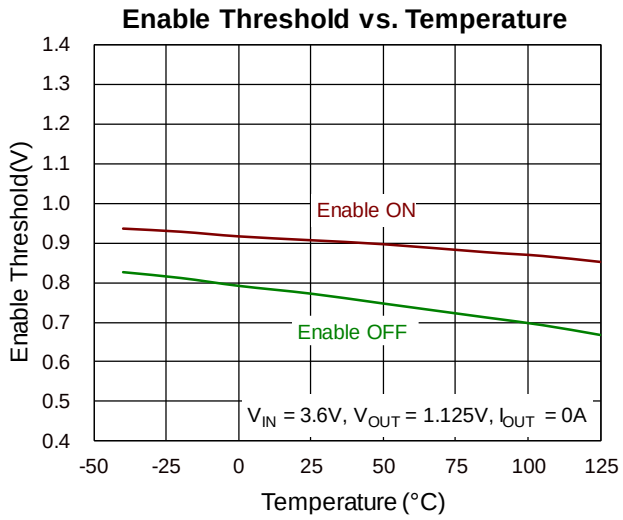


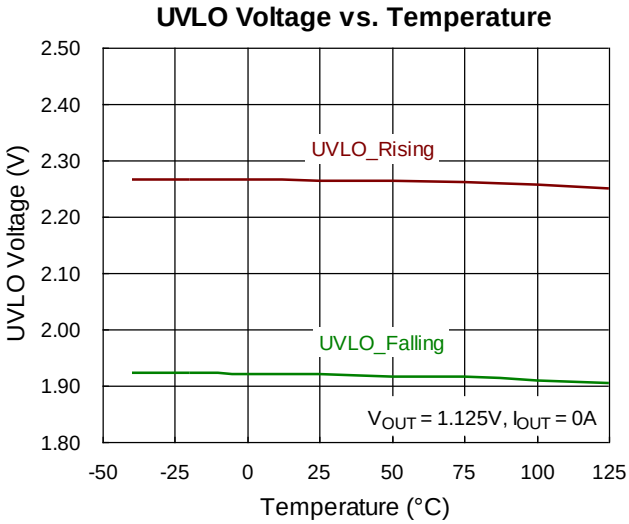
Efficiency vs. Output Current

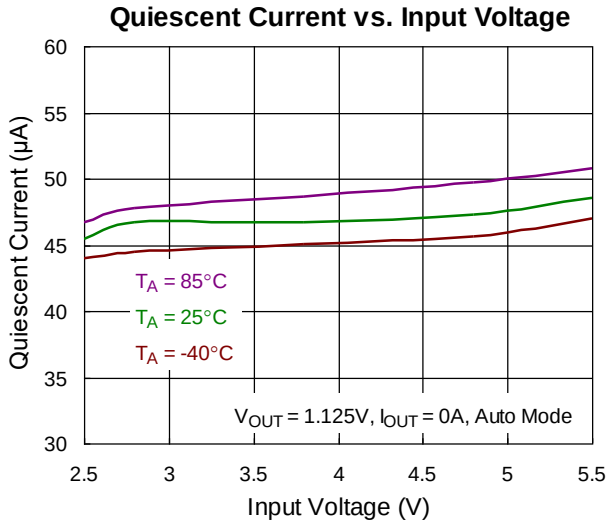


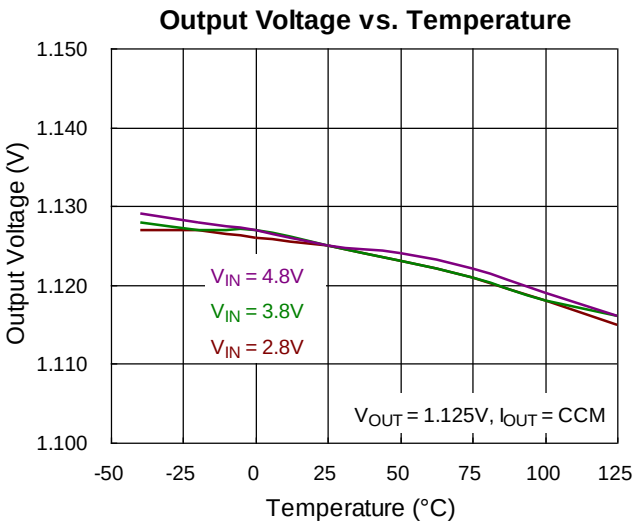




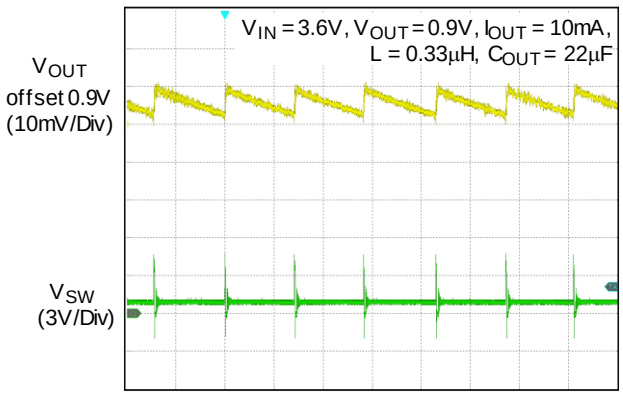






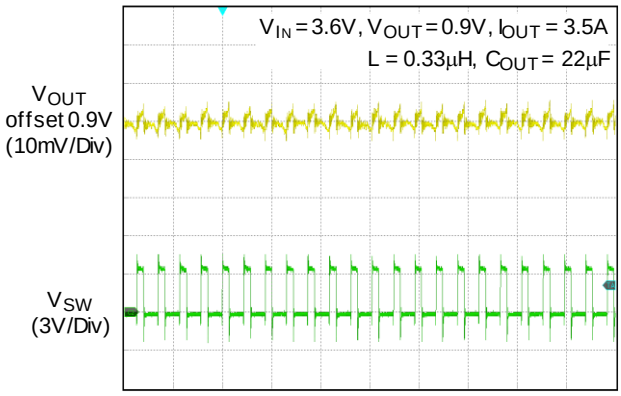


Output Ripple Voltage



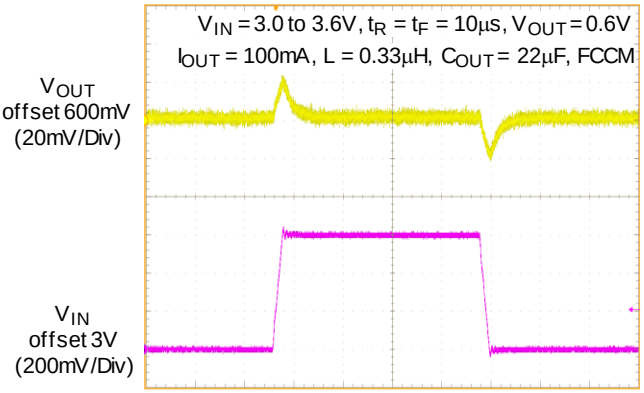
Time (10µs/Div)

Output Ripple Voltage



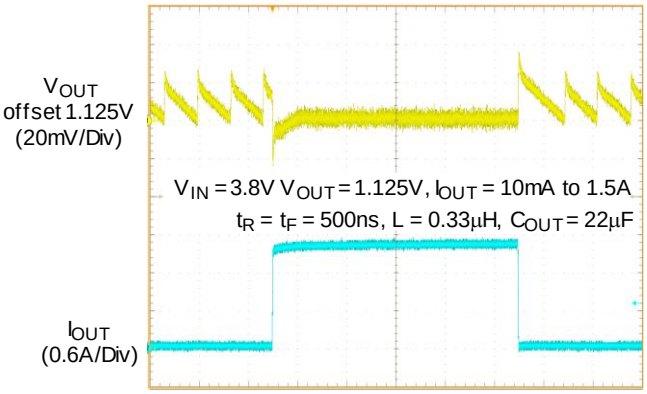
Time (1µs/Div)

Line Transient Response



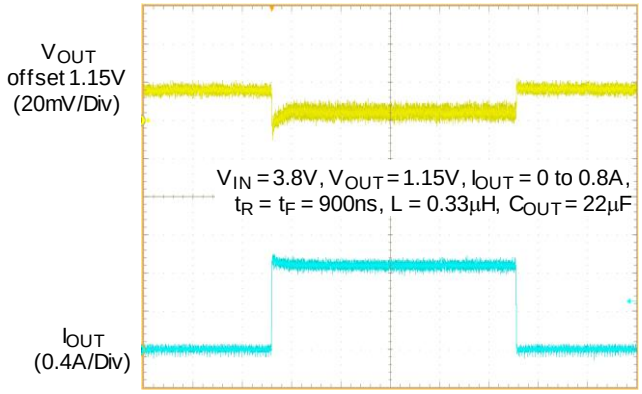
Time (50µs/Div)

Load Transient Response



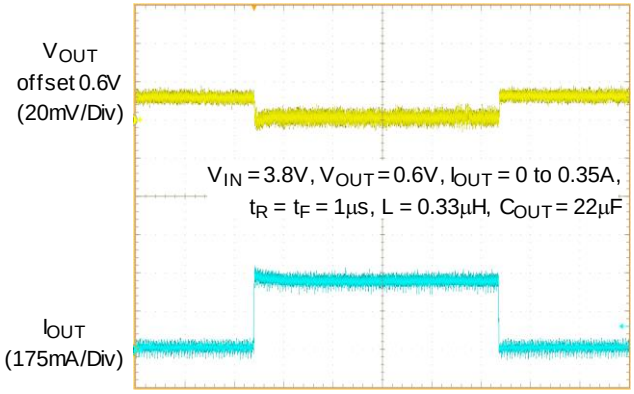
Time (50µs/Div)

Load Transient Response



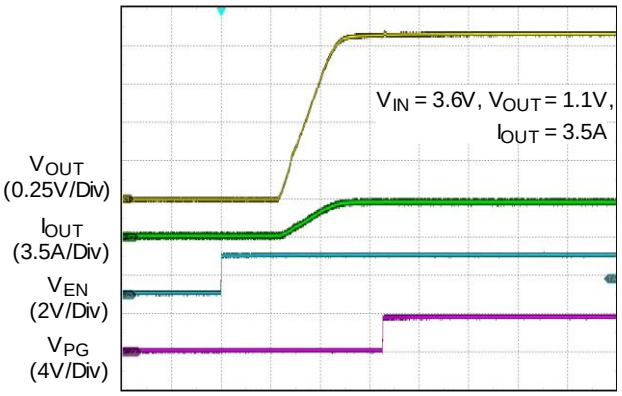
Time (50µs/Div)

Load Transient Response



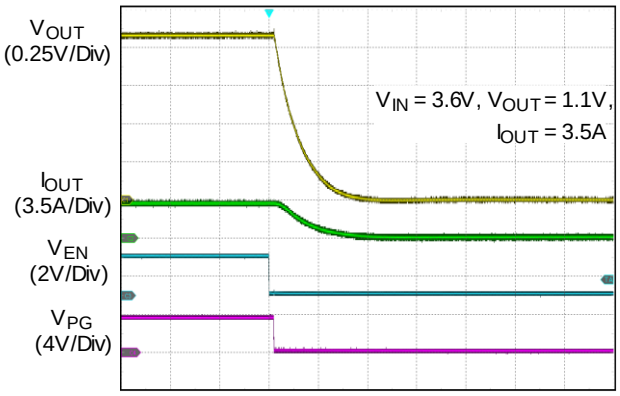
Time (50µs/Div)

Power On from EN



Time (2μs/Div)

Power Off from EN



Time (20μs/Div)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The basic RT5733 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value, operating frequency, and followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in the equation below:

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. Lower ripple current reduces not only ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal.

The largest ripple current occurs at the highest V_{IN}. A reasonable starting point for selecting the ripple current is ΔI_L = 0.3 x I_{MAX} to 0.4 x I_{MAX}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$.

This simple worst-case condition is commonly used for design.

Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications.

However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right]$$

I²C Interface Function

The RT5733 uses the I²C interface to select VOUT voltage level, Dynamic Voltage Scaling (DVS) slew rate, Auto PFM/PSM or FCCM mode, and so on. The register of each function can be found from the following register map and it also explains how to use these functions.

VOUT Selection

The RT5733 all series products have programmable output voltage range from 0.27V to 1.4V with 6.25mV/bit resolution. Note that, the output voltage can be set by the NSELx register bit and the output voltage are given by the following equation and examples:

VOUT = 0.27V + NSELx x 6.25mV

For example:

if NSELx = 0111100 (60 decimal), then

VOUT = 0.27 + 60 x 6.25mV

= 0.27 + 0.375 = 0.645V.

The RT5733 also has external VSEL pin to select NSEL1(0x01) or NSEL0(0x00). Pull VSEL to high is for VSEL1 and pull VSEL to low is for VSEL0. Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

Enable and Soft-Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I²C cannot be written or read until input voltage is above the UVLO. The registers will reset when the EN pin is LOW or during a Power-On Reset (POR).

Once the EN pin is high, VOUT will ramp up at the chosen soft-start slew rate programmed in the CONTROL2 register SS_SR bit.

Raising EN while the EN_VSELx bit is HIGH activates the part and begins the soft-start cycle.

Discharge Function

In the CONTROL1 register, set the DISCHG bit to 1 can make VOUT discharge by internal resistor when the converter shuts down. If the DISCHG bit is set to 0, VOUT will decrease depending on the loading. When the EN pin is set to low, the RT5733 will default turn on internal 11Ω discharge resistor.

Slew Rate Setting

The RT5733 can control slew rate as VOUT changing between two voltage levels for both up and down.

In the CONTROL1 register, DVS_UP bits can control up-speed. In the CONTROL2 register, DVS_DN can control down-speed. The default slew rate of DVS_UP is 12mV/μs and the slew rate of DVS_DN is 3mV/μs.

The details of slew rate setting can be found in the register function description table.

Operation Mode Selection

In the CONTROL1 register, MODE_VSEL0 and MODE_VSEL1 can decide whether the converter is always at FCCM mode or enters power saving mode at light load conditions.

In auto PFM mode, the auto zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to get better efficiency.

The default operation mode of MODE_VSEL0 is auto PFM mode and MODE_VSEL1 can be selected by factory setting.

When output voltage is changing from high to low, the RT5733 will make transition operation at PWM mode and output voltage will decrease quickly.

Low Power Mode Operation

RT5733 features auto PFM/PWM mode to achieve power-saving operation. It generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a skip pulse or a sleep period to cut down current demand from input source to obtain high efficient at light load conditions. The load current is supported by the output capacitor during this sleep period depending on the load current and the inductor peak current.

To minimize the battery energy consumption, the system requests further quiescent current reduction operation such as shipping mode or suspend operation, etc. RT5733 features low power mode (LPM) operation, where several of the internal protection circuits (input

OVP, UVP) are shutdown to achieve lowest 36μA operating quiescent current for ultra-light load condition. LPM operation can be enabled by setting LPM control register (0x0A bit1) to 1 in the CONTROL5 register.

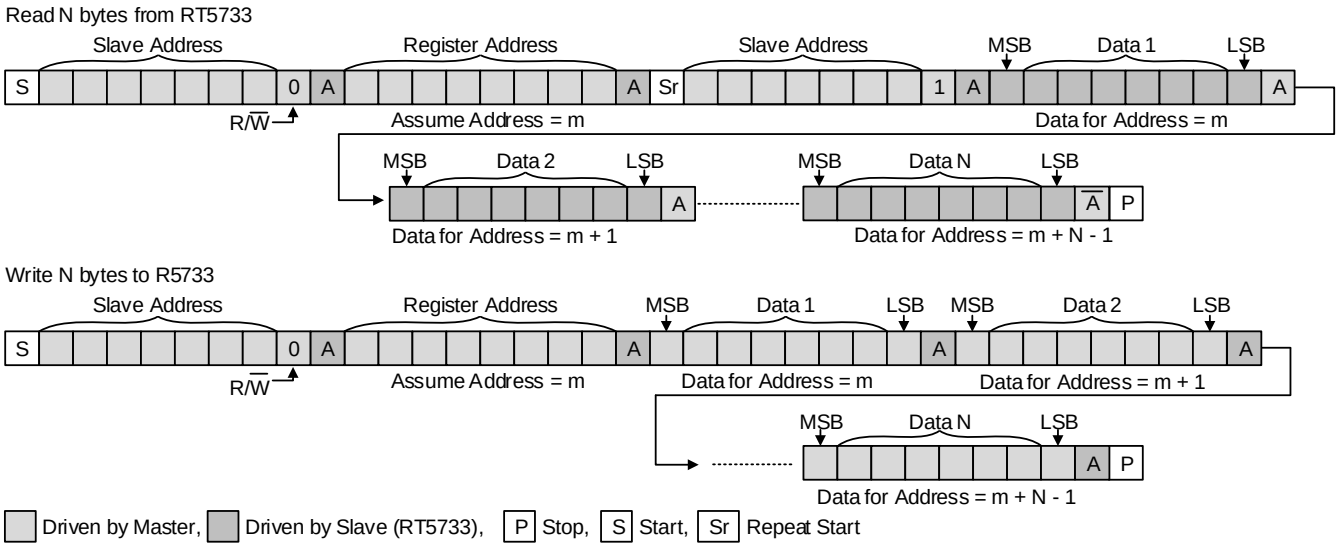
I²C Time Out Function

The RT5733 has built-in I²C time out function to make RT5733 resume listening state during communication bus error situation.

When RT5733 detects whether the SCL pin or SDA pin is pulled down for more than 30ms, RT5733 will reset its I²C interface. The I²C time out function can be enabled or disabled by control register (0x0A bit0). For more detail setting value, please refer to I²C register table.

I²C Interface

The all series of RT5733 are able to support fast mode I²C interface (bit rate 400kb/s), and different parts have their own slave address. For example, the default I²C slave address of the RT5733AGQW is 7'b1010000. The write or read bit stream (N ≥ 1) is shown below:



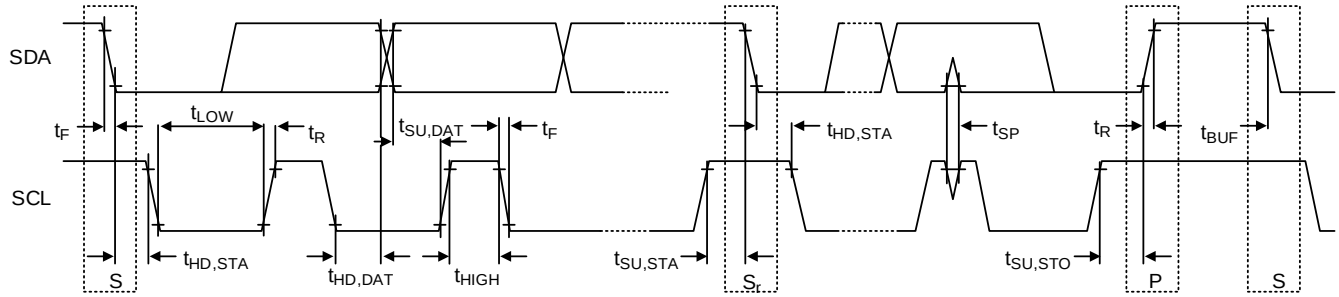


Figure 3. I²C Read and Write Stream and Timing Diagram

The RT5733 also supports High-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 4 and Figure 5 show detailed transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

- START condition (S)
- 8-bit master code (00001xxx)
- Not-acknowledge bit ($\overline{A}$)

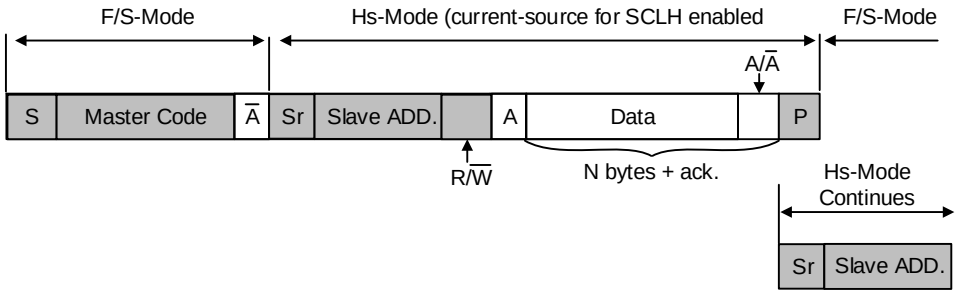


Figure 4. Data Transfer Format in HS-Mode

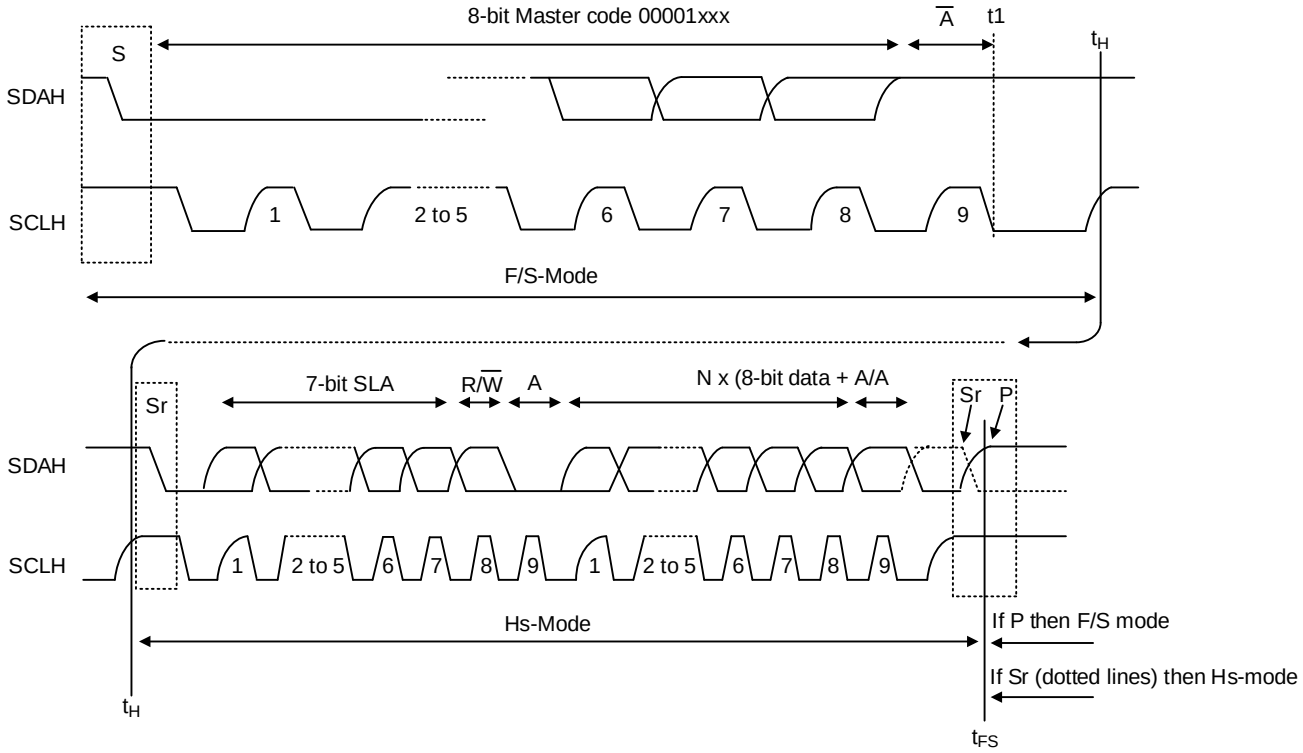


Figure 5. A Complete HS-Mode Transfer

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WQFN-20L 3.5x3.5 package, the thermal resistance, $\theta_{JA(EVB)}$, is 43.2°C/W on a high effective-thermal-conductivity four-layer test board. For a WL-CSP-15B 1.31x2.02 (BSC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 49.9°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation for both package at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(43.2°C/W) = 2.3W for a WQFN-20L 3.5x3.5 package.

$P_{D(MAX)}$ = (125°C – 25°C)/(49.9°C/W) = 2W for a WL-CSP-15B 1.31x2.02 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

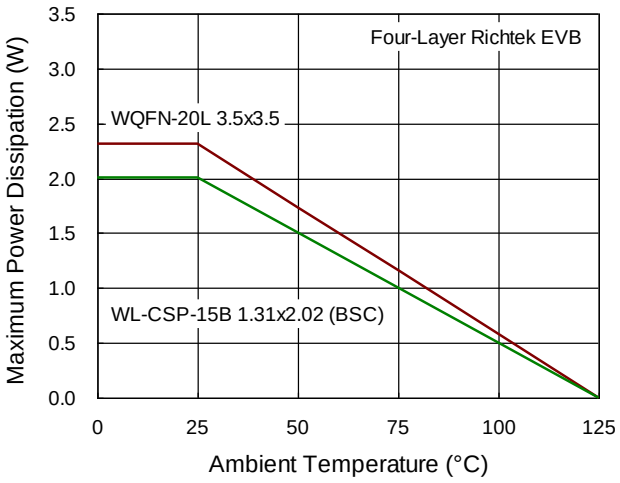


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT5733, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to the IC to minimize the power loop area. A typical 0.1μF decouple capacitor is recommended to reduce power loop area and any high frequency component on PVIN.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.
- For QFN package, please connect RC low pass filter as close as possible to the AVIN pin.
- Keep current protection setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.

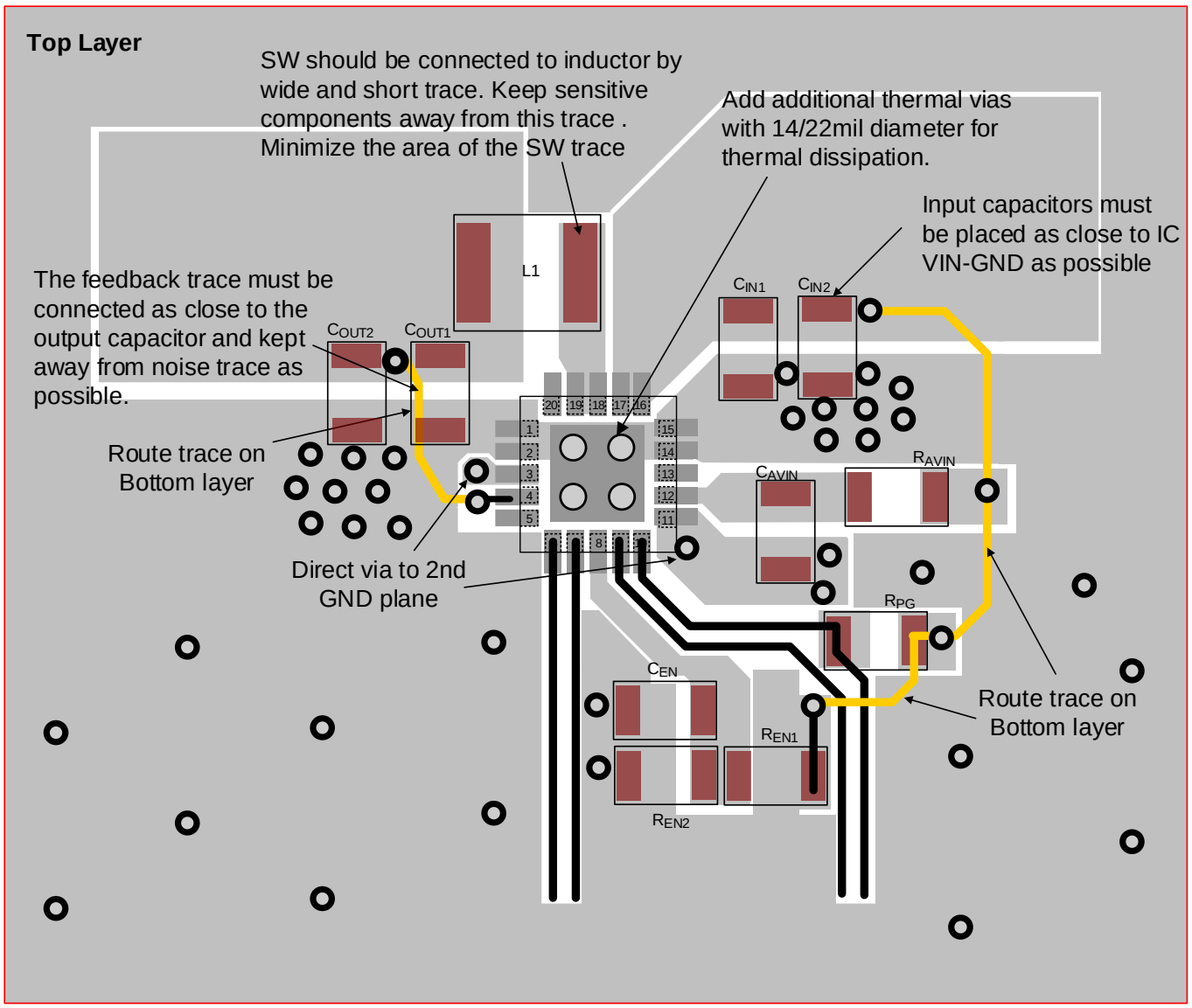


Figure 7. PCB Layout Guide for WQFN-20L 3.5x3.5 package

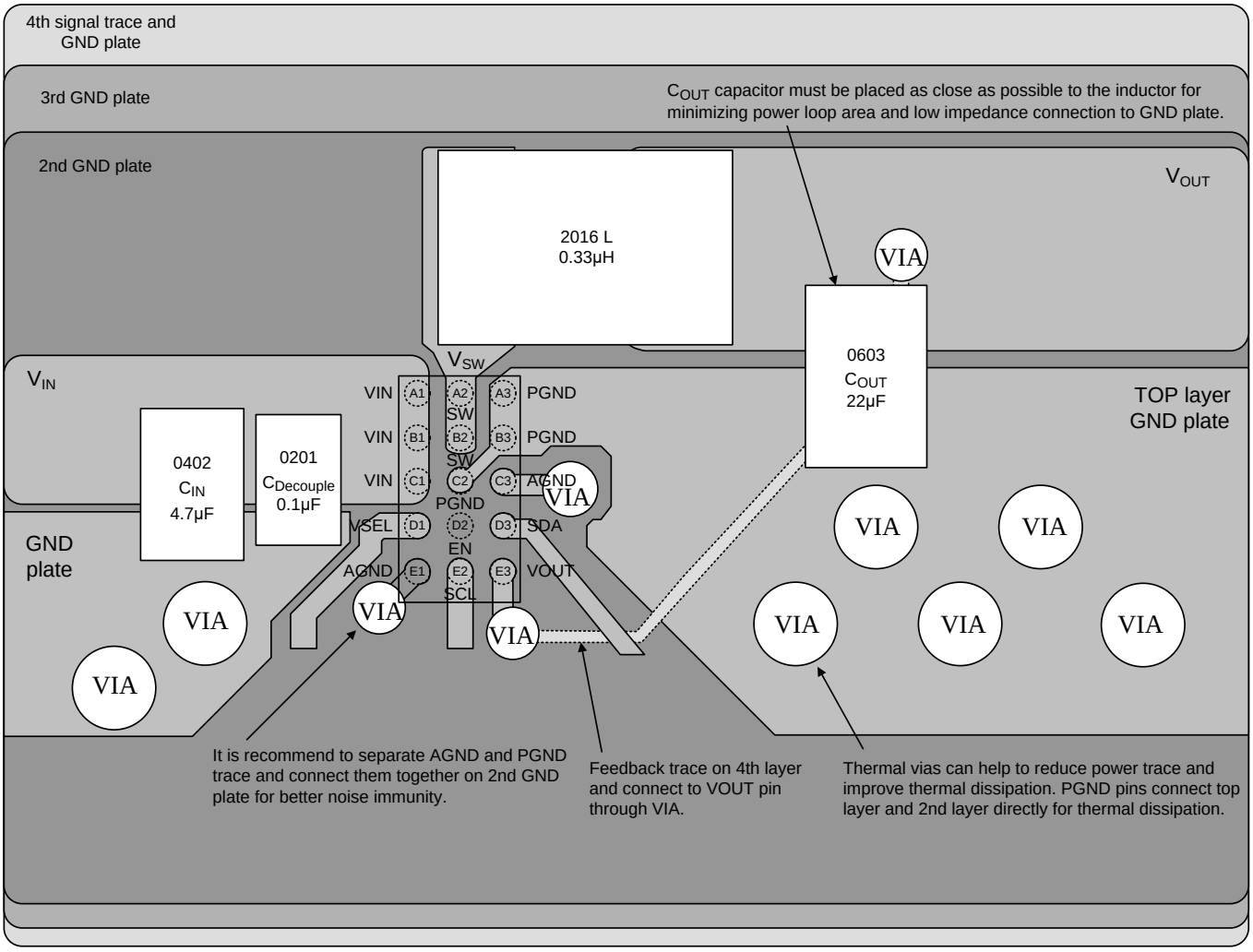
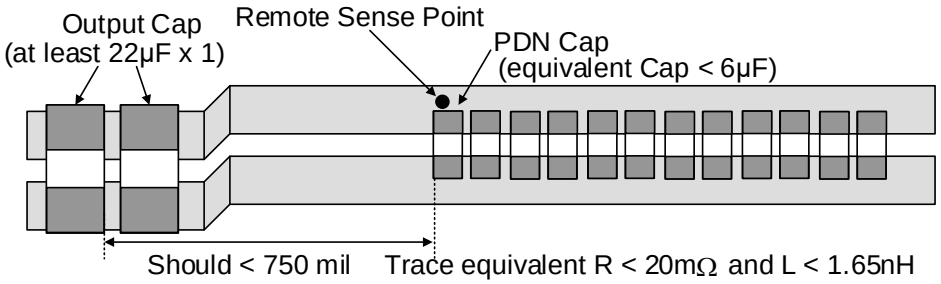
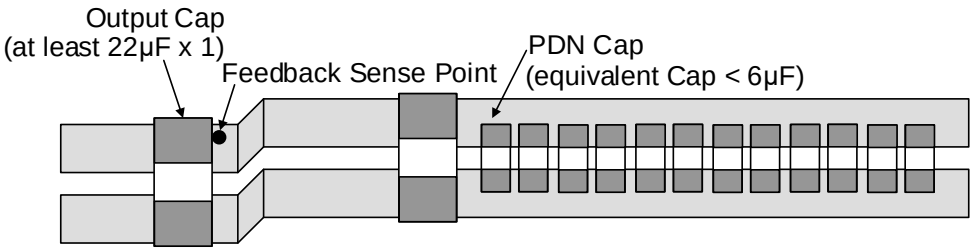


Figure 8. PCB Layout Guide for WL-CSP-15B 1.31x 2.02 (BSC) package

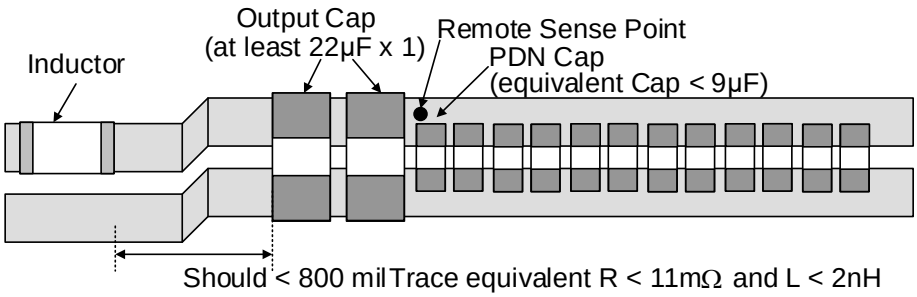
Layout Constraints for Remote Sense Applications



Case 1 :
If the remote sense point is located at PDN cap
, the distance between 1st 22µF cap and PDN cap should not exceed 750 mil.



Case 2 :
If the remote sense point is located at 1st 22µF cap
, there will be no constraint between 1st 22µF cap and PDN cap yet sacrifice AP transient performance with this configuration.



Case 3 :
If the remote sense point is located at PDN cap and there is long trace between 1st 22µF cap and inductor, the distance should not exceed 800mil.

Figure 9. Layout Constraints

I²C Interface

RT5733AGQW I²C slave address is 7'b1010000, and its default output voltage setting is 0.5V/0.9V.

RT5733AWSC I²C slave address is 7'b1010000, and its default output voltage setting is 0.5V/0.9V.

Address Name	Register Address		Part No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NSEL0	0x00	Meaning	VSEL0								
		Default	RT5733AGQW	0	0	1	0	0	1	0	1
			RT5733AWSC	0	0	1	0	0	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL1	0x01	Meaning	VSEL1								
		Default	RT5733AGQW	0	1	1	0	0	1	0	1
			RT5733AWSC	0	1	1	0	0	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Name	Register Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONTROL1	0x02	Meaning	DISCHG	UP_SR [2:0]		Reserved	SW_ RESET		MODE_ VSEL1	MODE_ VSEL0
		Default	1	0	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
ID1	0x03	Meaning	VENDOR_ID			Reserved	DIE_ID			
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
ID2	0x04	Meaning	Reserved				DIE_REV			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
MONITOR	0x05	Meaning	PGOOD	UVLO	Reserved	POS	NEG	RESET _ STAT	OT	BUCK_ STATUS
		Default	0	0	--	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_ VSEL0
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
CONTROL5	0x0A	Meaning	Reserved						LPM	REG_ I2C_ TIME_ OUT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R/W	R/W

The I²C register function description is introduced in the following table.

Register Name	Register Address		Part No.	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL0	0x00	Meaning	VSEL0								
		Default	RT5733AGQW	0	0	1	0	0	1	0	1
			RT5733AWSC	0	0	1	0	0	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL0			VID table satisfy: SEL[7:0] = 10110101: V_{OUT} = 1.40125V … SEL[7:0] = 00000000: 0.27V 6.25mV step for 0.27V to 1.40125V								

Register Name	Register Address		Part No	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL1	0x01	Meaning	VSEL1								
		Default	RT5733AGQW	0	1	1	0	0	1	0	1
			RT5733AWSC	0	1	1	0	0	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL1			VID table satisfy: SEL[7:0] = 10110101: V_{OUT} = 1.40125V … SEL[7:0] = 00000000: 0.27V 6.25mV step for 0.27V to 1.40125V								

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL1	0x02	Meaning	DISCHG	UP_SR[2:0]			Reserved	SW_ RESET	MODE_ VSEL1	MODE_ VSEL0
		Default	1	0	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DISCHG			0: Disable internal output discharge resistor							
			1: Enable internal output discharge resistor							
UP_SR[2:0]			DVS speed for DVS up 000 = 25mV/μs 001 = 12.5mV/μs 010 = 6.25mV/μs 011 = 3.1mV/μs 100 = 1.56mV/μs 101 = 0.75mV/μs 110 = 0.39mV/μs 111 = 0.19mV/μs							
SW_RESET			Write 1 to reset, always read 0							
MODE_VSEL1			0: Auto PFM/PWM mode							
			1: Forced PWM mode							
MODE_VSEL0			0: Auto PFM/PWM mode							
			1: Forced PWM mode							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
ID1	0x03	Meaning	VENDOR_ID[2:0]			Reserved	DIE_ID[3:0]			
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
VENDOR_ID[2:0]			Vendor_ID							
DIE_ID[3:0]			DIE_ID							
Register Name	**Register Address**		**b[7] (MSB)**	**b[6]**	**b[5]**	**b[4]**	**b[3]**	**b[2]**	**b[1]**	**b[0] (LSB)**
ID2	0x04	Meaning	Reserved				DIE_REV[3:0]			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
DIE_REV[3:0]			Revision_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
MONITOR	0x05	Meaning	PGOOD	UVLO	Reserved	POS	NEG	RESET_ STAT	OT	BUCK_ STATUS
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R

PGOOD	1: Buck is enabled and soft-start is completed.
UVLO	1: Signifies the V_{IN} is less than the UVLO threshold.
POS	1: Signifies a positive voltage transition is in progress
NEG	1: Signifies a negative voltage transition is in progress
RESET_STAT	1: Indicates that a register reset was performed.
OT	1: Signifies the thermal shutdown is active.
BUCK_STATUS	1: Buck enabled; 0: Buck disabled.

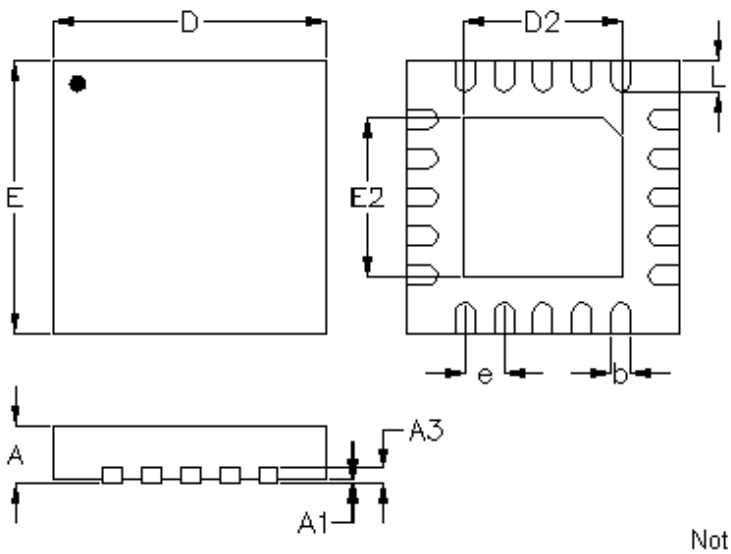
Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_ VSEL0
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

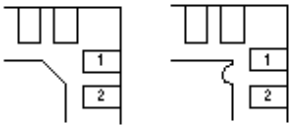
DN_SR[2:0]	DVS speed for DVS down 000 = 25mV/μs 001 = 12.5mV/μs 010 = 6.25mV/μs 011 = 3.1mV/μs 100 = 1.56mV/μs 101 = 0.75mV/μs 110 = 0.39mV/μs 111 = 0.19mV/μs
SS_SR[1:0]	DVS speed for soft-start DVS 00 = 10mV/μs 01 = 5mV/μs 10 = 2.5mV/μs 11 = 1.25mV/μs
EN_VSEL1	Software power-on/off control register (activate when the VSEL pin set to logic-high): 0: Disable output 1: Enable output
EN_VSEL0	Software power-on/off control register (activate when the VSEL pin set to logic-low): 0: Disable output 1: Enable output

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
DIS_DLY[5:0]			Delay applied upon disable (ms) 000000b = 0ms - 111111b = 63ms (steps of 1ms)							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL5	0x0A	Meaning	Reserved						LPM	REG_I2C_ TIME_OUT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
LPM			Low power mode (LPM) control register: 0: Disable low power mode function 1: Enable low power mode function for power saving.							
REG_I2C_TIME_OUT			I^2C time-out control register: 0: Disable I^2C time-out feature 1: Enable I^2C time-out feature to prevent from system hangout situation; the device will automatically reset I^2C to restore communication.							

Outline Dimension





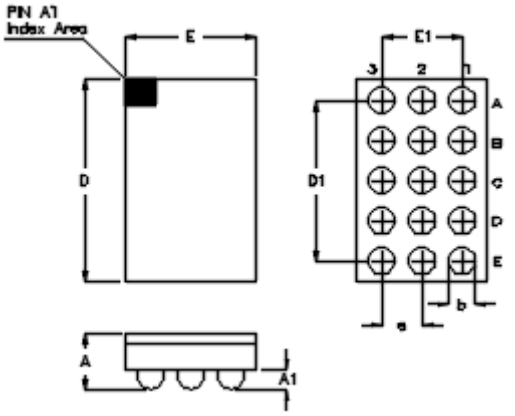
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

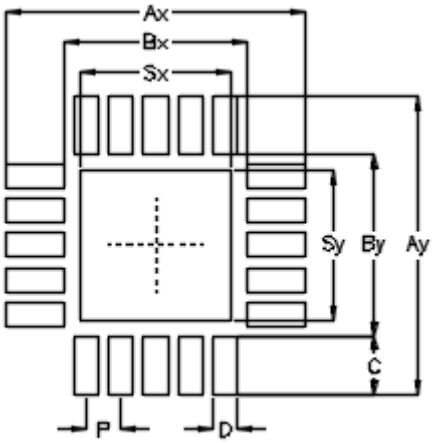
W-Type 20L QFN 3.5x3.5 Package



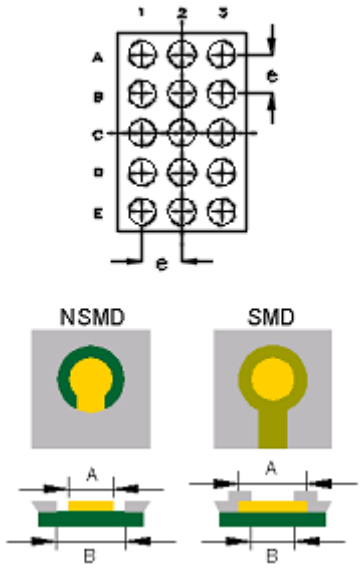
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.980	2.060	0.078	0.081
D1	1.600		0.063	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.31x2.02 Package (BSC)

Footprint Information



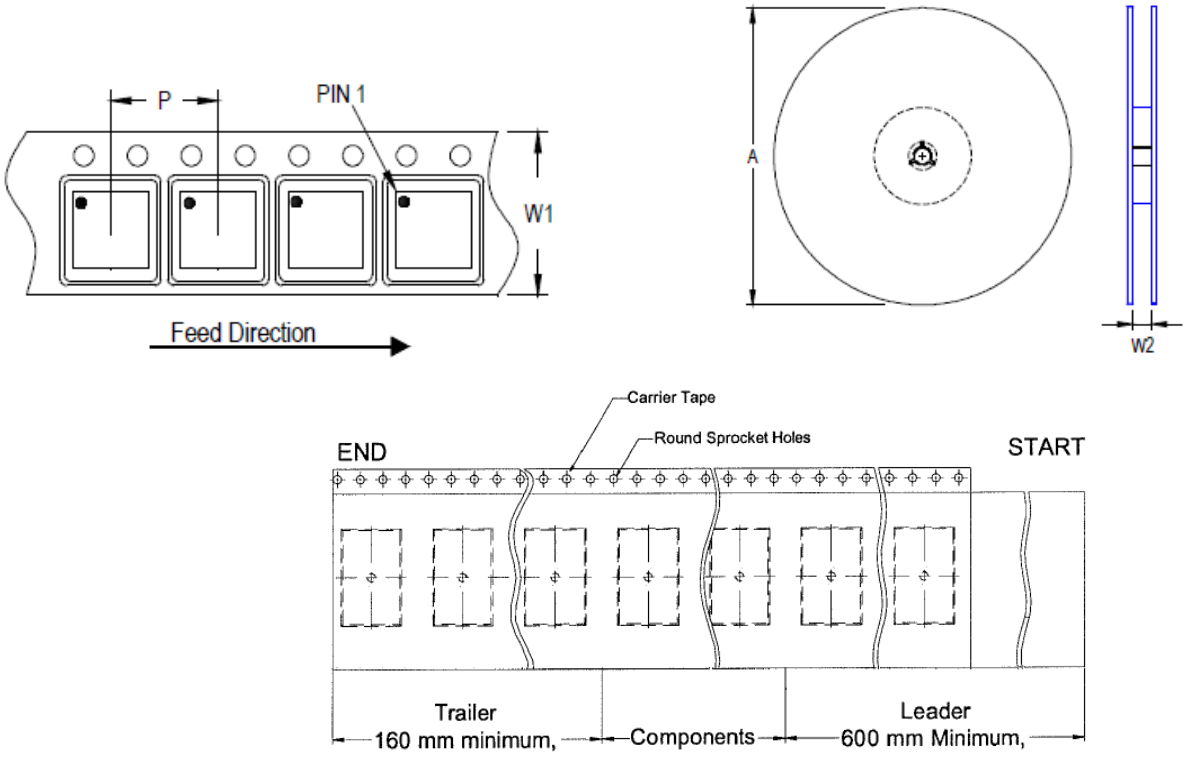
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*3.5-20	20	0.50	4.30	4.30	2.60	2.60	0.85	0.35	2.15	2.15	±0.05



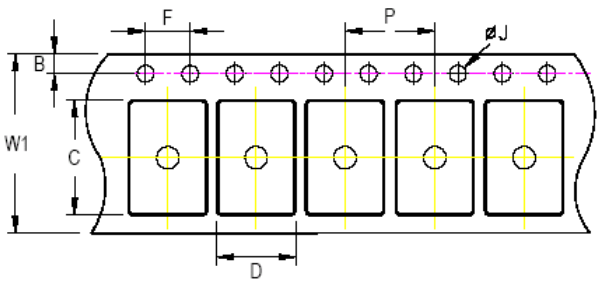
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31*2.02-15(BSC)	15	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Packing Information

Tape and Reel Data (QFN/DFN 3.5x3.5)



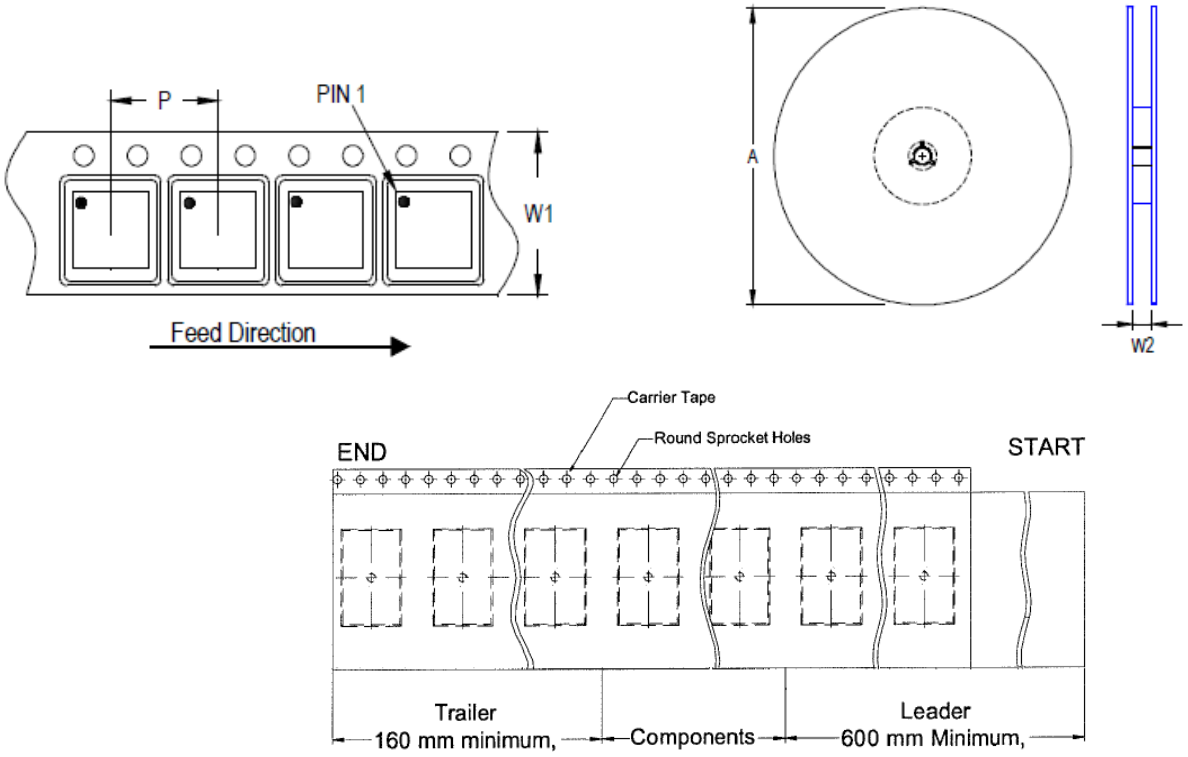
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3.5x3.5	12	8	180	7	1,500	160	600	12.4/14.4



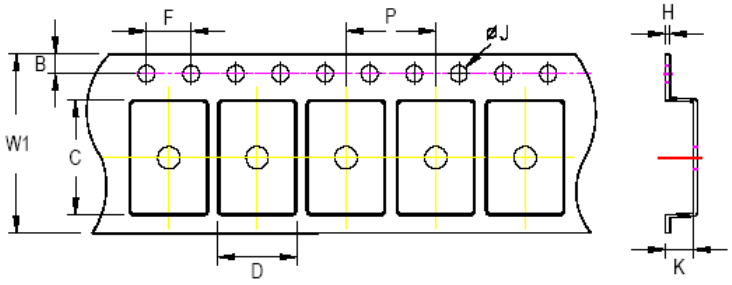
C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Data (WL-CSP 1.31x2.02)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.31x2.02	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing (QFN/DFN 3.5x3.5)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 3.5x3.5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Un-full Reel.			

Tape and Reel Packing (WL-CSP 1.31x2.02)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
WL-CSP 1.31x2.02	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Un-full Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$

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Datasheet Revision History

Version	Date	Description	Item
00	2023/2/1	Final	