6V 1A, ACOT® Buck Converter

General Description
The RT5750A/B is a simple, easy-to-use, 1A synchronous step-down DC-DC converter with an input supply voltage range from 2.5V to 6V. The device build-in an accurate 0.6V reference voltage and integrates low R_{DS(ON)} power MOSFETs to achieve high efficiency in a TSOT-23-5 and TSOT-23-6 package.

The RT5750A/B adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT5750A operate in automatic PSM that maintain high efficiency during light load operation. The RT5750B operate in Forced PWM that help to meet tight voltage regulation accuracy requirements.

The RT5750A/B senses both FETs current for a robust over-current protection. The device features cycle-by-cycle current limit protection and prevent the device from the catastrophic damage in output short circuit, over current or inductor saturation. A built-in soft-start function prevents inrush current during start-up. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection to provide safe and smooth operation in all operating conditions.

Features
- Input Voltage Range from 2.5V to 6V
- Integrated 120mΩ and 80mΩ FETs
- 1A Output Current, up to 95% Efficiency
- 100% Duty Cycle for Lowest Dropout
- 1.5% Internal Reference Voltage
- 1.5MHz Typical Switching Frequency
- Power Saving Mode for Light Loads (RT5750A)
- Low Quiescent Current: 25μA (Typ.)
- Fast Advanced Constant On-Time (ACOT®) Control
- Internal Soft Startup (0.6ms)
- Enable Control Input
- Power Good Indicator (TSOT-23-6)
- Both FETs Over-Current Protection
- Negative Over-Current Protection (RT5750B)
- Input Under-Voltage Lockout Protection
- Hiccup-Mode Output Under-Voltage Protection
- Over-Temperature Protection
- RoHS Compliant and Halogen Free

Applications
- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter

Simplified Application Circuit

![Simplified Application Circuit Diagram]

*PG : TSOT-23-6 only.
Ordering Information

RT5750

- Package Type
  - J5: TSOT-23-5
  - J6: TSOT-23-6
- Lead Plating System
  - G: Green (Halogen Free and Pb Free)
- UVP Option
  - H: Hiccup
- PWM Operation Mode
  - A: Automatic PSM
  - B: Forced PWM

Note:

Richtek products are:
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT5750AHGJ5

- 9M = Product Code
- DNN = Date Code

RT5750AHGJ6

- 3G = Product Code
- DNN = Date Code

RT5750BHGJ5

- 9L = Product Code
- DNN = Date Code

RT5750BHGJ6

- 3F = Product Code
- DNN = Date Code

Pin Configuration

(TOP VIEW)

- TSOT-23-5
- TSOT-23-6
## Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSOT-23-6</td>
<td>TSOT-23-5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EN</td>
<td>Enable control input. Connect this pin to logic high enables the device and connect this pin to GND disables the device. Do not leave this pin floating.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.</td>
</tr>
<tr>
<td>3</td>
<td>SW</td>
<td>Switch node between the internal switch. Connect this pin to the inductor.</td>
</tr>
<tr>
<td>4</td>
<td>VIN</td>
<td>Power input. The input voltage range is from 2.5V to 6V. Connect input capacitors directly to this pin and GND pins. MLCC with capacitance higher than 10µF is recommended.</td>
</tr>
<tr>
<td>5</td>
<td>--</td>
<td>Power good indicator. The output of this pin is an open-drain with external pull-up resistor. After soft startup, PG is pulled up when the FB voltage is within 90% (typ.). The PG status is low while EN is disable.</td>
</tr>
<tr>
<td>6</td>
<td>FB</td>
<td>Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at Feedback Reference Voltage, typically 0.6V.</td>
</tr>
</tbody>
</table>
Functional Block Diagram

For TSOT-23-6

For TSOT-23-5
Operation

The RT5750A/B is a high-efficiency, synchronous step-down DC-DC converter that can deliver up to 1A output current from a 2.5V to 6V input supply.

Advanced Constant On-Time Control and PWM Operation

The RT5750A/B adopts ACOT® control for its ultrafast transient response, low external component counts and stable with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (80ns, typ.) has timed out and the inductor current is below the current limit threshold, then the internal on-time one-shot circuitry is triggered and the high-side switch is turn-on. Since the minimum off-time is short, the device exhibits ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to input voltage and directly proportional to output voltage to achieve pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer expired, the high-side switch is turn-off and the low-side switch is turn-on until the on-time one-shot is triggered again. In the steady state, the error amplifier compares the feedback voltage $V_{FB}$ and an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator.

Power Saving Mode (RT5750A)

The RT5750A automatically enters power saving mode (PSM) at light load to maintain high efficiency. As the load current decreases and eventually the inductor current ripple valley touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level that requires the next on-time. The switching frequency decreases and is proportional to the load current to maintain high efficiency at light load.

Enable Control

The RT5750A/B provides an EN pin, as an external chip enable control, to enable or disable the device. If $V_{EN}$ is held below a logic-low threshold voltage ($V_{EN_L}$) of the enable input (EN), the converter will disable output voltage, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold ($V_{UVLO}$). During shutdown mode, the supply current can be reduced to $I_{SHDN}$ (1uA or below). If the EN voltage rises above the logic-high threshold voltage ($V_{EN,H}$) while the VIN voltage is higher than UVLO threshold, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. Do not leave this pin floating.

Soft-Start (SS)

The RT5750A/B provides an internal soft-start feature for inrush control. At power up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage $V_{FB}$ to ensure the converters have a smooth start-up from pre-biased output. The output voltage starts to rise in 0.1ms from EN rising, and the soft-start ramp-up time (10%$V_{OUT}$ to 90%$V_{OUT}$) is 0.6ms.

Maximum Duty Cycle Operation

The RT5750A/B is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off time
Power Good Indication (TSOT-23-6)
The RT5750A/B features an open-drain power-good output (PGOOD) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PGOOD with a resistor to VOUT or an external voltage below 6V. When VIN voltage rises above VUVLO, the power-good function is activated. After soft start is finished, the PGOOD pin is controlled by a comparator connected to the feedback signal VFB. If VFB rises above a power-good high threshold (VTH_PGLH) (typically 90% of the reference voltage), the PGOOD pin will be in high impedance and VPGOOD will be held high. When VFB falls short of power-good low threshold (VTH_PGHL) (typically 85% of the reference voltage), the PGOOD pin will be pulled low after a certain delay (60μs, typically) elapsed. Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND. The internal open-drain pull-down device (10Ω, typically) will pull the PGOOD pin low. The power good indication profile is shown below.

Input Under-Voltage Lockout
In addition to the EN pin, the RT5750A/B also provides enable control through the VIN pin. If VEN rises above VEN_H first, switching will still be inhibited until the VIN voltage rises above VUVLO. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage (VUVLO – ΔUVLO), this switching will be inhibited; if VIN rises above the UVLO rising threshold (VUVLO), the device will resume normal operation with a complete soft-start.

The Over-Current Protection
The RT5750A/B features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation.

The high-side MOSFET over-current protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (ILIM_H) after a certain amount of delay when the high-side switch being turned on each cycle. If an over-current condition occurs, the converter will immediately turns off the high-side switch and turns on the low-side switch to prevent the inductor current exceeding the high-side current limit.

The low-side MOSFET over-current protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (ILIM_L), the on-time one-shot will be inhibited until the inductor current

---

**Table 1. PG Pin Status**

<table>
<thead>
<tr>
<th>Conditions</th>
<th>PG Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable</td>
<td>VEN &gt; VEN_H, VFB &gt; VTH_PGLH</td>
</tr>
<tr>
<td></td>
<td>VEN &gt; VEN_H, VFB &lt; VTH_PGHL</td>
</tr>
<tr>
<td>Shutdown</td>
<td>VEN &lt; VEN_L</td>
</tr>
<tr>
<td>OTP</td>
<td>TJ &gt; TSD</td>
</tr>
</tbody>
</table>

---

Figure 2. The Logic of PGOOD

Copyright © 2020 Richtek Technology Corporation. All rights reserved. RICHTEK is a registered trademark of Richtek Technology Corporation.

www.richtek.com  DS5750A/B-00  May 2020
ramps down to the current limit level (\(I_{\text{LIM_L}}\)), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

**Over-Current Protection**

When the RT5750A/B is disabled by EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (150\(\Omega\)) connected to ground. This function prevents the reverse current flow from the output capacitors to the input capacitors once the input voltage collapses. It doesn’t need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

**Hiccup-Mode Output Under-Voltage Protection**

The RT5750A/B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage \(V_{\text{FB}}\). If \(V_{\text{FB}}\) drops below the under-voltage protection trip threshold (typically 50% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RT5750A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for \(t_{\text{HICCUP_OFF}}\) (2.4ms), and then attempt to recover automatically for \(t_{\text{HICCUP_ON}}\) (1.2ms). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short circuit protection and recovery profile is shown below.

**Thermal Shutdown**

The RT5750A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold (\(T_{\text{SD}}\)). Once the junction temperature cools down by a thermal shutdown hysteresis (\(\Delta T_{\text{SD}}\)), the IC will resume normal operation with a complete soft-start.

Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.
Negative Over-Current Limit (RT5750B)

The RT5750B is the part which is forced to PWM and allows negative current operation. In case of PWM operation, high negative current may be generated as an external power source which is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of low-side MOSFET and compares it with NOC threshold. Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect low-side MOSFET. However, the negative current can’t be limited at NOC threshold anymore since minimum off-time is reached.
Absolute Maximum Ratings  (Note 1)
- Supply Input Voltage, VIN----------------------------------------------- −0.3V to 6.5V
- Switch Voltage, SW----------------------------------------------- −0.3V to 6.5V
  < 50ns----------------------------------------------- −2.5V to 9V
- Other Pins----------------------------------------------- −0.3V to 6.5V
- Power Dissipation, $P_D @ T_A = 25^\circ C$
  TSOT-23-5----------------------------------------------- 1.26W
  TSOT-23-6----------------------------------------------- 1.35W
- Lead Temperature (Soldering, 10 sec.)----------------------------------------------- 260°C
- Junction Temperature----------------------------------------------- 150°C
- Storage Temperature Range----------------------------------------------- −65°C to 150°C

ESD Ratings
  ESD Susceptibility  (Note 2)
  HBM (Human Body Model)----------------------------------------------- 2kV

Recommended Operating Conditions  (Note 3)
- Supply Input Voltage----------------------------------------------- 2.5V to 6V
- Output Voltage----------------------------------------------- 0.6V to $V_{IN}$
- Junction Temperature Range----------------------------------------------- −40°C to 125°C

Thermal Information  (Note 4 and Note 5)

<table>
<thead>
<tr>
<th>Thermal Parameter</th>
<th>TSOT-23-5</th>
<th>TSOT-23-6</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>Junction-to-ambient thermal resistance (JEDEC standard)</td>
<td>230.6</td>
<td>197.6</td>
</tr>
<tr>
<td>$\theta_{JC(Top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>21.8</td>
<td>18.9</td>
</tr>
<tr>
<td>$\theta_{JC(Bottom)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>19.7</td>
<td>25</td>
</tr>
<tr>
<td>$\theta_{JA(EVB)}$</td>
<td>Junction-to-ambient thermal resistance (specific EVB)</td>
<td>79.1</td>
<td>74</td>
</tr>
<tr>
<td>$\Psi_{JC(Top)}$</td>
<td>Junction-to-top characterization parameter</td>
<td>7.1</td>
<td>10.7</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN Supply Input Operating Voltage</td>
<td>V_{IN}</td>
<td></td>
<td>2.5</td>
<td>--</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Under-Voltage Lockout Threshold</td>
<td>V_{UVLO}</td>
<td>V_{IN} rising</td>
<td>2.15</td>
<td>2.3</td>
<td>2.47</td>
<td>V</td>
</tr>
<tr>
<td>Under-Voltage Lockout Threshold Hysteresis</td>
<td></td>
<td>\Delta V_{UVLO}</td>
<td>--</td>
<td>300</td>
<td>--</td>
<td>mV</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>I_{SHDN}</td>
<td>V_{EN} = 0V</td>
<td>--</td>
<td>0.3</td>
<td>1</td>
<td>\mu A</td>
</tr>
<tr>
<td>Quiescent Current (RT5750A)</td>
<td>I_Q</td>
<td>V_{EN} = 2V, V_{FB} = 0.63V</td>
<td>--</td>
<td>25</td>
<td>35</td>
<td>\mu A</td>
</tr>
<tr>
<td>Quiescent Current (RT5750B)</td>
<td></td>
<td></td>
<td>--</td>
<td>300</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Soft-Start</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft-Start Time</td>
<td>t_{SS}</td>
<td>10%V_{OUT} to 90%V_{OUT}</td>
<td>--</td>
<td>0.6</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Enable Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Voltage Threshold</td>
<td>V_{EN_H}</td>
<td>EN high-level input voltage</td>
<td>0.6</td>
<td>0.82</td>
<td>0.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_{EN_L}</td>
<td>EN low-level input voltage</td>
<td>0.5</td>
<td>0.76</td>
<td>0.9</td>
<td></td>
</tr>
<tr>
<td>Feedback Voltage and Discharge Resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feedback Threshold Voltage</td>
<td>V_{FB}</td>
<td></td>
<td>591</td>
<td>600</td>
<td>609</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback Input Current</td>
<td>I_{FB}</td>
<td>V_{FB} = 0.6V, T_A = 25°C</td>
<td>--0.1</td>
<td>0</td>
<td>0.1</td>
<td>\mu A</td>
</tr>
<tr>
<td>Internal MOSFET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-Side On-Resistance</td>
<td>R_{DS(ON)}_H</td>
<td>--</td>
<td>120</td>
<td>--</td>
<td>--</td>
<td>m\Omega</td>
</tr>
<tr>
<td>Low-Side On-Resistance</td>
<td>R_{DS(ON)}_L</td>
<td>--</td>
<td>80</td>
<td>--</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-Side Switch Current Limit</td>
<td>I_{LIM_H}</td>
<td></td>
<td>1.85</td>
<td>2.65</td>
<td>--</td>
<td>A</td>
</tr>
<tr>
<td>Low-Side Switch Valley Current Limit</td>
<td>I_{LIM_L}</td>
<td></td>
<td>1.05</td>
<td>1.55</td>
<td>2.05</td>
<td></td>
</tr>
<tr>
<td>Low-Side Switch Negative Valley Current Limit</td>
<td>I_{LIM_NL}</td>
<td></td>
<td>--</td>
<td>1.5</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>f_{SW}</td>
<td></td>
<td>--</td>
<td>1.5</td>
<td>--</td>
<td>MHz</td>
</tr>
<tr>
<td>On-Time Timer Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>t_{OFF_MIN}</td>
<td></td>
<td>--</td>
<td>80</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>Hiccup-Mode Output Under-Voltage Protection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVP Trip Threshold</td>
<td>V_{UVP}</td>
<td>Hiccup detect</td>
<td>--</td>
<td>50</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Threshold</td>
<td>T_{SD}</td>
<td></td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>\Delta T_{SD}</td>
<td></td>
<td>--</td>
<td>30</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>----------------------</td>
<td>----------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>Power Good</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Good High Threshold</td>
<td>$V_{TH_PGLH}$</td>
<td>$V_{FB}$ rising, PGOOD goes high</td>
<td>--</td>
<td>90</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>Power Good High Hysteresis</td>
<td>$\Delta V_{TH_PGLH}$</td>
<td>$V_{FB}$ falling, PGOOD goes low</td>
<td>--</td>
<td>5</td>
<td>--</td>
<td>%</td>
</tr>
<tr>
<td>Power Good Falling Delay Time</td>
<td></td>
<td></td>
<td>--</td>
<td>60</td>
<td>--</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Output Discharge Resistor</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Discharge Resistor</td>
<td></td>
<td></td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

**Note 4.** $\theta_{JA}$ and $\theta_{JC}$ are measured or simulated at $T_A = 25^\circ$C based on the JEDEC 51-7 standard.

**Note 5.** $\theta_{JA(EVB)}$ and $\Psi_{JC(TOP)}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.
Typical Application Circuit

*PG : TSOT-23-6 only.

Table 2. Suggested Component Values

<table>
<thead>
<tr>
<th>VOUT (V)</th>
<th>RFB1 (kΩ)</th>
<th>RFB2 (kΩ)</th>
<th>L (µH)</th>
<th>CFF (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>45</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
<tr>
<td>1.8</td>
<td>20</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
<tr>
<td>1.5</td>
<td>15</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
<tr>
<td>1.2</td>
<td>10</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
<tr>
<td>1.05</td>
<td>7.5</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
<tr>
<td>1</td>
<td>6.65</td>
<td>10</td>
<td>1.5</td>
<td>--</td>
</tr>
</tbody>
</table>

Table 3. Recommended External Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Vendor P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>10µF, 6.3V, X5R, 0603</td>
<td>0603X106M6R3 (WALSIN) GRM188R60J106ME84 (MURATA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>*COUT</td>
<td>10µF, 6.3V, X5R, 0603</td>
<td>0603X106M6R3 (WALSIN) GRM188R60J106ME84 (MURATA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>1.5µH</td>
<td>DFE252010F-1R5 (MURATA) HMLQ25201B-1R5MSR (CYNTEC)</td>
</tr>
</tbody>
</table>

*COUT : Considering the effective capacitance de-rated with biased voltage level and size, the COUT component needs satisfy the effective capacitance at least 4µF for VOUT = 3.3V and 7µF for VOUT < 3.3V for stable and normal operation.
Typical Operating Characteristic

Efficiency vs. Output Current

- **RT5750A, $V_{IN} = 3.6V$**
  - $V_{OUT} = 1.8V$
  - $V_{OUT} = 1V$

- **RT5750B, $V_{IN} = 3.6V$**
  - $V_{OUT} = 1.8V$
  - $V_{OUT} = 1V$

Efficiency vs. Output Current

- **RT5750A, $V_{IN} = 5V$**
  - $V_{OUT} = 3.3V$
  - $V_{OUT} = 1.8V$
  - $V_{OUT} = 1V$

- **RT5750B, $V_{IN} = 5V$**
  - $V_{OUT} = 3.3V$
  - $V_{OUT} = 1.8V$
  - $V_{OUT} = 1V$

Output Voltage vs. Output Current

- **RT5750A, $V_{IN} = 5V$, $V_{OUT} = 1V$**

- **RT5750B, $V_{IN} = 5V$, $V_{OUT} = 1V$**
Quiescent Current vs. Temperature

UVLO Threshold vs. Temperature

Enable Threshold vs. Temperature

Reference Voltage vs. Temperature

Load Transient Response

Load Transient Response

V_{IN} = 3.6V, V_{OUT} = 1V, I_{OUT} = 0.5A to 1A
T_R = T_F = 0.5\mu s, L = 1.5\mu H, C_{OUT} = 10\mu F \times 1

V_{OUT} (20mV/Div)
I_{OUT} (500mA/Div)

Time (10\mu s/Div)
**Load Transient Response**

- **VIN = 5V, VOUT = 1V, IOUT = 10mA to 0.5A**
- **TR = TF = 0.5μs, L = 1.5μH, COUT = 10μF x 1**
- Time (10μs/Div)

- **VIN = 5V, VOUT = 1V, IOUT = 0.5A to 1A**
- **TR = TF = 0.5μs, L = 1.5μH, COUT = 10μF x 1**
- Time (10μs/Div)

**Output Ripple Voltage**

- **VIN = 3.6V, VOUT = 1V, IOUT = 10mA**
- Time (5μs/Div)

- **VIN = 3.6V, VOUT = 1V, IOUT = 1A**
- Time (400ns/Div)

- **VIN = 5V, VOUT = 1V, IOUT = 10mA**
- Time (5μs/Div)

- **VIN = 5V, VOUT = 1V, IOUT = 1A**
- Time (400ns/Div)
- **Power On from EN**
  - $V_{IN} = 3.6V, V_{OUT} = 1V, I_{OUT} = 1A$
  - Time (500$\mu$s/Div)

- **Power Off from EN**
  - $V_{IN} = 3.6V, V_{OUT} = 1V, I_{OUT} = 1A$
  - Time (10$\mu$s/Div)

- **Power On from VIN**
  - $V_{IN} = 3.6V, V_{OUT} = 1V, I_{OUT} = 1A$
  - Time (500$\mu$s/Div)

- **Power Off from VIN**
  - $V_{IN} = 3.6V, V_{OUT} = 1V, I_{OUT} = 1A$
  - Time (100$\mu$s/Div)
Application Information

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I\textsubscript{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 50% of the IC rated current.

\[ \text{I}_{\text{L(PEAK)}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times f_{\text{SW}} \times \Delta L \]

Once an inductor value is chosen, the ripple current (\Delta L) is calculated to determine the required peak inductor current.

\[ \Delta L = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times f_{\text{SW}} \times L \]

\[ \text{I}_{\text{L(PEAK)}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times f_{\text{SW}} \times L \]

\[ \text{I}_{\text{L(PEAK)}} = \text{I}_{\text{OUT(MAX)}} + \frac{\Delta L}{2} \]

\[ \text{I}_{\text{L(PEAK)}} \text{ should not exceed the minimum value of IC's upper current limit level. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.} \]

\[ \Delta V_{\text{CIN}} = D \times \text{I}_{\text{OUT}} \times \left( \frac{1}{C_{\text{IN}} \times f_{\text{SW}}} \right) + \text{I}_{\text{OUT}} \times \text{ESR} \]

\[ D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \eta \]

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below:

\[ C_{\text{IN,MIN}} = \frac{D(1-D)}{\Delta V_{\text{CIN,MAX}} \times f_{\text{SW}}} \]

\[ \Delta V_{\text{CIN,MAX}} \leq 100\text{mV} \]
In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} \approx I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}}} - 1$$

It is commonly to use the worse $$I_{RMS} \approx I_{OUT}/2$$ at $$V_{IN} = 2V_{OUT}$$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT5750A/B circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device’s rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1µF should be placed close to the VIN and GND pin. This capacitor should be 0402 or 0603 in size.

**Output Capacitor Selection**

The RT5750A/B are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on load apply) and soar (overshoot on load release).

**Output Ripple**

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor’s impedance. To derive the output voltage ripple, the output capacitor with capacitance, $$C_{OUT}$$, and its equivalent series resistance, $$R_{ESR}$$, must be taken into consideration. The output peak-to-peak ripple voltage $$V_{RIPPLE}$$, caused by the inductor current ripple $$\Delta L$$, is characterized by two components, which are ESR ripple $$V_{RIPPLE(ESR)}$$ and capacitive ripple $$V_{RIPPLE(C)}$$, can be expressed as below:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RT5750A/B’s Typical Application Circuit for output voltage of 1V, and actual inductor current ripple ($$\Delta L$$) of 0.36A, taking a 10µF ceramic capacitors of GRM188R60J106ME84 from Murata as example, the output ripple of the output capacitor is as below:

The ripple caused by the ESR of about 5mΩ can be calculated as

$$V_{RIPPLE(ESR)} = 0.36A \times 5m\Omega = 1.8mV$$

Due to DC bias capacitance degrading, the effective capacitance at output voltage of 1V is about 8µF.

$$V_{RIPPLE(C)} = \frac{0.36A}{8 \times 8\mu F \times 1.5MHz} = 3.75mV$$

$$V_{RIPPLE} = 1.8mV + 3.75mV = 5.55mV$$
Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components: the voltage steps caused by the output capacitor’s ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

\[ V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR} \]

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as:

\[ t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad \text{and} \quad D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}} \]

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

\[ V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN\_MIN} \times D_{MAX} - V_{OUT})} \]

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage:

\[ V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}} \]

Due to some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 6. The output voltage is set according to the following equation:

\[ V_{OUT} = 0.6V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \]

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin can be connected to the input supply \( V_{IN} \) directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to \( V_{IN} \) by adding a resistor \( R_{EN} \) and a capacitor \( C_{EN} \), as shown in Figure 7, to have an additional delay. The time delay can be calculated with the EN’s internal threshold, at which switching operation begins (typically 0.82V).

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 8. In this case, a pull-up resistor, \( R_{EN} \), is connected between \( V_{IN} \) and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when \( V_{IN} \) is smaller than the VOUT target level or some other desired voltage level, a resistive divider (\( R_{EN1} \) and \( R_{EN2} \)) can be used to externally set...
the input under-voltage lockout threshold, as shown in Figure 9.

\[
P_{D\text{(MAX)}} = \frac{(T_{J\text{(MAX)}} - T_A)}{\theta_{JA}}
\]

where \(T_{J\text{(MAX)}}\) is the maximum junction temperature, \(T_A\) is the ambient temperature, and \(\theta_{JA}\) is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, \(\theta_{JA}\), is highly package dependent. For a TSOT-23-5 package, the thermal resistance, \(\theta_{JA}\), is 79.1°C/W on a high effective-thermal-conductivity four-layer test board. For a TSOT-23-6 package, the thermal resistance, \(\theta_{JA}\), is 74°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at \(T_A = 25°C\) can be calculated as below:

\[
P_{D\text{(MAX)}} = \frac{(125°C - 25°C)}{(79.1°C/W)} = 1.26W \text{ for a TSOT-23-5 package.}
\]

\[
P_{D\text{(MAX)}} = \frac{(125°C - 25°C)}{(74°C/W)} = 1.35W \text{ for a TSOT-23-6 package.}
\]

The maximum power dissipation depends on the operating ambient temperature for the fixed \(T_{J\text{(MAX)}}\) and the thermal resistance, \(\theta_{JA}\). The derating curves in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

**Power-Good Output**

The PGGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 6V, \(V_{CC}\) or the output of the RT5750A/B if the output voltage is regulated under 6V. It is recommended to connect a 100kΩ between external voltage source to PGGOOD pin.

**Thermal Considerations**

The junction temperature should never exceed the absolute maximum junction temperature \(T_{J\text{(MAX)}}\), listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

\[
P_{D\text{(MAX)}} = \frac{(T_{J\text{(MAX)}} - T_A)}{\theta_{JA}}
\]

**Layout Considerations**

Follow the PCB layout guidelines for optimal performance of the device.
Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.

Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT5750A/B.

SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.

Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.

For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

An example of PCB layout guide is shown from Figure 11.
The VIN trace should have enough width, and use several vias to shunt the high input current.

Place the input MLCC capacitors as close to the VIN and GND pins as possible.

Add extra vias for thermal dissipation.

Place the feedback components next to the FB pin.

Connect feedback network behind the output.

Keep analog components away from the SW node to prevent stray capacitive noise pickup.

The VIN trace should have enough width, and use several vias to shunt the high input current.

Figure 11. Layout Guide
## Outline Dimension

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>0.700</td>
<td>1.000</td>
</tr>
<tr>
<td>A1</td>
<td>0.000</td>
<td>0.100</td>
</tr>
<tr>
<td>B</td>
<td>1.397</td>
<td>1.803</td>
</tr>
<tr>
<td>b</td>
<td>0.300</td>
<td>0.559</td>
</tr>
<tr>
<td>C</td>
<td>2.591</td>
<td>3.000</td>
</tr>
<tr>
<td>D</td>
<td>2.692</td>
<td>3.099</td>
</tr>
<tr>
<td>e</td>
<td>0.838</td>
<td>1.041</td>
</tr>
<tr>
<td>H</td>
<td>0.080</td>
<td>0.254</td>
</tr>
<tr>
<td>L</td>
<td>0.300</td>
<td>0.610</td>
</tr>
</tbody>
</table>

**TSOT-23-5 Surface Mount Package**
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>0.700</td>
<td>1.000</td>
</tr>
<tr>
<td>A1</td>
<td>0.000</td>
<td>0.100</td>
</tr>
<tr>
<td>B</td>
<td>1.397</td>
<td>1.803</td>
</tr>
<tr>
<td>b</td>
<td>0.300</td>
<td>0.559</td>
</tr>
<tr>
<td>C</td>
<td>2.591</td>
<td>3.000</td>
</tr>
<tr>
<td>D</td>
<td>2.692</td>
<td>3.099</td>
</tr>
<tr>
<td>e</td>
<td>0.838</td>
<td>1.041</td>
</tr>
<tr>
<td>H</td>
<td>0.080</td>
<td>0.254</td>
</tr>
<tr>
<td>L</td>
<td>0.300</td>
<td>0.610</td>
</tr>
</tbody>
</table>

TSOT-23-6 Surface Mount Package
# Footprint Information

![Footprint Diagram](image.png)

<table>
<thead>
<tr>
<th>Package</th>
<th>Number of Pin</th>
<th>Footprint Dimension (mm)</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSOT-25/TSOT-25(FC)/SOT-25</td>
<td>5</td>
<td>P1</td>
<td>P2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.95</td>
<td>1.90</td>
</tr>
<tr>
<td>Package</td>
<td>Number of Pin</td>
<td>Footprint Dimension (mm)</td>
<td>Tolerance</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>---------------</td>
<td>-------------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>TSOT-26/TSOT-26(FC)/SOT-26/SOT-26(COL)</td>
<td>6</td>
<td>P1: 0.95 A: 3.60 B: 1.60 C: 1.00 D: 0.70 M: 2.60</td>
<td>±0.10</td>
</tr>
</tbody>
</table>