9A, 6.5V, 1MHz, ACOT® Synchronous Step-Down Converter with I²C Interface

General Description

The RT5759 is a high-performance, synchronous step-down DC-DC converter that can deliver up to 9A output current from a 3V to 6.5V input supply. The output voltage can be programmable from 0.6V to 1.5V with I²C controlled 7-Bits VID.

The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode of bootstrap circuit to offer a very compact solution.

The RT5759 adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultrafast transient response and further reduce the external-component count. In steady states, the ACOT® operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier. The RT5759 offers automatic PSM that maintains high efficiency during light load operation. The RT5759 can also operate in Forced-CCM through I²C setting that helps meet tight voltage regulation accuracy requirements.

The device offers a variety of functions for more design flexibility. The switching frequency, current limit level and over temperature threshold are selectable via I²C. Independent enable control input pin and power good indicator are also provided for easy sequence control. Besides, the designers can also command the device to be enabled or shutdown via the I²C interface.

The device offers Independent enable control input pin and power good indicator for easily sequence control. To control the inrush current during the startup, the device provides a programmable soft-start up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit control, UVP, input UVLO and OTP.

The RT5759 is available in a thermally enhanced UQFN-13L 3x3 (FC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

Features

- **Dramatically Fast Transient Response**
- **Steady 1MHz ±20% Switching Frequency**
- **Advanced COT Control Loop**
- **Optimized for Ceramic Output Capacitors**
- **3V to 6.5V Input Voltage Range**
- **Integrated 12mΩ/8mΩ MOSFETs**
- **Internal Start-Up into Pre-Biased Outputs**
- **Power Good Indicator**
- **Enable Control**
- **Over-Current and Over-Temperature Protections**
- **Under-Voltage Protection with Hiccup Mode**
- **VID Control Range Via I²C Compatible Interface: 0.6V to 1.5V step = 10mV**

Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platform
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter
- TV

Ordering Information

RT5759 □□

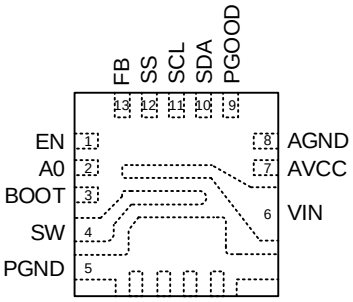
- Package Type
  QUF: UQFN-13L 3x3 (FC) (U-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

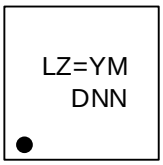
Pin Configuration

(TOP VIEW)



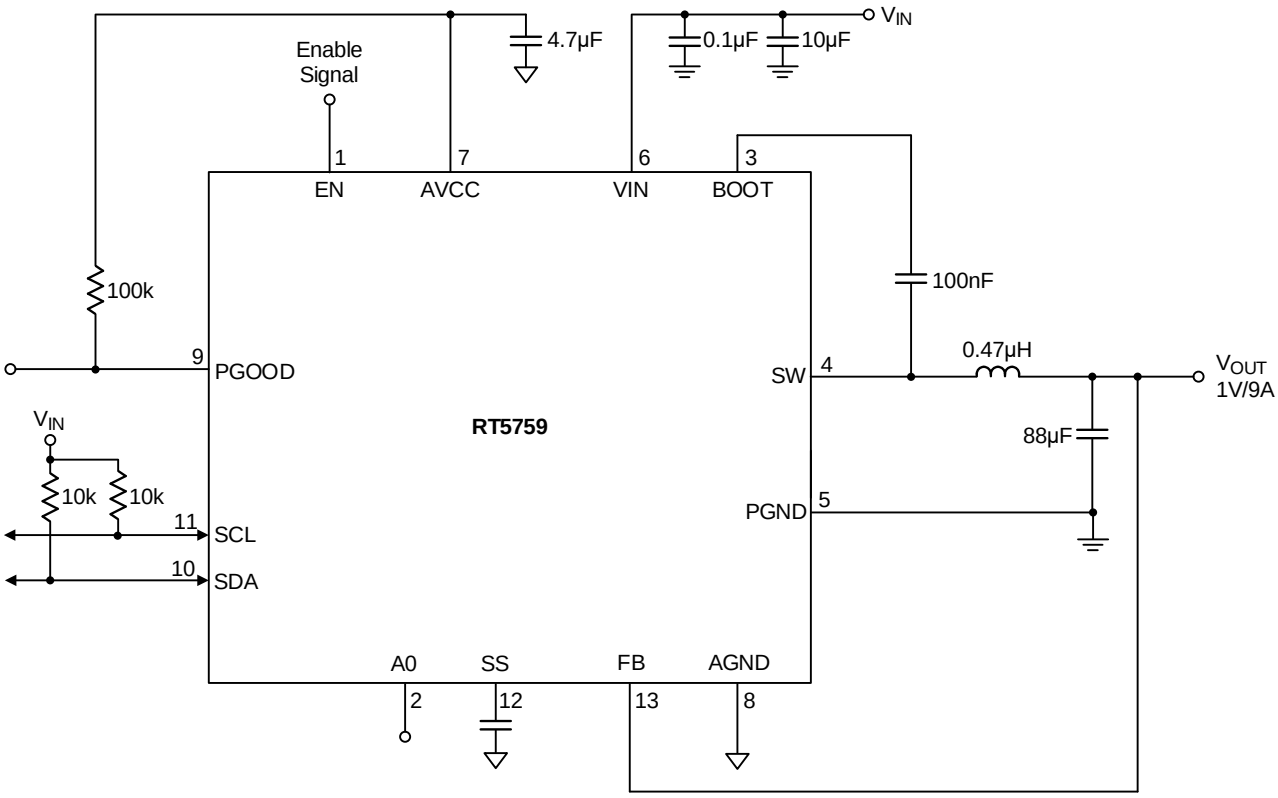
UQFN-13L 3x3 (FC)

Marking Information



LZ=: Product Code
YMDNN: Date Code

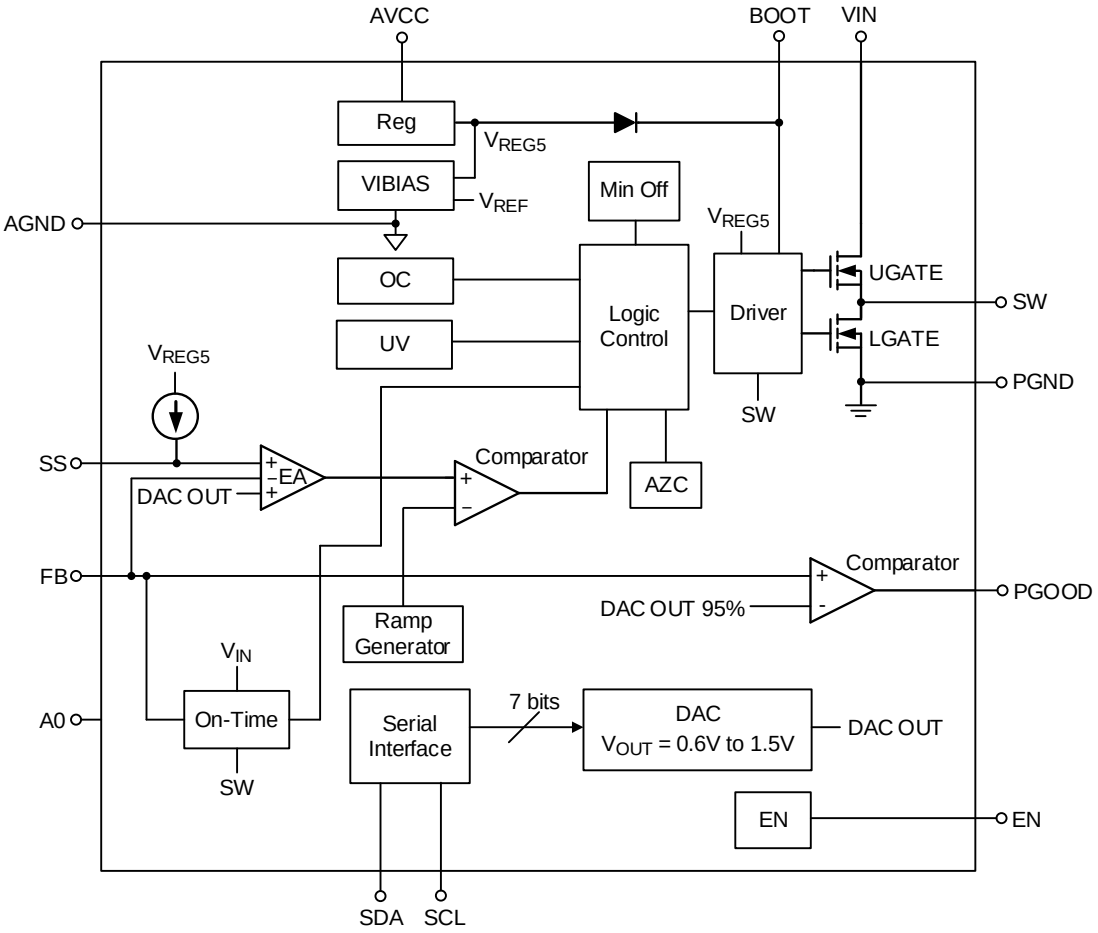
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode and reduces the supply current.
2	A0	I^2C setting. Device address select pin. High: xxxxx00, Low: xxxxx11, Floating: xxxxx10.
3	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
4	SW	Switch node. Connect this pin to an external L-C filter.
5	PGND	System GND. The power GND of the controller circuit. Use wide PCB traces to make the connections.
6	VIN	Input voltage. Support 3V to 6.5V input voltage. Connect this pin with a suitable capacitance for noise decoupling. The bypass capacitor should be placed as close to VIN pin as possible.
7	AVCC	LDO output for internal analog power. Connect a 4.7μF capacitor as close to the VCC pin as possible.
8	AGND	Analog GND. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
9	PGOOD	Power good indicator output. This pin has an open drain structure. Pull this pin high to a voltage source with a 100kΩ resistor.
10	SDA	I^2C interface, DATA.
11	SCL	I^2C interface, CLK.
12	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 1.045ms without external capacitor.
13	FB	Feedback input. The pin is used to set the output voltage of the converter via the I^2C interface.

Functional Block Diagram



Operation

The RT5759 is a low voltage synchronous step-down converter that can support input voltage ranging from 3V to 6.5V and the output current can be up to 9A. The RT5759 uses ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC.

This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors. In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Shutdown, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level of 0.74V. When V_{EN} is below this level the IC enters shutdown mode and supply current drops to less than 1μA. When V_{EN} exceeds its logic-high level of 0.92V the IC is fully operational. When V_{EN} exceeds its logic-high level, the pre-regulator turns on first. The power up sequence from EN logic high to PGOOD go high is shown as Figure 1.

Under-Voltage Protection (UVLO)

The UVLO continuously monitors the AVCC voltage to make sure the device works properly. When the AVCC is high enough to reach the UVLO high threshold voltage, the step-down converter softly starts or pre-bias to its regulated output voltage. When the AVCC decreases to its low threshold voltage, the device shuts down.

Power Good

Power Good pin is an open-drain logic output that is pulled to ground when the output voltage is lower or higher than its specified threshold under the conditions of OVP, OTP, dropout, EN shutdown, or during start up time. Start up time is the time of V_{OUT} soft-start when power up or enable up. During the start up time, the PGOOD is low even the output voltage is within the specified threshold voltage. Only the PGOOD indicator is high and output voltage is within the specified threshold voltage, then PGOOD is high.

External Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-MOSFET switch.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 70% reference voltage after soft-start, the UVP is triggered.

Over-Temperature Protection (OTP)

The RT5759 includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down and returns to 100°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

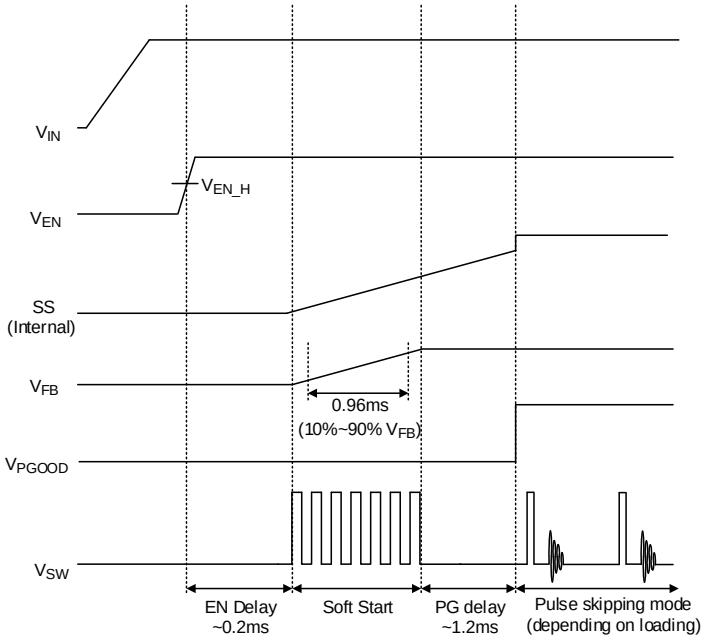


Figure 1. Power Up Sequence which is Following Internal Soft-Start

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 7V
- Switch Node Voltage, SW ---------- –0.3V to 7V
  (t ≤ 10ns) ---------- –3V to 8.5V
- Boot Voltage, BOOT ---------- –0.3V to 13V
- BOOT to SW (BOOT - SW) ---------- –0.3V to 6V
- Other Pins Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-13L 3x3 (FC) ---------- 2.62W
- Package Thermal Resistance (Note 2)
  UQFN-13L 3x3 (FC), θ_{JA} ---------- 38.1°C/W
  UQFN-13L 3x3 (FC), θ_{JC} ---------- 4.1°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 3V to 6.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Voltage	V_{IN}		3	--	6.5	V
Supply Current						
Sleep Supply Current	I_Q	V_{FB} > 0.6V	--	--	100	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V	--	--	1	μA
UVLO						
UVLO Rising Threshold	V_{UVLO_R}	V_{AVCC} rising	--	2.625	2.8	V
UVLO Falling Threshold	V_{UVLO_F}	V_{AVCC} falling	--	2.5	--	V
Logic Threshold						
EN Input Rising Threshold	V_{ENH}		0.77	0.92	1.07	V
EN Input Falling Threshold	V_{ENL}		0.58	0.74	0.9	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Hysteresis		ΔV_{EN}		--	0.18	--	V
Input Current		I_{EN}	V_{EN} = 2V	--	1	5	μA
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Recovery Threshold		T_{RC}		--	100	--	°C
Output Voltage and Soft-Start							
Output Voltage		V_{OUT}	CCM	0.985	1	1.015	V
Soft-Start Time		t_{SS}	V_{OUT} = 1V, leave SS pin floating, 10% to 90%V_{OUT}	--	1.6	--	ms
$R_{DS(ON)}$							
Switch On-Resistance	High-Side	$R_{DS(ON)\_H}$		--	12	--	mΩ
	Low-Side	$R_{DS(ON)\_L}$		--	8	--	
Current Limit							
Current Limit		I_{LIM}	Valley current	9.1	10.8	12.5	A
Switching Frequency and Minimum Off-Time							
Switching Frequency		f_{SW}	0x01[1:0] = 10b, CCM	0.8	1	1.2	MHz
Minimum Off-Time		t_{OFF_MIN}		--	100	--	ns
Protections							
UVP Trip Threshold		V_{UVP}		--	70	--	%
UVP Time Delay		t_{UVPDLY}		--	5	--	μs
Power Good							
PGOOD Rising Threshold		V_{TH_PGLH}	V_{FB} rising (Good)	--	95	--	%V_{FB}
		ΔV_{TH_PGLH}	V_{FB} rising (Fault)	--	110	--	
PG Falling Threshold		V_{TH_PGHL}	V_{FB} falling (Fault)	--	90	--	
		ΔV_{TH_PGHL}	V_{FB} falling (Good)	--	105	--	
PGOOD Enable Delay Time			0x05 PGDSET[3:2] = 01b	--	10	--	μs
Discharge Resistor							
Discharge Resistor		R_{DISCHG}	V_{EN} = 0V, V_{AVCC} = 5V	--	50	--	Ω
Regulation							
Line Regulation			CCM	--	0.5	--	%
Load Regulation (Note 5)			CCM	--	0.5	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C						
SDA, SCL Input Voltage		High level	1.2	--	--	V
		Low level	--	--	0.4	
Fast Mode						
SCL Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.6	--	--	µs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Set up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	µs
Data Set Up Time	$t_{SU;DAT}$		100	--	--	ns
Set Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time between a STOP and a START Condition	t_{BUF}		1.3	--	--	µs
Rising Time of Both SDA/SCL Signals	t_r		20	--	300	ns
Falling Time of Both SDA/SCL Signals	t_f		20	--	300	ns
SDA/SCL Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

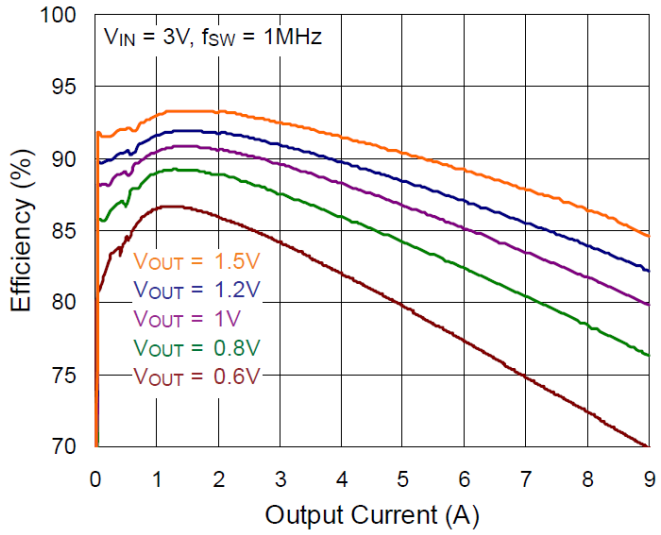
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

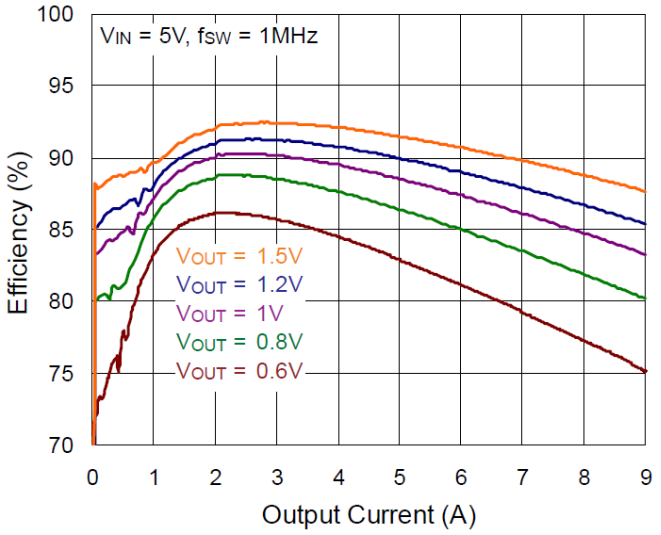
Note 5. Guaranteed by design.

Typical Operating Characteristic

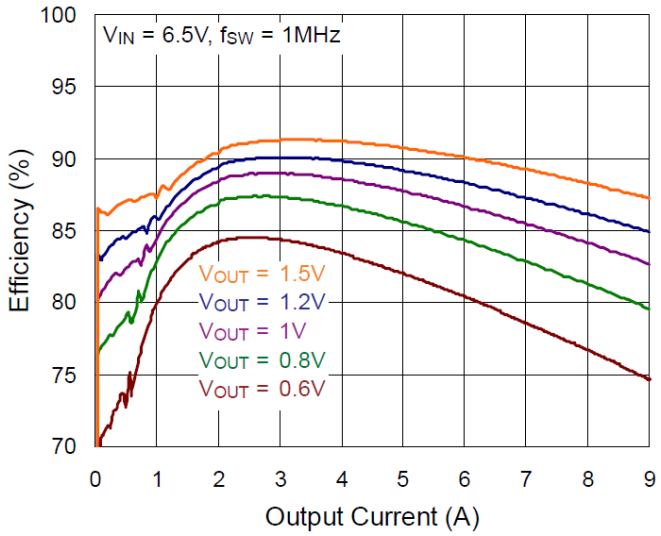
Efficiency vs. Output Current



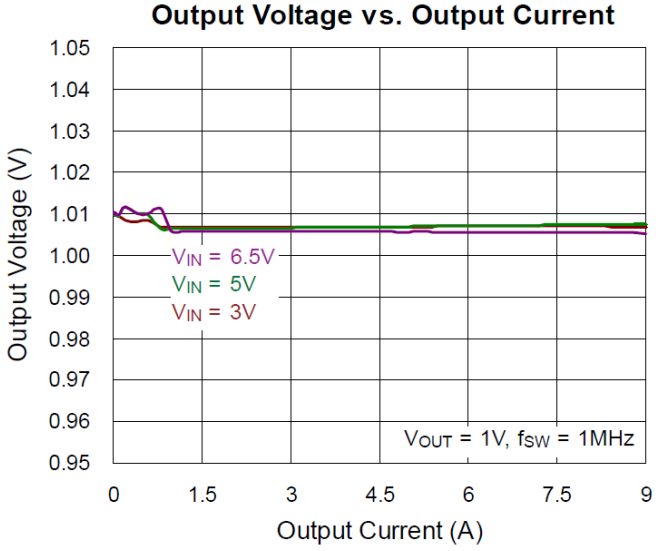
Efficiency vs. Output Current



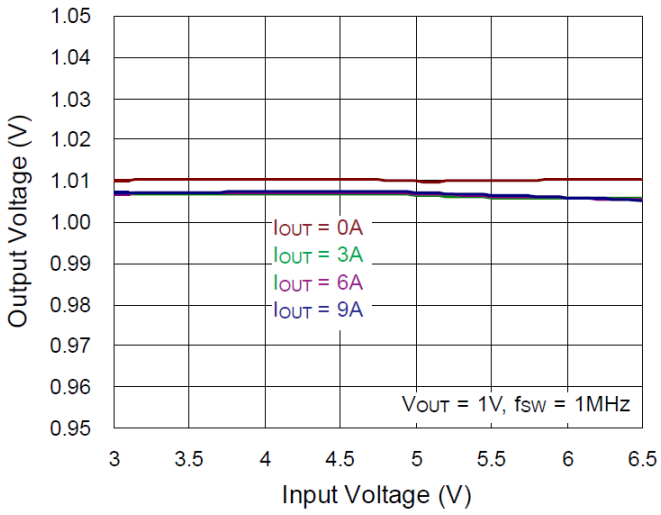
Efficiency vs. Output Current



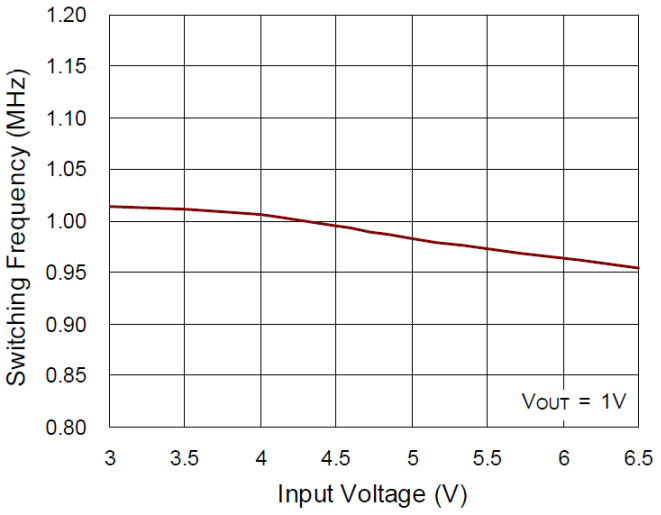
Output Voltage vs. Output Current



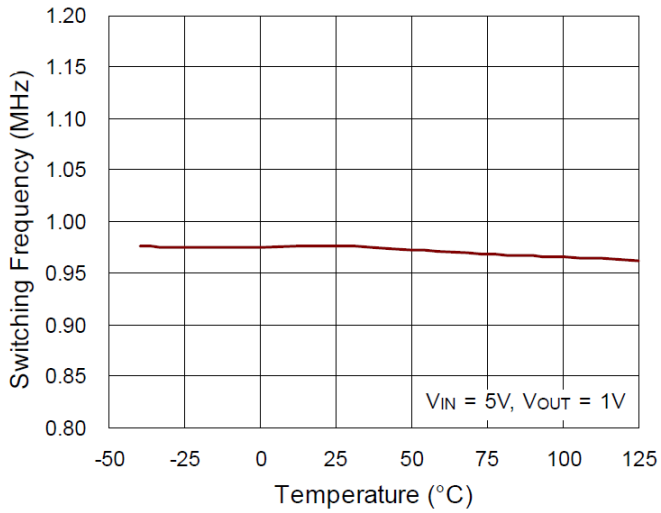
Output Voltage vs. Input Voltage



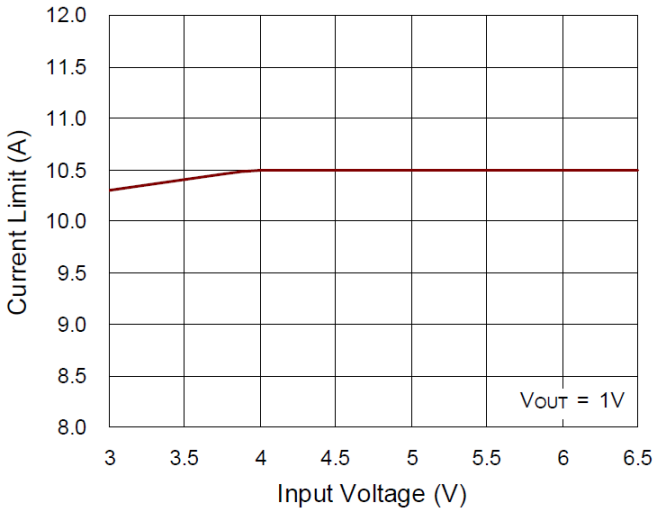
Switching Frequency vs. Input Voltage



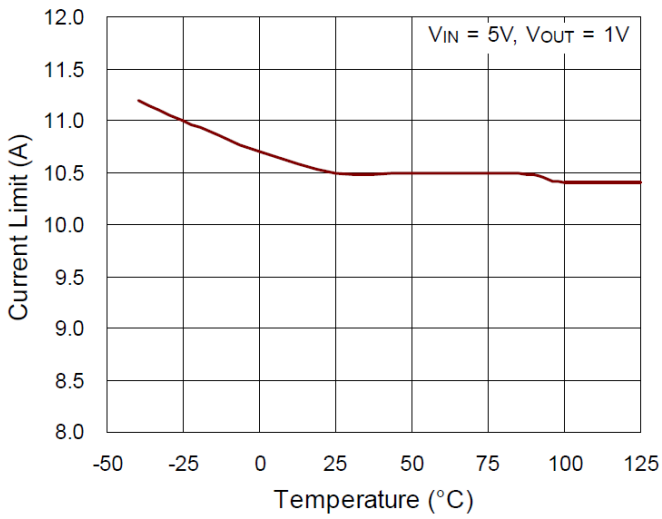
Switching Frequency vs. Temperature



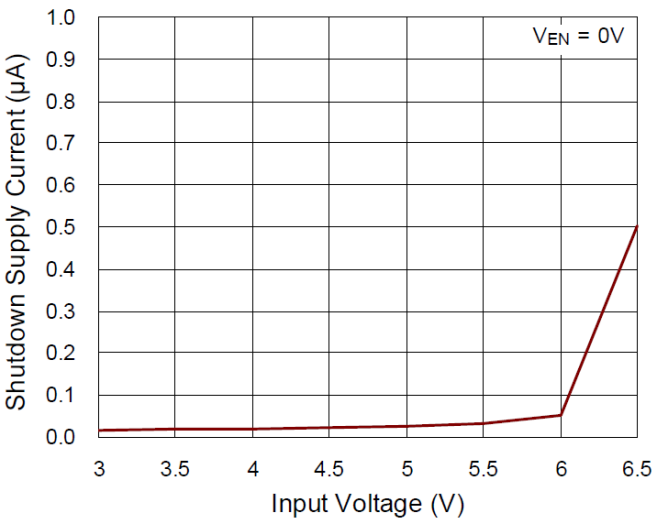
Current Limit vs. Input Voltage



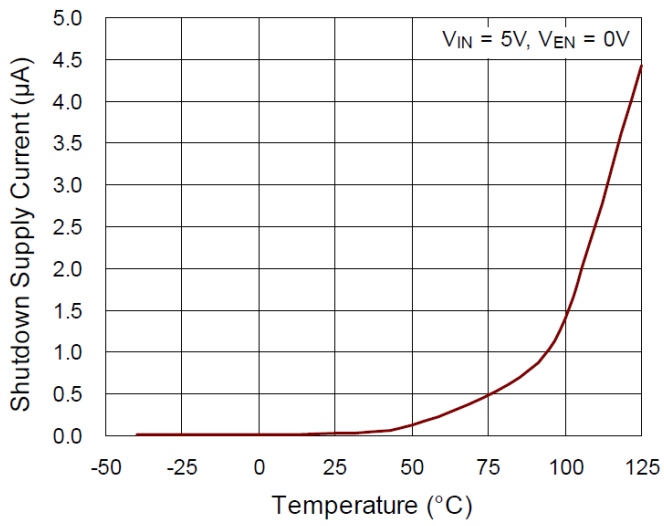
Current Limit vs. Temperature



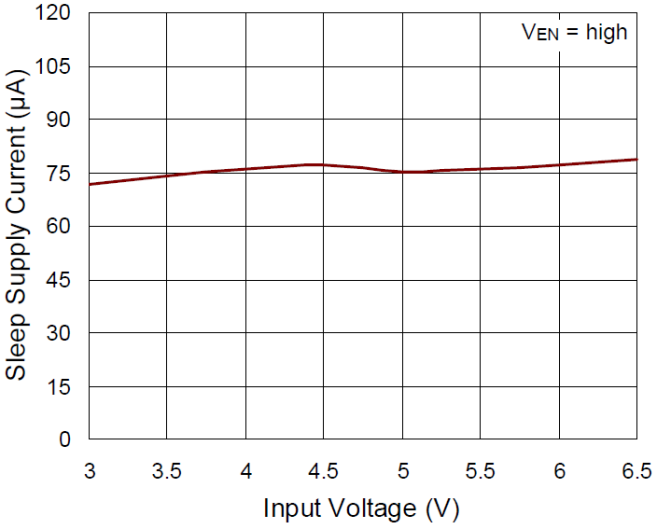
Shutdown Supply Current vs. Input Voltage



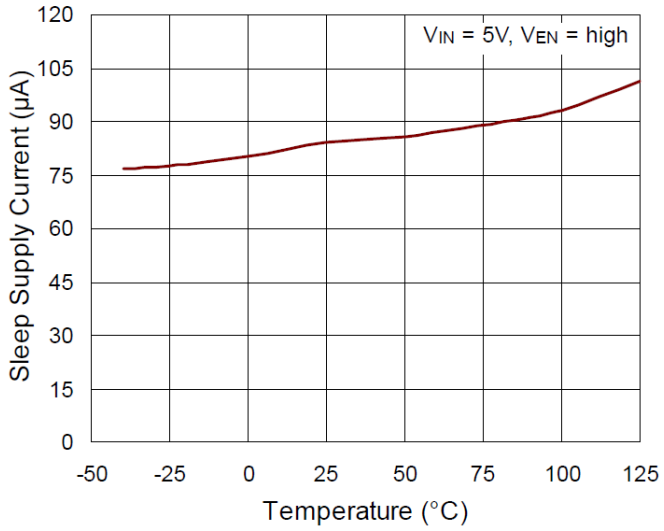
Shutdown Supply Current vs. Temperature



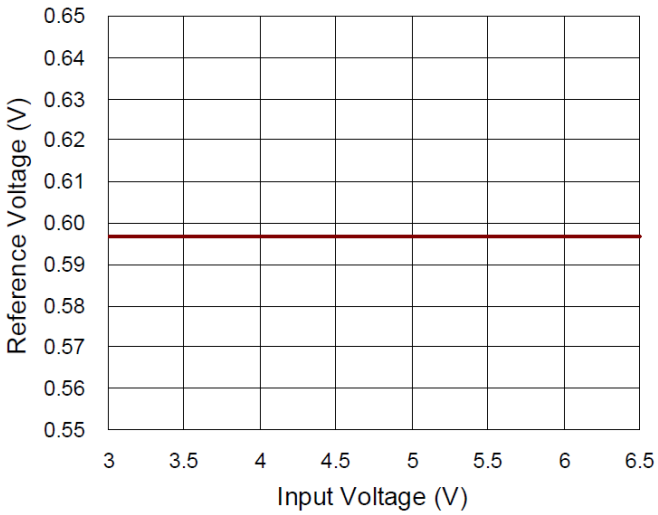
Sleep Supply Current vs. Input Voltage



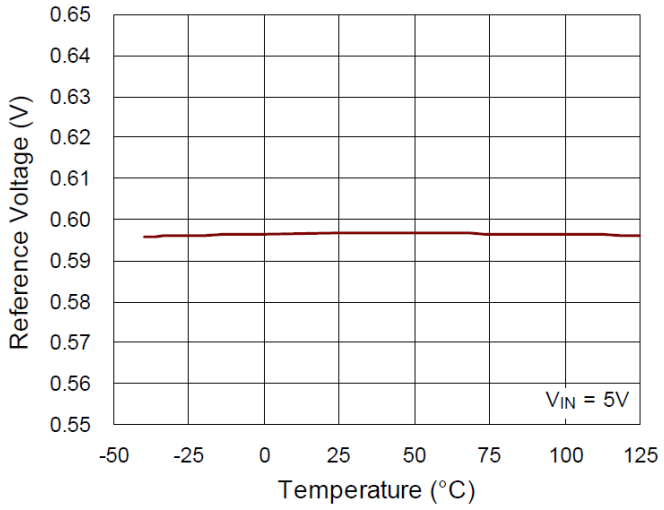
Sleep Supply Current vs. Temperature



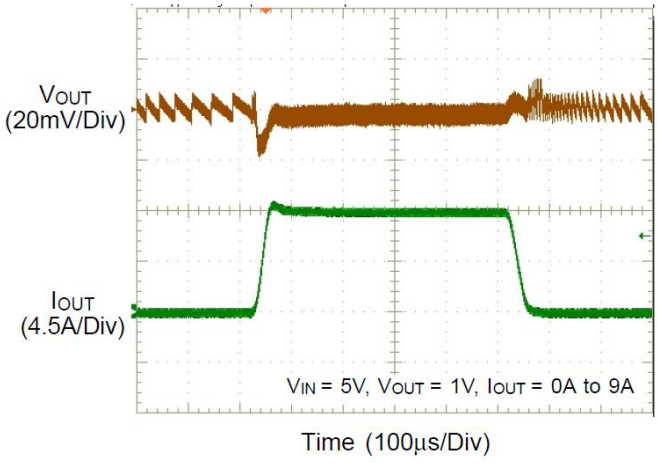
Reference Voltage vs. Input Voltage



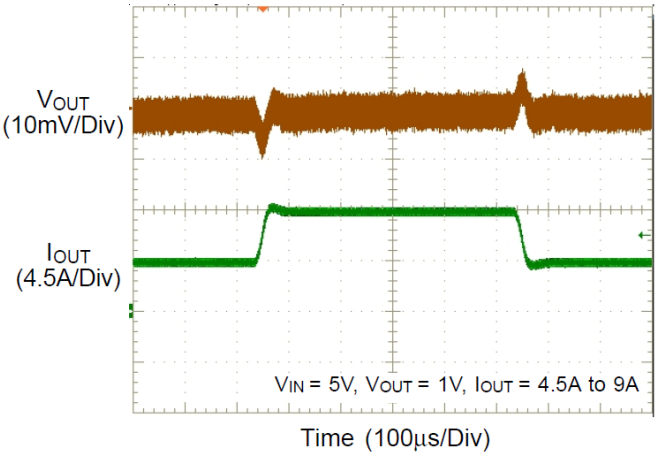
Reference Voltage vs. Temperature



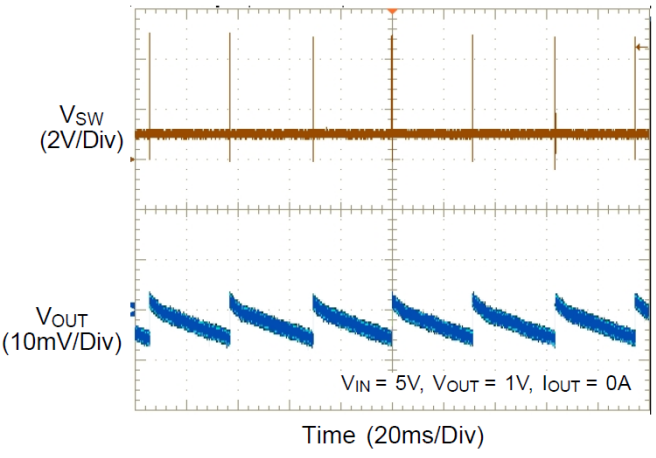
Load Transient Response



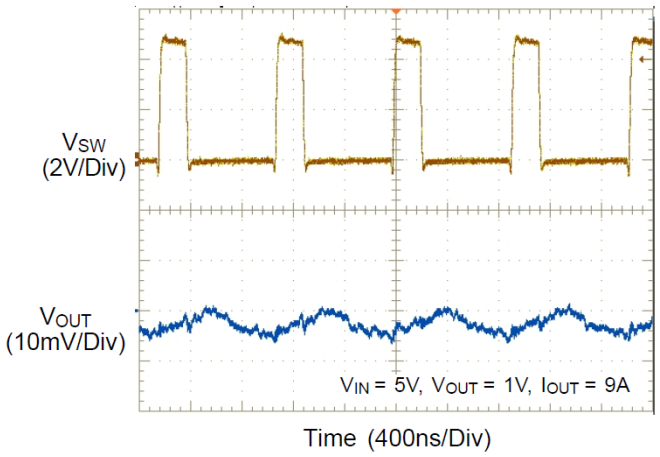
Load Transient Response



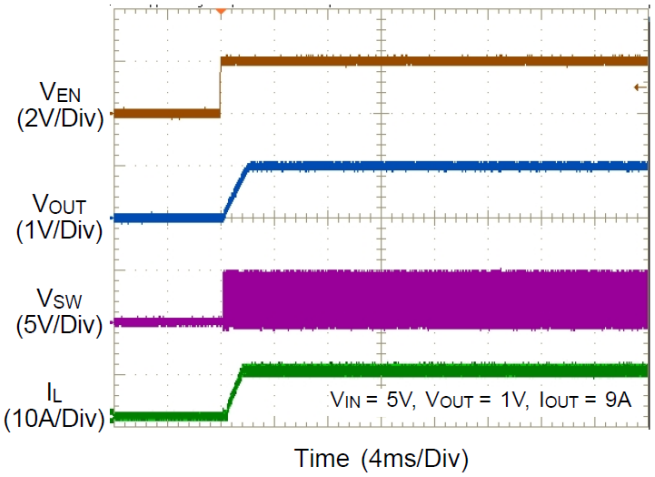
Output Ripple Voltage



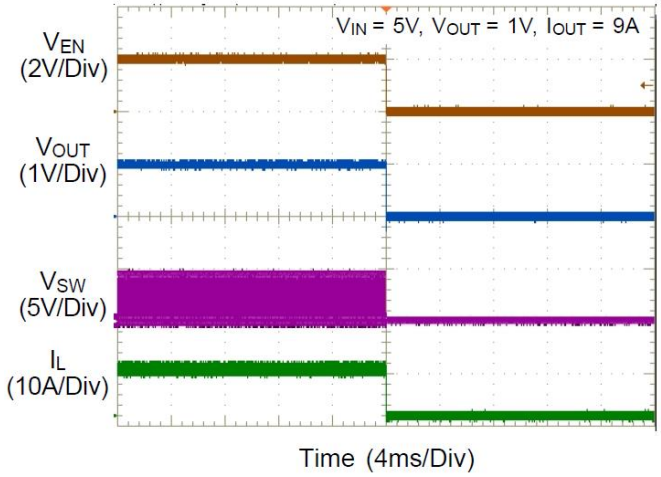
Output Ripple Voltage



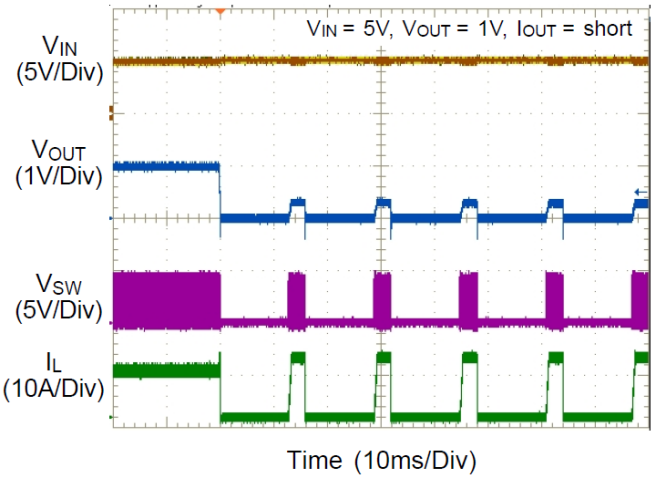
Power On from EN



Power Off from EN



UVP Short (Hiccup Mode)



Functional Register Table

Table 1. The RT5759 Register Summary

Name	Type	Register Reset	Address Offset
MANUFACTURER_ID	R	0x82h	0x00
FREQ_REG	RW	0x0Ah	0x01
SEL_REG	RW	0x28h	0x02
DCDCCTRL_REG	RW	0x0Ah	0x03
STATUS_REG	R	0x00h	0x04
DCDC_SET	RW	0xA4h	0x05

Table 2. MANUFACTURER_ID

Address: 0x00
Description: Manufacturer ID number register

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MANUFACTURER_ID							
Reset Value	0x82h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7:0	MANUFACTURER_ID	Return the manufacturer ID number: 0x82h

Table 3. FREQ_REG

Address: 0x01
Description: Configure register
Set VID change slew rate and PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved				TSTEP		FREQ	
Reset Value	0	0	0	0	1	0	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Bits	Name	Description
7:4	Reserved	Reserved bit
3:2	TSTEP	TSTEP[3:2] = 00b: 20mV/μs TSTEP[3:2] = 01b: 15mV/μs TSTEP[3:2] = 10b: 10mV/μs (default) TSTEP[3:2] = 11b: 5mV/μs
1:0	FREQ	FREQ[1:0] = 00b, 0.6MHz FREQ[1:0] = 01b, 0.8MHz FREQ[1:0] = 10b, 1.0MHz (default) FREQ[1:0] = 11b, 1.5MHz

Table 4. SEL_REG

Address: 0x02 **Description:** VID setting register								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL						
Reset Value	0	0	1	0	1	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6:0	SEL	Supply voltage: SEL[6:0] = 0000000b: 0.6V SEL[6:0] = 0000001b: 0.61V SEL[6:0] = 0000010b: 0.62V SEL[6:0] = 0000011b: 0.63V SEL[6:0] = 0000100b: 0.64V SEL[6:0] = 0000101b: 0.65V SEL[6:0] = 0000110b: 0.66V SEL[6:0] = 0000111b: 0.67V SEL[6:0] = 0001000b: 0.68V SEL[6:0] = 0001001b: 0.69V SEL[6:0] = 0001010b: 0.7V SEL[6:0] = 0001011b: 0.71V SEL[6:0] = 0001100b: 0.72V SEL[6:0] = 0001101b: 0.73V SEL[6:0] = 0001110b: 0.74V SEL[6:0] = 0001111b: 0.75V SEL[6:0] = 0010000b: 0.76V SEL[6:0] = 0010001b: 0.77V SEL[6:0] = 0010010b: 0.78V SEL[6:0] = 0010011b: 0.79V SEL[6:0] = 0010100b: 0.8V SEL[6:0] = 0010101b: 0.81V SEL[6:0] = 0010110b: 0.82V SEL[6:0] = 0010111b: 0.83V SEL[6:0] = 0011000b: 0.84V SEL[6:0] = 0011001b: 0.85V SEL[6:0] = 0011010b: 0.86V SEL[6:0] = 0011011b: 0.87V SEL[6:0] = 0011100b: 0.88V SEL[6:0] = 0011101b: 0.89V SEL[6:0] = 0011110b: 0.9V SEL[6:0] = 0011111b: 0.91V SEL[6:0] = 0100000b: 0.92V SEL[6:0] = 0100001b: 0.93V SEL[6:0] = 0100010b: 0.94V SEL[6:0] = 0100011b: 0.95V SEL[6:0] = 0100100b: 0.96V SEL[6:0] = 0100101b: 0.97V SEL[6:0] = 0100110b: 0.98V SEL[6:0] = 0100111b: 0.99V

Bits	Name	Description
7	Reserved	Reserved bit
6:0	SEL	Supply voltage: SEL[6:0] = 0101000b: 1V SEL[6:0] = 0101001b: 1.01V SEL[6:0] = 0101010b: 1.02V SEL[6:0] = 0101011b: 1.03V SEL[6:0] = 0101100b: 1.04V SEL[6:0] = 0101101b: 1.05V SEL[6:0] = 0101110b: 1.06V SEL[6:0] = 0101111b: 1.07V SEL[6:0] = 0110000b: 1.08V SEL[6:0] = 0110001b: 1.09V SEL[6:0] = 0110010b: 1.1V SEL[6:0] = 0110011b: 1.11V SEL[6:0] = 0110100b: 1.12V SEL[6:0] = 0110101b: 1.13V SEL[6:0] = 0110110b: 1.14V SEL[6:0] = 0110111b: 1.15V SEL[6:0] = 0111000b: 1.16V SEL[6:0] = 0111001b: 1.17V SEL[6:0] = 0111010b: 1.18V SEL[6:0] = 0111011b: 1.19V SEL[6:0] = 0111100b: 1.2V SEL[6:0] = 0111101b: 1.21V SEL[6:0] = 0111110b: 1.22V SEL[6:0] = 0111111b: 1.23V SEL[6:0] = 1000000b: 1.24V SEL[6:0] = 1000001b: 1.25V SEL[6:0] = 1000010b: 1.26V SEL[6:0] = 1000011b: 1.27V SEL[6:0] = 1000100b: 1.28V SEL[6:0] = 1000101b: 1.29V SEL[6:0] = 1000110b: 1.3V SEL[6:0] = 1000111b: 1.31V SEL[6:0] = 1001000b: 1.32V SEL[6:0] = 1001001b: 1.33V SEL[6:0] = 1001010b: 1.34V SEL[6:0] = 1001011b: 1.35V SEL[6:0] = 1001100b: 1.36V SEL[6:0] = 1001101b: 1.37V SEL[6:0] = 1001110b: 1.38V SEL[6:0] = 1001111b: 1.39V SEL[6:0] = 1010000b: 1.4V SEL[6:0] = 1010001b: 1.41V SEL[6:0] = 1010010b: 1.42V SEL[6:0] = 1010011b: 1.43V SEL[6:0] = 1010100b: 1.44V SEL[6:0] = 1010101b: 1.45V SEL[6:0] = 1010110b: 1.46V SEL[6:0] = 1010111b: 1.47V SEL[6:0] = 1011000b: 1.48V SEL[6:0] = 1011001b: 1.49V SEL[6:0] = 1011010b to 1111111b: 1.5V

Table 5. DCDCCTRL_REG

Address: 0x03 **Description:** Discharge resistor enable, PSKIP Mode/PWM control, and internal enable registers								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved				Discharge	PWM	Enable	Reserved
Reset Value	0	0	0	0	1	0	1	0
Read/Write	R	R	R	R	R/W	R/W	R/W	R

Bits	**Name**	**Description**
7 :4	Reserved	Reserved bit
3	Discharge	Discharge[3] = 0b: disable discharge resistor (Only OT/UVLO = 1, disable discharge; EN = 0, enable discharge) Discharge[3] = 1b: enable discharge resistor (default)
2	PWM	PWM[2] = 0b: PSKIP mode (default) PWM[2] = 1b: Force PWM
1	Enable	Enable[1] = 0b: disable Enable[1] = 1b: enable (default)
0	Reserved	Reserved bit

Table 6. STATUS_REG

Address: 0x04 **Description:** Indication of status								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved						OT	UV
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
7:2	Reserved	Reserved bit
1	OT	OT[1] = 0b: no OT OT[1] = 1b: OT
0	UV	UV[0] = 0b: no UV UV[0] = 1b: UV

Table 7. DCDC_SET

Address: 0x05
Description: current limit, thermal shutdown threshold, PGOOD enable delay time, VID

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OCSET		OTSET		PGDSET		VIDSET	Reserved
Reset Value	1	0	1	0	0	1	0	0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R

Bits	Name	Description
7:6	OCSET	OCSET[7:6] = 00b: no POC OCSET[7:6] = 01b: 9.8A OCSET[7:6] = 10b: 10.8A (default) OCSET[7:6] = 11b: 11.8A
5:4	OTSET	OTSET[5:4] = 00b: no OT OTSET[5:4] = 01b: 140°C OTSET[5:4] = 10b: 150°C (default) OTSET[5:4] = 11b: 170°C
3:2	PGDSET	PGDSET[3:2] = 00b: PGOOD enable delay time = 0μs PGDSET[3:2] = 01b: PGOOD enable delay time = 10μs (default) PGDSET[3:2] = 10b: PGOOD enable delay time = 20μs PGDSET[3:2] = 11b: PGOOD enable delay time = 40μs
1	VIDSET	VIDSET[1] = 0b: VID VIDSET[1] = 1b: No VID, SEL[6:0] = 0000000b : 0.6V with TSTEP[3:2] = 11b : 5mV/μs
0	Reserved	Reserved bit

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

Inductor Selection

When designing the output stage of the synchronous buck converter, it is recommended to start with the inductor. However, it may require several iterations because the exact inductor value is generally flexible and is optimized for low cost, small form factor, and high overall performance of the converter. Further, inductors vary with manufacturers in both material and value, and typically have a tolerance of ±20%.

Three key inductor parameters to be specified for operation with the device are inductance (L), inductor saturation current (I_{SAT}), and DC resistance (DCR), which affects performance of the output stage. An inductor with lower DCR is recommended for applications of higher peak current or load current, and it can improve system performance. Lower inductor values are beneficial to the system in physical size, cost, DCR, and transient response, but they will cause higher inductor peak current and output voltage ripple to decrease system efficiency. Conversely, higher inductor values can increase system efficiency at the expense of larger physical size, slower transient response due to the longer response time of the inductor. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) of about 20% to 50% of the desired full output load current. To meet the inductor current ripple (ΔI_L) requirements, a minimum inductance must be chosen and the approximate inductance can be calculated by the selected input voltage, output voltage, switching frequency (f_{SW}), and inductor current ripple (ΔI_L), as below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current (I_{L_PEAK}) can be calculated, as below:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

$$I_{L\_VALLEY} = I_{OUT\_MAX} - \frac{1}{2}\Delta I_L$$

where I_{OUT_MAX} is the maximum rated output current or the required peak current.

The inductor must be selected to have a saturation current and thermal rating which exceed the required peak inductor current I_{L_PEAK}. For a robust design to maintain control of inductor current in overload or short-circuit conditions, some applications may desire inductor saturation current rating up to the switch current limits of the device. However, the built-in output under-voltage protection (UVP) feature makes this unnecessary for most applications.

For best efficiency, a low-loss inductor having the lowest possible DCR that still fits in the allotted dimensions will be chosen. Ferrite cores are often the best choice. However, a shielded inductor, possibly larger or more expensive, will probably give fewer EMI and other noise problems.

The following design example is illustrated to walk through the steps to apply the equations defined above. The RT5759's Typical Application Circuit for output voltage of 1V at maximum output current of 9A and an input voltage of 5V with inductor current ripple of 1.8A (i.e., 20%, in the recommended range of 20% to 50%, of the maximum rated output current) is taken as the design example. The approximate minimum inductor value can first be calculated as below:

$$L = \frac{1 \times (5-1)}{5 \times 1MHz \times 1.8A} = 0.44\mu H$$

where f_{SW} is 1MHz. The inductor current ripple will be set at 1.8A, as long as the calculated inductance of 0.44μH is used. However, the inductor of the exact

inductance value may not be readily available, and therefore an inductor of a nearby value will be chosen. In this case, 0.47μH inductance is available and actually used in the Typical Application Circuit. The actual inductor current ripple (ΔI_L) and required peak inductor current (I_{L_PEAK}) can be calculated as below:

$$\Delta I_L = \frac{1\times(5-1)}{5\times 1MHz\times 0.47\mu H} = 1.702A$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L = 9 + \frac{1.702}{2} = 9.851A$$

For the 0.47μH inductance value, the inductor saturation current and thermal rating should exceed 9.851A.

Input Capacitor Selection

Input capacitors are needed to smooth out the RMS ripple current (I_{RMS}) imposed by the switching currents and drawn from the input power source, by reducing the ripple voltage amplitude seen at the input of the converters. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It is also important to consider the ripple current capabilities of capacitors.

The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation:

$$I_{RMS} = I_{OUT}\times\frac{V_{OUT}}{V_{IN}}\times\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. Furthermore, for a single phase buck converter, the duty cycle is approximately the ratio of output voltage to input voltage. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. The maximum I_{RMS}, as I_{RMS} (Max), can be approximated as 0.5 x I_{OUT_MAX}, where I_{OUT_MAX} is the maximum rated output current. Besides, the variation of the capacitance value with temperature, DC bias voltage, switching frequency, and allowable peal-to-peak ripple voltage that reflects back to the input, also need to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases; also, higher switching frequency allows the use of input capacitors of smaller capacitance values.

Ceramic capacitors are most commonly used to be placed right at the input of the converter to reduce ripple voltage amplitude because only ceramic capacitors have extremely low ESR which is required to reduce the ripple voltage. Note that the capacitors need to be placed as close as to the input pins as possible for highest effectiveness. Ceramic capacitors are preferred also due to their low cost, small size, high RMS current ratings, robust inrush surge current capabilities, and low parasitic inductance, which helps reduce the high-frequency ringing on the input supply.

However, care must be taken when ceramic capacitors are used at the input, and the input power is supplied by a wall adapter, connected through a long and thin wire. When a load step occurs at the output, a sudden inrush current will surge through the long inductive wire, which can induce ringing at the device's power input and potentially cause a very large voltage spike at the VIN pin to damage the device. For applications where the input power is located far from the device input, it may be required that the low-ESR ceramic input capacitors be placed in parallel with a bulk capacitor of other types, such as tantalum, electrolytic, or polymer, to dampen the voltage ringing and overshoot at the input, caused by the long input power path and input ceramic capacitor.

It is suggested to choose capacitors with higher temperature ratings than required. Several ceramic capacitors may be parallel to meet application requirements, such as the RMS current, size, and height. The Typical Application Circuit can use one 10μF and one high-frequency- noise-filtering 0.1μF low-ESR ceramic capacitors at the input.

Output Capacitor Selection

Output capacitance affects the output voltage of the converter, the response time of the output feedback loop, and the requirements for output voltage sag and soar. The sag occurs after a sudden load step current applied, and the soar occurs after a sudden load

removal. Increasing the output capacitance reduces the output voltage ripple and output sag and soar, while it increases the response time that the output voltage feedback loop takes to respond to step loads, Therefore, there is a tradeoff between output capacitance and output response. It is recommended to choose a minimum output capacitance to meet the output voltage requirements of the converter, and have a quick transient response to step loads.

The ESR of the output capacitor affects the damping of the output filter and the transient response. In general, low-ESR capacitors are good choices due to their excellent capability in energy storage and transient performance. The RT5759, therefore, is specially optimized for ceramic capacitors. Consider also DC bias and aging effects while selecting the output capacitor.

Output Voltage Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage ΔV_{P-P}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below:

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RT5759's Typical Application Circuit for output voltage of 1V, and actual inductor current ripple (ΔI_L) of 1.702A, using four paralleled 22μF ceramic capacitors with ESR of about 5mΩ as output capacitors, the two output ripple components are as below:

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR} = 1.702A \times 5m\Omega = 8.51mV$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} = \frac{1.702A}{8 \times 88\mu F \times 1MHz} = 2.42mV$$

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C} = 10.93mV$$

Output Transient Undershoot and Overshoot

In addition to the output voltage ripple at the switching frequency, the output capacitor and its ESR also affect output voltage sag, which is undershoot on a positive load step, and output voltage soar, which is overshoot on a negative load step. With the built-in ACOT® architecture, the IC can have very fast transient responses to the load steps and small output transients.

However, the combination of a small ceramic output capacitor (that is, of little capacitance) and a low output voltage (that is, only little charge stored in the output capacitor), used in low-duty-cycle applications (which require high inductance to get reasonable ripple currents for high input voltages), causes an increase in the size of voltage variations (i.e., sag/soar) in response to very quick load changes. Typically, the load changes slowly, compared with the IC's switching frequency. However, for present-day applications, more and more digital blocks may exhibit nearly instantaneous large transient load changes. Therefore, in the following section, how to calculate the worst-case voltage swings in response to very fast load steps will be explained in details.

Both of the output transient undershoot and overshoot have two components: a voltage step caused by the output capacitor's ESR, and a voltage sag or soar due to the finite output capacitance and the inductor current slew rate. The following formulas can be used to check if the ESR is low enough (which is usually not a problem with ceramic capacitors) and if the output capacitance is large enough to prevent excessive sag or soar on very fast load steps, with the chosen inductor value.

The voltage step (ΔV_{OUT_ESR}) caused by the ESR is a function of the load step (ΔI_{OUT}) and the ESR (R_{ESR}) of the output capacitor, described as below:

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \times R_{ESR}$$

The voltage amplitude (ΔV_{OUT_SAG}) of the capacitive sag is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), the input-to-output voltage differential, and the maximum duty cycle (D_{MAX}). And the maximum duty cycle during a fast transient can be determined by the on-time (t_{ON}) and the minimum off-time (t_{OFF_MIN}) since the ACOT® control scheme will ramp the current during on-times, which are spaced apart by a minimum off-time, that is, as fast as allowed. The approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage can be calculated according to the following equations:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

Note the actual on-time will be slightly larger than the calculated one as the IC will automatically adapt to compensate the internal voltage drops, such as the voltage across high-side switch due to on-resistance. However, both of these can be neglected since the on-time increase can compensate for the voltage drops. The output voltage sag (ΔV_{OUT_SAG}) can then be calculated as below:

$$\Delta V_{OUT\_SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The voltage amplitude of the capacitive soar is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), and the output voltage (V_{OUT}). And the output voltage soar (ΔV_{OUT_SOAR}) can be calculated as below:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with normal voltage rating, can be connected to the input supply V_{IN}, through a 100kΩ resistor. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 2, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 3. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 4.

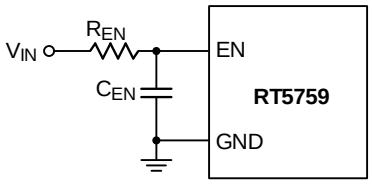


Figure 2. Enable Timing Control

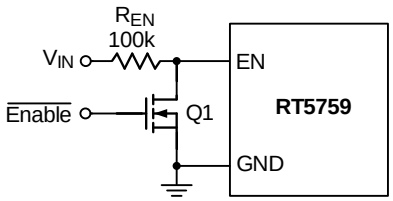


Figure 3. Logic Control for the EN Pin

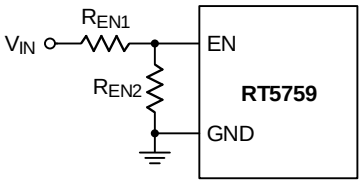


Figure 4. Resistive Divider for Under-Voltage Lockout Threshold Setting

Output Voltage Setting

The output voltage setting of rail is controlled through I^2C by the 0x02 VID setting register. Output voltage can be set via register of 0x02[6:0] from 0.6V to 1.5V and the default voltage is 1V.

External Bootstrap Diode

A bootstrap capacitor of 0.1μF low-ESR ceramic capacitor is connected between the BOOT and SW pins to supply the high-side gate driver. It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54.

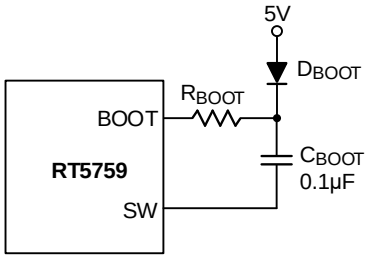


Figure 5. External Bootstrap Diode

Resistor at BOOT Pin

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 47Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 6, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

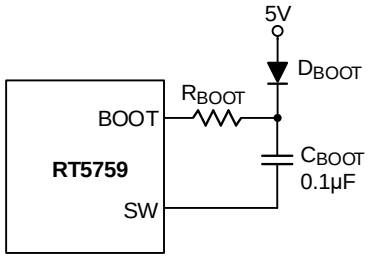


Figure 6. External Bootstrap Diode and Resistor at the BOOT Pin

Soft-Start Function

The RT5759 provides an adjustable soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The soft-start time is defined as the output voltage rising time from 10% to 90% of settled level and can be programmed by the external soft-start capacitor C_{SS} between the SS and GND pins. An internal current source I_{SS} (typically, 10μA) charges the capacitor to build a soft-start ramp voltage. The FB voltage will track the ramp voltage of SS pin during soft-start. The typical soft-start time can be calculated as follows:

Soft-Start Time

$$t_{SS}\ (ms) = \frac{C_{SS}(nF) \times V_{OUT} \times 0.8}{I_{SS}(\mu A)} = \frac{C_{SS}\ (nF) \times V_{OUT} \times 0.8}{10(\mu A)}$$

If we leave SS pin unconnected, the soft-start time has its minimum value. We only connect an external soft-start capacitor C_{SS} when we need longer soft-start time.

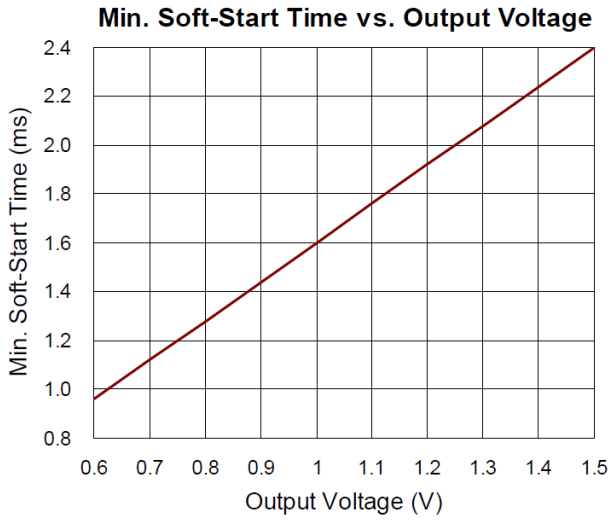


Figure 7. Min. Soft-Start Time vs. Output Voltage

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When VFB drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 110% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{TH_PGHL}, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND.

Output Under-Voltage Protection (Hiccup Mode)

The RT5759 includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 70% of the internal reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period of time, the RT5759 will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

Low-Side Current-Limit Protection

The RT5759 features a cycle-by-cycle valley-type current limit protection, measuring the inductor current through the synchronous rectifier (low-side switch). The inductor current level is determined by measuring the low-side switch voltage between the SW pin and GND, which is proportional to the switch current, during the low-side on-time. For greater accuracy, temperature compensation is added to the voltage sensing. Once the current rises above the low-side switch valley current limit (I_{LIM}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. This function can prevent the average output current from greatly exceeding the guaranteed low-side current limit value.

If the output load current exceeds the available inductor current (clamped by the above-mentioned low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

I^2C Interface

A general-purpose serial interface to control and monitor the configuration registers is provided in the RT5759 and the I^2C slave address of the RT5759 would be 0x60 (A0 pin = High Level), 0x62 (A0 pin floating), or 0x63 (A0 pin = Low Level). This I^2C interface supports standard slave mode (100kbps) and fast mode (400kbps). Multiple bytes reading or writing over the I^2C interface could also be done through the RT5759 (see Figure 8).

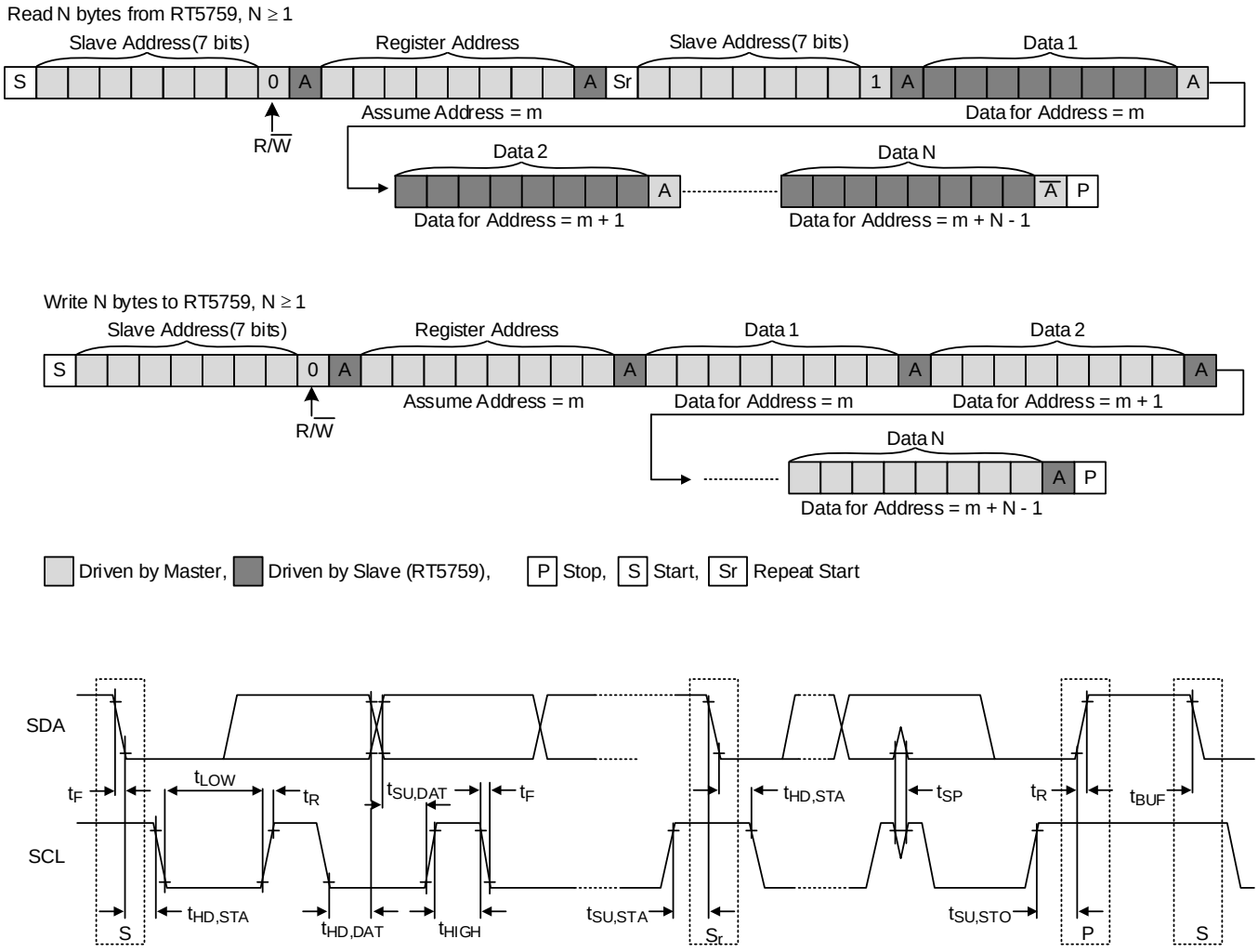


Figure 8. I²C Read/Write Stream and Timing Diagram

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-13L 3x3 (FC) package, the thermal resistance, θ_{JA}, is 38.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (30°C/W) = 2.62W for a UQFN-13L 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

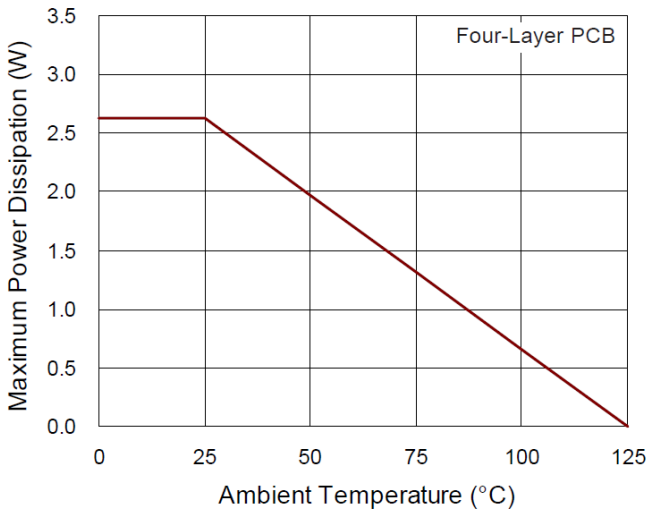


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

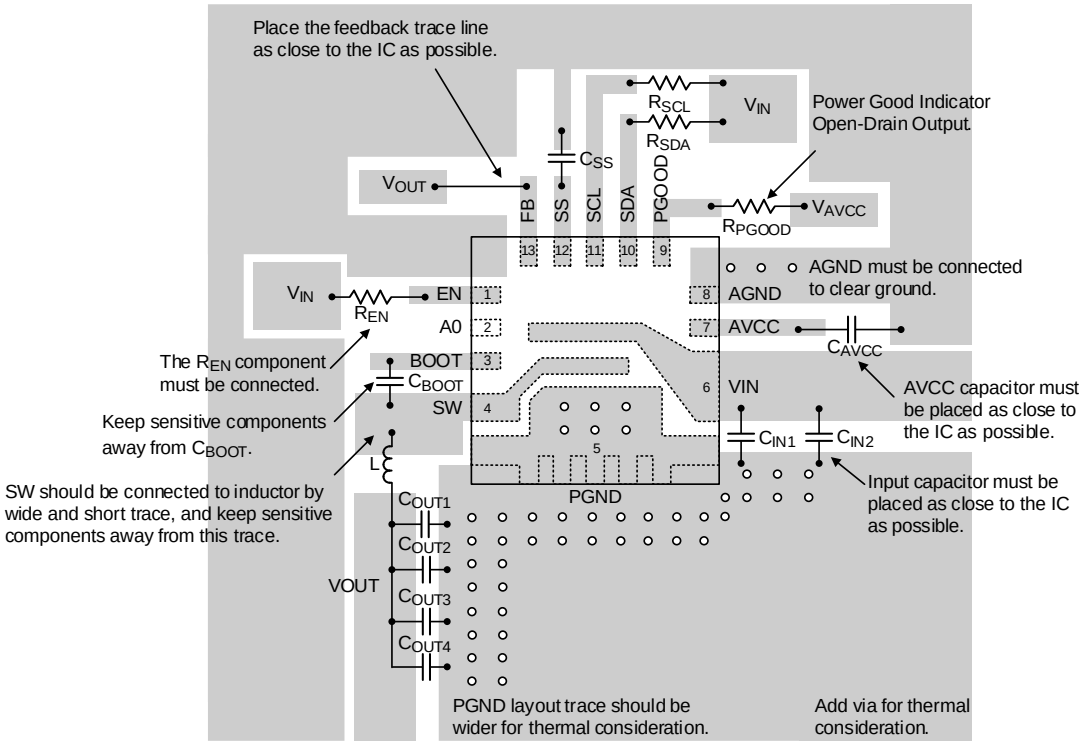


Figure 10. PCB Layout Guide (Top Layer)

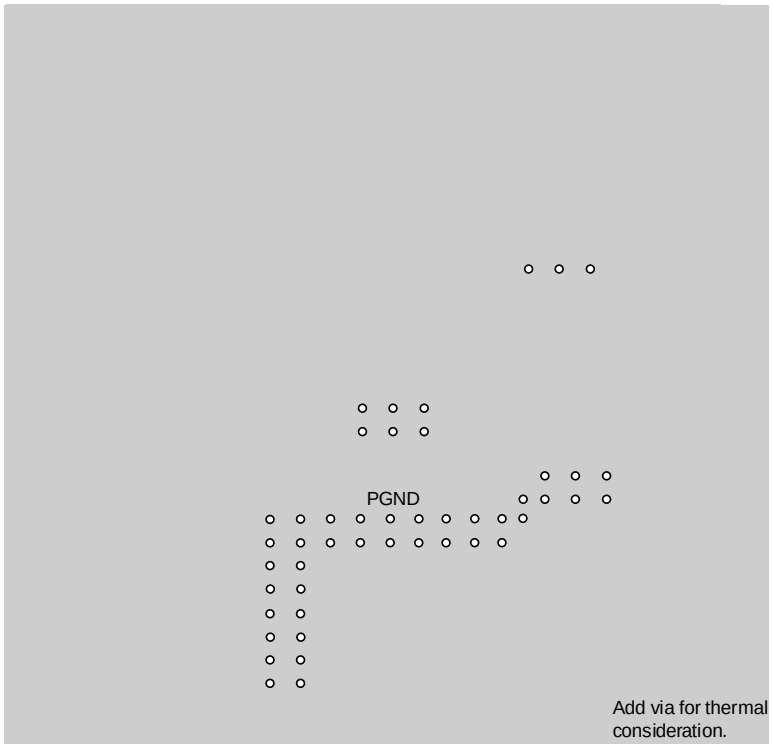


Figure 11. PCB Layout Guide (Bottom Layer)

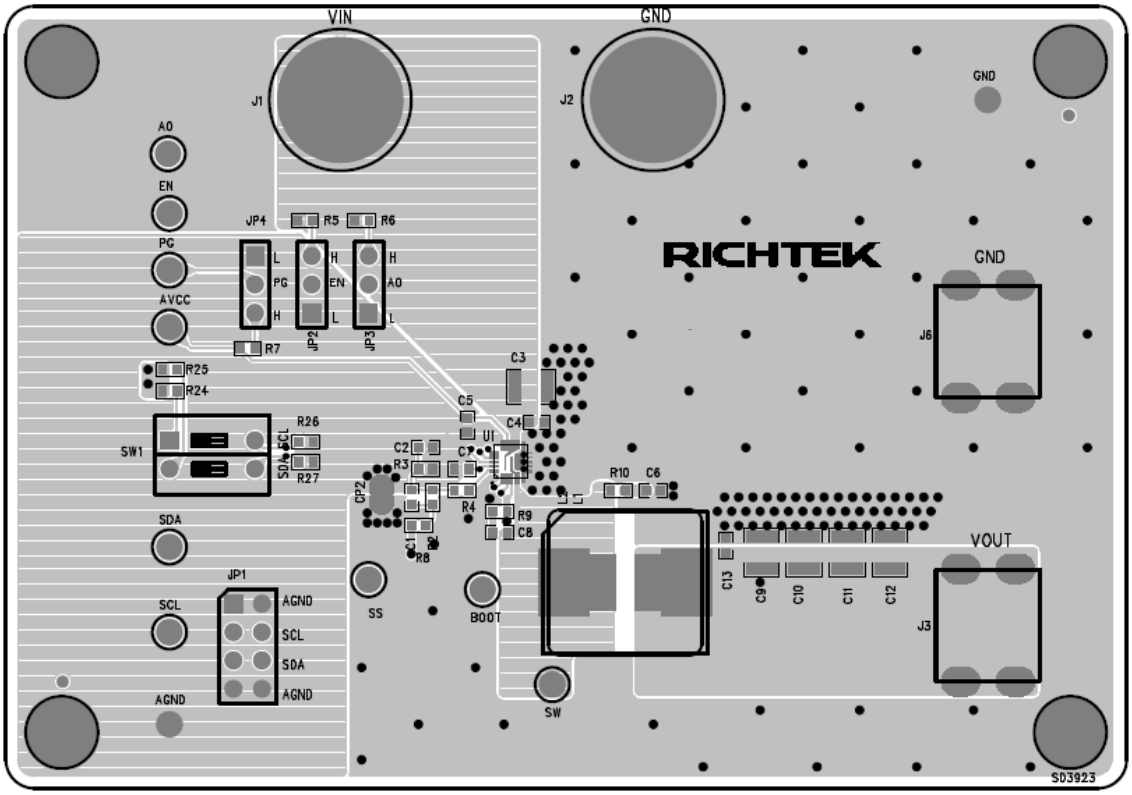


Figure 12. Top Layer PCB Layout

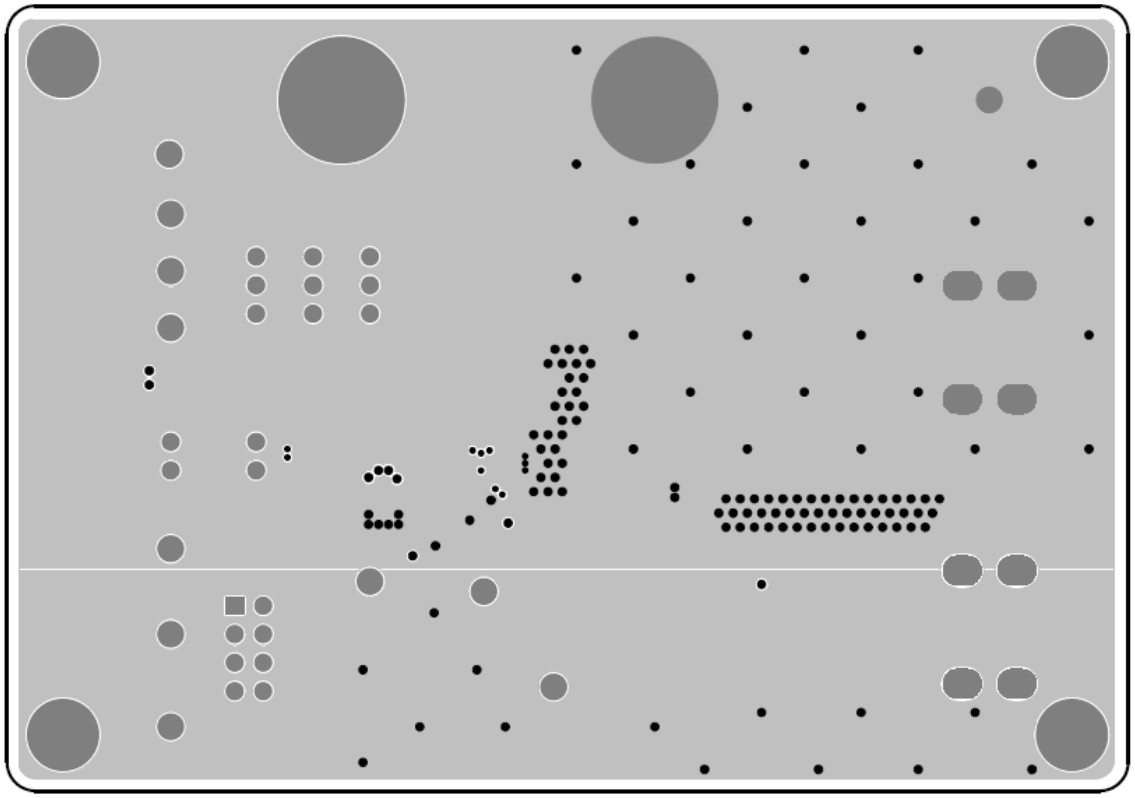


Figure 13. Inner Layer 1 PCB Layout

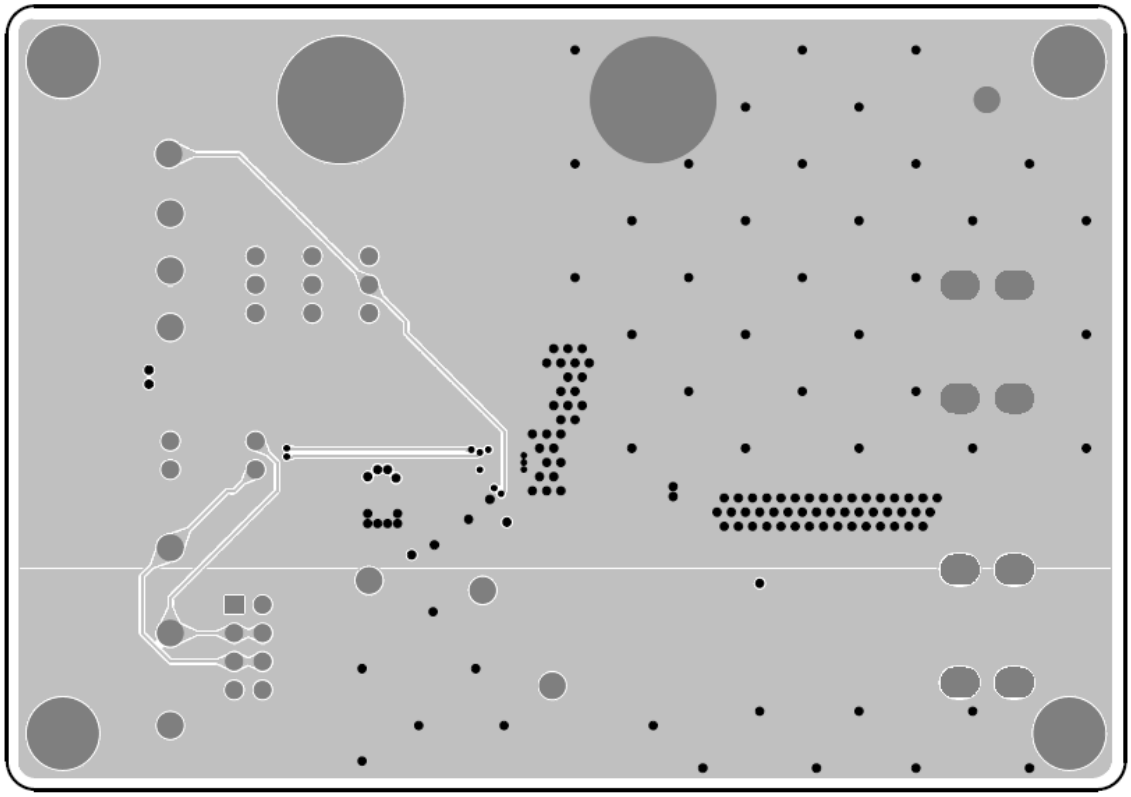


Figure 14. Inner Layer 2 PCB Layout

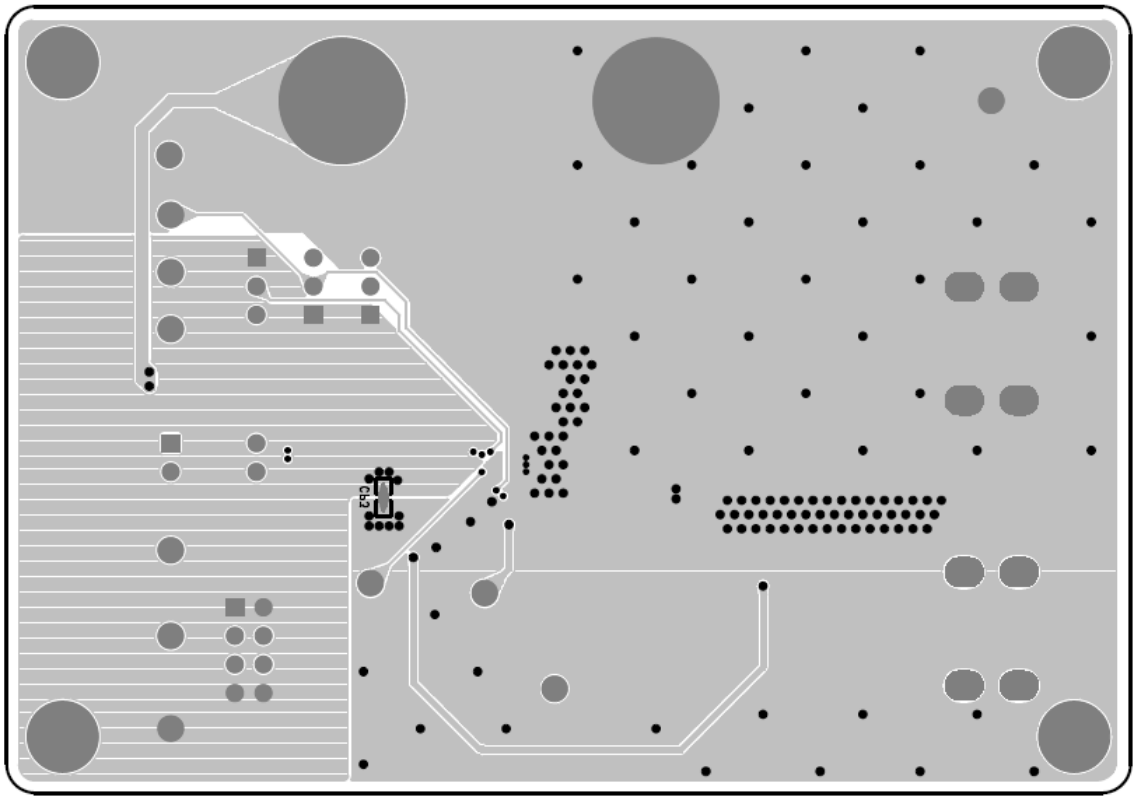


Figure 15. Bottom Layer PCB Layout

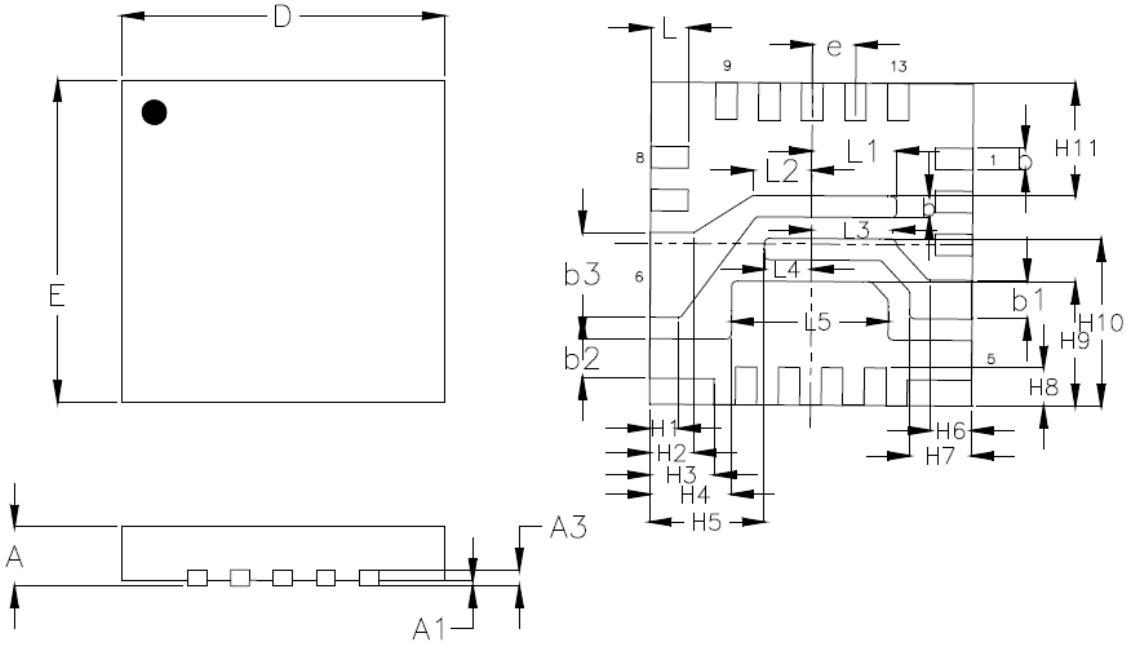
Suggested Inductors for Typical Application Circuit

Component Supplier	Part No.	Inductance (μH)	DCR (mΩ)	Dimensions (mm)
WE	744314047	0.47	1.35	7.0 x 7.0 x 5.0

Recommended Component Selection for Typical Application Circuit

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM32ER71H106KA12L	10	1210
TDK	C3225X5R1E226MT	22	1210
MURATA	GRM188R61C475KAAJ	4.7	0603

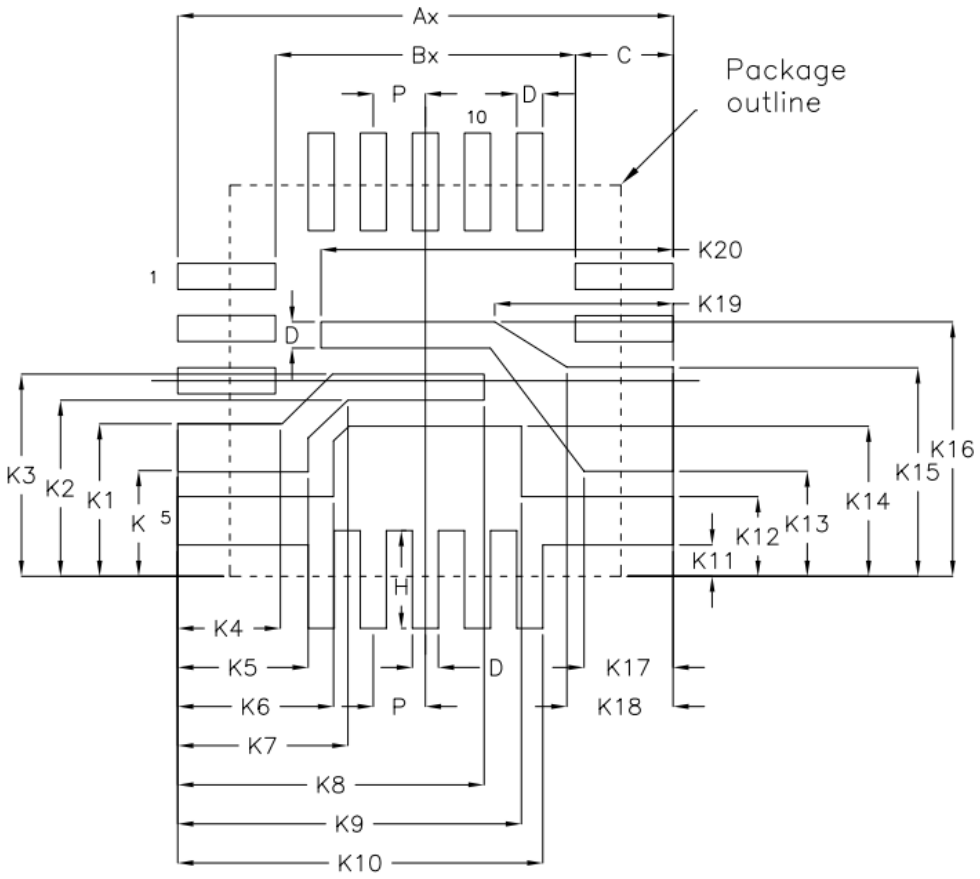
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
b	0.150	0.250	0.006	0.010
b1	0.310	0.410	0.012	0.016
b2	0.320	0.420	0.013	0.017
b3	0.740	0.840	0.029	0.033
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
e	0.400		0.016	
L	0.300	0.400	0.012	0.016
L1	0.740	0.840	0.029	0.033
L2	0.480	0.580	0.019	0.023
L3	0.740	0.840	0.029	0.033
L4	0.390	0.490	0.015	0.019
L5	1.410	1.510	0.056	0.059
H1	0.280		0.011	
H2	0.420		0.017	
H3	0.600		0.024	
H4	0.750		0.030	
H5	1.050		0.041	
H6	0.400		0.016	
H7	0.600		0.024	
H8	0.350		0.014	
H9	1.150		0.045	
H10	1.550		0.061	
H11	1.050		0.041	

U-Type 13L QFN 3x3 (FC) Package

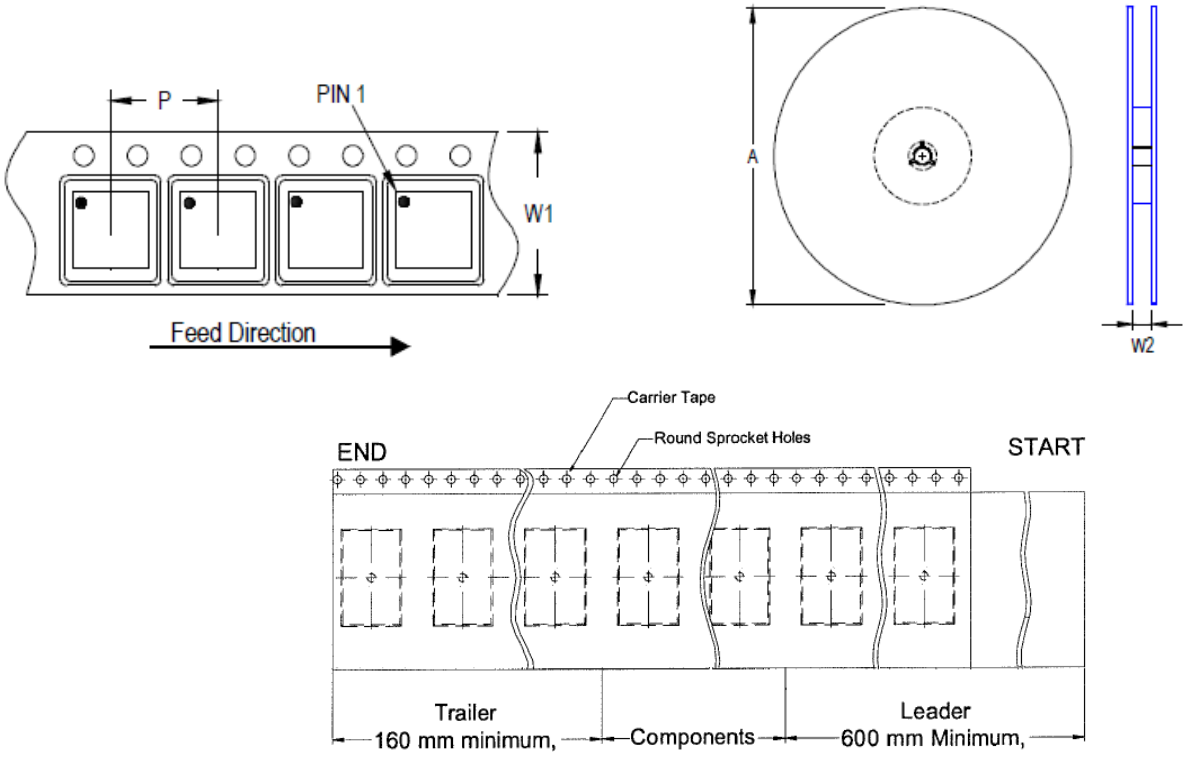
Footprint Information



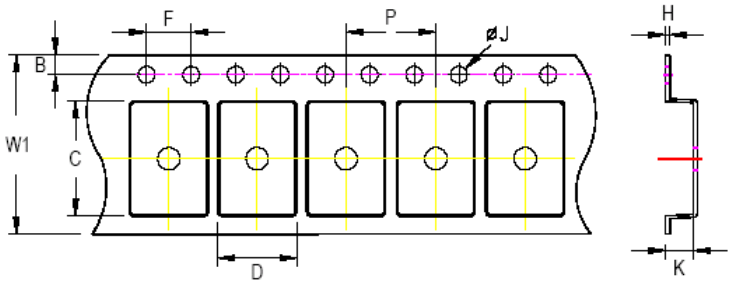
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
UQFN3x3-13(FC)	13	P	Ax	Bx	C	D	K	K1	K2	K3	±0.05
		0.40	3.80	2.30	0.75	0.20	0.80	1.17	1.35	1.55	
		K4	K5	K6	K7	K8	K9	K10	K11	K12	
		0.80	1.00	1.20	1.30	2.35	2.65	2.80	0.24	0.61	
		K13	K14	K15	K16	K17	K18	K19	K20	H	
		0.80	1.15	1.60	1.95	0.68	0.82	1.37	2.70	0.75	

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
01	2024/2/19	Modify	General Description on P1 Ordering Information on P1 Functional Pin Description on P3 Application Information on P19, 22, 27 Packing Information on P33, 34, 35