Low Quiescent, High-Efficiency 3A ACOT® Synchronous Buck-Boost Converter with Power-Good Indicator

1 General Description

The RT6167 is a high-efficiency, single-inductor and ACOT® (Advanced Constant On-Time) monolithic synchronous buck-boost converter that can deliver up to 3A output current from an input voltage range of 2.2V to 5.5V. It can regulate the digitally programmable output voltage from 2.025V to 5.2V, making it suitable for a wide range of input supply applications, regardless of whether the input voltage is lower, higher than, or equal to the output voltage. The ACOT® control architecture features outstanding line/load transient response, seamless transition between buck and boost modes, and provides stable operation with small ceramic output capacitors without the need for complicated external compensation.

Users can select two output voltages of the 128 types in Table 2, when the VSEL pin is in the low and high states, respectively. The RT6167 employs specific switching methods by adjusting the MODE pin. When set to low, the RT6167 operates in automatic PFM (Pulse Frequency Modulation) mode, featuring a low quiescent current design with a typical value of 2μA, maintaining high efficiency during light load operation. At higher loads, the device automatically switches to a 2.2MHz fixed frequency control, effectively smoothing out the switching ripple voltage with small package filtering elements. The integrated low $R_{DS(ON)}$ power MOSFETs exhibit excellent efficiency under heavy load conditions. In shutdown mode, the supply current is typically 0.1μA, contributing to reduce power consumption. If acoustic noise is a concern or a fixed frequency operation is required, the RT6167 can operate in either Ultra-Sonic Mode (USM) or Forced PWM Mode (FPWM). The RT6167 is available in a small WL-CSP-15B 1.4x2.3 (BSC) package.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

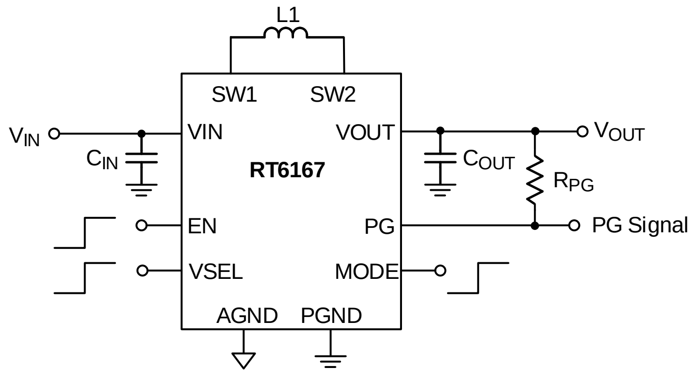
2 Features

- **Automatic Seamless Mode Transition with Real Buck, Buck-Boost, and Boost Operation**
- **Input Voltage Range: 2.2V to 5.5V**
- **Output Voltage Range: 2.025V to 5.2V (25mV/Steps)**
- **Maximum Continuous Output Current**
  - **Up to 2.5A for $V_{IN} \geq$ 2.5V, V_{OUT} = 3.3V**
  - **Up to 3A for $V_{IN} \geq$ 3V, V_{OUT} = 3.3V**
  - **Up to 2A for $V_{IN} \geq$ 3V, V_{OUT} = 5V**
- **Up to 95% Efficiency (V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{LOAD} = 1A)**
- **2μA Non-Switching Low Quiescent Current**
- **Automatic PFM Mode, Ultra-Sonic Mode, and Forced PWM Mode Selection**
- **Power Status Indication via PG Pin**
- **Protections: OCP, UVLO, OTP, OVP, UVP**
- **15-Ball WL-CSP Package**

3 Applications

- Smartphones and Tablets
- Portable Devices
- Wearable Devices
- System Pre-Regulators
- Point-of-Load Regulators
- Wifi Modules
- USB VCONN Supplies
- TWS Earbud Chargers

4 Simplified Application Circuit



5 Ordering Information

RT6167□-□□□

- **Packing**
  A: Standard
- **Operation Mode**
  (Refer to Operation Mode Table)
- **Output Voltage Combination**
  A: VSEL = L: 3.3V
  VSEL = H: 3.35V
- **Package Type**(1)
  P: WL-CSP-15B 1.4x2.3 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5.1 Operation Mode Table

Code	Mode = L	Mode = H
A	PFM	Ultra-Sonic
B	PFM	FPWM

6 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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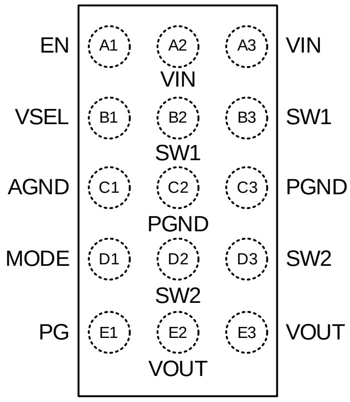
7 Pin Configuration

(TOP VIEW)

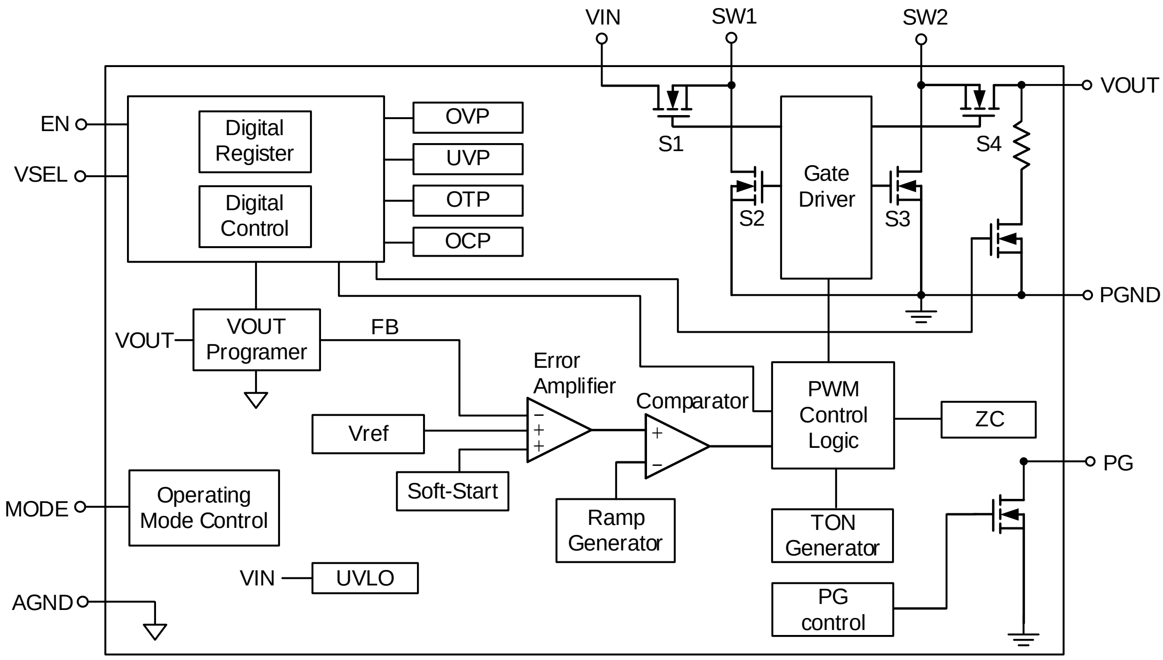


WL-CSP-15B 1.4x2.3 (BSC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
A2, A3	VIN	Power input. The input voltage range is from 2.2V to 5.5V after the soft-start is finished. Connect input capacitors between this pin and PGND with minimal path. It is recommended to use a 10μF/6.3V/X5R/0402 and a 0.1μF/6.3V/X5R/0201 ceramic capacitor.
B1	VSEL	Refer to Table 2 to determine the two application voltages. When this pin is tied to ground, VOUT is set to the first selected voltage; when tied to logic high, VOUT is set to the second selected voltage. Do not leave this pin floating.
B2, B3	SW1	Switching node 1. Connect to the inductor.
C1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
C2, C3	PGND	Power ground. The low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
D1	MODE	Mode select pin. Pull low for PFM operation and pull high for ultra-sonic mode operation (RT6167P-AA) or forced PWM mode operation (RT6167P-AB). Do not float this pin.
D2, D3	SW2	Switching node 2. Connect to the inductor.
E1	PG	Power-Good indication output. PG will be pulled low to ground if any internal protection is triggered. High indicates power is OK, while low indicates a fault. PG also goes low when EN is set to low.
E2, E3	VOUT	Output voltage sense through this pin. Connect to the output capacitor. It is recommended to use two 22μF/10V/X5R/0603 ceramic capacitors.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Input Voltage, VIN ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to 6.2V
- Switch Node Voltage, SW1, SW2

  DC ---------- –0.3V to 6V

  AC (<50ns) ---------- –5V to 8.5V
- Other I/O Pins Voltages (EN, VSEL, MODE, PG) ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-15B 1.4x2.3 (BSC) ---------- 1.88W
- Package Thermal Resistance (Note 3)

  WL-CSP-15B 1.4x2.3 (BSC), θ_{JA} ---------- 53°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-9 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Input Voltage, V_{IN} ---------- 2.2V to 5.5V
- Output Voltage, V_{OUT} ---------- 2.025V to 5.2V
- Output Current, I_{OUT} ---------- 0A to 3A
- Input Capacitance, C_{IN} (Note 6) ---------- 5μF (Minimum)
- Output Capacitance, C_{OUT} (Note 6) ---------- 16μF (Minimum)
- Inductance, L ---------- 0.39μH to 0.56μH
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. Effective capacitance after DC bias effects have been considered.

12 Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 3.3V, T_A = T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		2.2	--	5.5	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	2.11	2.14	2.19	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	2.02	2.05	2.08	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	90	--	mV
Quiescent Current (Switching Current)	I_{Q_SW}	V_{EN} = V_{IN} = 3.6V, I_{OUT} = 0A	--	3	6	μA
Quiescent Current (Non-Switching Current)	I_{Q_NSW}	V_{EN} = V_{IN} = 3.6V, I_{OUT} = 0A, not switching	--	2	4	
Shutdown Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 3.6V	--	0.1	1	μA
High-Level Input Current	I_{IH}	MODE = VSEL = 1.8V, no pull-up resistor	--	--	0.1	μA
Low-Level Input Current	I_{IL}	MODE = VSEL = 0V, no pull-up resistor	--	--	0.1	μA
Input Bias Current	I_{BIAS}	V_{EN} = 0 to 5.5V	--	--	0.1	μA
High-Side MOSFET Leakage Current	I_{LK_H}	V_{EN} = 0V, V_{SW} = 0V	--	1	--	μA
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	25	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	38	--	mΩ
Output Discharge Resistor	R_{DISCHG}	V_{EN} = 0V	--	5	--	Ω
EN Input Voltage Rising threshold	$V_{EN\ R}$	V_{IN} = 2.2V to 5.5V	1.2	--	--	V
EN Input Voltage Falling threshold	V_{EN_F}	V_{IN} = 2.2V to 5.5V	--	--	0.4	
Input Voltage Logic-High (MODE, VSEL)	V_{IH}		1.2	--	--	V
Input Voltage Logic-Low (MODE, VSEL)	V_{IL}		--	--	0.4	
Output Voltage Range	V_{OUT_RANGE}		2.025	--	5.2	V
Output Voltage Accuracy (PFM)	$V_{OUT\_ACC\_PFM}$	Auto PFM operation	–1	--	3	%
Output Voltage Accuracy (USM)	$V_{OUT\_ACC\_USM}$	Ultra-Sonic operation	–1	--	3	
Output Voltage Accuracy (FPWM)	$V_{OUT\_ACC\_FPWM}$	Forced PWM operation	–1	--	1	
Line Regulation	V_{LINE_REG}	(Note 7)	--	0.5	--	%
Load Regulation	V_{LOAD_REG}	(Note 7)	--	0.5	--	%
Maximum Continuous Output Current	I_{MAX}	V_{IN} ≥ 2.5V, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF (Note 8)	2.5	--	--	A
		V_{IN} ≥ 3V, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF (Note 8)	3	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Side Switch (Peak) Current Limit	I_{LIM_H}	V_{IN} = 3.6V, V_{OUT} = 3.3V	4.5	5	5.5	A
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	V_{IN} = 3.6V, V_{OUT} = 3.3V	4	4.5	5	A
PFM to PWM Threshold Inductor Current	$I_{L\_T\_PFM}$	V_{IN} = 3.6V, V_{OUT} = 3.3V, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	0.3	--	A
Efficiency	η	V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, auto PFM operation	--	95	--	%
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, ultra-sonic operation	--	94	--	
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, forced PWM operation	--	94	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, auto PFM operation	--	94	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, ultra-sonic operation	--	95	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, forced PWM operation	--	95	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Ripple Voltage	V_{OUT_RIPPLE}	V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, auto PFM operation (Note 7)	--	50	--	mV
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, ultra-sonic operation (Note 7)	--	20	--	
		V_{IN} = 3.3V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, forced PWM operation (Note 7)	--	20	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, auto PFM operation (Note 7)	--	25	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, ultra-sonic operation (Note 7)	--	10	--	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1A, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF, forced PWM operation (Note 7)	--	10	--	
Load Transient Response	V_{LOAD_TR}	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.05A to 1A, t_R = t_F = 1μs (Note 7)	–100	--	100	mV
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0.05A to 0.5A, t_R = t_F = 1μs (Note 7)	–50	--	50	
Line Transient Response	V_{LINE_TR}	I_{OUT} = 1A, V_{IN} = 3V to 3.6V to 3V, t_R = t_F = 10μs (Note 7)	–50	--	50	mV
Switching Frequency	f_{SW}	Boost or Buck operation	--	2.2	--	MHz
Switching Frequency at Ultra-Sonic Mode	f_{SW_USC}	I_{OUT} = 1mA	30	--	--	kHz
Switching Frequency Range	f_{SW_RANGE}	Forced PWM operation, I_{OUT} = 100mA	0.5	--	3	MHz
Minimum On-Time	t_{ON_MIN}		20	--	60	ns
Minimum Off-Time	t_{OFF_MIN}		20	--	60	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Rising Time Turn-On Rise Time	t_R	Output voltage ramp to output voltage 95%, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	300	1000	μs
Enable Delay Time	t_{DLY_EN}	Enable pin logic-high to output voltage ramp, L = 0.47μH, C_{IN} = 10μF, C_{OUT} = 44μF	--	220	300	μs
VSEL Delay Time	t_{DLY_VSEL}	Delay between rising edge of V_{SEL} and start of VOUT ramp	--	30	--	μs
PG Low-Level Output Voltage	V_{OL_PG}	Current into the PG pin is equal to 5mA	--	--	200	mV
PG Input Leakage Current	I_{LEAK_PG}	1.8V applied on the PG pin	--	--	1	μA
PG Delay Time	$t_{DLY\_F\_PG\_UVLO}$	PG falling	--	15	--	μs
	$t_{DLY\_F\_PG\_UV}$	PG falling	--	40	--	
	$t_{DLY\_F\_PG\_OV}$	PG falling	--	40	--	
	$t_{DLY\_F\_PG\_OC}$	PG falling	--	50	--	
	$t_{DLY\_F\_PG\_OT}$	PG falling	--	150	--	
PG Rising Threshold	V_{PG_R}	VOUT rising, referenced to VOUT nominal	--	95	--	%
PG Falling Threshold	V_{PG_F}	VOUT falling, referenced to VOUT nominal	--	90	--	%
Over-Temperature Protection Threshold	T_{OTP}	(Note 7)	140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	(Note 7)	--	20	--	°C

Note 7. Guaranteed by design.

Note 8. The device can sustain the maximum recommended output current. Users must verify that the thermal performance of the end application can support the maximum output current.

13 Typical Application Circuit

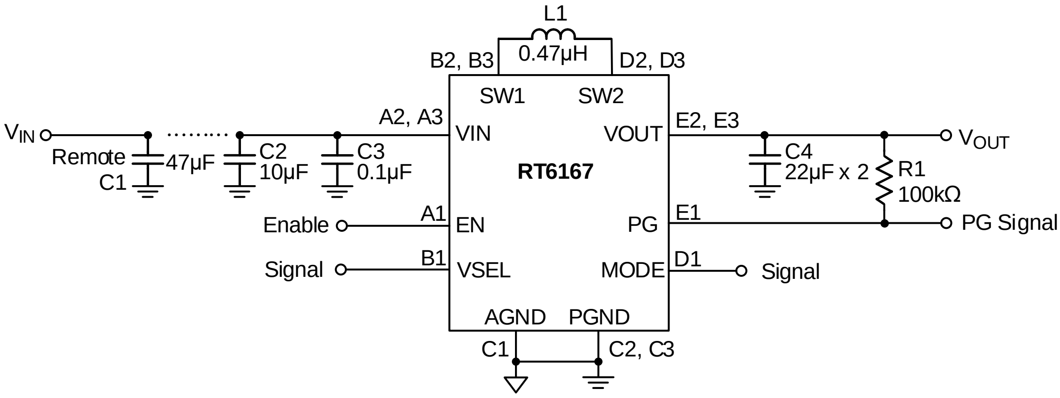


Table 1. Recommended Components Information (Note 9)

Reference	Part Number	Description	Package	Manufacturer
C1 (Note 10)	GRM32ER61C476KE15	47μF/16V/X5R	1210	Murata
C2	GRM155R60J106ME15	10μF/6.3V/X5R	0402	Murata
C3 (Note 11)	GRM033R60J104KE19	0.1μF/6.3V/X5R	0201	Murata
C4	GRM188R61A226ME15	22μF/10V/X5R	0603	Murata
L1	XFL4015-471MEC	0.47μH	4x4x1.5mm	Coilcraft
R1	Resistor, 1%, 100mW	100kΩ	0603	Standard

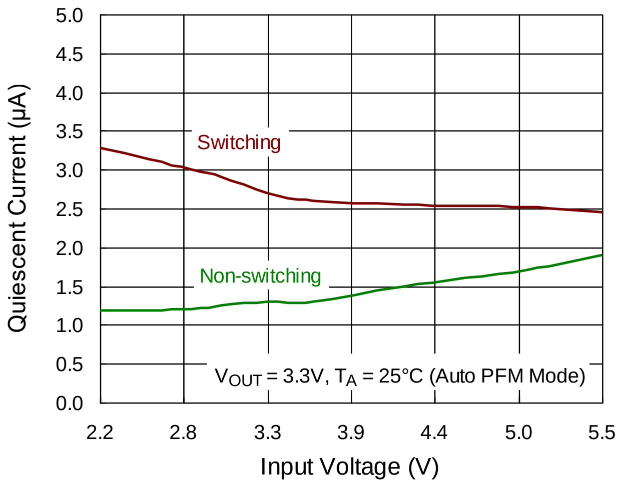
Note 9. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effects, such as DC bias.

Note 10. The decoupling capacitor C1 is a remote C_{OUT} capacitor. C1 is optional. The device is designed to operate with a DC supply voltage in the range of 2.2V to 5.5V. If the input supply is more than a few centimeters from the device, it is recommended to add some bulk capacitance to the ceramic bypass capacitors. A 47μF electrolytic capacitor is a typical selection for the bulk capacitance.

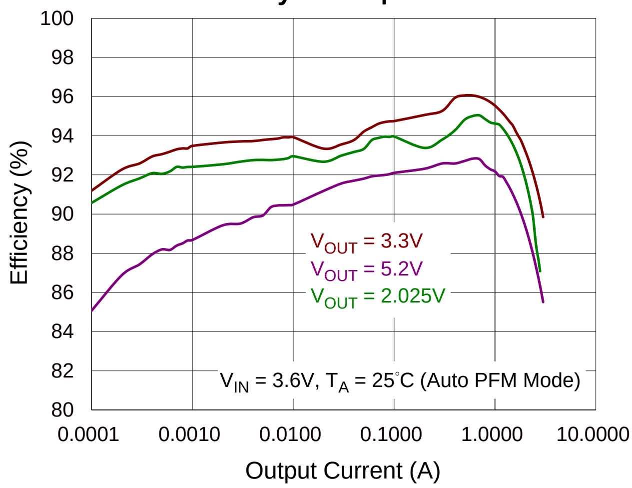
Note 11. The decoupling capacitor C3 is recommended to reduce any high-frequency components on the VIN bus. C3 is optional and used to filter any high-frequency components on the VIN bus.

14 Typical Operating Characteristics

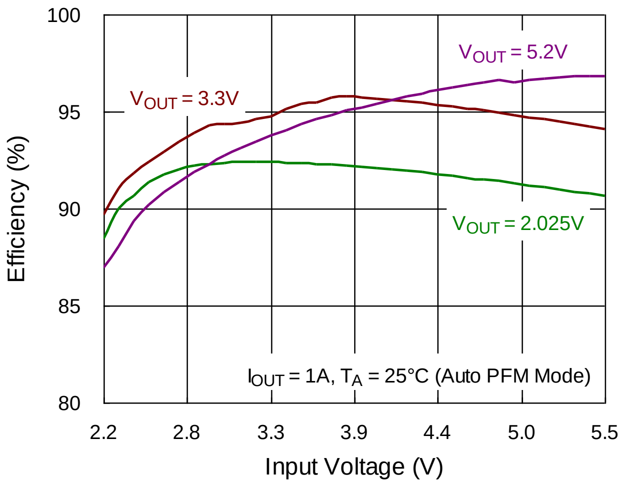
Quiescent Current vs. Input Voltage



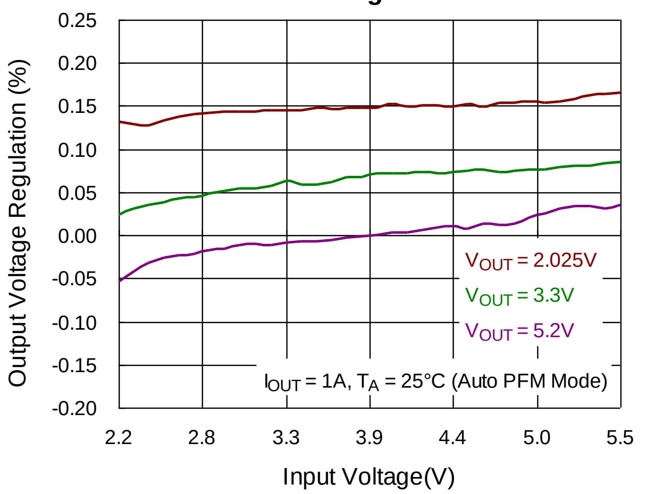
Efficiency vs. Output Current



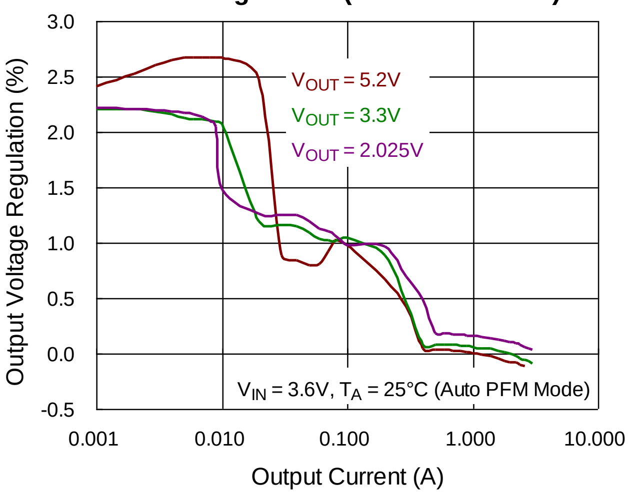
Efficiency vs. Input Voltage



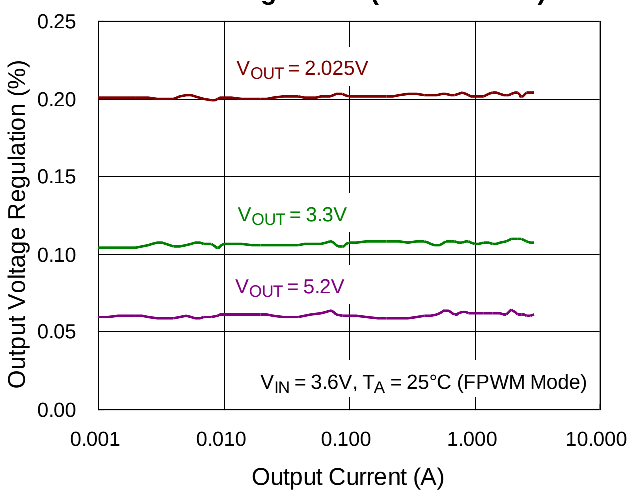
Line Regulation



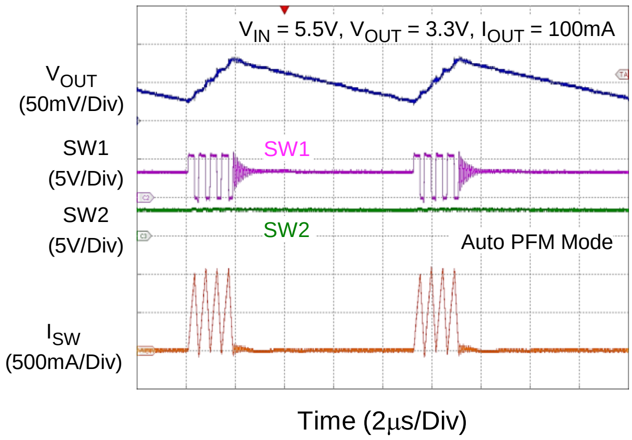
Load Regulation (Auto PFM Mode)



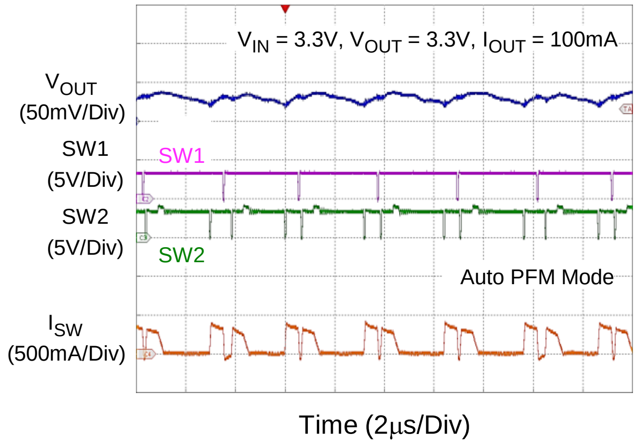
Load Regulation (FPWM Mode)



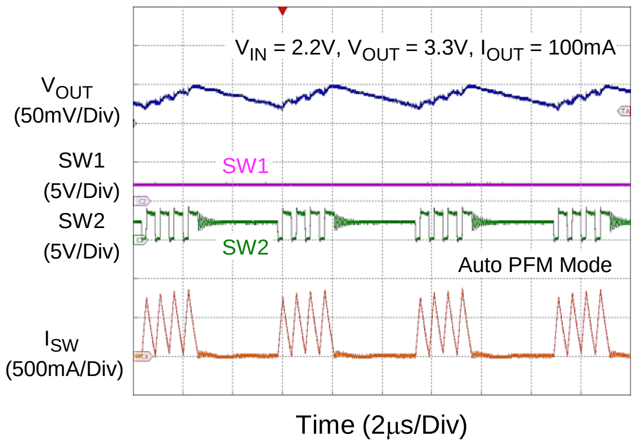
PFM Switching Waveforms (Buck Operation)



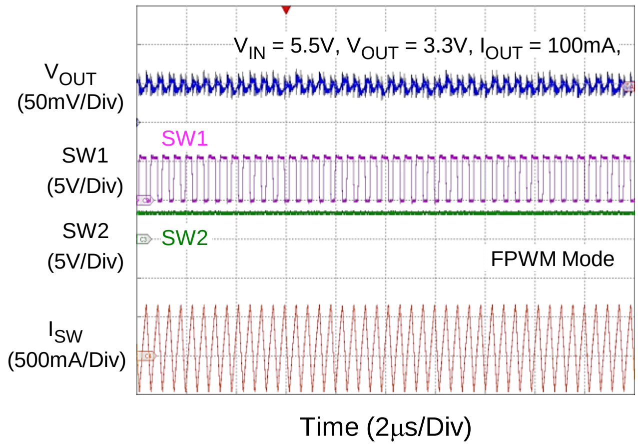
PFM Switching Waveforms (Buck-Boost Operation)



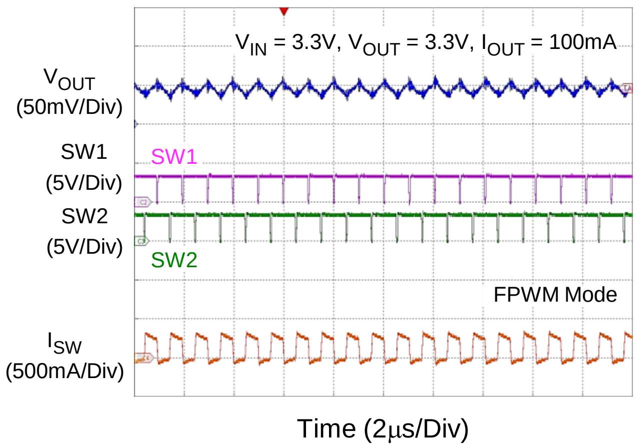
PFM Switching Waveforms (Boost Operation)



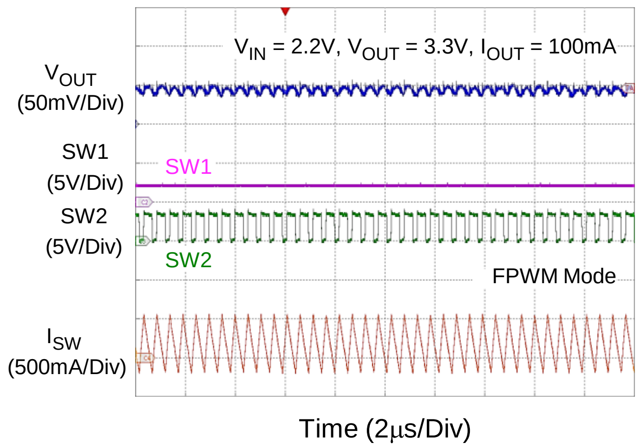
PWM Switching Waveforms (Buck Operation)



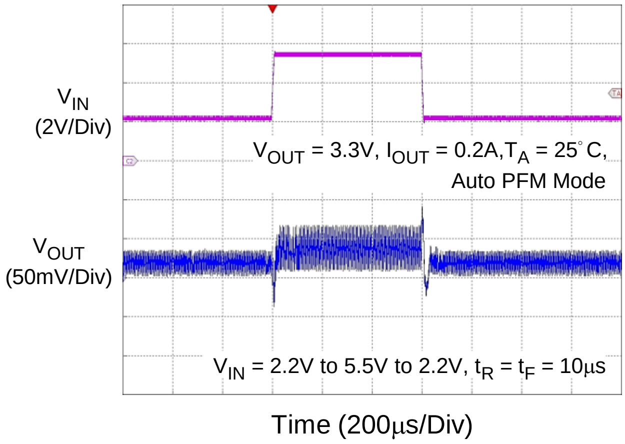
PWM Switching Waveforms (Buck-Boost Operation)



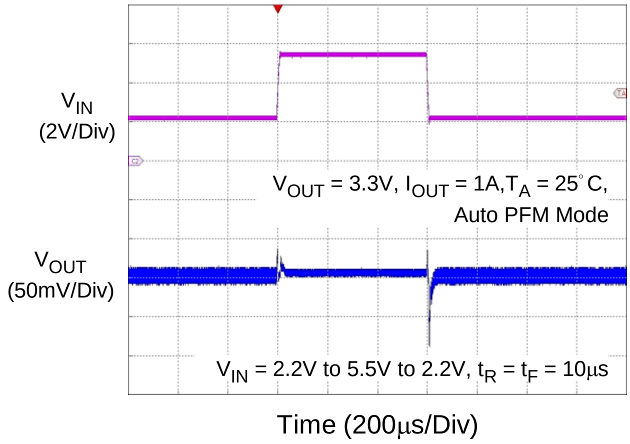
PWM Switching Waveforms (Boost Operation)



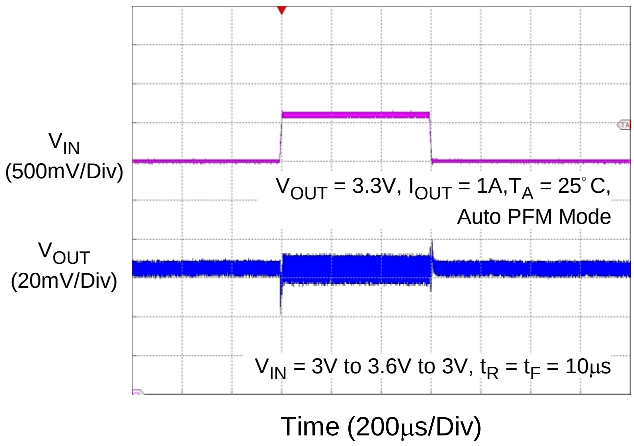
Line Transient Response (Light Load)



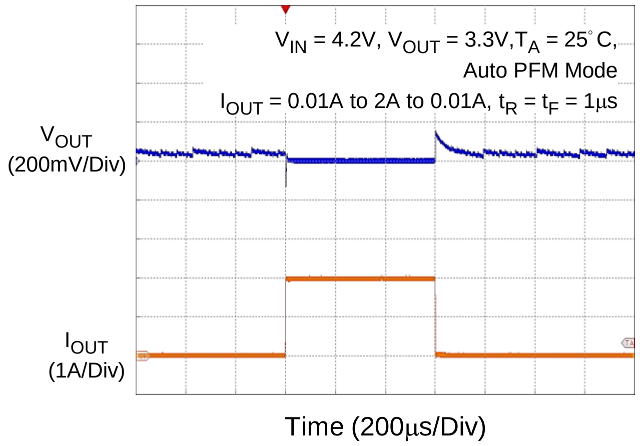
Line Transient Response (Heavy Load)



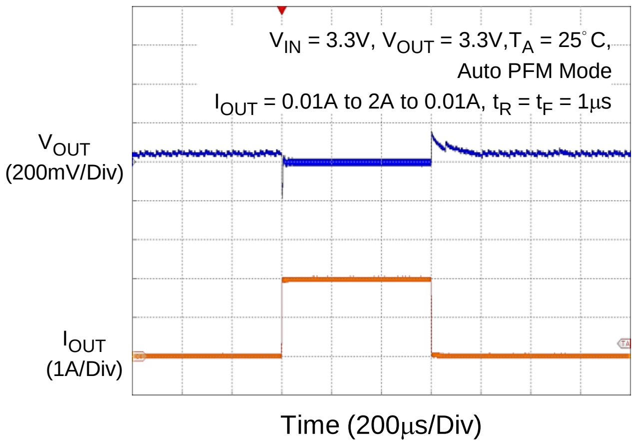
Line Transient Response (SPEC Condition)



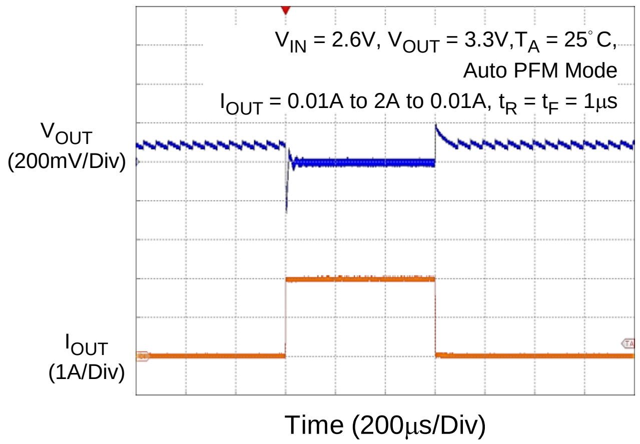
Load Transient Response (Buck)



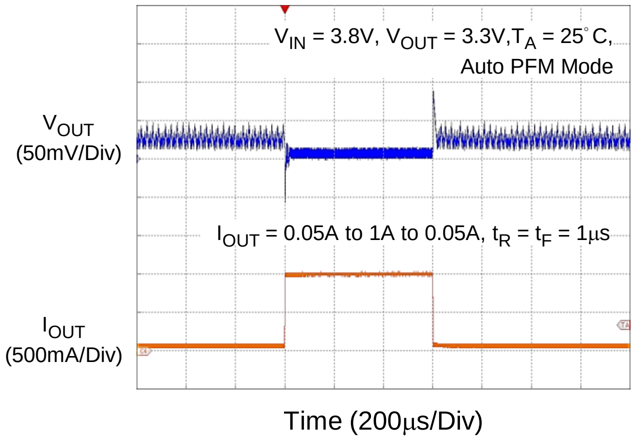
Load Transient Response (Buck-Boost)



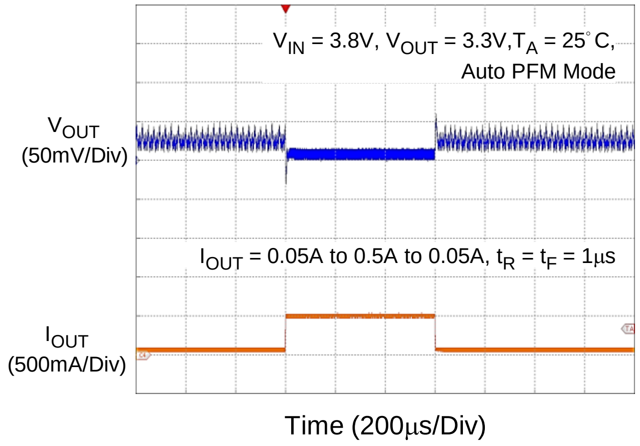
Load Transient Response (Boost)



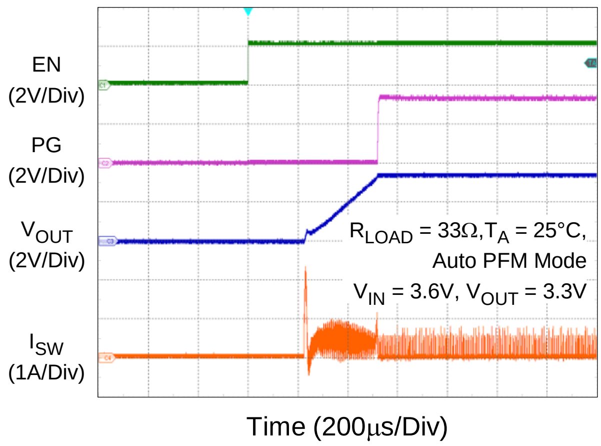
Load Transient Response (SPEC Condition1)



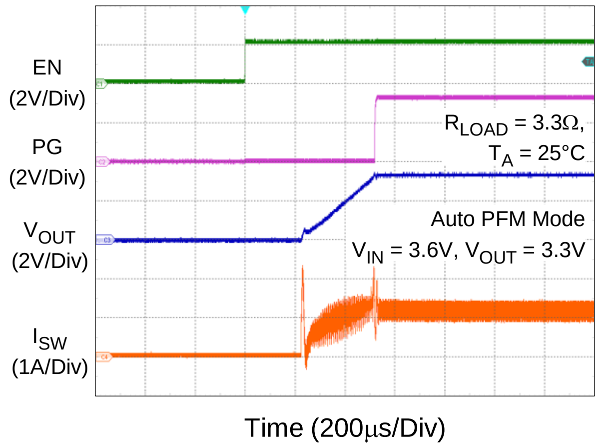
Load Transient Response (SPEC Condition2)



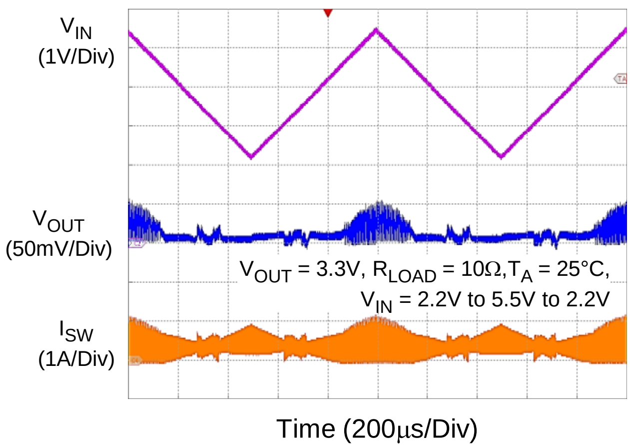
Start-Up Waveforms (Light Load)



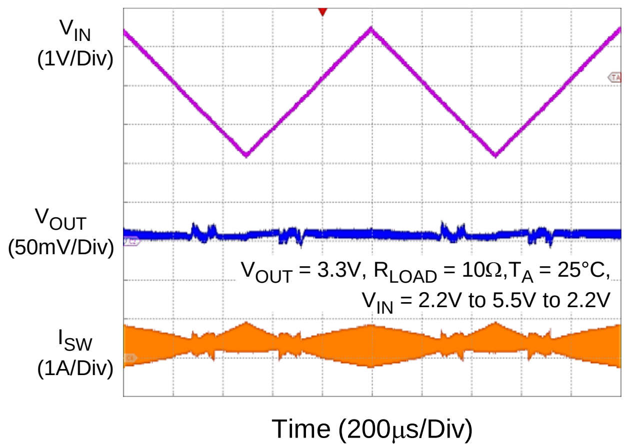
Start-Up Waveforms (Heavy Load)

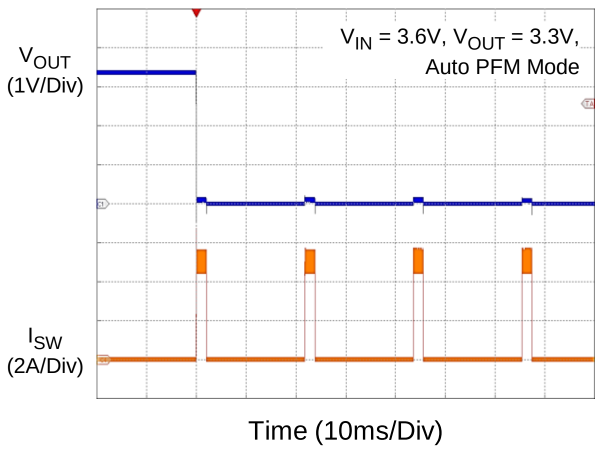


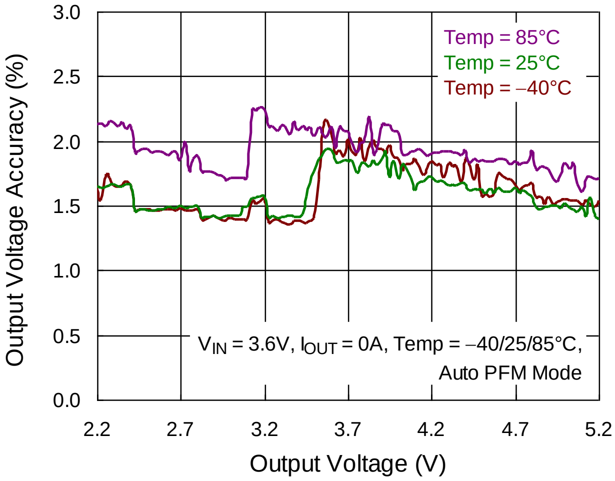
Line Sweep (Auto PFM Mode)

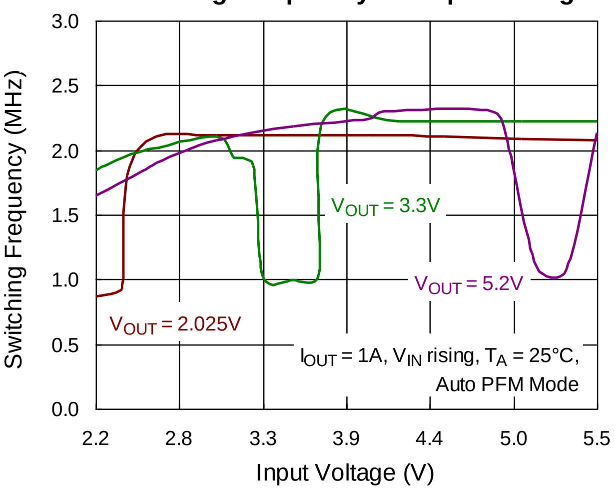


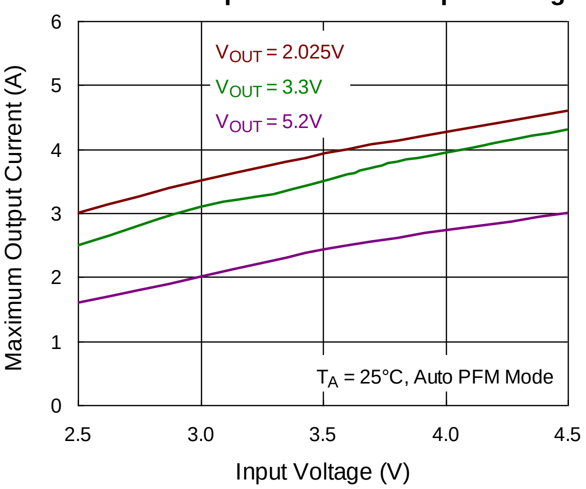
Line Sweep (FPWM Mode)




Output Short-Circuit Behavior
V_{IN} = 3.6V, V_{OUT} = 3.3V,
Auto PFM Mode
V_{OUT}
(1V/Div)
I_{SW}
(2A/Div)
Time (10ms/Div)


Output Voltage Accuracy
Temp = 85°C
Temp = 25°C
Temp = –40°C
V_{IN} = 3.6V, I_{OUT} = 0A, Temp = –40/25/85°C,
Auto PFM Mode
Output Voltage Accuracy (%)
Output Voltage (V)


Switching Frequency vs. Input Voltage
V_{OUT} = 3.3V
V_{OUT} = 5.2V
V_{OUT} = 2.025V
I_{OUT} = 1A, V_{IN} rising, T_A = 25°C,
Auto PFM Mode
Switching Frequency (MHz)
Input Voltage (V)


Maximum Output Current vs. Input Voltage
V_{OUT} = 2.025V
V_{OUT} = 3.3V
V_{OUT} = 5.2V
T_A = 25°C, Auto PFM Mode
Maximum Output Current (A)
Input Voltage (V)

15 Operation

The RT6167 adopts a high-efficiency, single-inductor, ACOT® (Advanced Constant On-Time) mode control mechanism designed to achieve a fast transient response and good stability with low-ESR ceramic capacitors.

The ACOT® control scheme uses a virtual inductor current ramp generated inside the IC to replace the ramp normally provided by the output capacitor's ESR. The internal ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

15.1 Buck Operation

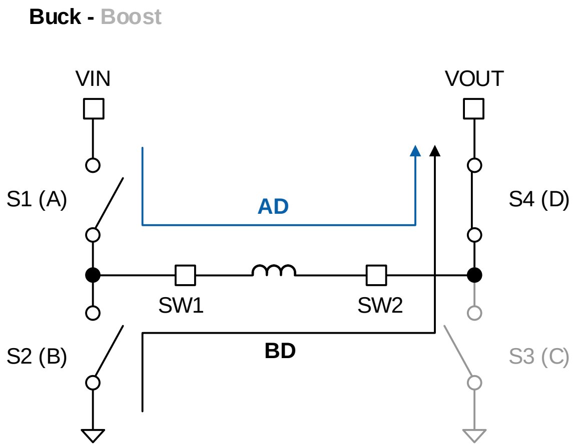


Figure 1. Buck Operation

When $V_{IN} > V_{OUT}$, the device operates like a buck converter. In steady-state buck-mode operation, the on-time pulse turns on the high-side switch S1, while S4 remains on, and the inductor current ramps up linearly. After the on-time period, the high-side switch S1 is turned off, and the synchronous rectifier switch S2 is turned on, while S4 remains on, and the inductor current ramps down linearly.

15.2 Boost Operation

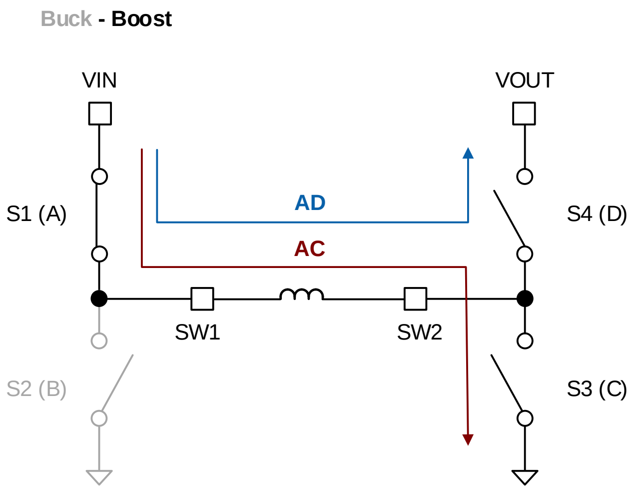


Figure 2. Boost Operation

When $V_{IN} < V_{OUT}$, the device operates like a boost converter. In boost mode under light load conditions, the on-time pulse turns on the S3 switch to maintain a constant on-time, while S1 remains on, and the inductor current ramps up linearly. After the on-time period, the S3 switch is turned off, and the synchronous rectifier switch S4 is turned on for a certain time, while S1 remains on, and the inductor current ramps down linearly. When the inductor current drops to zero, S4 will turn off. As the loading current increases, the device operates in CCM (continuous conduction mode), and the switches are modulated to maintain the desired output voltage. When the feedback signal is less than the reference value, the device turns on S3, while S1 remains on. After the off-time one-shot is cleared, the inductor current ramps up linearly. Then, the off-time one-shot turns on S4, while S1 remains on, and the inductor current ramps down linearly.

15.3 Buck-Boost Operation

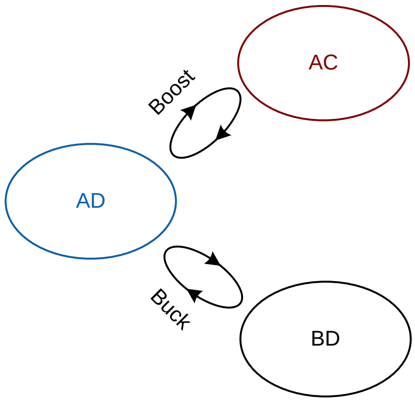


Figure 3. Buck-Boost Operation

When $V_{IN} \approx V_{OUT}$, all four transistors switch continuously, and the device operates in buck-boost mode. In buck-boost mode under light-load conditions, the device turns on switches S1 and S3, allowing the inductor current to increase linearly until it reaches the target peak-current level. When the inductor current reaches the peak-current level, switches S1 and S4 are turned on for a constant time, allowing the inductor current to decrease linearly. Afterward, switches S2 and S4 are turned on to ensure the inductor decreases to zero. At light-load conditions, the frequency increases as the load increases. Once the loading current is large enough, the converter will transition from boundary-conduction mode to continuous conduction mode. Furthermore, when V_{IN} is close to V_{OUT} in CCM, the switching frequency will decrease to half of the nominal switching frequency, and the device will maintain the output voltage tracking the target V_{OUT}.

16 Application Information

(Note 14)

The basic RT6167 application circuit is shown in the Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

16.1 Enable

The RT6167 provides an EN pin as an external chip enable control to enable or disable the device. If the EN voltage is held below the logic-high threshold (V_{EN_R}), switching is inhibited, even if the VIN voltage is above the UVLO rising threshold voltage (V_{UVLO_R}). If the EN voltage is held below 0.4V, the converter will enter shutdown mode; in this state, the converter is disabled, and the PG will be low state. During shutdown mode, the supply current can be reduced to I_{SHDN} (1μA or below). It is recommended that the VIN voltage should be higher than the VIN rising threshold voltage (V_{UVLO_R}) first. Then, when the EN voltage rises above the logic-high threshold (V_{EN_R}), the device will turn on, enabling switching and initiating the soft-start sequence.

16.2 Soft-Start and Shutdown Sequence

When the VIN voltage is held below Power-On Reset (POR) voltage, the PG state is undefined. Until VIN is higher than the POR level, PG will be reset and set to a low state. As the VIN voltage approaches V_{UVLO_R} and EN goes high, an internal current source charges an internal capacitor to build the soft-start ramp voltage. During the soft-start period, the device sets PG to “0” until VOUT reaches 99% of its set voltage. Otherwise, when the VIN voltage decreases to V_{UVLO_F}, the converter will shut down and the PG signal will transition to a low state after a delay time (t_dly) of 15μs. The PG will be in an undefined state because the VIN voltage is held below the POR voltage again. The start-up and shutdown flow are shown in Figure 4.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if

- The load current is large
- The output capacitance is large

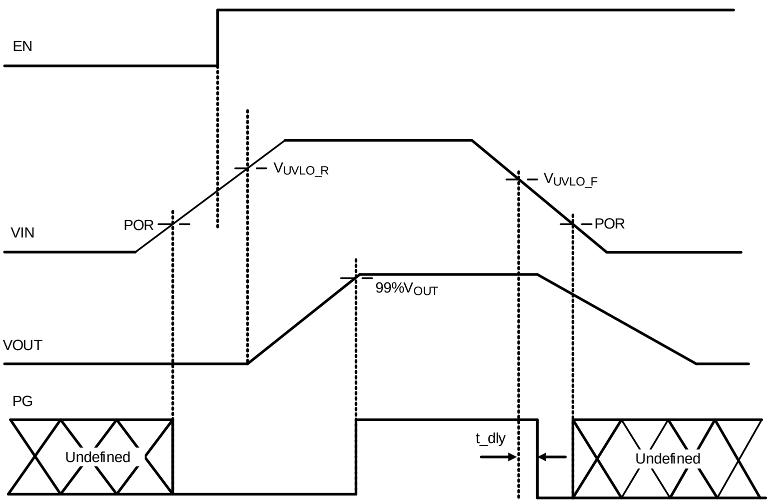


Figure 4. Soft-Start and Shutdown Sequence

16.3 VSEL

The RT6167 provides 128 output voltage options, as detailed in Table 2. Users can choose between two of these options by setting the VSEL pin to either high or low. These selections are determined by the internal address through factory trimming. Below is the register table for the output voltage.

Table 2. Register VOUT1/VOUT2[6:0] vs. Output Voltage

The output voltage 1 can be set based on the register table below when the VSEL pin is low, and the output voltage 2 can be set based on the register table below when the VSEL pin is high.

Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)	Register VOUT[6:0]	Output Voltage (V)
0000000	2.025	0100000	2.825	1000000	3.625	1100000	4.425
0000001	2.05	0100001	2.85	1000001	3.65	1100001	4.45
0000010	2.075	0100010	2.875	1000010	3.675	1100010	4.475
0000011	2.1	0100011	2.9	1000011	3.7	1100011	4.5
0000100	2.125	0100100	2.925	1000100	3.725	1100100	4.525
0000101	2.15	0100101	2.95	1000101	3.75	1100101	4.55
0000110	2.175	0100110	2.975	1000110	3.775	1100110	4.575
0000111	2.2	0100111	3	1000111	3.8	1100111	4.6
0001000	2.225	0101000	3.025	1001000	3.825	1101000	4.625
0001001	2.25	0101001	3.05	1001001	3.85	1101001	4.65
0001010	2.275	0101010	3.075	1001010	3.875	1101010	4.675
0001011	2.3	0101011	3.1	1001011	3.9	1101011	4.7
0001100	2.325	0101100	3.125	1001100	3.925	1101100	4.725
0001101	2.35	0101101	3.15	1001101	3.95	1101101	4.75
0001110	2.375	0101110	3.175	1001110	3.975	1101110	4.775
0001111	2.4	0101111	3.2	1001111	4	1101111	4.8
0010000	2.425	0110000	3.225	1010000	4.025	1110000	4.825
0010001	2.45	0110001	3.25	1010001	4.05	1110001	4.85
0010010	2.475	0110010	3.275	1010010	4.075	1110010	4.875
0010011	2.5	0110011	3.3	1010011	4.1	1110011	4.9
0010100	2.525	0110100	3.325	1010100	4.125	1110100	4.925
0010101	2.55	0110101	3.35	1010101	4.15	1110101	4.95
0010110	2.575	0110110	3.375	1010110	4.175	1110110	4.975
0010111	2.6	0110111	3.4	1010111	4.2	1110111	5
0011000	2.625	0111000	3.425	1011000	4.225	1111000	5.025
0011001	2.65	0111001	3.45	1011001	4.25	1111001	5.05
0011010	2.675	0111010	3.475	1011010	4.275	1111010	5.075
0011011	2.7	0111011	3.5	1011011	4.3	1111011	5.1
0011100	2.725	0111100	3.525	1011100	4.325	1111100	5.125
0011101	2.75	0111101	3.55	1011101	4.35	1111101	5.15
0011110	2.775	0111110	3.575	1011110	4.375	1111110	5.175
0011111	2.8	0111111	3.6	1011111	4.4	1111111	5.2

16.4 Auto Pulse Frequency Modulation Mode

Setting the MODE pin to a low state, the RT6167 will operate in PFM (Pulse Frequency Modulation) mode. To save power and improve efficiency at low loads, the buck/boost converter operates in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to the load to maintain output voltage regulation. When the load increases and the inductor current becomes continuous again, the buck/boost converter automatically switches back to PWM fixed frequency mode. Additionally, the RT6167 will enter DSLP (Deep Sleep) mode to achieve low input quiescent current at no load.

16.5 Ultra-Sonic Mode

Setting the MODE pin to a high state, the RT6167P-AA operates in ultra-sonic mode. To avoid acoustic noise problems during operation, the switching frequency is designed to always be higher than 30kHz, even when there is no load at the output.

16.6 Forced Pulse Width Modulation Mode

Setting the MODE pin to a high state, the RT6167P-AB will operate in FPWM Mode. The switching frequency is forced into PWM mode operation. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM.

16.7 Output Discharge

The device actively discharges the output in the following two conditions:

- The EN pin is low.
- When the voltage falls below the UVLO falling threshold (V_{UVLO_F}), the function will enable. However, if the voltage is too low to activate the discharge function, it will be disabled. This implies that if the VIN's slew rate of decrease is too rapid, the output voltage might not discharge completely. As described in the Typical Application Circuit, the drop rate of VIN should be slower than 0.22V/ms to achieve a full discharge when V_{OUT} = 3.3V.

16.8 Power-Good Indicator

The RT6167 features an open-drain Power-Good output (PG) to monitor the output voltage status. Connect a pull-up resistor with a value of 100kΩ from the PG pin to an external voltage. When the output voltage reaches 99% of its target value, the PG signal is pulled up to indicate “Power-Good” status until the device is disabled or any other protection is triggered. The truth table of the Power-Good indication is shown in Table 3. The SS_END indicates whether the soft-start action is finished or not. (SS_END = 1 means the soft-start action is finished.)

Table 3. Power-Good Indicator Truth Table (Note 12)

EN	VIN	Soft-Start	VOUT	Fault Event	PG Status
X	V_{IN} < POR	SS_END = 0	X	X	Undefined
X	POR < V_{IN} < V_{UVLO_R}	SS_END = 0	X	X	Low
Low	V_{UVLO_R} < V_{IN}	SS_END = 0	X	X	Low
High	V_{UVLO_F} < V_{IN}	SS_END = 0	V_{OUT} < 99% x V_{OUT_Target}	X	Low
High	V_{UVLO_F} < V_{IN}	SS_END = 1	99% x V_{OUT_Target} < V_{OUT}	OTP = 0 AND UVP = 0 AND OVP = 0 AND OCP = 0	High impedance

EN	VIN	Soft-Start	VOUT	Fault Event	PG Status
High	$V_{UVLO\_F} < V_{IN}$	SS_END = 1	After 99% x $V_{OUT\_Target} < V_{OUT}$, V_{OUT} < 90% x V_{OUT_Target} (UVP) or V_{OUT} > 6V (OVP)	OTP = 1 OR UVP = 1 OR OVP = 1 OR OCP = 1	Low
High	$V_{IN} < V_{UVLO\_F}$	SS_END = 1	X	X	Low

Note 12. X = Don't care.

16.9 Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW1 and SW2 waveforms to adjust the zero current threshold voltage. When the current of the low-side MOSFET decreases to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to achieve better efficiency.

16.10 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

16.11 PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominally 2.2MHz.

16.12 Inductor Selection

Choosing an inductor value will affect transient response, ripple, and other performance aspects. The RT6167 recommends a nominal inductance value of 0.47μH to achieve optimal performance.

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L, which is I_{MAX} multiplied by 0.3, will be a reasonable starting point.

The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor's current rating (causing a 40°C temperature rise from a 25°C ambient) should be greater than the maximum load current, and its saturation current should be greater than the short circuit peak current limit.

16.13 Input Capacitor Selection

The steady-state and transient response performance also depend on input voltage stability. The RT6167 recommends using at least a 10μF input capacitor to prevent input voltage instability during operation.

It is recommended to place the capacitor as close as possible to the VIN and GND pins of the IC. If the input supply is located more than a few centimeters from the device, adding some bulk capacitance to the ceramic bypass capacitors is recommended.

A 47μF electrolytic capacitor is a typical selection for the bulk capacitance.

16.14 Output Capacitor Selection

The ripple voltage is an important index for choosing the output capacitor. This portion consists of two parts: one is the product of ripple current with the ESR of the output capacitor, and the other part is formed by the charging and discharging process of the output capacitor.

The output capacitor is selected based on the output ripple, which is calculated using the equation below:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT_{CAP}}$$

$$\Delta V_{ESR} = I_{C_{RMS}} \times R_{C_{ESR}}$$

$$\Delta V_{OUT_{CAP}} = \frac{I_{OUT} \times Duty}{f_{SW} \times C_{MIN}}$$

Users can choose a capacitor using the equation to meet the system's ripple specifications. It is recommended to use at least two 22μF capacitors to match the application's requirements for VOUT ripple and stability performance.

Table 4. Protection Trigger Condition and Behavior

The RT6167 features several protections, such as OCP, OVP, UVLO, OTP, and UVP. The table below describes the protection actions.

Protection Type	Threshold Refer to Electrical Spec.	Deglitch Time	Protection Method	Reset Method
OCP (Note 13)	I_L > 5A	0	Turn off boost LG or Turn off buck UG	I_L < 4.5A
UVLO	V_{IN} < 2.08V (maximum)	0	Turn off all	V_{IN} > 2.17V (maximum)
OTP	TEMP > 150°C	0	Turn off all	OTP Hysteresis = 20°C
OVP	V_{OUT} > 6V	0	Turn off all	V_{OUT} < 5.6V
UVP	V_{OUT} < 0.9 x V_{OUT_Target}	2ms	Turn off all	V_{OUT} > 0.95 x V_{OUT_Target}

Note 13. Turn off all switches when OCP event occurs and is continuing for 2ms.

16.15 Overcurrent Protection

The Overcurrent Protection (OCP) function is implemented by UGATE and LGATE. When the inductor current reaches the UGATE current limit threshold, the high-side MOSFET will be turned-off. The low-side MOSFET turns on to discharge the inductor current until the inductor current drops below the LGATE current limit threshold. After the UGATE current limit is triggered, the maximum inductor current is determined by the inductor current rising rate and the response delay time of the internal network.

16.16 Input Undervoltage-Lockout Protection

In addition to the EN pin, the RT6167 also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the V_{IN} voltage rises above V_{UVLO_R}. This ensures that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. After the device is powered up, if the V_{IN} voltage goes below the UVLO falling threshold voltage (V_{UVLO_F}), switching will be inhibited. If the V_{IN} voltage rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume switching.

16.17 Over-Temperature Protection

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will automatically resume switching. This mechanism helps to avoid damage to the device caused by temperatures exceeding its limits.

16.18 Overvoltage Protection

When the VOUT pin is floating, the device will trigger overvoltage protection to prevent the output voltage from exceeding critical values. If the output reaches the OVP threshold, the device will regulate the voltage to maintain it at this threshold value. During PFM operation, the OVP function is disabled to enhance the performance of quiescent current (I_{Q_SW}) when the RT6167 enters the DSLP mode. OVP is only enabled when the UG MOSFET is active. Therefore, this function cannot be verified by forcing a voltage to VOUT. The above descriptions are guaranteed by design.

16.19 Undervoltage Protection

The RT6167 provides Hiccup Mode for Undervoltage Protection (UVP). When the V_{OUT} voltage drops below 90% of the target V_{OUT}, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT6167 will retry to build up the output voltage automatically. When the UVP condition is removed, the converter will soft-start to the target voltage and resume normal operation.

16.20 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-15B 1.4x2.3 (BSC) package, the thermal

resistance, θ_{JA}, is 53°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (53°C/W) = 1.88W for a WL-CSP-15B 1.4x2.3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

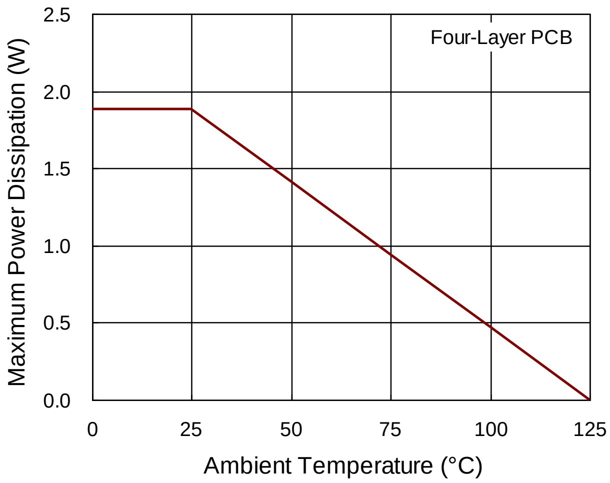


Figure 5. Derating Curve of Maximum Power Dissipation

16.21 Layout Considerations

For the best performance of the RT6167, the following layout guidelines must be strictly followed.

- The input capacitor must be placed as close as possible to the IC to minimize the power loop area. A typical 0.1μF decoupling capacitor is recommended to reduce the power loop area and any high-frequency components on VIN.
- The switching nodes (SW1 and SW2) have high-frequency voltage swings and should be kept at a small area. Keep analog components away from the SW1 and SW2 nodes to prevent stray capacitive noise pickup.
- Keep every power trace connected to the pin as wide as possible to improve thermal dissipation.
- The AGND pin is suggested to be connected to the 2^{nd} GND plane through a via from the top to the 2^{nd} layer.

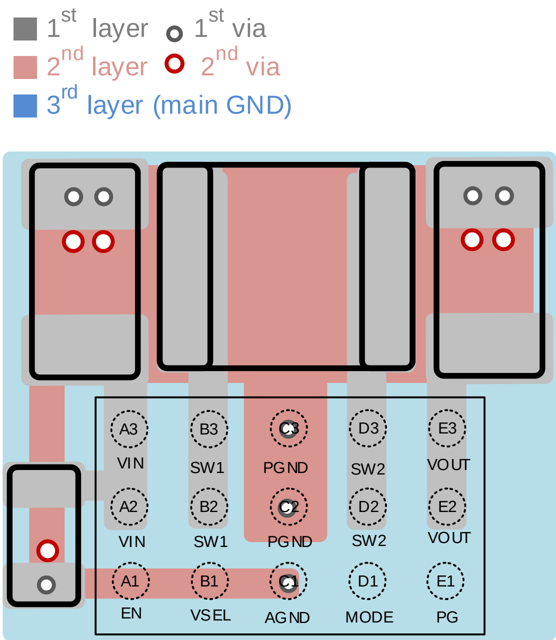
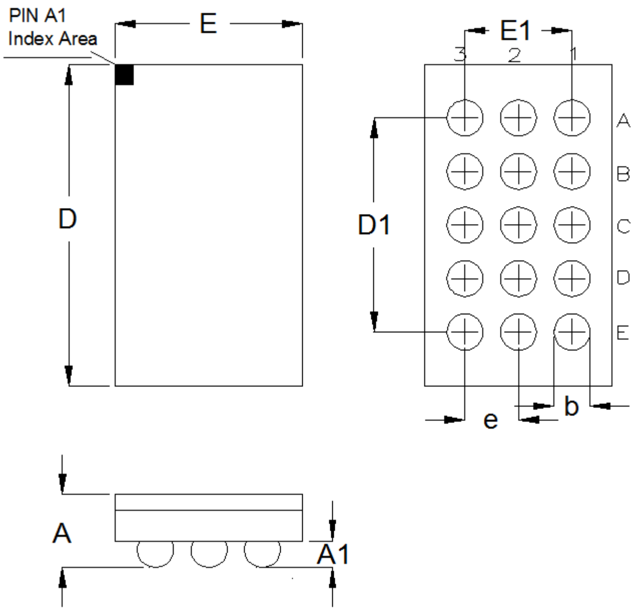


Figure 6. Layout Guide

1. The loop from VIN to CIN to PGND should be as short as possible to reduce the switching noise in buck mode.
2. The loop from VOUT to COUT to PGND should be as short as possible to reduce the switching noise in boost mode.
3. The loop from VIN to AGND should be separated from the PGND loop to reduce noise.
4. Connect AGND directly to C3 or C2 to reduce noise.

Note 14. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

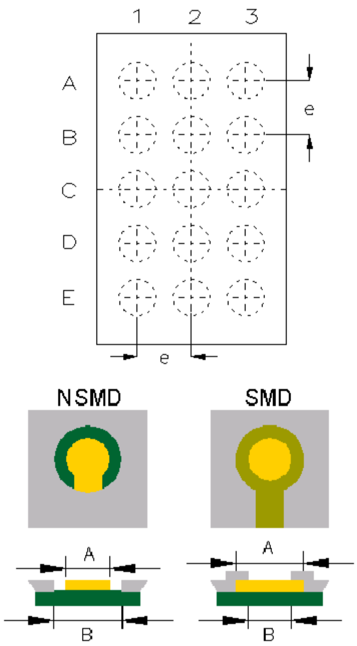
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.260	2.340	0.089	0.092
D1	1.600		0.063	
E	1.360	1.440	0.054	0.057
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.4x2.3 Package (BSC)

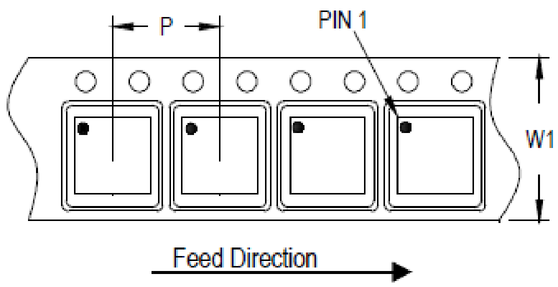
18 Footprint Information

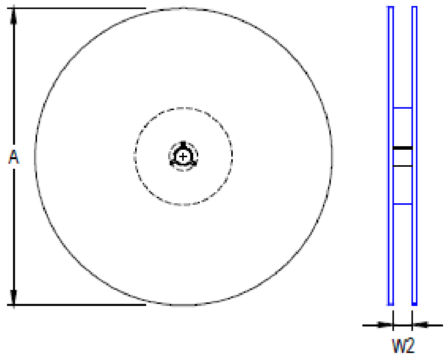


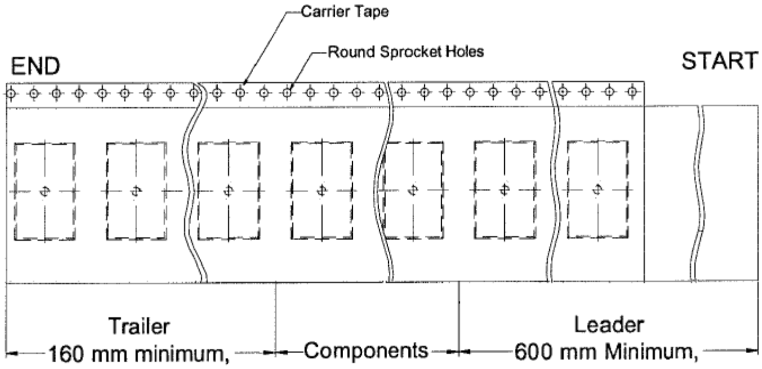
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.4x2.3-15(BSC)	15	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19 Packing Information

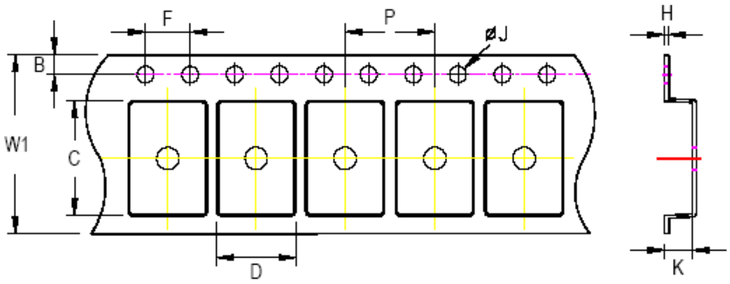
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
WL-CSP 1.4x2.3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.8mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.4x2.3	7"	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00	2024/12/12	Final	*Features on page 1* - Modified the quiescent current description *Typical Operating Characteristics on page 15* - Removed the redundant waveforms *Application Information on page 24* - Adjusted the order of DS statements *Packing Information on page 29* - Updated Tape and Reel Data
01	2025/7/4	Modify	*Ordering Information on page 1* - Updated ordering information