14A, 17V, 400kHz/800kHz/1200kHz Synchronous Step-Down Converter with VID Control

General Description

The RT6245 is a high-performance, synchronous step-down converter that delivers up to 14A output current with an input supply voltage range of 4.5V to 17V.

The output voltage can be programmable from 0.4375V to 1.3875V with I^{2}C controlled 7-Bits VID.

The RT6245 adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultrafast transient response and further reduces the external-component count. In steady states, the ACOT® operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The RT6245A offers automatic PSM that maintains high efficiency during light load operation.

The device offers a variety of functions for more design flexibility. The switching frequency, current limit level and V_{OUT} slew rate are selectable via I^{2}C. Independent enable control input pin and power good indicator are also provided for easy sequence control. Besides, the designers can also command the device to be enabled or shutdown via the I^{2}C interface.

To control the inrush current during the startup, the device provides a programmable soft start-up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit control, OVP, UVP, input UVLO and OTP.

The RT6245 is available in a thermally enhanced VQFN-19L 3.5x3.5 (FC) package.

Features

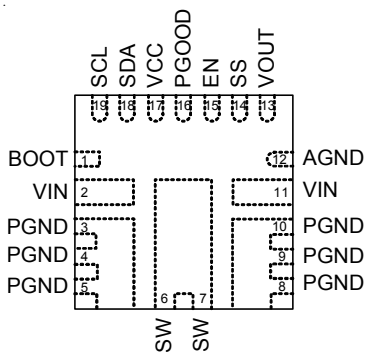
- **VID Control Range via I^{2}C Compatible Interface : 0.4375V to 1.3875V in 12.5mV Steps**
- **4.5V to 17V Input Voltage Range**
- **14A Output Current Only Support 400kHz**
- **Integrated 9.8mΩ/4.5mΩ MOSFETs**
- **Stable with Ceramic Output Capacitor**
- **ACOT® Control for Fast Transient Response**
- **Selectable Switching Frequency (400kHz/800kHz/1200kHz)**
- **Adjustable Current Limit Level**
- **Adjustable Thermal Shutdown Level**
- **Programmable Soft-Start Time with a Default 2ms**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **19-Lead VQFN (FC) Package**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Pin Configuration

(TOP VIEW)



VQFN-19L 3.5x3.5 (FC)

Ordering Information

RT6245 □□□

- Package Type
  QVF : VQFN-19L 3.5x3.5 (FC) (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- PWM Operation Mode
  A : DCM at Light Load
  B : FCCM at Light Load

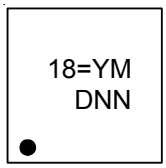
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

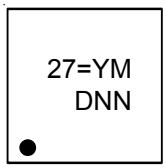
RT6245AGQVF



18= : Product Code

YMDNN : Date Code

RT6245BGQVF



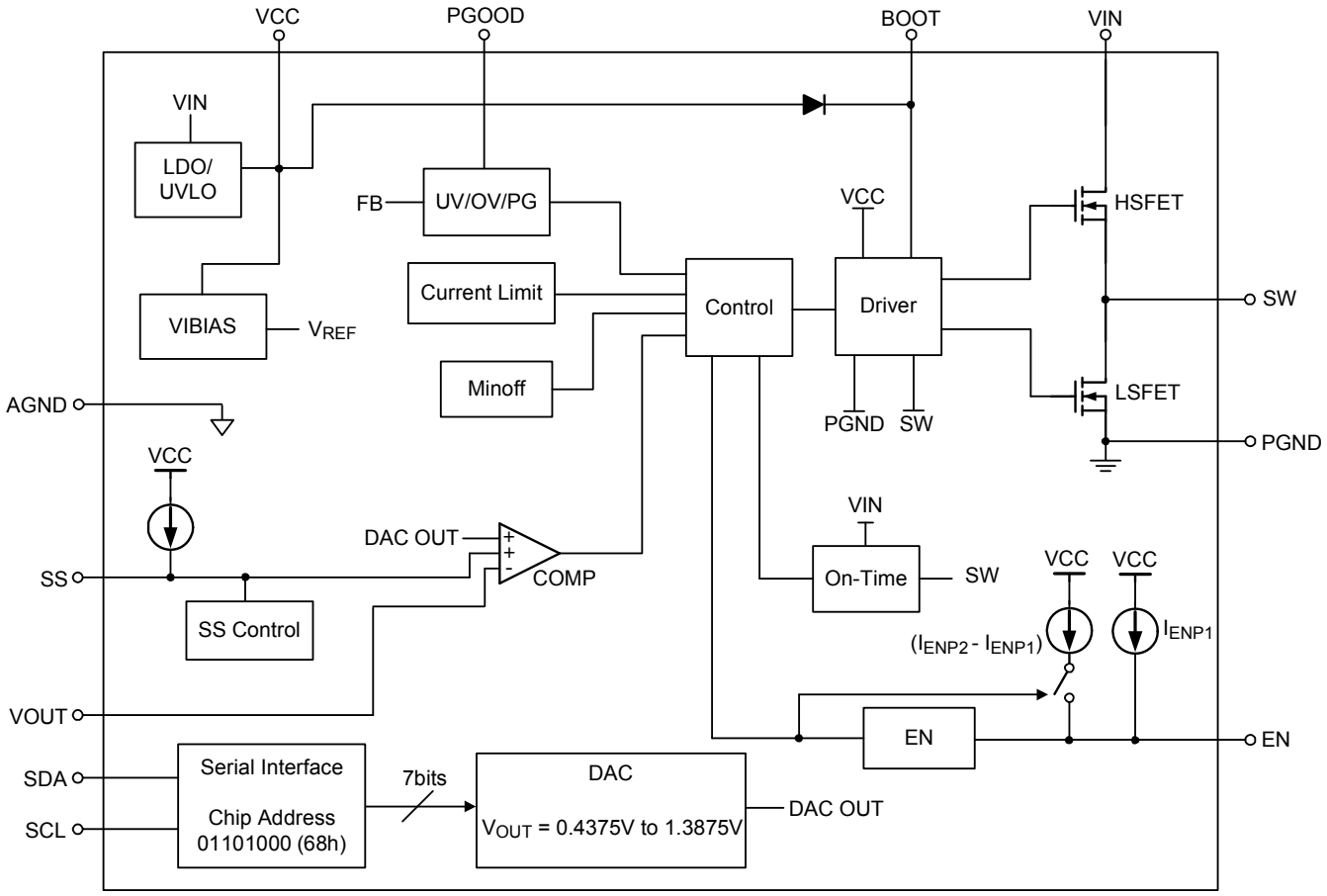
27= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
2, 11	VIN	Input voltage. Support 4.5V to 17V input voltage. It is suggested to place equal-value input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
3, 4, 5, 8, 9, 10	PGND	System GND. The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
6, 7	SW	Switch node. Connect to the power inductor.
12	AGND	Analog GND. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
13	VOUT	Output voltage sense pin, the output voltage is controlled by I^2C setting.
14	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 1ms without external capacitor.
15	EN	IC enable pin. Leave EN pin floating to enable the IC.
16	PGOOD	Open-drain, power good output. After soft-start, indicating the output voltage is regulating within tolerance. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
17	VCC	4.7V internal LDO output. Connect a 4.7μF capacitor as close to the VCC pin as possible. It does not recommend connecting VCC to supply others rails.
18	SDA	Serial interface data line. Pull down if I^2C is non-used.
19	SCL	Serial interface clock. Pull down if I^2C is non-used.

Functional Block Diagram



Operation

The RT6245 is a high efficiency synchronous step-down converter utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small capacitance to save the PCB size.

During normal operation, the internal high-side power switch (HSFET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET turns off, the low-side power switch (LSFET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has similar shape as the inductor current, and the output voltage ripple directly compared with the internal reference. When the minimum off-time one-shot (310ns, max.) has timed out and the inductor current is below the current limit threshold, the One-shot is triggered again if the output voltage falls below the internal reference voltage (0.75V, default.). To achieve stable operation with low-ESR ceramic output capacitors, an internal ramp signal is added to the internal reference voltage to simulate the output voltage ripple. ACOT®control architecture features ultrafast transient response. When a load is suddenly increased, the output voltage drops quickly, and almost immediately, a new On-time is triggered, and inductor current rises again.

Traditional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. But even with defined input and output voltages, a fixed on-time will mean that frequency will have to increase at higher load levels to compensate for the power losses in the MOSFETs and Inductor. ACOT®control further added a frequency locked loop system, which slowly adjusts the on-time to compensate the power losses, without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the RT6245 are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator that generates 4.7V at VCC. The voltage on VCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains the C_{BOOT} voltage is sufficient to turn-on the HSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is above the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VCC rail that can pull a current higher than the internal LDO's current limit from the VCC, then the VCC drops below the UVLO falling threshold and thereby shutting down the output of the RT6245.

Enable, Start-Up, Shutdown and UVLO

The RT6245 implements under-voltage lockout protection (UVLO) to prevent operation without fully turn-on the internal power MOSFETs. The UVLO monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device is shut off. UVLO is non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching and when the EN pin voltage falls below the turn-off threshold (V_{ENL}) it stops switching. The EN pin of the RT6245 has internally pull-up with current source.

When appropriate voltages are present on the VIN, VCC, and EN pins, the RT6245 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 6μA current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower than the internal 2ms soft-start, the output voltage will be limited by the ramp rate on the SS pin instead. Once both of the external and internal soft-start ramps have exceeded 0.85V, the output voltage will be in regulation. The typical

external soft-start time can be calculated by the equation below.

$$C_{SS}\,(nF) = \frac{t_{SS}\,(ms) \times I_{SS}\,(\mu A)}{V_{REF}\,(V)}$$

Where I_{SS} = 6μA, V_{REF} = 0.75V

When the V_{EN} is lower than V_{ENL}, the SS pin voltage is reset to GND.

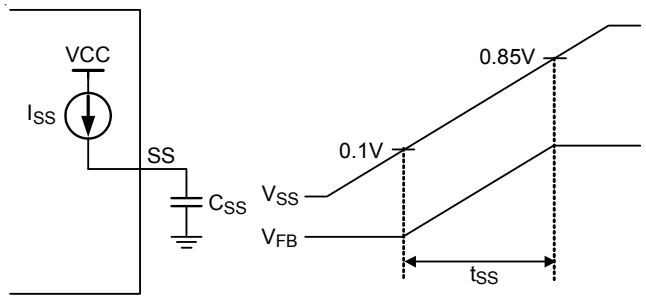


Figure 1. External Soft-Start Time Setting

Pre-Bias

If there is a residual voltage on output voltage before start-up, both of the internal HSFET and LSFET are prohibited switching until the soft-start ramp is higher than output voltage. When the soft-start ramp cross above the output voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated target.

Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero-current-detect circuitry which utilizing the LSFET $R_{DS(ON)}$ to sense the inductor current. The LSFET is turned off when the inductor current drops to zero, resulting in discontinuous operation (DCM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the output voltage falls below the internal reference voltage. The RT6245A with DCM operation maintains high efficiency at light load.

Switching Frequency, Minimum On-Time and Minimum Off-Time

The RT6245 offers three different switching frequency of 400kHz, 800kHz and 1200kHz via the I^2C setting. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

An additional constraint on operating frequency is the minimum controllable on-time and off-time. The minimum on-time is the smallest duration of time in which the high-side power MOSFET (HSFET) can be in its "on" state. This time is typically 54ns. In continuous mode operation, the minimum duty cycle can be estimated by ignoring component losses as follows

$$D_{MIN} = f_{SW} \times t_{ON\_MIN}$$

Where t_{ON_MIN} is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RT6245 is capable of turning on the low-side power MOSFET (LSFET), tripping the current comparator and turning the power MOSFET back off. This time is 310ns (max.). The minimum off-time limit imposes a maximum duty cycle of t_{ON} /(t_{ON} + t_{OFF_MIN}).

Current Limit and Output Under-Voltage Protection

The RT6245 can operate at four different current limits I_{LIM_1}, I_{LIM_2}, I_{LIM_3} and I_{LIM_4} to support an output continuous current of 14A, 12A, 10A and 8A respectively. The device cycle-by-cycle compares the valley current of the inductor against the current limit threshold, hence the output current will be half the ripple current higher than the valley current.

The inductor current level is monitored by measuring the low-side MOSFET voltage between the SW pin and GND, which is proportional to the switch current, during the on-time of LSFET. To improve the current measurement accuracy, temperature compensation is added internally. If the measured drain to source voltage of the LSFET is above the voltage proportional to current limit, the LSFET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support.

When the output voltage falls below Output UVP Threshold (V_{UVP}), the UVP comparator detects it and shuts down the device to avoid the excessive heat. If the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated. It is shown in Figure 2. When the overcurrent condition is removed, the output voltage returns to the regulated value.

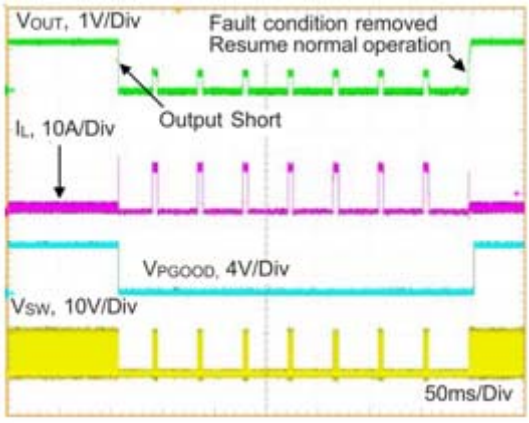


Figure 2. Current Limit and UVP

Similar to the forward overcurrent, the reverse current protection is realized by monitoring the current across the low-side MOSFET. When the LSFET current reaches –4A (typ.), the synchronous rectifier is turned off. This limits the ability of the regulator to actively pull-down on the output.

Power-Good Output

The PGOOD pin is an open-drain power-good indication which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{OUT}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{OUT} rises above a power-good threshold V_{TH_PGLH} (typically 93% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{OUT} drops by a V_{OUT} falling hysteresis ΔV_{TH_PGLH} (typically 9% of the target value) or exceeds V_{OUT} rising threshold V_{TH_PGHL} typically 116% of the target value), the PGOOD pin will be pulled low. For V_{OUT} above V_{OUT} falling hysteresis, V_{PGOOD} will be pulled high again when V_{OUT} drops back by a power-good hysteresis ΔV_{TH_PGHL} (typically 9% of the target value). Once being started-up, if any protection is triggered (UVP and OTP) or EN is from high to low, PGOOD will be pulled to GND. The internal open-drain pull down device with 250Ω resistance will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic VOUT changes, the RT6245's PGOOD falling edge includes a blanking delay of 10μs (default).

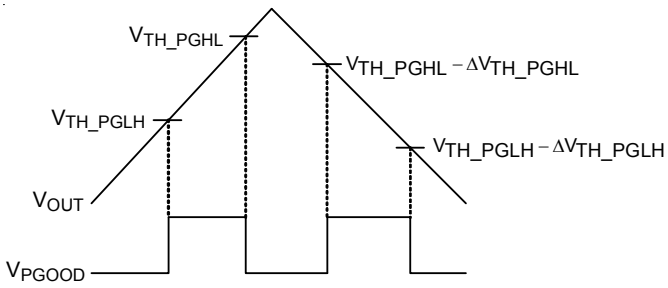


Figure 3. The Logic of PGOOD

Output Over-Voltage Protection (OVP)

The RT6245 provides an over-voltage protection (OVP), If the output voltage V_{OUT} rises above 121% of the internal reference voltage, the over-voltage protection is triggered, the discharging switch from SW to GND is turned on to discharge output voltage.

Over-Temperature Protection (OTP)

The RT6245 monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SD}, default 150°C), the RT6245 stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. During start up, if the device temperature is higher than T_{SD} the device does not start switching. The device re-starts switching when the temperature drops more than 15°C (typ.). Thermal shutdown threshold is adjustable by I^2C special codes.

Output Voltage Discharge

An internal 500Ω discharge switch that discharges the V_{OUT} through SW node during any fault events like OVP, UVP, OTP, VCC voltage below UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Enable Pin Voltage, EN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to 20V
  SW (t ≤ 100ns) ---------- –5V to 25V
- Boot Voltage, BOOT ---------- –0.3V to 26V
- BOOT to SW (BOOT–SW) ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-19L 3.5x3.5 (FC) ---------- 3.57W
- Package Thermal Resistance (Note 2)
  VQFN-19L 3.5x3.5 (FC), θ_{JA} ---------- 28°C/W
  VQFN-19L 3.5x3.5 (FC), θ_{JC} ---------- 2.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 4.5V to 17V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

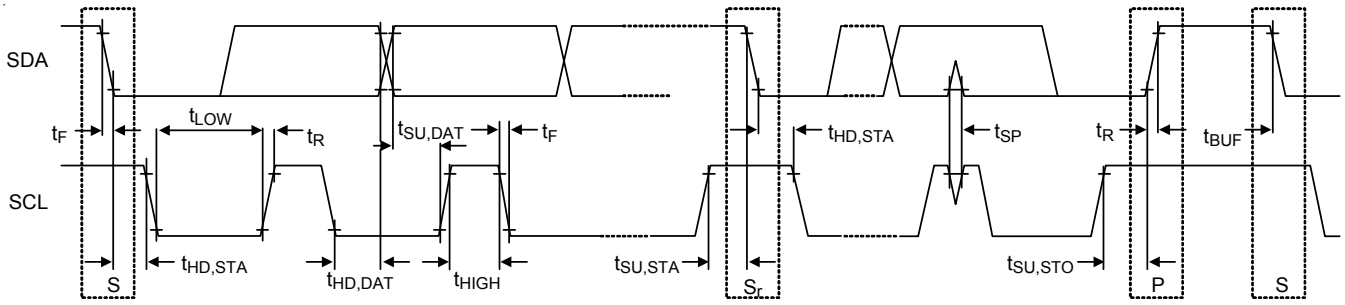
(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5	--	17	V
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V	--	7	--	μA
Supply Current by VID (Shutdown)	I_{SHDN_VID}	special code = 11110110	--	75	150	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 5V, non-switching	--	600	1200	μA
Logic Threshold						
EN Input Rising Threshold	V_{ENH}		1.175	1.225	1.3	V
EN Input Falling Threshold	V_{ENL}		1.025	1.104	1.15	V
EN Hysteresis	ΔV_{EN}		--	0.121	--	V
EN Pull-Up Current	I_{ENP1}	V_{EN} = 1V	0.35	2	2.95	μA
	I_{ENP2}	V_{EN} = 1.3V	3	4.2	5.5	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage						
Output Voltage	V_{OUT}	Regulation mode	0.7425	0.75	0.7575	V
Output Voltage by VID	V_{OUT_VID}	I^2C mode	Ideal V_{OUT} −1.5%	Ideal V_{OUT}	Ideal V_{OUT} +1.5%	V
Minimum Output Voltage Rising Time per 12.5mV		special code = 11100001 (default)	--	1	--	μs
Maximum Output Voltage Rising Time per 12.5mV		special code = 11101000 (default)	--	8	--	μs
$R_{DS(ON)}$						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$		--	9.8	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	4.5	--	mΩ
Current Limit						
Low-Side Switch Sourcing Current Limit	I_{LIM_1}	special code = 11110000	13.6	16.1	18.6	A
	I_{LIM_2}	special code = 01110001 (default)	11.7	13.8	15.9	
	I_{LIM_3}	special code = 01110010	9.7	11.5	13.3	
	I_{LIM_4}	special code = 01101111	7.4	9.2	11	
Low-Side Switch Negative Current Limit	V_{LIM_NEG}	Valley current	--	−4	--	A
Switching Frequency						
Switching Frequency	f_{SW1}	special code = 11111100	--	400	--	kHz
	f_{SW2}	special code = 01111101	--	800	--	kHz
	f_{SW3}	special code = 01111110	--	1200	--	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	54	--	ns
Minimum Off-Time	t_{OFF_MIN}	V_{FB} = 0.5V	--	--	310	ns
Soft-Start						
Soft-Start Time	t_{SS}	Internal soft-start time	--	2	--	ms
Soft-Start Charge Current	I_{SS}		4.9	6	7.1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVLO						
UVLO Rising Threshold	V_{UVLOH}	V_{LDO} rising	--	4.3	--	V
UVLO Hysteresis	ΔV_{UVLO}	V_{LDO} hysteresis	--	730	--	mV
LDO Output						
LDO Output Voltage	V_{CC}		--	4.7	--	V
LDO Output Current Limit	I_{LIM_LDO}		50	--	200	mA
Output Under-Voltage and Over-Voltage Protections						
Output OVP Threshold	V_{OVP}	OVP detect	--	120	--	$\%V_{OUT}$
Output UVP Threshold	V_{UVP}	UVP detect	--	68	--	$\%V_{OUT}$
Power Good						
Power Good Threshold	V_{PGOOD}	V_{OUT} rising threshold, PGOOD from low to high	--	92.5	--	$\%V_{OUT}$
		V_{OUT} falling hysteresis, PGOOD from high to low	--	9	--	$\%V_{OUT}$
		V_{OUT} rising threshold, PGOOD from high to low	--	115	--	$\%V_{OUT}$
		V_{OUT} falling hysteresis, PGOOD from low to high	--	9	--	$\%V_{OUT}$
Power Good Fault Delay		special code = 11111001 (default)	--	10	--	μs
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Special code = 11110011 (default)	--	150	--	°C
		Special code = 01110100	--	130	--	
		Special code = 11110101	--	170	--	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Serial Interface (SDA and SCL pins) Note(5)							
Input Voltage	High-Level	V_{IH}		2.5	--	--	V
	Low-Level	V_{IL}		--	--	0.6	
Low Level SDA Output Voltage		V_{OL1}	Open drain, 3mA sink current	--	--	0.5	V
SCL Clock Frequency		f_{SCL}		--	--	400	kHz
Hold Time (repeated) START Condition		$t_{HD,STA}$		0.6	--	--	µs
Low Period of SCL Clock		t_{LOW}		1.3	--	--	µs
High Period of SCL Clock		t_{HIGH}		0.6	--	--	µs
Set-Up Time for a Repeated START Condition		$t_{SU,STA}$		0.6	--	--	µs
Data Hold Time		$t_{HD,DAT}$		50	--	900	ns
Data Set-Up Time		$t_{SU,DAT}$		100	--		ns
Rise Time (SDA or SCL)		t_R	C_B: Capacitance of bus line in pF	20 + 0.1C_B	--	300	ns
Fall Time (SDA or SCL)		t_F	C_B: Capacitance of bus line in pF	20 + 0.1C_B	--	300	ns
Set-Up Time for STOP Condition		$t_{SU,STO}$		0.6	--	--	µs
Bus Free Time between STOP and START Condition		t_{BUF}		1.3	--	--	µs
Capacitive Load for Each Bus Line		C_B		--	--	400	pF



Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

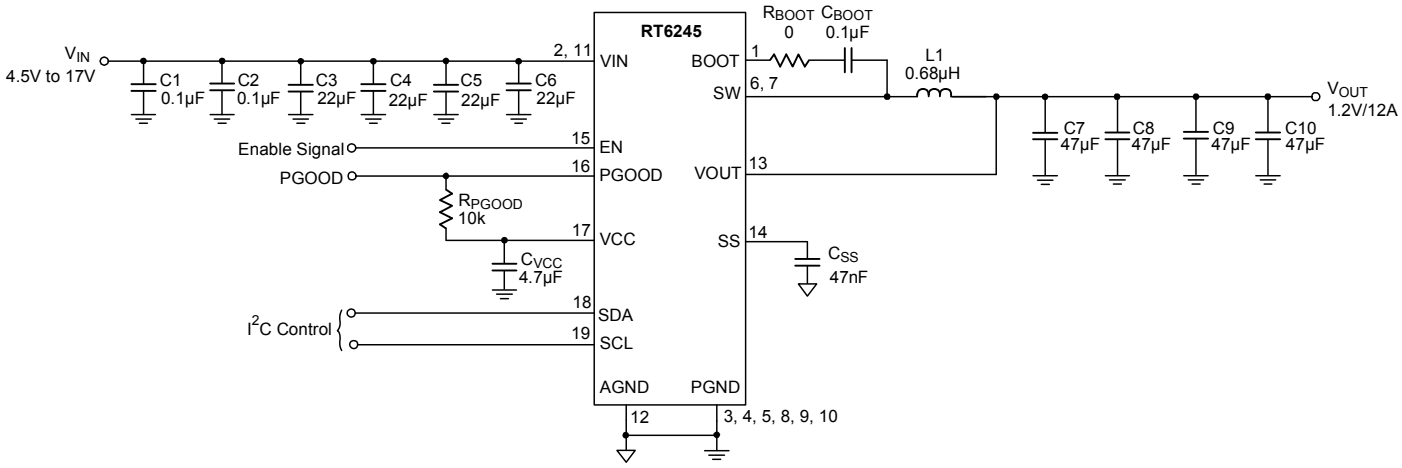
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a Four-layer Richtek Evaluation Board. θ_{JC} is measured at the top of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design and Characterized.

Typical Application Circuit



Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Table 1. Suggested Component Selections

V_{OUT} (V)	f_{SW} (kHz)	L1 (µH)	C_{OUT_MIN} (µF)	$C_{OUT\_TYPICAL}$ (µF)
0.6	400	0.47	88	188
	800	0.33	88	188
	1200	0.22	88	188
0.75	400	0.47	88	188
	800	0.33	88	188
	1200	0.22	88	188
0.9	400	0.68	88	188
	800	0.47	88	188
	1200	0.22	88	188
1.2	400	0.68	88	188
	800	0.47	88	188
	1200	0.22	88	188

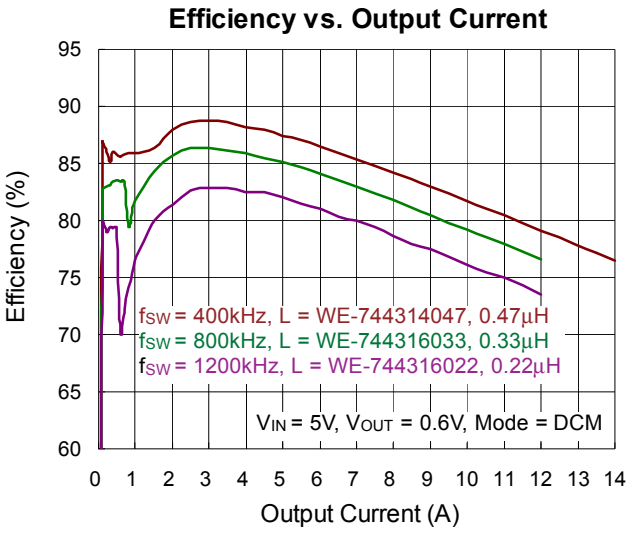
Table 2. Suggested Inductors for Typical Application Circuit

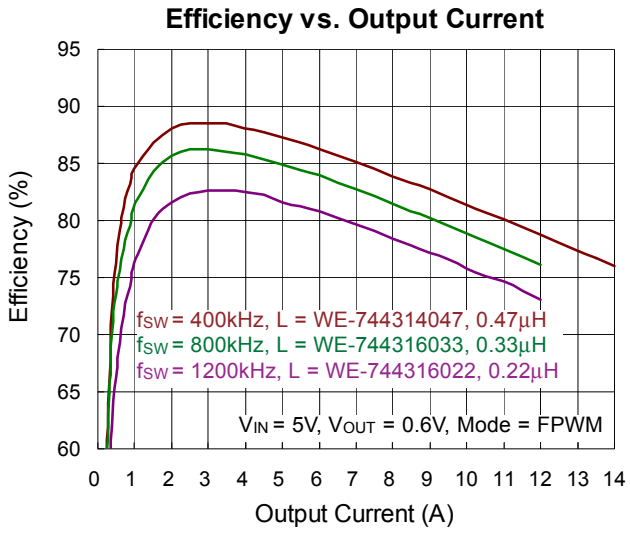
Inductance (μH)	Part No.	I_{SAT} (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.22	744316022	25	1.25	5.5 x 5.5 x 4.0	WE-HCI
0.33	744316033	20	1.925	5.5 x 5.5 x 4.0	WE-HCI
0.47	744314047	20	1.35	7.0 x 7.0 x 5.0	WE-HCI
0.68	744311068	20	3.1	7.0 x 7.0 x 4.0	WE-HCI

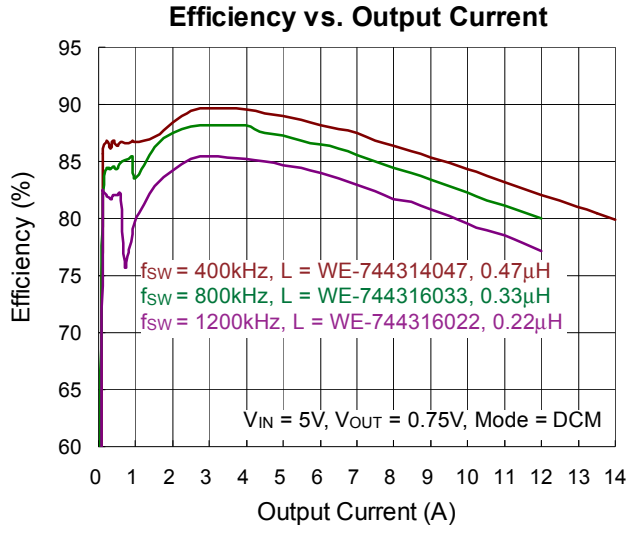
Table 3. Suggested Capacitor for Typical Application Circuit

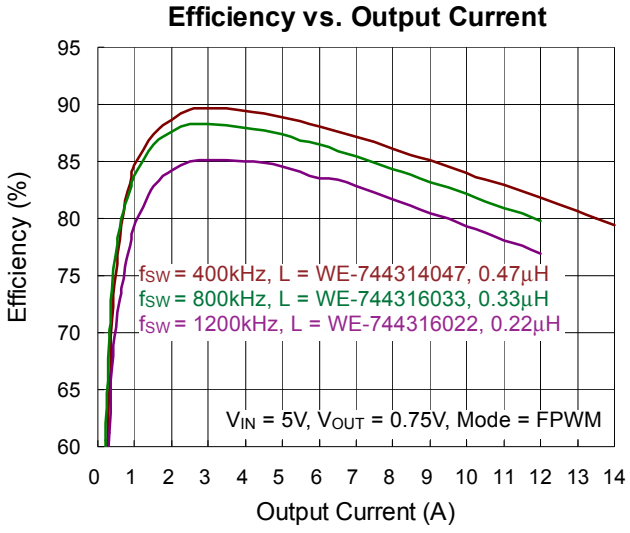
Capacitance (μF)	Part No.	Case Size	Component Supplier
22	GRM21BR61E226ME44	0805	Murata
47	GRM21BR61A476ME15	0805	Murata
4.7	GRM188R61E475KE11	0603	Murata
0.1	C1608X7R1H104K080AA	0603	TDK

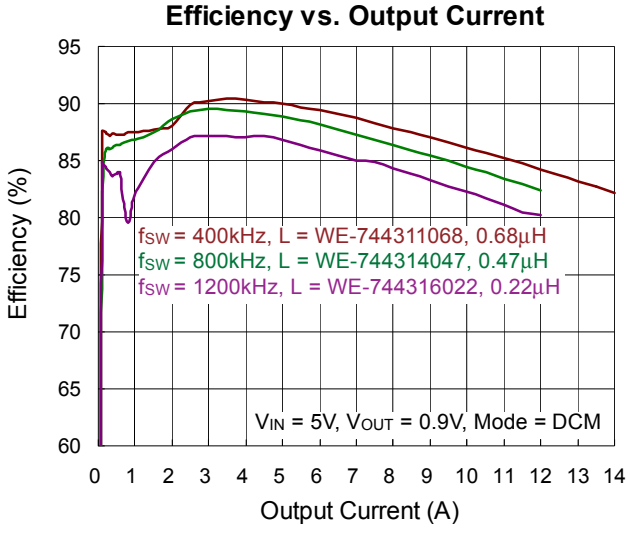
Typical Operating Characteristics

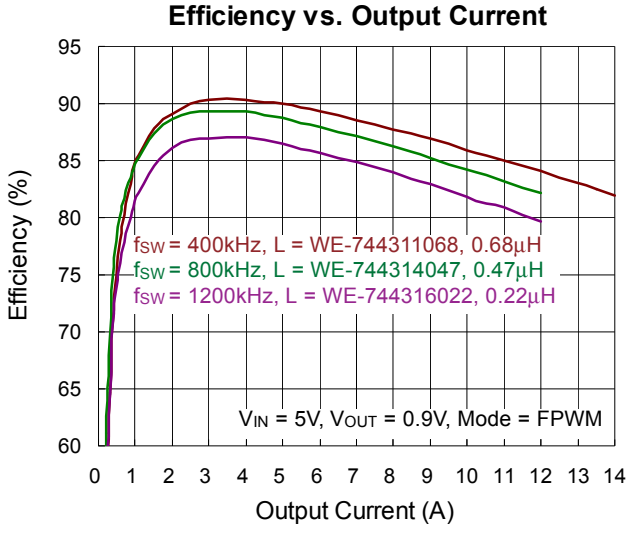




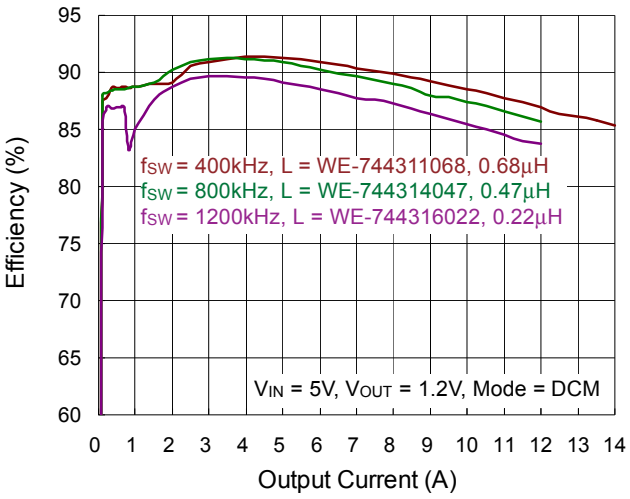




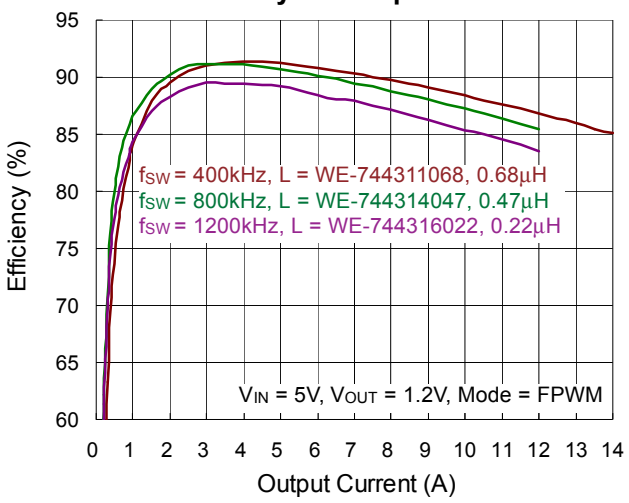




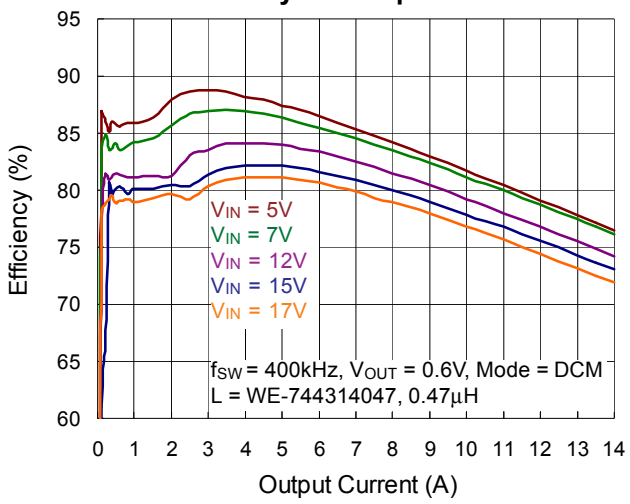
Efficiency vs. Output Current



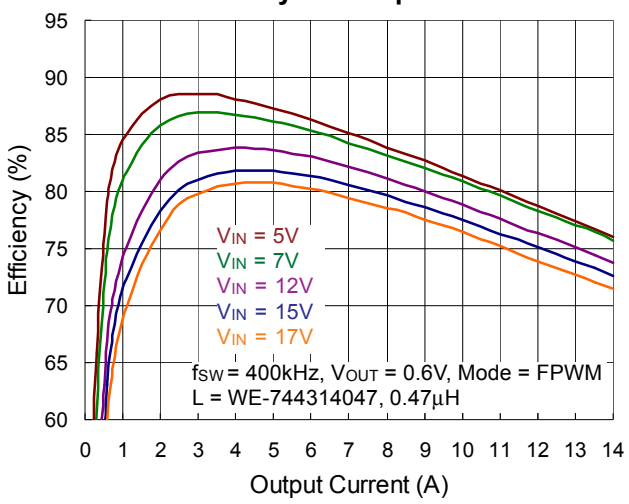
Efficiency vs. Output Current



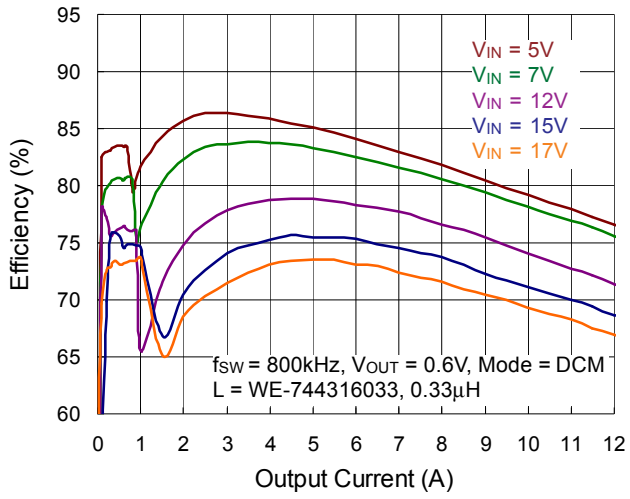
Efficiency vs. Output Current



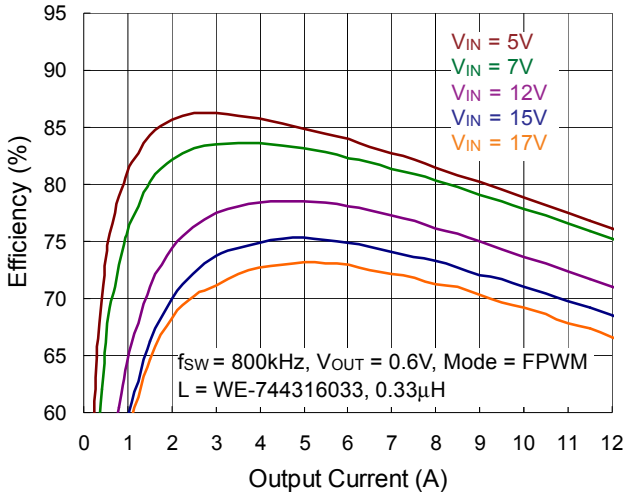
Efficiency vs. Output Current

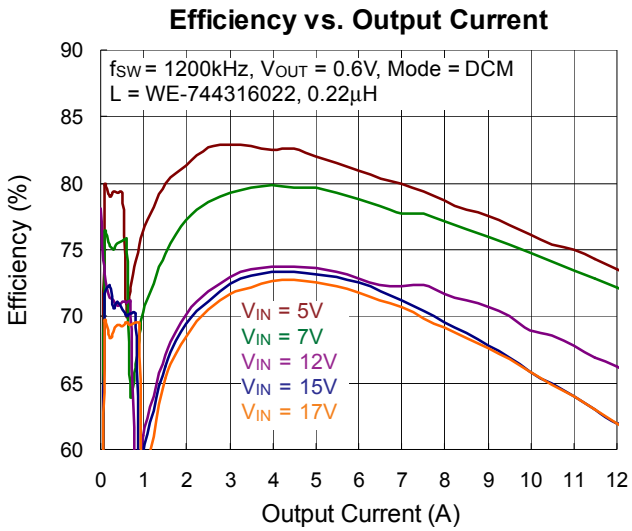


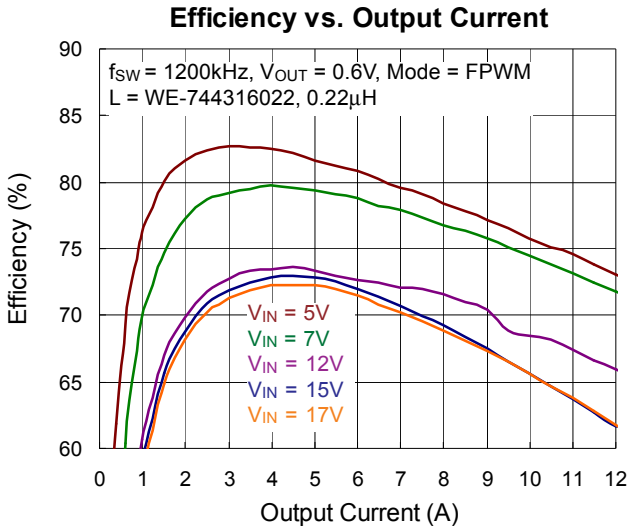
Efficiency vs. Output Current

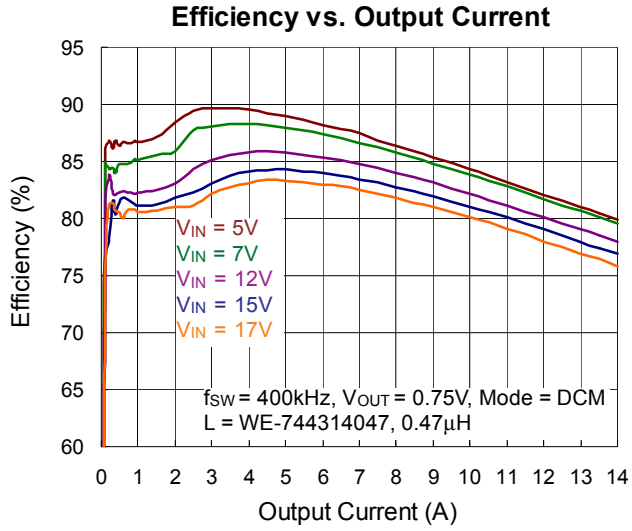


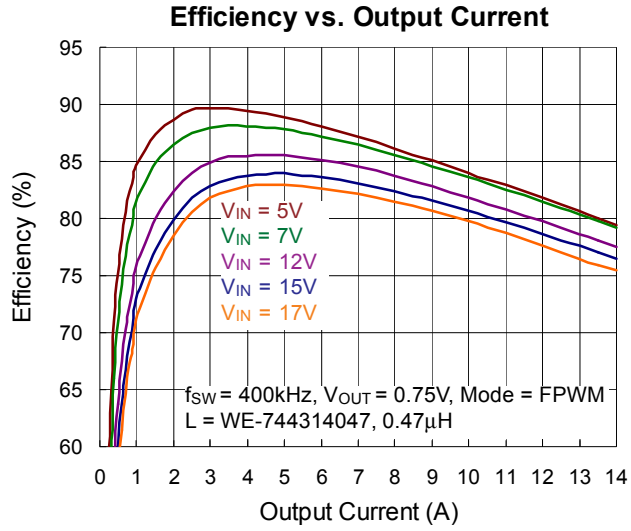
Efficiency vs. Output Current

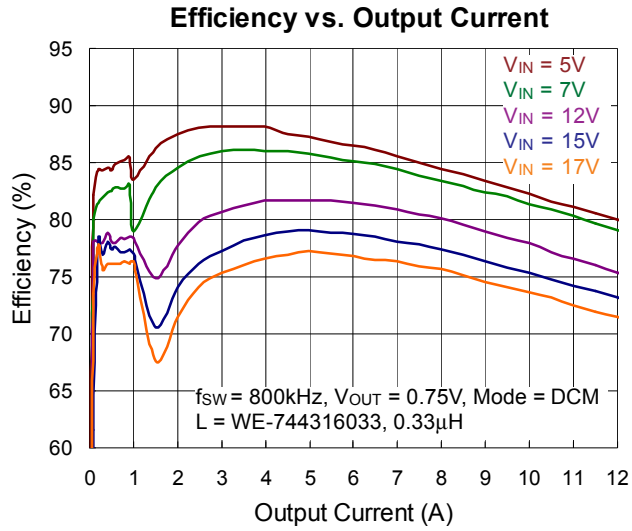


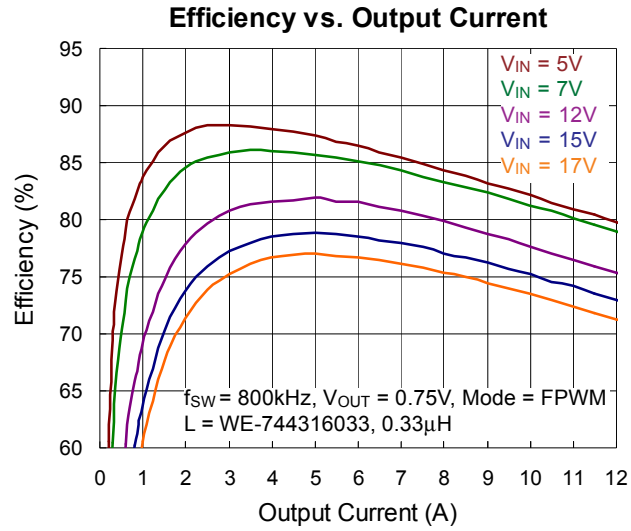




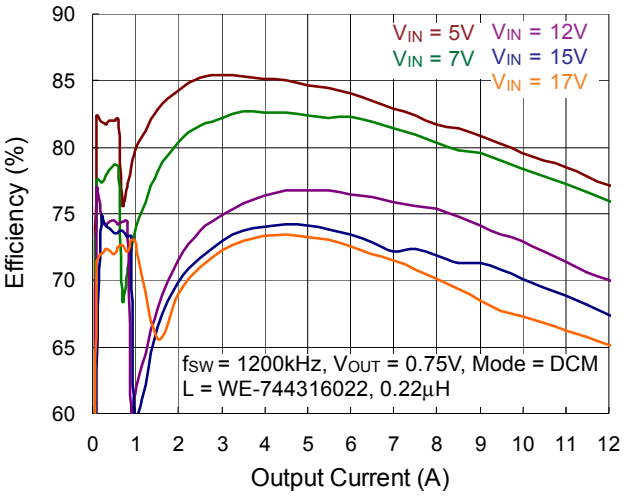




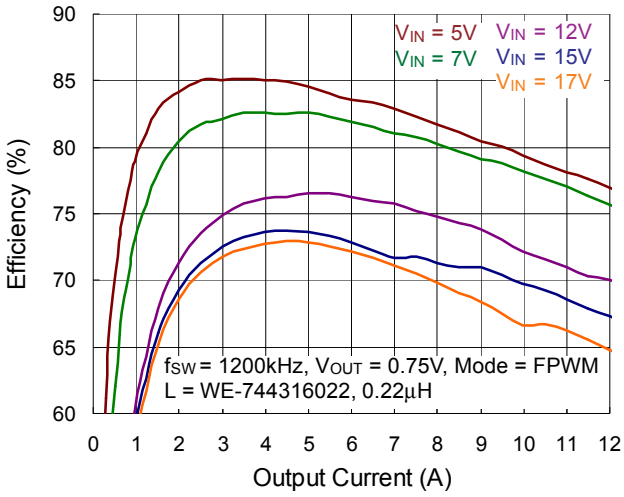




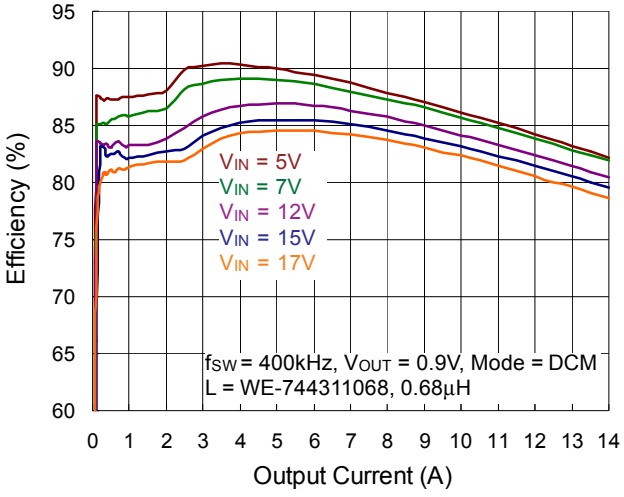
Efficiency vs. Output Current



Efficiency vs. Output Current



Efficiency vs. Output Current



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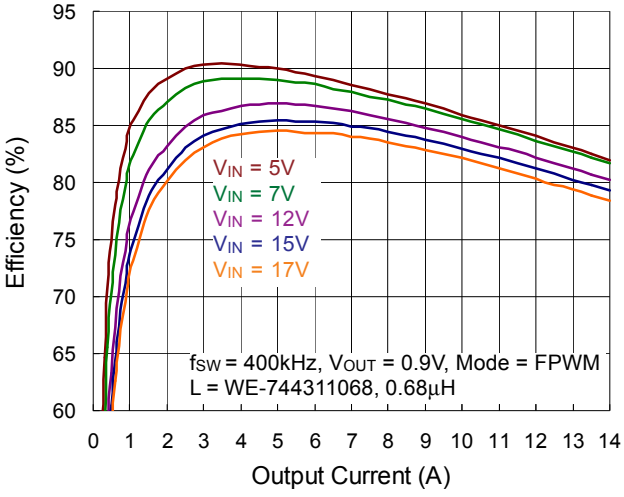

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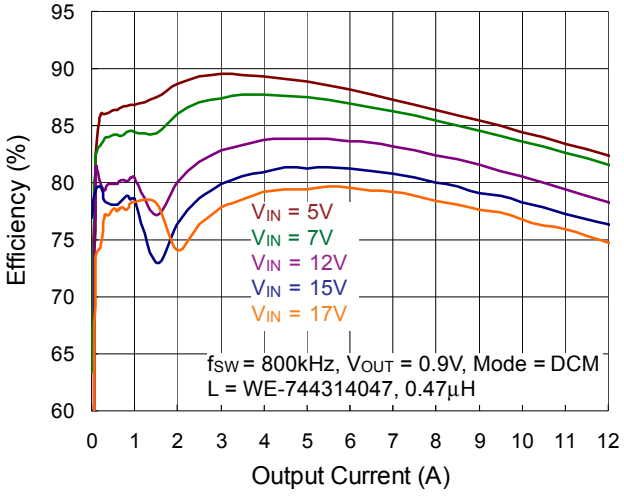

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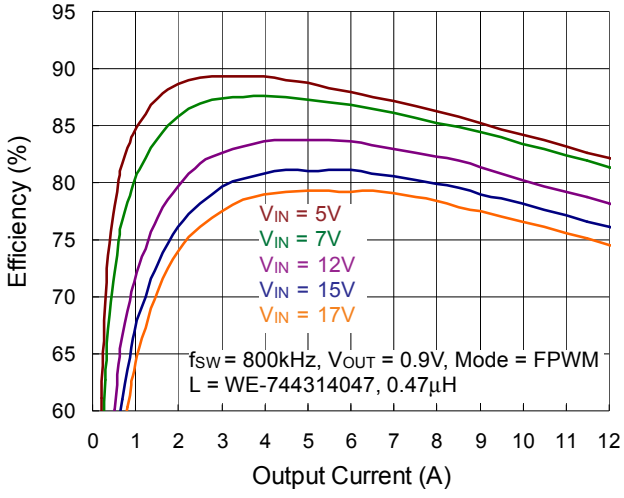
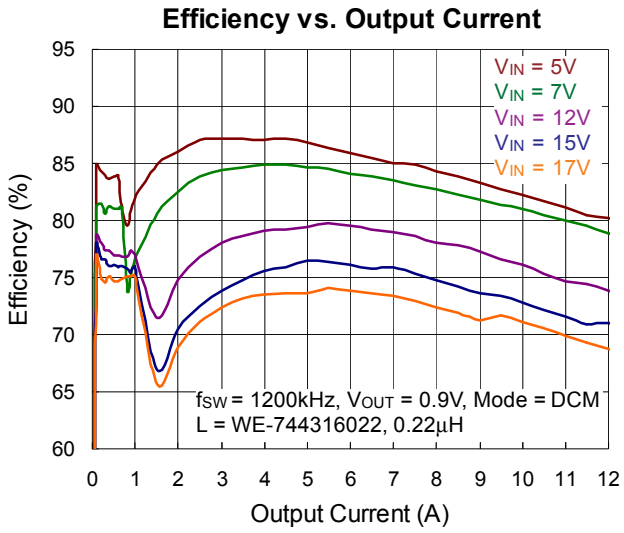
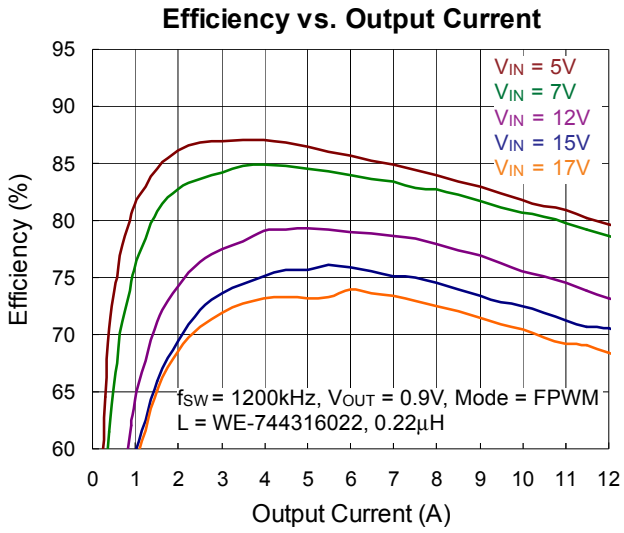
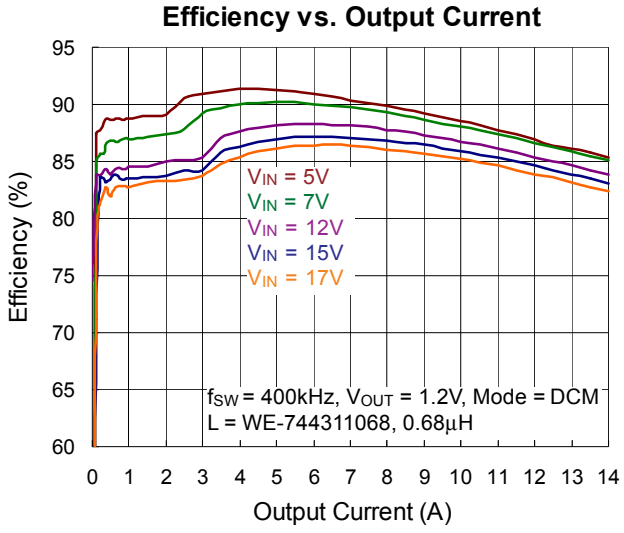
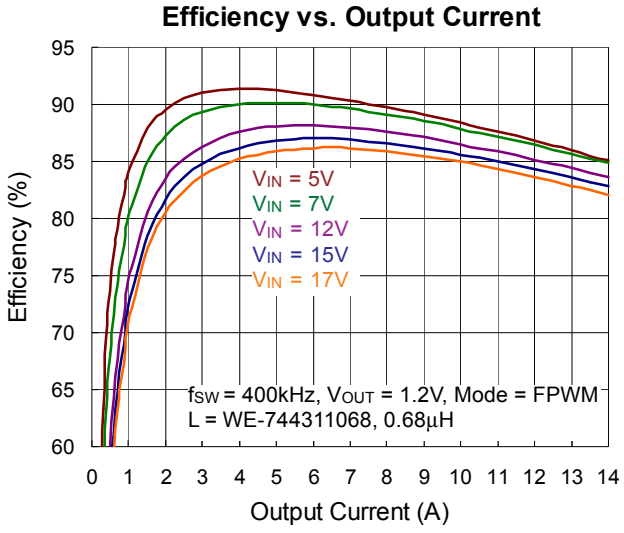
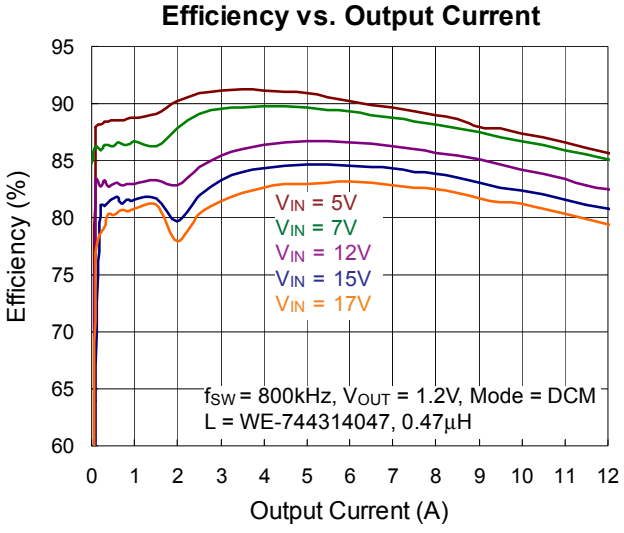


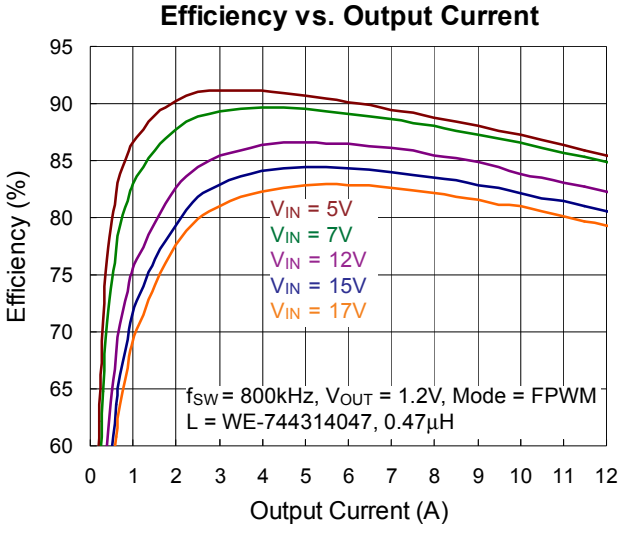




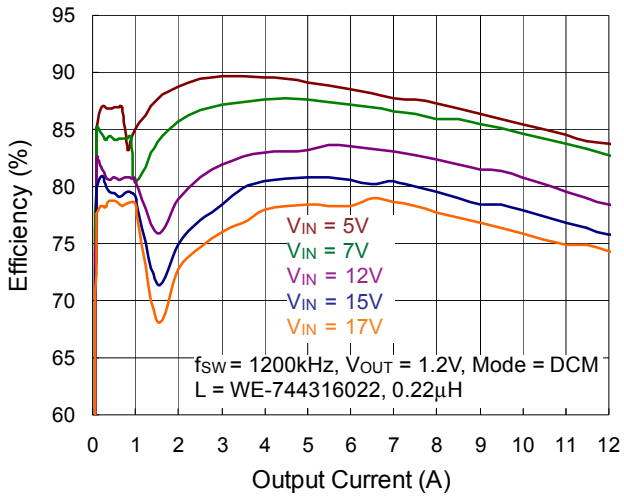




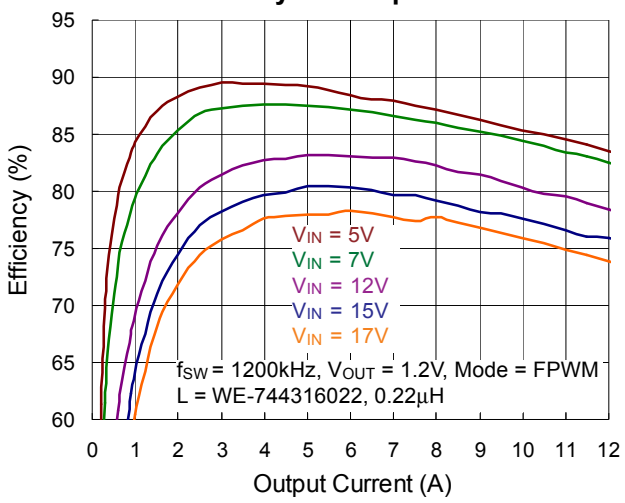




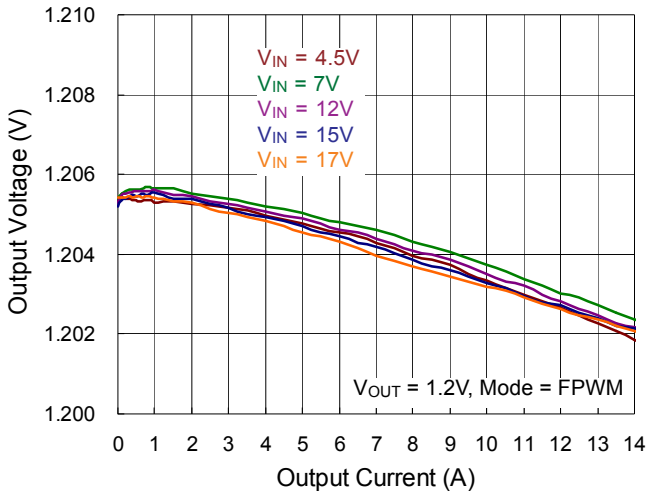
Efficiency vs. Output Current



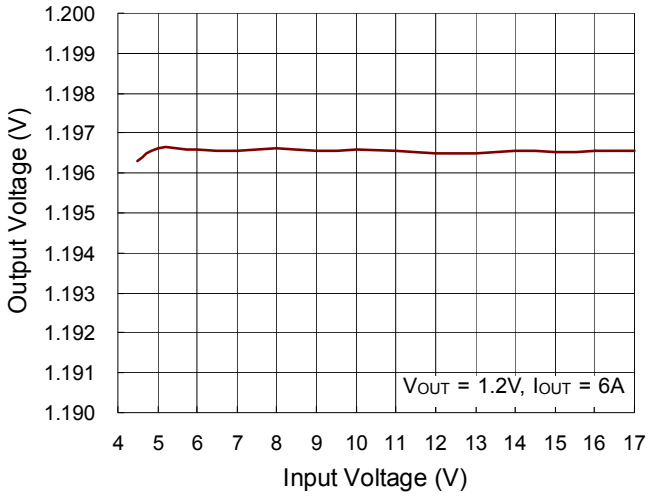
Efficiency vs. Output Current



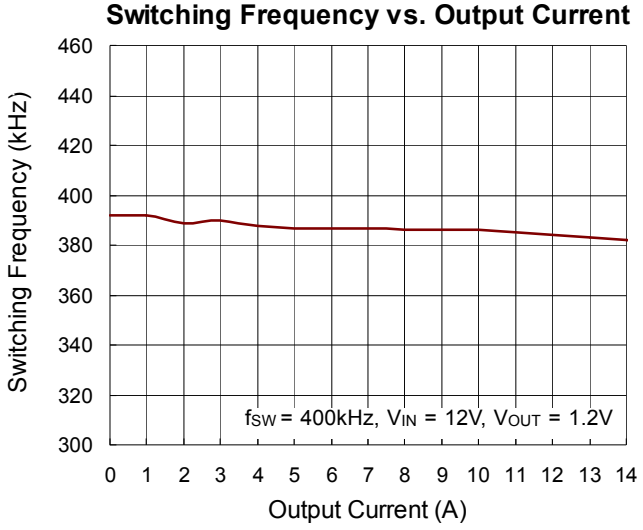
Output Voltage vs. Output Current



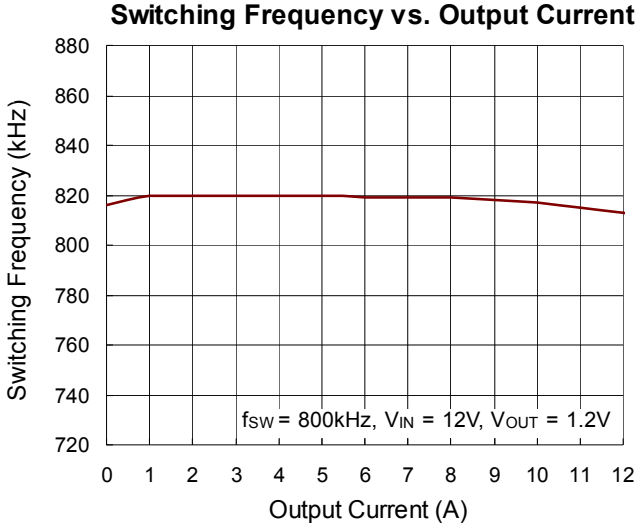
Output Voltage vs. Input Voltage



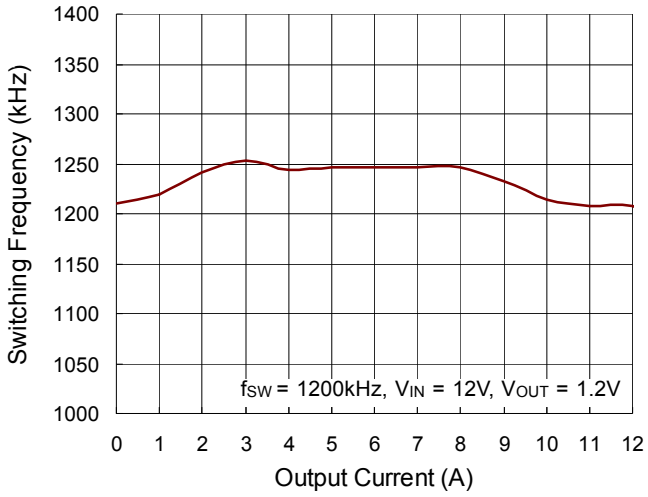
Switching Frequency vs. Output Current



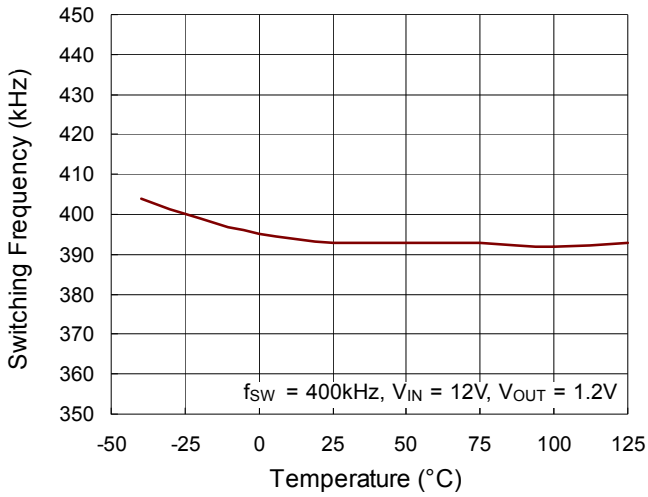
Switching Frequency vs. Output Current



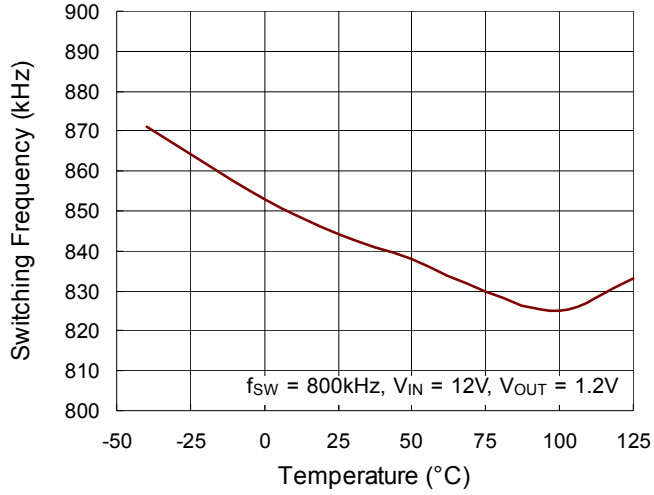
Switching Frequency vs. Output Current



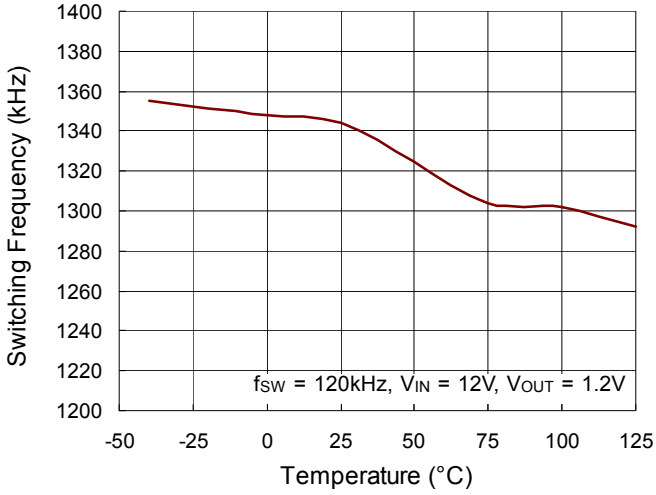
Switching Frequency vs. Temperature



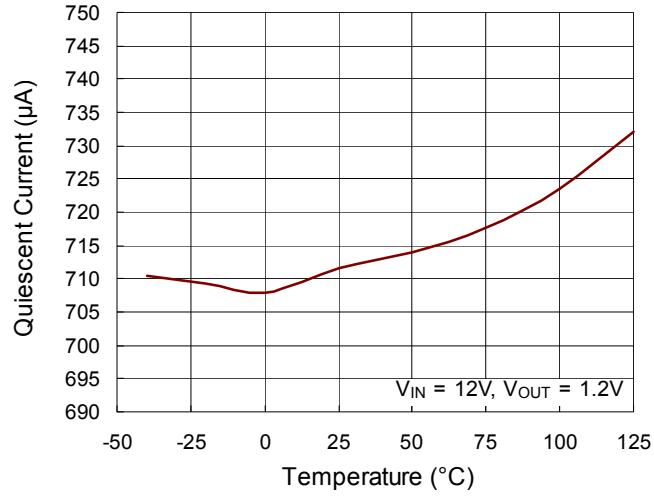
Switching Frequency vs. Temperature



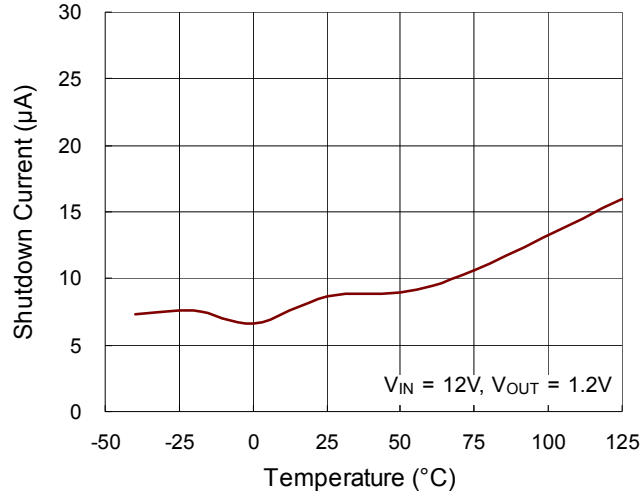
Switching Frequency vs. Temperature



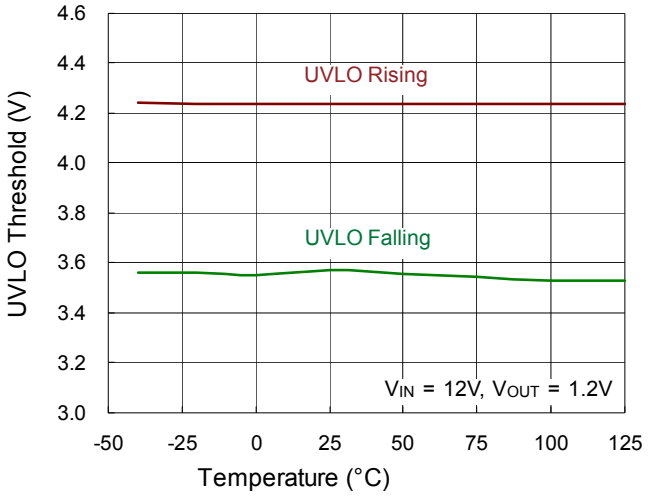
Quiescent Current vs. Temperature



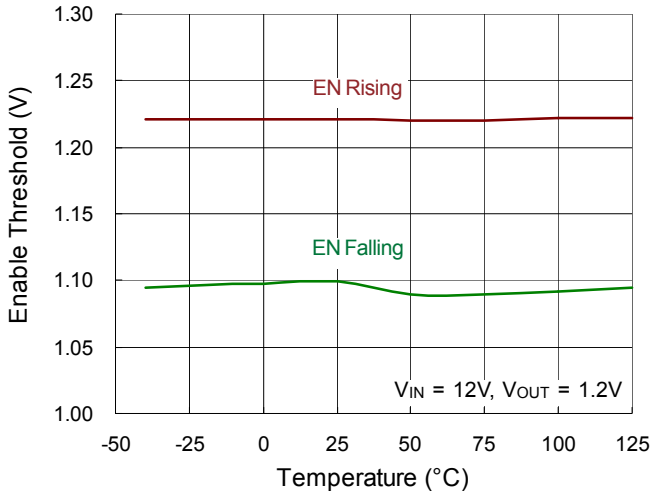
Shutdown Current vs. Temperature



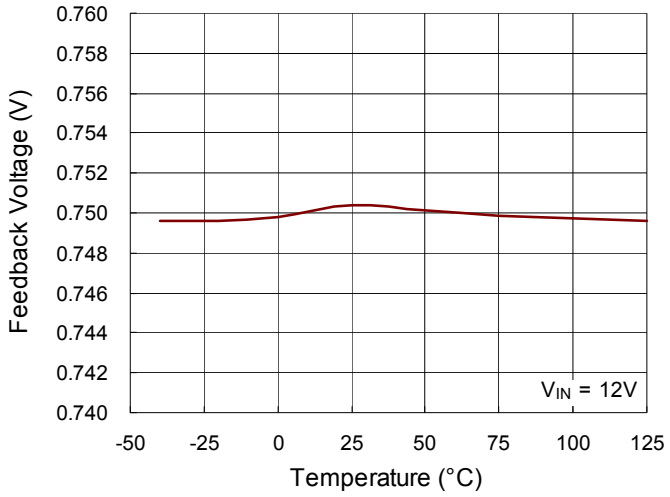
UVLO Threshold vs. Temperature



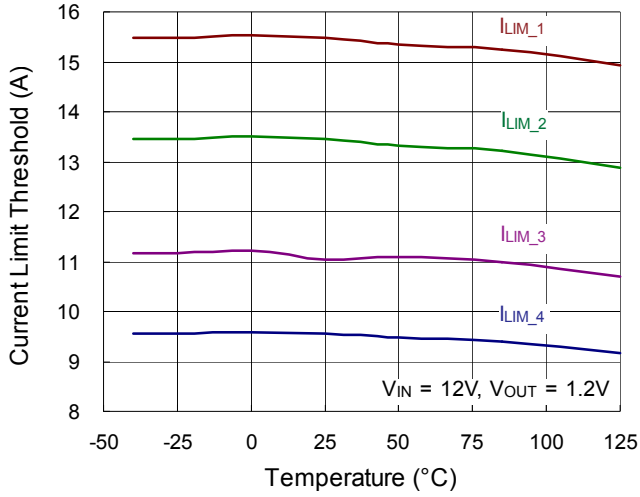
Enable Threshold vs. Temperature



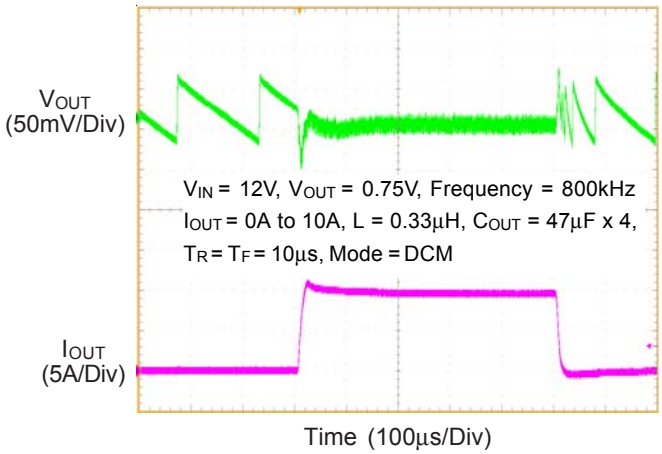
Feedback Voltage vs. Temperature



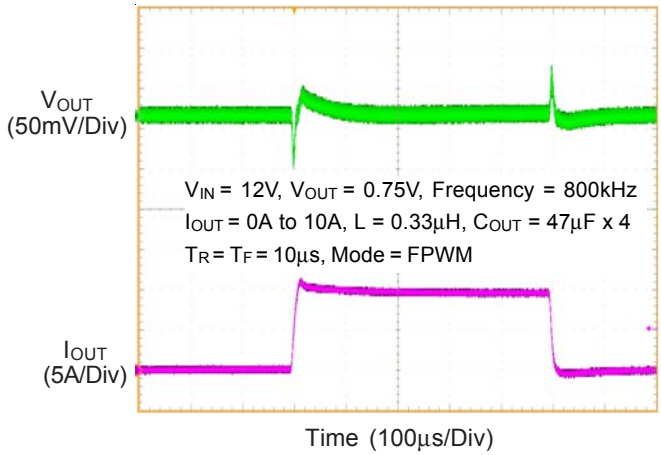
Current Limit Threshold vs. Temperature



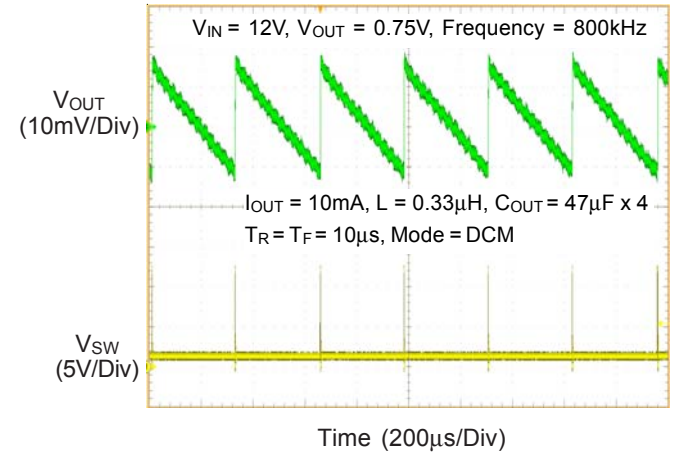
Load Transient Response



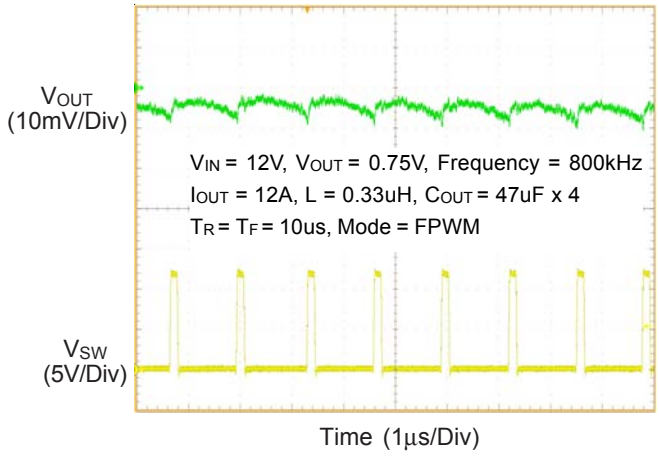
Load Transient Response



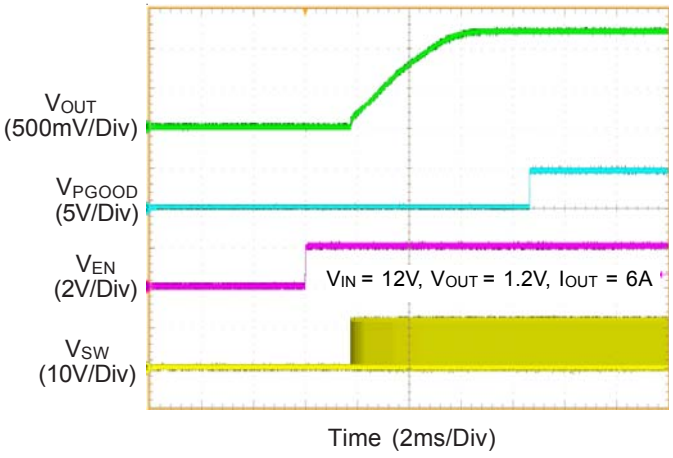
Output Ripple Voltage



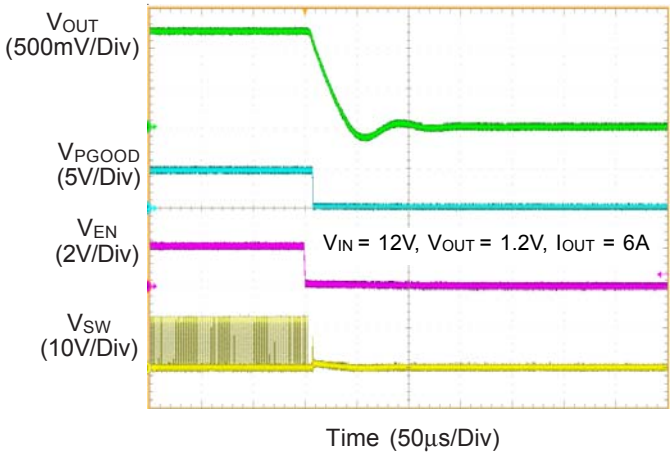
Output Ripple Voltage



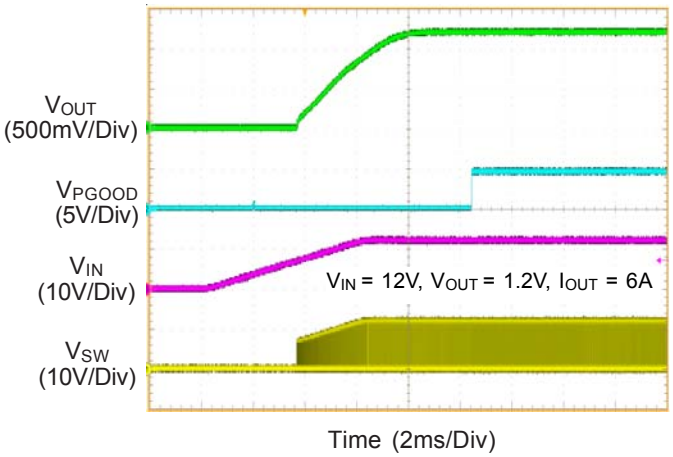
Power On from EN



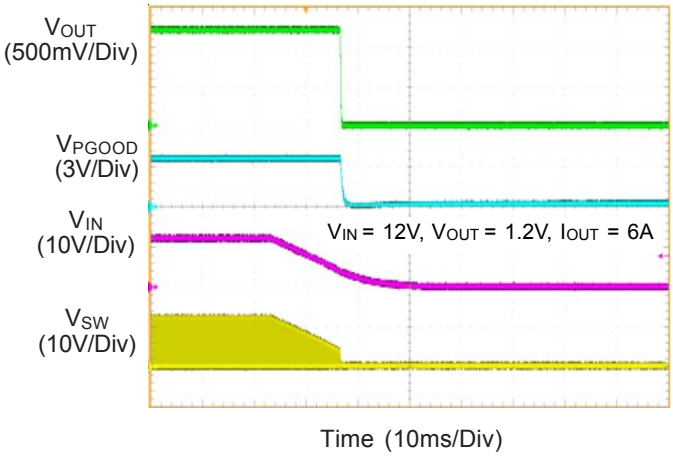
Power Off from EN



Power On from VIN



Power Off from VIN



Application Information

A general RT6245 application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the selection of the operating frequency and output voltage by I^2C setting. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT}, can be selected. Finally, the remaining optional external components can be selected for functions such as the EN and UVLO threshold, external soft-start time, and PGOOD.

I^2C Interface Function

The 7-bit address of the RT6245 with a WRITE operation bit can become an 8 bits "01101000" I^2C address byte.

Table 4 is the structure of the RT6245's Data Byte. Bit0 to Bit6 are the 7-bit code for one of 77 output voltage and special function. The bit7 is check-sum bit and Master should set this bit to be the Exclusive-OR of [Bit6:Bit0]. In other words, the sum is even. If not, the RT6245 will not send an ACK bit.

Table 4. Structure of the RT6245 Data Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ChkSum	D6	D5	D4	D3	D2	D1	D0

Table 5 shows special codes and relative function. Except shut down code, special codes are valid during the soft-start time. Shutdown code is valid after SSOK.

Table 5. Special Functions

Special Codes	Function	Description
01101111	OC = I_{LIM_4}	The over-current limit level selection. The switching frequency is set to 400kHz automatically when user sets over-current limit level to I_{LIM_1}.
11110000	OC = I_{LIM_1}	
01110001	OC = I_{LIM_2} (default)	
01110010	OC = I_{LIM_3}	
11110011	OT = 150°C (default)	To change the over-temperature protection level
01110100	OT = 130°C	
11110101	OT = 170°C	
11110110	Shut down code	To shut down and start up IC. The output voltage is reset to default value if the shutdown code is executed. When the IC stays in software shutdown mode, all of the write to V_{OUT} code are invalid except the special function.
01110111	Start up Code	
01111000	PGOOD fault delay time set to 0μs	When V_{OUT} is changed for a large step, especially at light load conditions, it maybe need a long setting time. It is easy to trig UV/OV function and it will cause fault power good signal. Users can use the special codes to set the PGOOD delay time to avoid undesired behavior.
11111001	PGOOD fault delay time set to 10μs (default)	
11111010	PGOOD fault delay time set to 20μs	
01111011	PGOOD fault delay time set to 40μs	
11100001	V_{OUT} slew rate = 12.5mV/1μs (default)	To change the V_{OUT} slew rate when it is controlled from low level voltage to high level voltage.
11100010	V_{OUT} slew rate = 12.5mV/2μs	
01100011	V_{OUT} slew rate = 12.5mV /3μs	
11100100	V_{OUT} slew rate = 12.5mV/4μs	
01100101	V_{OUT} slew rate = 12.5mV/5μs	
01100110	V_{OUT} slew rate = 12.5mV/6μs	
11100111	V_{OUT} slew rate = 12.5mV/7μs	
11101000	V_{OUT} slew rate = 12.5mV/8μs	
11111100	Switching frequency = 400kHz	Switching Frequency Selection
01111101	Switching frequency = 800kHz (default)	
01111110	Switching frequency = 1200kHz	

Output Voltage Programming

The output voltage can be set by I²C interface after the soft-start is finished. Master can send 8 bits data to control the V_{OUT} of the converter. The voltages can be selected from Table 6.

Table 6. VOUT Control Table

Code	Binary	V_{OUT} (V)	Code	Binary	V_{OUT} (V)	Code	Binary	V_{OUT} (V)
0	00000000	0.4375	26	10011010	0.7625	52	10110100	1.0875
1	10000001	0.45	27	00011011	0.775	53	00110101	1.1
2	10000010	0.4625	28	10011100	0.7875	54	00110110	1.1125
3	00000011	0.475	29	00011101	0.8	55	10110111	1.125
4	10000100	0.4875	30	00011110	0.8125	56	10111000	1.1375
5	00000101	0.5	31	10011111	0.825	57	00111001	1.15
6	00000110	0.5125	32	10100000	0.8375	58	00111010	1.1625
7	10000111	0.525	33	00100001	0.85	59	10111011	1.175
8	10001000	0.5375	34	00100010	0.8625	60	00111100	1.1875
9	00001001	0.55	35	10100011	0.875	61	10111101	1.2
10	00001010	0.5625	36	00100100	0.8875	62	10111110	1.2125
11	10001011	0.575	37	10100101	0.9	63	00111111	1.225
12	00001100	0.5875	38	10100110	0.9125	64	11000000	1.2375
13	10001101	0.6	39	00100111	0.925	65	01000001	1.25
14	10001110	0.6125	40	00101000	0.9375	66	01000010	1.2625
15	00001111	0.625	41	10101001	0.95	67	11000011	1.275
16	10010000	0.6375	42	10101010	0.9625	68	01000100	1.2875
17	00010001	0.65	43	00101011	0.975	69	11000101	1.3
18	00010010	0.6625	44	10101100	0.9875	70	11000110	1.3125
19	10010011	0.675	45	00101101	1	71	01000111	1.325
20	00010100	0.6875	46	00101110	1.0125	72	01001000	1.3375
21	10010101	0.7	47	10101111	1.025	73	11001001	1.35
22	10010110	0.7125	48	00110000	1.0375	74	11001010	1.3625
23	00010111	0.725	49	10110001	1.05	75	01001011	1.375
24	00011000	0.7375	50	10110010	1.0625	76	11001100	1.3875
25	10011001	0.75	51	00110011	1.075	--	--	--

Switching Frequency Selection

Switching Frequency, current limit are set by the I²C interface. Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold and increases the AC losses in the inductor. To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs.

The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} = 200mV for typical application (V_{IN} > 7V)

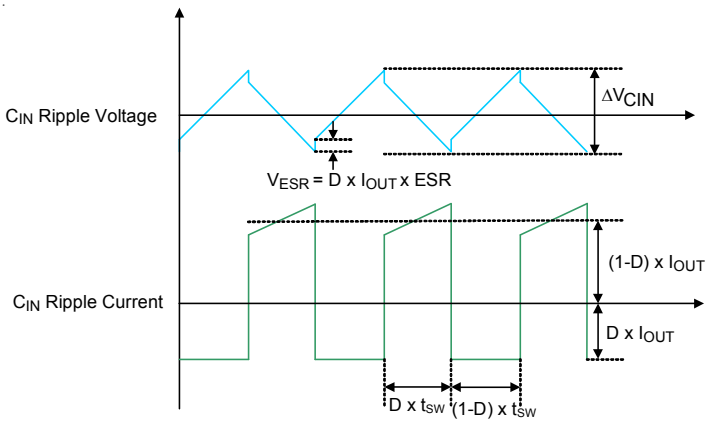


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT6245 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, two small ceramic capacitors of 0.1μF should be placed close to the part; one at the VIN1/PGND1 pins and a second at VIN2/PGND2 pins. These capacitors should be 0402 or 0603 in size.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below :

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by :

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as :

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Internal VCC Regulator

Good bypassing at VCC pin is necessary to supply the high transient currents required by the power MOSFET gate drivers. Place a low ESR MLCC capacitor with capacitance ≥ 4.7μF (or effective capacitance ≥ 1.5μF) as close as possible to VCC pin, the rated voltage of C_{VCC} should be higher than 10V with 0603 or 0805 in size.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect

VCC to provide power to other devices or loads.

HSFET Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between BOOT pin and SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage equal to approximately V_{VCC} each time the LSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications, a 0.1µF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

It is recommended to add an external bootstrap Schottky diode between an external 5V voltage supply and the BOOT pin as shown in Figure 5 to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage, V_{IN}, is below 5V. The bootstrap Schottky diode can be a low-cost one, such as BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6245. Note that the BOOT voltage V_{BOOT} must be lower than 5.5V. The Figure 6 shows the efficiency with/without an external 5V supply.

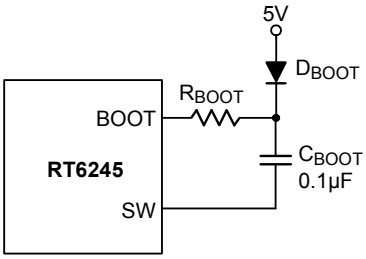


Figure 5. External Bootstrap Diode and Resistor at the BOOT Pin

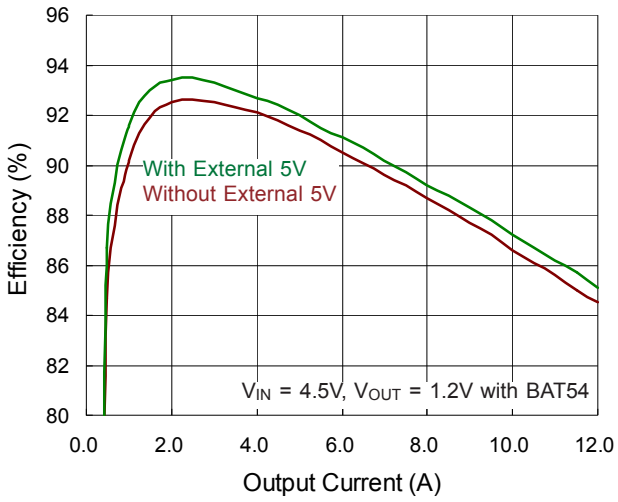


Figure 6. Efficiency Comparison with/without External 5V Supply.

EMI issue is worse when the switch is turned on rapidly due to high di/dt noises. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 20Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 5, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching, and it stops switching when the EN pin voltage falls below the turn-off threshold (V_{ENL}). The EN pin of the RT6245 has internally pull-up with current source. Figure 7. shows an example if an enable time delay is required :

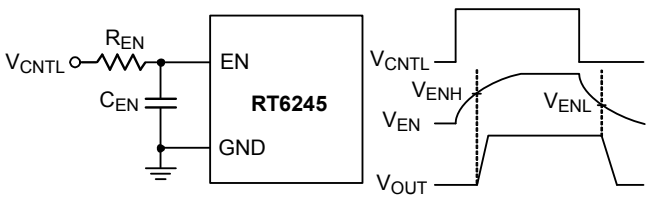


Figure 7. Enable Timing Control

Figure 8 shows examples of configurations for driving the EN pin from logic.

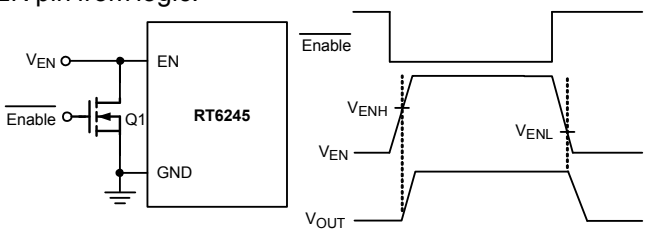


Figure 8. Logic Control for the EN Pin

Figure 9 shows the internal block of RT6245 EN pin. A resistor divider between VIN and EN can set a different turn-on (V_{START}) and turn-off thresholds (V_{STOP}) respectively. The EN pin has a pull-up current I_{ENP1} that sets the default state of the pin when it is floating. This current increases to I_{ENP2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set as below :

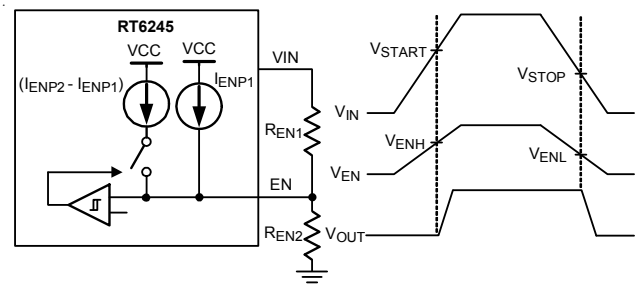


Figure 9. Adjustable VIN UVLO

$$R_{EN1} = \frac{V_{START} \times \frac{V_{ENL}}{V_{ENH}} - V_{STOP}}{I_{ENP1}\left(1 - \frac{V_{ENL}}{V_{ENH}}\right) + (I_{ENP2} - I_{ENP1})}$$

$$R_{EN2} = \frac{R_{EN1} \times V_{ENH}}{V_{START} + (R_{EN1} \times I_{ENP1}) - V_{ENH}}$$

Where

I_{ENP2} = 4.2μA

I_{ENP1} = 2μA

V_{ENL} = 1.104V

V_{ENH} = 1.225V

Thermal Considerations

In many applications, the RT6245 does not generate much heat due to its high efficiency and low thermal resistance of its flip-chip VQFN-19L 3.5x3.5 (FC) package. However, in applications which the RT6245 is running at a high ambient temperature, high input voltage and high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 160°C, the RT6245 stop switching the power MOSFETs until the temperature drops about 15°C cooler.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 125°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Table 7 shows the simulated thermal resistance of the RT6245 which is mounted on PCB with difference tack-up and copper thickness. The layout of thermal model refers to the RT6245 evaluation board.

Table 7. Simulated Thermal Resistance with Difference Tack-Up and Copper Thickness

Simulated θ_{JA}	θ_{JA} (°C/W)
4 Layer with 2oz copper	28
4 Layer with 1oz copper	40
2 Layer with 1oz copper	52.5

As an example, consider the case when the RT6245 is used in applications where V_{IN} = 12V, I_{OUT} = 12A, f_{SW} = 800kHz, V_{OUT} = 1.2V.

The efficiency at 1.2V, 12A is 84% by using WE-744311068 (0.68µH, 3.1mΩ DCR) as the inductor and measured at room temperature. The core loss 0.125W can be obtained from its website. In this case, the power dissipation of the RT6245 is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 2.17W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 33.6°C/W by using the RT6245 evaluation board with 4 layers PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

$$T_J = 2.17W \times 33.6°C/W + 25°C = 98°C$$

Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RT6245 :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- VIN pins should have equal input capacitors on each side of IC. Place these input capacitors as close to VIN pins as possible.
- Place the VCC decoupling capacitor, C_{VCC}, as close to VCC pin as possible.
- Place bootstrap capacitor, C_{BOOT}, as close to IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RT6245 to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Connect the output voltage sense network behind via of output capacitor.
- The ground connection between analog ground and power ground should be close to IC to minimum the ground current loops. If there is only one ground plane, it should keep enough isolation between analog return signals and high power signals.

Figure 10 is the layout example which uses 3"x3" (76mm x76mm), four-layer PCB with 2oz copper.

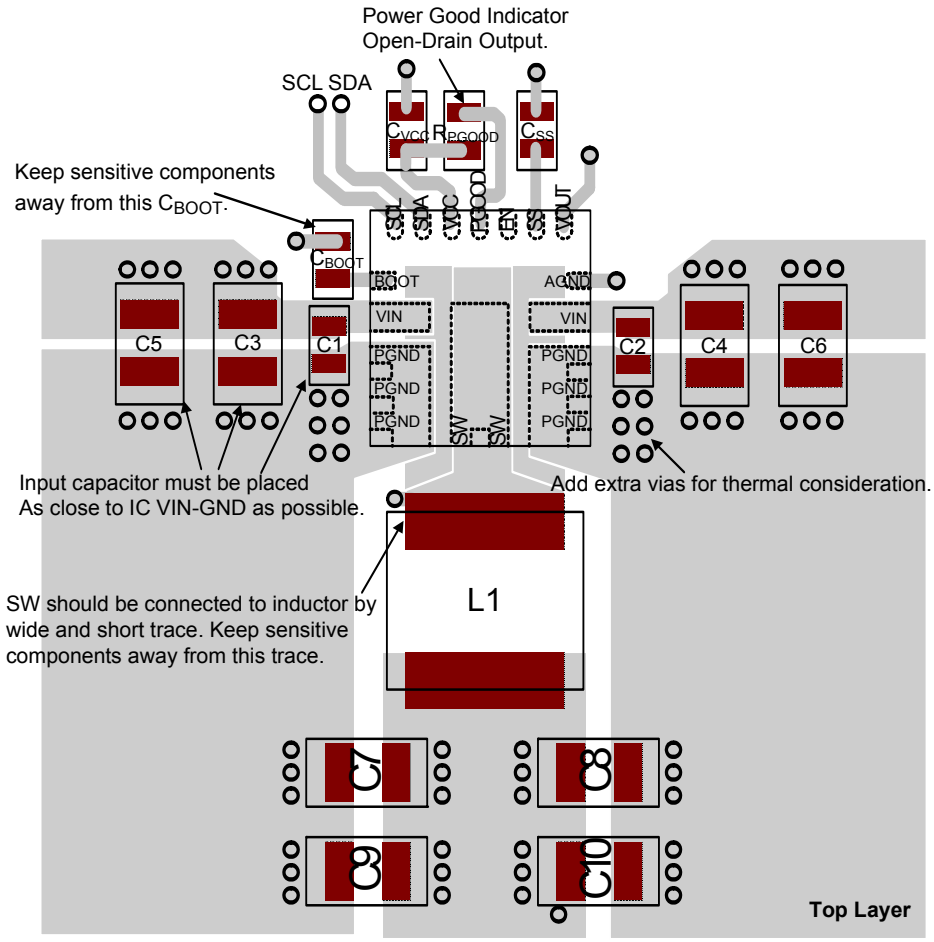
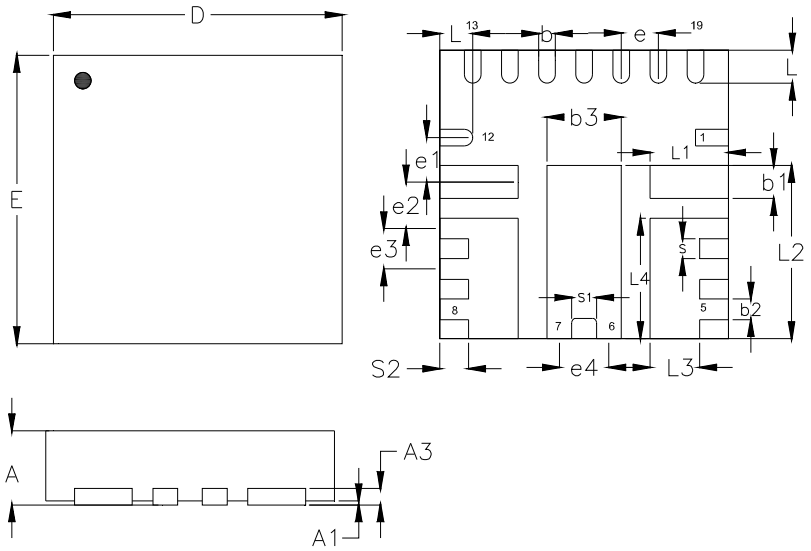


Figure 10. Layout Guide (Top Layer)

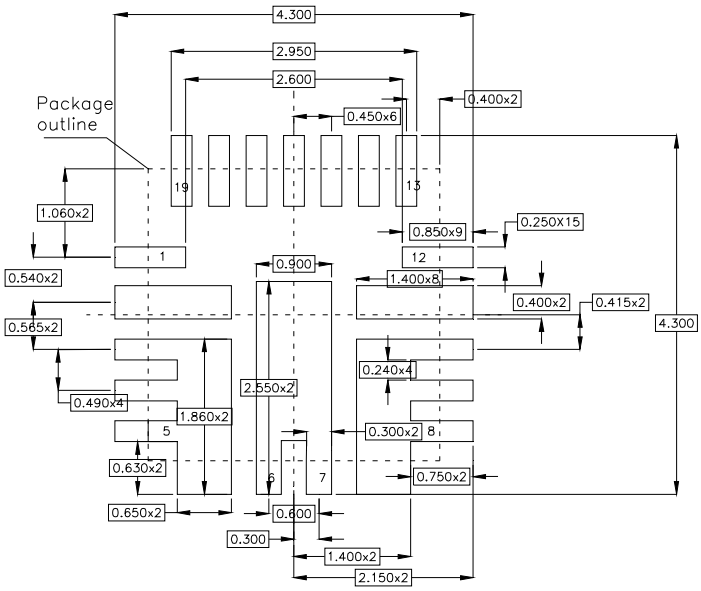
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
b1	0.350	0.450	0.014	0.018
b2	0.200	0.300	0.008	0.012
b3	0.850	0.950	0.033	0.037
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.450		0.018	
e1	0.540		0.021	
e2	0.565		0.022	
e3	0.490		0.019	
e4	0.600		0.024	
L	0.350	0.450	0.014	0.018
L1	0.900	1.000	0.035	0.039
L2	2.050	2.150	0.081	0.085
L3	0.550	0.650	0.022	0.026
L4	1.410	1.510	0.056	0.059
S	0.190	0.290	0.007	0.011
S1	0.250	0.350	0.010	0.014
S2	0.300	0.400	0.012	0.016

V-Type 19L QFN 3.5x3.5 Package

Footprint Information



Package	Number of Pin	Tolerance
V/W/U/XQFN3.5x3.5-19(FC)	19	±0.05

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