2.4A, 36V, 100kHz Asynchronous Step-Down Converter with Load Line Compensation

General Description
The RT6266 is a high-efficiency, monolithic asynchronous step-down DC/DC converter that can deliver up to 2.4A output current from a 7.5V to 36V input supply. The RT6266’s current mode architecture with internal compensation is optimized for 5V car charger application over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT6266 also provides output over voltage protection output under voltage protection and thermal shutdown protection. The low current (<3μA) shutdown mode provides output disconnect, enabling easy power management in battery-powered systems. The RT6266 is available in a SOP-8 (Exposed Pad) package.

Features
- ±2% High Accuracy Feedback Voltage
- 7.5V to 36V Input Voltage Range
- 2.4A Continuous Output Current (2.7A Peak)
- CC/CV Mode Control
- Adjustable Load Line Compensation
- Short Circuit Protection
- Integrated N-MOSFET Switches
- Current Mode Control
- Fixed Frequency Operation : 100kHz
- Programmable Output Current Limit
- 110mΩ Internal Power MOSFET Switch
- Low EMI signature
- Up to 95% Efficiency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Output Under Voltage Protection
- Thermal Shutdown Protection

Applications
- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers
- DC/DC Converters with Current Limited

Marking Information
RT6266
GSPYMDNN
RT6266GSP : Product Number
YMDNN : Date Code

Ordering Information
RT6266
Package Type
SP: SOP-8(Exposed Pad-Option 2)
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :
Richtek products are :
> RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
> Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit
# Pin Configurations

( TOP VIEW )

## Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td>Input Supply Voltage, 7.5V to 36V. Must bypass with a suitably large ceramic capacitor.</td>
</tr>
<tr>
<td>2</td>
<td>BOOT</td>
<td>Bootstrap for High-Side Gate Driver. Connect 0.1µF or greater ceramic capacitor from BOOT to SW pins.</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td>Enable Input Pin. A logic high enables the converter; a logic low forces the RT6266 into shutdown mode reducing the supply current to less than 3µA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.</td>
</tr>
<tr>
<td>4</td>
<td>FB</td>
<td>Feedback Input Pin. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an external resistive voltage divider. For an adjustable output, an external resistive divider is connected to this pin.</td>
</tr>
<tr>
<td>5</td>
<td>CSN</td>
<td>Current Sense Negative Input. It is used for load current limiting and load line drop compensation.</td>
</tr>
<tr>
<td>6</td>
<td>CSP</td>
<td>Current Sense Positive Input. It is used for load current limiting and load line drop compensation.</td>
</tr>
<tr>
<td>7, 9 (Exposed Pad)</td>
<td>GND</td>
<td>Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. (Connect the exposed pad to Pin 7)</td>
</tr>
<tr>
<td>8</td>
<td>SW</td>
<td>Switch Output -- Connect to external L-C filter and Schottky diode.</td>
</tr>
</tbody>
</table>
Operation

The RT6266 is a constant frequency, current mode asynchronous step-down converter with CC and CV control. In normal operation, the high side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the N-MOSFET is turned off, the inductor current conducts through the external diode.

Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal ($V_{FB}$) with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the error amplifier’s output voltage then rises to allow higher inductor current to match the load current.

Oscillator

The internal oscillator runs at fixed frequency 100kHz. In short circuit condition, the frequency is reduced to 20kHz for low power consumption.

Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high side gate driver.

Enable

The converter is turned on when the EN pin is higher than 1.4V and turned off when the EN pin is lower than 0.4V. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
Soft-Start (SS)
An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 3.5ms.

Output Line Drop Compensation
If the trace from RT6266 output terminator to the load is too long, there will be a voltage drop on the long trace which is variable with load current. RT6266 is capable of compensating the output voltage drop to keep a constant voltage at load, whatever the load current is. The output voltage is compensated by feeding a current to the top feedback resistance R1. The load line compensation gain can be programmed according to $R_{\text{SENSE}}$ and $R_{\text{trace}}$ values.

$$I_{\text{OUT}} \times R_{\text{SENSE}} \times 20 \mu \Omega \times R_1 = I_{\text{OUT}} \times R_{\text{trace}}$$

$$R_1 = \frac{R_{\text{trace}}}{20 \mu \Omega \times R_{\text{SENSE}}}$$

Internal Current Limit Protection
When the external $R_{\text{SENSE}}$ is too small and the external peak current is higher than 4.4A, the high-side switch will turn off immediately and then turn at the next clock cycle. The inductor's peak current will be limited at 4.4A by internal current limit.

Output Short-Circuit Protection
When $V_{\text{OUT}}$ is short ($V_{\text{FB}} < 0.3V$), the short-circuit protection function can be started that restart the regulator cycle by cycle. The cycle time is set by the driver internally. The internal current limit time is $t_1$ and the regulator off time is $t_2$. The typically $t_1 = 5ms$, $t_2 = 200ms$.

Under Voltage Lockout (UVLO)
To avoid mis-operation at low input voltage, when input voltage falls below 6.2V, and under voltage lockout is induced and the device is disabled.

Thermal Shutdown
The over temperature protection function will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the converter will automatically resume switching.
Absolute Maximum Ratings  (Note 1)

- Supply Input Voltage: -0.3V to 40V
- Switch Voltage, SW: -0.3V to (Vin + 0.3V)
- VBOOT - VSW: -0.3V to 6V
- EN, FB, CSP, CSN: -0.3V to 6V
- Power Dissipation, PD @ TA = 25°C: 2.041W
- Package Thermal Resistance  (Note 2)
  - SOP-8 (Exposed Pad), θJA: 49°C/W
  - SOP-8 (Exposed Pad), θJC: 15°C/W
- Lead Temperature (Soldering, 10 sec.): 260°C
- Junction Temperature: 150°C
- Storage Temperature Range: -65°C to 150°C
- ESD Susceptibility  (Note 3)
- HBM Susceptibility: 2kV

Recommended Operating Conditions  (Note 4)

- Supply Input Voltage: 7.5V to 36V
- Ambient Temperature Range: -40°C to 85°C
- Junction Temperature Range: -40°C to 125°C

Electrical Characteristics

(VIN = 12V, VOUT = 5V, TA = 25°C, Load Current = 0A, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT OVP Detect Voltage</td>
<td>VOVP</td>
<td>Normal Operation.</td>
<td>--</td>
<td>5.8</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>VOUT OVP Hysteresis</td>
<td>ΔVOVP</td>
<td>Normal Operation.</td>
<td>--</td>
<td>0.3</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>ISD</td>
<td>VEN = 0V</td>
<td>--</td>
<td>1.5</td>
<td>3</td>
<td>μA</td>
</tr>
<tr>
<td>Supply Current</td>
<td>IQ</td>
<td>VEN = 3V, VFB = 0.9V</td>
<td>--</td>
<td>0.8</td>
<td>1.2</td>
<td>mA</td>
</tr>
<tr>
<td>Feedback Voltage (*)</td>
<td>VFB</td>
<td>7.5V ≤ VIN ≤ 36V</td>
<td>0.784</td>
<td>0.8</td>
<td>0.816</td>
<td>V</td>
</tr>
<tr>
<td>High-Side Switch On-Resistance</td>
<td>RDS(ON),U</td>
<td>Normal Operation.</td>
<td>--</td>
<td>100</td>
<td>--</td>
<td>mΩ</td>
</tr>
<tr>
<td>Low-Side Switch On-Resistance</td>
<td>RDS(ON),L</td>
<td>Normal Operation.</td>
<td>--</td>
<td>15</td>
<td>--</td>
<td>Ω</td>
</tr>
<tr>
<td>High-Side Switch Leakage Current</td>
<td>ISWLEAK</td>
<td>VEN = 0V, VSW = 0V</td>
<td>--</td>
<td>0</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>Upper Switch Current Limit</td>
<td>IUM</td>
<td>Normal Operation.</td>
<td>--</td>
<td>4.4</td>
<td>--</td>
<td>A</td>
</tr>
<tr>
<td>Load Line Compensation Gain</td>
<td>GLC</td>
<td>VCSP - VCSN = 100mV, check IFB</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>μA/V</td>
</tr>
<tr>
<td>Current Sense Voltage (*)</td>
<td>VSENSE</td>
<td>VCSP - VCSN</td>
<td>98</td>
<td>100</td>
<td>102</td>
<td>mV</td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>fOSC1</td>
<td>Normal Operation.</td>
<td>85</td>
<td>100</td>
<td>115</td>
<td>kHz</td>
</tr>
<tr>
<td>Short Circuit Oscillation Frequency</td>
<td>fOSC2</td>
<td>VFB = 0V</td>
<td>--</td>
<td>20</td>
<td>--</td>
<td>kHz</td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>tOFF</td>
<td>Normal Operation.</td>
<td>--</td>
<td>200</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>tON</td>
<td>Normal Operation.</td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>ns</td>
</tr>
</tbody>
</table>
### Parameter Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN Input Threshold Voltage</td>
<td>V_IH</td>
<td>Logic-High</td>
<td>2.7</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_IL</td>
<td>Logic-Low</td>
<td>--</td>
<td>--</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Input Under Voltage Lockout Threshold</td>
<td>V_UVLO</td>
<td>VIN Rising</td>
<td>6.3</td>
<td>6.7</td>
<td>7.2</td>
<td>V</td>
</tr>
<tr>
<td>Input Under Voltage Lockout Hysteresis</td>
<td>( \Delta V_UVLO )</td>
<td>--</td>
<td>0.5</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Soft-Start Period</td>
<td>ISS</td>
<td>--</td>
<td>3.5</td>
<td>--</td>
<td>--</td>
<td>ms</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>T_SD</td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>--</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** \( \theta\_JA \) is measured at \( T\_A = 25^\circ\text{C} \) on a high effective thermal conductivity four-layer test board per JEDEC 51-7. \( \theta\_JC \) is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

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**Typical Application Circuit**

[Typical Application Circuit Diagram]

VIN: 7.5V to 36V
C\_BOOT: 100nF
R\_SENSE: 33mΩ
VOUT: 5V/2.4A
R\_1: 180kΩ
R\_2: 34.3kΩ
Typical Operating Characteristics

**Efficiency vs. Output Current**

- Efficiency (%) vs. Output Current (A)
  - $V_{IN} = 12V$
  - $V_{IN} = 24V$
  - $V_{OUT} = 5V$

**Stanby Supply Current vs. Input Voltage**

- Stanby Current (mA) vs. Input Voltage (V)
  - $V_{OUT} = 5V$

**Over Current Limit vs. Input Voltage**

- Over Current Limit (A) vs. Input Voltage (V)
  - $V_{OUT} = 5V$, $I_{OUT} = 2.4A$

**Output Current vs. Temperature**

- Output Current (A) vs. Temperature (°C)
  - $V_{OUT} = 5V$

**Frequency vs. Input Voltage**

- Frequency (kHz) vs. Input Voltage (V)
  - $V_{OUT} = 5V$, $I_{OUT} = 2.4A$

**UVLO Threshold vs. Temperature**

- UVLO Threshold (V) vs. Temperature (°C)
  - Rising
  - Falling
  - $V_{OUT} = 5V$
Application Information

Output Voltage Setting
The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

![Resistive Divider Diagram]

Figure 1. Output Voltage Setting
The output voltage is set by an external resistive voltage divider according to the following equation:

\[ V_{\text{OUT}} = V_{\text{REF}} \left( 1 + \frac{R_1}{R_2} \right) \]

Where \( V_{\text{REF}} \) is the reference voltage (0.8V typ.).

External Bootstrap Diode
Connect a 0.1\( \mu \)F low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

Inductor Selection
The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current \( \Delta I_L \) increases with higher \( V_{\text{IN}} \) and decreases with higher inductance.

\[ \Delta I_L = \left[ \frac{V_{\text{OUT}}}{f \times L} \right] \times \left[ 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right] \]

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of \( \Delta I_L = 0.24(I_{\text{MAX}}) \) will be a reasonable starting point. The largest ripple current occurs at the highest \( V_{\text{IN}} \). To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

\[ L = \left[ \frac{V_{\text{OUT}}}{f \times I_{\text{MAX}}} \right] \times \left[ 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right] \]

The inductor's current rating (caused a 40\(^\circ\)C temperature rising from 25\(^\circ\)C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

<table>
<thead>
<tr>
<th>Component Supplier</th>
<th>Series</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAG.LAYERS</td>
<td>MCD110C-390K-LV</td>
<td>10 x 6.5 x 10.5</td>
</tr>
</tbody>
</table>

\( C_{\text{IN}} \) and \( C_{\text{OUT}} \) Selection
The input capacitance, \( C_{\text{IN}} \), is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current is given:

\[ I_{\text{RMS}} = I_{\text{OUT(MAX)}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \sqrt{\frac{V_{\text{IN}}}{V_{\text{OUT}}}} \]

This formula has a maximum at \( V_{\text{IN}} = 2V_{\text{OUT}} \), where \( I_{\text{RMS}} = I_{\text{OUT}}/2 \). This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10\( \mu \)F low ESR ceramic capacitors are Suggested. For the Suggested capacitor, please refer to Table 3 for more details. The selection of \( C_{\text{OUT}} \) is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for \( C_{\text{OUT}} \) selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, \( \Delta V_{\text{OUT}} \), is determined by:

\[ \Delta V_{\text{OUT}} \leq \Delta L \left[ ESR + \frac{1}{8C_{\text{OUT}}} \right] \]
The output ripple will be the highest at the maximum input voltage since \( \Delta i_L \) increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, \( V_{IN} \). At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at \( V_{IN} \) large enough to damage the part.

**Thermal Considerations**

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

\[
P_{D(\text{MAX})} = (T_{J(\text{MAX})} - T_A) / \theta_{JA}
\]

where \( T_{J(\text{MAX})} \) is the maximum junction temperature, \( T_A \) is the ambient temperature, and \( \theta_{JA} \) is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, \( \theta_{JA} \), is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, \( \theta_{JA} \), is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at \( T_A = 25^\circ\text{C} \) can be calculated by the following formula:

\[
P_{D(\text{MAX})} = (125°C - 25°C) / (49°C/W) = 2.041 \text{W for SOP-8 (Exposed Pad) package}
\]

The maximum power dissipation depends on the operating ambient temperature for fixed \( T_{J(\text{MAX})} \) and thermal resistance, \( \theta_{JA} \). The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

**Layout Consideration**

Follow the PCB layout guidelines for optimal performance of the RT6266.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT6266.
- An example of PCB layout guide is shown in Figure 3 for reference.
## Outline Dimension

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>4.801</td>
<td>5.004</td>
</tr>
<tr>
<td>B</td>
<td>3.810</td>
<td>4.000</td>
</tr>
<tr>
<td>C</td>
<td>1.346</td>
<td>1.753</td>
</tr>
<tr>
<td>D</td>
<td>0.330</td>
<td>0.510</td>
</tr>
<tr>
<td>F</td>
<td>1.194</td>
<td>1.346</td>
</tr>
<tr>
<td>H</td>
<td>0.170</td>
<td>0.254</td>
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<td>I</td>
<td>0.000</td>
<td>0.152</td>
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<td>J</td>
<td>5.791</td>
<td>6.200</td>
</tr>
<tr>
<td>M</td>
<td>0.406</td>
<td>1.270</td>
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<td>Option 1</td>
<td>X</td>
<td>2.000</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>2.000</td>
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<tr>
<td>Option 2</td>
<td>X</td>
<td>2.100</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>3.000</td>
</tr>
</tbody>
</table>

8-Lead SOP (Exposed Pad) Plastic Package

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