Complete LPDDR5/5X Memory Power Solution

1 General Description

The RT6300C/RT6300CH/RT6300D/RT6300DH is an integrated power management IC solution for LPDDR5 and LPDDR5X memory.

This device provides two single buck voltage regulators VDD2H (RT6300C/ RT6300CH:1.065V/8A, RT6300D/RT6300DH:1.05V/8A) and VDDQ (0.52V or 0.32V/3A), one LDO VDD2L (0.92V/1.5A), and one load switch VDD1 (1.8V/1A).

The RT6300C/RT6300CH/RT6300D/RT6300DH supports VDD2L and 1-bit VID to dynamically adjust the VDDQ output voltage, thus satisfying the requirements of LPDDR5/5X DVFSC and DVFSQ applications.

The RT6300C/RT6300CH/RT6300D/RT6300DH adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultra-fast transient response and further reduces the number of external components. In steady states, the ACOT® operates at a nearly constant switching frequency across line, load, and output voltage ranges, and simplifies the EMI filter design.

The RT6300C/RT6300CH/RT6300D/RT6300DH operates in diode emulation mode (DEM) under the light load condition, offering optimal light load efficiency. It also supports multiple operational modes, S0, S3, and S4/5, controlled by the EN/EN_VDDQ control inputs.

The RT6300C/RT6300CH/RT6300D/RT6300DH provides full protection functions, including the cycle-by-cycle current limit, OVP, UVP, input UVLO, and OTP.

All functions are integrated in a WQFN-19L 3x3 (FC) package. The recommended junction temperature range is –40°C to 125°C.

2 Features

- **Wide Input Supply Range: 4.5V to 23V for HV Buck Converter**
- **Four High-Efficiency Output Regulators:**
  - **VDD1 (Load Switch): 1.8V/1A**
  - **VDD2H (HV Buck Converter): RT6300C/RT6300CH:1.065V/8A, RT6300D/RT6300DH:1.05V/8A**
  - **VDD2L (LDO): 0.92V/1.5A**
  - **VDDQ (LV Buck Converter): 0.32V/3A or 0.52V/3A (Selectable by VSEL Pin)**
- **12A Peak Output Current for VDD2H**
- **Support DVFSC and DVFSQ for LPDDR5/5X**
- **Compliant with LPDDR5/5X Power-On and Power-Off Sequences in JEDEC Standard**
- **Protection Option:**
  - **RT6300C/RT6300D: Latch Mode**
  - **RT6300CH/RT6300DH: Hiccup Mode**
- **Stable Operation with POSCAP and MLCC Capacitors**
- **Fast Transient Response with ACOT® Control**
- **Diode Emulation Mode (DEM) for Power Saving**
- **Low $R_{DS(ON)}$ Internal Power MOSFETs**
- **Current-Limit Protection**
- **Output Undervoltage or Overvoltage Protection (UVP/OVP)**
- **Input Undervoltage-Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
- **Power-Good Indicator**

3 Applications

- Laptop Computers
- Tablet PCs
- Networking Systems
- Distributed Power Systems

4 Ordering Information

RT6300 □□-□

Packing
A: Standard

Package Type(1)
N: WQFN-19L 3x3 (FC) (W-Type)

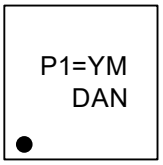
VOUT_VDD2H & Protection Option
C: 1.065V, Latch Mode
CH: 1.065V, Hiccup Mode
D: 1.05V, Latch Mode
DH: 1.05V, Hiccup Mode

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

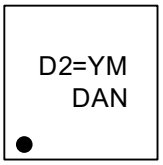
5 Marking Information

RT6300CN-A



P1=: Product Code
YMDAN: Date Code

RT6300CHN-A



D2=: Product Code
YMDAN: Date Code

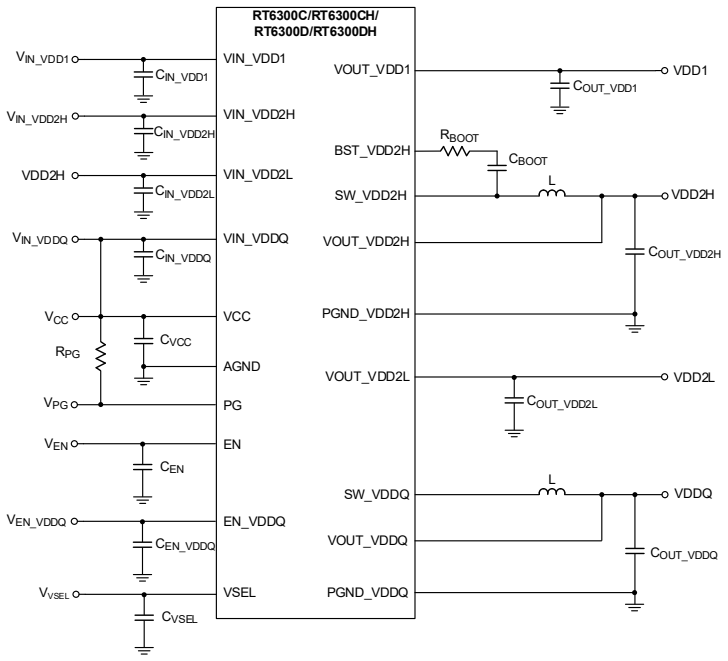
RT6300DN-A

LV=: Product Code
YMDAN: Date Code

RT6300DHN-A

LN=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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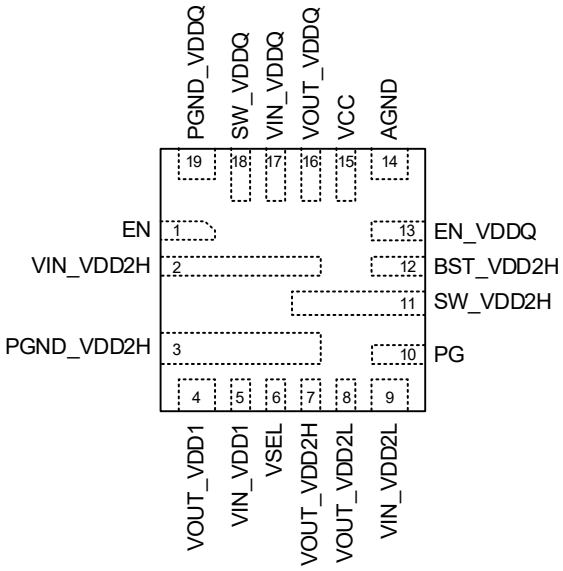
7 Pin Configuration

(TOP VIEW)



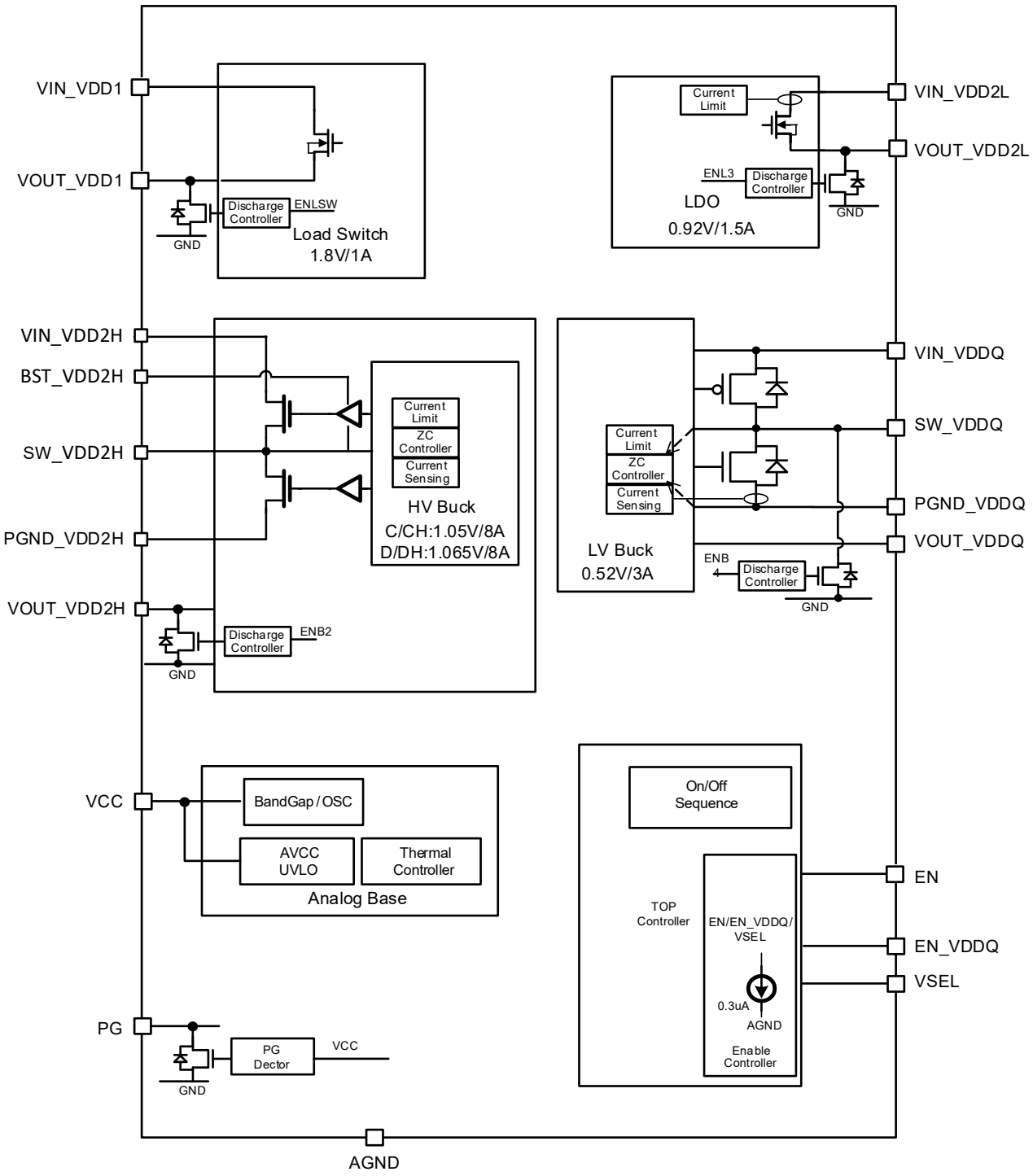
WQFN-19L 3x3 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input. It is for VDD1 load switch, VDD2H Buck, and VDD2L LDO enable control. For the EN control logic of the RT6300C/RT6300CH/RT6300D/RT6300DH, refer to Table 5 EN is pulled low internally.
2	VIN_VDD2H	VDD2H input supply voltage pin. This pin is used to supply the VDD2H internal MOSFET and regulator. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. It is necessary to connect the ceramic capacitor as close as possible from the VIN_VDD2H pin to the PGND_VDD2H pin.
3	PGND_VDD2H	Power ground. Directly soldering to a large PCB PGND plane and connecting thermal vias near the PGND_VDD2H pin are required to minimize the parasitic impedance and thermal resistance.
4	VOUT_VDD1	VDD1 output voltage pin. It is necessary to connect a 22μF ceramic capacitor as close as possible from the VOUT_VDD1 pin to the PGND plane.
5	VIN_VDD1	VDD1 input supply voltage pin. A 1.8V power supply is recommended for the load switch input. Place a 10μF ceramic capacitor as close as possible to this pin.
6	VSEL	VSEL control input pin. Drive this pin with an external control circuit. The VDDQ output voltage decreases from 0.52V to 0.32V if the status of this pin changes from logic high to logic low. Conversely, the VDDQ output voltage increases from 0.32V to 0.52V if the status of this pin changes from logic low to logic high. VSEL is pulled low internally.
7	VOUT_VDD2H	VDD2H output voltage sense feedback pin. Connect this pin to the positive terminal of the output capacitor for the VDD2H buck converter. The VDD2H output voltage can be adjusted by adding a voltage divider resistor to VOUT_VDD2H, allowing for a range of 0% to 10%. Additionally, the upper arm resistor must be less than 10Ω.

Pin No.	Pin Name	Pin Function
8	VOUT_VDD2L	VDD2L output voltage pin. It is necessary to connect the ceramic capacitor as close as possible from the VOUT_VDD2L pin to the PGND plane. If VDD2L is not used, leave this pin floating.
9	VIN_VDD2L	VDD2L input supply voltage pin. Connect to the VDD2H output voltage with a wide trace as the supply voltage for the LDO. Ensure that the wiring trace is separated from the VOUT_VDD2H sense feedback trace to avoid additional voltage drop.
10	PG	Power-good indicator is an open-drain output. This pin is pulled low as UVP, OVP, OTP, and EN are low, or the output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or another external rail is required, with the recommended pull-up resistor ranging from 10kΩ to 100kΩ. Do not pull the PG voltage higher than 6V.
11	SW_VDD2H	The switch node of the VDD2H buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. This pin is also used for internal ramp generation, on-time generation, and current detection. Connect this pin to the output inductor and keep the sensitive traces and signals away.
12	BST_VDD2H	Bootstrap supply for the VDD2H high-side gate driver. Connect a high-quality and low ESR ceramic capacitor (minimum C = 0.1μF/0603) from the BOOT pin to the SW pin through short and low inductance paths. During the period when the low-side MOSFET is turned on, the bootstrap capacitor is charged by the BOOT pin to store the required energy for the high-side gate driver. A bootstrap resistor (0603 size, ≤10Ω) in series with the bootstrap capacitor is strongly recommended for reducing the voltage spike at the SW node.
13	EN_VDDQ	VDDQ enable control input. For the EN_VDDQ control logic of the RT6300C/RT6300CH/RT6300D/RT6300DH, refer to Table 5 EN_VDDQ is pulled low internally.
14	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
15	VCC	External 5V VCC input supply pin. Used as a supply to internal control circuits. Connect a high-quality capacitor (C = 4.7μF/0603) from this pin to AGND.
16	VOUT_VDDQ	VDDQ output voltage sense feedback pin. Connect this pin to the output capacitor of the VDDQ buck converter. The VDDQ output voltage can be adjusted by adding a voltage divider resistor to VOUT_VDDQ, allowing for a range of 0% to 10%. Additionally, the upper arm resistor must be less than 100Ω.
17	VIN_VDDQ	VDDQ input voltage supply pin. This pin is used to supply the VDDQ internal MOSFET and regulator. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. It is necessary to connect the ceramic capacitor as close as possible from the VIN_VDDQ pin to the PGND_VDDQ pin.
18	SW_VDDQ	The switch node of the VDDQ buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. This pin is also used for internal ramp generation, on-time generation, and current detection. Connect this pin to the output inductor and keep the sensitive traces and signals away.
19	PGND_VDDQ	VDDQ power ground. Directly soldering to a large PCB PGND plane and connecting thermal vias near the PGND_VDDQ pin are required to minimize parasitic impedance and thermal resistance.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, V_{CC} ---------- –0.3V to 6.5V
- Supply Input Voltage, V_{IN_VDD1} ---------- –0.3V to 6.5V
- Supply Input Voltage, V_{IN_VDD2H} ---------- –0.3V to 28V
- Supply Input Voltage, V_{IN_VDD2L} ---------- –0.3V to 6.5V
- Supply Input Voltage, V_{IN_VDDQ} ---------- –0.3V to 6.5V
- Switch Voltage, V_{SW_VDD2H} ---------- –0.3V to (V_{IN_VDD2H} + 0.3V)
  < 10ns ---------- –16V to 38V
- Switch Voltage, V_{SW_VDDQ} ---------- –0.3V to (V_{IN_VDDQ} + 0.3V)
  < 10ns ---------- –7V to 12V
- Boot Voltage, V_{BST_VDD2H} ---------- (V_{SW_VDD2H}–0.3V) to (V_{SW_VDD2H} + 6.5V)
- Other I/O Pin Voltages ---------- –0.3V to 6.5V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage V_{CC} ---------- 4.5V to 5.5V
- Supply Input Voltage V_{IN_VDD1} ---------- 1.7V to 1.9V
- Supply Input Voltage V_{IN_VDD2H} ---------- 4.5V to 23V
- Supply Input Voltage V_{IN_VDD2L} ---------- 1.01V to 1.12V
- Supply Input Voltage V_{IN_VDDQ} ---------- 3V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

Thermal Parameter		WQFN-19L 3x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	51.9	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	30.67	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.75	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	34.31	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.09	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.37	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

(V_{IN_VDD2H} = 12V, V_{EN} = V_{EN_VDDQ} = 5V, V_{CC} = 5V. The typical values are referenced to T_A = T_J = 25°C. Both minimum and maximum values are referenced to T_A = T_J from −10°C to 105°C. Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCC Supply Current all Rail on (S0 Mode)	I_{VCC_S0}	V_{EN} = V_{EN_VDDQ} = 5V no load, no switching	--	240	--	μA
VCC Supply Current VDD1 & VDD2H & VDD2L on (S3 Mode)	I_{VCC_S3}	V_{EN} = 5V, V_{EN_VDDQ} = 0V no load, no switching	--	190	--	μA
VCC Supply Current VDD1 & VDD2H & VDDQ on (S0 Mode, No VDD2L)	$I_{VCC\_S0\_N2L}$	V_{EN} = V_{EN_VDDQ} = 5V, V_{OUT_VDD2L} = floating, no load, no switching	--	200	--	μA
VCC Supply Current VDD1 & VDD2H on (S3 Mode)	I_{VCC_S3}	V_{EN} = 5V, V_{EN_VDDQ} = 0V, V_{OUT_VDD2L} = floating, no load, no switching	--	150	--	μA
Shutdown Supply Current (S4/S5 Mode)	I_{VCC_SHDN}	V_{EN} = 0V, VCC < 2V	--	1	--	μA
UVLO						
VCC UVLO Rising Threshold	$V_{CC\_UVLO\_R}$		--	4	--	V
VCC UVLO Falling Threshold	$V_{CC\_UVLO\_F}$		--	3.8	--	V
VIN_VDD2H UVLO Rising Threshold	$V_{IN\_VDD2H\_UVLO\_R}$		--	4	--	V
VIN_VDD2H UVLO Falling Threshold	$V_{IN\_VDD2H\_UVLO\_F}$		--	3.8	--	V
VIN_VDDQ UVLO Rising Threshold	$V_{IN\_VDDQ\_UVLO\_R}$		--	2.8	--	V
VIN_VDDQ UVLO Falling Threshold	$V_{IN\_VDDQ\_UVLO\_F}$		--	2.6	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN_VDD1 UVLO Rising Threshold	$V_{IN\_VDD1\_UVLO\_R}$		--	1.65	--	V
VIN_VDD1 UVLO Falling Threshold	$V_{IN\_VDD1\_UVLO\_F}$		--	1.55	--	V
Logic Threshold						
EN Input High Voltage	V_{EN_H}		1.2	--	--	V
EN_VDDQ Input High Voltage	$V_{EN\_VDDQ\_H}$		1.2	--	--	V
VSEL Input High Voltage	V_{SEL_H}		1.2	--	--	V
EN Input Low Voltage	V_{EN_L}		--	--	0.4	V
EN_VDDQ Input Low Voltage	$V_{EN\_VDDQ\_L}$		--	--	0.4	V
VSEL Input Low Voltage	V_{SEL_L}		--	--	0.4	V
EN Input Leakage Current	I_{EN_LK}	V_{EN} = 2V	--	0.3	--	μA
EN_VDDQ Input Leakage Current	$I_{EN\_VDDQ\_LK}$	V_{EN_VDDQ} = 2V	--	0.3	--	μA
VSEL Input Leakage Current	I_{VSEL_LK}	V_{SEL} = 2V	--	0.3	--	μA
PG Pull Low Voltage	V_{PG_L}	I_{PG} = 10mA	--	--	0.4	V
VDD2H On Resistance						
High-Side MOSFET On-Resistance	$R_{DSON\_H\_VDD2H}$	$T_A = T_J$ = 25°C	--	28	--	mΩ
Low-Side MOSFET On-Resistance	$R_{DSON\_L\_VDD2H}$	$T_A = T_J$ = 25°C	--	14	--	mΩ
VDD2H Reference						
Output Voltage	V_{OUT_VDD2H}	RT6300C/RT6300CH, $T_A = T_J$ = 25°C, CCM	1.054	1.065	1.076	V
		RT6300D/RT6300DH, $T_A = T_J$ = 25°C, CCM	1.039	1.05	1.06	V
VDD2H Switching Frequency						
Switching Frequency	f_{SW_VDD2H}	$T_A = T_J$ = 25°C	400	500	600	kHz
VDD2H On-Time Timer Control						
Minimum On-Time	$t_{ON\_MIN\_VDD2H}$		--	55	--	ns
Minimum Off-Time	$t_{OFF\_MIN\_VDD2H}$		--	260	--	ns
VDD2H Current Limit						
L/S Valley Current Limit	$I_{LIM\_L\_VDD2H}$	$T_A = T_J$ = 25°C	12	15	18	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD2H Protection						
OVP Threshold	$V_{DD2H\_OVP\_R}$		--	125	--	%
OVP Hysteresis	$V_{DD2H\_OVP\_HYS}$		--	10	--	%
OVP Timer Latch (Deglitch)	$t_{DLY\_OVP\_VDD2H}$		--	20	--	µs
UVP Threshold	$V_{DD2H\_UVP\_F}$		--	60	--	%
UVP Hysteresis	$V_{DD2H\_UVP\_HYS}$		--	10	--	%
UVP Timer Latch (Deglitch)	$t_{DLY\_UVP\_VDD2H}$		--	20	--	µs
VDD2H Discharge Resistor						
Discharge Resistor	R_{DISCHG_VDD2H}	V_{EN} = 0V, V_{OUT} = 0.1V	--	10	--	Ω
VDDQ On-Resistance						
High-Side MOSFET On-Resistance	$R_{DSON\_H\_VDDQ}$	$T_A = T_J$ = 25°C	--	100	--	mΩ
Low-Side MOSFET On-Resistance	$R_{DSON\_L\_VDDQ}$	$T_A = T_J$ = 25°C	--	50	--	mΩ
VDDQ Reference						
Output Voltage	V_{OUT_VDDQ}	VIN_VDDQ = 3.3V, V_{SEL} = 5V, $T_A = T_J$ = 25°C, CCM and for general purpose	0.505	0.52	0.53	V
		VIN_VDDQ = 3.3V, V_{SEL} = 0V, $T_A = T_J$ = 25°C, CCM and for general purpose	0.305	0.32	0.33	
		VIN_VDDQ = 5V, V_{SEL} = 5V, $T_A = T_J$ = 25°C, CCM and for general purpose	0.51	0.52	0.53	
		VIN_VDDQ = 5V, V_{SEL} = 0V, $T_A = T_J$ = 25°C, CCM and for general purpose	0.31	0.32	0.33	
VDDQ Switching Frequency						
Switching Frequency	f_{SW_VDDQ}		1.6	2	2.4	MHz
VDDQ Current Limit						
L/S Valley Current Limit	$I_{LIM\_L\_VDDQ}$	$T_A = T_J$ = 25°C	2.9	3.5	4.1	A
VDDQ On-Time Timer Control						
Minimum Off-Time	$t_{OFF\_MIN\_VDDQ}$		--	170	--	ns
VDDQ Protection						
OVP Threshold	$V_{DDQ\_OVP\_R}$		--	125	--	%
OVP Hysteresis	$V_{DDQ\_OVP\_HYS}$		--	10	--	%
OVP Timer Latch (Deglitch)	$t_{DLY\_OVP\_VDDQ}$		--	20	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVP Threshold	$V_{DDQ\_UVP\_F}$		--	60	--	%
UVP Hysteresis	$V_{DDQ\_UVP\_HYS}$		--	10	--	%
UVP Timer Latch (Deglitch)	$t_{DLY\_UVP\_VDDQ}$		--	20	--	µs
VDDQ Discharge Resistor						
Discharge Resistor	R_{DISCHG_VDDQ}	V_{EN} = 0V, V_{OUT} = 0.1V	--	10	--	Ω
VDD1 On-Resistance						
Load Switch MOSFET On-Resistance	R_{DSON_VDD1}	T_A = T_J = 25°C	--	60	--	mΩ
VDD1 Reference						
Output Voltage	V_{OUT_VDD1}	V_{IN_VDD1} = 1.8V, T_A = T_J = 25°C, depend on V_{IN_VDD1}	--	1.8	--	V
VDD1 Current Limit and Protection						
Current Limit	I_{LIM_VDD1}	T_A = T_J = 25°C	1.05	1.35	1.65	A
Current Limit Delay	$t_{DLY\_LIM\_VDD1}$		--	2	10	µs
UVP Threshold	$V_{DD1\_UVP\_F}$		--	60	--	%
UVP Hysteresis	$V_{DD1\_UVP\_HYS}$		--	10	--	%
UVP Timer Latch (Deglitch)	$t_{DLY\_UVP\_VDD1}$		--	20	--	µs
VDD1 Discharge Resistor						
Discharge Resistor	R_{DISCHG_VDD1}	V_{EN} = 0V, V_{OUT} = 0.1V	--	10	30	Ω
VDD2L Dropout Voltage						
Dropout Voltage	V_{DROP_VDD2L}	I_{OUT} = 1.5A	--	60	110	mV
VDD2L Reference						
Output Voltage	V_{OUT_VDD2L}	T_A = T_J = 25°C	0.911	0.92	0.929	V
VDD2L Current Limit and Protection						
Current Limit	I_{LIM_VDD2L}	T_A = T_J = 25°C	--	1.8	--	A
OVP Threshold	$V_{DD2L\_OVP\_R}$		--	125	--	%
OVP Hysteresis	$V_{DD2L\_OVP\_HYS}$		--	10	--	%
OVP Timer Latch (Deglitch)	$t_{DLY\_OVP\_VDD2L}$		--	20	--	µs
UVP Threshold	$V_{DD2L\_UVP\_F}$		--	60	--	%
UVP Hysteresis	$V_{DD2L\_UVP\_HYS}$		--	10	--	%
UVP Timer Latch (Deglitch)	$t_{DLY\_UVP\_VDD2L}$		--	20	--	µs
VDD2L Discharge Resistor						
Discharge Resistor	R_{DISCHG_VDD2L}	V_{EN} = 0V, V_{OUT} = 0.1V	--	10	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD1/VDD2H/VDD2L/VDDQ Soft-Start						
VDD1 Soft-Start Slew Rate	SR_{SS_VDD1}	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	5	--	mV/μs
VDD2H Soft-Start Slew Rate	SR_{SS_VDD2H}	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	5	--	mV/μs
VDD2L Soft-Start Slew Rate	SR_{SS_VDD2L}	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	5	--	mV/μs
VDDQ Soft-Start Slew Rate	SR_{SS_VDDQ}	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	5	--	mV/μs
VSEL Timing Control						
Dynamic Voltage Up Slew Rate	SR_{DVS_UP}	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	2.5	--	mV/μs
Dynamic Voltage Down Slew Rate	SR_{DVS_DN}	$T_A = T_J = 25°C$, from 90% to 10% V_{OUT}	--	2.5	--	mV/μs
Power-Good Indicator						
VDD2H PG Rising Threshold	$V_{DD2H\_PG\_R}$		--	90	--	%
VDD2H PG Falling Threshold	$V_{DD2H\_PG\_F}$		--	80	--	%
VDD2L PG Rising Threshold	$V_{DD2L\_PG\_R}$		--	90	--	%
VDD2L PG Falling Threshold	$V_{DD2L\_PG\_F}$		--	80	--	%
VDD1 PG Rising Threshold	$V_{DD1\_PG\_R}$		--	90	--	%
VDD1 PG Falling Threshold	$V_{DD1\_PG\_F}$		--	80	--	%
VDDQ PG Rising Threshold	$V_{DDQ\_PG\_R}$		--	85	--	%
VDDQ PG Falling Threshold	$V_{DDQ\_PG\_F}$		--	60	--	%
Power Good Low to High Deglitch Time	t_{DLY_PGH}		--	20	--	μs
Power Good High to Low Deglitch Time	t_{DLY_PGL}		--	20	--	μs
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	25	--	°C

15 Typical Application Circuit

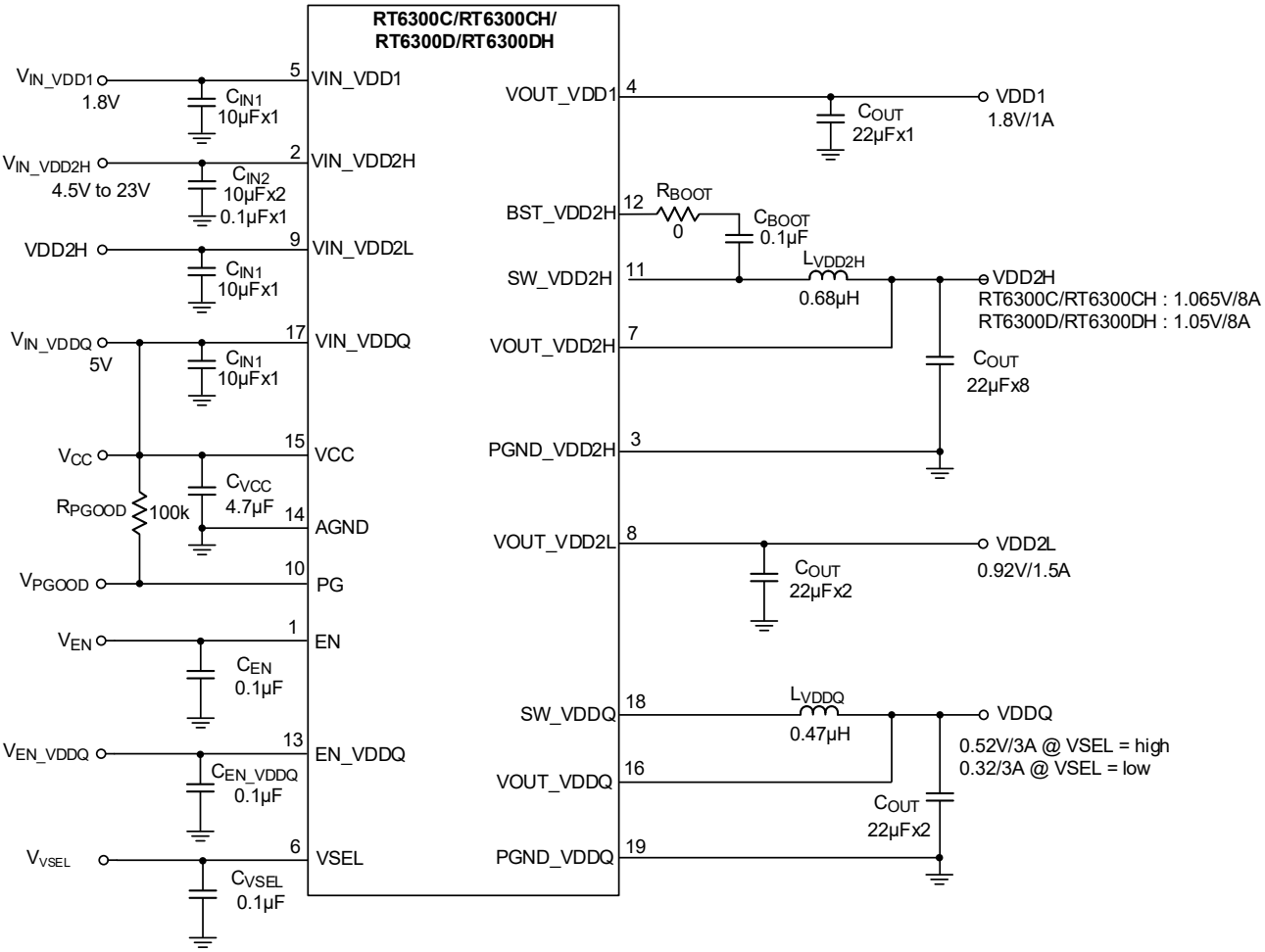


Table 1. Effective Input Capacitance of All Channels

Input Capacitance					
Rail	**Symbol**	**Part Number**	**Value**	**Qty**	**Min. Ceff (Note 6)**
VDD1	C_{IN1}	GRM188R60J106ME47D	10µF/6.3V/X5R/0603	1	5.75µF@VIN = 1.8V
VDD2H	C_{IN2}	GRM21BR6YA106ME43	10µF/35V/X5R/0805	2	3.3µF@VIN = 20V
		GCM188R71H104KA57	0.1µF/50V/X7R/0603	1	
VDD2L	C_{IN3}	GRM188R60J106ME47D	10µF/6.3V/X5R/0603	1	6.53µF@1.065V
VDDQ	C_{IN4}	GRM188R60J106ME47D	10µF/6.3V/X5R/0603	1	2.87µF@VIN = 5V
		GCM188R71H104KA57	0.1µF/50V/X7R/0603	1	

Note 6. The total effective capacitance value is specified for AC 0.01 Vrms across the overall operating temperature range.

Table 2. Effective Output Capacitance of All Channels

Output Capacitance						
Rail	**Part Number**	**Value**		**Qty**	**Min. Ceff (Note 6)**	**Inductor**
VDD1	GRM188R60J226MEA0	22μF/6.3V/X5R/0603		1	11.9μF@VOUT = 1.8V	NA
VDD2H	GRM188R60J226MEA0	VOUT tolerance ±5% with Icc_max 0% - 70% and 30% - 100% with SR = 1A/μs (Note 7)	22μF/6.3V/X5R/0603	8	114μF@VOUT = 1.065V	0.68μH (Note 8)
VDD2L	GRM155R60J226ME11	22μF/6.3V/X5R/0402		2	26.5μF@VOUT = 0.92V	NA
VDDQ	GRM188R60J226MEA0	22μF/6.3V/X5R/0603		2	31.4μF@VOUT = 0.5V	0.47μH (Note 9)

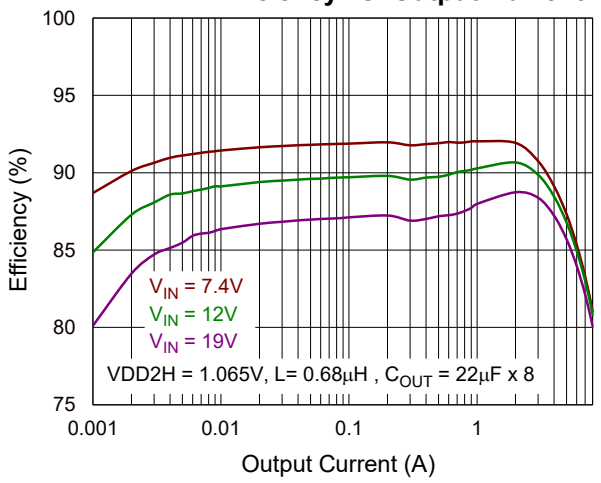
Note 7. ICC_max = 10.92A

Note 8. PEUE063T-R68MS: Size(mm) = 7.3 x 6.8 x 3, L = 0.68μH, DCR = 4.3mΩ, I_{SAT} = 18.5A

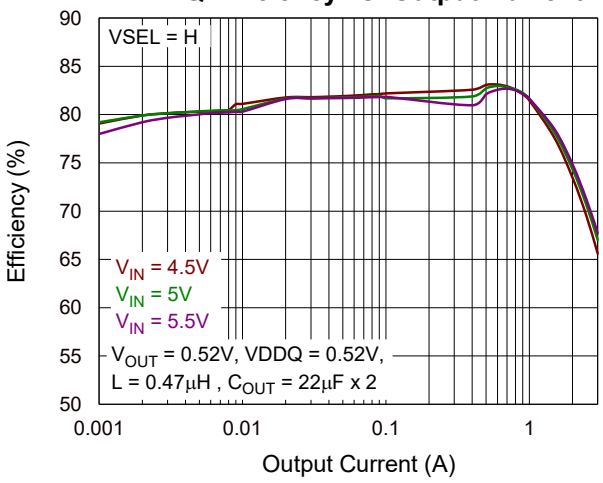
Note 9. MPCA-0618-R47-M: Size(mm) = 7.3 x 6.8 x 1.8, L = 0.47μH, DCR = 8mΩ, I_{SAT} = 11.5A

16 Typical Operating Characteristics

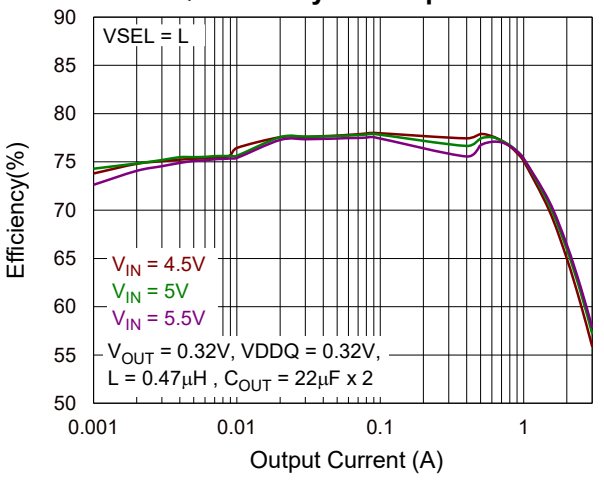
VDD2H Efficiency vs. Output Current



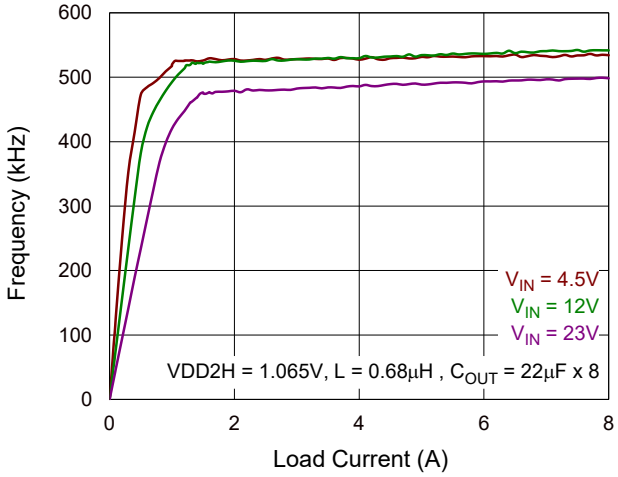
VDDQ Efficiency vs. Output Current



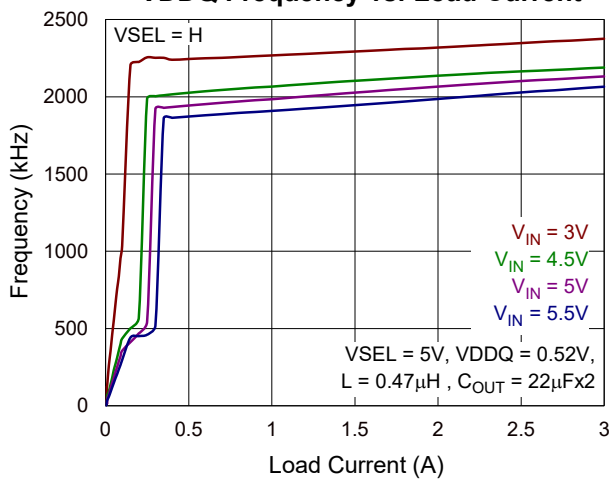
VDDQ Efficiency vs. Output Current



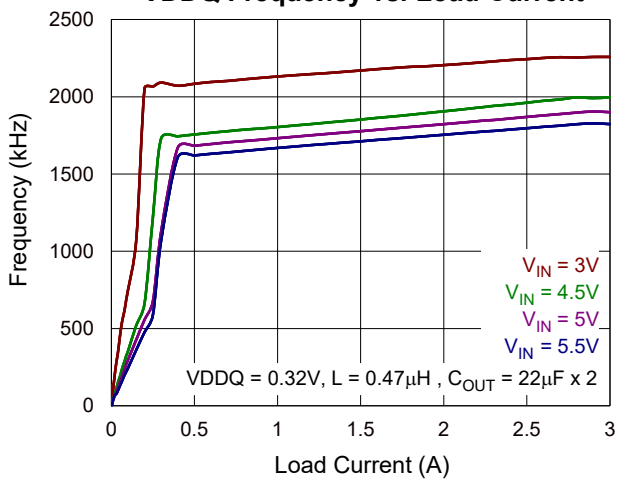
VDD2H Frequency vs. Load Current



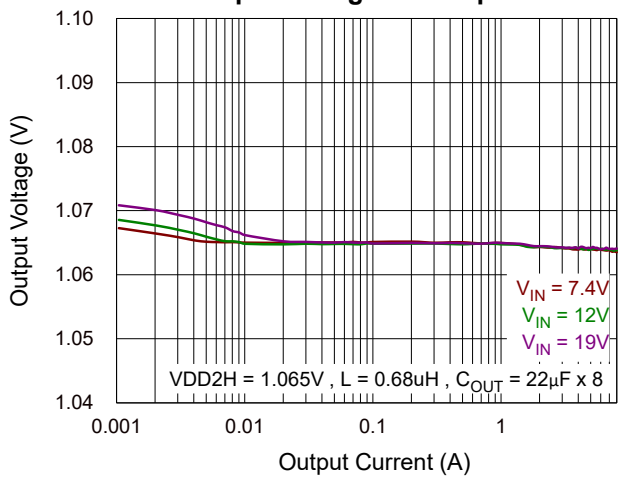
VDDQ Frequency vs. Load Current



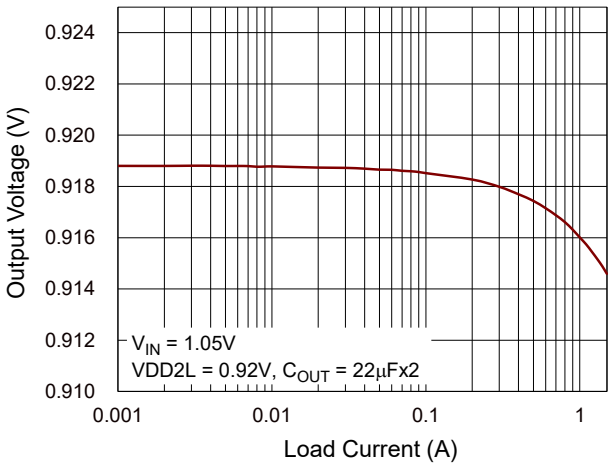
VDDQ Frequency vs. Load Current



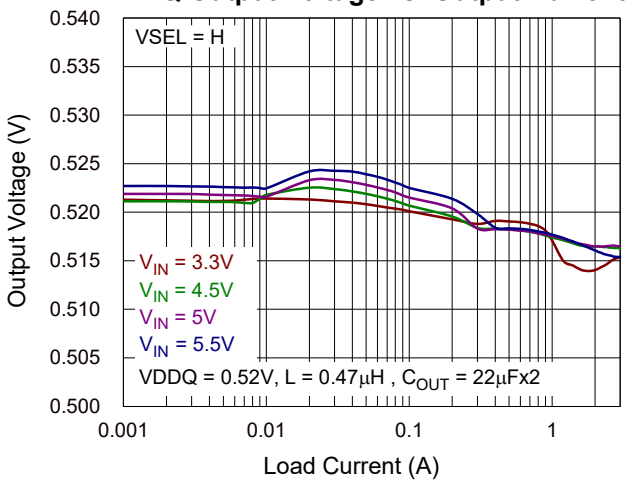
VDD2H Output Voltage vs. Output Current



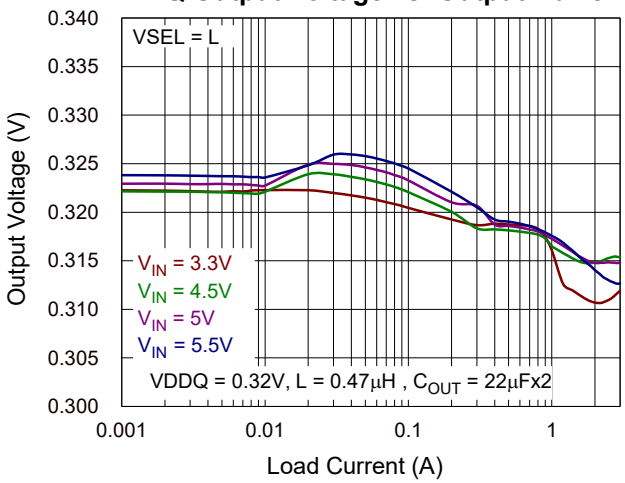
VDD2L Output Voltage vs. Output Current



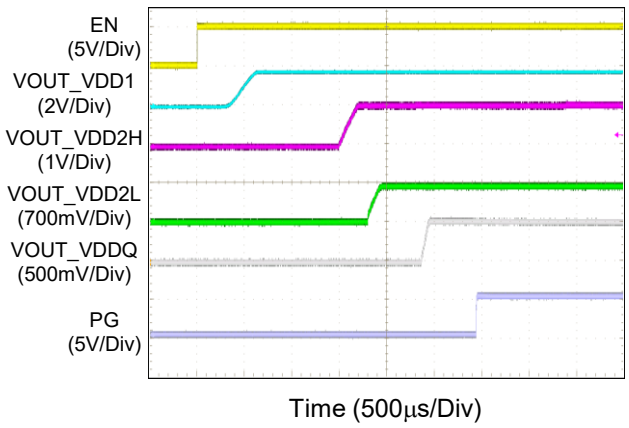
VDDQ Output Voltage vs. Output Current



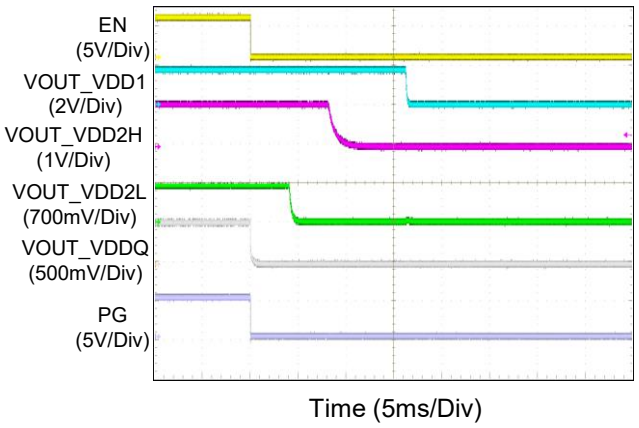
VDDQ Output Voltage vs. Output Current



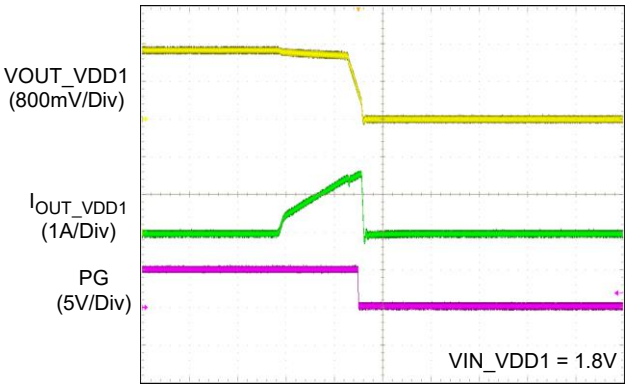
Power On by EN



Power Off by EN

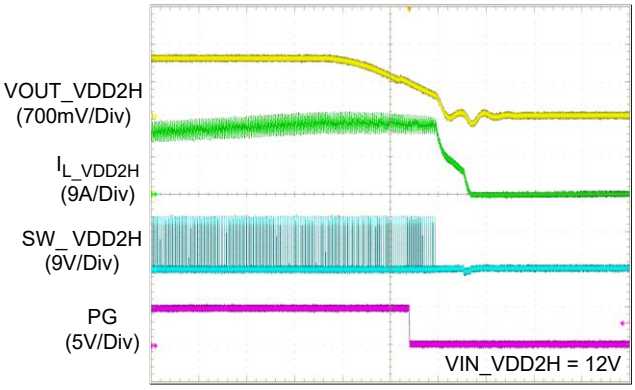


VDD1 OCP



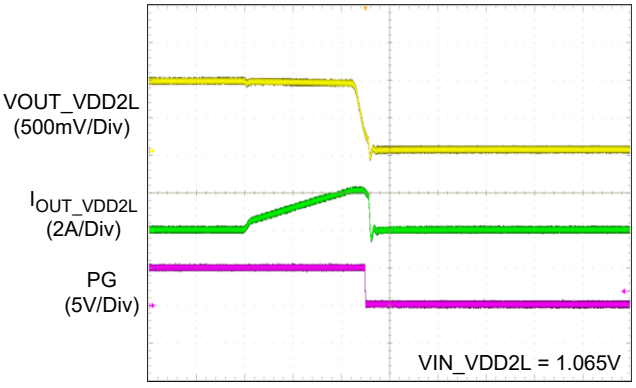
Time (50μs/Div)

VDD2H OCP



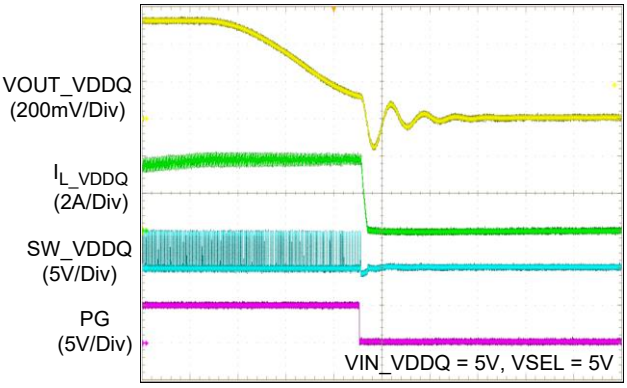
Time (50μs/Div)

VDD2L OCP



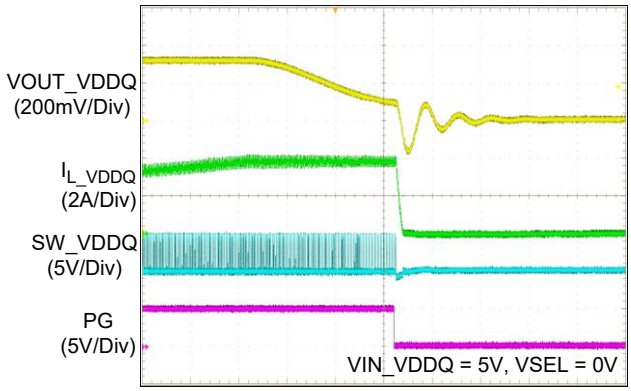
Time (200μs/Div)

VDDQ OCP



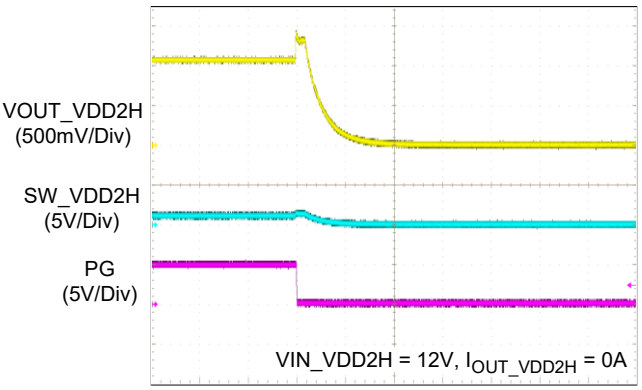
Time (20μs/Div)

VDDQ OCP



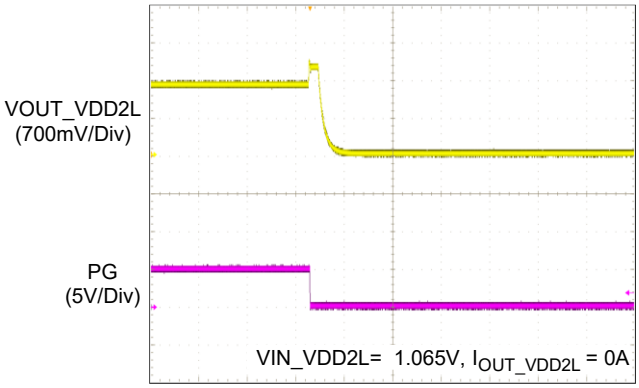
Time (20μs/Div)

VDD2H OVP



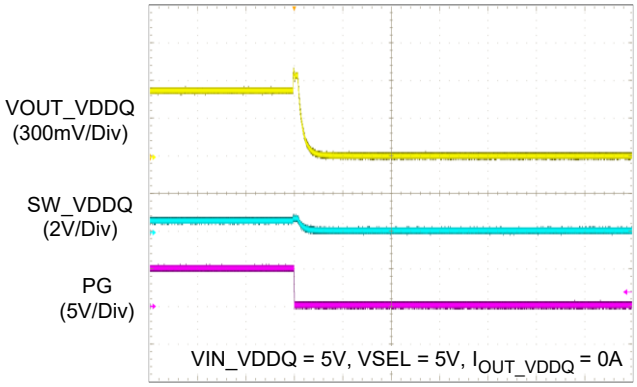
Time (2ms/Div)

VDD2L OVP



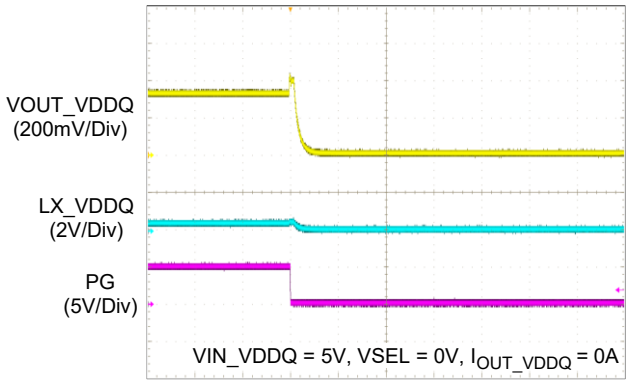
Time (2ms/Div)

VDDQ OVP



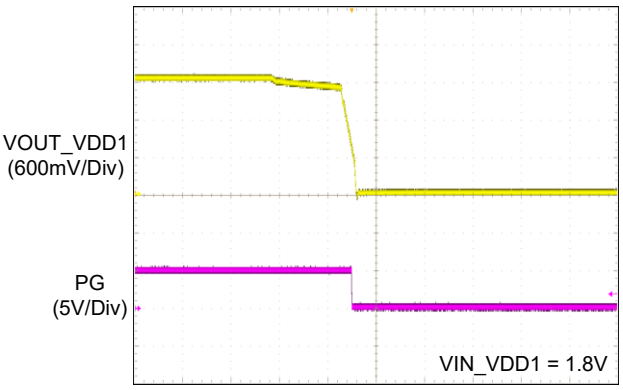
Time (2ms/Div)

VDDQ OVP



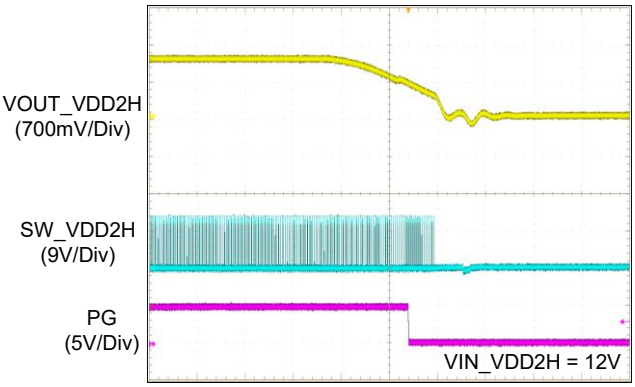
Time (2ms/Div)

VDD1 UVP



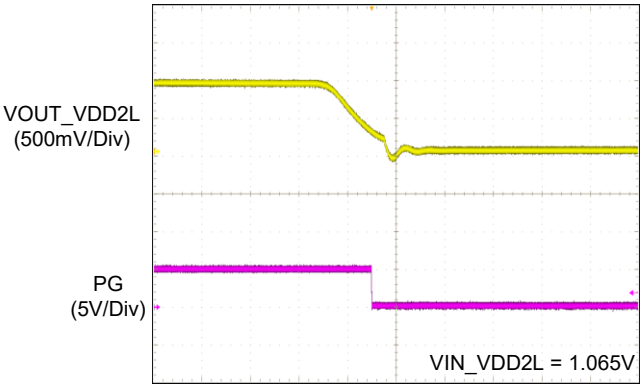
Time (50µs/Div)

VDD2H UVP



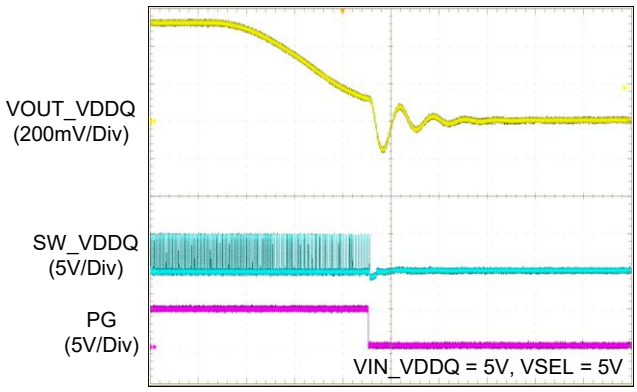
Time (50µs/Div)

VDD2L UVP



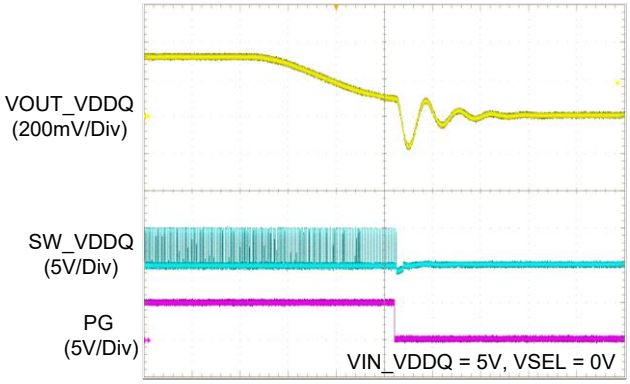
Time (50µs/Div)

VDDQ UVP



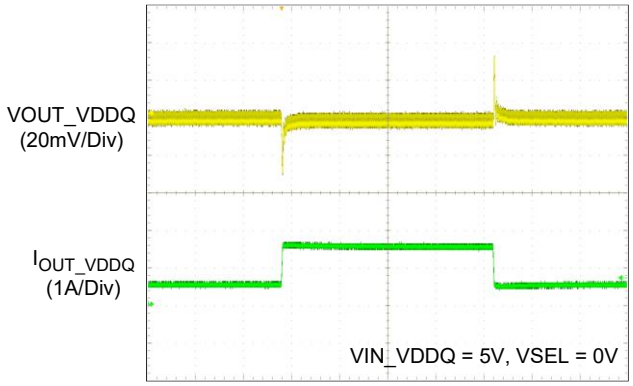
Time (20μs/Div)

VDDQ UVP



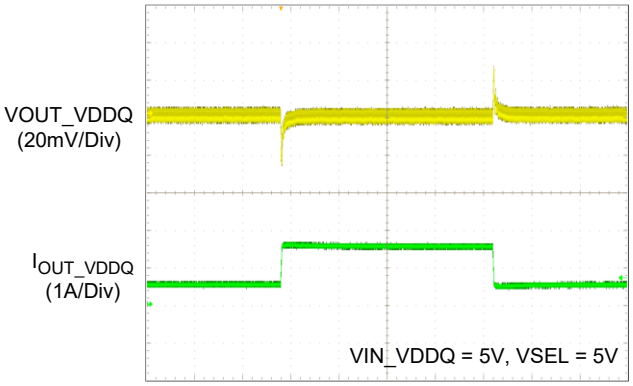
Time (20μs/Div)

VDDQ Load Transient



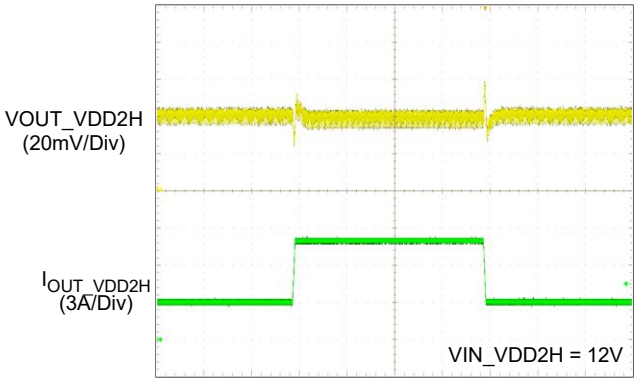
Time (100μs/Div)

VDDQ Load Transient



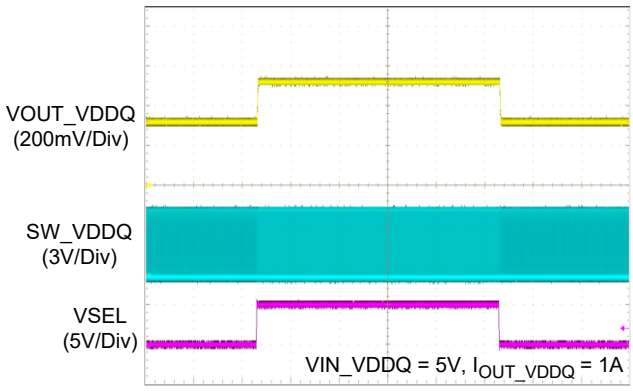
Time (100μs/Div)

VDD2H Load Transient



Time (100μs/Div)

VDDQ VID Change



Time (100μs/Div)

17 Operation

The RT6300C/RT6300CH/RT6300D/RT6300DH is an integrated power solution comprising two high-efficiency synchronous buck converters for VDD2H and VDDQ, a 0.92V/1.5A LDO for VDD2L, and a 1.8V/1A load switch for VDD1. The high-efficiency synchronous buck converters, VDD2H and VDDQ, utilize the proprietary Advanced Constant On-Time (ACOT®) control architecture, providing a very fast transient response. The ultra-fast ACOT® control enables the use of small output capacitance and optimizes the component size without an additional compensation network.

During normal operation, the high-side MOSFET turns on with a fixed one-shot on-time timer after the beginning of each clock cycle. The inductor current linearly increases when the high-side MOSFET turns on and the low-side MOSFET turns off. Similarly, the inductor current linearly decreases when the high-side MOSFET turns off and the low-side MOSFET turns on. The voltage ripple on the output has a similar shape to the inductor current due to the output capacitor ESR.

The feedback voltage ripple, compared with an internal reference, is captured by the output feedback pin. When a fixed minimum off-time timer times out and the inductor valley current is below the valley current-limit threshold, the fixed one-shot one-time timer is triggered if the feedback voltage falls below the feedback reference voltage. Therefore, the output voltage is regulated through the previously mentioned principle.

17.1 ACOT® Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated within the IC. The internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Conventional COT control implements the on-time timer proportional to V_{OUT} and inversely proportional to V_{IN} to achieve pseudo-fixed frequency with a wide VIN range. A fixed on-time timer in conventional COT control has no compensation for the voltage drop of the MOSFETs and the inductor during higher load conditions.

In order to address the voltage drop of MOSFETs and the inductor without influencing the fast transient behavior of the COT topology, a frequency-locked loop system with slowly adjusting on-time timer is further added to the ACOT® control.

17.2 Average Output Voltage Control Loop

In continuous conduction mode, conventional COT control has a DC offset between $V_{FB(average)}$ and V_{REF}, as shown in Figure 1. In order to cancel the DC offset, the RT6300C/RT6300CH/RT6300D/RT6300DH provides an average output voltage control loop to adjust the comparator input V_{REF}. Hence, the $V_{FB(average)}$ always follows the designed value. The control loop efficiently improves the load and line regulation without affecting the transient performance.

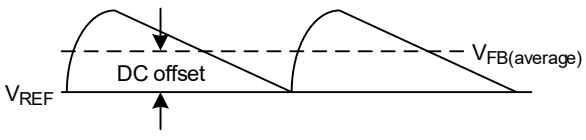


Figure 1. Conventional COT Control Loop Operation

17.3 Diode Emulation Mode (DEM)

In diode emulation mode, the RT6300C/RT6300CH/RT6300D/RT6300DH automatically and smoothly reduces the switching frequency at light-load conditions. As the output current decreases from heavy load to light load, the inductor current is naturally reduced. Once the valley point of the inductor current reaches zero during the decreasing output current, the behavior is the boundary mode between continuous conduction mode and discontinuous conduction mode. In order to emulate the behavior of a free-wheeling diode, the device only allows partial negative current flow from the drain to the source of the low-side MOSFET when the inductor free-wheeling current becomes negative.

During decreasing the output current, the discharge time of the output capacitor is gradually longer. When the voltage on the output capacitor is lower than the reference regulating voltage, the next one-shot on-time timer is activated. On the contrary, when the output current increases from light load to heavy load and the inductor current finally reaches the continuous conduction, the switching frequency smoothly increases to the preset value. The boundary load condition between continuous conduction mode and discontinuous conduction mode is shown in Figure 2 and is calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times t_{ON}$$

where I_{LOAD} is the output loading current and t_{ON} is the on-time.

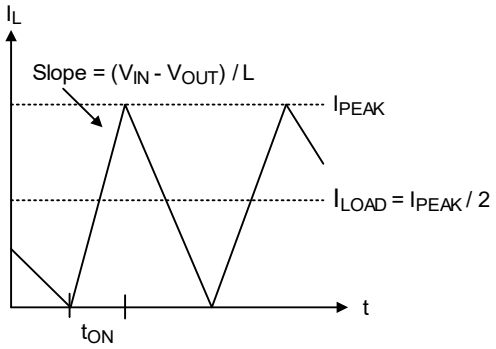


Figure 2. Boundary Condition of CCM/DEM

As mentioned above, the diode emulation mode features naturally high efficiency under light-load conditions. In DEM operation (assuming the coil resistance remains fixed), a low inductor value has high efficiency and high output voltage ripple. However, a high inductor value features low efficiency and reduces output voltage ripple. The drawback of using a high inductor value includes a larger physical size and a slower load transient response (especially at low input voltage levels).

17.4 EN, EN_VDDQ, and VSEL Pins Sink Current

The RT6300C/RT6300CH/RT6300D/RT6300DH does not permit uncertain voltages on the EN, EN_VDDQ, or VSEL pins, as these may lead to logic or behavioral errors in the device. To prevent these pins from floating, the RT6300C/RT6300CH/RT6300D/RT6300DH incorporates an internal 0.3μA pull-down current to eliminate any floating voltages.

17.5 VDD1 and VDD2L Current Limit

The current limit circuitry prevents damage to the power switch MOSFET and the backend device. The current limit circuit monitors the current of the path from input to output using a current sensing circuit and controls the pass transistor's gate voltage. When the path current exceeds the current limit, the current limit circuit adjusts the gate voltage to limit the output current.

17.6 VDD2H and VDDQ Valley Current Limit

The RT6300C/RT6300CH/RT6300D/RT6300DH features a cycle-by-cycle valley current limit for avoiding large output currents and overheating. The device cycle-by-cycle compares the valley current of the inductor with the valley current-limit threshold. The output current is limited to the sum of the valley current and half of the ripple current when the inductor valley current reaches valley current-limit threshold.

After the device completes the minimum off-time and keeps the ON state of the low-side MOSFET, the inductor valley current level is monitored by measuring the low-side MOSFET voltage between the SW pin and PGND pin during the ON state of the low-side MOSFET. During the ON state of the low-side MOSFET, the measured low-side MOSFET voltage is proportional to the low-side MOSFET current. In order to improve the accuracy of the measured current, the temperature compensation circuit is built internally.

In order to prevent the device from overcurrent, if the measured low-side MOSFET current is higher than the valley current-limit threshold, the device remains the low-side MOSFET in the ON state and the one-shot on-time timer is inhibited until its current linearly decreases lower than the valley current-limit threshold. Once the low-side MOSFET current is below the valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle valley current limit works in every switching cycle.

17.7 Output Undervoltage Protection (UVP)

The RT6300C/RT6300CH/RT6300D/RT6300DH implements output UVP to prevent the end device from low voltage operation. If the valley current of the inductor (VDD2H/VDDQ) or the output current (VDD1/VDD2L) is higher than the current-limit threshold during heavy-load conditions, the output voltage tends to drop because the load demand exceeds that the converters (VDD2H/VDDQ), LDO (VDD2L), or load switch (VDD1) can support.

When the load demand is larger than the current ability, the V_{OUT_VDD2H}, V_{OUT_VDDQ}, V_{OUT_VDD1}, and V_{OUT_VDD2L} begin to decrease. If one of the voltages V_{OUT_VDD2H}, V_{OUT_VDDQ}, V_{OUT_VDD1}, and V_{OUT_VDD2L} drops below 60% of the target voltage and the time length of this state is larger than the time width 20μs (typical), the UVP is triggered. Once UVP is triggered, the IC stops switching and shuts down all rails using the discharge function.

17.8 VDD2H, VDD2L, and VDDQ Output Overvoltage Protection (OVP)

The RT6300C/RT6300CH/RT6300D/RT6300DH implements output OVP to prevent the end device from overvoltage operation. If one of the voltages V_{OUT_VDD2H} (VDD2H), V_{OUT_VDDQ} (VDDQ), and V_{OUT_VDD2L} (VDD2L) rises above 125% of the target voltage and the time length of this state is larger than the time width 20μs (typical), the OVP is triggered.

Once OVP is triggered, the IC stops switching and shuts down all rails using the discharge function.

17.9 Over-Temperature Protection (OTP)

The RT6300C/RT6300CH/RT6300D/RT6300DH implements OTP circuitry to prevent the device from overheating due to excessive power dissipation. If the junction temperature of the device exceeds a typical 150°C, the OTP is triggered to stop the temperature rising. Once the OTP is triggered, the IC shuts down all rails using the discharge function.

17.10 Input Undervoltage-Lockout (UVLO)

The RT6300C/RT6300CH/RT6300D/RT6300DH provides an Undervoltage-Lockout (UVLO) function that monitors the input voltage. In order to protect the device from operating at insufficient input voltage, the UVLO function inhibits switching when the input voltage drops below the UVLO falling threshold.

17.11 Protection Mode

The RT6300 series includes two models: Latch Mode (RT6300C/RT6300D) and Hiccup Mode (RT6300CH/RT6300DH). Refer to Table 3 for the protection modes corresponding to VDD1, VDD2H, VDD2L, and VDDQ.

Table 3. Protection Table

Part number	OTP	VCC UVLO	VDD1_VIN UVLO	VDD2H_VIN UVLO	VDD2L_VIN UVLO	VDDQ_VIN UVLO	UVP (Note 11)	OVP (Note 12)
RT6300C	Latch	Auto-recovery	Latch	Latch	X (Note 10)	Auto-recovery	Latch	Latch
RT6300CH	Auto-recovery	Auto-recovery	Auto-recovery	Auto-recovery	X (Note 10)	Auto-recovery	Auto-recovery	Auto-recovery
RT6300D	Latch	Auto-recovery	Latch	Latch	X (Note 10)	Auto-recovery	Latch	Latch
RT6300DH	Auto-recovery	Auto-recovery	Auto-recovery	Auto-recovery	X (Note 10)	Auto-recovery	Auto-recovery	Auto-recovery

Note 10. "X" is not implemented.

Note 11. It refers to the UVP of all rails.

Note 12. It refers to the OVP of all rails.

17.12 VSEL Logic Control

The VSEL pin of the RT6300C/RT6300CH/RT6300D/RT6300DH provides a 1-bit VID function to dynamically adjust the target voltage of VDDQ. If the voltage of VSEL is larger than 1.2V, the VDDQ output voltage is 0.52V. If the voltage of VSEL is less than 0.4V, the VDDQ output voltage is 0.32V. For the VSEL control logic, refer to Table 4.

Table 4. VSEL Control Logic

VSEL Logic Status	VDDQ Output Voltage
1	0.52V
0	0.32V

Note 13. VSEL: Logic = 1 means V_{SEL} > 1.2V. Logic = 0 means V_{SEL} < 0.4V.

17.13 EN and EN_VDDQ Logic Control

The EN and EN_VDDQ pins integrate enable control and mode selection (S0, S3, and S4/S5) for the RT6300C/RT6300CH/RT6300D/RT6300DH. If the voltage of EN and EN_VDDQ is greater than 1.2V, all the rails are turned on (S0). If the voltage of EN is greater than 1.2V and the voltage of EN_VDDQ is less than 0.4V, VDD1, VDD2H, and VDD2L are turned on, while VDDQ is turned off (S3). Moreover, regardless of the logic state of EN_VDDQ, if the EN voltage is less than 0.4V, all the rails are turned off (S4/S5 or other). For the EN and EN_VDDQ control logic, refer to Table 5.

Table 5. EN and EN_VDDQ Control Logic

0 = Logic low, 1 = Logic high, ON = Active, OFF = Inactive						
State	EN	EN_VDDQ	VDD1	VDD2H	VDD2L	VDDQ
S0	1	1	ON	ON	ON	ON
S3	1	0	ON	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF	OFF
Other	0	1	OFF	OFF	OFF	OFF

Note 14. EN: Logic = 1 means V_{EN} > 1.2V. Logic = 0 means V_{EN} < 0.4V.

EN_VDDQ: Logic = 1 means V_{EN_VDDQ} > 1.2V and Logic = 0 means V_{EN_VDDQ} < 0.4V

17.14 Soft-Shutdown and Internal Output Voltage Discharge

When EN or EN_VDDQ is pulled low, the VDDQ ramps down using a soft shutdown function, while the other rails use an output voltage discharge function to discharge their output to GND. Moreover, the output voltage discharge function, which includes VDD1, VDD2H, VDD2L, and VDDQ, utilizes an internal MOSFET 10Ω (typical). The internal MOSFET is enabled when any of the following events are triggered:

- Input undervoltage-lockout (UVLO)
- Output undervoltage/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)

17.15 Power-Good Indicator (PG)

The PG pin is an open-drain output. An external pull-up resistor to VCC or another external rail is required, and the recommended pull-up resistor ranges from 10kΩ to 100kΩ. Do not pull the PG voltage higher than 6V. In order to prevent unwanted PG glitches during load transients or dynamic V_{OUT} changes, the RT6300C/RT6300CH/RT6300D/RT6300DH provides a PG low deglitch time with typical 20μs.

The PG pin is pulled low when any of the following specified events are triggered:

- Input undervoltage-lockout (UVLO)
- Output undervoltage/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN pin is pulled low
- Soft-start is not completed
- The VOUT pin voltage is lower than the PG falling threshold (PG rising threshold minus PG hysteresis voltage) of the target voltage

17.16 Soft-Start Function

The RT6300C/RT6300CH/RT6300D/RT6300DH provides an internal soft-start function to prevent large input inrush currents and output voltage overshoot. If the EN and EN_VDDQ voltages and input voltages of each power rail exceed their respective rising thresholds, the soft-start function is activated. The V_{OUT} starts to track the internal reference voltage, ranging from zero to the target.

17.17 Power-On and Power-Off Sequences

The power sequence of the RT6300C/RT6300CH/RT6300D/RT6300DH can always meet the JEDEC power-on and power-off standard requirements by controlling the EN and EN_VDDQ pins. The detailed power-on and power-off sequences diagrams are shown in Figure 3 to Figure 11.

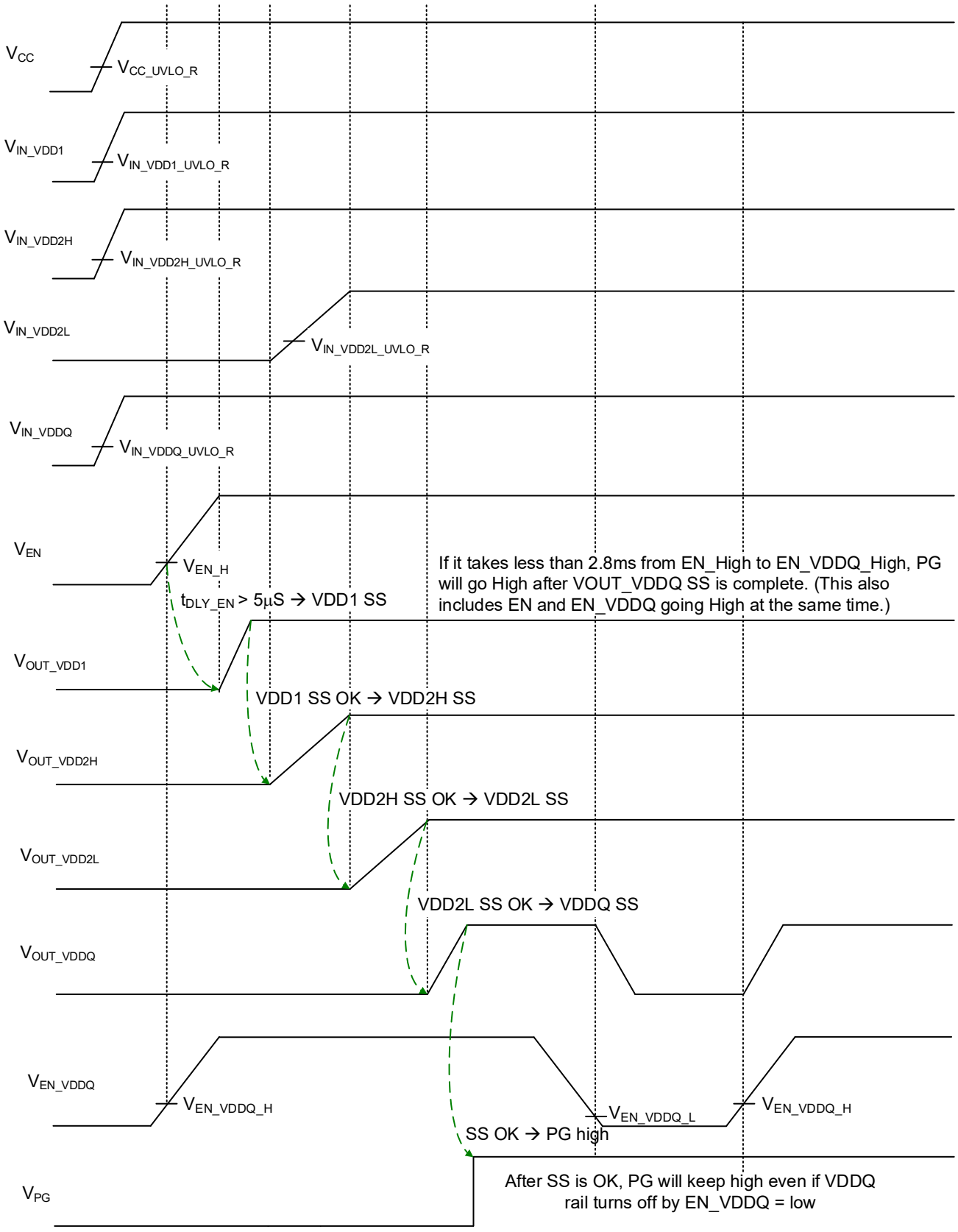


Figure 3. Power-On Sequence-I

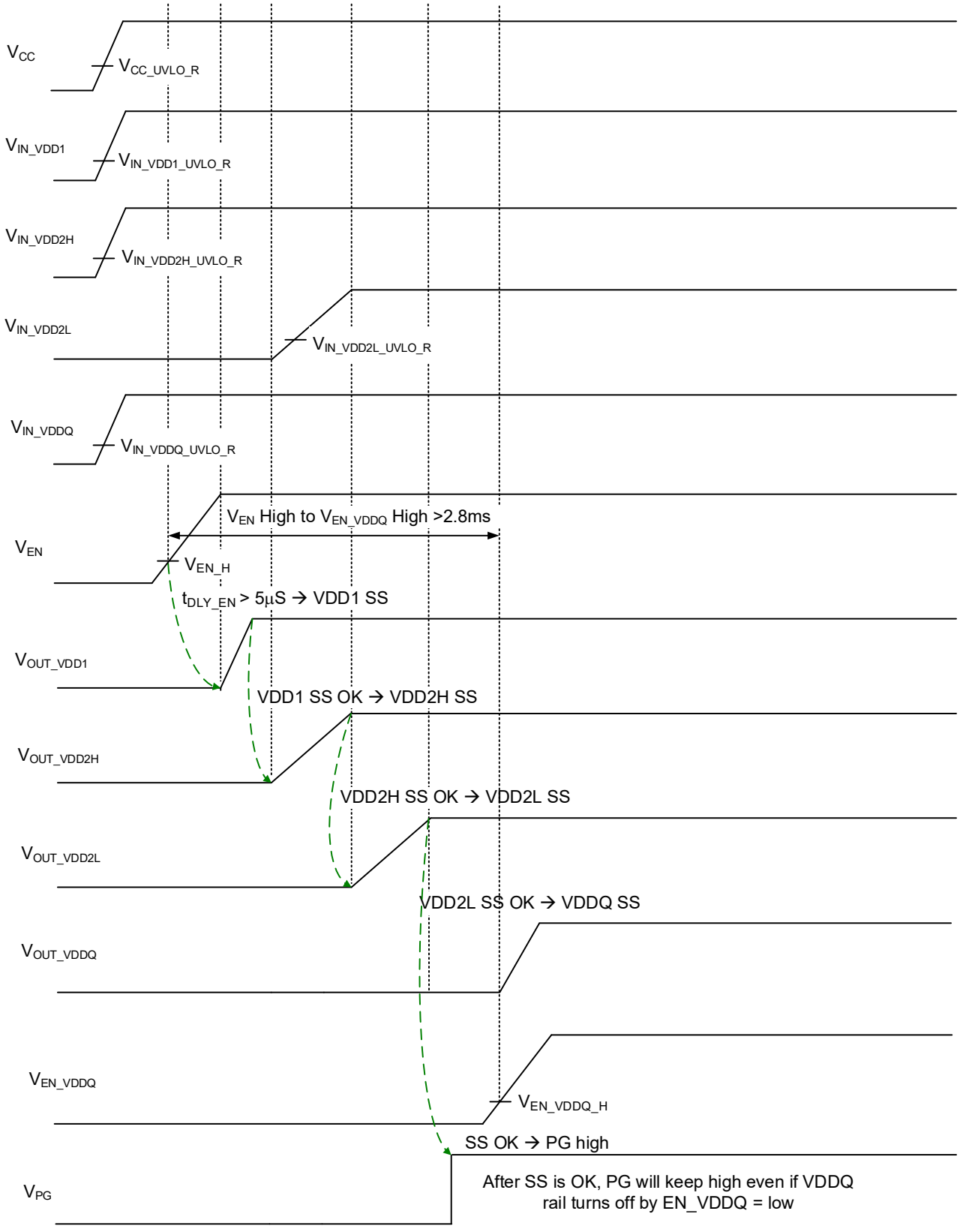


Figure 4. Power-On Sequence-II

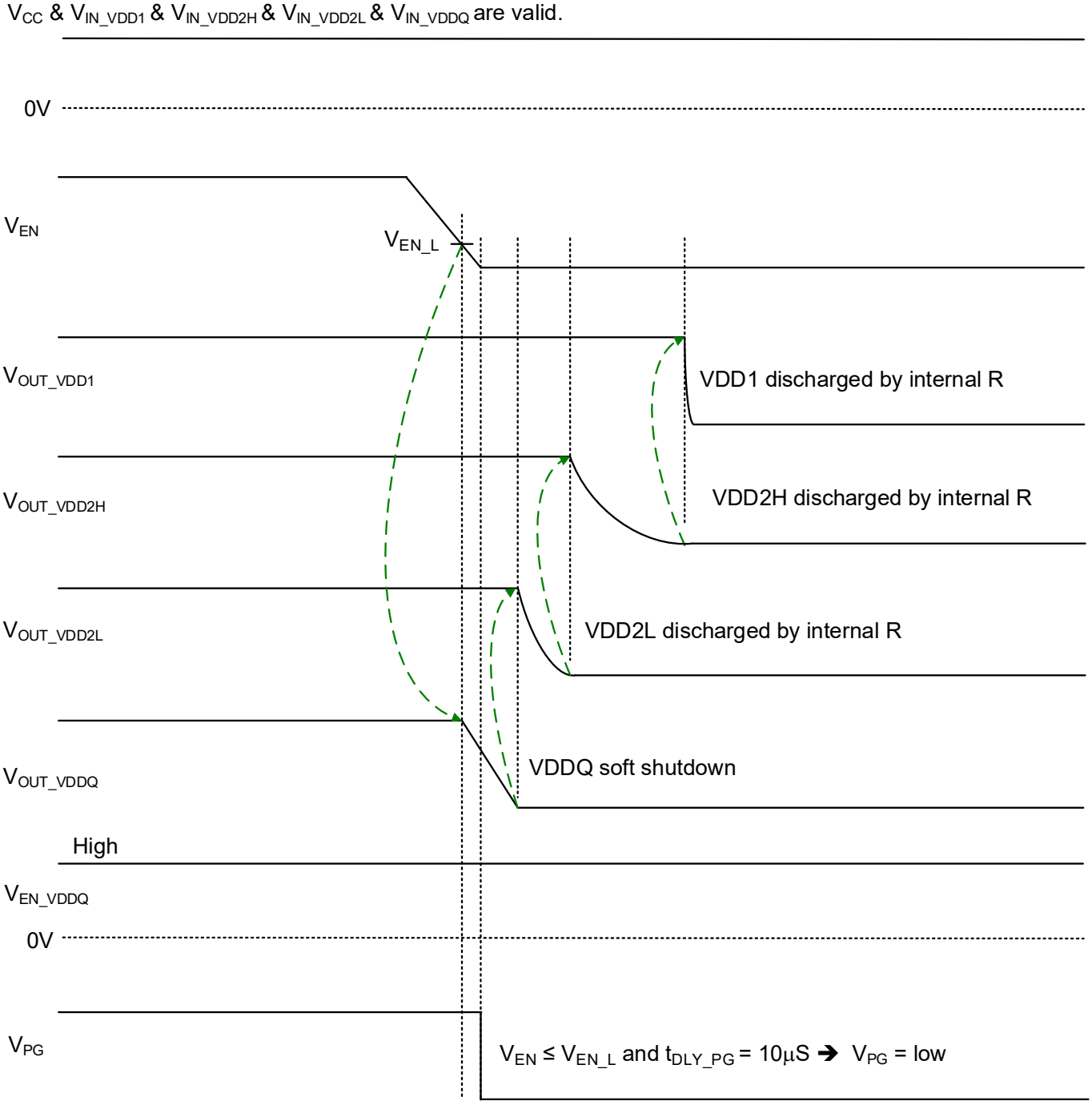


Figure 5. Power-Off Sequence

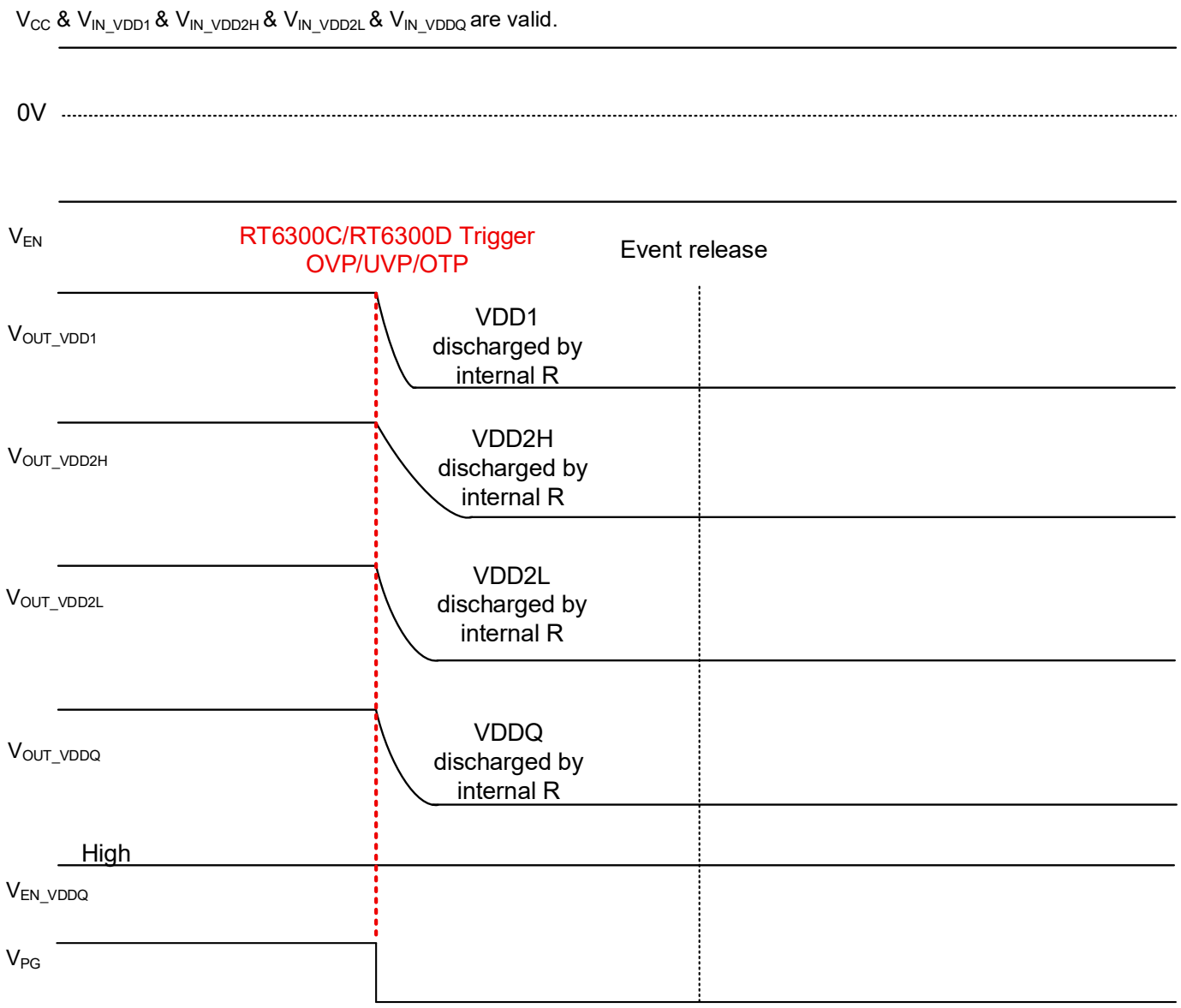


Figure 6. OVP/UVP/OTP Event Trigger Sequence for RT6300C and RT6300D

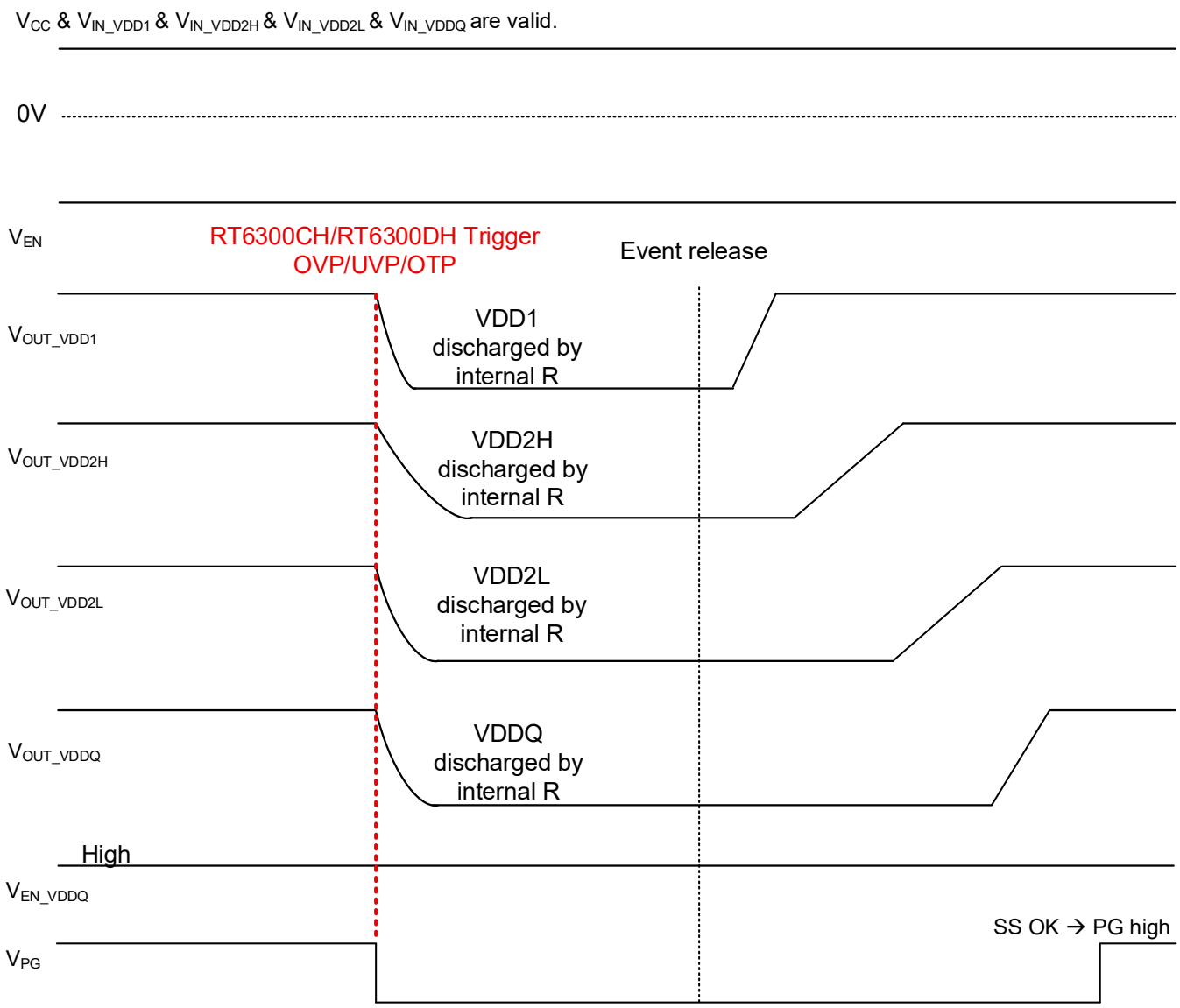


Figure 7. OVP/UVP/OTP Event Trigger Sequence for RT6300CH and RT6300DH

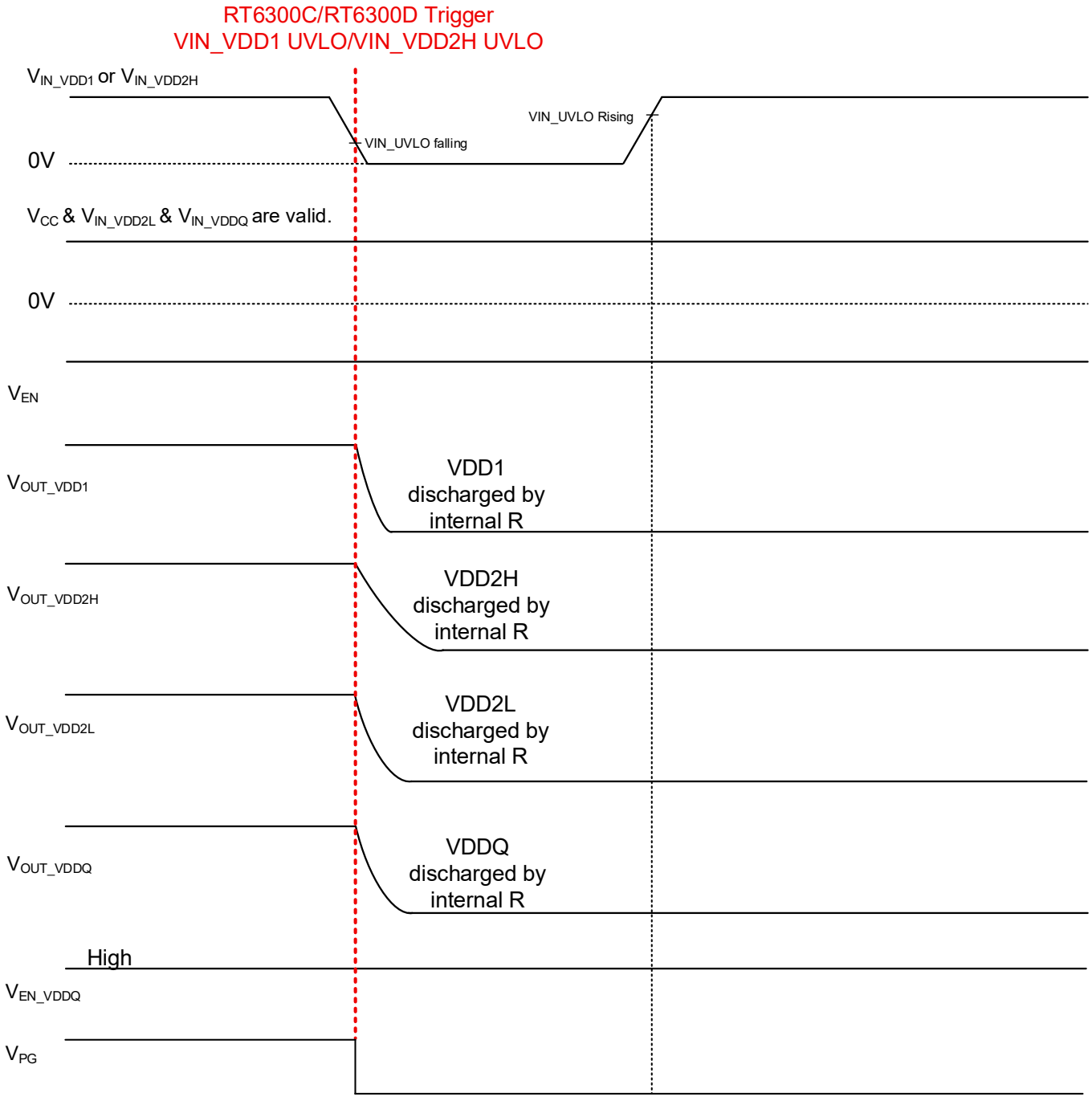


Figure 8. VIN_VDD1 UVLO/VIN_VDD2H UVLO Event Trigger Sequence for RT6300C and RT6300D

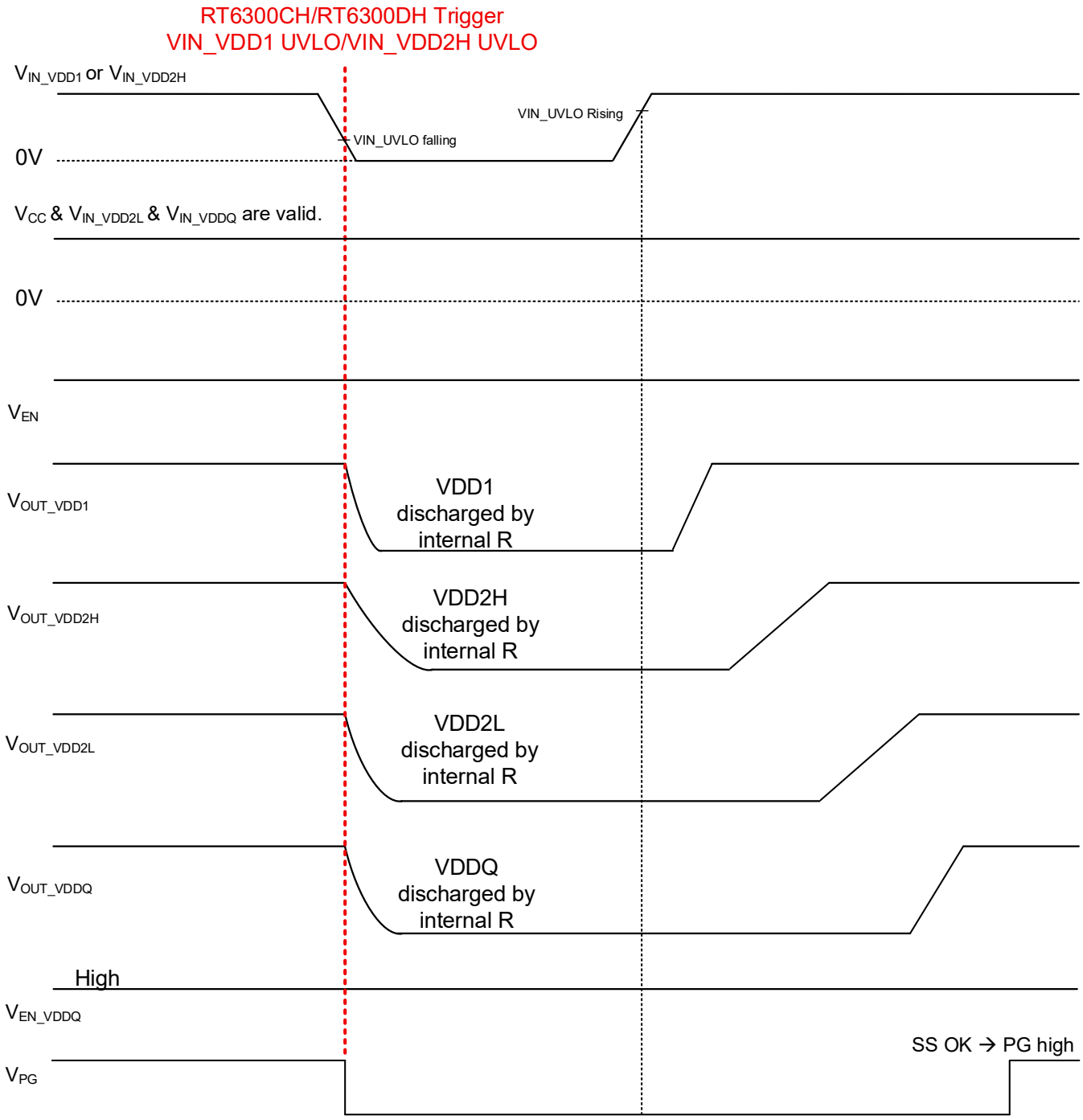


Figure 9. VIN_VDD1 UVLO/VIN_VDD2H UVLO Event Trigger Sequence for RT6300CH and RT6300DH

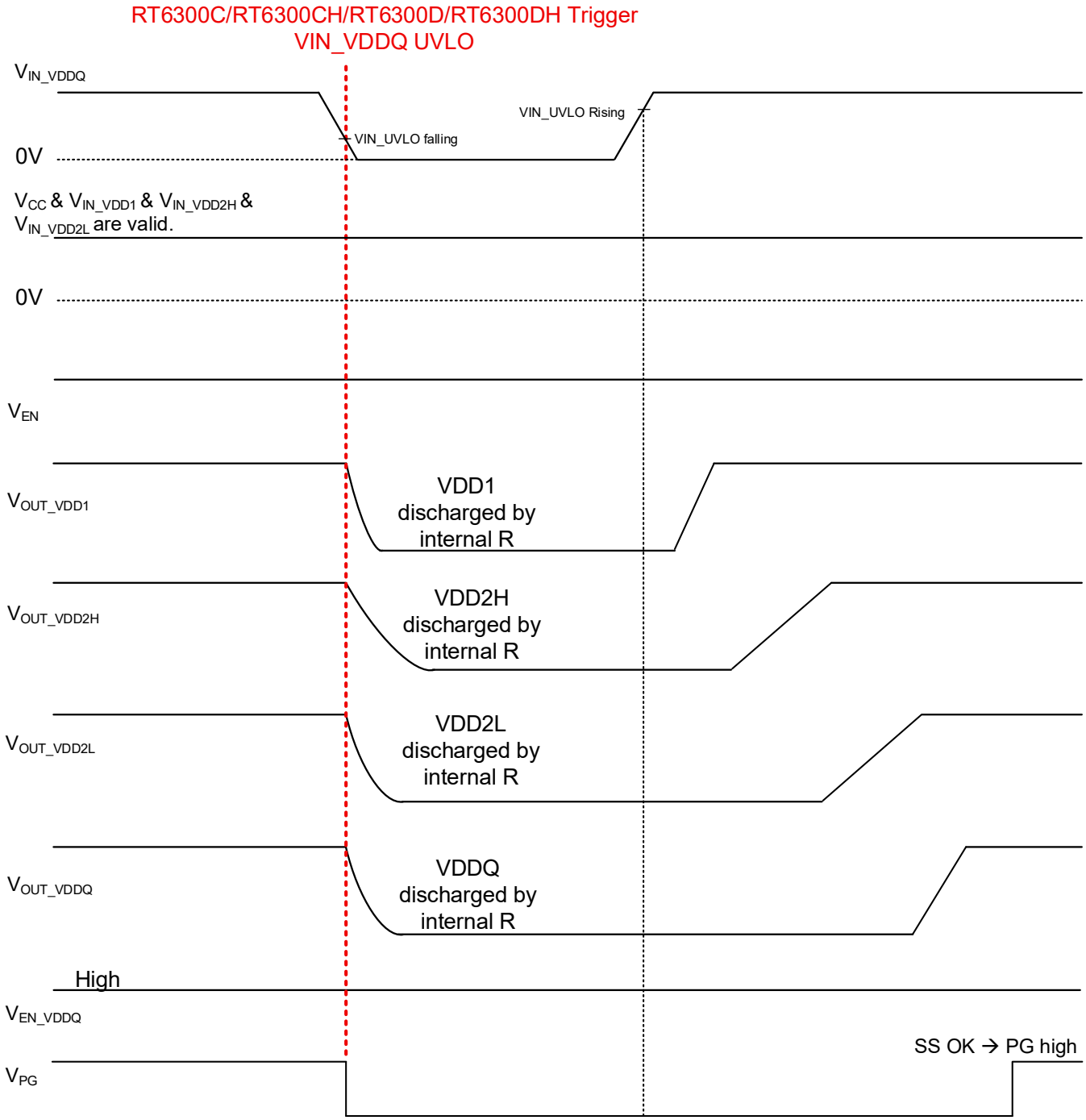


Figure 10. VIN_VDDQ UVLO Event Trigger Sequence for RT6300C, RT6300CH, RT6300D, and RT6300DH

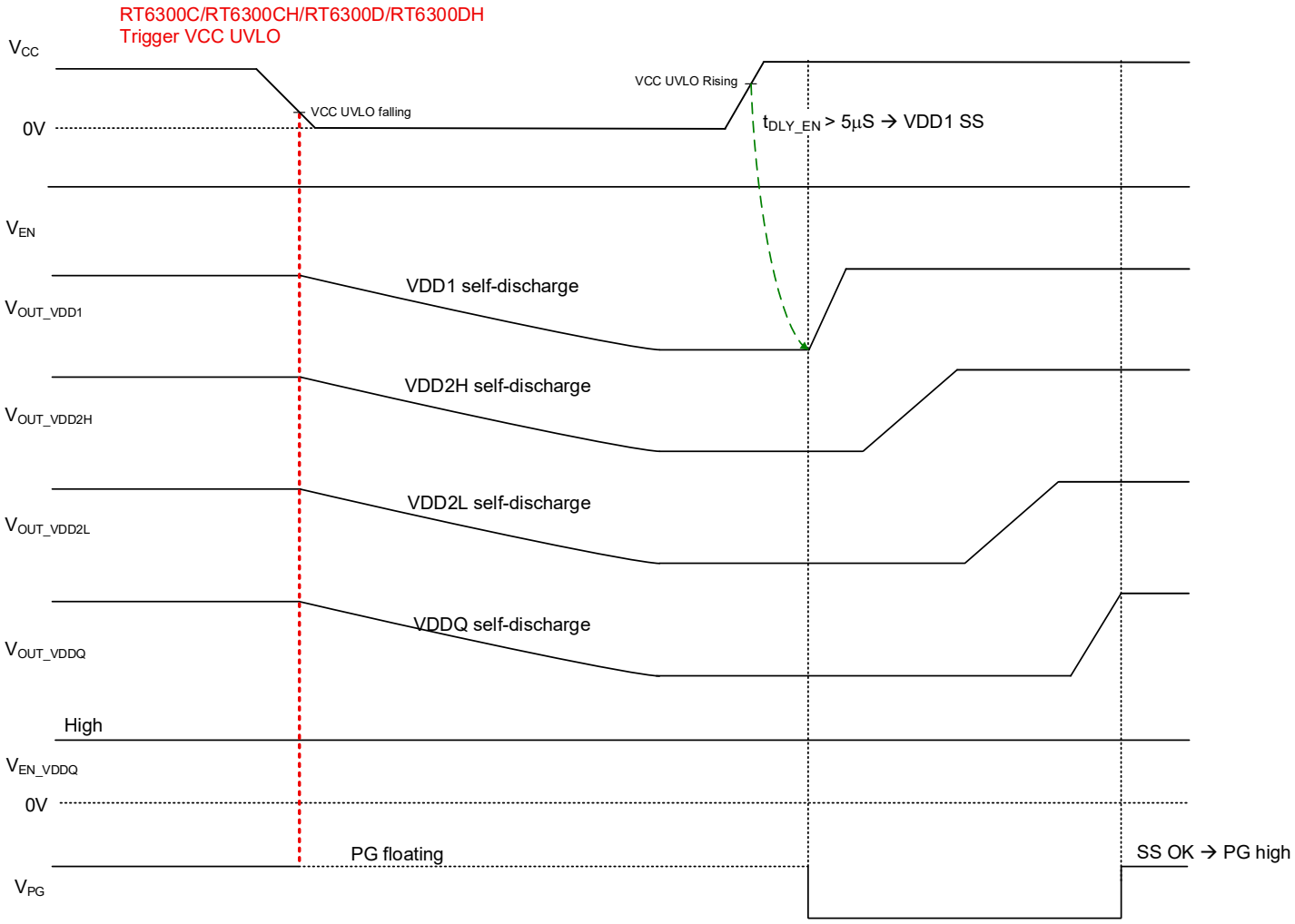


Figure 11. VCC_UVLO Event Trigger Sequence for RT6300C, RT6300CH, RT6300D, and RT6300DH

18 Application Information

(Note 15)

A general application circuit for the RT6300C/RT6300CH/RT6300D/RT6300DH is shown in the Typical Application Circuit section. The external component selection is primarily determined by the load requirements. In this section, the key external components such as the inductor L, the input capacitor C_{IN}, the output capacitor C_{OUT}, the external V_{CC} capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} are introduced.

18.1 Inductor Selection

Inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L relative to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but slightly degraded transient response. Lower inductance values allow for a smaller case size, but the larger ripple current increases the AC losses in the inductor. To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits within the allotted dimensions. The inductor value determines not only the ripple current but also the load current boundary between DEM and CCM.

In applications, the RT6300C/RT6300CH/RT6300D/RT6300DH may encounter events such as power-on inrush current (due to capacitive load or heavy load) and output overloading. The RT6300C/RT6300CH/RT6300D/RT6300DH provides valley current-limit protections to prevent the device from damages. Moreover, to make the current-limit protection effective, the saturation current rating of the inductor must be greater than the valley current limit of the RT6300C/RT6300CH/RT6300D/RT6300DH.

18.2 Input Capacitor Selection

Input capacitance (C_{IN}) is needed to filter the pulsating current at the drain of the high-side MOSFET. The large ripple voltage on the VIN pin must be minimized by C_{IN}. The peak-to-peak voltage ripple on the input capacitor is estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times R_{ESR}$$

where R_{ESR} is the equivalent series resistance of C_{IN} and

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, so the ripple caused by ESR can be ignored. The minimum input capacitance is estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D \times (1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

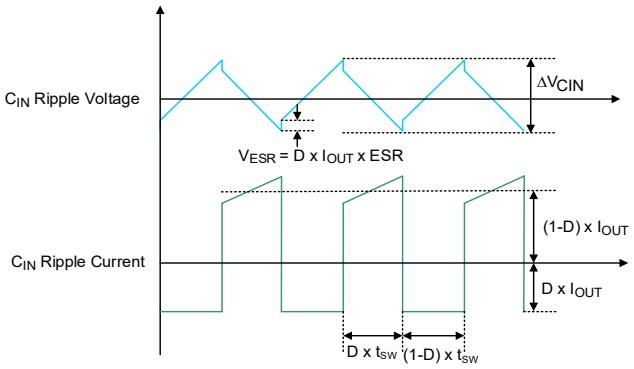


Figure 12. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worst-case $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. Therefore, the de-rating of capacitors is worse in actual applications. Selecting capacitors with higher temperature rating is required to reduce de-rating.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality factor (under-damped) tank circuit. If the RT6300C/RT6300CH/RT6300D/RT6300DH circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitor of 0.1μF should be placed close to the VIN pin. The capacitor should be 0402 or 0603 in size.

18.3 Output Capacitor Selection

The selection of C_{OUT} should satisfy the voltage ripple, transient loads, and ensure that control loop is stable. Loop stability can be checked by observing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, which are expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where ΔI_L is the peak-to-peak inductor ripple current, and R_{ESR} is the equivalent series resistance of C_{OUT}.

The output ripple is highest at the maximum input voltage since ΔI_L increases with the input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which is calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage is determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

When the load is removed, the amount of overshoot due to stored inductor energy is calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.4 External Vcc Capacitor

Good bypassing at the VCC pin is necessary to supply the high transient currents required by the MOSFET gate drivers. Place a low ESR MLCC capacitor (C = 4.7μF/0603) as close as possible to the VCC pin and the AGND pin. Do not connect the VCC pin to provide power to other devices or loads.

18.5 External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF/0603 low ESR ceramic capacitor and a ≤ 10Ω resistor between the BOOT pin and the SW pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side MOSFET. The internal gate driver is optimized to turn the high-side MOSFET on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Most of the EMI occurs since V_{SW} rises rapidly when the high-side MOSFET is turned on fast. In some cases, slightly increasing the R_{BOOT} reduces EMI and the SW pin spike directly, but the switching loss of the high-side MOSFET and die/case temperature are also increased.

18.6 Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WQFN-19L 3x3 (FC package, the thermal resistance, $\theta_{JA(EVB)}$, is 34.31°C/W on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (34.31°C/W) = 2.91W for a WQFN-19L 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curve in Figure 13 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

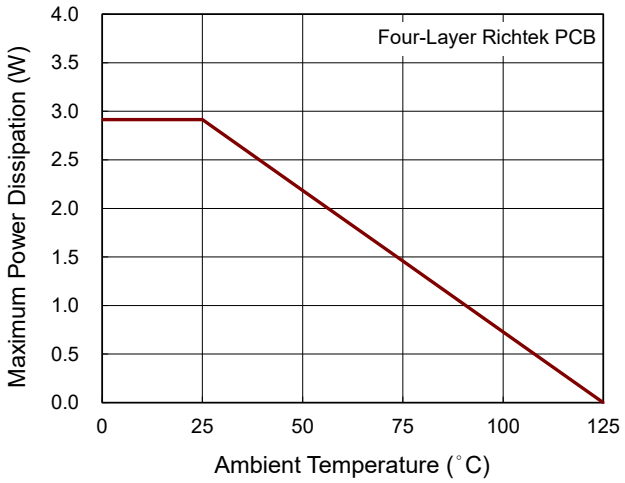


Figure 13. Derating Curve of Maximum Power Dissipation

18.7 Layout Considerations

Printed circuit board (PCB) layout design for switch-mode power supply ICs is critical and important. An improper PCB layout brings lots of problems in the power supply, such as poor output voltage regulation, switching jitter, bad thermal performance, excessive radiated noise, and reduced component reliability. To avoid these issues, designers have to understand the current trace and signal flow in the switching power supply. The following are design considerations of PCB layout for switching power supplies:

- For suppressing phase ringing and extra power losses that affect device reliability, the input capacitors must be placed close to the VIN pin to reduce the influence of parasitic inductance.
- For thermal stress and power consumption considerations, the current paths of V_{IN} and V_{OUT} should be as short and wide as possible to decrease the trace impedance.

- Since the SW node voltage swings from V_{IN} to 0V with very fast rising and falling times, switching power supplies suffer quite serious EMI issues. To eliminate EMI problems, the inductor must be placed as close as possible to the IC to narrow the SW node area. Besides, the SW node should be arranged on the same plate to reduce coupling noise paths caused by parasitic capacitance.
- For system stability and coupling noise elimination, sensitive components and signals, such as control signals and feedback loops, should be kept away from the SW node.
- For enhancing noise immunity on the VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to the IC.
- The feedback signal path from V_{OUT} to the IC should be wide and kept away from high switching paths.
- The trace width and numbers of vias should be designed based on application current. Ensure the switching power supply has great thermal performance and good efficiency.
- To optimize regulation and enhance load transient performance, thereby reducing the number of required output capacitors, it is strongly recommended to place the output capacitors as close as possible to the feedback sensing node that is connected to the IC's feedback pin.

An example of a PCB layout guide is shown in Figure 14 for reference.

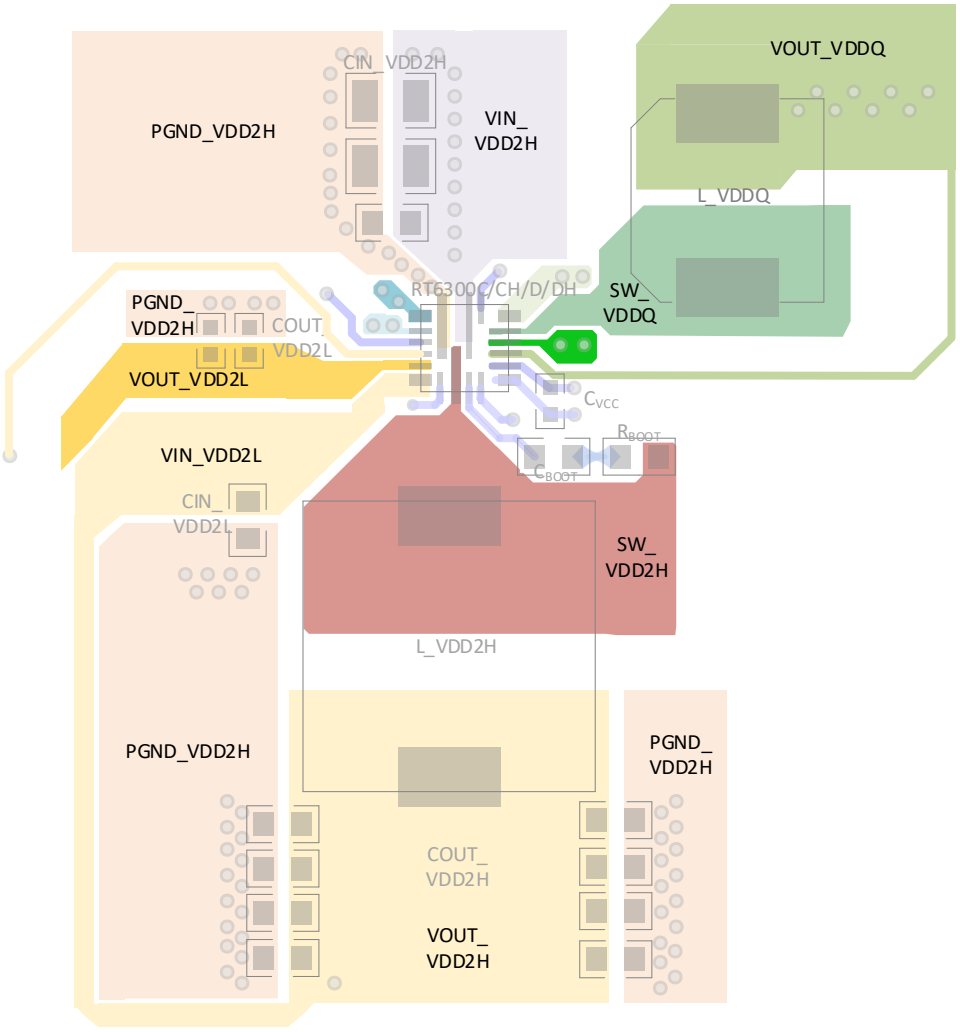


Figure 14. Layout Guide (Top Layer)

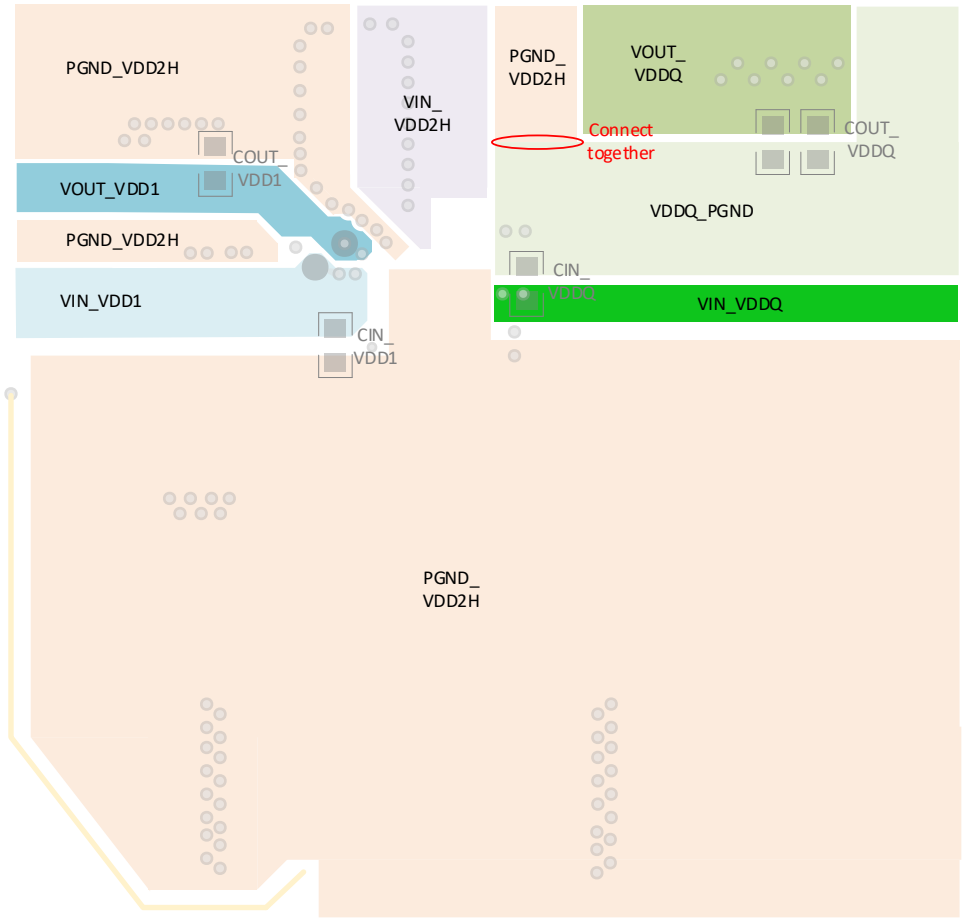
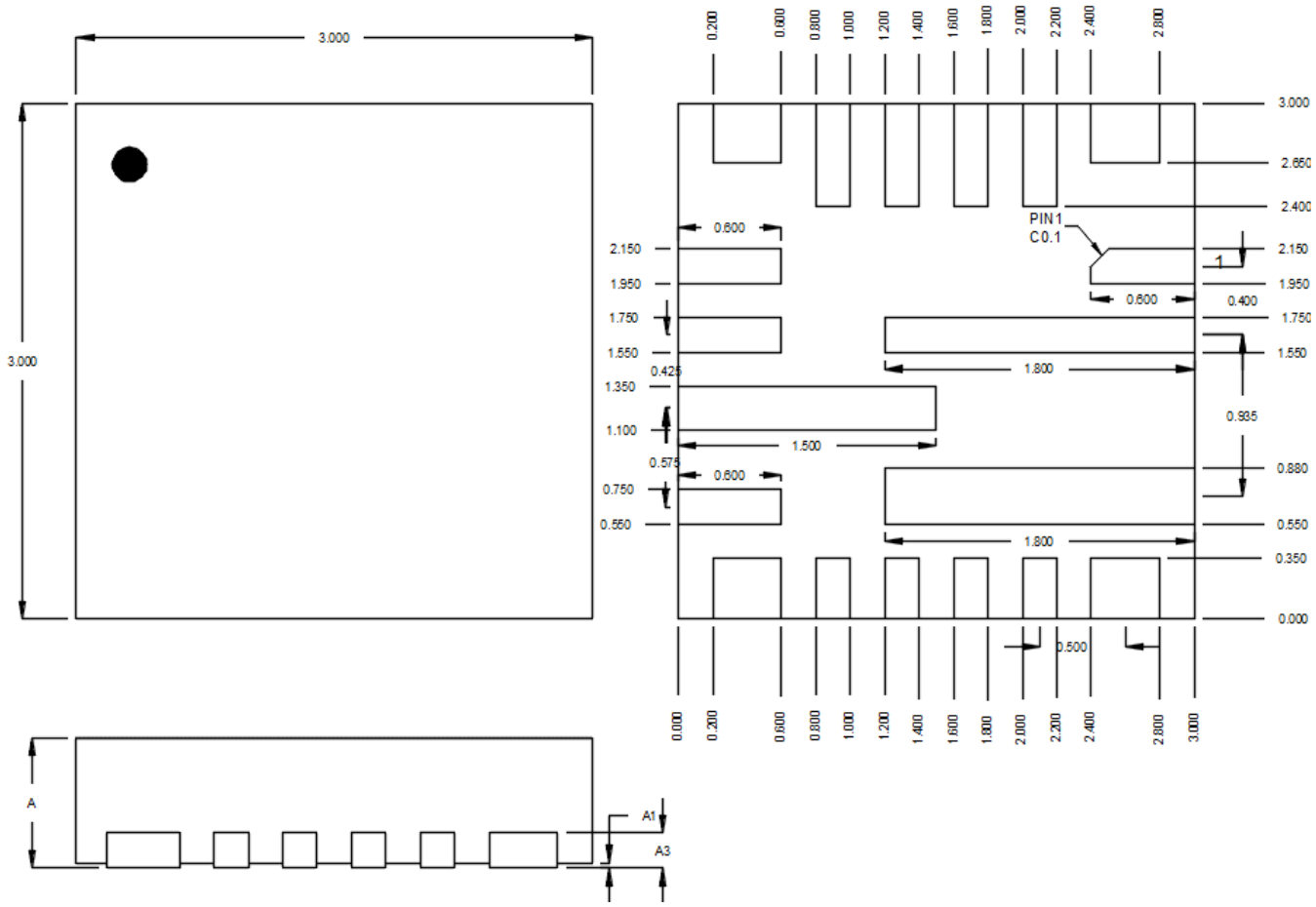


Figure 15. Layout Guide (Bottom Layer)

Note 15. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements..

19 Outline Dimension

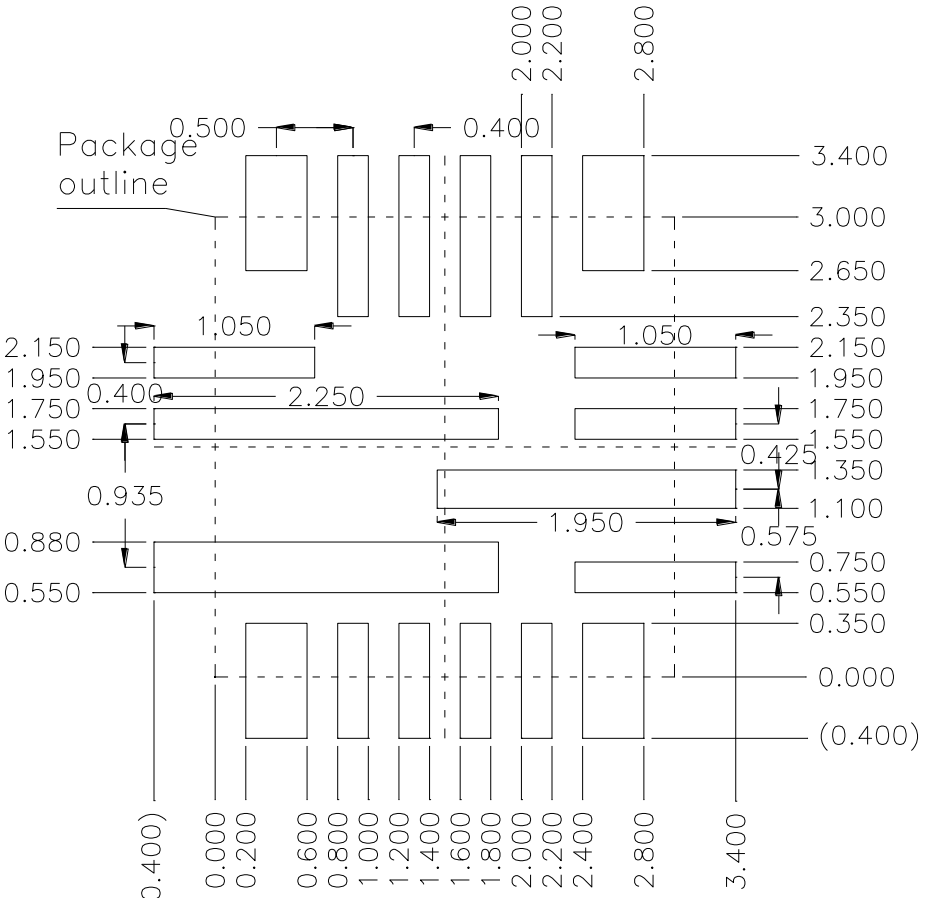


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

W-Type 19L QFN 3x3 Package (FC)

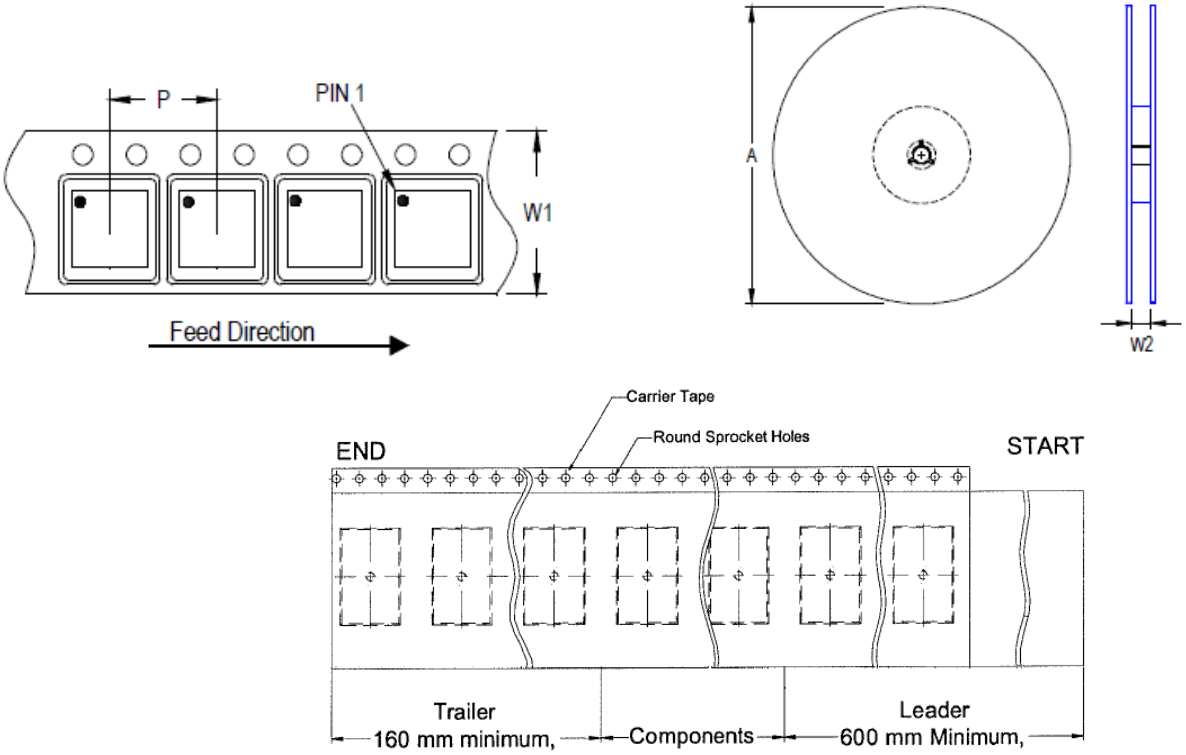
20 Footprint Information



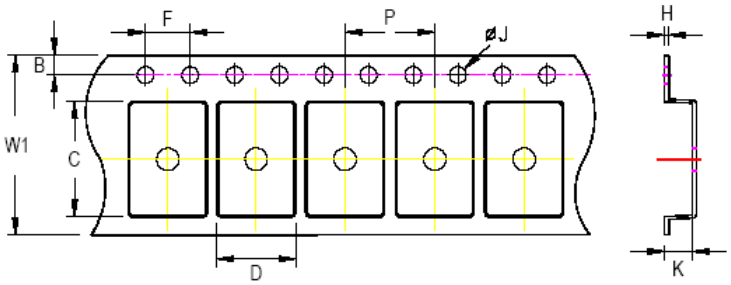
Package	Number of Pins	Tolerance
V/W/U/XQFN3x3-19(FC)	19	±0.05 mm

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
00	2025/7/22	*Marking Information on page 2* *Typical Application Circuit on page 15 to 19* *Application Information on page 31* *Functional Block Diagram on page 6* *Electrical Characteristics on page 8, 9*
01	2026/01/12	Thermal Information Typical Application Circuit Add more figures in Power-On and Power-Off Sequences.