RICHTEK®

RT6335A

23V, 14A High Efficiency Synchronous Buck Converter

1 General Description

The RT6335A is a synchronous buck converter with an output current that can achieve up to 14A of continuous current. It operates within an input voltage range of 4.5V to 23V and offers a fixed output voltage of 0.77V.

The RT6335A features an Advanced Constant On-Time (ACOT®) control architecture, which provides ultra-fast transient response and further reduces the external component count. In steady states, the ACOT® operates at nearly constant switching frequency over line, load, and output voltage ranges, making the EMI filter design easier.

The RT6335A offers programmable switching frequency, valley current limit. It also includes operating mode selection for DEM/FCCM, where DEM provides high light load efficiency and FCCM provides low output ripple voltage. Additionally, it provides a power-good indicator for easy system sequence control. Full protection features are integrated in the device, including Current-Limit Protection, OVP, UVP, input UVLO, and OTP.

All above functions are integrated in a VQFN-19TL 3x4 (FC) package. The recommended junction temperature range is –40°C to 125°C.

2 Ordering Information

RT6335A□-□

Packing
B: Standard

Package Type(1)
N: VQFN-19TL 3x4 (FC) (V-Type)

Note 1.

Marked with (1) indicated: Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

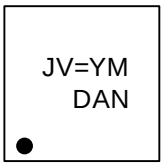
3 Features

- **Optimized for VNNAON Application**
- **Input Voltage Range: 4.5V to 23V**
- **14A Continuous Output Current**
- **Output Voltage: 0.77V**
- **ACOT® for Fast Transient**
- **Stable with POSCAP and MLCC Capacitor**
- **Internal Power MOSFETs: 12mΩ/4.8mΩ**
- **Selectable Design Parameters**
  - **Switching Frequency: 650k/850k/950k/1.1MHz**
  - **Valley Current Limit: 18.4A/23A/27.5A/31.9A**
  - **Operating Mode: DEM/FCCM**
- **Fault Protections: Current-Limit Protection, UVP, UVLO, OVP, and OTP**
- **Available in a VQFN-19TL 3x4 (FC) Package**

4 Applications

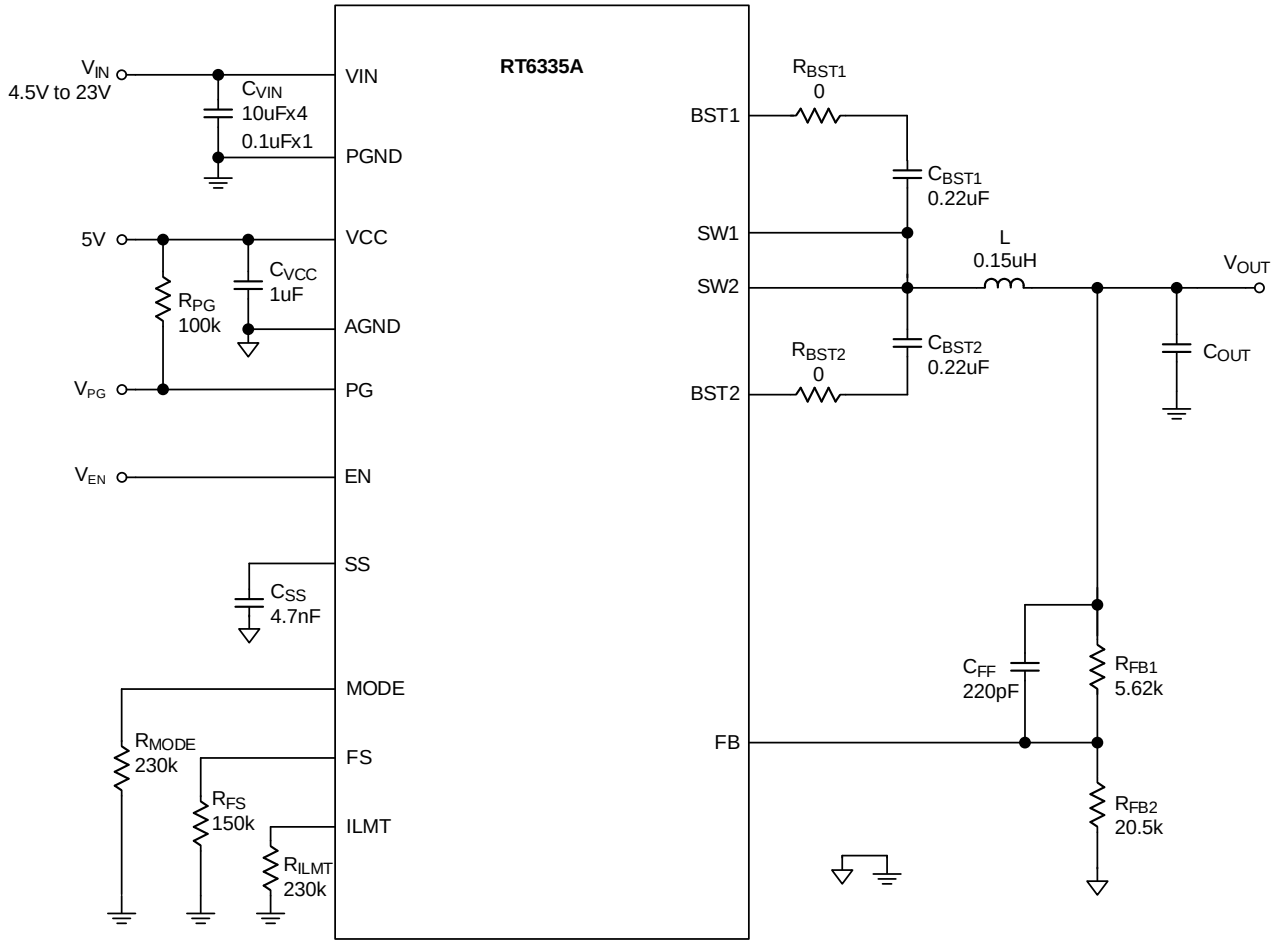
- Laptop Computers
- Intel VNNAON

5 Marking Information



JV=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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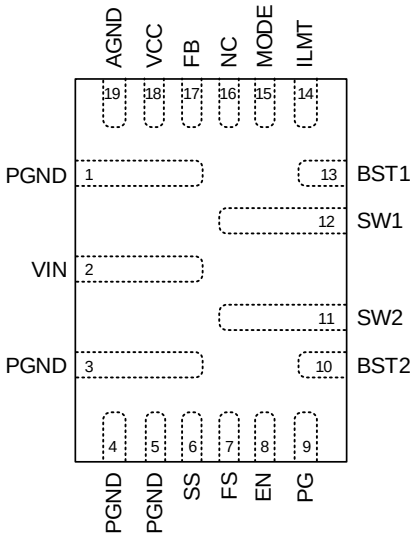
7 Pin Configuration

(TOP VIEW)



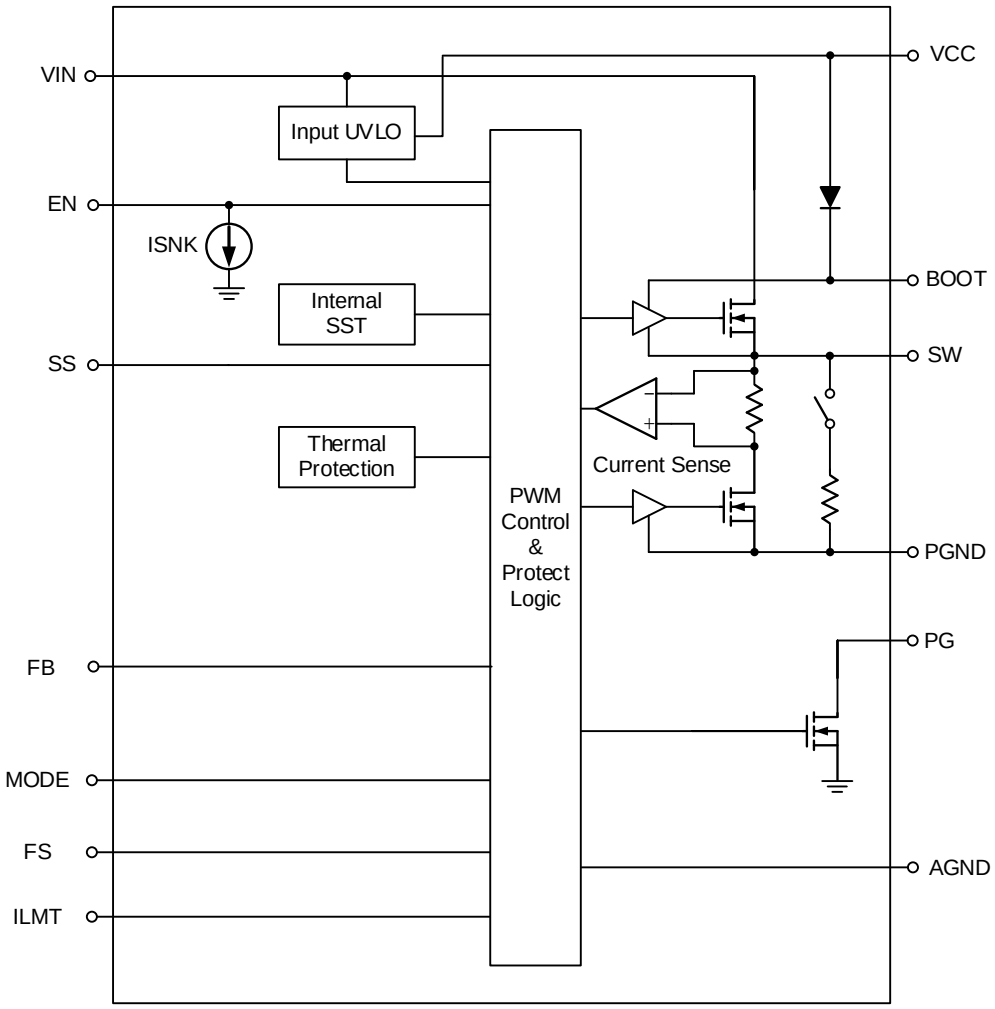
VQFN-19TL 3x4 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 3, 4, 5	PGND	Ground return from the low-side power MOSFET and its driver requires direct soldering to a large PCB PGND plane, along with the connection of thermal vias under the PGND pin. These steps are necessary to minimize parasitic impedance and thermal resistance.
2	VIN	Input voltage pin. The VIN pin is used to supply the internal MOSFETs. Use wide PCB traces and multiple vias to make the connection. Employ at least two layers for the input trace. It is essential to connect the ceramic capacitor (C = 10 μF/25V/0603x4 + 0.1μF/50V/0603x1) as close as possible to the VIN pin, ensuring a direct link to the PGND pin.
19	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
6	SS	Soft-start ramp output pin. Connect a capacitor 4.7nF from the AGND pin to the SS pin. DO NOT leave this pin floating.
7	FS	The FS pin is used for switching frequency selection. Connect a resistor from FS to PGND to set the switching frequency. Four different switching frequencies are available. 650kHz: R_{FS} = 0Ω 850kHz: R_{FS} = 90kΩ 950kHz: R_{FS} = 150kΩ 1100kHz: $R_{FS} \geq$ 230kΩ or floating
8	EN	Enable control input. DO NOT leave this pin floating. Device is enabled when EN pin is logic high (V_{EN} > 1.4V). Conversely, the device is disabled when the EN pin is logic low (V_{EN} < 0.7V).

Pin No.	Pin Name	Pin Function
9	PG	The power good (PG) indicator is an open-drain output with its gate connected to VIN. An external pull-up resistor must be connected to VCC or another suitable external rail, and the voltage should not exceed 6V. The recommended value for the pull-up resistor is between 10kΩ and 100kΩ. The pin is pulled low under the following conditions: when VIN or VCC is below the UVLO threshold, during output undervoltage protection (UVP) and overvoltage protection (OVP), when over-temperature protection (OTP) is triggered, when EN is logic-low, or when the output voltage is outside the predefined PG range. After the soft-start process is complete, the PG pin is pulled high if the output voltage is between 95% and 105% of the target voltage.
10	BST2	The second bootstrap supply for the high-side gate driver. Connect a high-quality, low ESR ceramic capacitor (minimum C = 0.1μF/0603) from the BOOT pin to the SW pin through short, low inductance paths. During the low-side MOSFET turn-on period, the bootstrap capacitor is charged by the BOOT pin to store the required energy for the high-side gate driver. It is recommended to use a bootstrap resistor (0603 size, 0Ω) in series with the bootstrap capacitor to reduce the voltage spike at the SW node.
11	SW2	The second switch node of the buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. SW1 and SW2 are used for internal ramp generation, on-time generation, and current detection. SW1 and SW2 must be connected first for paralleling the pair of high/low-side MOSFETs. Connect SW1 and SW2 pins to one inductor and keep the sensitive traces and signals away.
12	SW1	The first switch node of the buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. SW1 and SW2 are used for internal ramp generation, on-time generation, and current detection. SW1 and SW2 must be connected first for paralleling the pair of high/low-side MOSFETs. Connect SW1 and SW2 pins to one inductor and keep the sensitive traces and signals away.
13	BST1	The first bootstrap supply for the high-side gate driver. Connect a high-quality, low ESR ceramic capacitor (minimum C = 0.1 μF/0603) from the BOOT pin to the SW pin through short, low inductance paths. During the low-side MOSFET turn-on period, the bootstrap capacitor is charged by the BOOT pin to store the required energy for the high-side gate driver. It is recommended to use a bootstrap resistor (0603 size, 0Ω) in series with the bootstrap capacitor to reduce the voltage spike at the SW node.
14	ILMT	Valley current limit selection pin. Connect a resistor from the ILMT pin to the PGND pin to set the current-limit threshold. 18.4A: R_{ILMT} = 0Ω 23A: R_{ILMT} = 90kΩ 27.5A: R_{ILMT} = 150kΩ 31.9A: $R_{ILMT} \geq$ 230kΩ or floating
15	MODE	Mode selection pin. Connect a resistor from the MODE pin to the PGND pin to set the required operation mode. Refer to Table 2.
16	NC	No connection.
17	FB	Feedback voltage input. A voltage divider with R_{FB1}=5.62kΩ and R_{FB2}=20.5kΩ is recommended to set up the voltage to 0.77V. Furthermore, the FB pin is used to detect the output voltage status for OVP, UVP, or PG.
18	VCC	External voltage input for VCC. Connect an external 5V supply voltage for the internal analog control circuit and driver. To avoid any noise disturbance, including switching noise, the external 5V supply voltage must be stable and constant. Therefore, an RC filter (R = 2.2Ω /0603 and C = 1μF/0603) is necessary between the external 5V supply voltage and the VCC pin. It should be placed as close as possible to the VCC pin.

9 Function Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN to PGND ---------- –0.3 to 28V
- SW1/SW2 to PGND
  - DC ---------- –0.3 to (V_{IN}+0.3V)
  - AC (<10ns) ---------- –10 to 30V
  - AC (<5ns) ---------- –14 to 35V
- BST1/BTS2 to PGND
  - DC ---------- (V_{SW}–0.3V) to (V_{SW}+6V)
- Other Pins ---------- –0.3 to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Input Voltage, V_{IN} ---------- 4.5 to 23V
- VCC Supply Voltage, V_{CC} ---------- 4.5 to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

12 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		VQFN-19TL 3x4 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	52.57	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	27.40	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.15	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	26.91	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.62	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.76	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board (Richtek EVB) which is in size of 126mm x 80mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

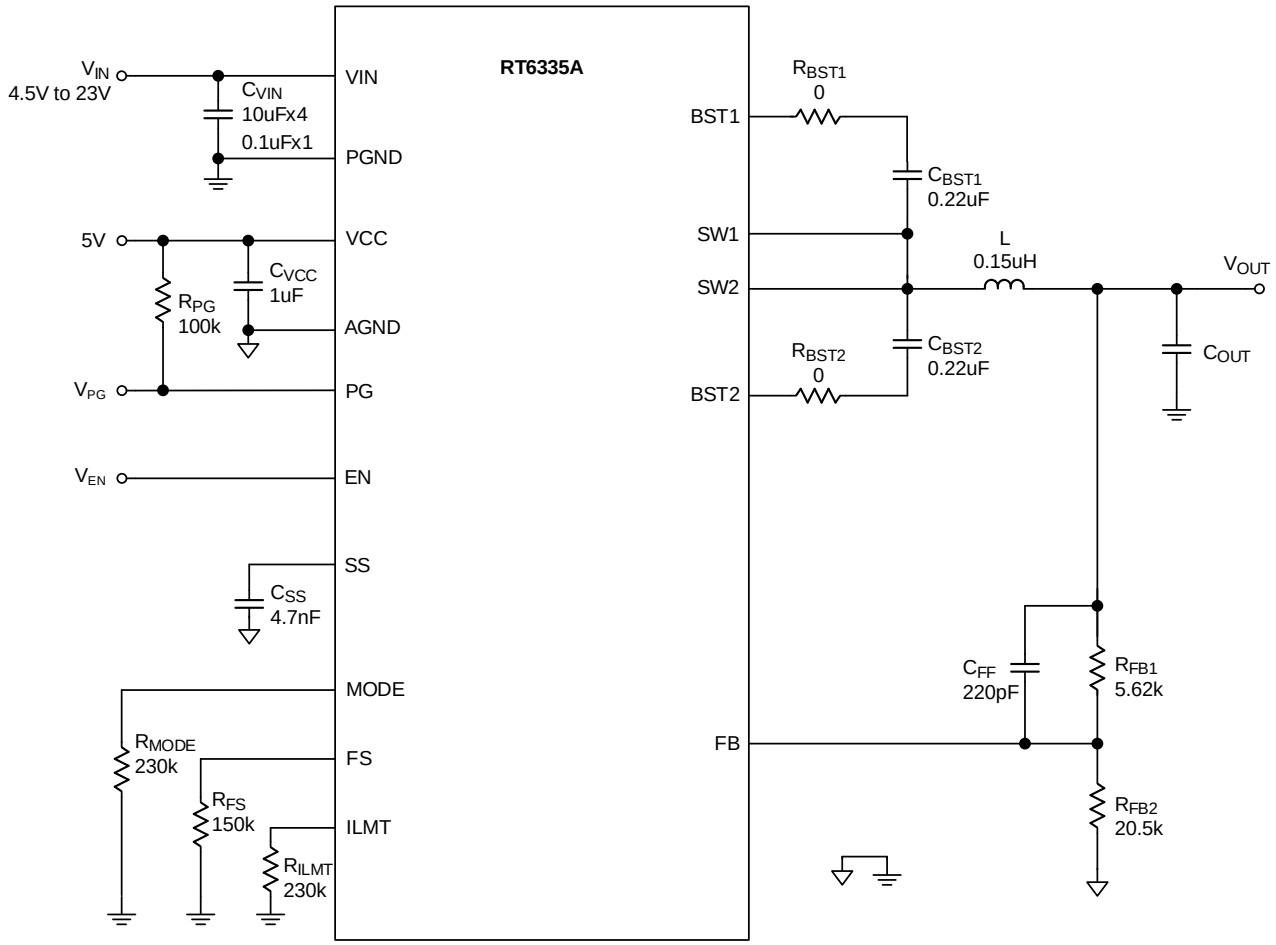
13 Electrical Characteristics

(V_{IN} = 12V, V_{CC} = 5V, R_{MODE} = 0Ω, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J from –40°C to 125°C, unless otherwise noted).

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Current						
VCC Quiescent Current	$I_{VCC\_Q\_NSW}$	V_{EN} = 2V, V_{OUT} = V_{SET} x 105%, R_{MODE} = 0Ω, non-switching, T_J = 25°C	70	100	130	μA
VCC Shutdown Current	I_{VCC_SHDN}	V_{EN} = 0V, R_{MODE} = 0Ω, T_J = 25°C	0	1	2	μA
Supply Input Voltage Protection						
VCC Undervoltage-Lockout Rising Threshold	$V_{CC\_UVLO\_R}$	T_J = 25°C	3.7	4.1	4.5	V
VCC Undervoltage-Lockout Hysteresis	$V_{CC\_UVLO\_HYS}$		--	0.3	--	V
VIN Undervoltage-Lockout Rising Threshold	$V_{IN\_UVLO\_R}$		--	4.1	4.4	V
VIN Undervoltage-Lockout Hysteresis	$V_{IN\_UVLO\_HYS}$		---	0.4	--	V
Enable Control Input						
EN Input Voltage Rising Threshold	V_{EN_R}		1	1.2	1.4	V
EN Threshold Hysteresis	V_{EN_HYS}		--	0.3	--	V
Enable Input Current	I_{EN}	V_{EN} = 2V	--	6	--	μA
MOSFETs						
On-Resistance of High-side MOSFET	R_{DSON_H}	T_J = 25°C	--	12	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}	T_J = 25°C	--	4.8	--	mΩ
SW Discharge Resistor	R_{SW_DISCHG}	V_{EN} = 0V	--	60	--	Ω
PWM Modulator						
Switching Frequency	f_{SW}	V_{OUT} = 0.77V, I_{OUT} = 9.5A, R_{FS} = 0kΩ ±10%	--	650	--	kHz
		V_{OUT} = 0.77V, I_{OUT} = 9.5A, R_{FS} = 90kΩ ±10%	--	850	--	kHz
		V_{OUT} = 0.77V, I_{OUT} = 9.5A, R_{FS} = 150kΩ ±10%	--	950	--	kHz
		V_{OUT} = 0.77V, I_{OUT} = 9.5A, R_{FS} = >230kΩ ±10% or floating	--	1100	--	kHz
Minimum On-Time	t_{ON_MIN}		--	40	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	220	--	ns
Reference						
Reference voltage	V_{REF}	T_J = 25°C	0.594	0.6	0.606	V
Mode Pin Output						
MODE Current Source	I_{MODE}		--	10	--	μA

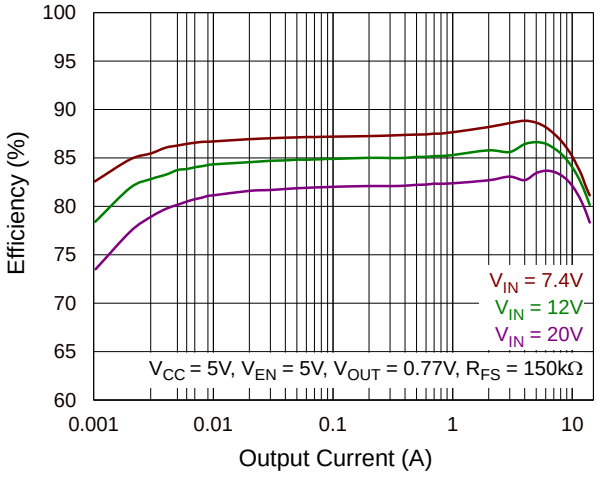
Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft-start Control						
Soft-Start Current	I_{SS}	V_{SS} = 0V	--	1.8	--	μA
Soft-Start Time	t_{SS}	C_{SS} = 4.7nF, From EN high to PG high	--	2.2	--	ms
Power-Good Indicator (PG)						
PG Undervoltage Rising Threshold	$V_{PG\_UV\_R}$	V_{FB} ramps up and PG transits from low to high	--	95	--	%V_{REF}
PG Undervoltage Falling Threshold	$V_{PG\_UV\_F}$	V_{FB} ramps down and PG transits from high to low	--	90	--	%V_{REF}
PG Overvoltage Rising Threshold	$V_{PG\_OV\_R}$	V_{FB} ramps up and PG transits from high to low	--	115	--	%V_{REF}
PG Overvoltage Falling Threshold	$V_{PG\_OV\_F}$	V_{FB} ramps down and PG transits from low to high	--	105	--	%V_{REF}
PG Deglitch Time	$t_{PG\_DEGLITCH}$	PG transition from low to high	--	15	25	μs
EN Low to PG Low Delay Time	$t_{PGTD\_EN\_LOW}$		--	300	-	ns
PG Sink Current Capability	V_{PG_SINK}	Sink 1mA	--	--	0.4	V
Current-Limit Protection Threshold						
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	R_{ILMT} = 0Ω ±10%	14	18.4	--	A
		R_{ILMT} = 90kΩ ±10%	--	23	--	
		R_{ILMT} = 150kΩ ±10%	--	27.5	--	
		R_{ILMT} = >230kΩ ±0% or floating	25	31.9	--	
Output OVP and UVP Threshold						
Output Overvoltage Rising Threshold	V_{OVP_R}		120	125	130	%V_{REF}
Output Overvoltage Deglitch Time	$t_{OVP\_DEGLITCH}$		--	15	--	μs
Output Undervoltage Falling Threshold	V_{UVP_F}		40	45	50	%V_{REF}
Output Undervoltage Deglitch Time	$t_{UVP\_DEGLITCH}$		--	15	--	μs
Thermal Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C

14 Typical Application Circuit

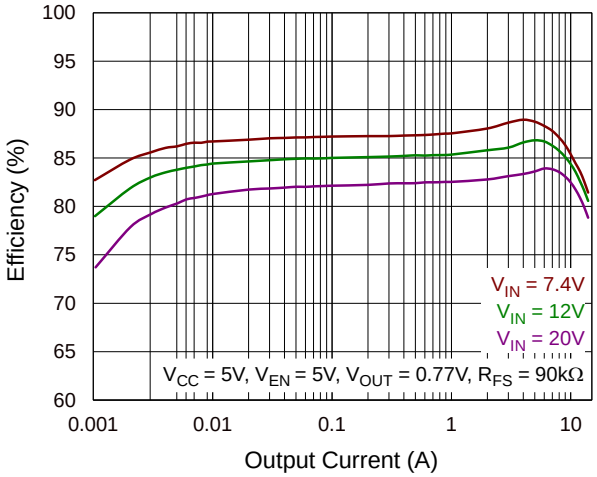


15 Typical Operation Characteristics

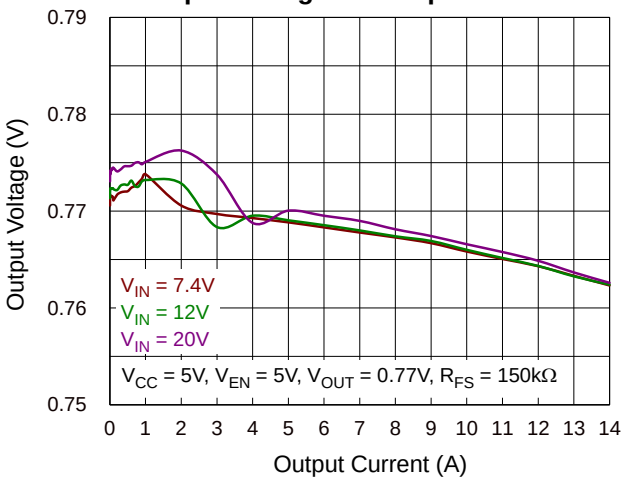
Efficiency vs. Output Current



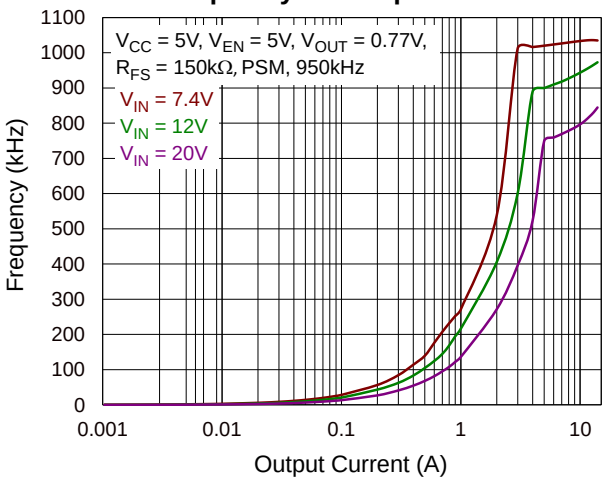
Efficiency vs. Output Current



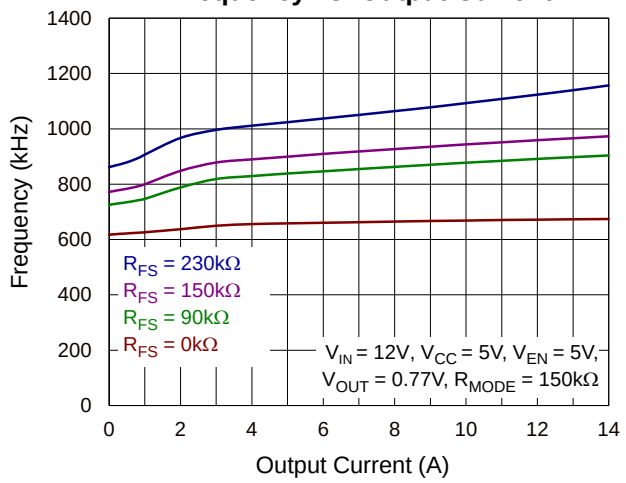
Output Voltage vs. Output Current



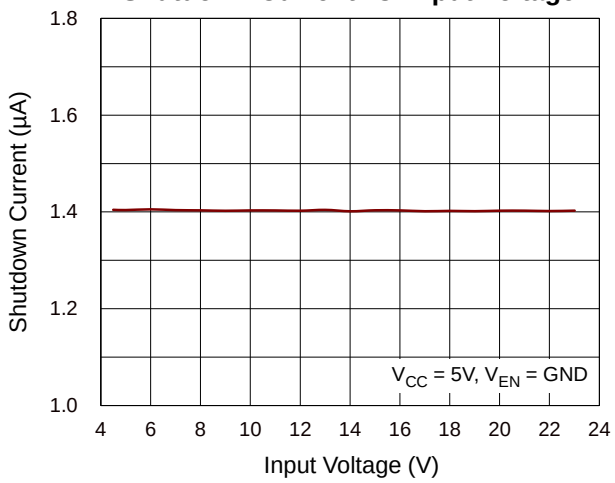
Frequency vs. Output Current



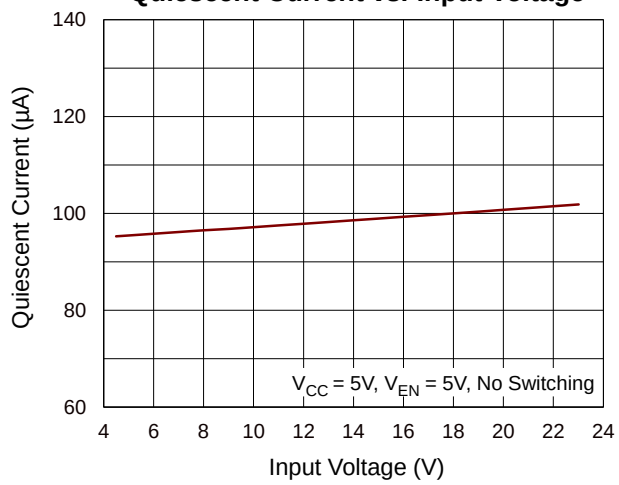
Frequency vs. Output Current



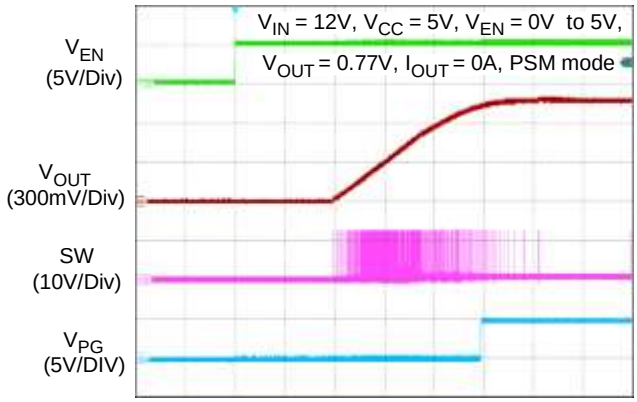
Shutdown Current vs. Input Voltage



Quiescent Current vs. Input Voltage

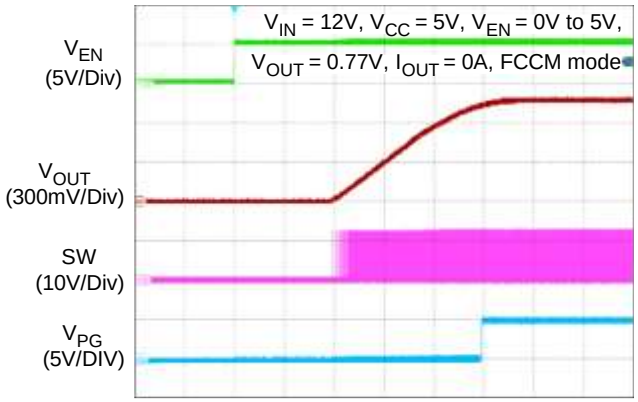


Power On from EN



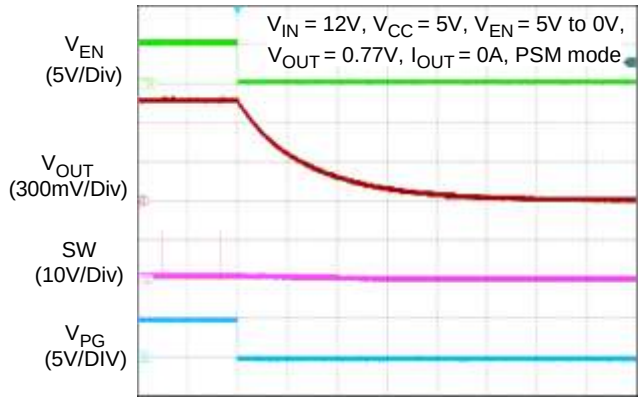
Time (400μs/Div)

Power On from EN



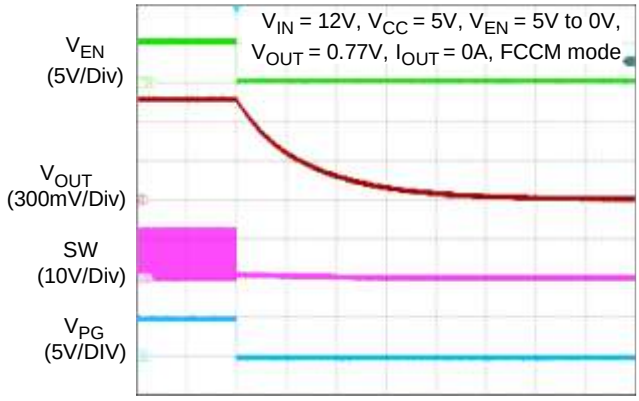
Time (400μs/Div)

Power Off from EN



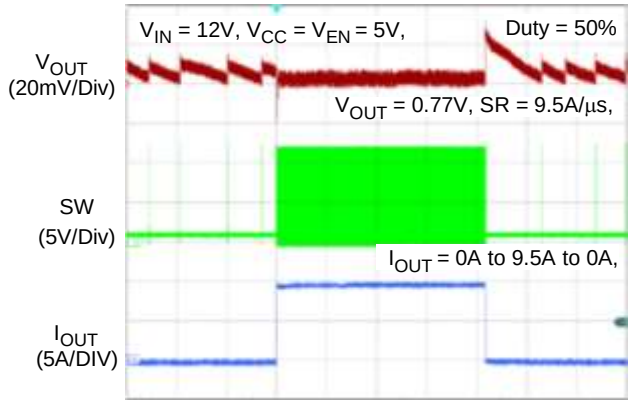
Time (50ms/Div)

Power Off from EN



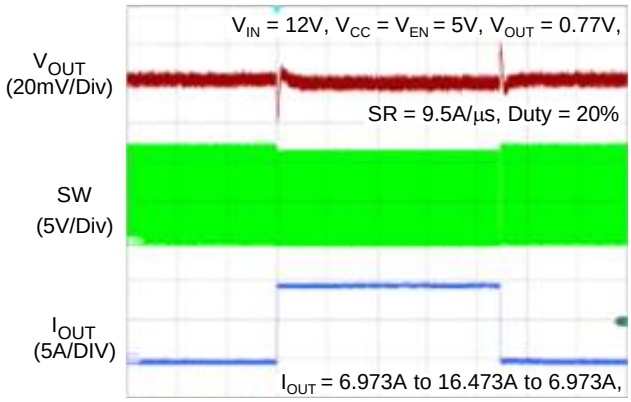
Time (50ms/Div)

Load Transient

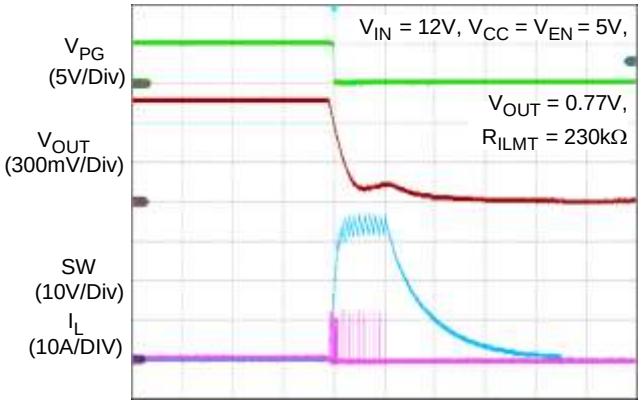


Time (400μs/Div)

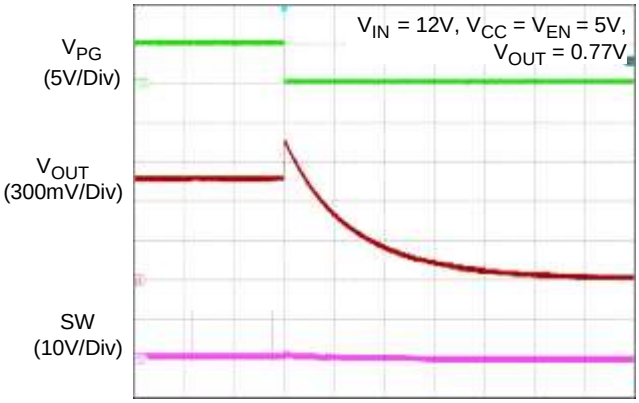
Load Transient



Undervoltage Protection



Overvoltage Protection



16 Operation

The RT6335A is a high-efficiency synchronous buck converter with integrated MOSFETs. The RT6335A utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture providing vary fast transient response. The ultra-fast ACOT® control enables the use of small output capacitance and optimizes the component size without additional compensation network.

During normal operation, the high-side MOSFET turns on with a fixed one-shot on-time timer after the beginning of each clock cycle. The inductor current linearly increases when the high-side MOSFET turns on and the low-side MOSFET turns off. Similarly, the inductor current linearly decreases when the high-side MOSFET turns off and the low-side MOSFET turns on. The voltage ripple on the output has similar shape to the inductor current due to the output capacitor ESR.

The feedback voltage ripple comparing with an internal reference is caught by feedback resistor network. When a fixed minimum off-time timer is timeout and the inductor valley current is below the valley current-limit threshold, the fixed one-shot one-time timer is triggered if the feedback voltage falls below the feedback reference voltage. Therefore, the output voltage is regulated.

16.1 ACOT® Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. The internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Conventional COT control implements the on-time timer proportional to VOUT and inversely proportional to VIN to achieve pseudo-fixed frequency with wide VIN range. A fixed on-time timer of conventional COT control has no compensation for the voltage drop of the MOSFETs and inductor during higher load condition.

In order to compensate the voltage drop of MOSFETs and inductor without influencing the fast transient behavior of the COT topology, a frequency locked loop system with slowly adjusting on-time timer is further added to the ACOT® control.

16.2 Diode Emulation Mode (DEM)

Diode emulation mode is selected by the external resistor connected to the MODE pin. In diode emulation mode, the RT6335A automatically and smoothly reduces switching frequency at light-load conditions. As the output current decreases from heavy load to light load, the inductor current is naturally reduced. Once the valley point of inductor current touches to zero during decreasing output current, the behavior is boundary mode between continuous conduction and discontinuous conduction mode. In order to emulate the behavior of free-wheeling diode, the device only allows partial negative current to flow from drain to source of the low-side MOSFET when inductor free-wheeling current becomes negative.

During decreasing output current, the discharge time of the output capacitor is gradually longer. When the voltage on output capacitor is lower than the reference of regulating voltage, the next one-shot on-time timer is activated. On the contrary, when the output current increases from light load to heavy load and inductor current finally reaches to the continuous conduction, the switching frequency smoothly increases to preset value. The boundary load condition between continuous conduction and discontinuous conduction mode is shown in Figure 1 and is calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times t_{ON}$$

where I_{LOAD} is the output loading current and t_{ON} is the on-time

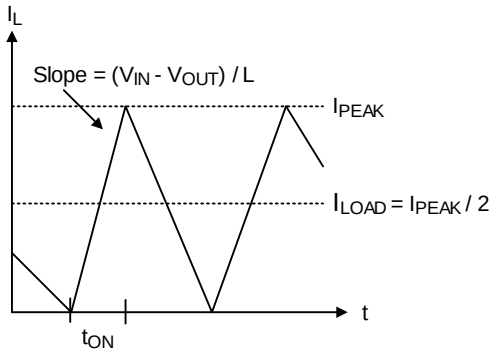


Figure 1. Boundary Condition of CCM/DEM

As mentioned above, diode emulation mode features natural high efficiency in the light-load conditions. In DEM operation (assuming that the coil resistance remains fixed), low inductor value has high efficiency and high output voltage ripple. However, high inductor value features low efficiency and less output voltage ripple. The drawback of using high inductor value includes larger physical size and lower load transient response (especially at low input voltage level).

16.3 EN Sink Current

The RT6335A does not allow uncertain voltage on EN pin, which may cause the logic or behavior error on device. In order to prevent the EN pin from floating, the RT6335A builds the EN sink current for eliminating floating voltage on the EN pin.

16.4 Soft-Start Function

The RT6335A provides an internal soft-start to prevent large input inrush current and output voltage overshoot. If the EN voltage, input voltage, and VCC voltage exceed their rising thresholds, the soft-start function is activated. The V_{FB} starts to track the internal reference voltage ranging from zero to the target.

16.5 Switching Frequency Selection

The RT6335A provides four different switching frequencies for flexible application by the user. The switching frequency is set by the external FS pin with different resistor values before power-on. Table 1 shows the resistor settings corresponding to different switching frequencies.

Table 1. Switching Frequency Selection

State	fsw	Resistor to GND
M1	650kHz	0Ω
M2	850kHz	90kΩ
M3	950kHz	150kΩ
M4	1100kHz	≥ 230kΩ or floating

16.6 Mode Pin Selection

The RT6335A offers two different operating modes for users to choose from: DEM mode and FCCM mode. The operating mode is determined by the external resistor connected to the MODE pin before the RT6335A is powered on. Table 2 shows the resistor settings corresponding to the different modes.

Table 2. Mode Pin Selection

State	Operating Mode	Resistor to GND
M1	DEM	0Ω
		≥ 230kΩ or floating
M2	FCCM	90kΩ
		150kΩ

16.7 Valley Current Limit

The RT6335A features a cycle-by-cycle valley current limit for avoiding the large output current and overheat. The device cycle-by-cycle compares the valley current of the inductor with the valley current-limit threshold. The output current is limited to the sum of the valley current and a half of the ripple current when valley current of the inductor reaches valley current-limit threshold.

After the device completes the minimum off-time and keeps ON state of the low-side MOSFET, the inductor valley current level is monitored by measuring the low-side MOSFET voltage between the SW pin and PGND pin during the ON state of low-side MOSFET. During the ON state of low-side MOSFET, the measured low-side MOSFET voltage is proportional to the low-side MOSFET current. In order to improve the accuracy of measured current, the temperature compensation circuit is built internally.

In order to prevent the device from overcurrent, if the measured low-side MOSFET current is higher than the valley current-limit threshold, the device remains ON state of the low-side MOSFET and the one-shot on-time timer is inhibited until its current linearly decreases lower than the valley current-limit threshold. Once the low-side MOSFET current is below valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle valley current limit works in every switching cycle.

16.7.1 Valley Current-Limit Setting

The RT6335A provides valley current-limit setting pin to adjust current-limit level. When both "VIN and VCC rises to its UVLO rising threshold" and "EN is activated" are satisfied and kept for 600μs, the RT6335A determines and locks the current-limit level according to the voltage on the ILMT pin. Beside the previous described timing behavior, any change of valley current-limit status is invalid. Refer to 錯誤! 找不到參照來源。 for the valley current limit setting level selection:

Table 3. ILMT Selection

State	Current Limit	Resistor to GND
M1	18.4A	0Ω
M2	23A	90kΩ
M3	27.5A	150kΩ
M4	31.9A	≥ 230kΩ or floating

16.8 Output Undervoltage Protection (UVP)

The output undervoltage protection of the RT6335A is latched mode. If the inductor current is higher than the current-limit threshold (valley current-limit threshold) during heavy-load condition, the output voltage tends to drop

because the load demand exceeds that the converter can support.

When the load demand is larger than the current ability of the converter, the V_{FB} starts to drop. Once the V_{FB} drops below typical 45% of the reference voltage and the time length of this state is larger than the time width 15μs (typical), the latched mode UVP is triggered. The behavior for latched mode UVP is as follows:

The RT6335A provides output undervoltage protection (UVP) with latched mode. Once UVP is triggered, the IC stops PWM switching and enter latched mode. If UVP event is released, users should re-toggle the EN pin or power recycle VIN or VCC supply to re-power on the device.

16.9 Output Overvoltage Protection (OVP)

The output overvoltage protection of the RT6335A is latched mode. If the V_{FB} rises above typical 125% of the reference voltage and the time length of this state is larger than the time width 15μs (typical), the latched mode OVP is triggered. The behavior of latched mode OVP is as follows:

The RT6335A provides output overvoltage protection (OVP) with latched mode. Once OVP is triggered, the IC stops PWM switching and enter latched mode. If OVP event is released, users should re-toggle the EN pin or power recycle VIN or VCC supply to re-power on the device.

16.10 Over-Temperature Protection (OTP)

The RT6335A features non-latched over-temperature protection (OTP) to prevent overheating from excessive power dissipation. If the junction temperature exceeds 160°C, the OTP is triggered, stopping PWM switching. When the temperature drops below 145°C, the device re-enables the soft-start function to establish the output voltage.

16.11 Input and VCC Undervoltage-Lockout (UVLO)

The RT6335A provides an Undervoltage-Lockout (UVLO) function that monitors the input voltage and VCC voltage. In order to protect the device from operating at insufficient input voltage and VCC voltage, the UVLO function inhibits switching when the input voltage drops below the UVLO falling threshold. The IC resumes switching when the input voltage and VCC voltage exceed the UVLO rising threshold.

16.12 Internal Output Voltage Discharge

The RT6335A has an output voltage discharge function by using an internal MOSFET 60Ω (typical), which is connected from the SW pin to the PGND pin. The output voltage discharge function is enabled if any of the following events is triggered:

- VCC undervoltage-lockout (VCC UVLO)
- Output undervoltage-/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN pin is pulled low

16.13 Power-Good Indicator (PG)

The PG pin is an open-drain output. An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor ranges from 10kΩ to 100kΩ. Do not pull the PG voltage higher than 6V. After V_{FB} reaches 95% of reference, PG is pulled high after a delay time (≤ 10μs). When V_{FB} drops below 90% of reference, PG is pulled low.

The PG pin is pulled low when any of the following specified events is triggered:

- Input or VCC undervoltage-lockout (VIN/VCC UVLO)
- Output undervoltage/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN pin is pulled low
- Soft-start function is not completed
- The FB pin voltage is lower than the PG falling threshold (PG rising threshold minus PG hysteresis voltage) of the target voltage

17 Application Information

(Note 7)

The Typical Application Circuit section introduces the circuit configuration of the RT6335A in VNNAON applications. Within this section, critical external components are introduced, including the inductor (L), the input capacitor (C_{IN}), the output capacitor (C_{OUT}), the internal regulator capacitor (C_{VCC}), and the bootstrap capacitor (C_{BOOT}).

17.1 Inductor Selection

Selecting an inductor involves trade-offs among size, cost, efficiency, and transient response requirements. There are three primary inductor parameters to be specified for compatibility with the device: the inductance value (L), the inductor's saturation current (I_{SAT}), and its DC resistance (DCR).

Achieving a balance between size and loss often involves targeting a 30% peak-to-peak ripple current (ΔI_L) relative to the IC's rated current. The inductance value is determined by the switching frequency, input voltage, output voltage, and the chosen inductor ripple current, as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values lead to lower output ripple voltage and increased efficiency but may slightly impair the transient response. Conversely, lower inductance values permit a smaller case size, yet result in a larger ripple current, escalating the AC losses within the inductor. To optimize efficiency, select a low-loss inductor with the minimum possible DC resistance that can be accommodated within the given dimensions. The inductance not only influences the ripple current but also defines the load current at the boundary between DEM and CCM.

In VNNAON applications, the RT6335A may experience events such as power-on inrush current (caused by a capacitive or heavy load) and output overloading. The RT6335A is equipped with valley current limit protections to safeguard the device from damage. Furthermore, for the current-limit protection to be effective, the inductor's saturation current rating must exceed the valley current limit specification of the RT6335A.

17.2 Input Capacitor Selection

Input capacitance (C_{IN}) is required to filter the pulsating current from the drain of the high-side MOSFET. A large ripple voltage on the VIN pin must be minimized by C_{IN}. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times R_{ESR}$$

where R_{ESR} is the equivalent series resistance of C_{IN} and

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, which have a very low equivalent series resistance (ESR), the ripple caused by ESR can be ignored. The minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D \times (1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{IN_MAX} = 200mV for typical applications (V_{IN} > 7V)

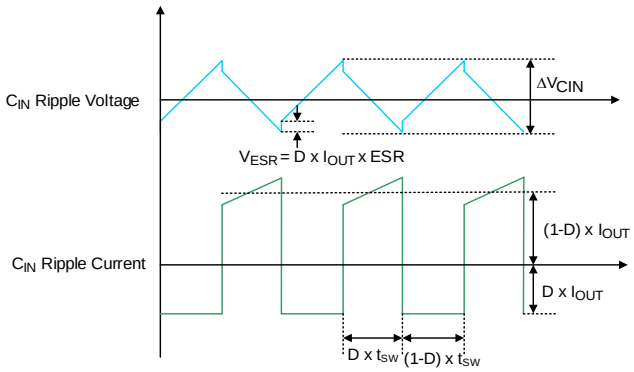


Figure 2. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor requires a very low ESR and must be rated to withstand the worst-case RMS input current, as follows:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common practice to use the worst-case $I_{RMS} \approx I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design purposes. Note that capacitor manufacturers often base ripple current ratings on a lifespan of only 2000 hours. As a result, capacitors typically experience greater de-rating in actual applications. Selecting capacitors with a higher temperature rating is required to minimize this de-rating.

Parallel connection of several capacitors may be employed to satisfy size, height, and thermal design requirements. For applications with low input voltage, sufficient bulk input capacitance is necessary to minimize transient effects during load changes on the output.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, caution is required when using these capacitors at the input. A ceramic input capacitor, in combination with trace or cable inductance, forms a high-quality factor (under-damped) tank circuit. If the RT6335A circuit is plugged into an active supply, the input voltage may experience ringing up to twice its nominal value, potentially exceeding the device's rating. This issue can be easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor that has a higher ESR to dampen the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low-inductance connection to the IC's PGND. Along with a larger bulk capacitor, a small ceramic capacitor of 0.1µF should also be situated close to the VIN pin. The capacitor should be of size 0402 or 0603.

17.3 Output Capacitor Selection

The selection of C_{OUT} should satisfy the requirements for the voltage ripple, transient loads, and ensure that the control loop remains stable. Loop stability can be assessed by observing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components: ESR ripple (ΔV_{P-P_ESR}) and capacitive ripple (ΔV_{P-P_C}), which are expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where ΔI_L represents the peak-to-peak inductor ripple current, and R_{ESR} is the equivalent series resistance of C_{OUT}.

The output ripple is highest at the maximum input voltage because ΔI_L increases with the input voltage. To meet the ESR and RMS current handling requirements, it may be necessary to use multiple capacitors in parallel.

Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration when choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which is calculated from the on-time and the minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage is determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

When the load is removed, the amount of overshoot due to the stored inductor energy is calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors, with their very low equivalent series resistance (ESR), offer superior ripple performance. However, it is important to take into account the voltage coefficient of ceramic capacitors when selecting their value and case size. Notably, most ceramic capacitors lose 50% or more of their rated capacitance when operated near their rated voltage.

17.4 VCC Capacitor Selection

The VCC pin requires a good and clean power supply to maintain the stability of the internal reference voltage and to provide the large instantaneous current needed for the MOSFET gate driver. Place a low-ESR MLCC capacitor (C = 1μF/0603) as close as possible to the VCC and AGND pins.

17.5 External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF/0603 low-ESR ceramic capacitor and a 0Ω resistor (or use a direct wire connection) between the BOOT pin and the SW pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side MOSFET. The internal gate driver is optimized to turn on the high-side MOSFET quickly enough to minimize power loss and maximize efficiency, while also turning on slowly enough to mitigate EMI. Most EMI is generated because V_{SW} rises rapidly when the high-side MOSFET is turned on quickly. In some cases, slightly increasing the resistance of R_{BOOT} can directly reduce EMI and the voltage spike at the SW pin; however, it can also lead to increased switching loss for the high-side MOSFET and higher die or case temperatures.

17.6 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated

using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a VQFN-19TL 3x4 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, 26.91°C/W is measured in the natural convection at T_A = 25°C on a four-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C − 25°C) / (26.91°C/W) = 3.72W for a VQFN-19TL 3x4 (FC) package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

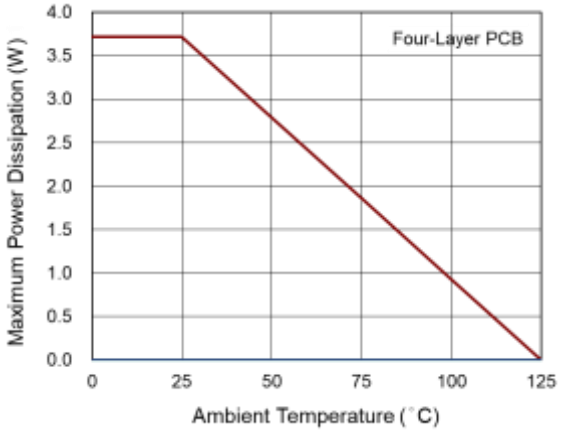


Figure 3. Derating Curve of Maximum Power Dissipation

17.7 Layout Considerations

The design of printed circuit board (PCB) layouts for switch-mode power supply ICs is both critical and important. An improper PCB layout can cause numerous problems for the power supply, including poor output voltage regulation, switching jitter, bad thermal performance, excessive noise radiation, and reduced component reliability. To avoid those issues, designers have to understand current trace and signal flow in the switching power supply. The following suggestions are design considerations for PCB layouts in switching power supplies:

- Place the input capacitor close to the VIN pin to suppress phase ringing and extra power losses, thereby enhancing device reliability by reducing the influence of parasitic inductance.
- Minimize thermal stress and power consumption by ensuring the current paths of V_{IN} and V_{OUT} are as short and wide as possible, thereby decreasing the trace impedance.
- Given the SW node voltage swings from V_{IN} to 0V with rapid rising and falling times, the switching power supply is prone to significant EMI issues. To eliminate EMI problems, the inductor must be put as close as possible to the IC to narrow the SW node area. Besides, the SW node should be arranged in the same plate to reduce coupling noise path caused by parasitic capacitance.
- For system stability and coupling noise elimination, the sensitive components and signals, such as control signals and feedback loops, should be kept away from theSW node.

- To enhance noise immunity on the VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to the IC.
- The feedback signal path from VOUT to the IC should be wide and kept away from high switching paths.
- The trace width and numbers of vias should be designed based on the application current. Make sure the switching power supply has great thermal performance and good efficiency.

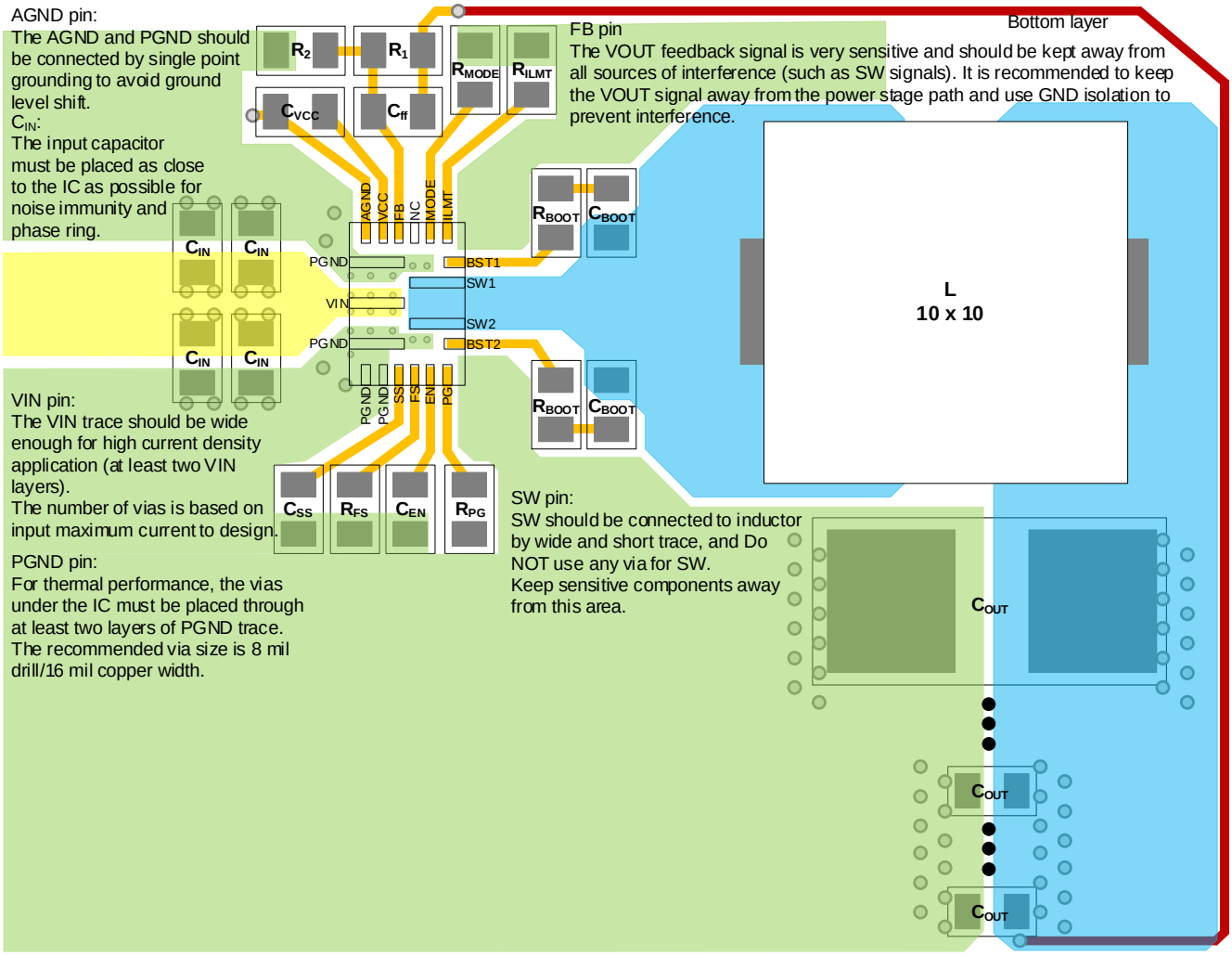
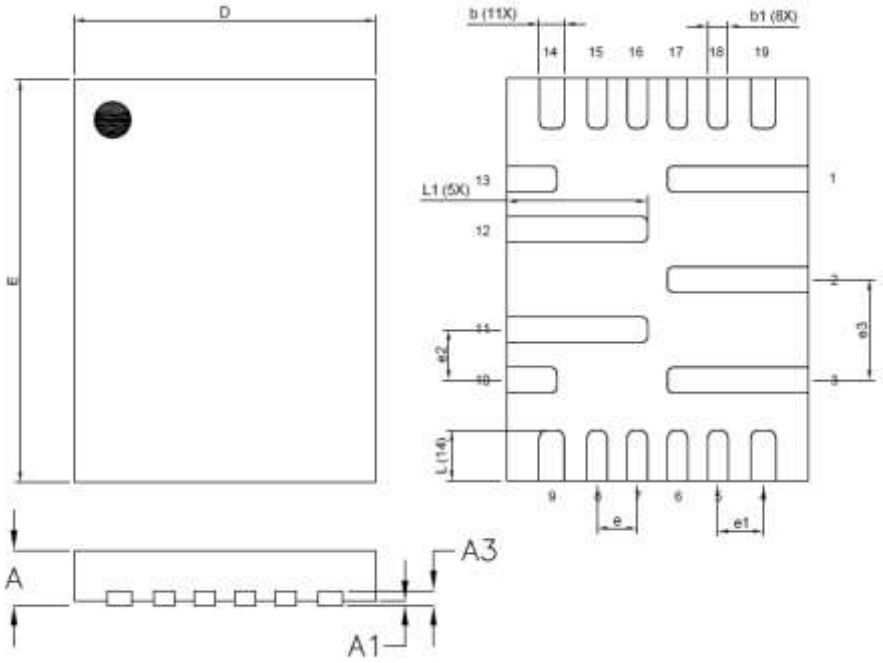


Figure 4. Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

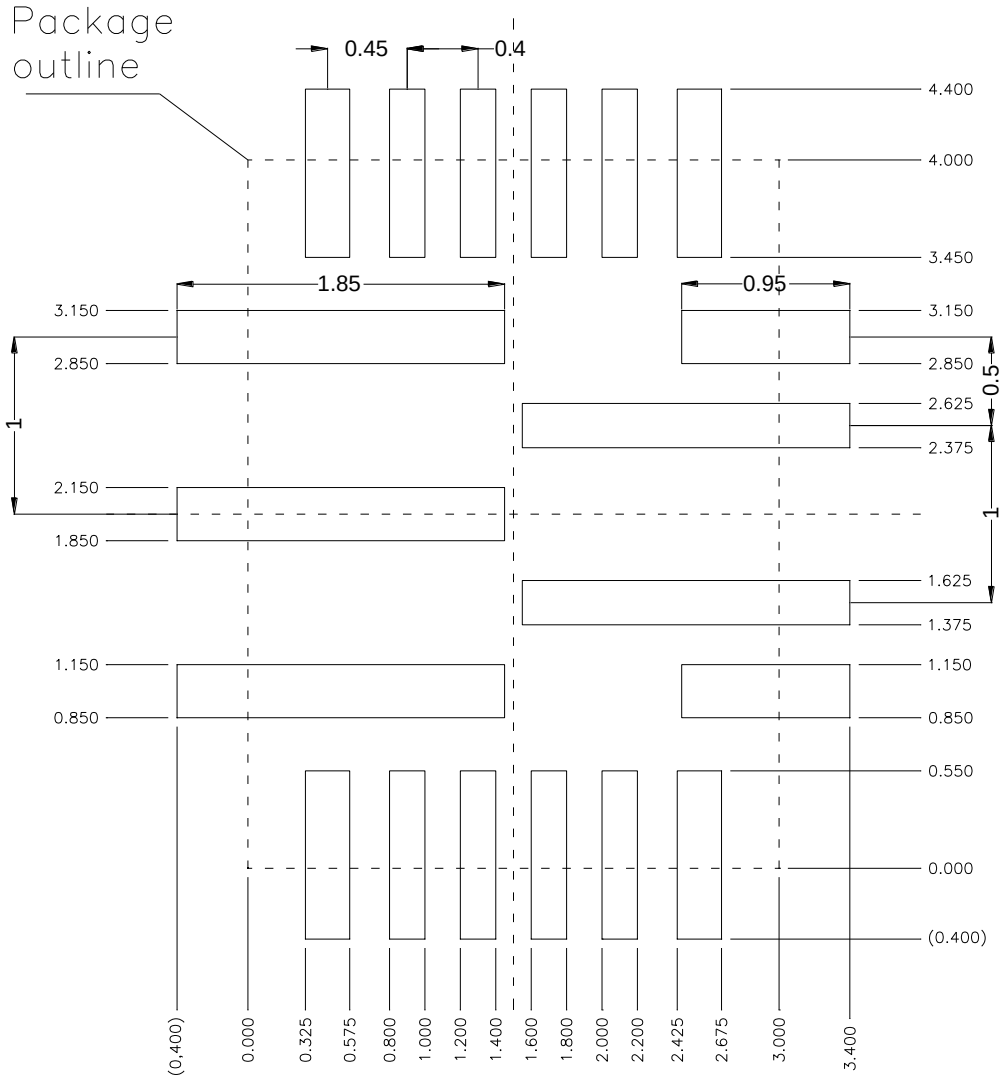
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
b1	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
E	3.950	4.050	0.156	0.159
e	0.400		0.016	
e1	0.450		0.018	
e2	0.500		0.020	
e3	1.000		0.039	
L	0.450	0.550	0.018	0.022
L1	1.350	1.450	0.053	0.057

V-Type 19TL QFN 3x4 Package (FC)

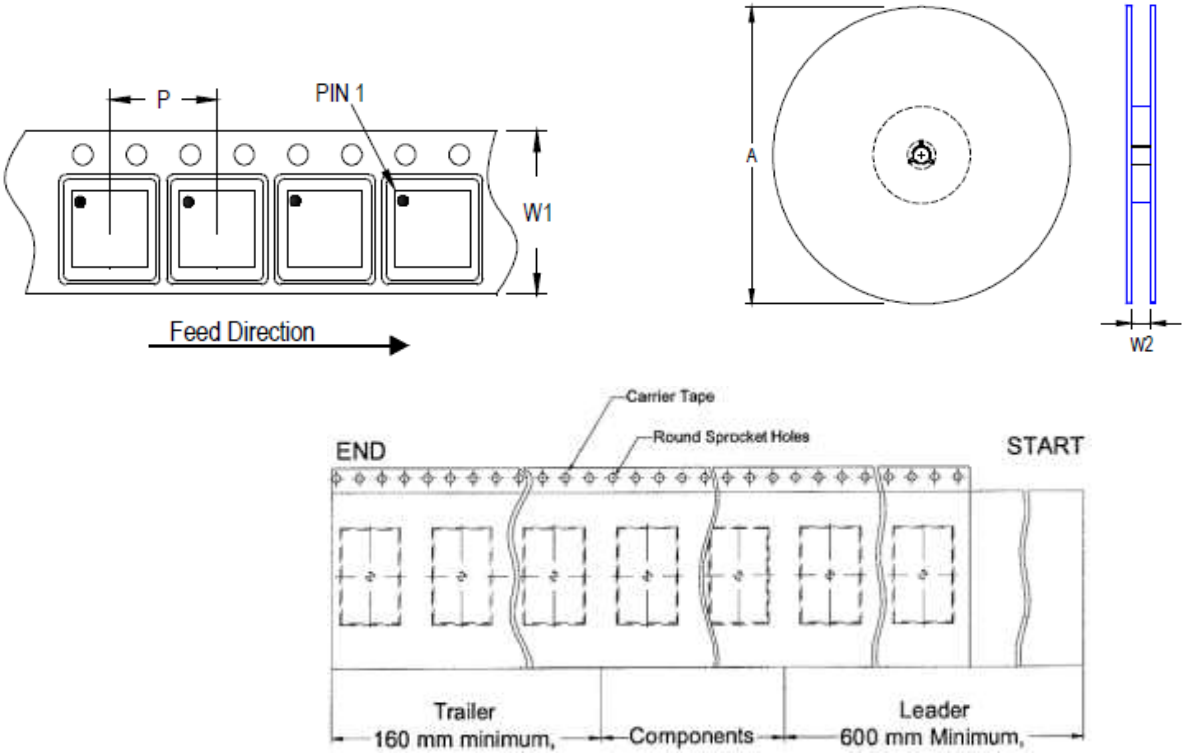
19 Footprint Information



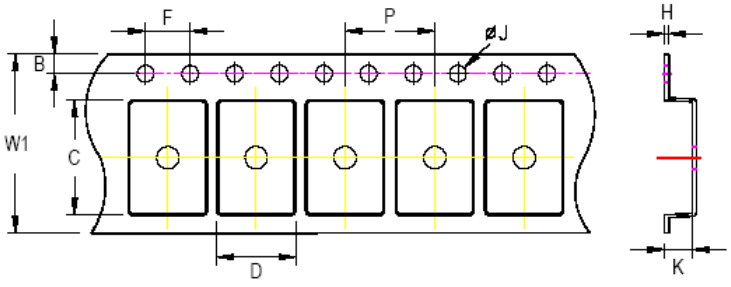
Package	Number of Pins	Tolerance
V/W/U/XQFN3x4-19T(FC)	19	±0.05

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2025/7/10	Final	*Features on page 1* - Modified Valley Current Limit