RICHTEK®

RT6360

60V, 0.5A, Asynchronous Buck Converter with Low Quiescent Current

1 General Description

The RT6360 is a 0.5A, high-efficiency, peak current mode control asynchronous buck converter. The device operates with input voltages from 4V to 60V. The device can program the output voltage between 0.8V to VIN. The low quiescent current design with the integrated low $R_{DS(ON)}$ of high-side MOSFET achieves high efficiency over the wide load range. The peak current mode control with simple external compensation allows the use of small inductors and results in fast transient response and good loop stability.

The wide switching frequency of 100kHz to 2500kHz allows for efficiency and size optimization when selecting the output filter components. The ultra-low minimum on-time enables constant-frequency operation even at very high step-down ratios. For switching noise-sensitive applications, it can be externally synchronized from 300kHz to 2200kHz.

The RT6360 provides comprehensive protection functions such as input undervoltage-lockout, output undervoltage protection, output overvoltage protection, overcurrent protection (OCP), and over-temperature protection. Cycle-by-cycle current limit provides protection against shorted outputs, and the soft-start function eliminates input current surges during start-up. The RT6360 is available in WDFN-10SL 3x3 and SOP-8 (Exposed pad) packages. The recommended junction temperature range is –40°C to 150°C

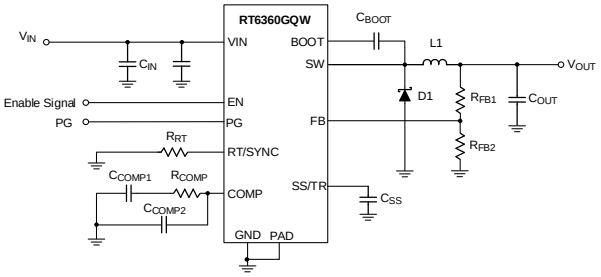
2 Features

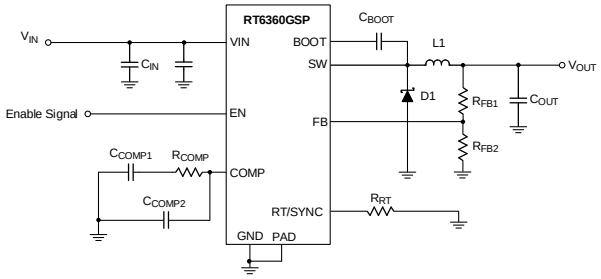
- **Wide Input Voltage Range**
  - **4.5V to 60V**
  - **4V to 60V (After Soft-Start Is Finished)**
- **Wide Output Voltage Range: 0.8V to VIN**
- **0.8V ±1.5% Reference Accuracy**
- **Peak Current Mode Control**
- **Integrated 170mΩ High-Side MOSFET**
- **Low Quiescent Current: 90μA**
- **Low Shutdown Current: 1.3μA**
- **Adjustable Switching Frequency: 100kHz to 2.5MHz**
- **Synchronizable Switching: 300kHz to 2.2MHz**
- **Power Saving Mode (PSM) at Light Load**
- **Low Dropout at Light Loads with Integrated Boot Recharge MOSFET**
- **Externally Adjustable Soft-Start by Part Number Option**
- **Power-Good Indication by Part Number Option**
- **Enable Control**
- **Adjustable UVLO Voltage and Hysteresis**
- **Built-In Protections: UVLO, UVP, OVP, OCP, OTP**

3 Applications

- 12V, 24V, and 48V Power Systems
- GPS, Entertainment Devices

4 Simplified Application Circuit





5 Ordering Information

RT6360□□□

Pin 1 Orientation
Empty: Quadrant 1
(2): Quadrant 2, Follow EIA-481
(WDFN-10SL 3x3 only)

Package Type(1)
SP: SOP-8 (Exposed Pad)
(Exposed Pad-Option 2)
QW: WDFN-10SL 3x3 (W-Type)

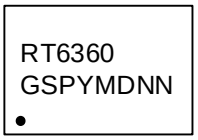
Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

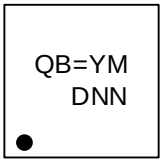
6 Marking Information

RT6360GSP



RT6360GSP: Product Code
YMDNN: Date Code

RT6360GQW



QB= : Product Code
YMDNN : Date Code

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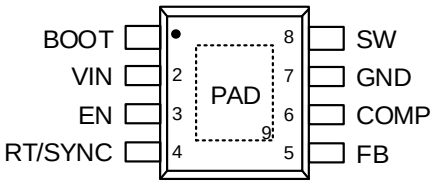
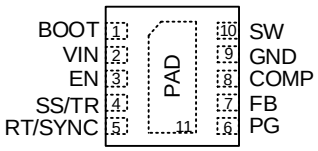
7 Pin Configuration

(TOP VIEW)



SOP-8 (Exposed pad)



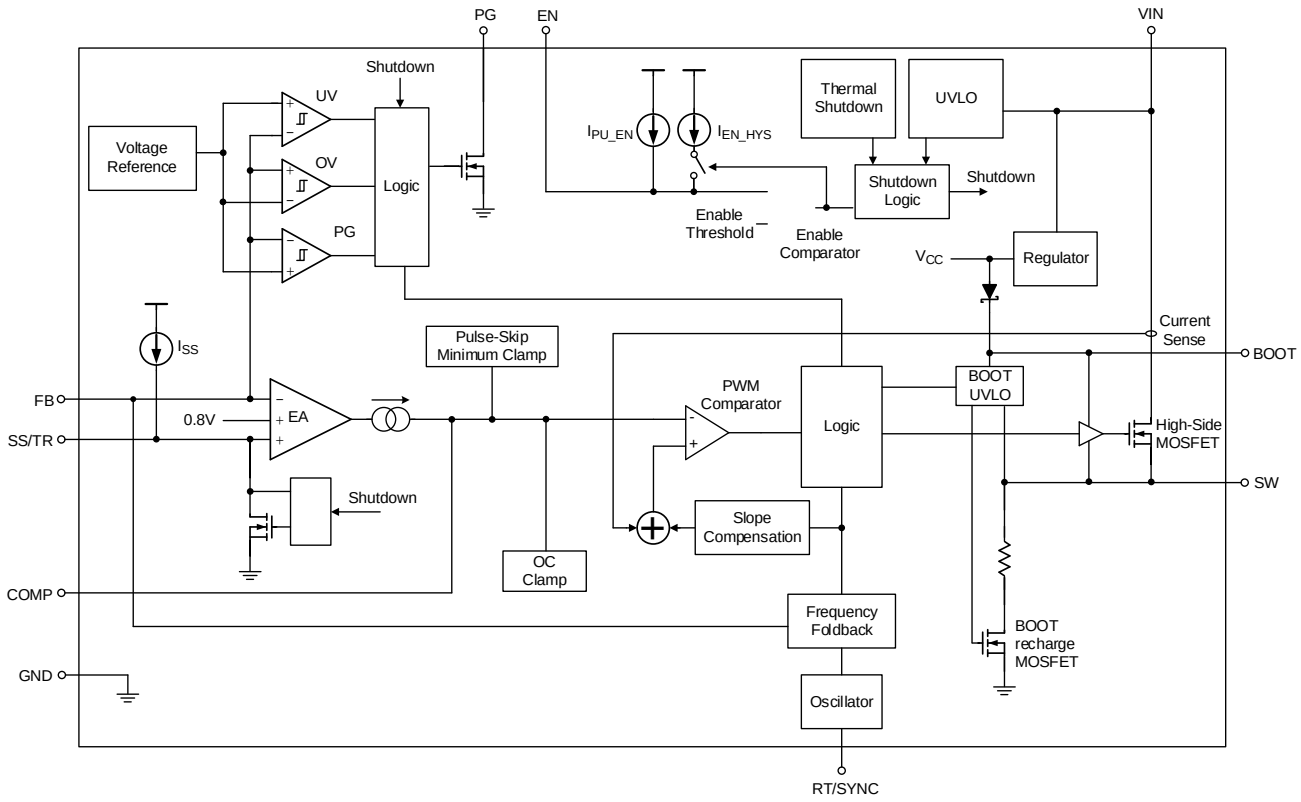
WDFN-10SL 3x3

8 Functional Pin Description

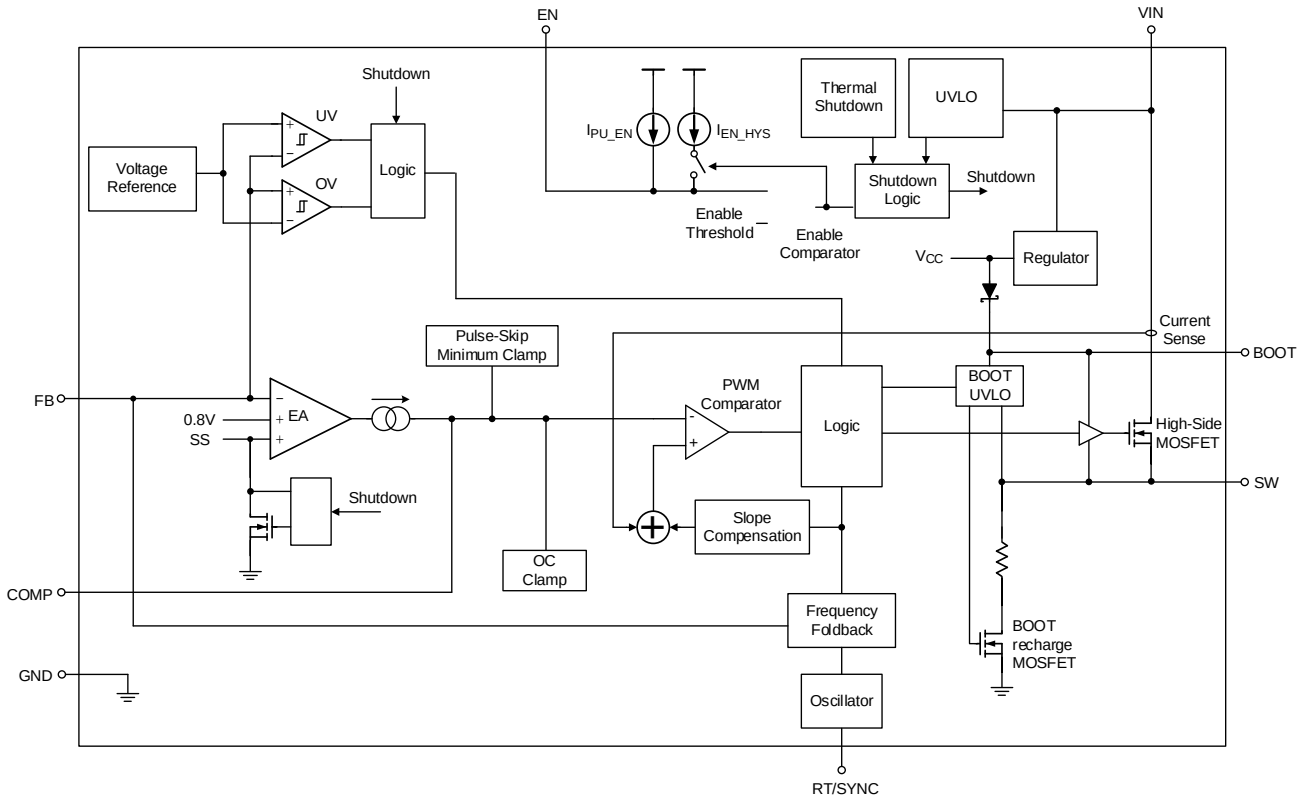
Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10SL 3x3		
1	1	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the SW pin.
2	2	VIN	Power input. The input voltage range is from 4V to 42V. Connect a suitable input capacitor between this pin and GND, usually two 2.2μF or larger ceramic capacitors with one typical capacitance 4.7μF.
3	3	EN	Enable control pin with internal pull-up current source. Float or provide a logic-high (≥ 1.25V) to enable the converter; a logic-low forces the device into shutdown mode.
--	4	SS/TR	Soft-start and tracking control input. Connect a capacitor from SS to GND to set the soft-start period. ”Do Not” leave this pin floating to avoid inrush current during power-up. It can also be used to track and sequence because the SS/TR pin voltage can override the internal reference voltage.
4	5	RT/SYNC	Frequency setting and external synchronous signal input. Connect a resistor from this pin to GND to set the switching frequency. Tie to a clock source for synchronization to an external frequency.
--	6	PG	Open-drain power-good indication output. Once started up, PG will be pulled low to GND if any internal protection is triggered.
5	7	FB	Output voltage sense. Sense the output voltage at the FB pin through a resistive divider. The feedback reference voltage is 0.8V typically.
6	8	COMP	Compensation node. Connect external compensation elements to this pin to stabilize the control loop.
7	9	GND	Ground. Provide the ground return path for the control circuitry.
8	10	SW	Switch node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
9 (Exposed Pad)	11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PCB copper area for maximum power dissipation.

9 Functional Block Diagram

9.1 WDFN-10SL 3x3



9.2 SOP-8 (Exposed Pad)



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- –0.3V to 65V
- Enable Voltage, EN ---------- –0.3V to 65V
- Switch Voltage, SW ---------- –0.6V to 65V
- SW (t ≤ 100ns) ---------- –5V to 70V
- SW (t ≤ 5ns) ---------- –7V to 70V
- Power-Good Voltage, PG ---------- –0.3V to 50V
- BOOT to SW (BOOT – SW) ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 4V to 60V
- Output Voltage ---------- 0.8V to V_{IN}
- Junction Temperature Range ---------- –40°C to 150°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WDFN-10SL 3x3	SOP-8 (Exposed Pad)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	34.1	31.8	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	77.6	74.1	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5.9	4.9	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	38.8	31.4	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.3	14.7	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, outer layers with 2 oz. Cu and inner layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = 25°C, unless otherwise specified.)

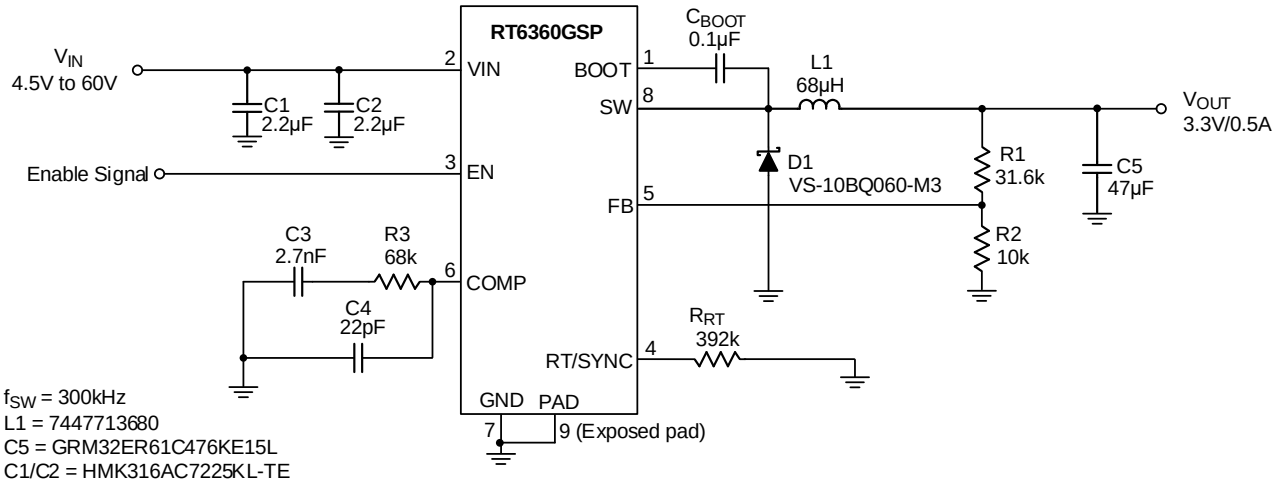
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}	After soft-start is finished	4	--	60	V
Input Undervoltage-Lockout Rising and Falling Threshold	V_{UVLO_R}	V_{IN} rising	4.1	4.3	4.5	V
	V_{UVLO_F}	V_{IN} falling	3.8	3.9	4	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	1.3	4	µA
Supply Current (Non-Switching)	I_{Q_NSW}	V_{EN} = 2V, V_{FB} = 0.83V, not switching	--	90	130	µA
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}		1.15	1.25	1.36	V
Enable to COMP Active		V_{IN} = 12V, T_A = 25°C	--	450	--	µs
EN Pull-Up Current	I_{PU_EN}	V_{TH_EN} + 50mV	--	3.8	--	µA
		V_{TH_EN} – 50mV	--	0.9	--	
Hysteresis Current	I_{EN_HYS}		--	2.9	--	µA
Reference Voltage						
Reference Voltage	V_{REF}		0.788	0.8	0.812	V
MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}	V_{IN} = 12V, V_{BOOT} – V_{SW} = 5V	--	170	300	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
Input Current			--	50	--	nA
Error Amplifier Trans-Conductance	gm	Normal operation $-2\mu A < I_{COMP} < 2\mu A$ V_{COMP} = 1V	--	97	--	μA/V
		During SS, $-2\mu A < I_{COMP} < 2\mu A$ V_{COMP} = 1V, V_{FB} = 0.4V	--	26	--	
Error Amplifier DC Gain		V_{FB} = 0.8V	--	10000	--	V/V
Error Amplifier Bandwidth			--	2700	--	kHz
Source/Sink Current		V_{COMP} = 1V, 100mV overdrive	--	±7	--	μA
COMP to Current Sense Trans-Conductance	gm_cs		--	2	--	A/V
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	f_{SW} = 500kHz, V_{OUT} = 5V	0.72	0.9	1.08	A
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	I_{OUT} = 1A	--	100	130	ns
Timing Resistor and External Clock						
Switching Frequency 1	f_{SW1}	$R_{RT/SYNC}$ = 1.2MΩ	85	100	115	kHz
Switching Frequency 2	f_{SW2}	$R_{RT/SYNC}$ = 200kΩ	520	580	640	kHz
Switching Frequency 3	f_{SW3}	$R_{RT/SYNC}$ = 44.2kΩ	2250	2500	2750	kHz
SYNC Frequency Range		External clock	0.3	--	2.2	MHz
Minimum Sync Pulse Width			--	40	--	ns
SYNC Threshold Voltage	V_{IH_SYNC}		--	1.9	2.2	V
	V_{IL_SYNC}		0.5	0.7	--	
RT/SYNC Falling Edge to SW Rising Edge Delay			--	60	--	ns
Soft-Start and Tracking						
Internal Charge Current	I_{SS}	$V_{SS/TR}$ = 0.4V, RT6360GQW	--	2	--	μA
SS/TR to FB Offset		$V_{SS/TR}$ = 0.4V, RT6360GQW	--	75	--	mV
SS/TR-to-Reference Crossover		98% nominal, RT6360GQW	--	0.9	--	V
SS/TR Discharge Voltage		V_{FB} = 0V, RT6360GQW	--	54	--	mV
Internal Soft-Start Time						
Soft-Start Period		10% to 90%, RT6360GSP	1.4	2	2.6	ms

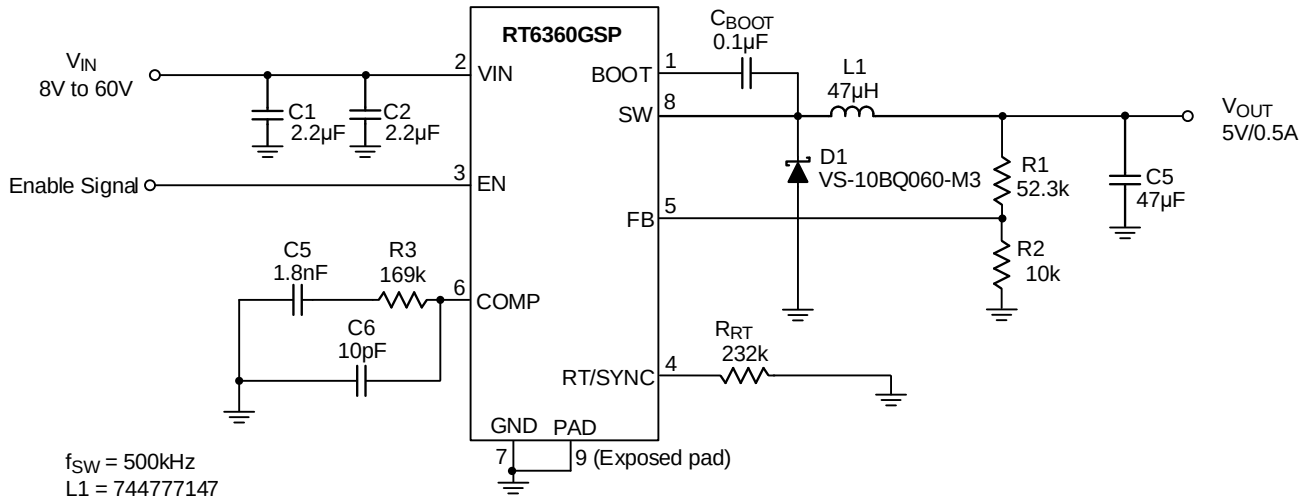
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good Function						
Power-Good Voltage Threshold	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF}, PG from low to high, RT6360GQW	90	94	98	%
	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF}, PG from high to low, RT6360GQW	105	109	113	
	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF}, PG from high to low, RT6360GQW	88	92	96	
	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF}, PG from low to high, RT6360GQW	102	106	110	
Power-Good Voltage Hysteresis		V_{FB} falling, RT6360GQW	--	2	--	%
Power-Good Leakage Current	I_{LK_PG}	V_{PG} = 5.5V, T_A = 25°C, RT6360GQW	--	10	500	nA
On-Resistance		I_{PG} = 3mA, V_{FB} < 0.79V, RT6360GQW	--	6	15	Ω
Minimum VIN for Defined Output		V_{PGOOOD} < 0.5V, I_{PG} = 100μA, RT6360GQW	--	0.95	1.5	V
Spread Spectrum						
Spread-Spectrum Range SSP	SSP		--	+6	--	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	175	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C
Output Undervoltage Protection						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	--	0.4	--	V

15 Typical Application Circuit

15.1 3.3V, 0.5A, 300kHz, Buck Converter

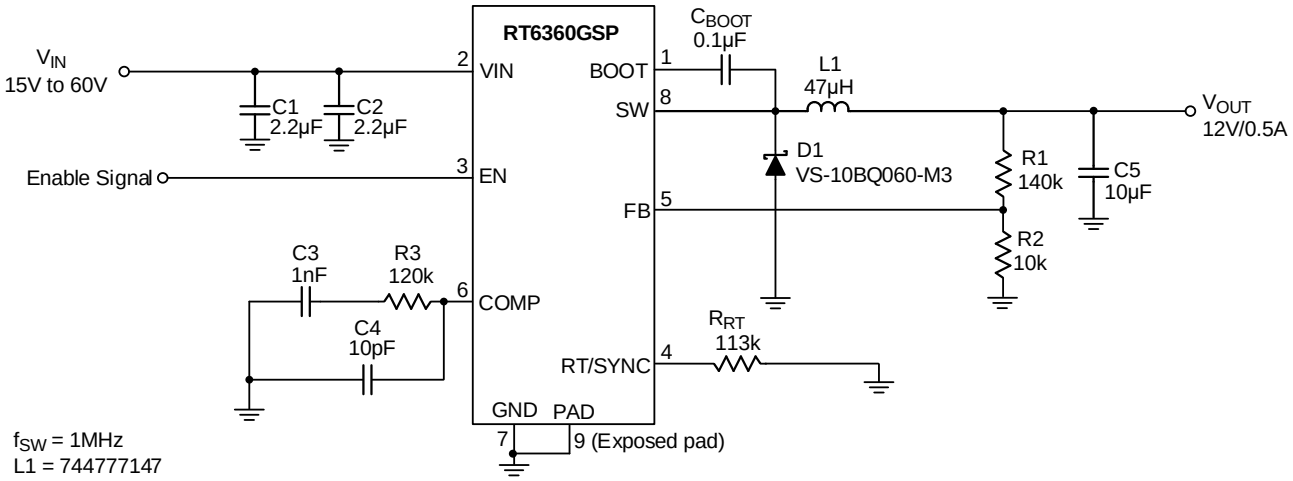


15.2 5V, 0.5A, 500kHz, Buck Converter

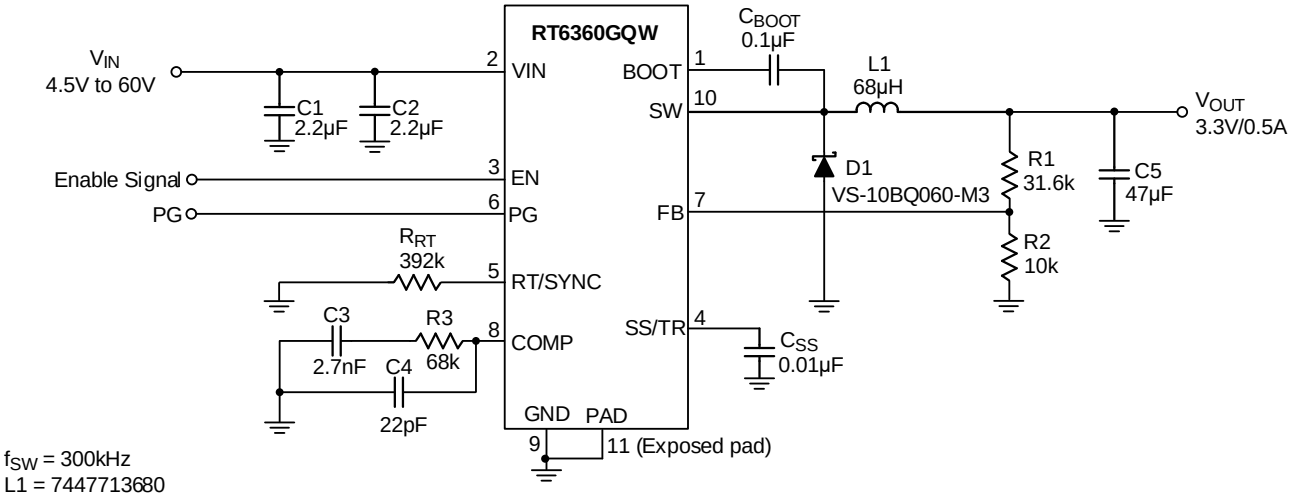


Note 7. While the input voltage is below 5.5V or the duty ratio is higher than 65%, an external bootstrap diode must be added between an external 5V voltage supply and the BOOT pin to enhance the drive capability for the high-side MOSFET. Refer to the External Bootstrap Diode section.

15.3 12V, 0.5A, 500kHz, Buck Converter

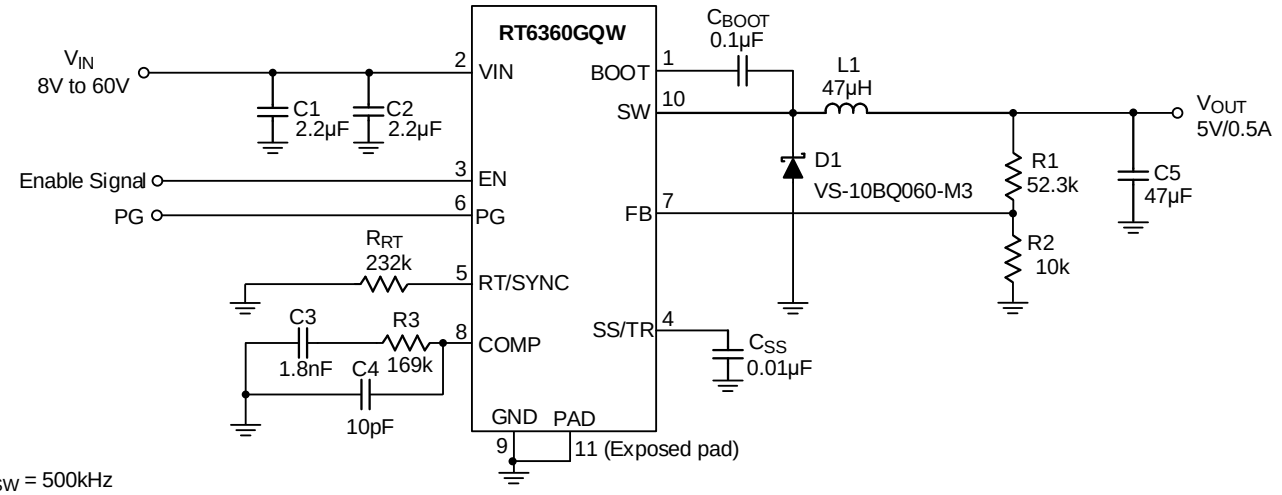


15.4 3.3V, 0.5A, 300kHz, Buck Converter



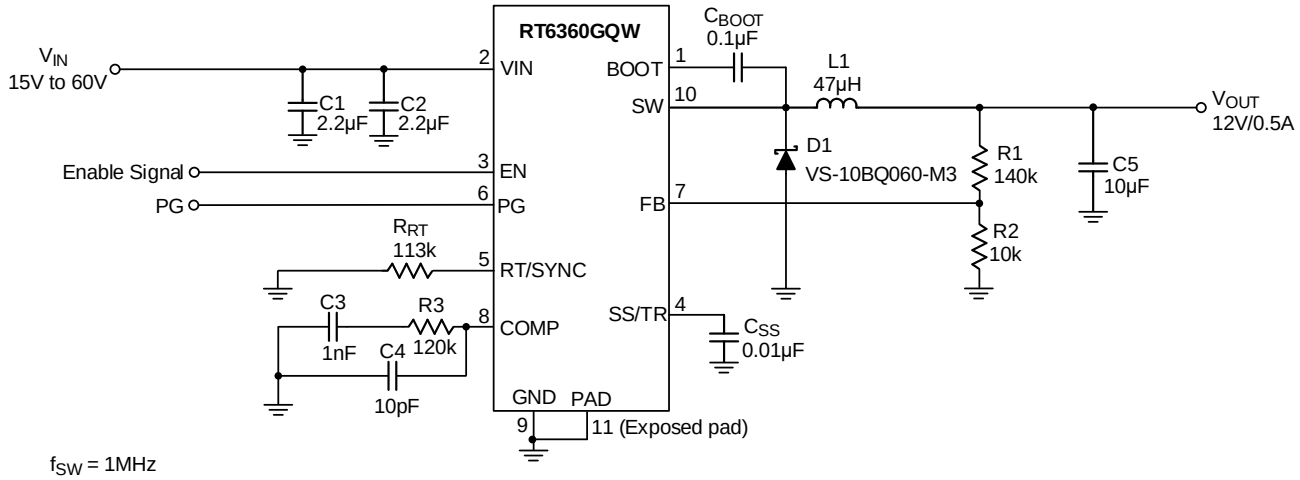
Note 8. While the input voltage is below 5.5V or the duty ratio is higher than 65%, an external bootstrap diode must be added between an external 5V voltage supply and the BOOT pin to enhance the drive capability for the high-side MOSFET. Refer to the External Bootstrap Diode section.

15.5 5V, 0.5A, 500kHz, Buck Converter



f_{SW} = 500kHz
L1 = 744777147
C5 = GRM32ER61C476KE15L
C1/C2 = HMK316AC7225KL-TE

15.6 12V, 0.5A, 1MHz, Buck Converter

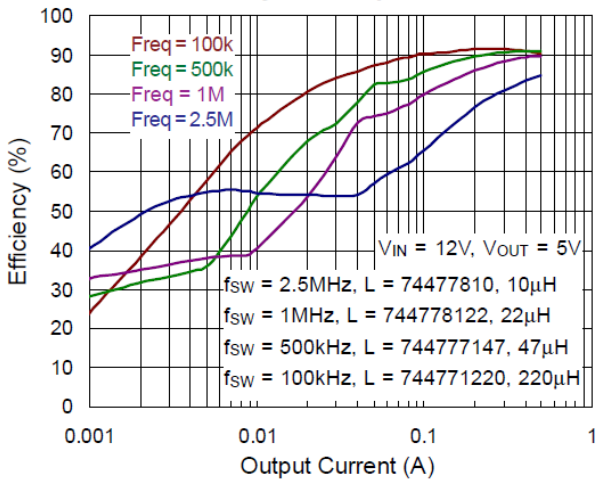


f_{SW} = 1MHz
L1 = 744777147
C5 = UMK325AB7106KM
C1/C2 = HMK316AC7225KL-TE

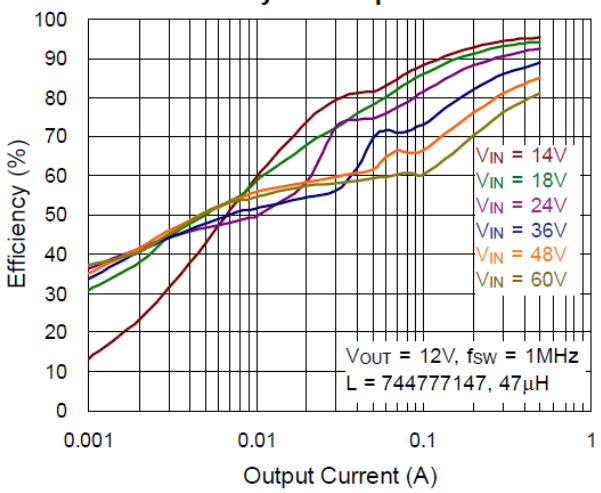
Note 9. While the input voltage is below 5.5V or the duty ratio is higher than 65%, an external bootstrap diode must be added between an external 5V voltage supply and the BOOT pin to enhance the drive capability for the high-side MOSFET. Refer to the External Bootstrap Diode section.

16 Typical Operating Characteristics

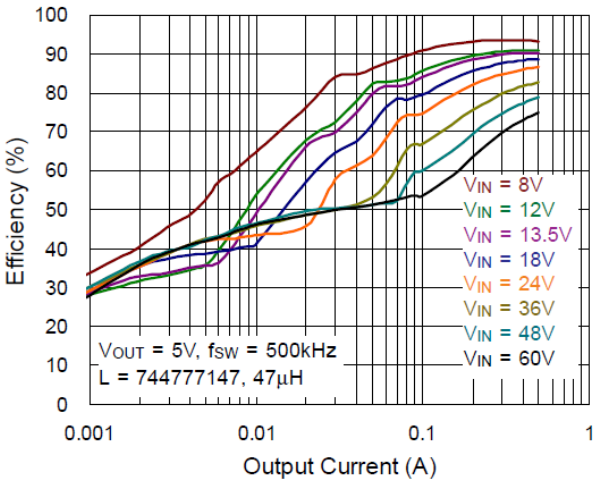
Efficiency vs. Output Current



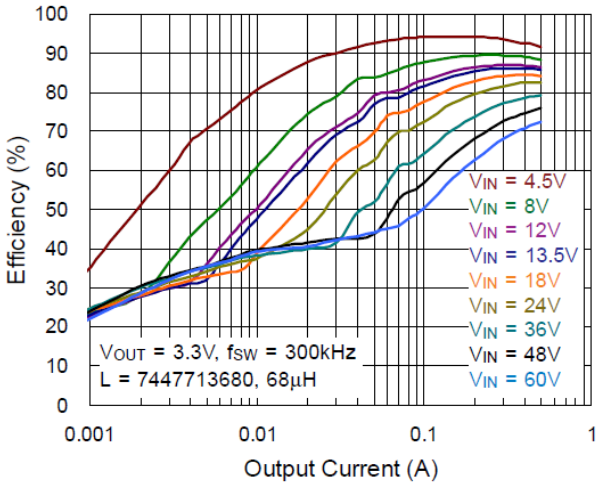
Efficiency vs. Output Current



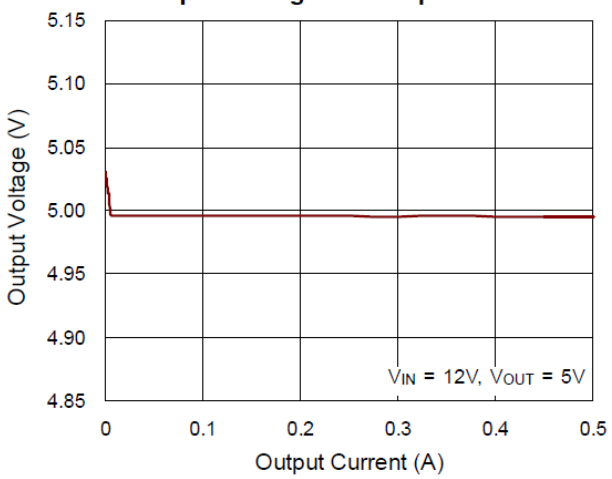
Efficiency vs. Output Current



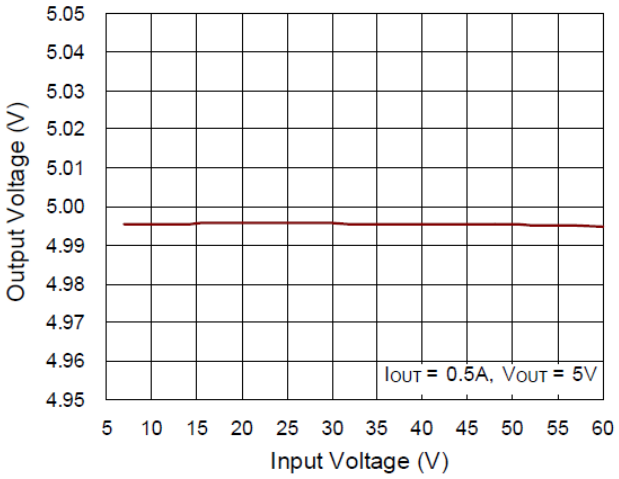
Efficiency vs. Output Current



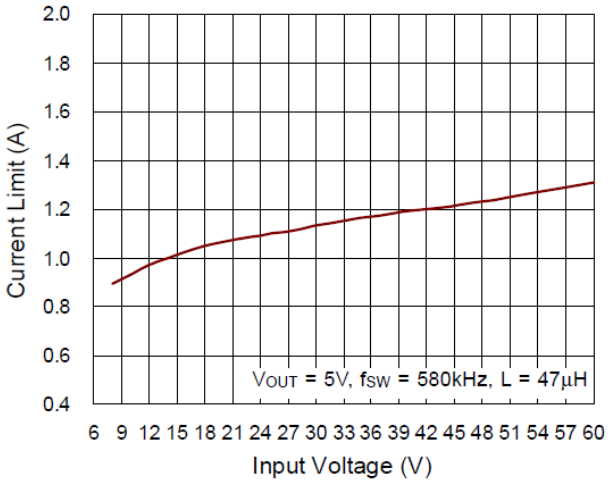
Output Voltage vs. Output Current



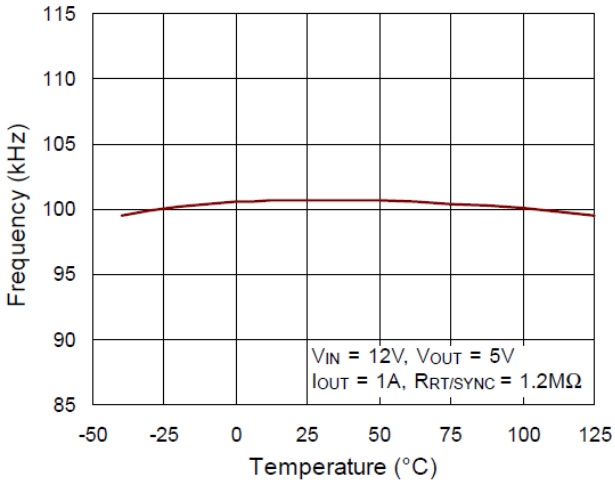
Output Voltage vs. Input Voltage



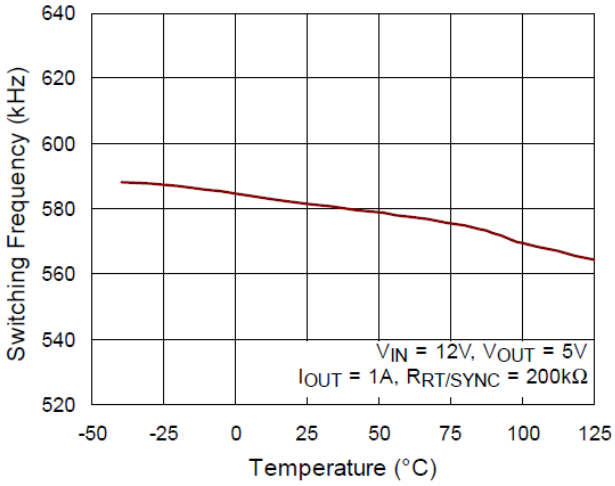
Current Limit vs. Input Voltage



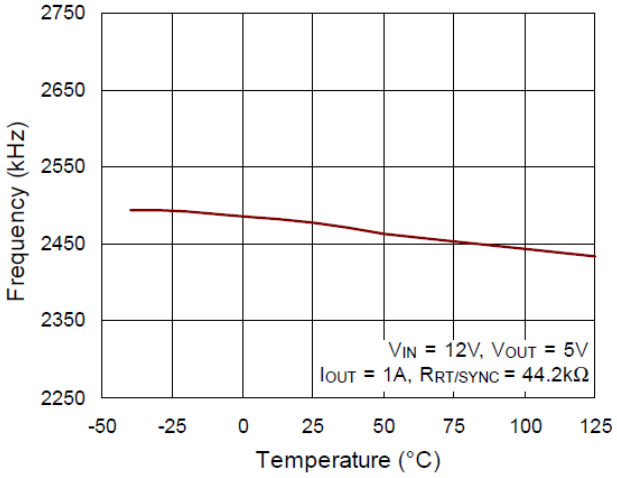
Switching Frequency vs. Temperature



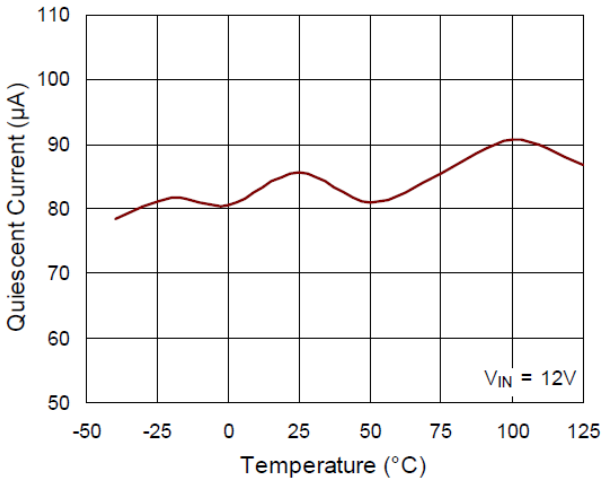
Switching Frequency vs. Temperature



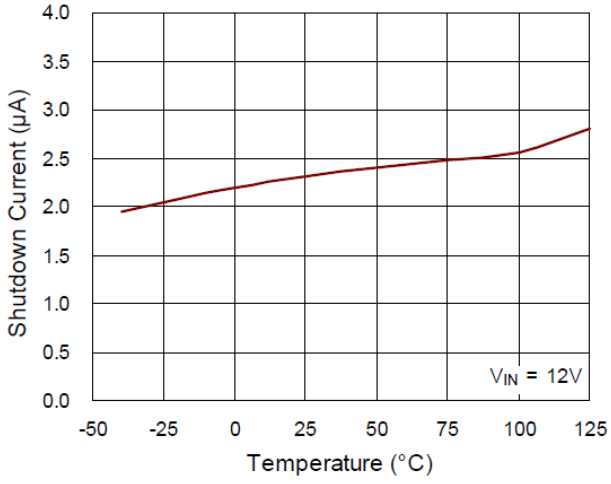
Switching Frequency vs. Temperature



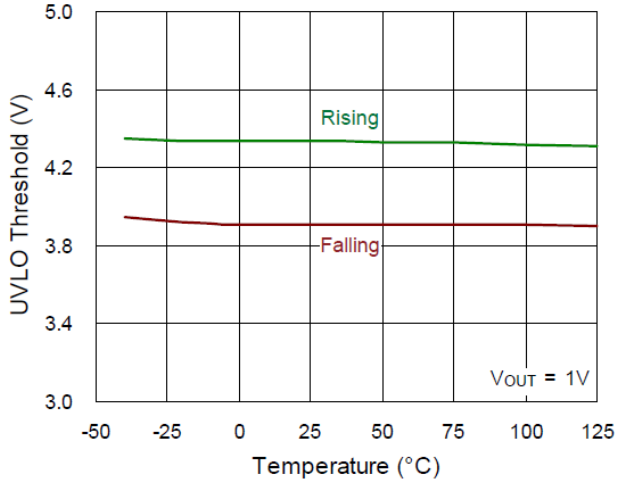
Quiescent Current vs. Temperature



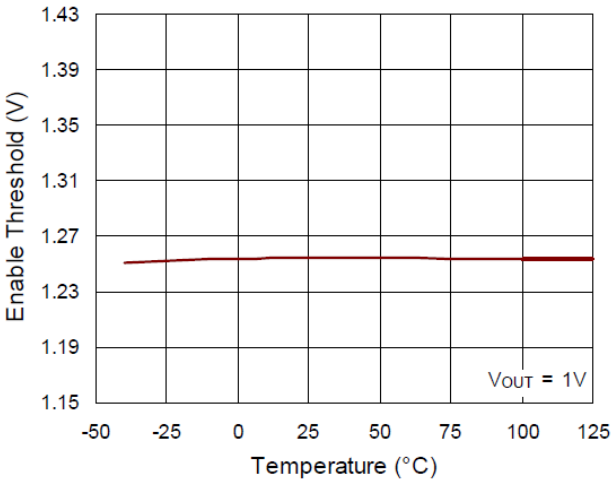
Shutdown Current vs. Temperature



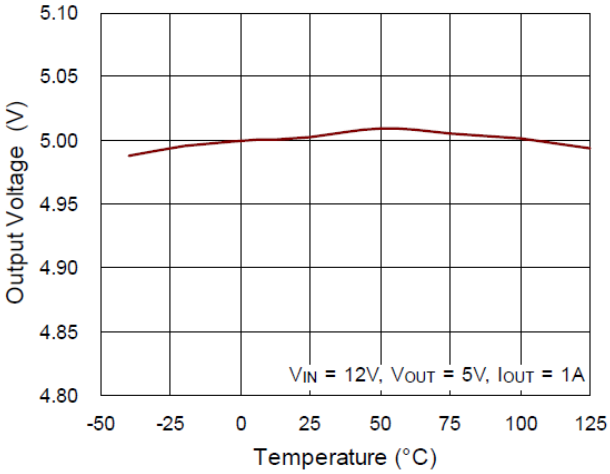
UVLO Threshold vs. Temperature



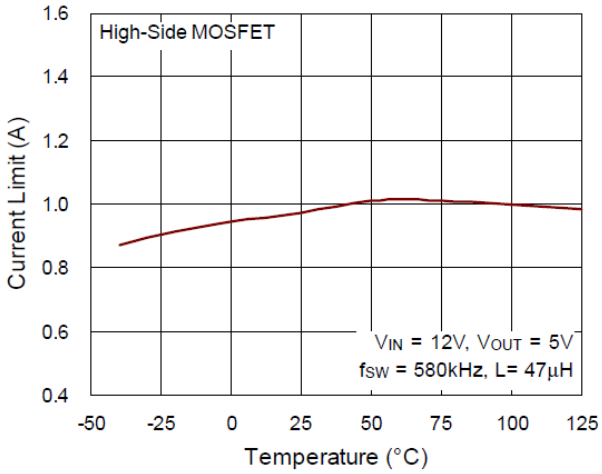
Enable Threshold vs. Temperature



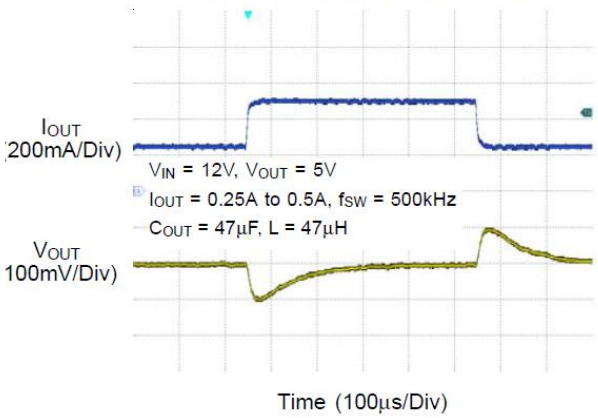
Output Voltage vs. Temperature



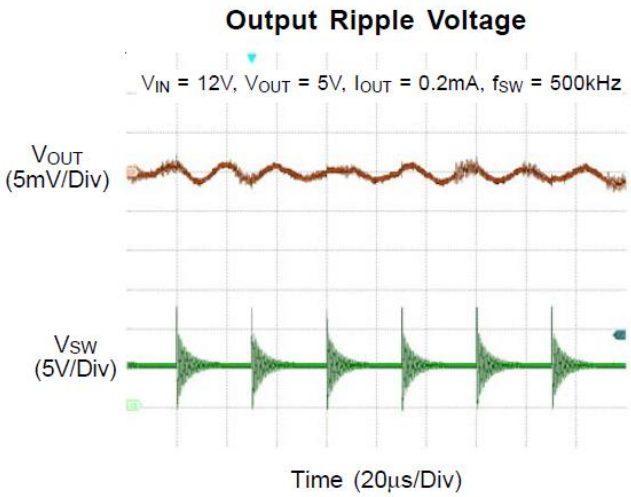
Current Limit vs. Temperature



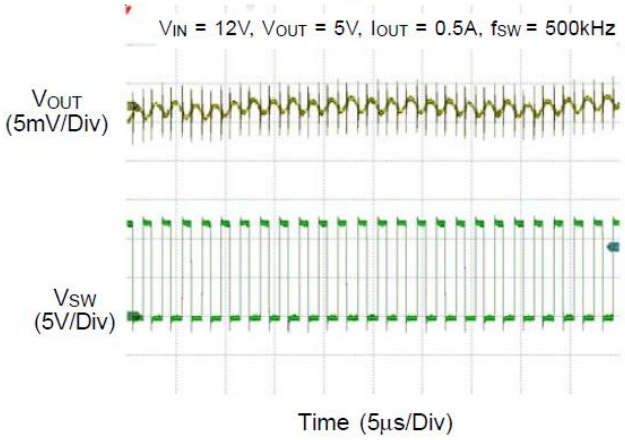
Load Transient Response



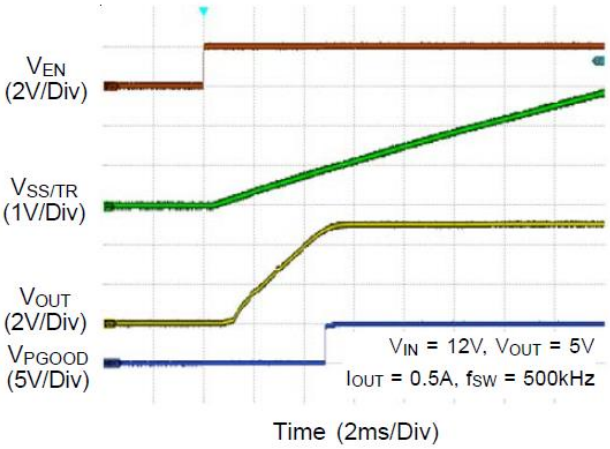
Output Ripple Voltage



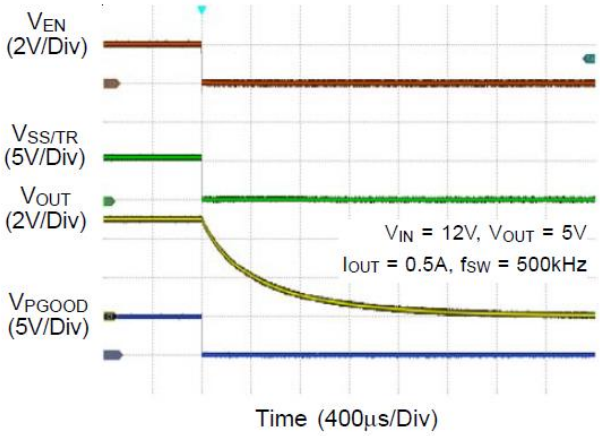
Output Ripple Voltage



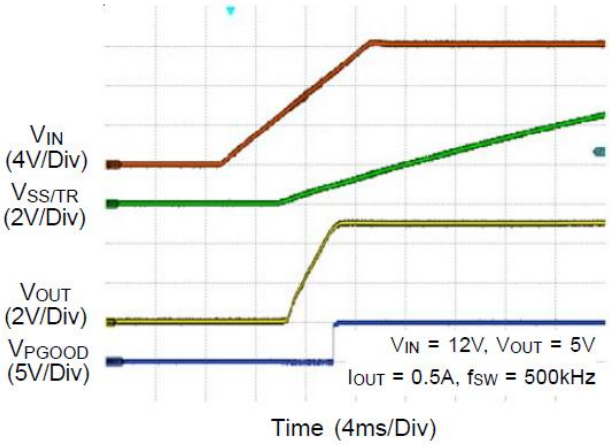
Power On from EN



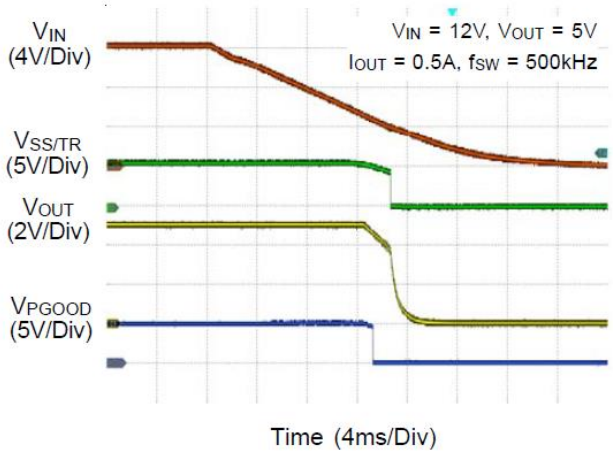
Power Off from EN



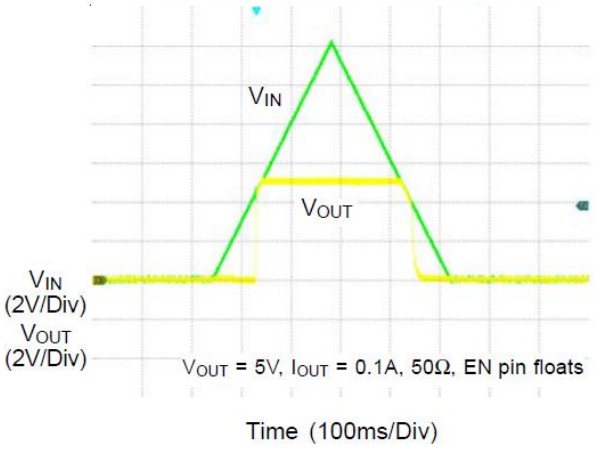
Power On from VIN



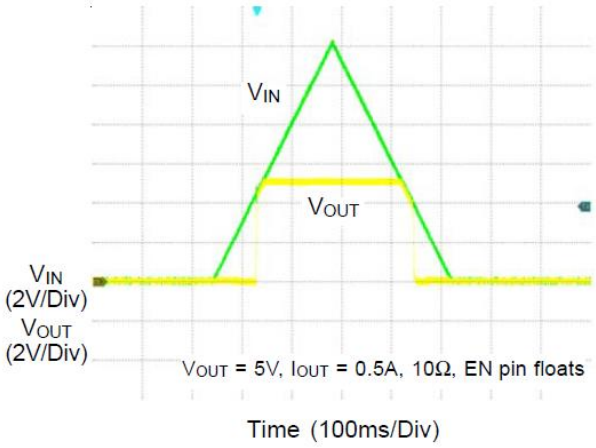
Power Off from VIN



Start-Up Dropout Performance



Start-Up Dropout Performance



17 Operation

17.1 Control Loop

The RT6360 is a high-efficiency asynchronous buck converter that utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET. At the beginning of each clock cycle, the internal high-side MOSFET turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (V_{REF}) to generate a compensation signal (V_{COMP}) on the COMP pin. A control signal derived from the inductor current is compared to the voltage at the COMP pin, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET is turned off and the inductor current ramps down. While the high-side MOSFET is off, the inductor current is supplied through the external low-side diode, or freewheel diode, connected between the SW pin and GND. This cycle repeats at the next clock cycle. In this way, the duty-cycle and output voltage are controlled by regulating the inductor current.

17.2 Light Load Operation

The RT6360 operates in power saving mode (PSM) at light load to improve light load efficiency. The IC starts to switch when V_{FB} is lower than PSM threshold (typically V_{REF} x 1.005) and stops switching when V_{FB} is high enough.

During PSM, the peak inductor current (I_{L_PEAK}) is controlled by the minimum on-time of the high-side MOSFET to ensure the low output voltage ripple. During the non-switching period, most of the internal circuit is shut down, and the supply current drops to the quiescent current (90μA, typically) to reduce the quiescent power consumption. With lower output loading, the non-switching period is longer, so the effective switching frequency becomes lower to reduce the switching loss and switch driving loss.

17.3 Switching Frequency Selection and Synchronization

The RT6360 provides an RT/SYNC pin for switching frequency selection. The switching frequency can be set using an external resistor $R_{RT/SYNC}$ and the switching frequency range is from 100kHz to 2.5MHz. The RT6360 can also be synchronized with an external clock ranging from 300kHz to 2.2MHz by the RT/SYNC pin. The switching frequency of synchronization should be equal to or higher than the frequency set by the RT resistor. For example, if the switching frequency of synchronization is 500kHz or higher, the $R_{RT/SYNC}$ should be selected for 500kHz.

The RT6360 implements a frequency foldback function to protect the device at overload or short-circuit conditions, especially at higher switching frequencies and input voltages. The switching frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8V to 0V for switching frequency control in both the RT resistor setting mode and the synchronization mode. The frequency foldback function increases the switching cycle period and provides more time for the inductor current to ramp down.

17.4 Maximum Duty Cycle Operation

The RT6360 is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than minimum off-time, the RT6360 starts to enable the skip off-time function and keeps the high-side MOSFET on continuously.

The RT6360 implements the skip off-time function to achieve a high duty cycle approaching 100% and the maximum output voltage is near the minimum input supply voltage of the application for the input voltage momentarily falls down to the normal output voltage requirement. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the

efficiency of the design.

For normal operation, the minimum input voltage can be calculated using the following equation:

$$V_{IN\_MIN} = \frac{V_{OUT} + I_{OUT\_MAX} \times R_L + V_D}{1 - f_{SW} \times t_{OFF\_MIN}} + I_{OUT\_MAX} \times R_{DSON\_H} - V_D$$

where V_{IN_MIN} is the minimum normal operating input voltage; R_{DSON_H} is the on-resistance of the high-side MOSFET; V_D is the forward conduction voltage of the freewheel diode; R_L is the DC resistance of the inductor.

17.5 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of the BOOT capacitor for turning on the high-side MOSFET under any conditions. The BOOT UVLO usually actives at an extremely high conversion ratio or when the higher VOUT application operates at a very light load. Under such conditions, when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_F}$ (typically 2.7V), the device turns on the internal BOOT recharge MOSFET (typically 150ns) to charge the BOOT capacitor. The BOOT UVLO is sustained until the BOOT to SW voltage is higher than $V_{BOOT\_UVLO\_R}$ (typically 2.8V).

17.6 Enable Control

The RT6360 provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below the enable threshold voltage, switching is inhibited even if the VIN voltage is above the VIN undervoltage-lockout threshold (V_{UVLO_R}). If V_{EN} is held below 0.4V, the converter will enter shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (typically 1.3μA). If the EN voltage rises above the enable threshold voltage while the VIN voltage is higher than V_{UVLO_R}, the device will be turned on, that is, switching is enabled and the soft-start sequence is initiated. The EN pin has an internal pull-up current source I_{PU_EN} (typically 0.9μA) that enables the operation of the RT6360 when the EN pin is floating. The EN pin can be used to adjust the undervoltage-lockout (UVLO) threshold and hysteresis by using two external resistors. The RT6360 implements an additional hysteresis current source I_{EN_HYS} (typically 2.9μA) to adjust the UVLO. The I_{EN_HYS} is sourced out of the EN pin when V_{EN} is larger than enable threshold voltage. When the V_{EN} falls below the enable threshold voltage, the I_{EN_HYS} will stop sourcing out of the EN pin.

17.7 Soft-Start and Tracking Control

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ6360GSP provides an internal soft-start and the RT6360GQW provides an external soft-start function for inrush currents control. The RQT6363GQW provides an SS/TR pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor $C_{SS/TR}$ connected from the SS/TR pin to ground or controlled by external ramp voltage to the SS/TR pin. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically 2μA) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The high-side MOSFET will start switching if the voltage difference between the SS/TR pin and the FB pin is equal to 75mV (typically $V_{SS/TR} - V_{FB}$ = 75mV,) during the power-up period. If the output is pre-biased to a certain voltage during start-up, the device will not start switching until the voltage difference between the SS/TR pin and the FB pin is equal to 75mV (typical). Only when this ramp voltage is higher than the feedback voltage V_{FB}, the switching will resume. The FB voltage will track the SS/TR pin ramp voltage with an SS/TR to FB offset voltage (typically 75mV) during the soft-start interval. The output voltage can then ramp up smoothly to its target regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected. After the FB pin voltage rises above 94% of V_{REF} (typical), the PG pin will be in high impedance and the V_{PG} will be held high. The typical start-up waveform shown in Figure 1 indicates the sequence and timing between the output voltage and related voltages.

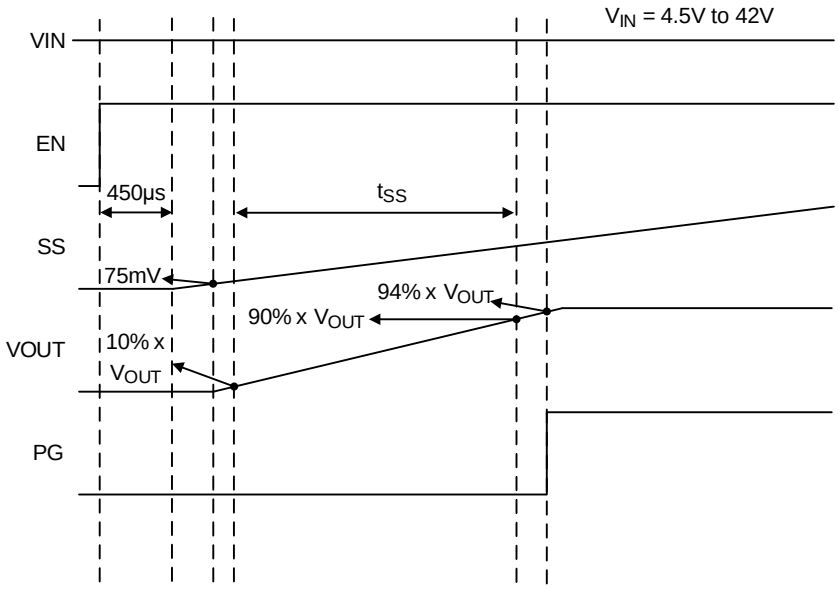


Figure 1. Start-Up Sequence for RT6360GQW

17.8 Power-Good Indication

The RT6360GQW features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of the comparator prevents false flag operations for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to an external voltage source and it is recommended to use a pull-up resistance between the values of 1kΩ and 10kΩ to reduce switching noise coupling to the PG pin. The PG assertion requires an input voltage above 1.5V. The power-good function is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above the power-good high threshold (V_{TH_PGLH1}) (typically 94% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high after a certain delay. When V_{FB} falls below the power-good low threshold (V_{TH_PGHL2}) (typically 92% of the reference voltage) or exceeds V_{TH_PGHL1} (typically 109% of the reference voltage), the PG pin will be pulled low. For V_{FB} higher than V_{TH_PGHL1}, V_{PG} can be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 106% of the reference voltage). Once started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device (typically 6Ω) will pull the PG pin low. The Power-Good indication profile is shown in Figure 2.

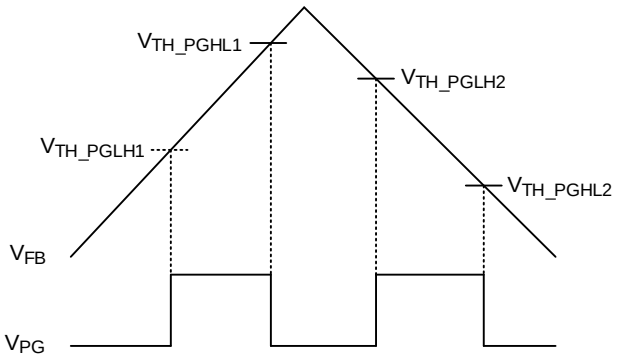


Figure 2. The Logic of PG for RT6360GQW

17.9 Spread-Spectrum Operation

Due to the periodicity of the switching signals, the energy is radiated which can cause EMI issues. The built-in spread-spectrum frequency modulation further helps system designers with better EMC management. The spread spectrum can be active when soft-start is finished and zero-current is not detected. The spread-spectrum is implemented using a pseudo-random sequence and applies a +6% spread to the switching frequency. For example, when the RT6360 is programmed to 2.1MHz, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RT6360 still guarantees that the 2.1MHz switching frequency does not drop into the AM band limit of 1.8MHz.

17.10 Input Undervoltage-Lockout

In addition to the EN pin, the RT6360 also provides an enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, the switching will be inhibited until the VIN voltage rises above V_{UVLO_R}. This ensures that the internal regulator is ready so that the operation with a not-fully-enhanced internal high-side MOSFET can be prevented. After the device is powered up, if the input voltage V_{IN} falls below the UVLO falling threshold voltage (V_{UVLO_L}), this switching will be inhibited; if V_{IN} rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume switching. Note that V_{IN} = 4V is only designed for the input voltage momentarily falls to the UVLO threshold voltage requirement, and the normal input voltage should be higher than V_{UVLO_R}.

17.11 High-Side Switch Current-Limit Protection

The RT6360 includes a cycle-by-cycle high-side switch current-limit protection against the condition that the inductor current increasing abnormally, even exceeding the inductor saturation current rating. The inductor current through the high-side MOSFET will be measured after a certain amount of delay when the high-side MOSFET is turned on. If a current-limit condition occurs, the converter will immediately turn off the high-side MOSFET to prevent the inductor current from exceeding the high-side switch current limit (I_{LIM_H}).

17.12 Output Undervoltage Protection

The RT6360 includes output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the internal high-side switch. If the output undervoltage condition continues for a period of time, the RT6360 enters the output undervoltage protection with hiccup mode and discharges the $C_{SS/TR}$ by an internal discharging current source I_{SS_DIS} (typically 0.5μA). During hiccup mode, the device remains shutdown. After the SS pin voltage is discharged to less than 54mV (typical), the RT6360 attempts to restart, and the internal charging current source I_{SS} (typically 2μA) gradually increases the voltage on $C_{SS/TR}$. The high-side MOSFET will start switching when the voltage difference between the SS pin and the FB pin equals 75mV (typical, $V_{SS} - V_{FB}$ = 75mV). If the output undervoltage condition is not removed, the high-side MOSFET stops switching when the voltage difference between the SS pin and the FB pin is 1.2V (typical, $V_{SS} - V_{FB}$ = 1.2V) and then the I_{SS_DIS} discharging current source begins to discharge $C_{SS/TR}$. Upon completion of the soft-start sequence, if the output undervoltage condition is removed, the converter will resume normal operation; otherwise, the auto-recovery cycle will repeat until the output undervoltage condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short-circuit condition is removed.

A short-circuit protection and recovery profile is shown in Figure 3.

Since the $C_{SS/TR}$ will be discharged to 54mV when the RT6360 enters output undervoltage protection, the first discharging time (t_{SS_DIS1}) can be calculated as follows:

$$t_{SS\_DIS1} = C_{SS} \times \frac{V_{SS} - 0.054}{I_{SS\_DIS}}$$

The equation below assumes that the V_{FB} will be 0 during a short-circuit condition and can be used to calculate the $C_{SS/TR}$ discharging time (t_{SS_DIS2}) and charging time (t_{SS_CH}) during hiccup mode.

$$t_{SS\_DIS2} = C_{SS} \times \frac{1.146}{I_{SS\_DIS}}$$

$$t_{SS\_CH} = C_{SS} \times \frac{1.146}{I_{SS\_CH}}$$

Figure 3. Short-Circuit Protection and Recovery

17.13 Output Overvoltage Protection

The RT6360 includes an output overvoltage protection (OVP) circuit to limit output voltage. When the V_{FB} is lower than the reference voltage (V_{REF}) under overload or short-circuit conditions, the COMP voltage will be high to demand maximum output current. Once the overload or short-circuit condition is removed, the COMP voltage returns to the normal voltage to regulate the output voltage. The output voltage leads to the possibility of an output overshoot if the load transient is faster than the COMP voltage transient response, especially for small output capacitance. If the V_{FB} exceeds 109% of the reference voltage, the high-side MOSFET will be forced off to limit the output voltage. When the V_{FB} drops below 106% of the reference voltage, the high-side MOSFET will resume operation.

17.14 Pin-Short Protection

The RT6360 provides pin-short protection for neighbor pins. The internal protection fuse will burn out to prevent IC smoke, fire, and sparks when the BOOT pin is shorted to the VIN pin. The EN pin with its high-voltage rating, can avoid IC burn-out when the EN pin is shorted to the VIN pin. The hiccup mode protection will be triggered to avoid IC burn-out when the SW pin is shorted to ground when the internal high-side MOSFET is turned on.

17.15 Over-Temperature Protection

The RT6360 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operations when the junction temperature exceeds the over-temperature protection threshold T_{OTP}. Once the junction temperature cools down by the over-temperature protection hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions.

The protection is activated outside the absolute maximum operational range as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or cause permanent damage.

18 Application Information

(Note 11)

A general RT6360 application circuit is shown in the Typical Application Circuit section. External component selection is largely driven by the load requirements and begins with the switching frequency selection using the external resistor RT/SYNC. Next, the inductor L, the input capacitor C_{IN}, the output capacitor C_{OUT} and freewheel diode are chosen. Next, feedback resistors and the compensation circuit are selected to set the desired output voltage and crossover frequency, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as EN, external soft-start, PG, and synchronization.

18.1 Switching Frequency Setting

The RT6360 offers an adjustable switching frequency setting, which can be set using the external resistor $R_{RT/SYNC}$. The switching frequency range is from 100kHz to 2.5MHz. The selection of the operating frequency is a trade-off between efficiency and component size. High-frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage. Additional constraints on operating frequency include the minimum on-time and minimum off-time. The minimum on-time, t_{ON_MIN}, is the shortest duration in which the high-side switch can be in its “on” state. The minimum on-time of the RT6360 is 100ns (typical). In continuous mode operation, the maximum operating frequency, f_{SW_MAX}, can be derived from the minimum on-time according to the formula below:

$$f_{SW\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times V_{IN\_MAX}}$$

where V_{IN_MAX} is the maximum operating input voltage.

The minimum off-time, t_{OFF_MIN}, is the shortest duration that the RT6360 can trip the current comparator and turn the high-side MOSFET back off. The minimum off-time of the RT6360 is 130ns (typical). If the switching frequency should be constant, the required off-time needs to be larger than the minimum off-time. The calculation for the minimum off-time, considering loss terms, is shown as follows:

$$t_{OFF\_MIN} \leq \frac{1 - \left[\frac{V_{OUT} + (I_{OUT\_MAX} \times R_L) + V_D}{V_{IN\_MIN} - (I_{OUT\_MAX} \times R_{DSON\_H}) + V_D}\right]}{f_{SW}}$$

where R_{DSON_H} is the on-resistance of the high-side MOSFET; V_D is the forward conduction voltage of the freewheel diode; R_L is the DC resistance of the inductor.

The switching frequency f_{SW} is set by the external resistor $R_{RT/SYNC}$ connected between the RT/SYNC pin and ground. The failure mode and effects analysis (FMEA) considerations are applied to the RT/SYNC pin setting to avoid abnormal switching frequency operation under failure conditions. This includes failure scenarios such as a short-circuit to ground or the pin being left open. The switching frequency will be 860kHz (typical) when the RT/SYNC pin is shorted to ground, and 230kHz (typical) when the pin is left open. The equation below shows the relation between setting frequency and the $R_{RT/SYNC}$ value.

$$R_{RT/SYNC}\ (k\Omega) = \frac{140398}{f_{SW}^{1.03}}$$

where f_{SW} (kHz) is the desired setting frequency. It is recommended to use resistors with 1% tolerance or better, and the temperature coefficient of 100 ppm or less. Figure 4 shows the relationship between switching frequency and the $R_{RT/SYNC}$ resistor.

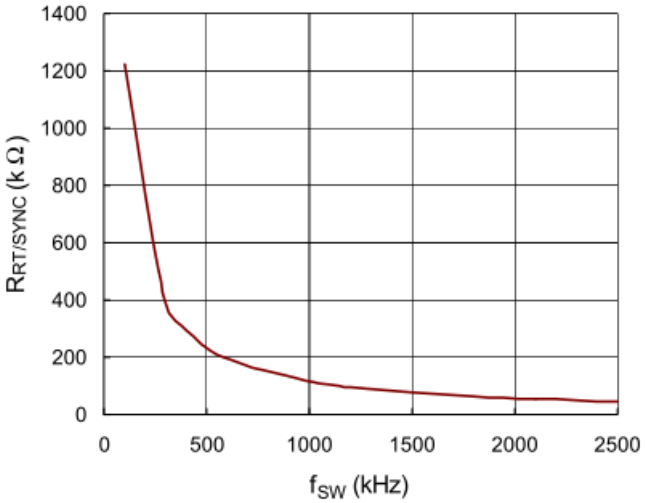


Figure 4. Switching Frequency vs. $R_{RT/SYNC}$

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This results in additional phase lag in the loop and reduces the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for a smaller case size, but the increased ripple lowers the effective current-limit threshold and increases the AC losses in the inductor. It also causes insufficient slope compensation and ultimately loop instability as the duty cycle approaches or exceeds 50%. When the duty cycle exceeds 50%, the following condition needs to be satisfied:

$$0.5 \times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (0.5A).

To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits within the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

18.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET. The C_{IN} should be sized appropriately to prevent large variations in input voltage. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 5 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors.

For ceramic capacitors, the equivalent series resistance (ESR) is very low, so that the ripple caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} is the maximum input ripple voltage.

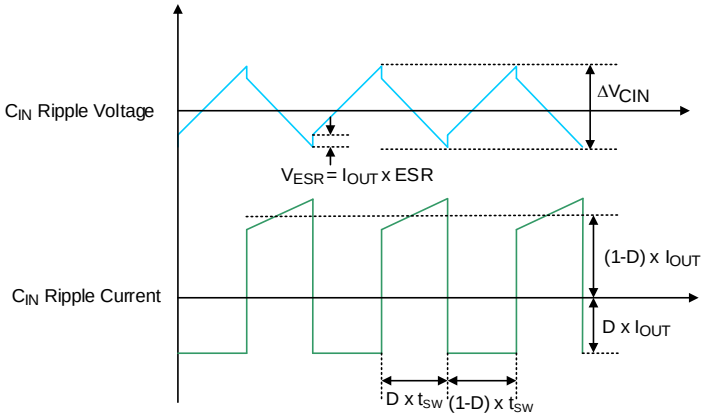


Figure 5. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) using the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the

requirement to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at a 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, making it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (under-damped) tank circuit. If the RT6360 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin with a low inductance connection to the GND of the IC. The VIN pin must be bypassed to ground with a minimum value of effective capacitance 1.5μF. For a 500kHz switching frequency application, two 2.2μF, X7R capacitors can be connected between the VIN pin and the GND pin. The larger input capacitance is required when a lower switching frequency is used. For filtering high-frequency noise, an additional small 0.1μF capacitor should be placed close to the part, and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.4 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The highest output ripple is at maximum input voltage since ΔI_L increases with the input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the effective output capacitance value. The amount of the output sag/soar is a function of the crossover frequency factor at PWM, and can be calculated using the following equation:

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The X7R dielectric capacitor is recommended for the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage, and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated values when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance

will also decrease the output voltage ripple.

18.5 Freewheel Diode Selection

When the high-side MOSFET turns off, the inductor current is supplied through the external low-side diode, known as the freewheel diode, which is connected between the SW pin and GND.

The reverse voltage rating of the freewheel diode should be equal to or greater than the V_{IN_MAX}. The maximum average forward rectified current of the freewheel diode should be equal to or greater than the maximum load current. Considering the efficient performance, the diode must have a minimum forward voltage and reverse recovery time. Therefore, Schottky diodes are recommended for use as freewheel diodes.

The selected forward voltage of the Schottky diode must be less than the forward voltage restriction in Figure 6 at operating temperature range to avoid the IC malfunction.

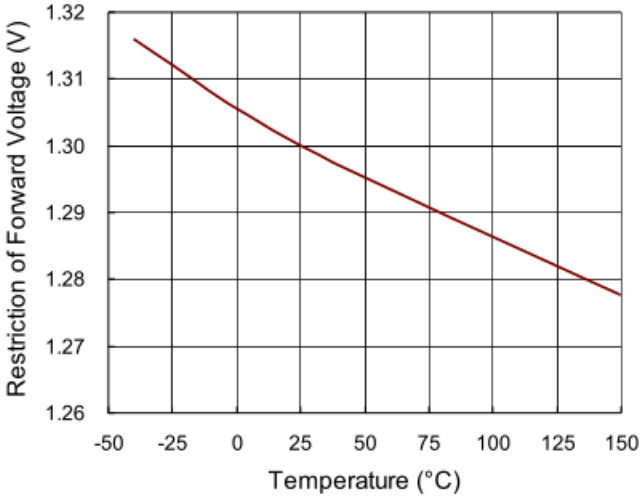


Figure 6. Restriction of Forward Voltage vs. Temperature

The losses of the freewheel diode must be considered to ensure sufficient power rating for diode selection. The conduction loss in the diode is determined by the forward voltage of the diode, and the switching loss in the diode can be determined by the junction capacitor of the diode. The power dissipation of the diode can be calculated using the following formula:

$$P_D = P_{D\_CON} + P_{D\_SW} = I_{OUT} \times V_D \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{2} \times C_J \times (V_{IN} + V_D)^2 \times f_{SW}$$

where C_J is the junction capacitance of the freewheel diode.

18.6 Output Voltage Programming

The output voltage can be programmed using a resistive divider connected from the output to ground, with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 7. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage V_{REF} is 0.8V (typical).

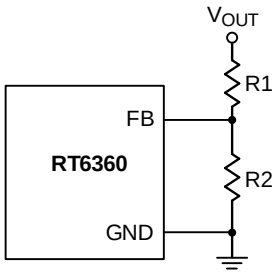


Figure 7. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 should not exceed 80kΩ for noise immunity consideration. The resistance of R1 can then be calculated using the following equation:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

18.7 Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operation. Typical symptoms of an unstable power supply include audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFET, and so on.

In most cases, the peak current mode control architecture used in the RT6360 only requires two external components to achieve a stable design, as shown in Figure 8. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. Around the crossover frequency, the peak current mode control (PCMC) equivalent circuit of a Buck converter can be simplified, as shown in Figure 9. The method presented here is easy to calculate and ignores the effects of the internal slope compensation. Since the slope compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot fully account of the circuit parasitics and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer, while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the steps below to calculate the compensation components:

1. Set up the crossover frequency, f_C. For stability purposes, the target is to have a loop gain slope that is −20dB/decade from a very low frequency to beyond the crossover frequency. In general, one-twentieth to one-tenth of the switching frequency (5% to 10% of f_{SW}) is recommended to be the crossover frequency. Do "NOT" design the crossover frequency over 80kHz with the RT6360. For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside of the high bandwidth is that it increases the susceptibility of the regulators to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.
2. R_{COMP} can be determined by:

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF} \times gm\_cs} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_cs} \times \frac{R1 + R2}{R2}$$

where gm is the error amplifier gain of transconductance (97μA/V); gm_cs is COMP to current sense transconductance (2A/V); the variation of C_{OUT} with temperature, DC bias voltage, and switching frequency needs

to be taken into consideration.

3. A compensation zero can be placed at or before the dominant pole of the buck, which is provided by the output capacitor and maximum output loading (R_L). Calculate C_{COMP}:

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

4. Set the compensation pole to the frequency at the ESR zero or 1/2 of the operating frequency. The output capacitor and its ESR provide a zero, and optional C_{COMP2} can be used to cancel this zero.

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

If 1/2 of the operating frequency is lower than the ESR zero, the compensation pole is set at 1/2 of the operating frequency.

$$C_{COMP2} = \frac{1}{2 \times \pi \times \frac{fsw}{2} \times R_{COMP}}$$

Note 10. Generally, C_{COMP2} is an optional component used to enhance noise immunity.

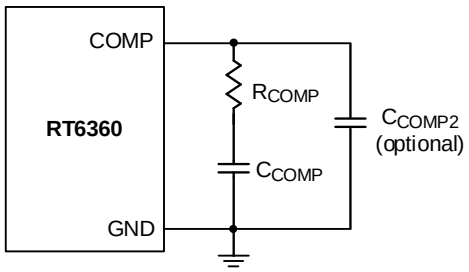


Figure 8. External Compensation Components

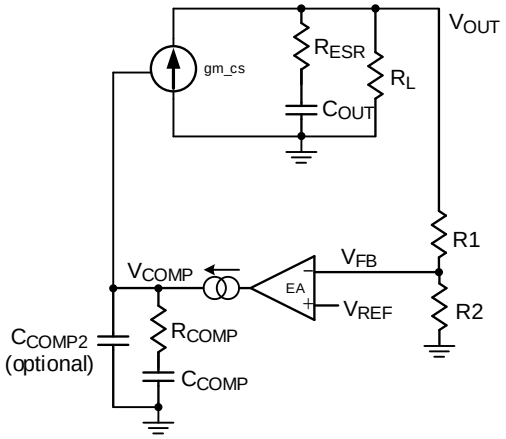


Figure 9. Simplified Equivalent Circuit of Buck Converter with PCMC

18.8 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the bootstrap capacitor is charged through an internal diode to an internal voltage source each time the low-side freewheel diode conducts. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1µF, 0603 ceramic capacitor with X7R is recommended, and the capacitor should have a 6.3 V or higher voltage rating.

18.9 External Bootstrap Diode

An external bootstrap diode should be added between an external 5V voltage supply and the BOOT pin to enhance the high-side MOSFET and improve efficiency when the input voltage is below 5.5V or the duty ratio is higher than 65%. The recommended application circuit is shown in Figure 10. The bootstrap diode can be a low-cost one, such as 1N4148. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6360. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. Figure 11 shows an efficiency comparison between with and without bootstrap diode.

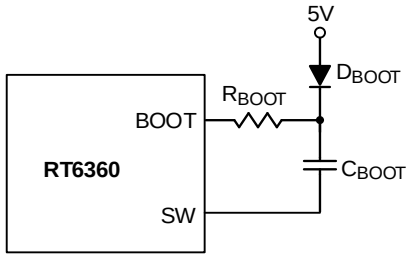


Figure 10. External Bootstrap Diode

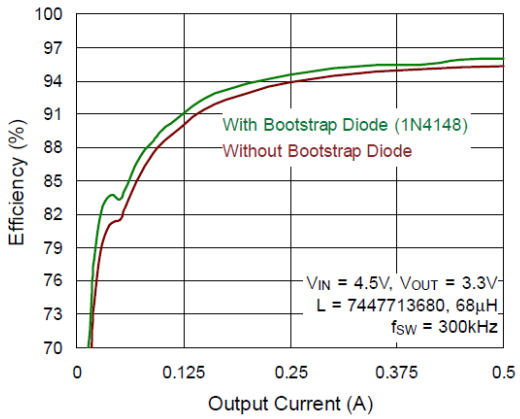


Figure 11. Efficiency Comparison between with and without Bootstrap Diode

18.10 External Bootstrap Resistor (Optional)

The gate driver of an internal high-side MOSFET, utilized as a high-side switch, is optimized for turning on the switch. The gate driver is not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to induced high di/dt noises. When the high-side MOSFET is turned off, the SW node will be discharged relatively slowly by the inductor current because of the presence of the dead time when both the high-side MOSFET and low-side freewheel diode are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation.

The turn-on rate of the high-side MOSFET can be slowed by placing a small bootstrap resistor R_{BOOT} between the BOOT pin and the external bootstrap capacitor, as shown in Figure 12. The recommended range for R_{BOOT} is several ohms to 10 ohms, and it can be 0402 or 0603 in size.

This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhance the internal high-side MOSFET, the recommended application circuit is shown in Figure 13, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection.

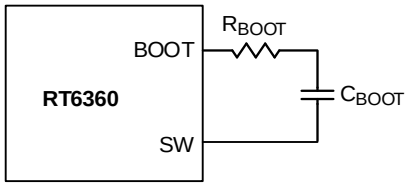


Figure 12. External Bootstrap Resistor at the BOOT Pin

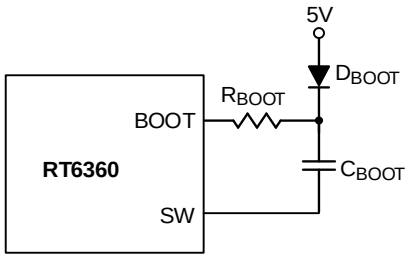


Figure 13. External Bootstrap Diode and Resistor at the BOOT Pin

18.11 EN Pin for Start-Up and UVLO Adjustment

For automatic start-up, the EN pin has an internal pull-up current source I_{EN} (typically 0.9μA) that enables the operation of the RT6360 when the EN pin is left floating. If the EN voltage rises above the V_{TH_EN} (typically 1.25V) and the VIN voltage is higher than V_{UVLO_R} (typically 4.3V), the device will be turned on, that is, switching is enabled and the soft-start sequence is initiated. If the high UVLO is required, the EN pin can be used to adjust the undervoltage-lockout (UVLO) threshold and hysteresis. There is an additional hysteresis current source I_{EN_HYS} (typically 2.9μA), which is sourced from the EN pin when the EN pin voltage exceeds V_{TH_EN}. When the EN pin drops below V_{TH_EN}, the I_{EN_HYS} is removed. Therefore, the EN pin can be externally connected to V_{IN} by adding two resistors, R_{ENH} and R_{ENL} to achieve UVLO adjustment, as shown in Figure 14.

According to the desired start and stop input voltages, the resistance of R_{EN1} and R_{EN2} can be obtained using the following formula:

$$R_{EN1} = \frac{V_{Start} - V_{Stop}}{I_{EN\_Hys}}$$

$$R_{EN2} = \frac{V_{TH\_EN}}{\frac{V_{Start} - V_{TH\_EN}}{R_{EN1}} + I_{EN}}$$

where I_{EN} is the enable pull-up current source value before the EN pin voltage exceeds the V_{TH_EN} (typically 0.9μA).

The EN pin, with high-voltage rating, supports a wide input voltage range to adjust the VIN UVLO.

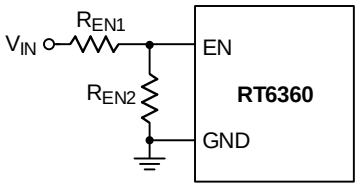


Figure 14. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.12 Soft-Start and Tracking Control

The RT6360GQW provides an adjustable soft-start function, which is used to prevent large inrush currents during power-up. The RT6360GQW provides an SS/TR pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor $C_{SS/TR}$ connected from the SS/TR pin to ground or controlled by an external ramp voltage to the SS/TR pin. An internal current source I_{SS} (typically 1.7μA) charges an external capacitor to build a soft-start ramp voltage. The internal charging current source I_{SS} gradually increases the voltage on $C_{SS/TR}$, and the high-side MOSFET will start switching if the voltage difference between the SS/TR pin and the FB pin is equal to 42mV (typically $V_{SS/TR} - V_{FB}$ = 75mV) during the power-up period. The FB voltage will track the SS/TR pin ramp voltage with an SS/TR to FB offset voltage (typically 75mV) during the soft-start interval. The typical soft-start time (t_{SS}), which is the duration of V_{OUT} rises from 10% to 90% of the set value, is calculated as follows:

$$t_{SS} = C_{SS/TR} \times \frac{V_{REF} \times 0.8}{I_{SS}}$$

If a heavy load is added to the output with large capacitance, the output voltage will never enter regulation because of UVP. Thus, the device remains in hiccup operation. The $C_{SS/TR}$ should be large enough to ensure the soft-start period ends after C_{OUT} is fully charged.

$$C_{SS/TR} \geq C_{OUT} \times \frac{I_{SS} \times V_{OUT}}{0.8 \times I_{COUT\_CHG}}$$

where I_{COUT_CHG} is the C_{OUT} charge current, which is related to the switching frequency, inductance, high-side MOSFET peak current limit, and load current.

18.13 Power-Good Output

The RT6360GQW features an open-drain power-good output (PG) to monitor the output voltage status. The PG pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

It is recommended to use a pull-up resistor between 1kΩ and 10kΩ to reduce the switching noise coupling to the PG pin.

18.14 Synchronization

The RT6360 can be synchronized with an external clock ranging from 300kHz to 2.2MHz, which is applied to the RT/SYNC pin. The minimum synchronous pulse width of the external clock applied to the RT/SYNC pin must be larger than 40ns, and the amplitude should have valleys below 0.5V and peaks above 2.2V (up to 6V). The rising edge of the SW will be synchronized to the falling edge of the RT/SYNC pin signal.

The switching frequency control of the RT6360 will switch from the RT resistor setting mode to the synchronization mode when the external clock is applied to the RT/SYNC pin. The RT6360 transitions from the RT resistor setting mode to the synchronization mode within 60 microseconds. Figure 15 and Figure 16 show the device synchronized to an external system clock in power-saving mode (PSM) and continuous conduction mode (CCM).

The sub-harmonic oscillation may occur for duty cycle greater than 50% in CCM at synchronization mode. By choosing a larger inductor, more slope compensation can be achieved, thereby eliminating the risk of such sub-harmonic oscillations.

The switching frequency of synchronization should be equal to or higher than the frequency set with the RT resistor. For example, if the switching frequency of synchronization is 500kHz and higher, the $R_{RT/SYNC}$ should be selected for 500kHz. Be careful to design the compensation network and inductance for switching frequency control in both RT resistor setting mode and the synchronization mode.

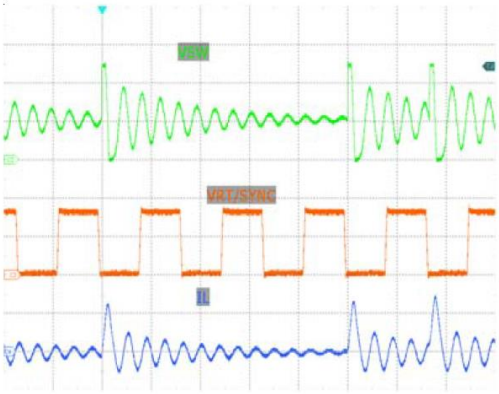


Figure 15. Synchronization Mode in PSM

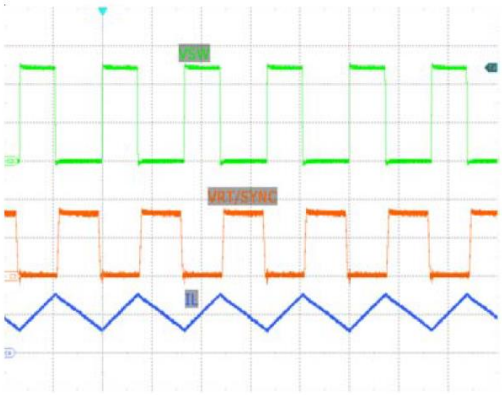


Figure 16. Synchronization Mode in CCM

18.15 Thermal Considerations

In many applications, the RT6360 does not generate much heat due to its high efficiency and the low thermal resistance of its WDFN-10L 4x4 and SOP-8 (Exposed Pad) packages. However, in applications where the RT6360 operates at a high ambient temperature, high input voltage, or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RT6360 stops switching the high-side MOSFET until the temperature cools down by 15°C.

The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition

specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance. Carefully select the freewheel diode to ensure that thermal performance will not be limited by the freewheel diode.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

If the application requires a higher ambient temperature and may exceed the recommended maximum junction temperature of 150°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18.16 Layout Guidelines

When designing the printed circuit board, the following checklist should be used to ensure proper operation of the RT6360:

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place the high-frequency decoupling capacitor C_{IN5} as close to the IC as possible to reduce the loop impedance and minimize switch node ringing.
- Place the bootstrap capacitor, C_{BOOT}, as close to the IC as possible. Route the trace with a width of 20 mils or wider.
- Place multiple vias under the device near VIN and GND, and close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible. Add thermal vias under and near the RT6360 to additional ground planes within the circuit board and on the bottom side.
- The high-frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Place the freewheel diode, D1, and inductor, L1, as close to the IC as possible to reduce the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind the via of the output capacitor.
- Place the feedback components R_{FB1}, R_{FB2}, and C_{FF} near the IC.
- Place the compensation components R_{CP1}, C_{CP1}, and C_{CP2} near the IC.
- The RT/SYNC resistor, $R_{RT/SYNC}$, should be placed as close to the IC as possible because the RT/SYNC pin is sensitive to noise.

Figure 17 and Figure 18 are the RT6360GQW layout examples.

Figure 19 and Figure 20 are the RT6360GSP layout examples.

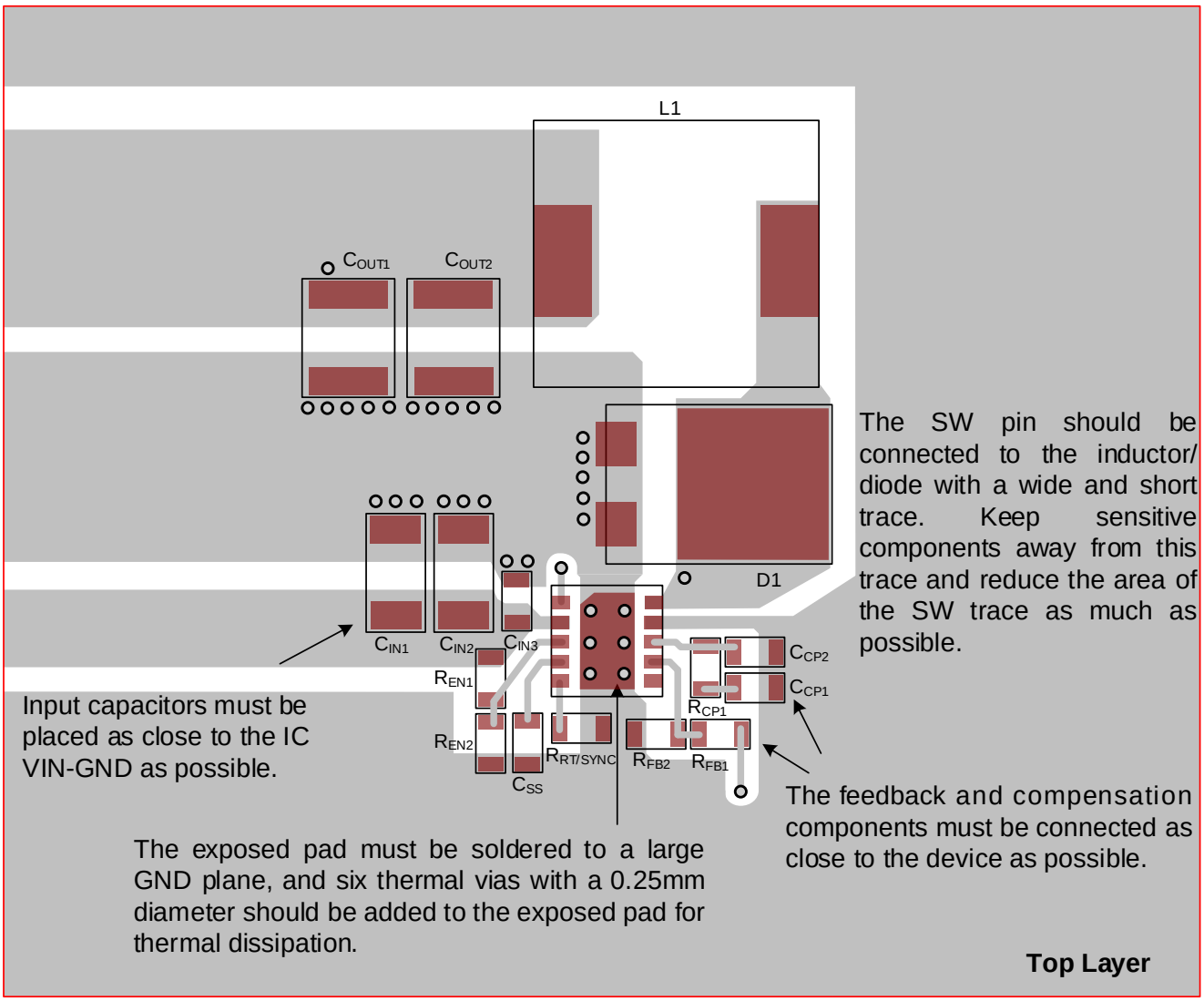


Figure 17. Layout Guide for RT6360GQW (Top Layer)

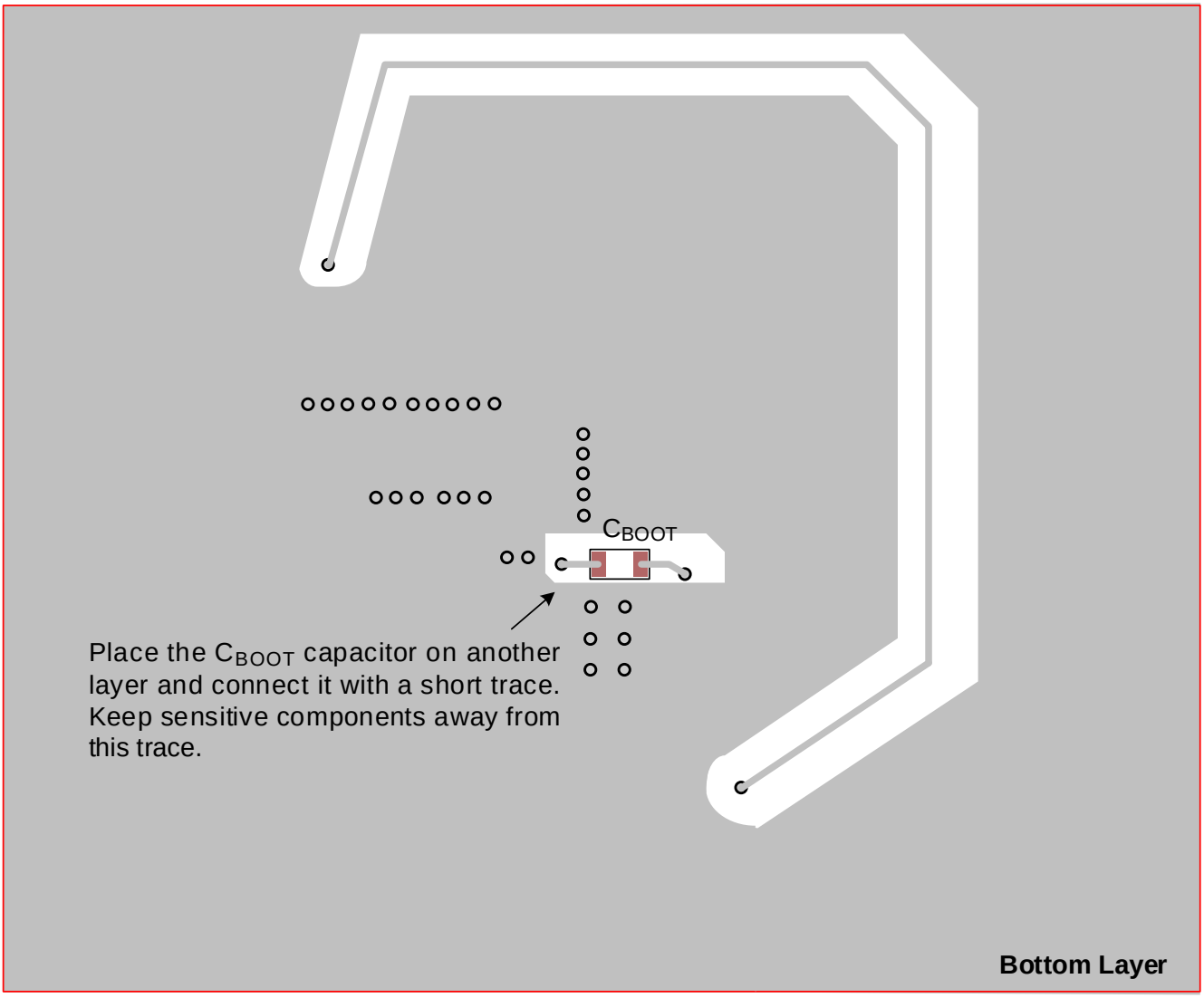


Figure 18. Layout Guide for RT6360GQW (Bottom Layer)

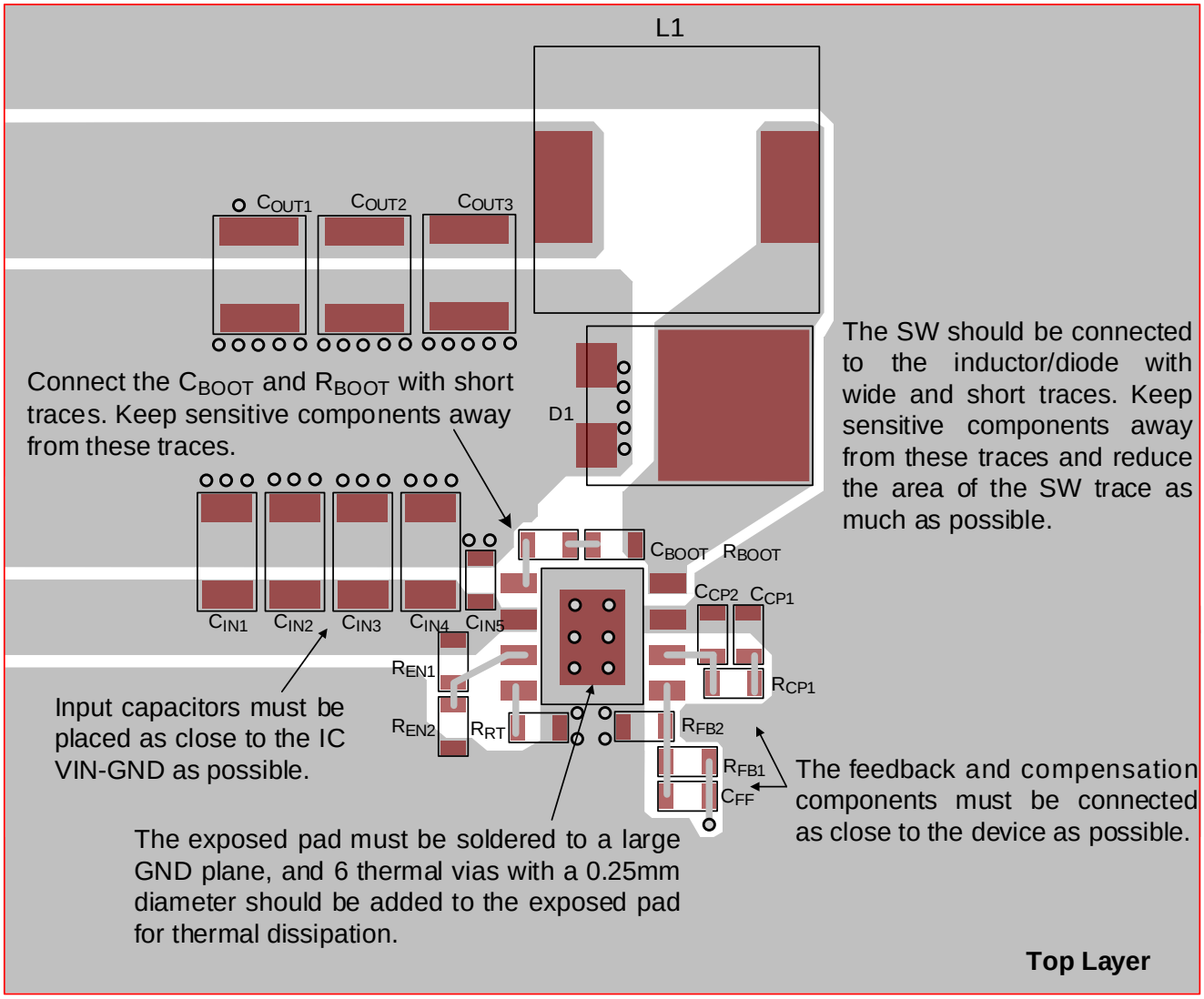


Figure 19. Layout Guide for RT6360GSP (Top Layer)

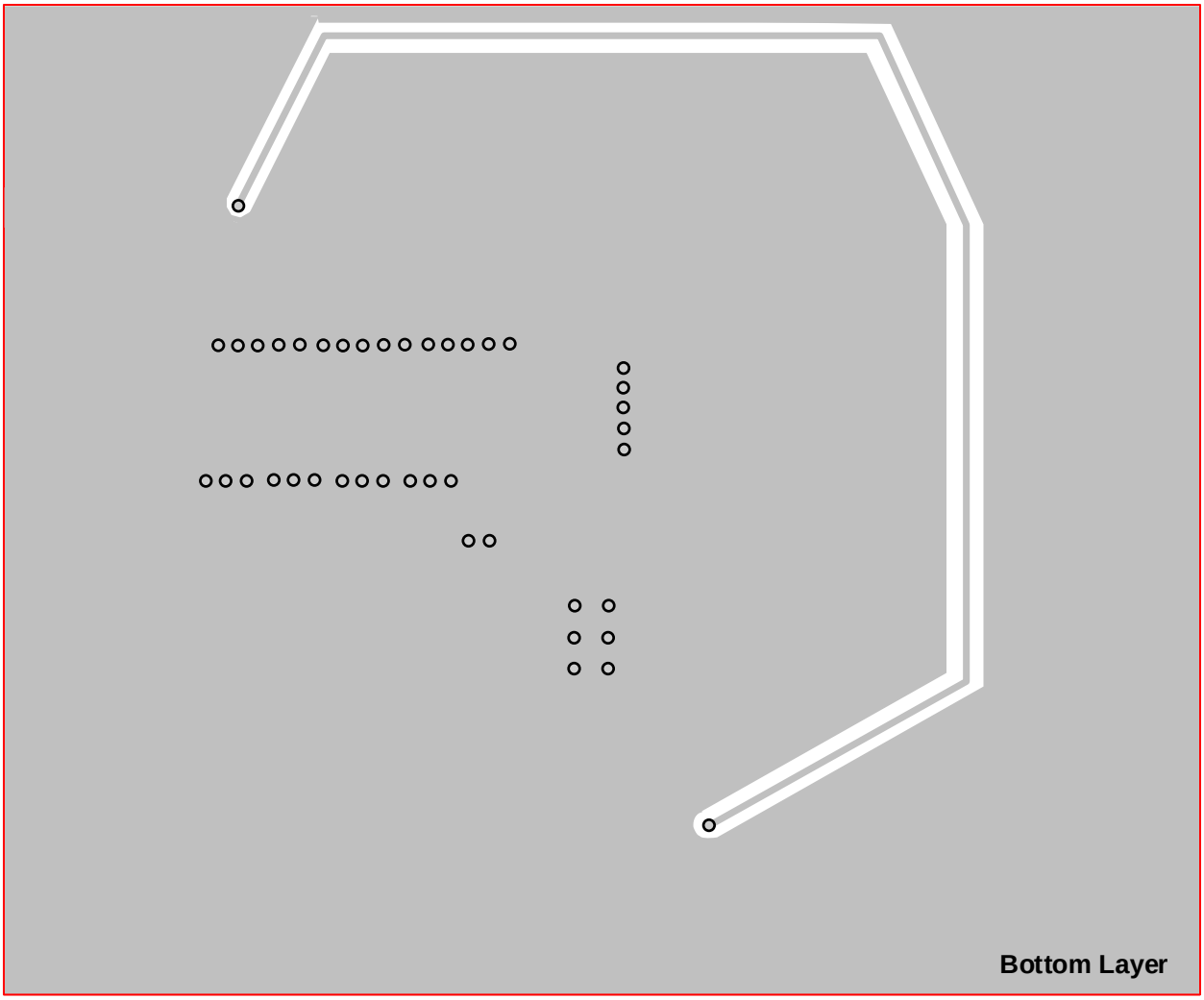
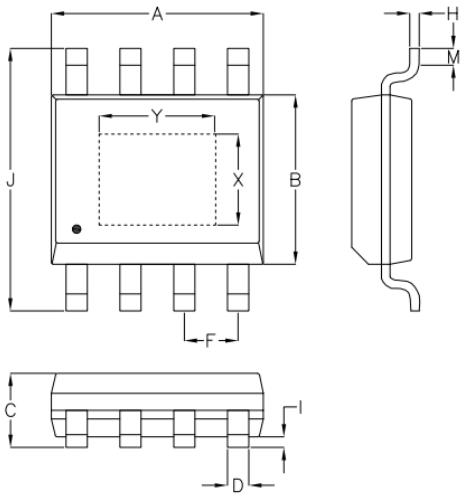


Figure 20. Layout Guide for RT6360GSP (Bottom Layer)

Note 11. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

19.1 SOP-8 (Exposed Pad)

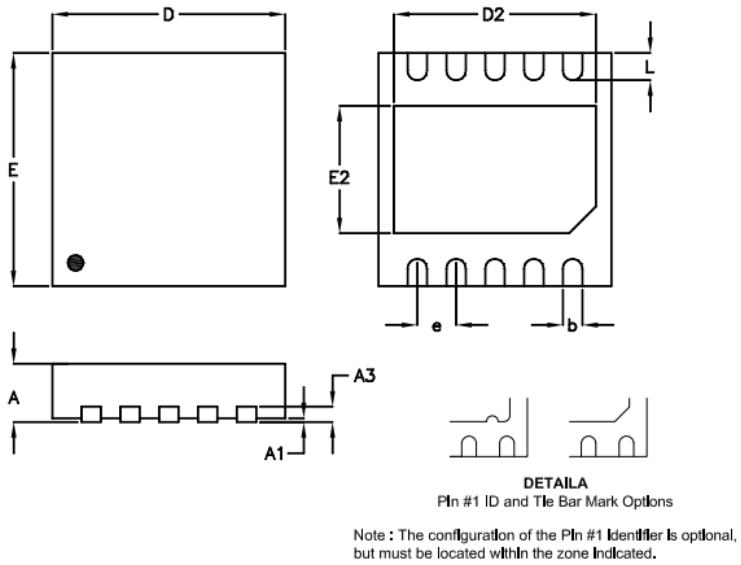


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 12. The package of the RT6360 uses Option 2.

19.2 WDFN-10SL 3x3

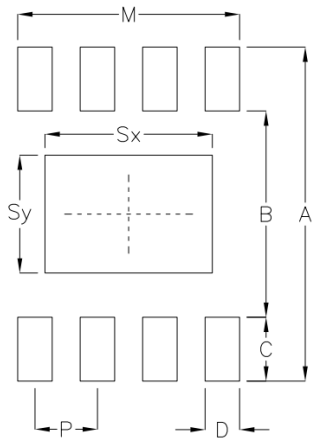


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.900	3.100	0.114	0.122
D2	2.550	2.650	0.100	0.104
E	2.900	3.100	0.114	0.122
E2	1.590	1.690	0.063	0.067
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 10SL DFN 3x3 Package

20 Footprint Information

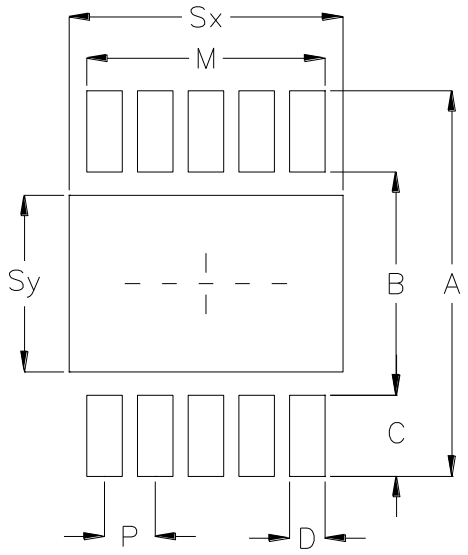
20.1 SOP-8 (Exposed Pad)



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

Note 13. The package of the RT6360 uses Option 2.

20.2 WDFN-10SL 3x3

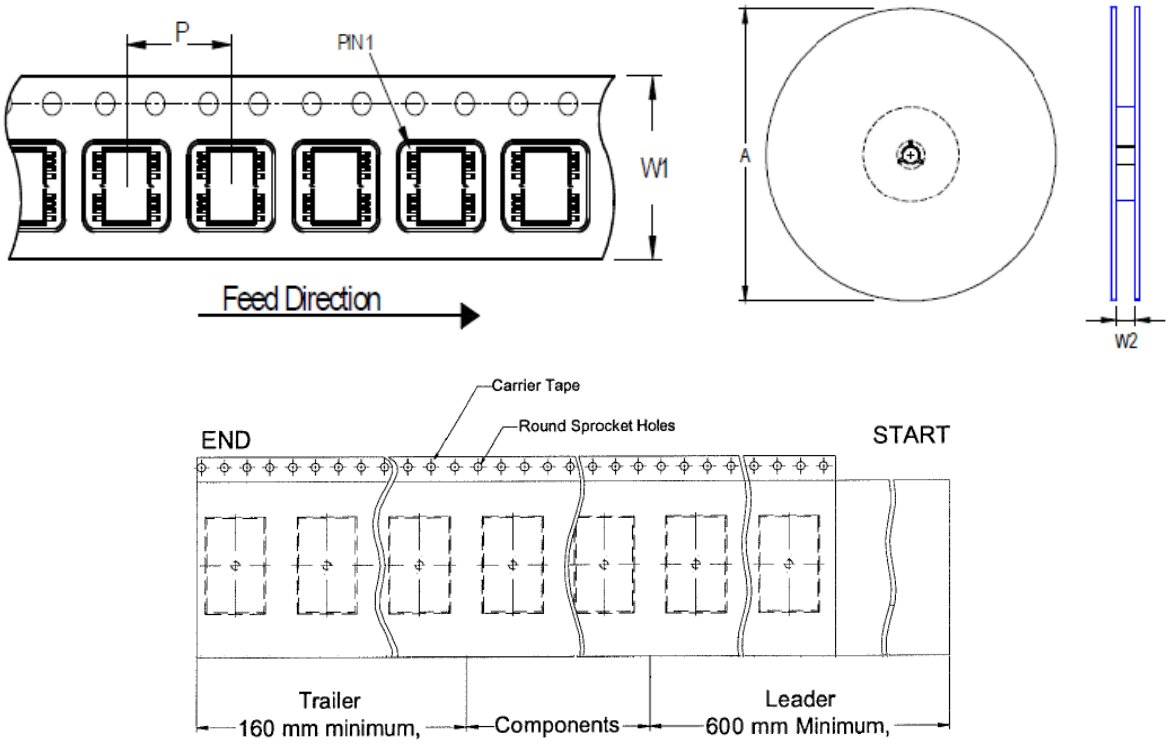


Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN3x3-10S	10	0.50	3.80	2.20	0.80	0.35	2.70	1.74	2.35	±0.05

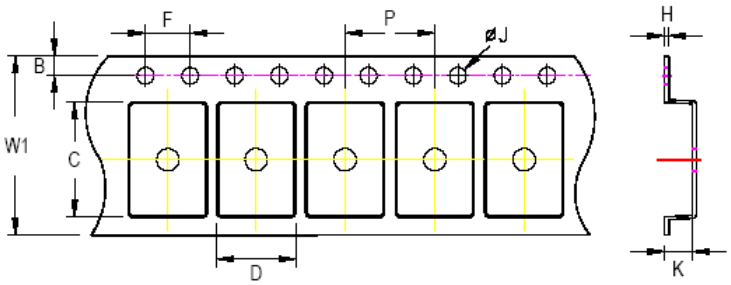
21 Packing Information

21.1 Tape and Reel Data

21.1.1 SOP-8 (Exposed pad)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4

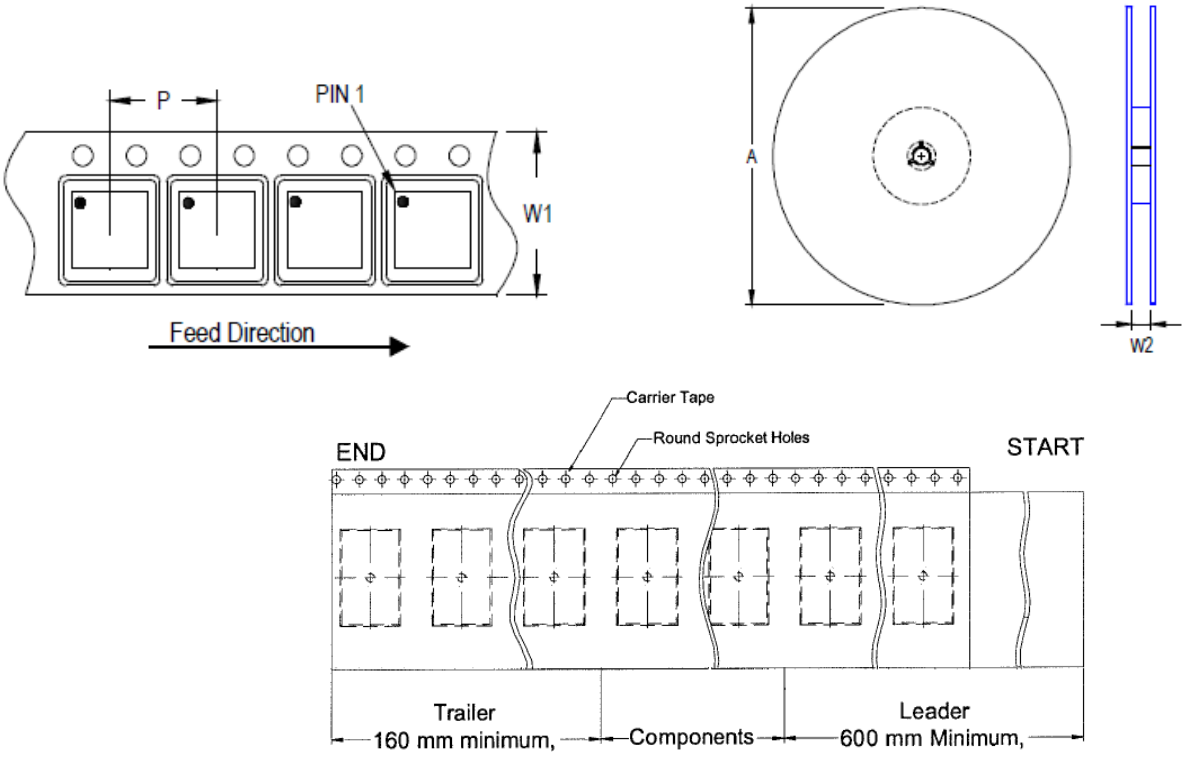


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

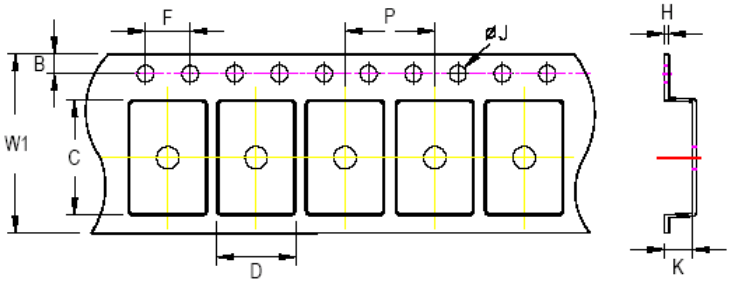
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

21.1.2 WDFN-10SL 3x3



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

21.2 Tape and Reel Packing

21.2.1 SOP-8 (Exposed pad)

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

21.2.2 WDFN-10SL 3x3

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
03	2025/3/4	Modify	*Changed the names PGOOD to PG.* *General Description on page 1* *Ordering Information on page 2* *Functional Pin Description on page 4* *Functional Block Diagram on page 5* *Absolute Maximum Ratings on page 6* *Thermal Information on page 7* *Electrical Characteristics on page 7, 8, 9* *Typical Application Circuit on page 10, 11, 12* *Operation on page 18 to 23* *Application Information on page 24 to 39* *Packing Information on page 44 to 48* - Added packing information