Synchronous DC-DC Step-Down Controller with 5V LDO

General Description

The RT6550A is a step-down, controller generating supply voltages for battery-powered systems. It includes Pulse-Width Modulation (PWM) controller adjustable from 2V to 5.5V, and a 5V linear regulator which provides up to 100mA output current. Other features include on-board power-up sequencing, internal soft-start, and soft-discharge output that prevents negative voltage during shutdown.

A constant current ripple PWM control scheme operates without sense resistors and provides 100ns response to load transient. The RT6550A is available in the WDFN-10L 3x3 package.

Ordering Information

RT6550A□□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

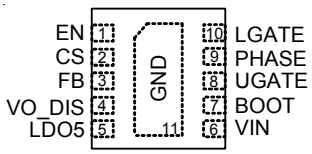
- **Support Connected Shutdown Mode for Ultrabook**
- **CCRCOT Control with 100ns Load Step Response**
- **PWM Maximum Duty Ratio > 98%**
- **5V to 25V Input Voltage Range**
- **2V to 5.5V Output Voltage Range**
- **5V LDO with 100mA Output Current**
- **Internal Frequency Setting with 300kHz @ V_{IN} =12V**
- **Internal Soft-Start and Soft-Discharge**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Independent Switcher Enable Control**
- **Built-In OVP/UVP/OCP/OTP**
- **Non-Latch UVLO**

Applications

- Notebook and Sub-Notebook Computers
- System Power Supplies
- 3-Cell and 4-Cell Li+ Battery-Powered Devices

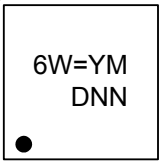
Pin Configuration

(TOP VIEW)



WDFN-10L 3x3

Marking Information



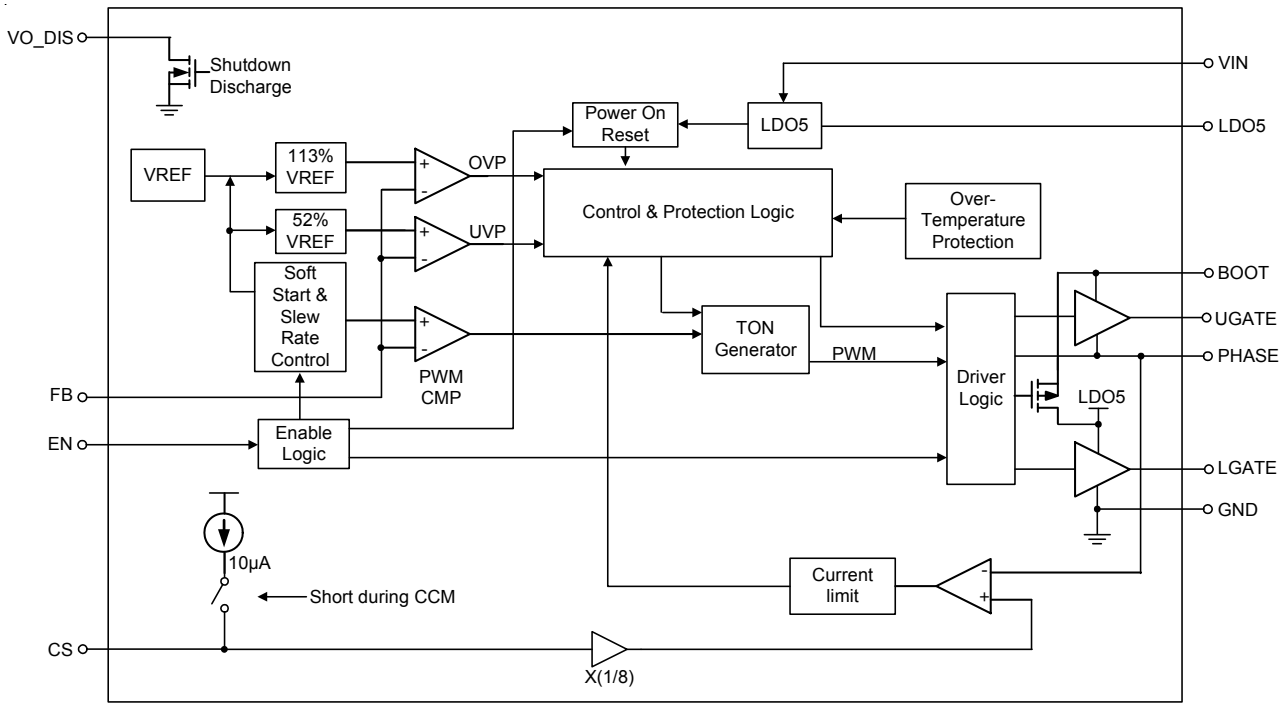
6W= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable control input.
2	CS	Current limit setting. Connect a resistor to GND to set the threshold for synchronous $R_{DS(ON)}$ sense. The GND - PHASE current limit threshold is 1/8th the voltage seen at CS over a 0.2V to 2V range. There is an internal 10μA current source from LDO5 to CS.
3	FB	Feedback voltage input. Connect FB to a resistive voltage divider from VOUT to GND to adjust output from 2V to 5.5V.
4	VO_DIS	Output discharge function.
5	LDO5	5V linear regulator output. LDO5 is also the supply voltage for the low-side MOSFET and analog supply voltage for the device.
6	VIN	Power input for 5V LDO regulator and buck controller.
7	BOOT	Bootstrap supply for high-side gate driver. Connect to an external capacitor according to the typical application circuit.
8	UGATE	High-side gate driver output. UGATE swings between PHASE and BOOT.
9	PHASE	Switch node of MOSFETs. PHASE is the internal lower supply rail for the UGATE high-side gate driver. PHASE is also the current sense input.
10	LGATE	Low-side gate driver output. LGATE swings between GND and LDO5.
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT6550A includes constant on-time synchronou step-down controller and linear regulator.

Buck Controller

In normal operation, the high-side N-MOSFET is turned on when the output is lower than VREF, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

Current Limit

The current limit circuit employs an unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The channel output voltage is continuously monitored for over-voltage and under-voltage conditions. When the output voltage exceeds over-voltage threshold (113% of VOUT), UGATE goes low and LGATE is forced high; when it is less than 52% of reference voltage, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until EN is reset or LDO5 is re-supplied.

LDO5

The LDO5 can be power on by EN. The linear regulator LDO5 provides 5V regulated output.

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- –0.3V to 30V
- BOOT to GND
  - DC ---------- –0.3V to 36V
  - <100ns ---------- –5V to 42V
- BOOT to PHASE
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- PHASE to GND
  - DC ---------- –5V to 30V
  - <100ns ---------- –10V to 42V
- UGATE to GND
  - DC ---------- –5V to 36V
  - <100ns ---------- –10V to 42V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{EN} = 3.3V, V_{CS} = 2V, No Load, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Power On Reset	V_{IN_POR}	Rising Threshold	--	4.6	4.9	V
		Falling Threshold	3.2	3.7	--	
VIN Shutdown Supply Current	I_{VIN_SBY}	Buck Controller Off, V_{EN} = GND	--	20	35	μA
VIN Quiescent Current	I_{VIN}	UGATE / LGATE Floating, V_{IN} = 12V, No Switching	--	420	750	μA
Buck Controllers Output and FB Voltage						
FB Valley Trip Voltage	V_{FB}	CCM Operation	1.98	2	2.02	V
VO_DIS Discharge Current	I_{DCHG}	V_{VO_DIS} = 0.5V	10	45	--	mA
PHASE Discharge Current	I_{DCHG_LX}	V_{PHASE} = 0.5V	5	8	--	mA
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 5V	240	300	360	kHz
Minimum Off-Time	$t_{OFF(MIN)}$	V_{FB} = 1.9V	--	200	275	ns
Soft-Start						
Soft-Start Time	t_{SS}	V_{OUT} Ramp-up Time	--	0.9	--	ms
Current Sense						
CS Source Current	I_{CS}	V_{CS} = 1V	9	10	11	μA
CS Current Temperature Coefficient	TCI_{CS}	In Comparison with 25°C	--	4700	--	ppm/°C
Internal Regulator						
LDO5 Output Voltage	V_{LDO5}	V_{IN} = 12V, No Load	4.9	5	5.1	V
		V_{IN} > 7V, I_{LDO5} < 100mA	4.8	5	5.1	
		V_{IN} > 5.5V, I_{LDO5} < 35mA	4.8	5	5.1	
		V_{IN} > 5V, I_{LDO5} < 20mA	4.5	4.75	5.1	
LDO5 Output Current	I_{LDO5}	V_{LDO5} = 4.5V, V_{IN} = 7.4V	100	175	--	mA
UVLO						
LDO5 UVLO Threshold	V_{UVLO5}	Rising Edge	--	4.3	4.6	V
		Falling Edge	3.7	3.9	4.1	
Fault Detection						
OVP Trip Threshold	V_{OVP}	FB with Respect to Internal Reference	109	113	117	%
OVP Propagation Delay			--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP Detect, FB Falling Edge	47	52	57	%
UVP Shutdown Blanking Time	t_{SHDN_UVP}	From EN Enable	--	1.3	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
Thermal Shutdown	T_{SD}		--	150	--	°C
Logic Inputs						
EN Threshold Voltage	V_{EN_H}	SMPS On	1.6	--	--	V
	V_{EN_L}	SMPS Off	--	--	0.4	
Internal Boost Switch						
Internal Boost Switch On-Resistance	R_{BOOST}	LDO5 to BOOT	--	80	--	Ω
Power MOSFET Drivers						
UGATE On-Resistance	R_{UGATE}	High State, $V_{BOOT} - V_{UGATE}$ = 0.25V, $V_{BOOT} - V_{PHASE}$ = 5V	--	3	--	Ω
		Low State, $V_{UGATE} - V_{PAHSE}$ = 0.25V, $V_{BOOT} - V_{PHASE}$ = 5V	--	2	--	
LGATE On-Resistance	R_{LGATE}	High State, $V_{LDO5} - V_{LGATE}$ = 0.25V, V_{LDO5} = 5V	--	3	--	Ω
		Low State, V_{LGATE} – GND = 0.25V	--	1	--	
Dead-Time	t_D	LGATE Rising	--	20	--	ns
		UGATE Rising	--	30	--	

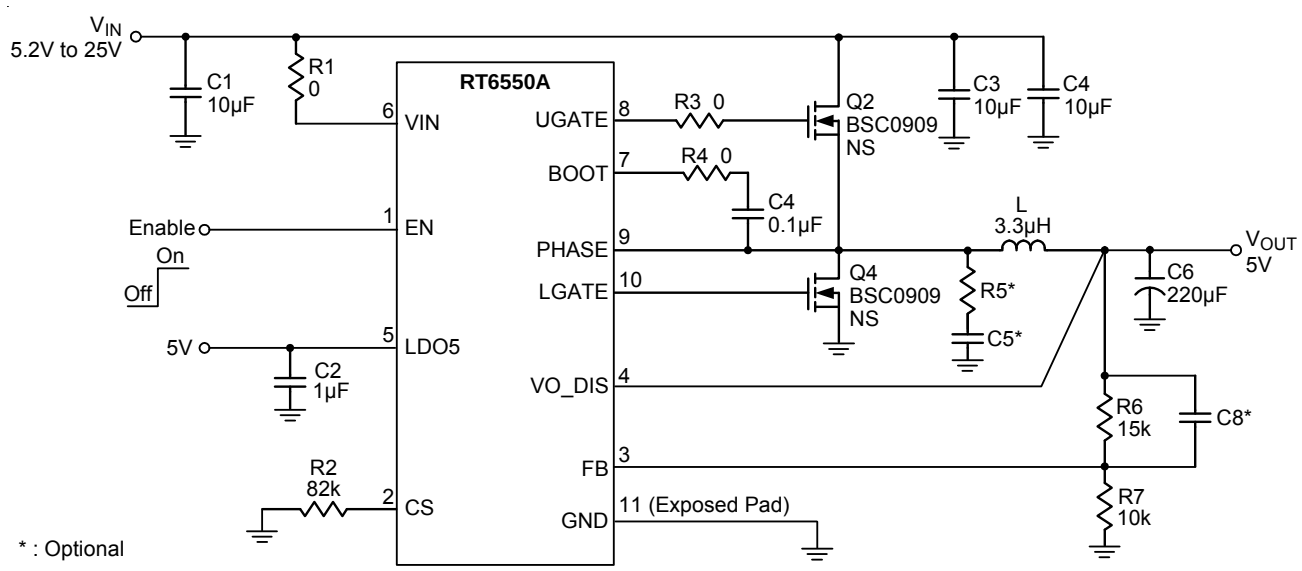
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

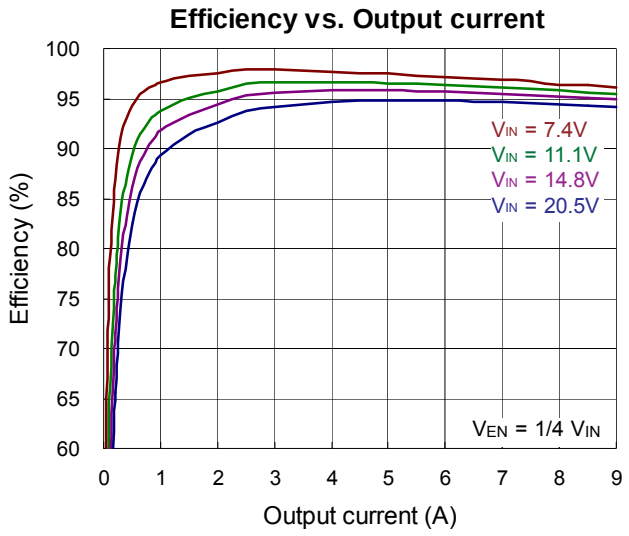
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

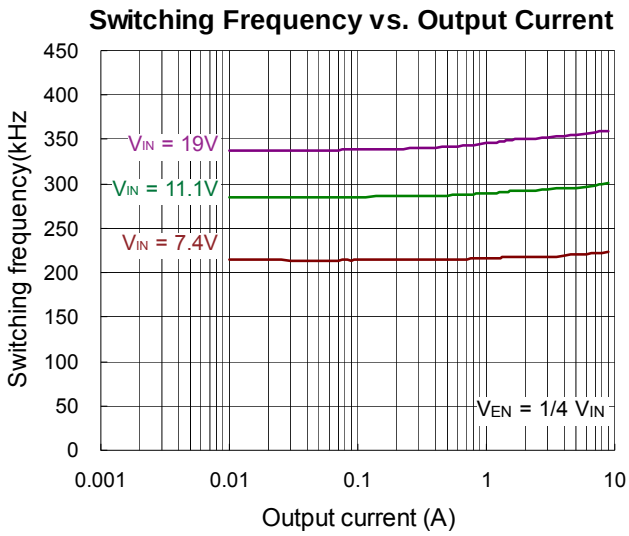
Note 4. The device is not guaranteed to function outside its operating conditions.

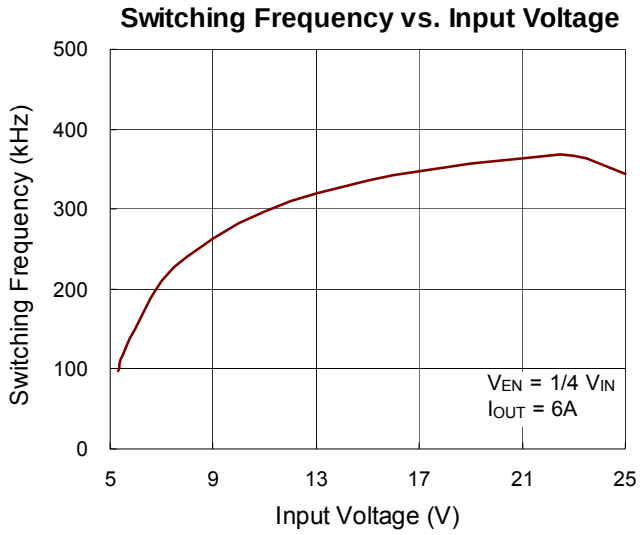
Typical Application Circuit

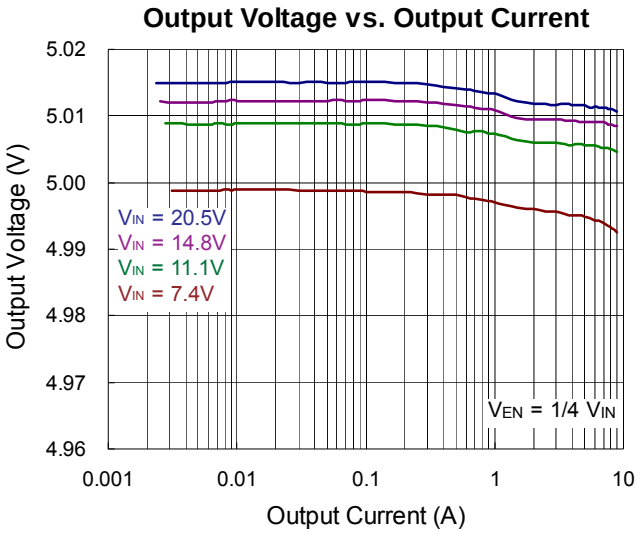


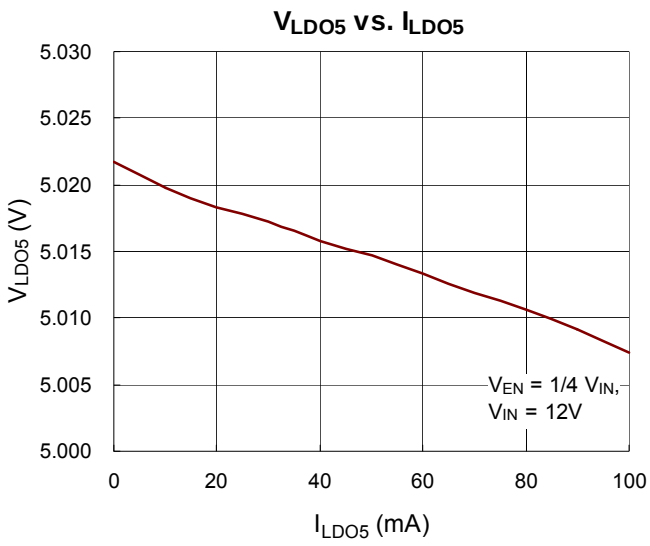
Typical Operating Characteristics

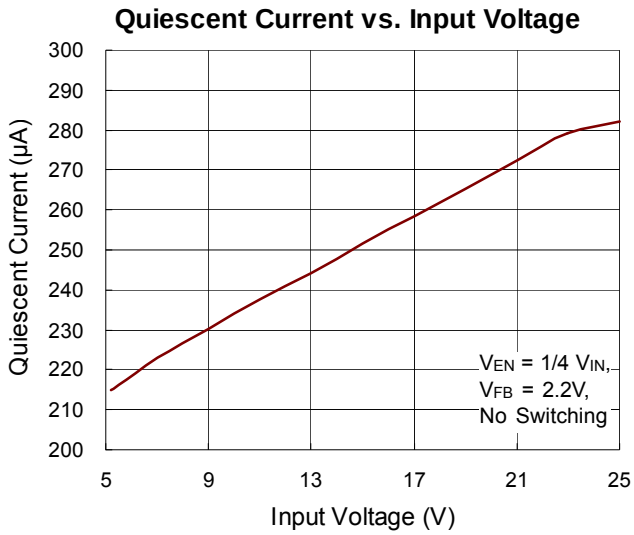




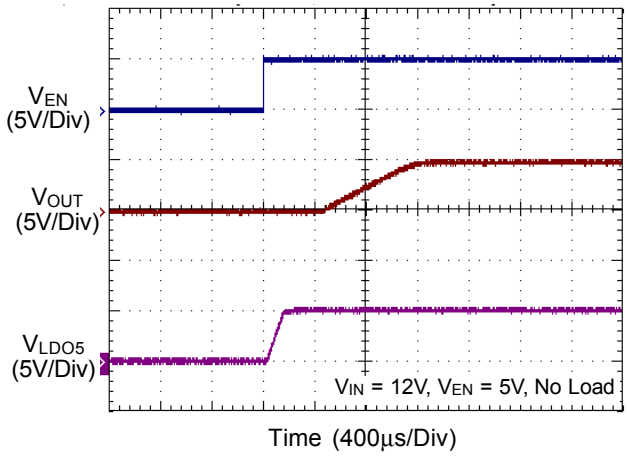




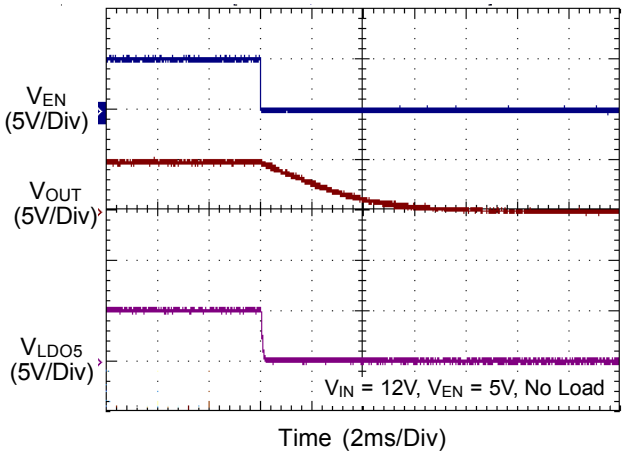




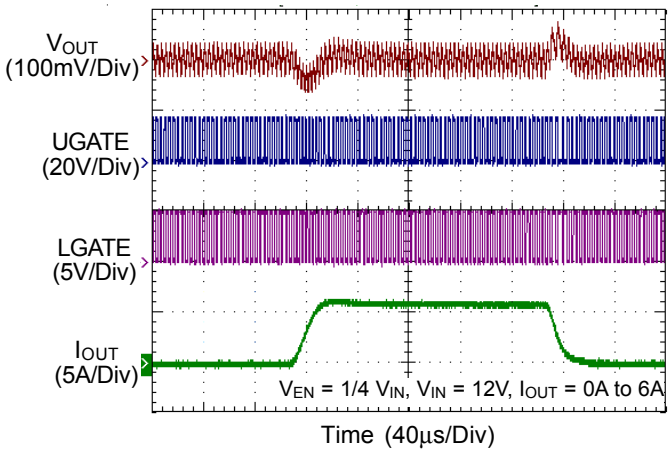
Power On from EN



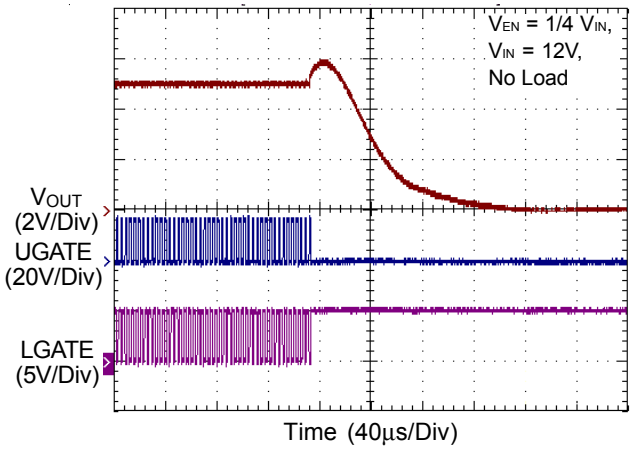
Power Off from EN



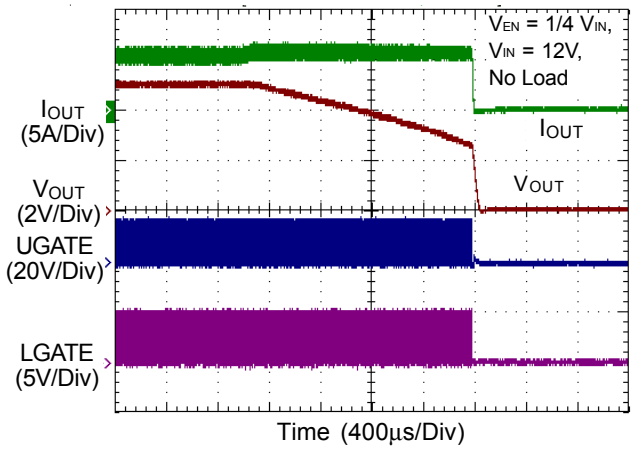
Load Transient Response



OVP



UVP



Application Information

The RT6550A is a low quiescent, Mach Response™ DRV™ mode synchronous Buck controller targeted for Ultrabook system power supply solutions. Richtek's Mach Response™ technology provides fast response to load steps. The topology solves the poor load transient response timing problems of fixed frequency current mode PWMs, and avoids the problems caused by widely varying switching frequencies in CCR (constant current ripple) constant on-time PWM schemes. A special adaptive on-time control trades off the performance and efficiency over wide input voltage range. The RT6550A includes 5V (LDO5) linear regulators. The LDO5 linear regulator steps down the battery voltage to supply internal circuitry and gate drivers. The synchronous switch gate drivers are directly powered by LDO5.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so that the output ripple voltage provides the PWM ramp signal. Referring to the RT6550A's Function Block Diagram, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (200ns typ.). The on-time one-shot will be triggered if the error comparator is high, the low-side switch current is below the current limit threshold, and the minimum off-time one-shot has timed out.

PWM Frequency and On-time Control

For each specific input voltage range, the Mach Response™ control architecture runs with pseudo constant frequency by feed forwarding the input and output voltage into the on-time one-shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by V_{IN} and proportional to the output voltage. The inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

The RT6550A adaptively changes the operation frequency according to the input voltage. Higher input voltage usually comes from an external adapter, so the RT6550A operates with higher frequency to have better performance. Lower input voltage usually comes from a battery, so the RT6550A operates with lower switching frequency for lower switching losses. For a specific input voltage range, the switching cycle period is given by :

For 5V VOUT,

$$\text{Period (usec.)} = \frac{V_{IN} \times 2.025}{V_{IN} - 3.79}$$

where the VIN is in volt.

The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high-side power MOSFET.

Forced-CCM Mode

The low noise, forced-CCM mode disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate-drive waveform to become the complement of the high side gate-drive waveform. This in turn causes the inductor current to reverse at ligt loads as the PWM loop to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost : The no-load battery current can be up to 10mA, depending on the external MOSFETs.

Linear Regulators (LDO5)

The RT6550A includes 5V (LDO5) linear regulators. The regulator can supply up to 100mA for external loads. Bypass LDO with 1μF (min) to 4.7μF (max), and the recommended value is 1μF ceramic capacitor.

Current Limit Setting

The RT6550A has cycle-by-cycle current limit control and the OCP function only operation at CCM , it is disabled at FCCM in order to reduce quiescent current. The current limit circuit employs an unique "valley" current sensing algorithm. If the magnitude of the current sense signal at

PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

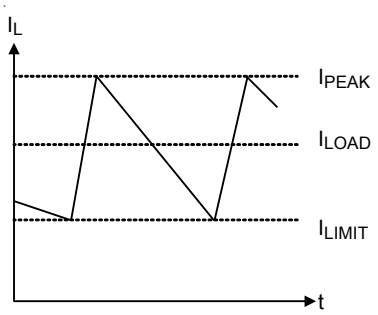


Figure 2. "Valley" Current Limit

The RT6550A uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIM} resistor between the CS pin and GND sets the current limit threshold. The resistor R_{ILIM} is connected to a current source from CS which is 10μA (typ.) at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low-side MOSFET equals 1/8 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high-side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/8 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor according to the following equation :

$V_{LIMIT} = (R_{LIMIT} \times 10\mu A) / 8 = I_{LIMIT} \times R_{DS(ON)}$

$R_{LIMIT} = (I_{LIMIT} \times R_{DS(ON)}) \times 8 / 10\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASE and GND. Mount or place the IC close to the low-side MOSFET.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between the BOOT and PHASE pins. A dead-time to prevent shoot through is internally generated from high-side MOSFET off to low-side MOSFET on and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATE low is robust, with a 1Ω typical on-resistance. A 5V bias voltage is delivered from the LDO5 supply. The instantaneous drive current is supplied by an input capacitor connected between LDO5 and GND.

For high current applications, some combinations of high and low-side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing, and shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time. See Figure 3.

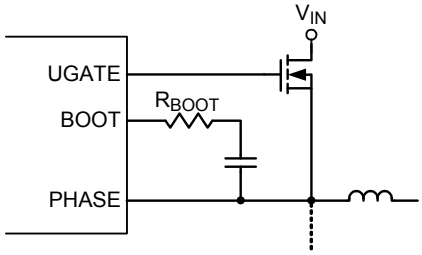


Figure 3. Increasing the UGATE Rise Time

Soft-Start

The RT6550A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 0.9ms. An unique PWM duty limit control that prevents output over-voltage during soft-start period is designed specifically for FB floating.

UVLO Protection

The RT6550A has LDO5 under-voltage lock out protection (UVLO). When the LDO5 voltage is lower than 3.9V (typ.), both switch power supply is shut off. This is a non-latch protection.

Output Over-Voltage Protection (OVP)

The output voltage can be continuously monitored for over-voltage condition. If the output voltage exceeds 13% of its set voltage threshold, the over-voltage protection is triggered and the LGATE low-side gate drivers is forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and pulls the output voltage downward.

The RT6550A is latched once OVP is triggered and can only be released by either toggling EN or cycling VIN. There is a 1μs delay built into the over-voltage protection circuit to prevent false transition.

Note that latching LGATE high will cause the output voltage to dip slightly negative due to previously stored energy in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over-voltage condition is caused by a shorted in high-side switch, turning the low-side MOSFET on 100% will create an electrical shorted circuit between the battery and GND to blow the fuse and disconnecting the battery from the output.

Output Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under-voltage condition. If the output is less than 52% (typ.) of its set voltage threshold, the under-voltage protection will be triggered and then both UGATE and LGATE gate drivers will be forced low. The UVP is ignored for at least 1.3ms (typ.) after a start-up or a rising edge on EN. Toggle EN or cycle VIN to reset the UVP fault latch and restart the controller.

Thermal Protection

The RT6550A features thermal shutdown to prevent damage from excessive heat dissipation. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitries are turned off during thermal shutdown. The RT6550A triggers thermal shutdown while input voltage on VIN and drawing current from LDO5 are too high.

Discharge Mode (Soft Discharge)

When EN is low the output under-voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

Shutdown Mode

When VIN exceeds POR threshold and EN < 0.4V, the RT6550A operate in shutdown mode, and PWM contoller is OFF state. For the RT6550A, LDO5 is OFF and approximately consumes 17μA of input current.

Power-Up Sequencing and On/Off Controls (EN)

EN controls the power-up sequencing of the Buck converter. The 0.4V falling edge threshold on EN can be used to detect a specific analog voltage level and to shutdown the device. Once in shutdown, the 1.6V rising edge threshold activates, providing sufficient hysteresis for most applications.

Table 1. Operation Mode Truth Table

Mode	Condition	Comment
LDO Over Current Limit	LDO < UVLO threshold	Transitions to discharge mode after VIN POR. LDO5 remains active.
Run	EN = high, V_{OUT} is enabled	Normal Operation.
Over-Voltage Protection	Either output >113% of the nominal level.	LGATE is forced high. LDO5 is active. Exit by VIN POR or by toggling EN.
Under-Voltage Protection	Either output < 52% of the nominal level after 1.3ms time-out expires and output is enabled	Both UGATE and LGATE are forced low and enter discharge mode. LDO5 is active. Exit by VIN POR or by toggling EN.
Discharge	Either output is still high in shutdown mode	During discharge mode, there is one path to discharge the output capacitors' residual charge to GND via an internal switch.
Shutdown	VIN > POR, VEN < 0.4V	LDO5 and VO_DIS discharge
Thermal Shutdown	T_J > 150°C	All circuitries are off. Exit by VIN POR.

Table 2. Enabling State (RT6550A)

EN	LDO5	PWM Controller (5VOUT)
OFF	OFF	OFF
ON	ON	ON

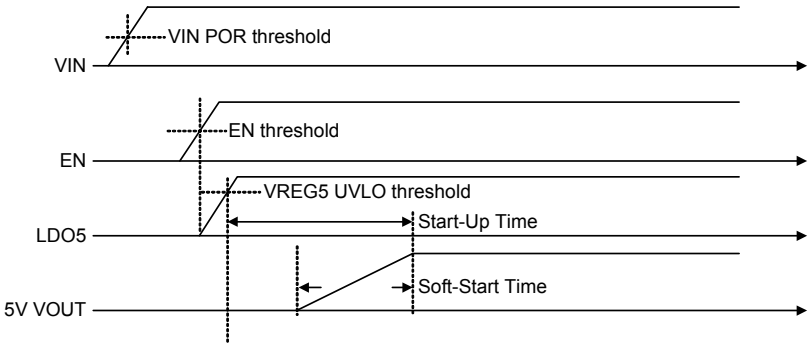


Figure 4. Timing

Output Voltage Setting (FB)

Connect a resistive voltage divider at the FB pin between V_{OUT} and GND to adjust the output voltage between 2V and 5.5V (Figure 5). The recommended R2 is between 10kΩ to 20kΩ, and solve for R1 using the equation below:

$$V_{OUT\ (valley)} = V_{FB} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$

where V_{FB} is 2V (typ.).

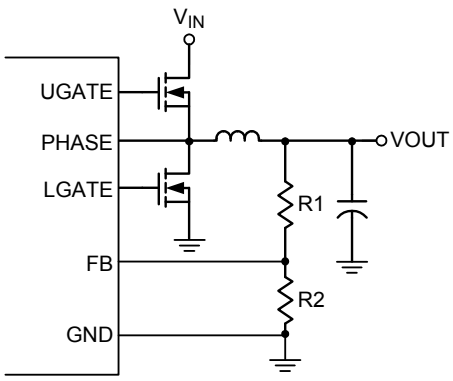


Figure 5. Setting V_{OUT} with a resistive voltage divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK} :

$I_{PEAK} = I_{LOAD(MAX)} + [(LIR / 2) \times I_{LOAD(MAX)}]$

The calculation above shall serve as a general reference. To further improve transient response, the output inductance can be further reduced. Of course, besides the inductor, the output capacitor should also be considered when improving transient response.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from the equations below :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUTx} (t_{ON} + t_{OFF(MIN)}) \right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f} \right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot and overshoot voltage during load transient, V_{p-p} is the output ripple voltage, and $t_{OFF(MIN)}$ is the minimum off-time.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.27W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

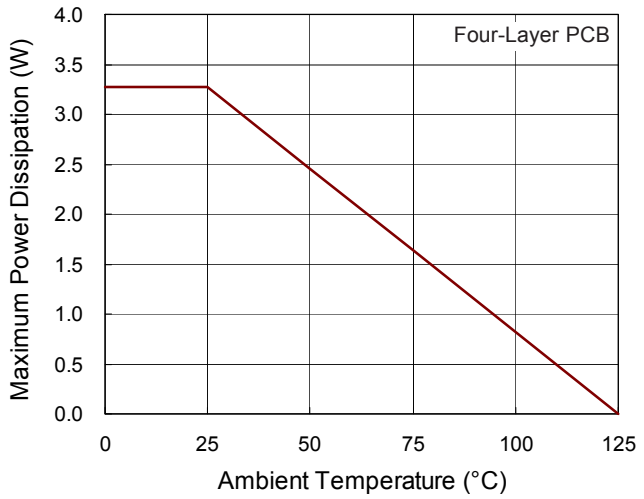


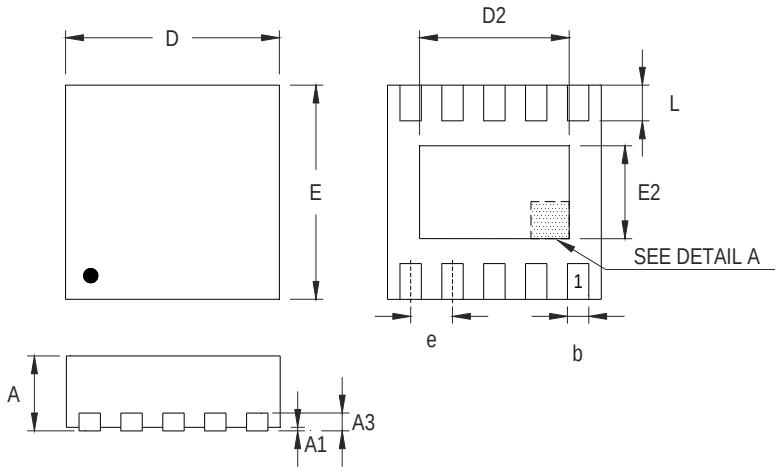
Figure 6. Derating Curve of Maximum Power Dissipation

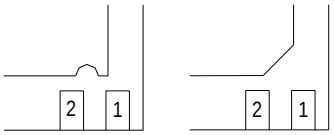
Layout Considerations

Layout is very important in high frequency switching converter design. Improper PCB layout can radiate excessive noise and contribute to the converter's instability. Certain points must be considered before starting a layout with the RT6550A.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as FB, PGOOD, and should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place ground terminal of VIN capacitor(s), V_{OUT} capacitor(s), and Source of low-side MOSFETs as close to each other as possible. The PCB trace of PHASE node, which connects to Source of high-side MOSFET, Drain of low-side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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