Highly-Integrated USB Type-C Power Delivery Controller with Built-In Blocking N-MOSFET

General Description

The RT7206KNx series is a USB Type-C Power Delivery (PD) controller, that mainly utilized in the secondary side for off-line AC-DC power converters. Through the high integration of control regulators and built-in blocking N-MOSFET, more compact designs are easily implemented. The embedded MCU solution and Bi-phase Mark Coding (BMC) Transmitter are incorporated to handle PD Protocol. Furthermore, the digital-to-analog (DAC) and analog-to-digital (ADC) converters are introduced to achieve high-precision control in various applications.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

Ordering Information

RT7206KN □□□-□

- □ (last): Programmed Firmware Code AABBX
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- □ (third): Package Type
  - S : SOP-8
- □ (second): Lead Plating System
  - G : Richtek Green Policy Compliant
- □ (first): RT7206KN Version
  - (Refer to Version Table)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

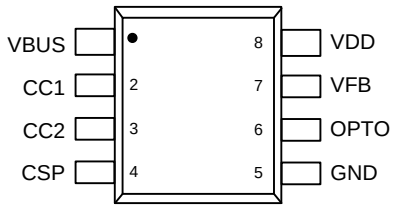
- **Protocol Support**
  - **USB PD3.0 and PPS**
- **High Integration**
  - **Wide Operating Range from 3.3V to 21V**
  - **Built-In Shunt Regulator for Constant-Voltage and Constant-Current Regulations**
  - **Built-In Blocking N-MOSFET**
  - **Built-In Quick Discharge in VDD and VBUS**
  - **Built-In VCONN Power and Switch**
  - **Linear Cable Compensation**
  - **Power-Saving Mode Supported**
  - **Embedded MCU with 16kB OTP-ROM**
  - **Embedded BMC Transmitter**
- **Protection**
  - **VDD Adaptive Over-Voltage Protection (OVP)**
  - **VDD Adaptive Under-Voltage Protection (UVP)**
  - **VBUS Short-Circuit Protection (SCP)**
  - **CC1/CC2 Over-Voltage Protection (IO OVP)**
  - **Over-Current Protection (OCP)**
  - **Over-Temperature Protection (OTP)**

Applications

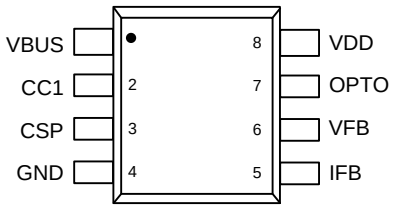
- USB Type-C PD Controller in Source Application for Chargers/Adapters of Smartphone, Tablet, Notebook, and Other Electronics
- USB Type-C PD Controller in Sink Application for IoT Devices of Power Over Ethernet, Smart Speaker, Projector, and Other Electronics

Pin Configuration

(TOP VIEW)



SOP-8 (RT7206KN)

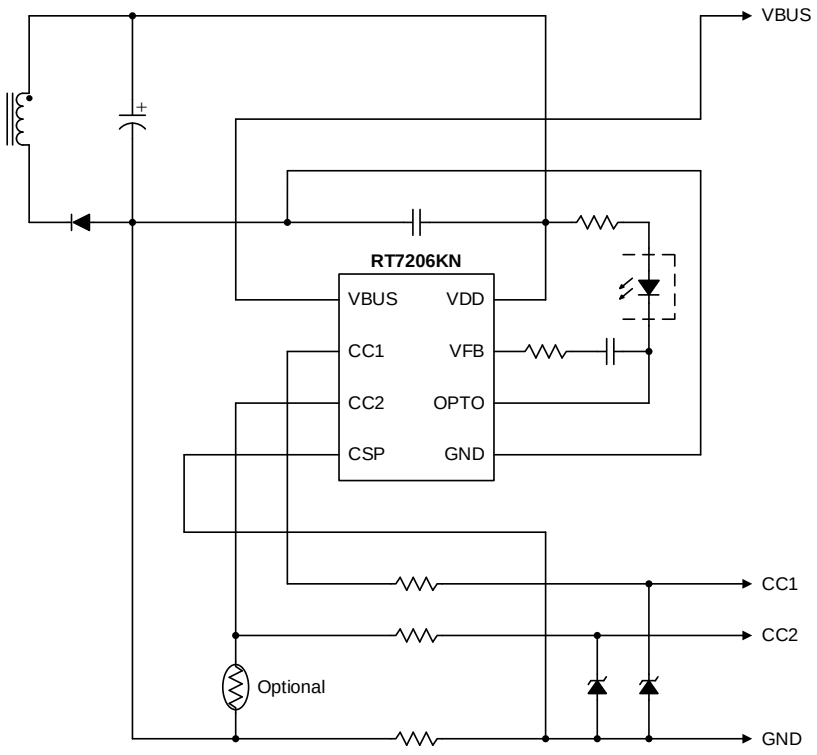


SOP-8 (RT7206KNC)

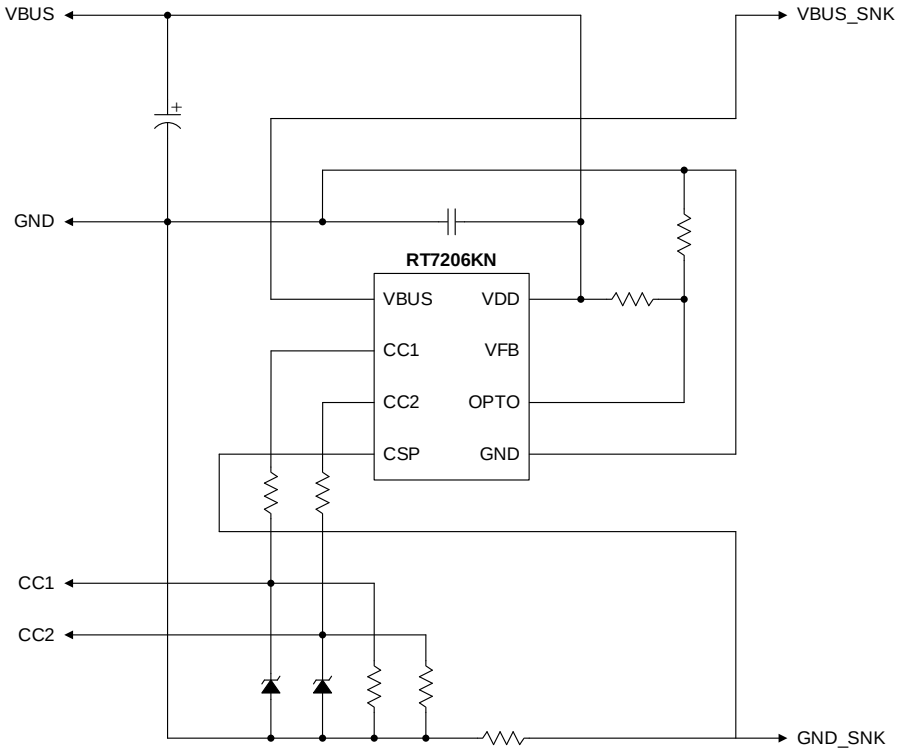
RT7206KN Version Table

Version	RT7206KN	RT7206KNC
Operating Range	3.3V to 21V	3.3V to 21V
CC1/CC2 Configuration	O	CC1 Only
Constant-Current Regulation	X	O
Package Type	SOP-8	SOP-8

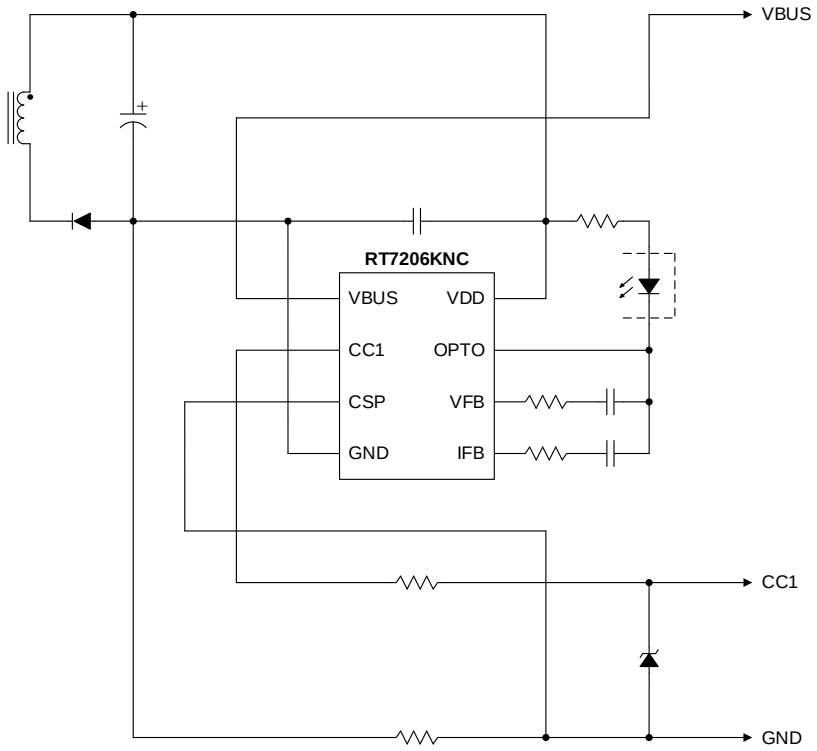
Simplified Application Circuit



RT7206KN Simplified Circuit for Source Application



RT7206KN Simplified Circuit for Sink Application



RT7206KNC Simplified Circuit for Source Application

Functional Pin Description

RT7206KN

Pin No.	Pin Name	Type	Pin Function
1	VBUS	PWR	Source terminal of blocking N-MOSFET
2	CC1	A/D IO	Type-C connector Configuration Channel 1, used to detect cable-plug event, determine the cable orientation, and supply VCONN power
3	CC2	A/D IO	Type-C connector Configuration Channel 2, used to detect cable-plug event, determine the cable orientation, and supply VCONN power
4	CSP	A I	Positive input of current-sense amplifier for sensing output current
5	GND	GND	Ground
6	OPTO	A/D IO	Current-sink output connected to optocoupler
7	VFB	A I	Feedback input for constant-voltage loop
8	VDD	PWR	Supply input voltage and Drain terminal of blocking N-MOSFET

RT7206KNC

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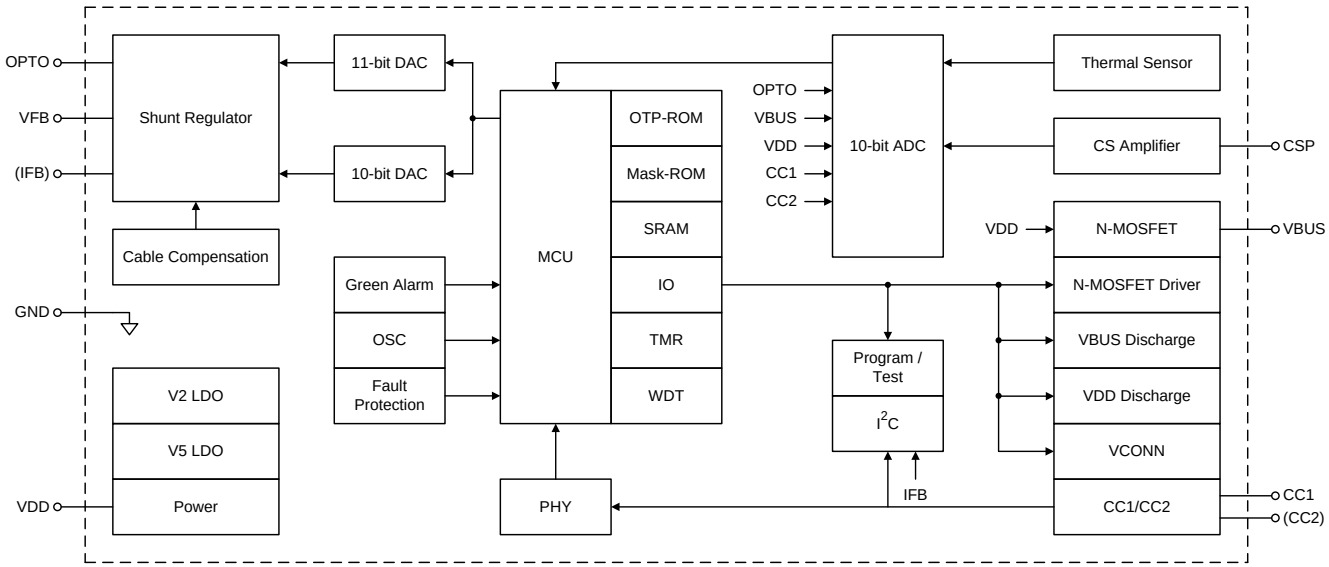
Functional Block Diagram



Operation

Constant-Voltage (CV) and Constant-Current (CC) Regulators in Source Application

The RT7206KNx series integrates a shunt regulator for CV and CC regulations. Both outputs of CV and CC regulators are connected to OPTO in parallel as the analog output. The operation of each feedback loop is similar to that of TL431-based regulator. However, the wider operating range of OPTO, from 0.3V to 25V, improves the design of power converters with a wider output range. If the voltage related to VDD, V_{DD}, is still below the turn-on threshold, V_{VDD_ON}, OPTO will keep in high impedance to ensure a soft start-up sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, are analog outputs from the embedded DACs which provide 10mV-resolution and 10mA-resolution for each CV and CC regulations.

Capability Selector in Sink Application

When the RT7206KNx series is utilized in a Sink port, OPTO will always keep in high impedance. The embedded ADC resolves the voltage related to OPTO, V_{OPTO}, as the analog input. According to the voltage level of V_{OPTO}, the RT7206KNx series, will send the request to a Source port to get the correspond capabilities.

Current-Sense Amplifier

The current in the power-ground bus can be sensed by an external current-sense resistor, R_{CS}. In order to minimize the power loss of R_{CS} and the noise, a differential amplifier with output gain, K_{CS}, and output offset, V_{CS_OFFSET}, is integrated.

CC1/CC2 Interface

The specific I/O pins, CC1/CC2, are integrated to handle USB Type-C compliance and PD protocol. When the RT7206KNx series configured as a Source device, the optional current capabilities of 80μA, 180μA, and 330μA, provided by each of CC1 and CC2, will be advertised to a Sink device, implying the USB Type-C current of default, 1.5A, and 3.0A respectively.

Absolute Maximum Ratings (Note 1)

- VDD, VBUS, OPTO to GND ---------- –0.3V to 28V
- VFB, IFB, CC1, CC2, CSP to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOP-8, θ_{JA} ---------- 261.1°C/W
  SOP-8, θ_{JC} ---------- 47°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{DD} ---------- 3.3V to 21V
- Supply Input Current, I_{DD} (Based on T_J < 125°C) ---------- 0A to 4A
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Start-Up Current	I_{VDD_START}	V_{DD} = 2.8V	50	100	150	µA
VDD Nominal Current	I_{VDD_NOM}	V_{DD} = 5V	3	4	5	mA
VDD Idle-Mode Current	I_{VDD_IDLE}	V_{DD} = 5V	1	1.5	2	mA
VDD Green-Mode Current	I_{VDD_GREEN}	V_{DD} = 5V	500	650	800	µA
VDD Maximum Over-Voltage Protection Threshold	V_{VDD_MAXOVP}		23	24	25	V
VDD Adaptive Over-Voltage Protection Threshold	V_{VDD_OVP}	(Enable/Disable) (Note 6)	105	110	115	%
			110	115	120	
			115	120	125	
VDD Over-Voltage Protection Deglitch	t_{VDD_OVP}	(Note 5)	25	30	35	µs
VDD Adaptive Under-Voltage Protection Threshold	V_{VDD_UVP}	(Enable/Disable) (Note 6)	80	85	90	%
			85	90	95	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Under-Voltage Protection Deglitch	t_{VDD_UVP}	(Note 5)	30	50	70	μs
VDD Threshold for CC1/CC2 Over-Voltage Protection	V_{VDD_IOOVP}		5.75	6	6.25	V
VDD Constant-Discharge Current	I_{DIS_VDD}	V_{DD} > 3.3V (Note 6)	63	90	117	mA
			84	120	156	
			120	150	180	
			150	180	210	
VFB/IFB/OPTO Regulator Section						
VFB Resistor Divider for Voltage Feedback	R_{VFB}	R_{VFB} = R_{VFB1} + R_{VFB2} R_{VFB1} : VDD to VFB R_{VFB2} : VFB to GND	294	420	546	kΩ
VFB Resistor Divider Scaling Factor for Voltage Feedback	K_{VFB}		9.9	10	10.1	--
Standby Reference Voltage for CV Regulator	$V_{REF\_CV\_ST}$		0.485	0.5	0.515	V
Typical Reference Voltage from DAC for CV Regulator	V_{REF_CV}		0.152	--	2.2	V
Typical Reference Voltage from DAC for CC Regulator	V_{REF_CC}	V_{DD} > 3.3V	0	--	1.5	V
Ratio of Change in Reference Voltage to Change in OPTO Voltage	$\Delta V_{REF}/\Delta V_{OPTO}$	V_{OPTO} = 25V to V_{REF} (Note 5)	–2.4	–1.2	–0.1	mV/V
OPTO Dynamic Impedance	$\lvert Z_{OPTO} \rvert$	V_{OPTO} = V_{REF}, I_{OPTO} = 1mA, f < 1kHz (Note 5)	0.1	0.22	0.5	Ω
OPTO Turn-On Sinking Current Capability	I_{OPTO_ON}	V_{DD} = 5V, V_{OPTO} = 3V (Note 5)	0	--	120	mA
OPTO Turn-On Impedance	R_{OPTO_ON}	I_{OPTO} = 20mA	1	--	200	Ω
OPTO Pull-Up Impedance	R_{p_OPTO}	OPTO shorted to VDD (Enable/Disable)	1	--	200	Ω
OPTO Pull-Down Impedance	R_{d_OPTO}	OPTO shorted to GND (Enable/Disable)	1	--	200	Ω
CSP Section						
Current-Sense Amplifier Gain	K_{CS}	(Note 6)	19.8	20	20.2	V/V
			29.7	30	30.3	
Current-Sense Amplifier Output Offset Voltage	V_{CS_OFFSET}		0.36	0.4	0.44	V
Current-Sense Amplifier Unit-Gain Bandwidth		(Note 5)	1000	--	5000	kHz
Current-Sense Amplifier Output Threshold for Exiting Power-Saving Mode	$V_{CS\_PSM\_EX}$	$V_{CS\_PSM\_EX}$ = V_{CSP} x K_{CS} + V_{CS_OFFSET} (Enable/Disable) (Note 6)	0.41	0.45	0.49	V
			0.51	0.55	0.59	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cable-Compensation Resistance	R_{CABLE_COMP}	(Enable/Disable) (Note 6)	40	50	60	mΩ
			65	75	85	
			90	100	110	
			105	125	145	
			130	150	170	
			180	200	220	
			230	250	270	
Cable-Compensation Transconductance Amplifier Bandwidth		(Note 5)	20	--	65	kHz
CC1/CC2 Section						
CC1/CC2 Open-Circuit Voltage	V_{CC_OC}	V_{DD} > 5V	2.9	3.25	3.6	V
CC1/CC2 Leakage Current	I_{CC_LK}	V_{DD} = 0V, V_{CC} = 5V	0	--	0.2	μA
CC1/CC2 Cable-Detached Threshold	V_{CC_CD}		2.5	2.6	2.7	V
CC1/CC2 Over-Voltage Protection Threshold	V_{CC_OVP}	(Note 6)	4.2	4.35	4.5	V
			3.85	4	4.15	
CC1/CC2 Over-Voltage Protection Debounce	t_{CC_OVP}	(Note 5) (Note 6)	0.095	0.1	0.105	ms
			0.95	1	1.05	
CC1/CC2 Sourcing Current Source	I_{SRC_CC}	V_{DD} > V_{VDD_ON} (Enable/Disable) (Note 6)	76	80	84	μA
			171	180	189	
			304	330	356	
CC1/CC2 BMC Transmitter Tx Output-High Voltage	V_{OH_CC}		1.05	1.125	1.2	V
CC1/CC2 BMC Transmitter Tx Output-Low Voltage	V_{OL_CC}		0	0.0375	0.075	V
CC1/CC2 BMC Transmitter Tx Rise Time	t_{RISE_CC}	C_{LOAD} < 470pF	300	--	700	ns
CC1/CC2 BMC Transmitter Tx Fall Time	t_{FALL_CC}	C_{LOAD} < 470pF	300	--	700	ns
CC1/CC2 BMC Transmitter Rx Input-High Voltage	V_{IH_CC}	(Note 6)	0.8	0.9	1.0	V
			0.7	0.8	0.9	
			0.6	0.7	0.8	
			0.5	0.6	0.7	
CC1/CC2 BMC Transmitter Rx Input-Low Voltage	V_{IL_CC}	(Note 6)	V_{IH_CC} - 0.1	V_{IH_CC} - 0.1	V_{IH_CC} - 0.1	V
CC1/CC2 VCONN Voltage	V_{CONN}	V_{DD} = 5V, I_{VCONN} = 0mA	3.8	4	4.2	V
		V_{DD} = 5V, I_{VCONN} = 30mA	3.3	--	3.5	
CC1/CC2 VCONN Short-Circuit Current	I_{VCONN_SC}		45	70	95	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Section						
VBUS Built-In Blocking N-MOSFET Turn-On Resistance	R_{ON_VBUS}	V_{GS} = 10V, I_{DS} = 4A @ T_C = 25°C Measured between VDD and VBUS	11	12.2	13.4	mΩ
		V_{GS} = 10V, I_{DS} = 4A @ T_C = 105°C Measured between VDD and VBUS (Note 5)	15.4	--	18.76	
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V Freq = 1MHz	--	1094	--	pF
Output Capacitance	C_{oss}		--	147	--	
Reverse Transfer Capacitance	C_{rss}		--	127	--	
Drain to Source Breakdown Voltage	BV_{DSS}	I_{DS} = 250μA, V_{GS} = 0V	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	--	--	1	μA
Gate to Source Breakdown Voltage	V_{GSS}	V_{DS} = 24V, V_{GS} = 0V	–20	--	20	V
Gate Threshold Voltage	V_{GS_TH}	V_{GS} = V_{DS}, I_{DS} = 250μA	1	--	2.5	V
Body Diode Forward Voltage	V_{SD}	I_{SD} = 1A, V_{GS} = 0V	--	0.7	1.1	V
Revers Recovery Time	t_{rr}	I_F = 1A, V_R = 0V dI_F/dt = 100A/μs	--	14	--	ns
Revers Recovery Charge	Q_{rr}		--	5.6	--	nC
VBUS Short-Circuit Protection Threshold	V_{VBUS_SCP}	N-MOSFET driver = ON V_{DD} - V_{BUS} > V_{VBUS_SCP} (Enable/Disable) (Note 6)	0.05	0.15	0.25	V
			0.2	0.3	0.4	
VBUS Short-Circuit Protection Deglitch	t_{VBUS_SCP}	(Note 5) (Note 6)	8	10	12	μs
			16	20	24	
VBUS Discharge Impedance	R_{DIS_VBUS}	N-MOSFET driver = OFF I_{DIS_VBUS} = 20mA	0.7	1	1.3	kΩ
Accuracy Section						
Voltage Regulation Accuracy	E_{VOUT}	V_{OUT} = 3.3V to 21V, I_{OUT} = 1A to 4A	–100	--	100	mV
Current Regulation Accuracy	E_{IOUT}	V_{OUT} = 3.3V to 21V, I_{OUT} = 1A to 4A, R_{CS} = 1% accuracy	–150	--	150	mA
Internal Thermal Sensor Accuracy	E_{TS}	T_C = –40°C to 105°C	–7	--	7	°C

Note1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

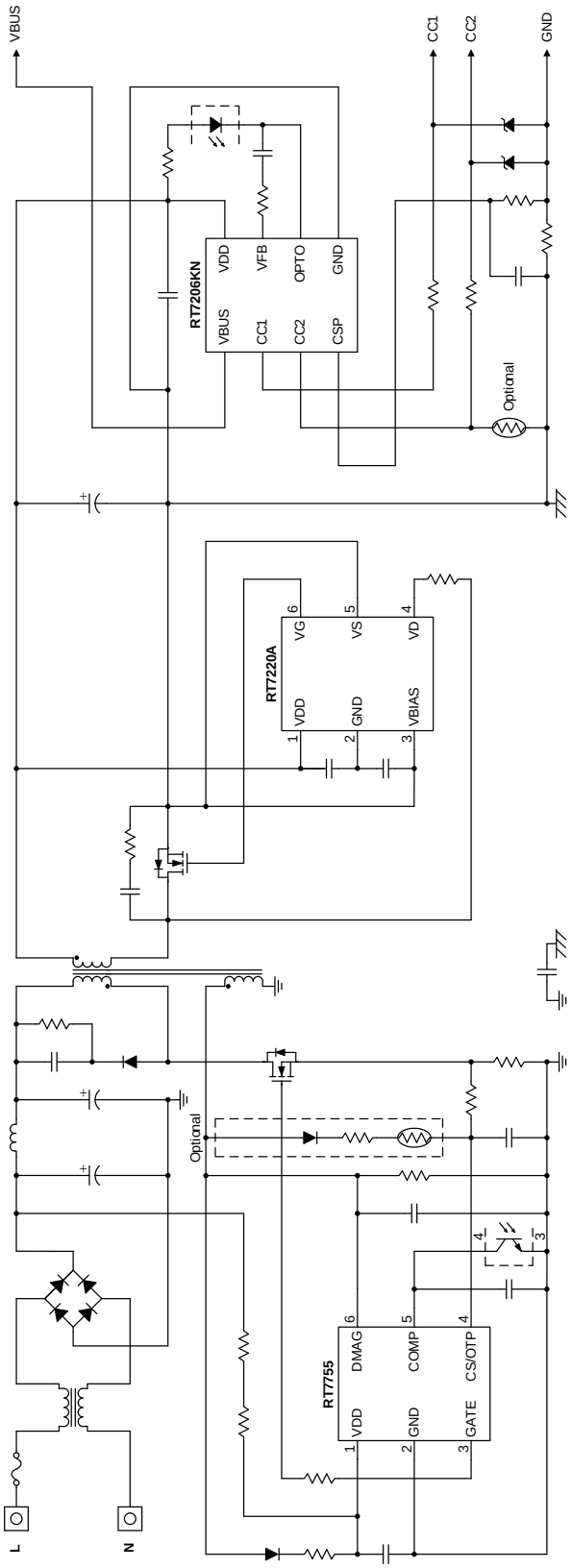
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

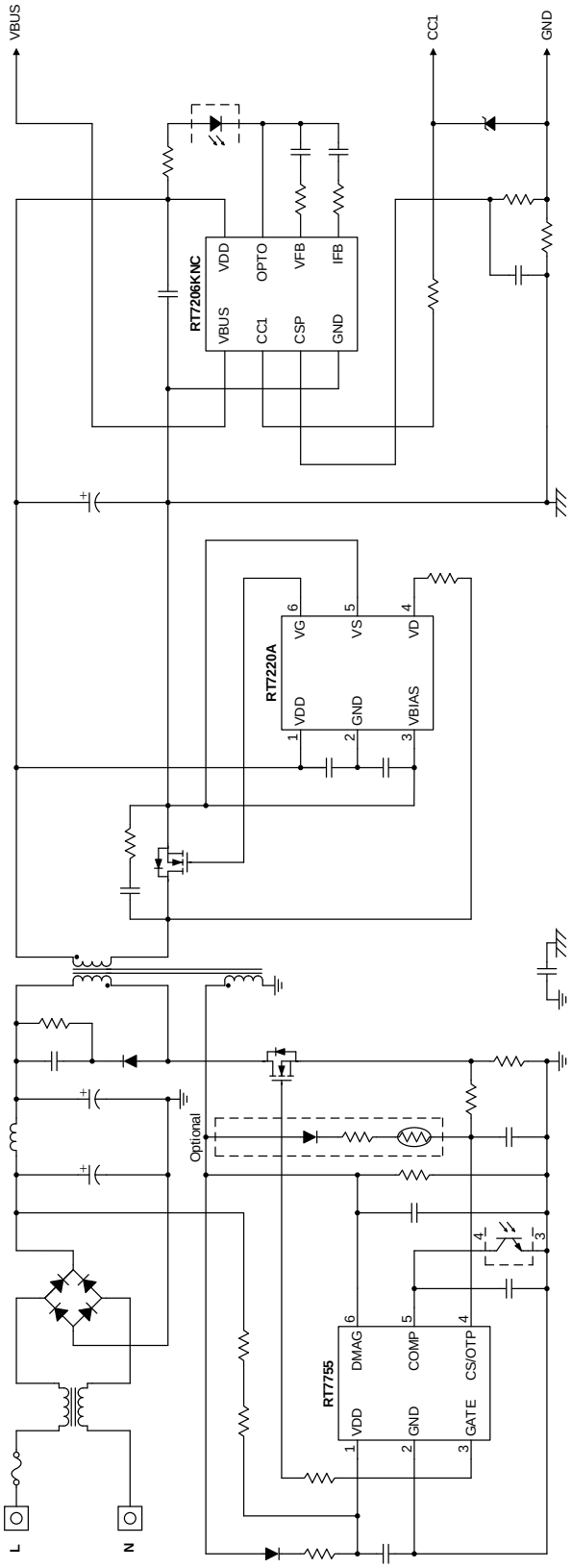
Note 5. Guaranteed by design.

Note 6. Register option by OTP program.

Typical Application Circuit

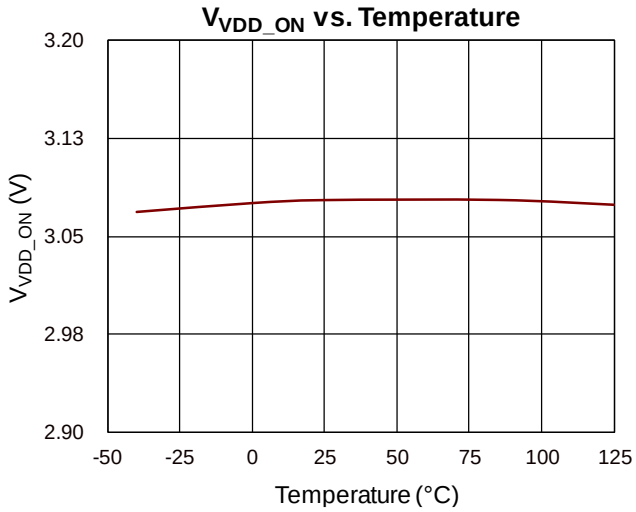


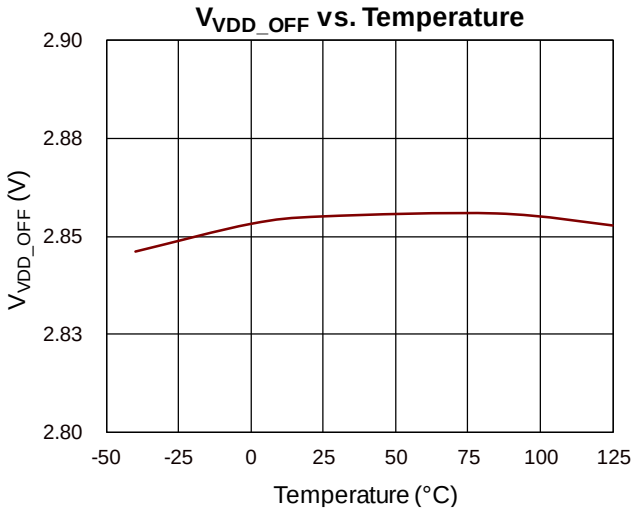
RT7206KN Typical Application Circuit

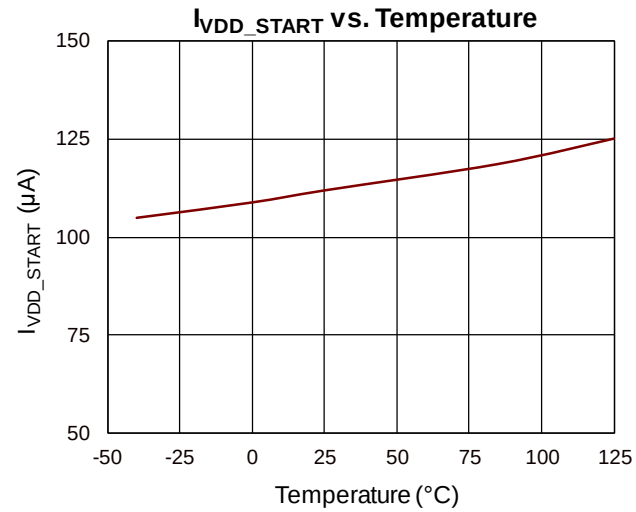


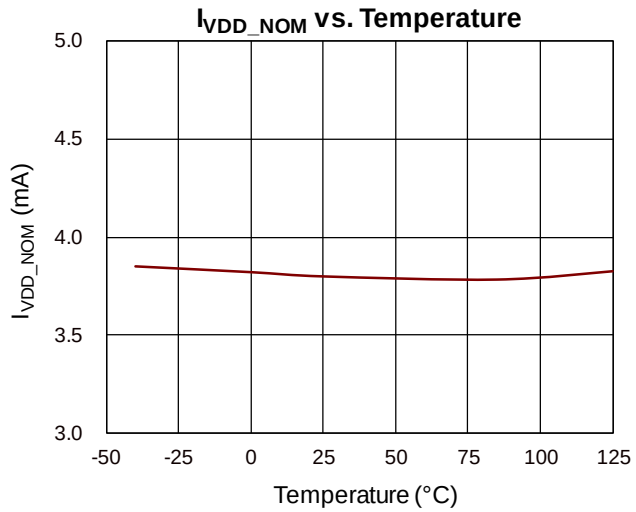
RT7206KNC Typical Application Circuit

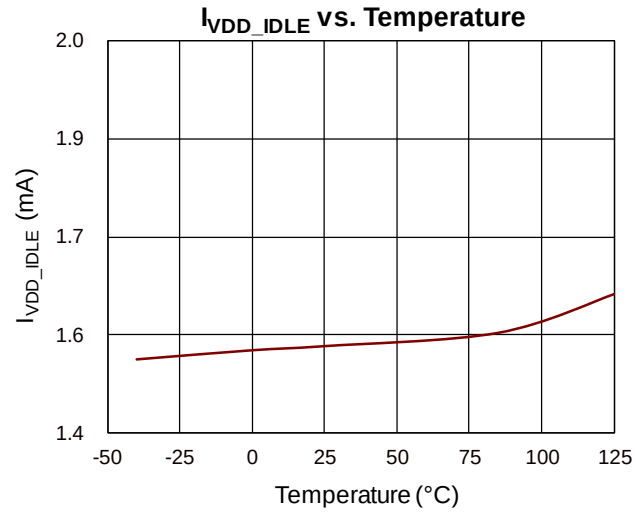
Typical Operating Characteristics

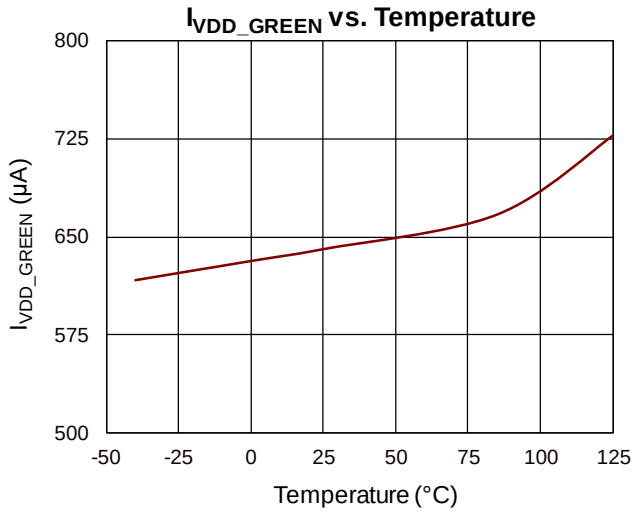


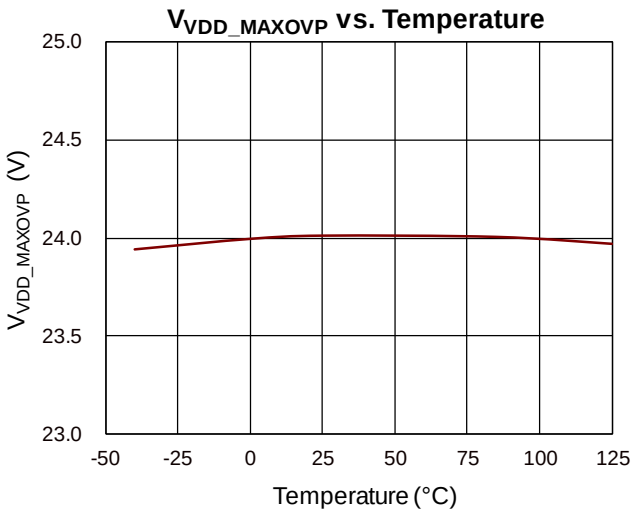


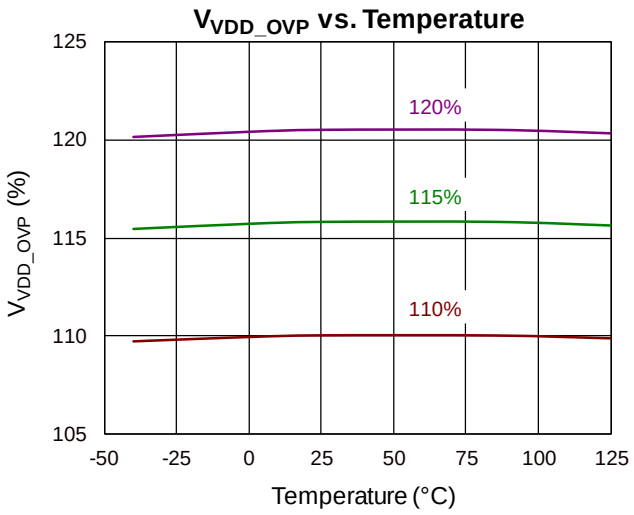


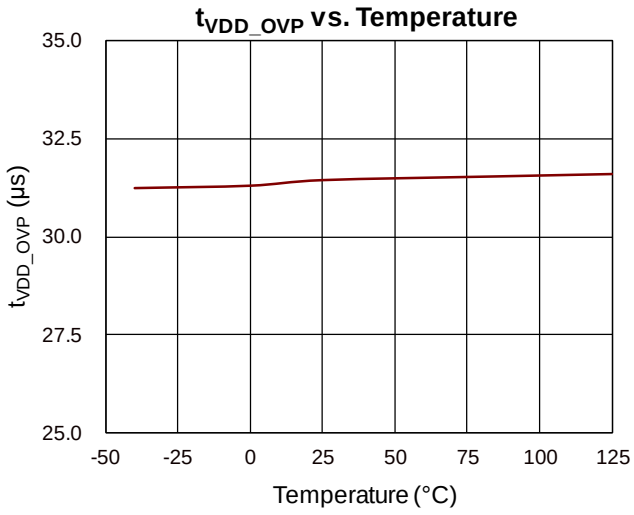


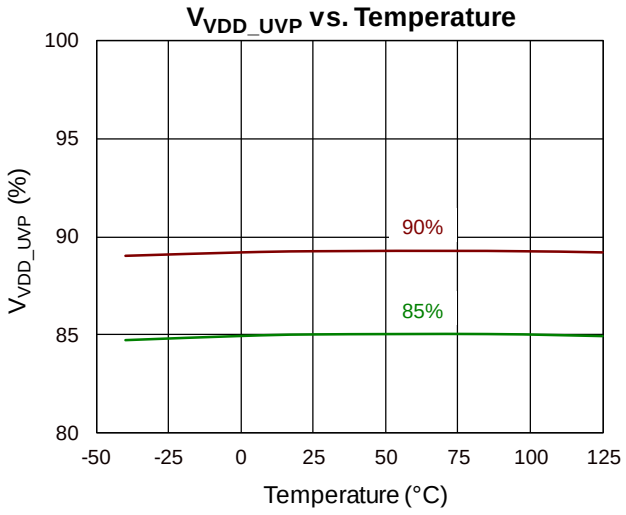


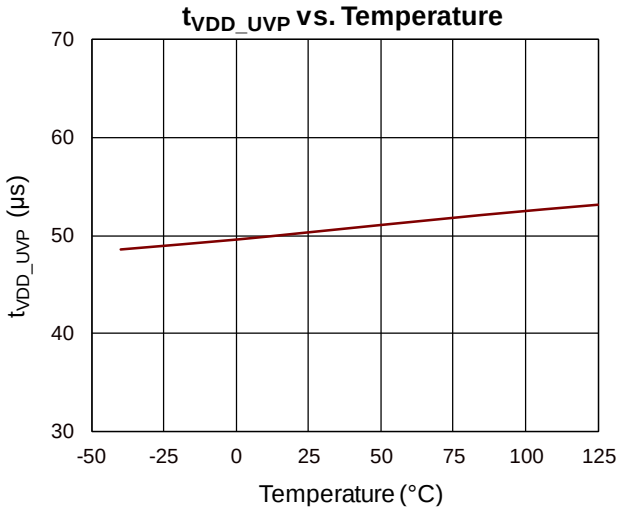


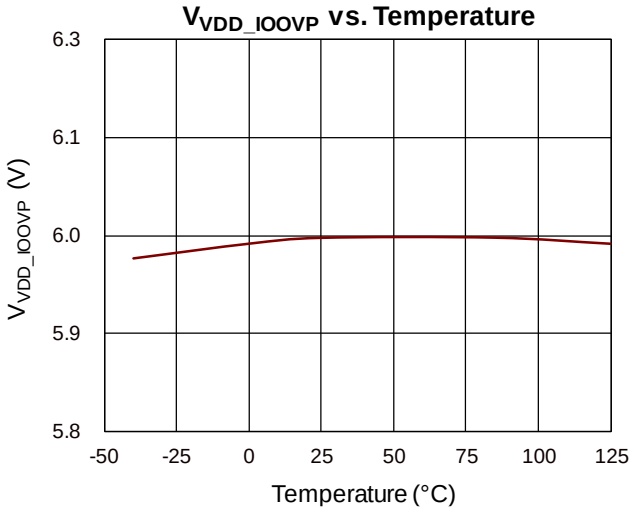


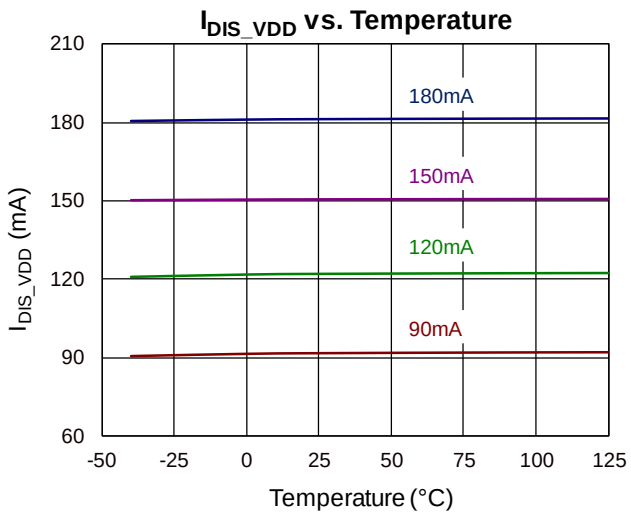


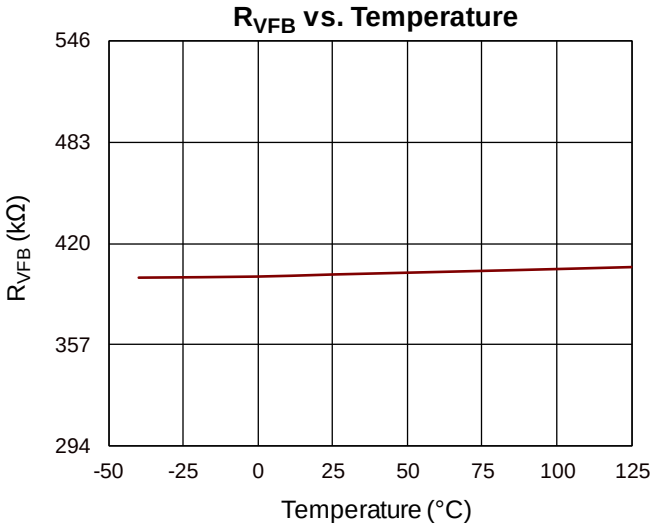


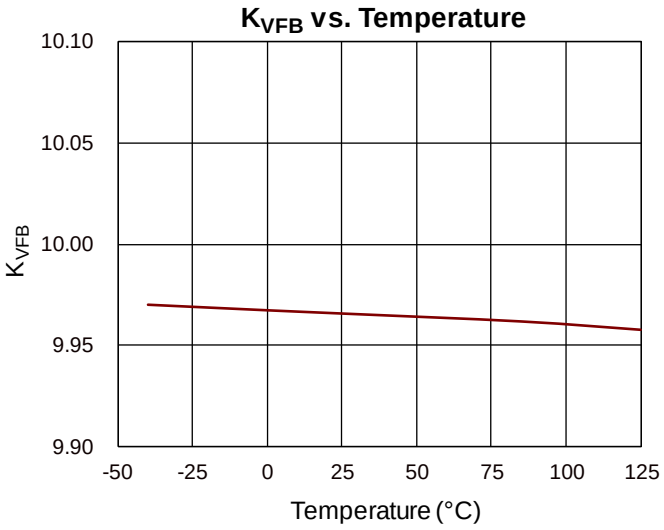


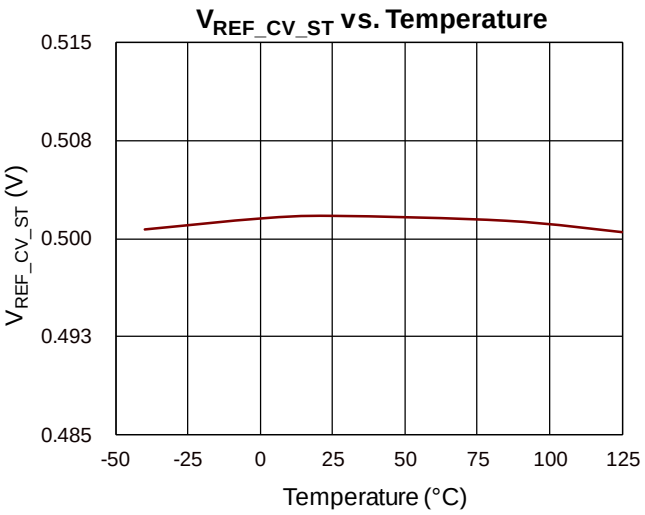


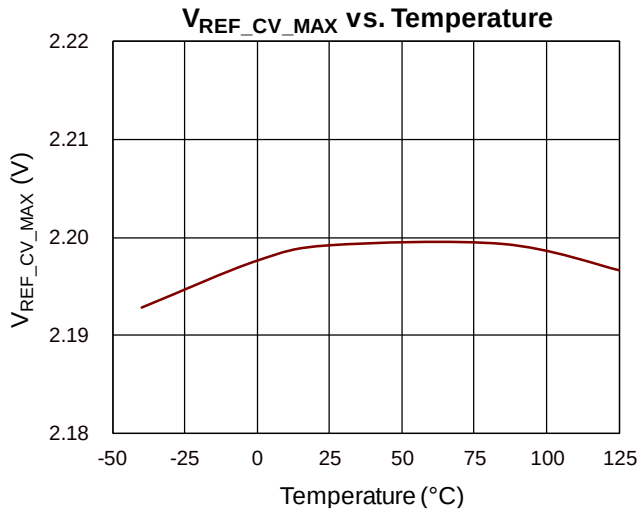


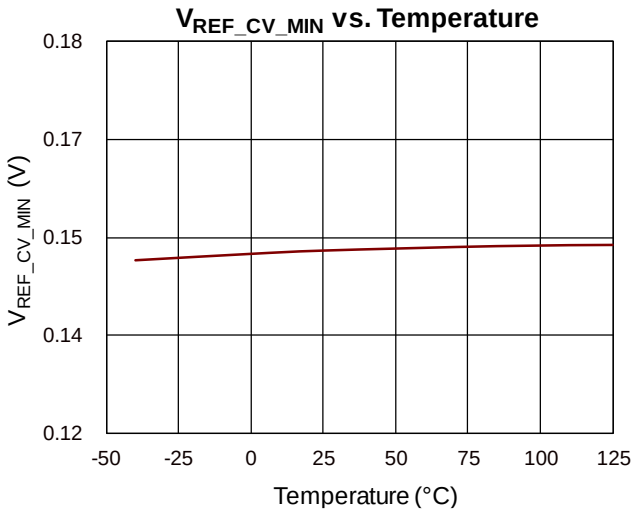


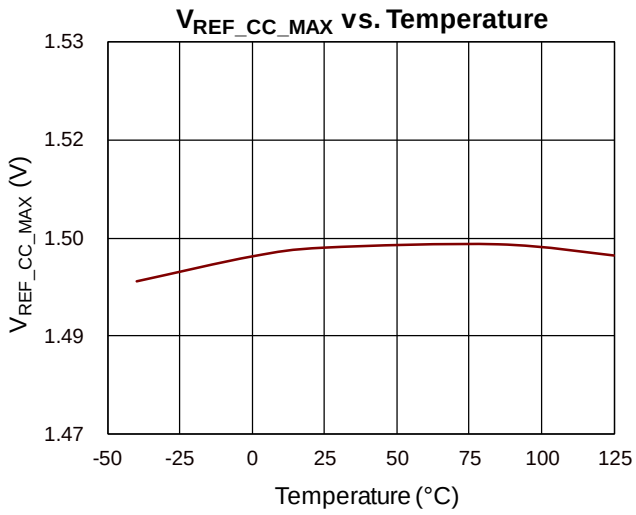


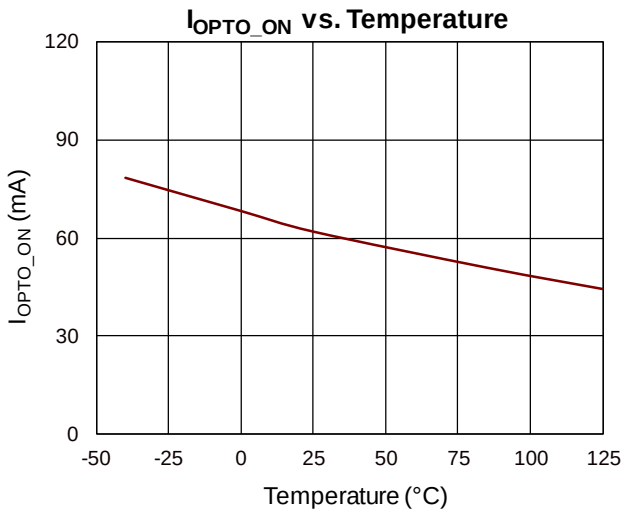


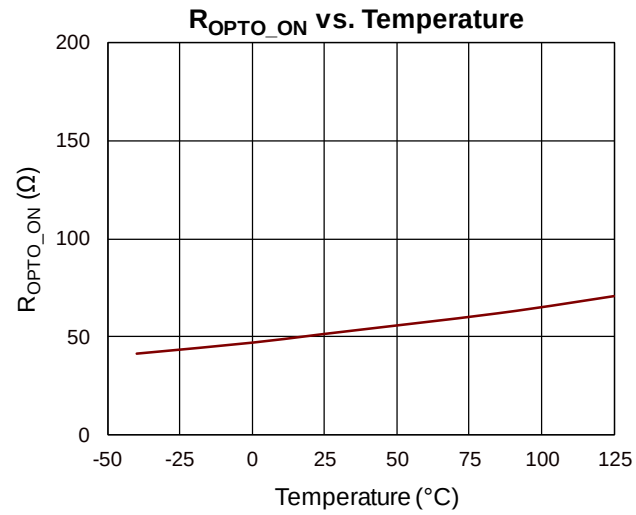


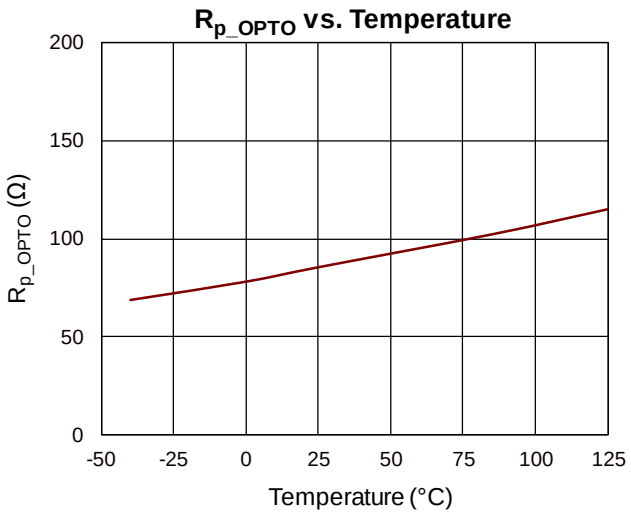


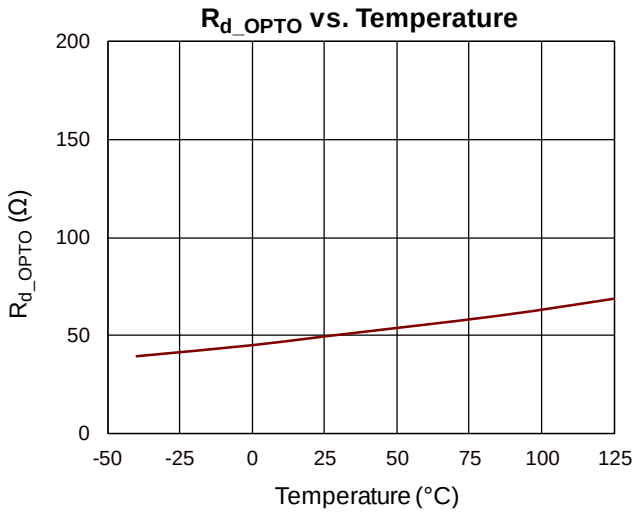


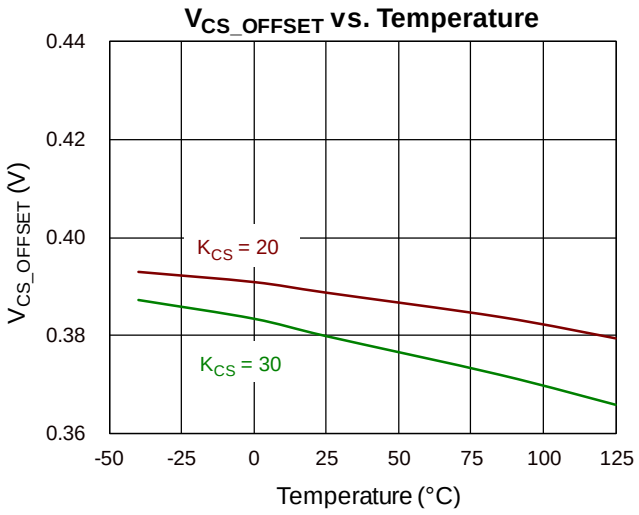


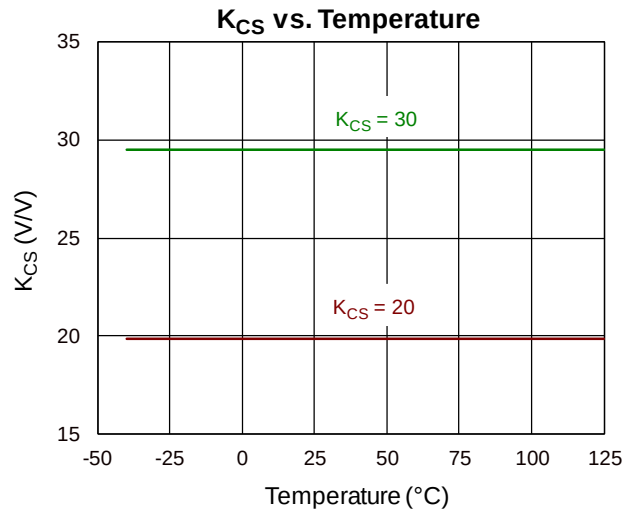


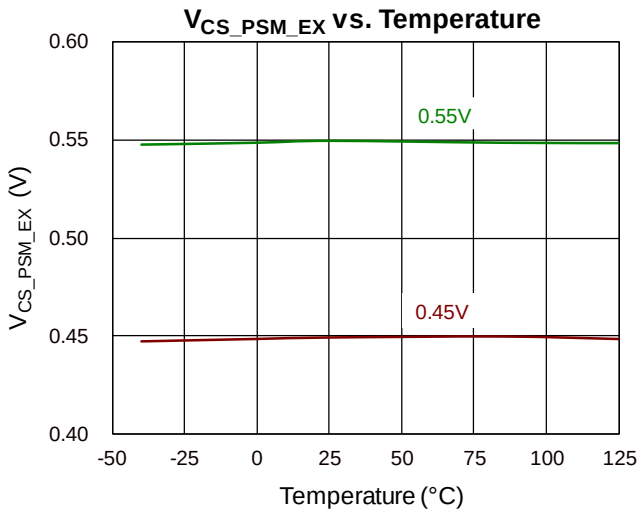


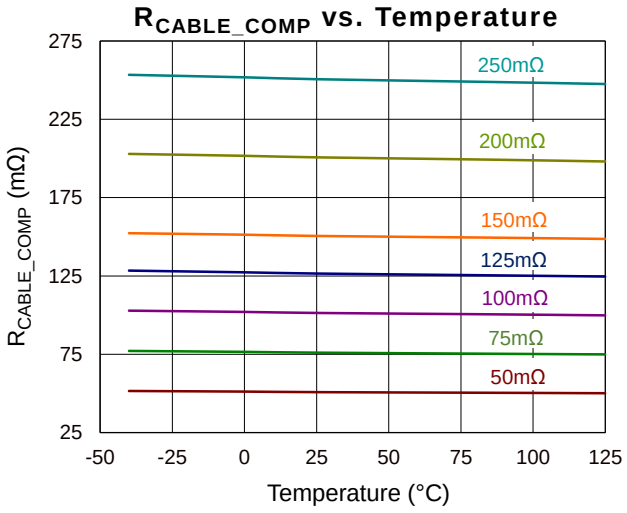


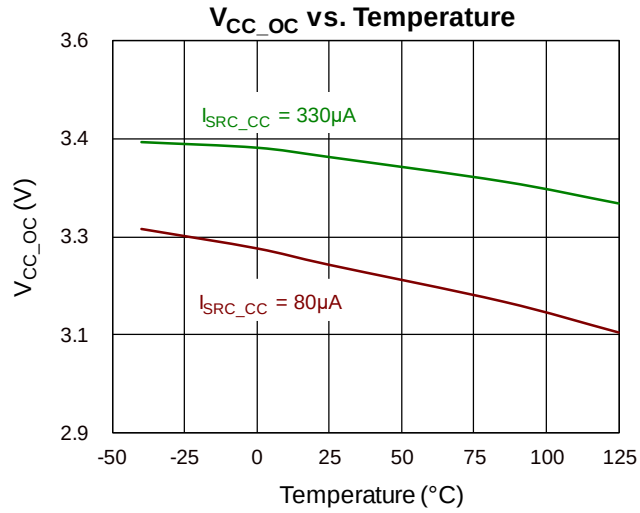


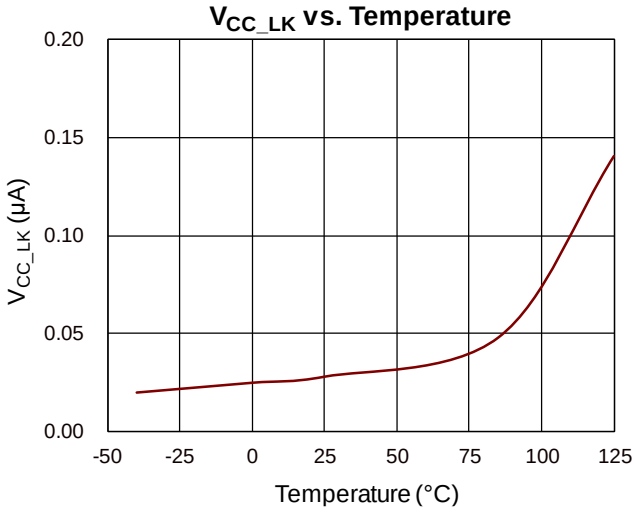


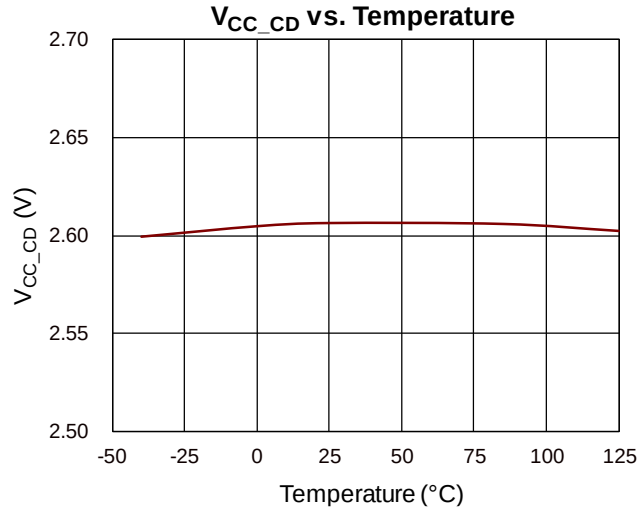


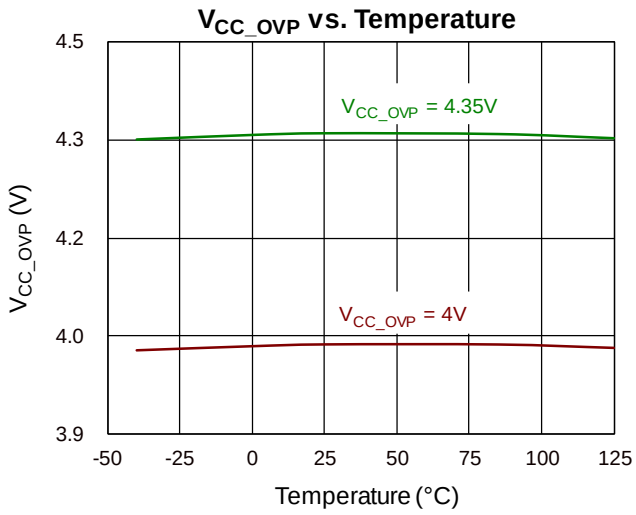


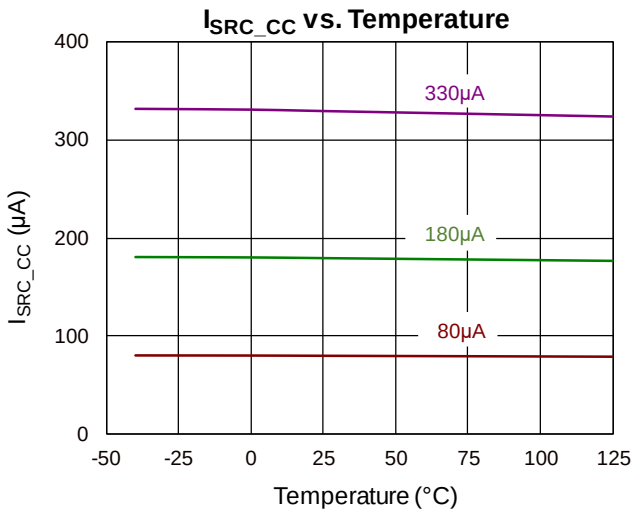


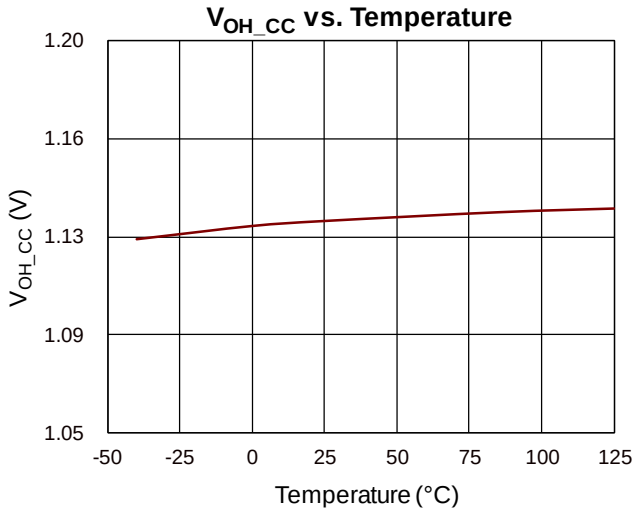


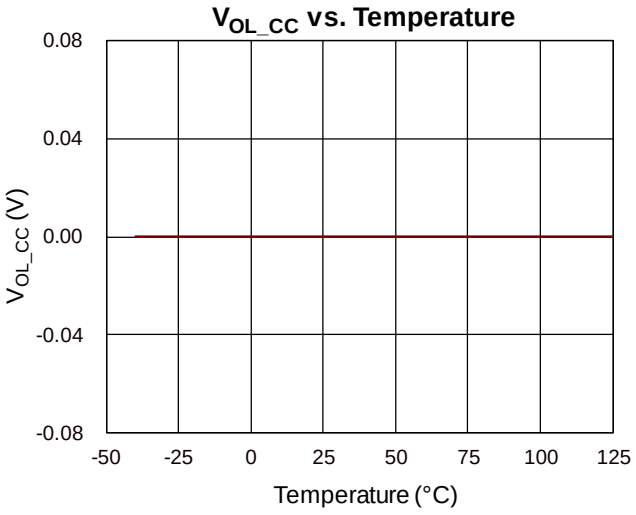


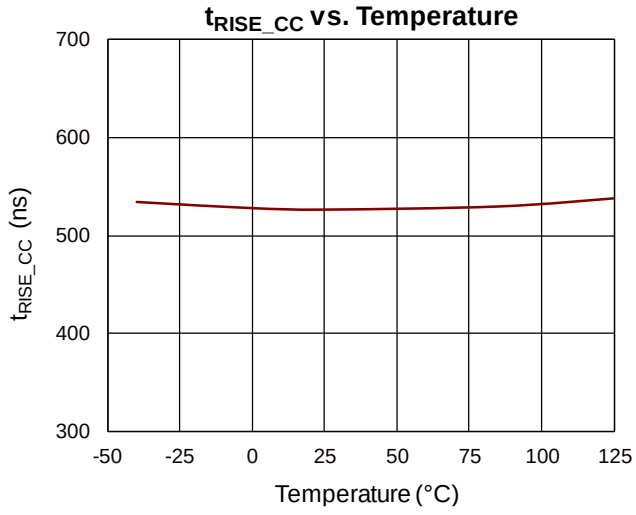


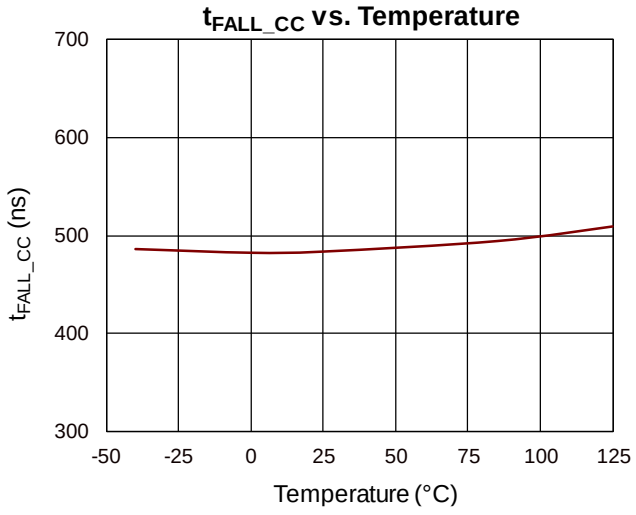


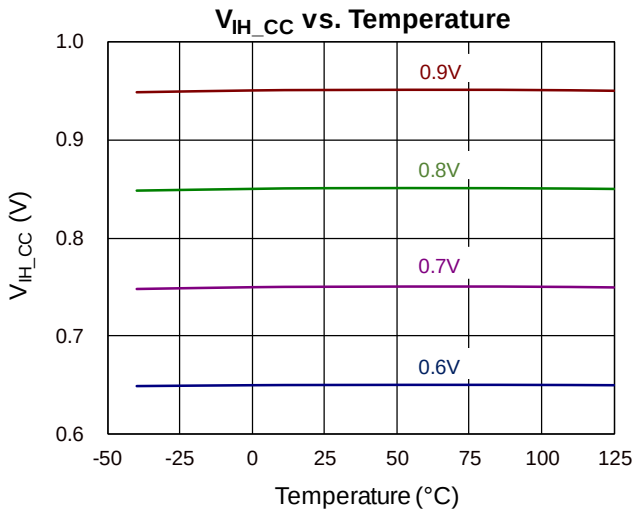


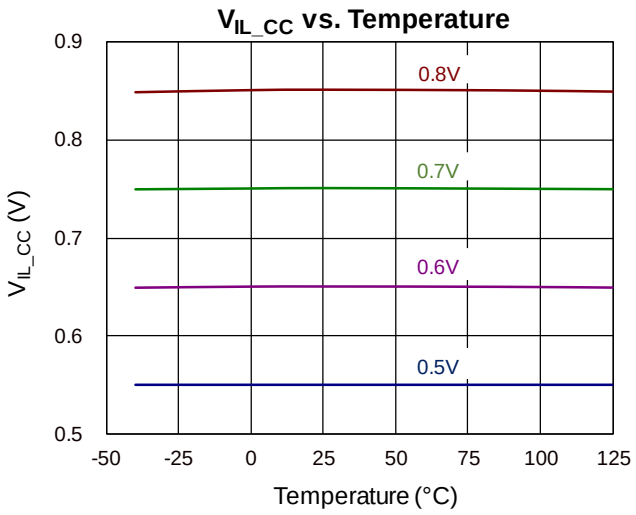


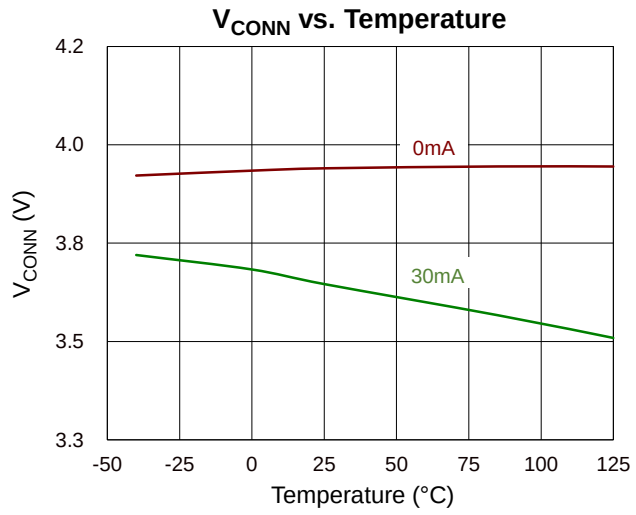


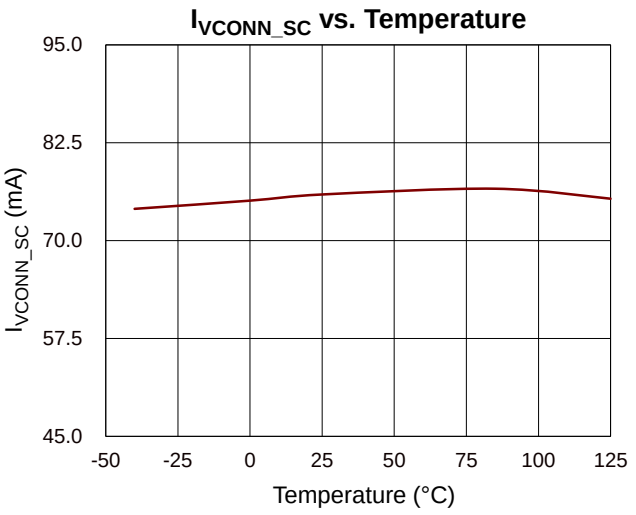


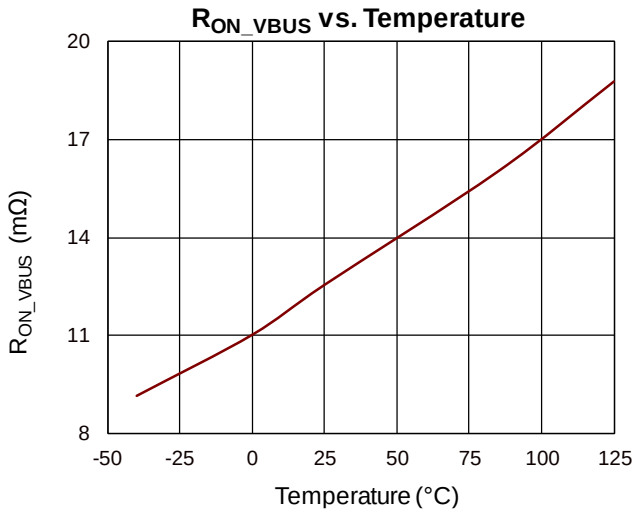


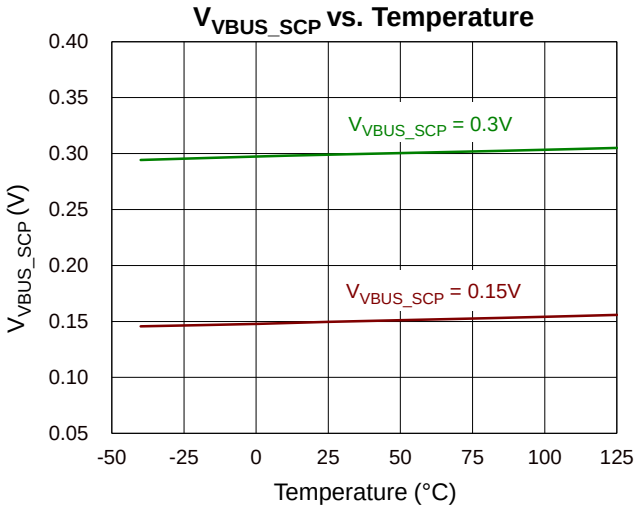


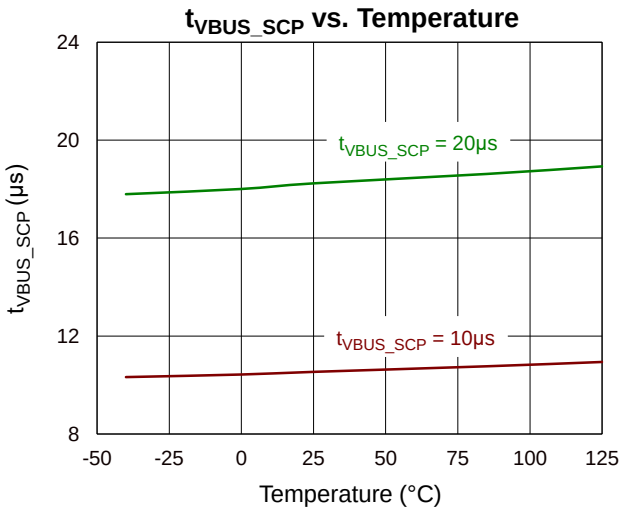


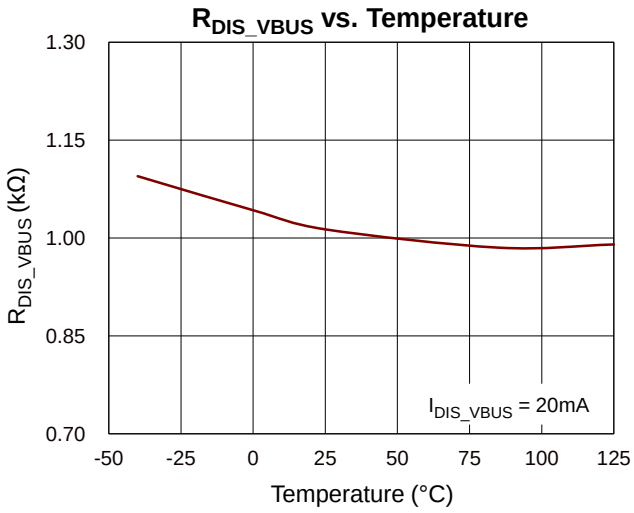












Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

AC-DC Source Port

- **Voltage Sense and Current Sense**

  The RT7206KNx series integrates a resistor divider, R_{VFB}, for voltage feedback as shown in Figure 1. The voltage related to VDD, V_{DD} is determined as :

  $V_{DD} = K_{VFB} \times V_{VFB}$

  $K_{VFB} = (R_{VFB1} + R_{VFB2}) / R_{VFB2} = 10$

  The RT7206KNx series also integrates a differential amplifier so that the sensed current, I_{CS}, through the current-sense resistor, R_{CS}, is determined as :

  $I_{CS} = (V_{IFB} – V_{CS\_OFFSET}) / (R_{CS} \times K_{CS})$

- **Constant-Voltage (CV) and Constant-Current (CC) Regulations**

  For the CV loop, V_{DD} is determined by the reference voltage of CV regulator, V_{REF_CV}. For the CC loop, I_{CS} is determined by the reference voltage of CC regulator, V_{REF_CC}. Two loops incorporate an error amplifier respectively and both of them are connected to OPTO, driving the sinking current from the external circuit with an optocoupler and a resistor, R_D, in series to V_{DD}. The optocoupler transfers the compensation signal from the secondary side to the primary side. Note that for better linearity of the compensation range, R_D is suggested to be designed for satisfying the maximum COMP current of PWM controller, I_{COMP_MAX}, at the minimum voltage related to VDD, V_{DD_MIN}.

$$\frac{(V_{DD\_MIN} - V_F - 0.3V)}{R_D} \times CTR \geq I_{COMP\_MAX}$$

  CTR : Current transfer ratio of the optocoupler

  V_F : Forward voltage of the optocoupler

  0.3V : The threshold of OPTO voltage for driving the minimum OPTO sinking current

- **Linear Cable Compensation**

  A transconductance amplifier is integrated for linear cable compensation. The compensation voltage, V_{CABLE_COMP}, is determined as :

  $V_{CABLE\_COMP} = I_{CS} \times R_{CABLE\_COMP}$

  In addition, a programmable solution is reserved by ADC-measurement as a proprietary function.

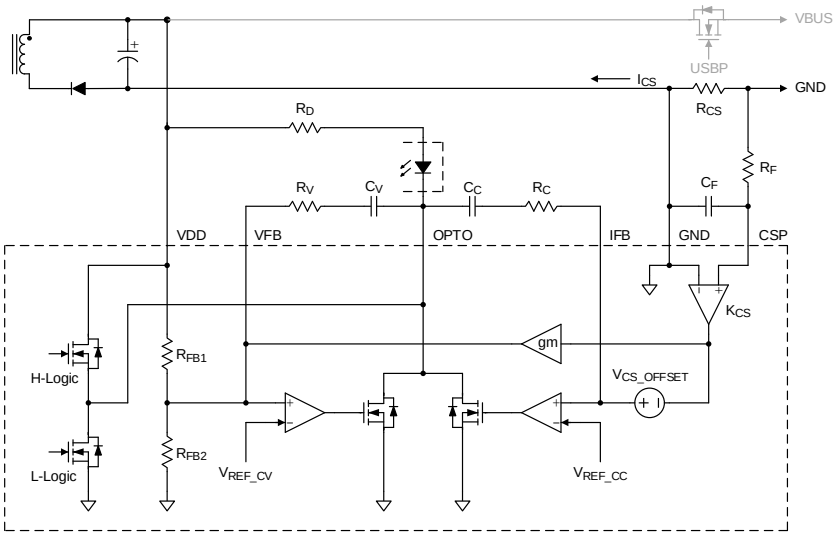


Figure 1. Application Circuit for CV and CC Regulations

Power Sequence

When start-up, V_{REF_CV} is set to the standby reference voltage, $V_{REF\_CV\_ST}$, and then V_{DD} is regulated to 5V. Once a Type-C cable attached, the Sink port will deliver power request back to the embedded MCU, changing V_{REF_CV} and regulating V_{DD} to the correspond voltage level. In contrary, once the Type-C cable detached, the embedded MCU will enter power-saving mode and back to 5V.

Rising and Falling Regulation

As shown in Figure 2, when PD protocol is detected, V_{REF_CV} can be set by the request of the Sink port. Both rise and fall time of V_{DD} must meet PD compliance, defined as 275ms. The slope of V_{REF_CV} during rising interval, S_{RISE}, can be determined as:

$$S_{RISE} \geq \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

V_{DD_MAX} : Maximum voltage request

V_{DD_MIN} : Minimum voltage request

275ms : Rise and fall time of PD compliance

25ms : Time margin from transient response of system

During the falling interval, the constant-discharge current, I_{DIS_VDD}, is enabled. The capability of I_{DIS_VDD} must take the output capacitors of system, C_{OUT}, in consideration. I_{DIS_VDD} can be determined as :

$$I_{DIS\_VDD} \geq C_{OUT} \times \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

The slope of V_{REF_CV} during falling interval, S_{FALL}, can be determined as :

$$\frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms} \leq S_{FALL} \leq \frac{I_{DIS\_VDD}}{C_{OUT}}$$

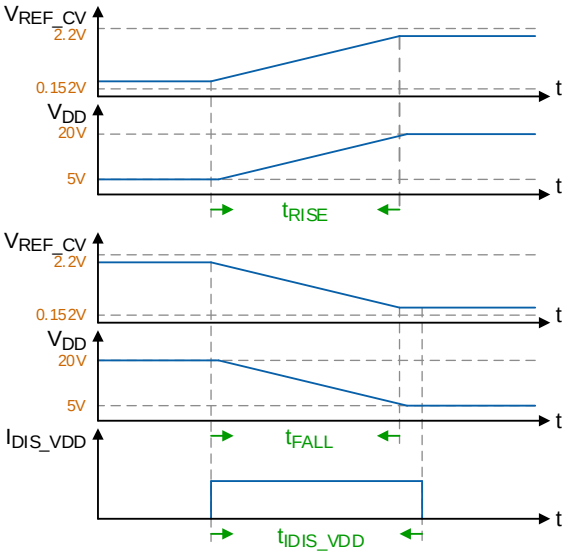


Figure 2. Rising and Falling Regulation

Programmable Shutdown Flow from Protections

The RT7206KNx series can achieve multiple behaviors for any abnormal condition occurs.

- Auto-Recovery

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is forced down to V_{VDD_OFF} by pulling V_{OPTO} down. After V_{DD} turned-off, V_{OPTO} is released and V_{DD} is powered up again.

- Output-Latch

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is set back to 5V. To recover the system, the DC cable must be removed and then attached again.

- Power-Latch

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is set back to 5V. After that, V_{OPTO} is pulled high to trigger the protection from the primary-side PWM controller, which is supposed to be a latch behavior. To recover the system, the AC cable must be removed and then attached again.

Over/Under-Voltage Protection (OVP/UVP)

As shown in Figure 3 and Figure 4, the RT7206KNx series provides a quick-interruption solution to turn off the blocking N-MOSFET when either over-voltage or under-voltage condition occurs in VDD, such as the malfunction of feedback loop due to aging of the optocoupler. Once V_{DD} is higher than the over-voltage protection threshold, V_{VDD_OVP}, over the deglitch time, t_{VDD_OVP}, or V_{DD} is lower than the under-voltage protection threshold, V_{VDD_UVP}, over the deglitch time, t_{VDD_UVP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU. Besides, a programmable solution is reserved by ADC-measurement as a proprietary function.

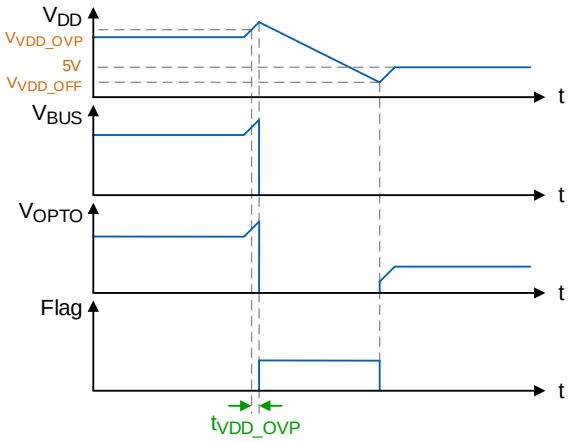


Figure 3. Timing Sequence of OVP with Auto-Recovery

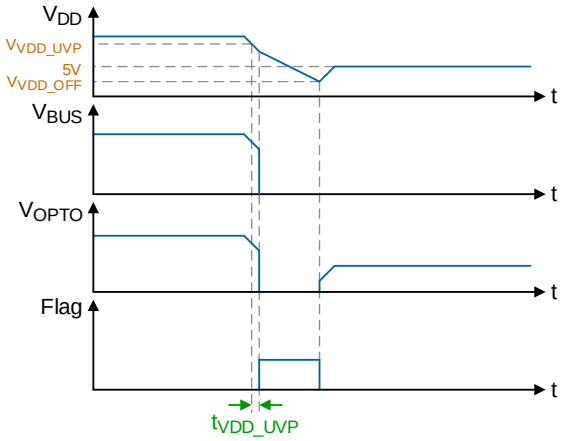


Figure 4. Timing Sequence of UVP with Auto-Recovery

Short-Circuit Protection (SCP)

As shown in Figure 5, a quick-interruption solution is designed to preventing the damage from short-circuit condition in VBUS. When the situation happens, the voltage difference between VDD and VBUS, V_{ON_VBUS}, will Instantaneously rise due to the huge current. Once V_{ON_VBUS} is higher than the short-circuit protection threshold, V_{VBUS_SCP}, over the deglitch time, t_{VBUS_SCP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU.

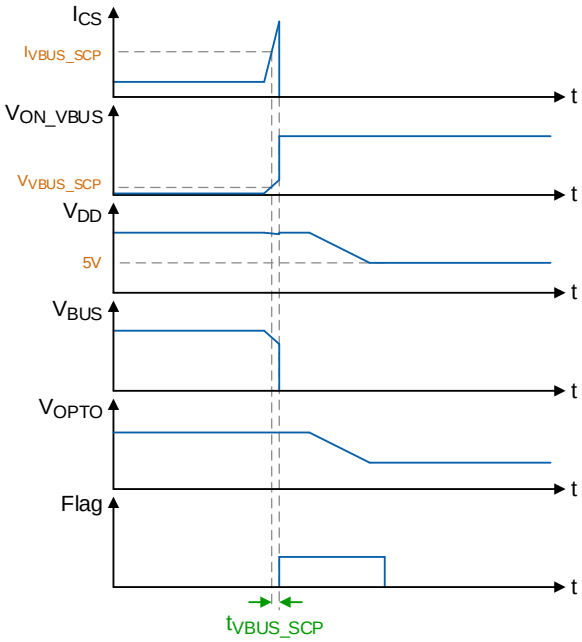


Figure 5. Timing Sequence of SCP with Output-Latch

CC1/CC2 Over-Voltage Protection (IO OVP)

In order to prevent the damage of CC1/CC2 from the abnormal contact to VBUS at the USB Type-C receptacle, a quick-interruption solution is designed to turn off the blocking N-MOSFET as shown in Figure 6. Once V_{DD} is higher than the threshold for CC1/CC2 over-voltage protection, V_{VDD_IOOVP}, and the voltage related to CC1/CC2, V_{CC} is higher than the CC1/CC2 over-voltage protection threshold, V_{CC_OVP}, over the debounce time, t_{CC_OVP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU.

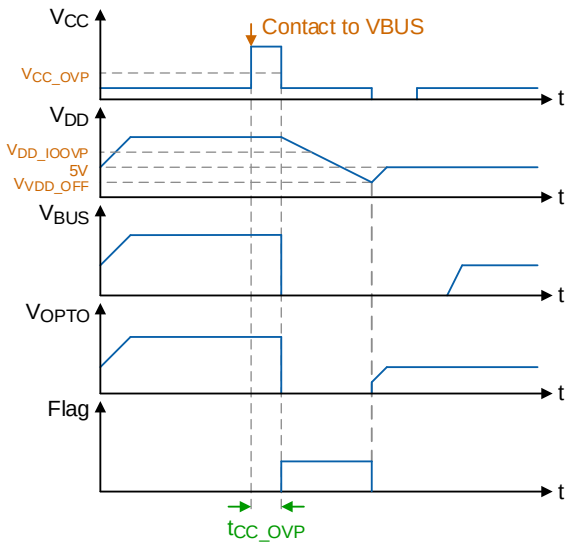


Figure 6. Timing Sequence of CC1/CC2 OVP with Auto-Recovery

- **Over-Current Protection (OCP)**

The RT7206KNx series provides a programmable solution by ADC-measurement to achieve over-current protection as shown sin Figure 7. Once I_{CS} is higher than the programming threshold, I_{OCP_ADC}, over a debounce time, t_{OCP_ADC}, the programmable shutdown flow will be triggered.

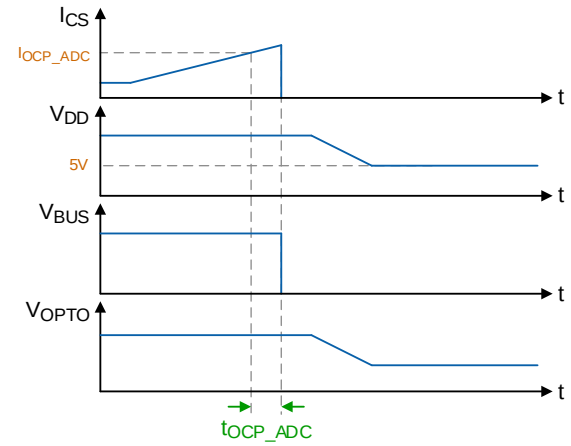


Figure 7. Timing Sequence of OCP with Output-Latch

- **Over-Temperature Protection (OTP)**

A programmable solution by ADC-measurement to achieve over-temperature protection is designed as shown in Figure 8. If any of specific I/O pins, CC1/CC2, can be defined as general purpose I/O, the internal sourcing current source, I_{SRC_CC}, will be set to 80μA. By using an NTC/PTC connected between CC1/CC2 and GND, the ambient in the specific region can be monitored. Once the voltage related to CC1/CC2, V_{CC}, is lower than the over-temperature threshold, V_{OTP_ADC}, over a debounce time, t_{OTP_ADC}, the programmable shutdown flow will be triggered.

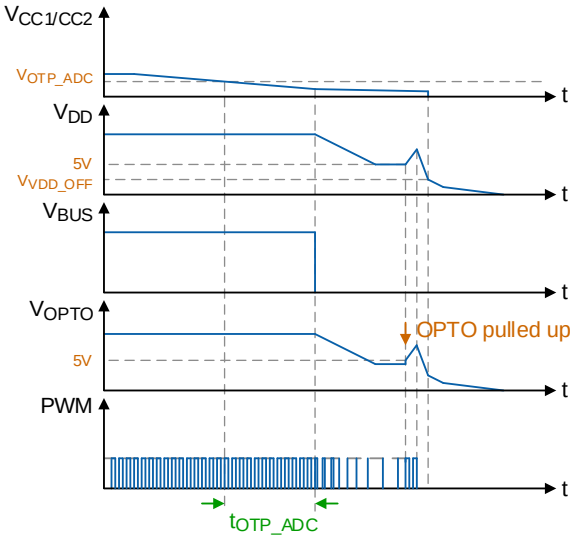


Figure 8. Timing Sequence of OTP with Power-Latch

Sink Port (RT7206KN Only)

- **Power Sequence**

  When a Type-C cable attached, VDD will be powered up by 5V from the Source port. After that, the embedded MCU will read the ADC voltage in OPTO, V_{ADC_OPTO}, to get the correspond power request. If Source Capabilities of the Source port is compatible, the request will be delivered to the Source port, changing 5V to the correspond voltage level. Once the ADC voltage in VDD, V_{ADC_VDD}, is recognized, the blocking N-MOSFET will be turned on for delivering power to the Host.

- **Capability Selection**

  The level of V_{OPTO} can be easily designed by the resistors, R_{SEL1} and R_{SEL2}, with 1% tolerance between VDD and GND as shown in Figure 9.

Sink Capabilities		R_{SEL1}	R_{SEL2}
1	User Define	Open	Short
2	User Define	Open	11kΩ
3	User Define	Open	24.9kΩ
4	User Define	Open	56kΩ
5	User Define	Open	220kΩ
6	User Define	130kΩ	Open
7	User Define	19.6kΩ	Open
8	User Define	Short	Open

- **Programmable Shutdown Flow from Protections**

  As the Sink port, RT7206KN provides the solutions below once any abnormal condition occurs.

  - Output-Latch

    Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off. To recover the system, the output cable must be removed and then attached again.

- **Over/Under-Voltage Protection (OVP/UVP)**

  The RT7206KN series provides a programmable solution by ADC-measurement to achieve over-voltage or under-voltage protection. Once V_{DD} is higher than the programming threshold, V_{OVP_ADC}, over a debounce time, t_{OVP_ADC}, or V_{DD} is lower than the programming threshold, V_{UVP_ADC}, over a debounce time, t_{UVP_ADC}, the programmable shutdown flow will be triggered.

- **Over-Current Protection (OCP)**

  The RT7206KN also provides a programmable solution by ADC-measurement to achieve over-current protection. Once I_{CS} is higher than the programming threshold, I_{OCP_ADC}, over a debounce time, t_{OCP_ADC}, the programmable shutdown flow will be triggered.

- **Over-Temperature Protection (OTP)**

  A programmable solution by ADC-measurement to achieve over-temperature protection is designed. Once the voltage of the internal thermal sensor, V_{TS}, is higher than the programming threshold, V_{OTP_ADC}, over a debounce time, t_{OTP_ADC}, the programmable shutdown flow will be triggered.

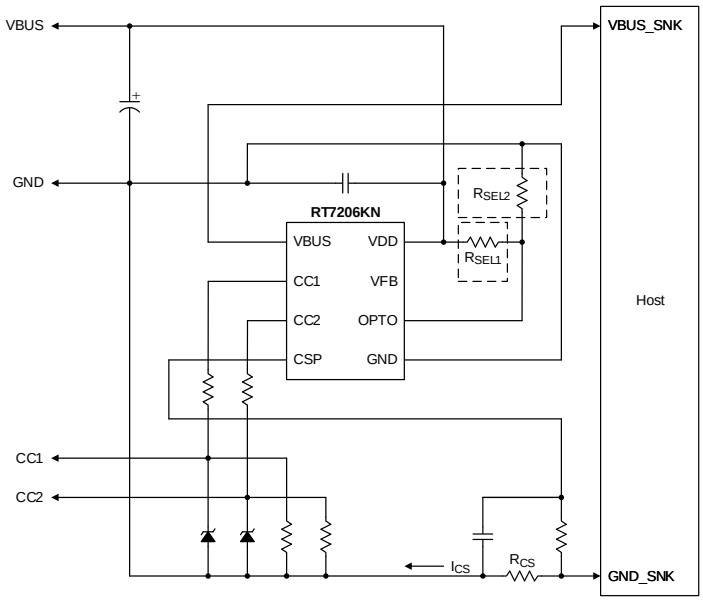


Figure 9. Application Circuit for Capability Selection

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA}, is 261.1°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (261.1°C/W) = 0.38W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 10 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

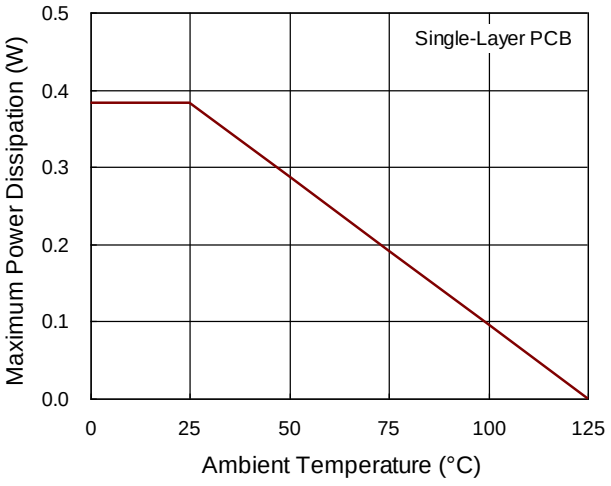
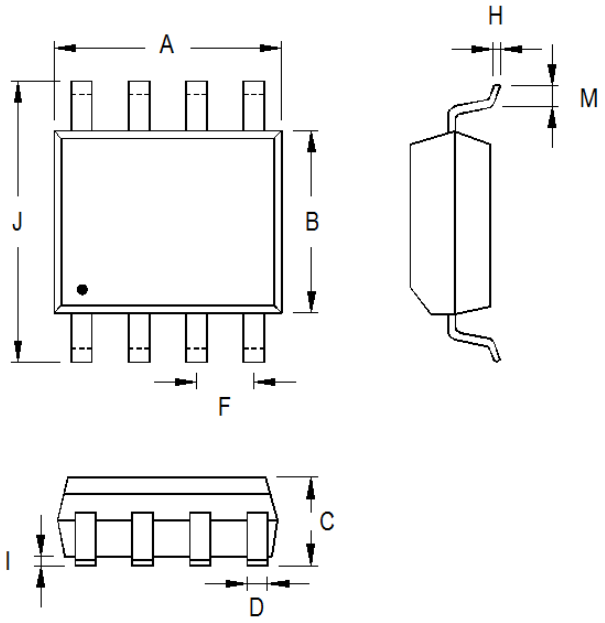


Figure 10. Derating Curve of Maximum Power Dissipation

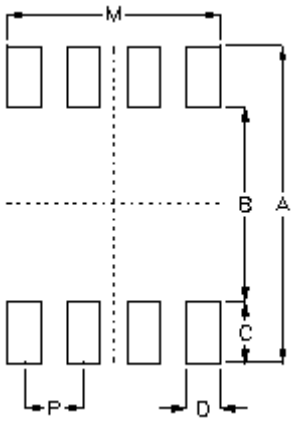
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

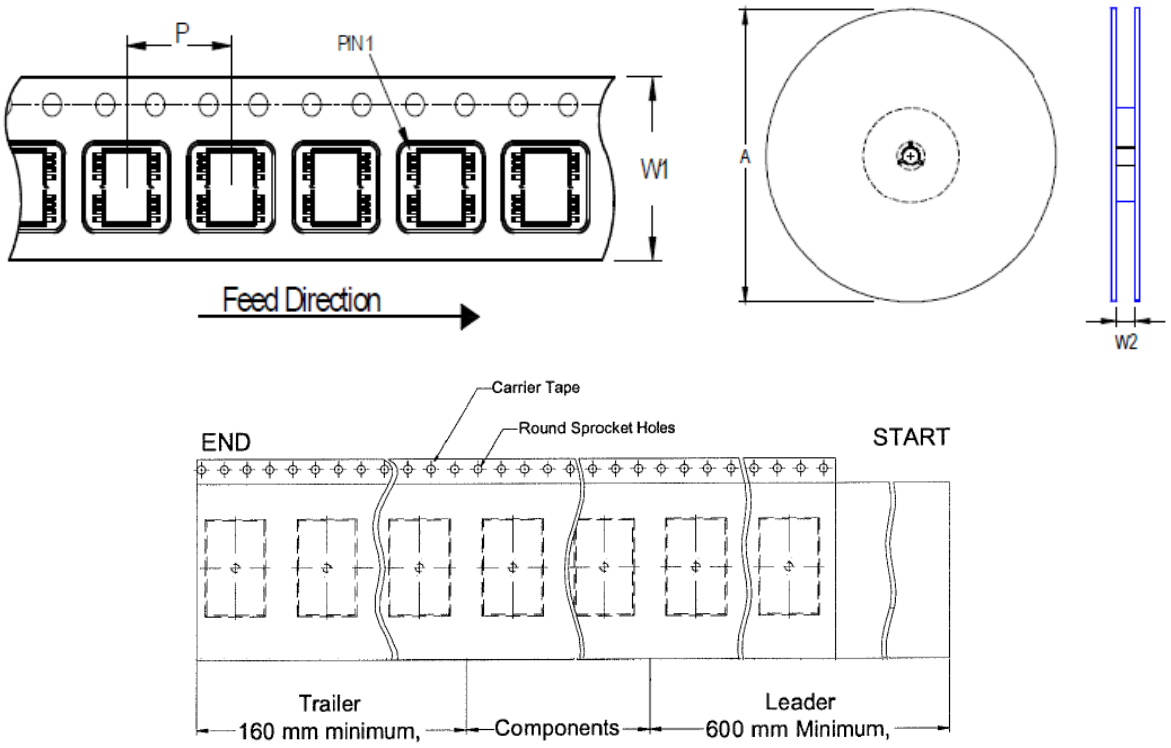
Footprint Information



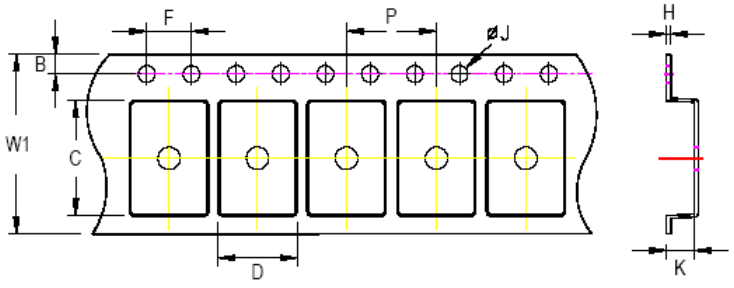
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8/SOP-8(FC)	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo / Description	Step	Photo / Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
01	2023/2/22	Modify	Simplified Application Circuit on P2, 3 Functional Pin Description on P4 Operation on P5 Recommended Operating Conditions on P6 Electrical Characteristics on P6 to P9 Typical Application Circuit on P10, 11 Typical Operating Characteristics on P16, 18, 19 Application Information on P20 to P25
02	2023/9/22	Modify	General Description on P1 Ordering Information on P1 Electrical Characteristics on P9 Application Information on P21