

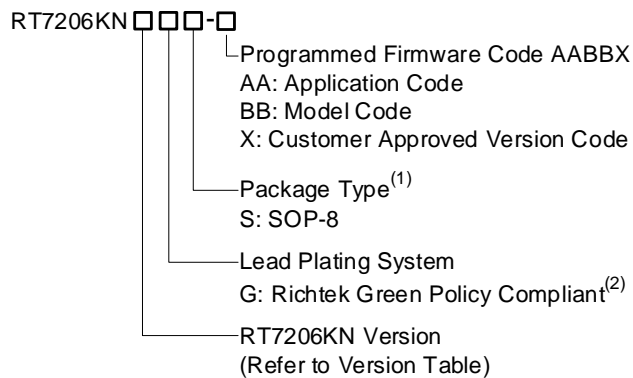
# Highly-Integrated USB Type-C Power Delivery Controller with Built-In Blocking N-MOSFET

## 1 General Description

The RT7206KNx series is a USB Type-C Power Delivery (PD) controller, that mainly utilized in the secondary side for off-line AC-DC power converters. Through the high integration of control regulators and built-in blocking N-MOSFET, more compact designs are easily implemented. The embedded MCU solution and Bi-phase Mark Coding (BMC) Transmitter are incorporated to handle PD Protocol. Furthermore, the digital-to-analog (DAC) and analog-to-digital (ADC) converters are introduced to achieve high-precision control in various applications.

The recommended junction temperature range is -40°C to 125°C, and the ambient temperature range is -40°C to 105°C.

## 2 Ordering Information



**Note 1.**

- Marked with <sup>(1)</sup> indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with <sup>(2)</sup> indicated: Richtek products are Richtek Green Policy compliant.

## 3 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

## 4 Features

- **Protocol Support**
  - USB PD3.0 and PPS
- **High Integration**
  - Wide Operating Range from 3.3V to 21V
  - Built-In Shunt Regulator for Constant-Voltage and Constant-Current Regulations
  - Built-In Blocking N-MOSFET
  - Built-In Quick Discharge in VDD and VBUS
  - Built-In VCONN Power and Switch
  - Linear Cable Compensation
  - Power-Saving Mode Supported
  - Embedded MCU with 16kB OTP-ROM
  - Embedded BMC Transmitter
- **Protection**
  - VDD Adaptive Overvoltage Protection (OVP)
  - VDD Adaptive Undervoltage Protection (UVP)
  - VBUS Short-Circuit Protection (SCP)
  - CC1/CC2 Overvoltage Protection (IO OVP)
  - Overcurrent Protection (OCP)
  - Over-Temperature Protection (OTP)

## 5 Applications

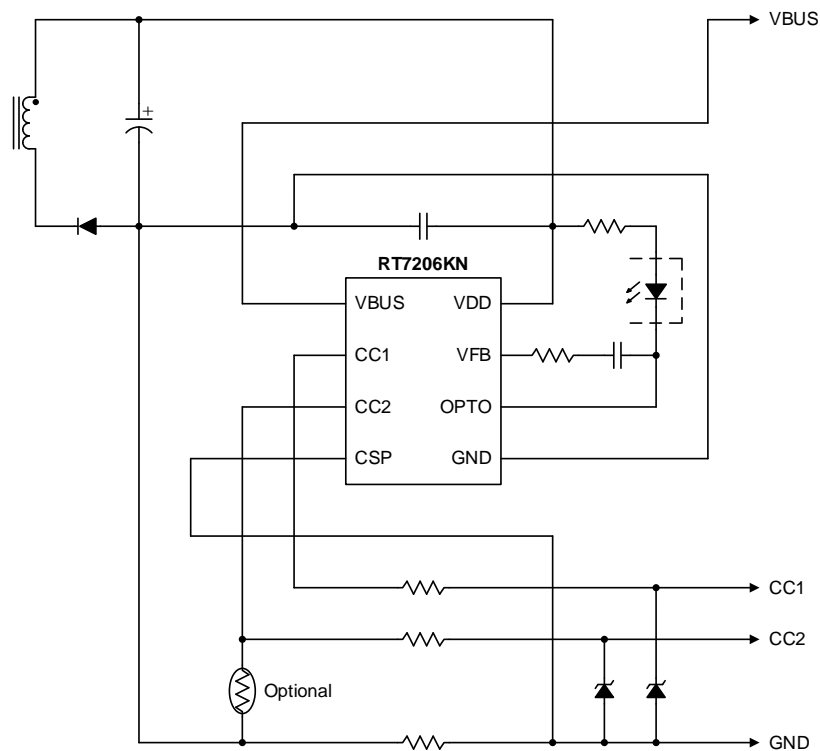
- USB Type-C PD Controller in Source Application for Chargers/Adapters of Smartphone, Tablet, Notebook, and Other Electronics
- USB Type-C PD Controller in Sink Application for IoT Devices of Power Over Ethernet, Smart Speaker, Projector, and Other Electronics

6 RT7206KN Version Table

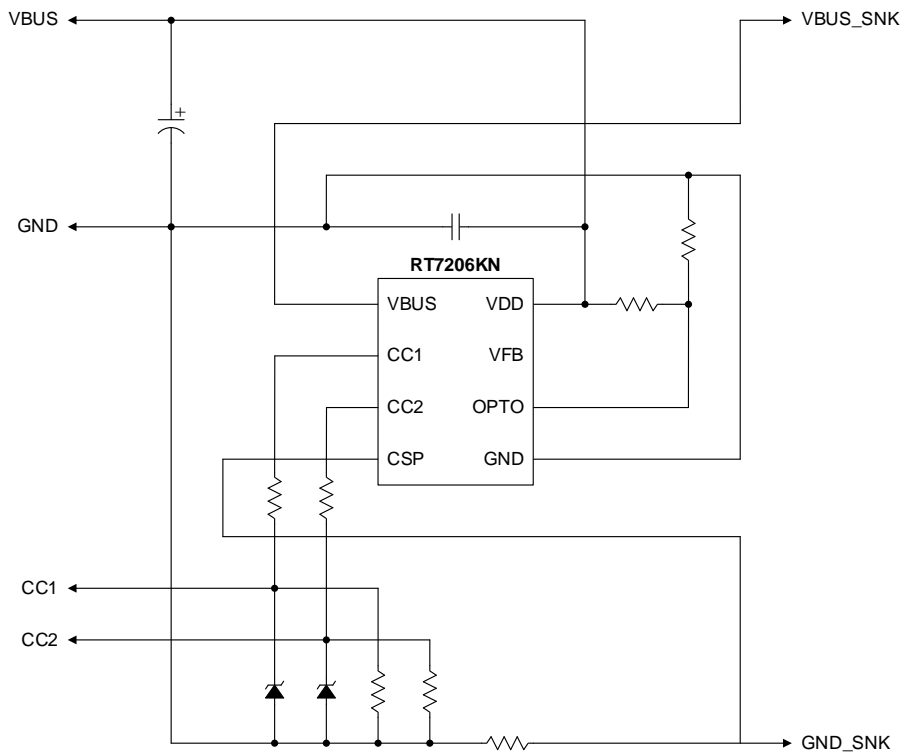
Version	RT7206KN	RT7206KNC
Operating Range	3.3V to 21V	3.3V to 21V
CC1/CC2 Configuration	O	CC1 Only
Constant-Current Regulation	X	O
Package Type	SOP-8	SOP-8

7 Simplified Application Circuit

7.1 RT7206KN Simplified Circuit for Source Application



**7.2 RT7206KN Simplified Circuit for Sink Application**



**7.3 RT7206KNC Simplified Circuit for Source Application**

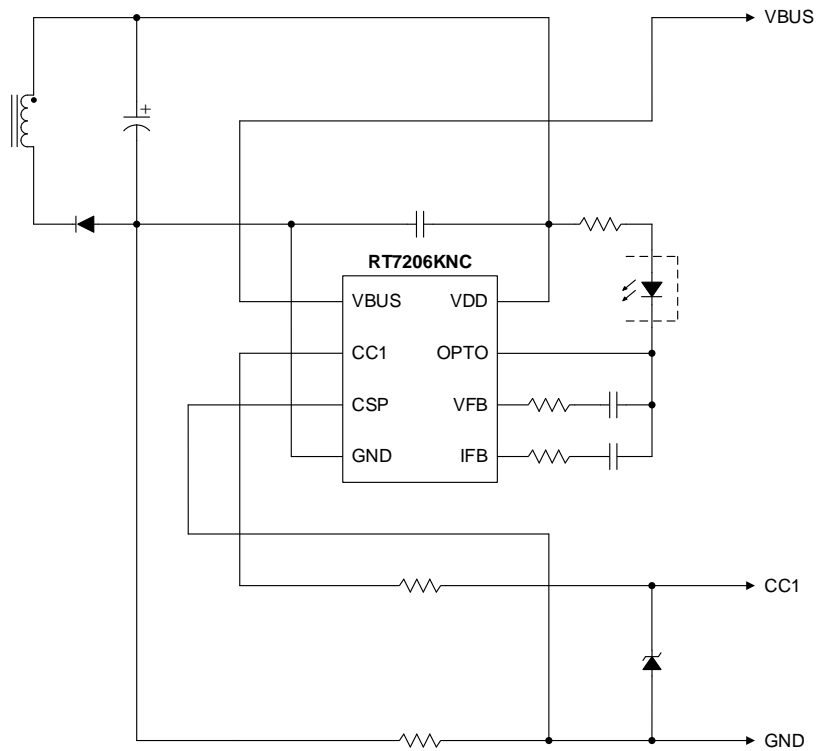
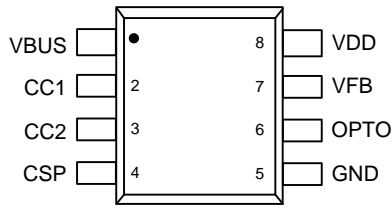


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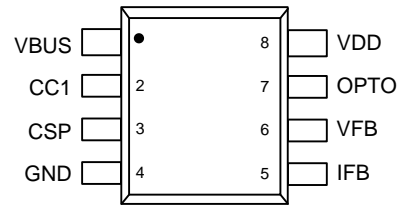
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## 8 Pin Configuration

(TOP VIEW)



SOP-8 (RT7206KN)



SOP-8 (RT7206KNC)

## 9 Functional Pin Description

### 9.1 RT7206KN

Pin No.	Pin Name	Type	Pin Function
1	VBUS	PWR	Source terminal of blocking N-MOSFET
2	CC1	A/D IO	Type-C connector Configuration Channel 1, used to detect cable-plug event, determine the cable orientation, and supply VCONN power
3	CC2	A/D IO	Type-C connector Configuration Channel 2, used to detect cable-plug event, determine the cable orientation, and supply VCONN power
4	CSP	A I	Positive input of current-sense amplifier for sensing output current
5	GND	GND	Ground
6	OPTO	A/D IO	Current-sink output connected to optocoupler
7	VFB	A I	Feedback input for constant-voltage loop
8	VDD	PWR	Supply input voltage and Drain terminal of blocking N-MOSFET

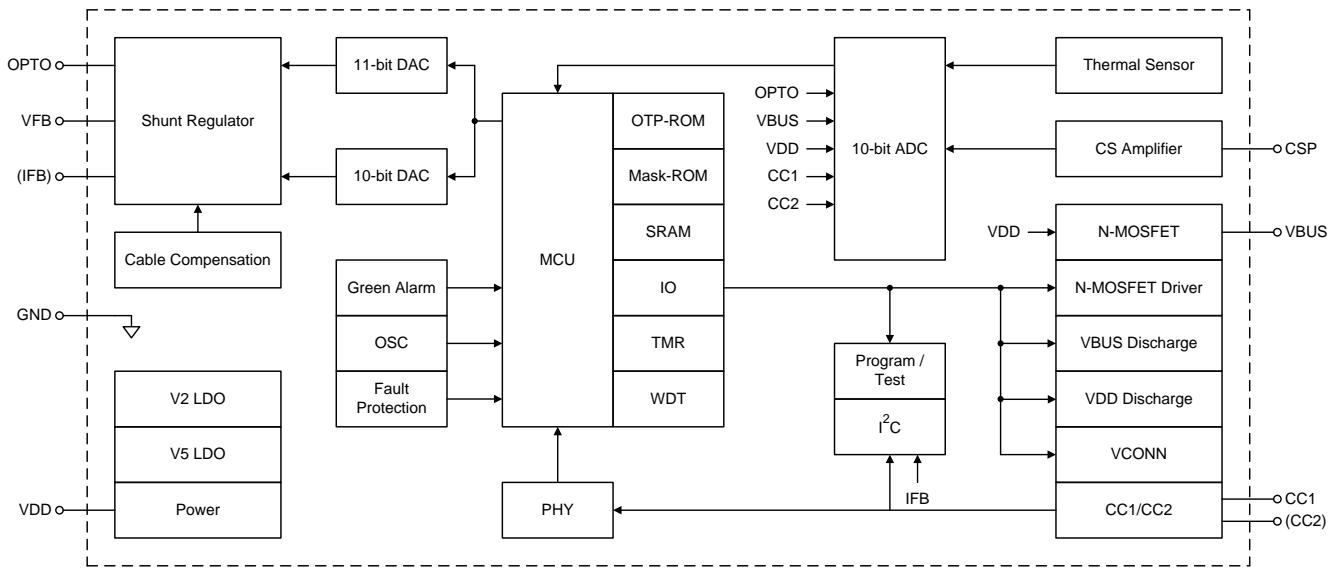
### 9.2 RT7206KNC

Pin No.	Pin Name	Type	Pin Function
1	VBUS	PWR	Source terminal of blocking N-MOSFET
2	CC1	A/D IO	Type-C connector Configuration Channel 1, used to detect cable-plug event, determine the cable orientation, and supply VCONN power
3	CSP	A I	Positive input of current-sense amplifier for sensing output current
4	GND	GND	Ground
5	IFB	A I	Feedback input for constant-current loop
6	VFB	A I	Feedback input for constant-voltage loop
7	OPTO	A/D IO	Current-sink output connected to optocoupler
8	VDD	PWR	Supply input voltage and Drain terminal of blocking N-MOSFET

### 9.3 IO Type Definition

- PWR: Power Pin
- GND: Ground Pin
- A I: Analog Input Pin
- A/D IO: Analog/Digital Input/Output Pin

10 Functional Block Diagram



## 11 Absolute Maximum Ratings

(Note 2)

- VDD, VBUS, OPTO to GND ----- -0.3V to 28V
- VFB, IFB, CC1, CC2, CSP to GND ----- -0.3V to 6.5V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C  
   SOP-8----- 0.38W
- Package Thermal Resistance (Note 3)  
   SOP-8, θ<sub>JA</sub>----- 261.1°C/W  
   SOP-8, θ<sub>JC</sub>----- 47°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10sec.)----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)  
   HBM (Human Body Model) ----- 2kV

**Note 2.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 3.** θ<sub>JA</sub> is measured under natural convection (still air) at T<sub>A</sub> = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ<sub>JC</sub> is measured at the exposed pad of the package.

**Note 4.** Devices are ESD sensitive. Handling precautions are recommended.

## 12 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, V<sub>DD</sub>----- 3.3V to 21V
- Supply Input Current, I<sub>DD</sub> (Based on T<sub>J</sub> < 125°C)----- 0A to 4A
- Junction Temperature Range----- -40°C to 125°C
- Ambient Temperature Range----- -40°C to 105°C

**Note 5.** The device is not guaranteed to function outside its operating conditions.

## 13 Electrical Characteristics

(T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>VDD Section</b>						
VDD Turn-On Threshold	V <sub>VDD_ON</sub>		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V <sub>VDD_OFF</sub>		2.8	2.85	2.9	V
VDD Start-Up Current	I <sub>VDD_START</sub>	V <sub>DD</sub> = 2.8V	50	100	150	μA
VDD Nominal Current	I <sub>VDD_NOM</sub>	V <sub>DD</sub> = 5V	3	4	5	mA
VDD Idle-Mode Current	I <sub>VDD_IDLE</sub>	V <sub>DD</sub> = 5V	1	1.5	2	mA
VDD Green-Mode Current	I <sub>VDD_GREEN</sub>	V <sub>DD</sub> = 5V	500	650	800	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Maximum Overvoltage Protection Threshold	V <sub>VDD_MAXOVP</sub>		23	24	25	V
VDD Adaptive Overvoltage Protection Threshold	V <sub>VDD_OVP</sub>	(Enable/Disable) (Note 7)	105	110	115	%
			110	115	120	
			115	120	125	
VDD Overvoltage Protection Deglitch	t <sub>VDD_OVP</sub>	(Note 6)	25	30	35	μs
VDD Adaptive Undervoltage Protection Threshold	V <sub>VDD_UVP</sub>	(Enable/Disable) (Note 7)	80	85	90	%
			85	90	95	
VDD Undervoltage Protection Deglitch	t <sub>VDD_UVP</sub>	(Note 6)	30	50	70	μs
VDD Threshold for CC1/CC2 Overvoltage Protection	V <sub>VDD_IOOVP</sub>		5.75	6	6.25	V
VDD Constant-Discharge Current	I <sub>DIS_VDD</sub>	V <sub>VDD</sub> > 3.3V (Note 7)	63	90	117	mA
			84	120	156	
			120	150	180	
			150	180	210	
<b>VFB/IFB/OPTO Regulator Section</b>						
VFB Resistor Divider for Voltage Feedback	R <sub>VFB</sub>	R <sub>VFB</sub> = R <sub>VFB1</sub> + R <sub>VFB2</sub> R <sub>VFB1</sub> : VDD to VFB R <sub>VFB2</sub> : VFB to GND	294	420	546	kΩ
VFB Resistor Divider Scaling Factor for Voltage Feedback	K <sub>VFB</sub>		9.9	10	10.1	--
Standby Reference Voltage for CV Regulator	V <sub>REF_CV_ST</sub>		0.485	0.5	0.515	V
Typical Reference Voltage from DAC for CV Regulator	V <sub>REF_CV</sub>		0.152	--	2.2	V
Typical Reference Voltage from DAC for CC Regulator	V <sub>REF_CC</sub>	V <sub>VDD</sub> > 3.3V	0	--	1.5	V
Ratio of Change in Reference Voltage to Change in OPTO Voltage	ΔV <sub>REF</sub> /ΔV <sub>OPTO</sub>	V <sub>OPTO</sub> = 25V to V <sub>REF</sub> (Note 6)	-2.4	-1.2	-0.1	mV/V
OPTO Dynamic Impedance	Z <sub>OPTO</sub>	V <sub>OPTO</sub> = V <sub>REF</sub> , I <sub>OPTO</sub> = 1mA, f < 1kHz (Note 6)	0.1	0.22	0.5	Ω
OPTO Turn-On Sinking Current Capability	I <sub>OPTO_ON</sub>	V <sub>VDD</sub> = 5V, V <sub>OPTO</sub> = 3V (Note 6)	0	--	120	mA
OPTO Turn-On Impedance	R <sub>OPTO_ON</sub>	I <sub>OPTO</sub> = 20mA	1	--	200	Ω
OPTO Pull-Up Impedance	R <sub>p_OPTO</sub>	OPTO shorted to VDD (Enable/Disable)	1	--	200	Ω
OPTO Pull-Down Impedance	R <sub>d_OPTO</sub>	OPTO shorted to GND (Enable/Disable)	1	--	200	Ω



Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>CSP Section</b>						
Current-Sense Amplifier Gain	Kcs	(Note 7)	19.8	20	20.2	V/V
			29.7	30	30.3	
Current-Sense Amplifier Output Offset Voltage	VCS_OFFSET		0.36	0.4	0.44	V
Current-Sense Amplifier Unit-Gain Bandwidth		(Note 6)	1000	--	5000	kHz
Current-Sense Amplifier Output Threshold for Exiting Power-Saving Mode	VCS_PSM_EX	VCS_PSM_EX = VCSP x KCS + VCS_OFFSET (Enable/Disable) (Note 7)	0.41	0.45	0.49	V
			0.51	0.55	0.59	
Cable-Compensation Resistance	RCABLE_COMP	(Enable/Disable) (Note 7)	40	50	60	mΩ
			65	75	85	
			90	100	110	
			105	125	145	
			130	150	170	
			180	200	220	
			230	250	270	
Cable-Compensation Transconductance Amplifier Bandwidth		(Note 6)	20	--	65	kHz
<b>CC1/CC2 Section</b>						
CC1/CC2 Open-Circuit Voltage	VCC_OC	VDD > 5V	2.9	3.25	3.6	V
CC1/CC2 Leakage Current	ICC_LK	VDD = 0V, VCC = 5V	0	--	0.2	μA
CC1/CC2 Cable-Detached Threshold	VCC_CD		2.5	2.6	2.7	V
CC1/CC2 Overvoltage Protection Threshold	VCC_OVP	(Note 7)	4.2	4.35	4.5	V
			3.85	4	4.15	
CC1/CC2 Overvoltage Protection Debounce	tCC_OVP	(Note 6) (Note 7)	0.095	0.1	0.105	ms
			0.95	1	1.05	
CC1/CC2 Sourcing Current Source	ISRC_CC	VDD > VVDD_ON (Enable/Disable) (Note 7)	76	80	84	μA
			171	180	189	
			304	330	356	
CC1/CC2 BMC Transmitter Tx Output-High Voltage	VOH_CC		1.05	1.125	1.2	V
CC1/CC2 BMC Transmitter Tx Output-Low Voltage	VOL_CC		0	0.0375	0.075	V
CC1/CC2 BMC Transmitter Tx Rise Time	trISE_CC	CLOAD < 470pF	300	--	700	ns
CC1/CC2 BMC Transmitter Tx Fall Time	tfALL_CC	CLOAD < 470pF	300	--	700	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CC1/CC2 BMC Transmitter Rx Input-High Voltage	V <sub>IH_CC</sub>	(Note 7)	0.8	0.9	1.0	V
			0.7	0.8	0.9	
			0.6	0.7	0.8	
			0.5	0.6	0.7	
CC1/CC2 BMC Transmitter Rx Input-Low Voltage	V <sub>IL_CC</sub>	(Note 7)	V <sub>IH_CC</sub> - 0.1	V <sub>IH_CC</sub> - 0.1	V <sub>IH_CC</sub> - 0.1	V
CC1/CC2 VCONN Voltage	V <sub>CONN</sub>	V <sub>DD</sub> = 5V, I <sub>VCONN</sub> = 0mA	3.8	4	4.2	V
		V <sub>DD</sub> = 5V, I <sub>VCONN</sub> = 30mA	3.3	--	3.5	
CC1/CC2 VCONN Short-Circuit Current	I <sub>VCONN_SC</sub>		45	70	95	mA
<b>VBUS Section</b>						
VBUS Built-In Blocking N-MOSFET Turn-On Resistance	R <sub>ON_VBUS</sub>	V <sub>GS</sub> = 10V, I <sub>DS</sub> = 4A @ T <sub>C</sub> = 25°C Measured between V <sub>DD</sub> and V <sub>BUS</sub>	11	12.2	13.4	mΩ
		V <sub>GS</sub> = 10V, I <sub>DS</sub> = 4A @ T <sub>C</sub> = 105°C Measured between V <sub>DD</sub> and V <sub>BUS</sub> (Note 6)	15.4	--	18.76	
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V Freq = 1MHz	--	1094	--	pF
Output Capacitance	C <sub>oss</sub>					
Reverse Transfer Capacitance	C <sub>rss</sub>					
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>DS</sub> = 250μA, V <sub>GS</sub> = 0V	30	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V	--	--	1	μA
Gate to Source Breakdown Voltage	V <sub>GSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V	-20	--	20	V
Gate Threshold Voltage	V <sub>GS_TH</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>DS</sub> = 250μA	1	--	2.5	V
Body Diode Forward Voltage	V <sub>SD</sub>	I <sub>SD</sub> = 1A, V <sub>GS</sub> = 0V	--	0.7	1.1	V
Revers Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1A, V <sub>R</sub> = 0V	--	14	--	ns
Revers Recovery Charge	Q <sub>rr</sub>	dI <sub>F</sub> /dt = 100A/μs	--	5.6	--	nC
VBUS Short-Circuit Protection Threshold	V <sub>VBUS_SCP</sub>	N-MOSFET driver = ON V <sub>DD</sub> - V <sub>BUS</sub> > V <sub>VBUS_SCP</sub> (Enable/Disable) (Note 7)	0.05	0.15	0.25	V
			0.2	0.3	0.4	
VBUS Short-Circuit Protection Deglitch	t <sub>VBUS_SCP</sub>	(Note 6) (Note 7)	8	10	12	μs
			16	20	24	
VBUS Discharge Impedance	R <sub>DIS_VBUS</sub>	N-MOSFET driver = OFF I <sub>DIS_VBUS</sub> = 20mA	0.7	1	1.3	kΩ

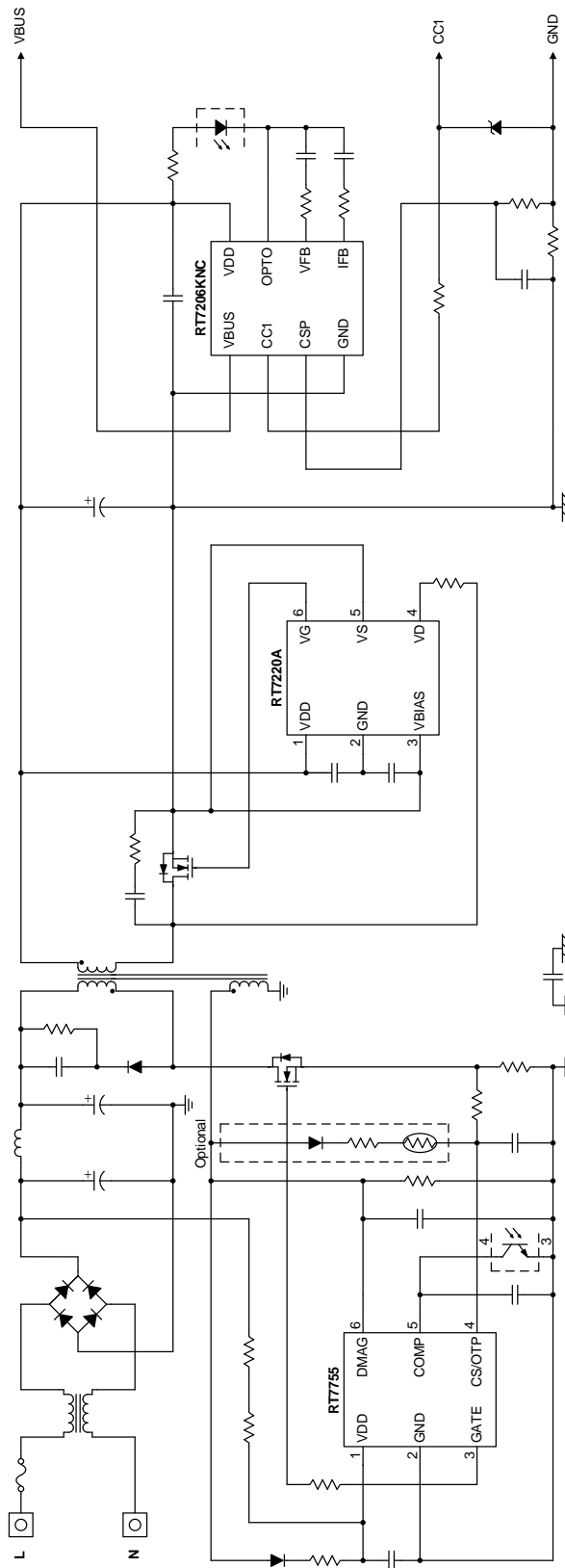
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Accuracy Section</b>						
Voltage Regulation Accuracy	EVOUT	V <sub>OUT</sub> = 3.3V to 21V, I <sub>OUT</sub> = 1A to 4A	-100	--	100	mV
Current Regulation Accuracy	EIOUT	V <sub>OUT</sub> = 3.3V to 21V, I <sub>OUT</sub> = 1A to 4A, RCS = 1% accuracy	-150	--	150	mA
Internal Thermal Sensor Accuracy	ETS	T <sub>C</sub> = -40°C to 105°C	-7	--	7	°C

**Note 6.** Guaranteed by design.

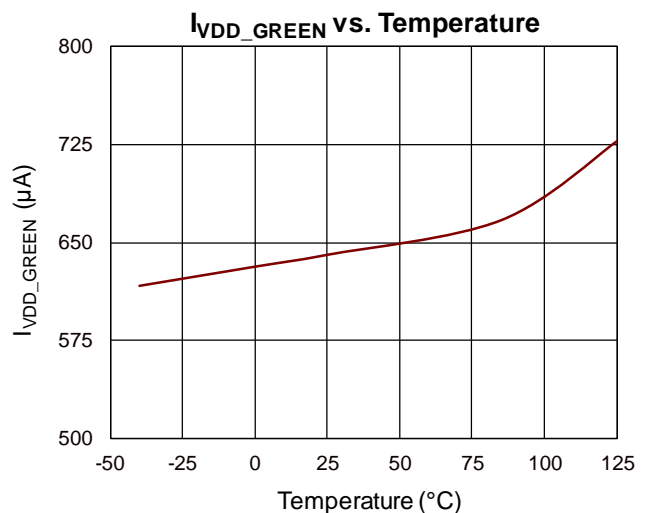
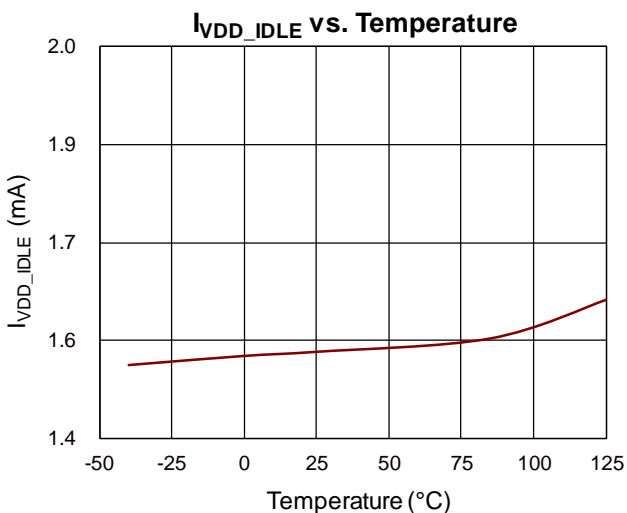
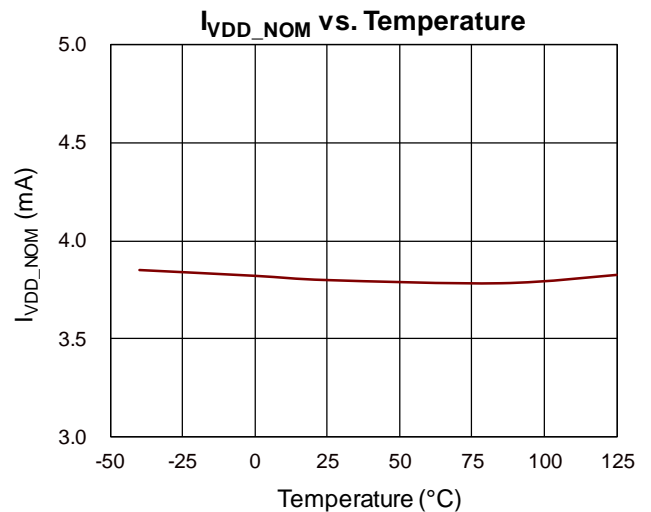
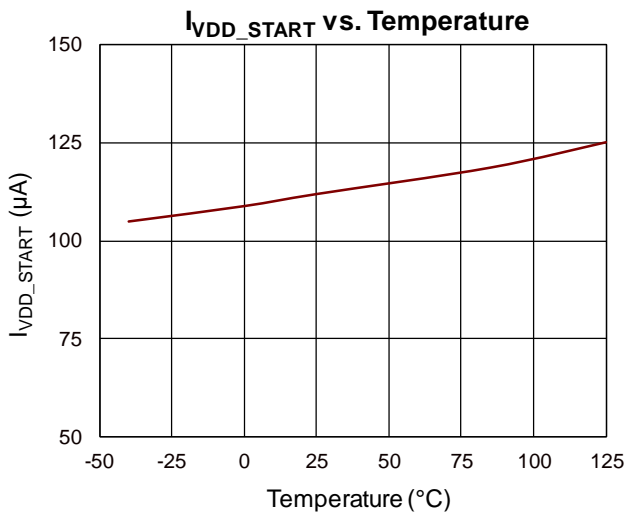
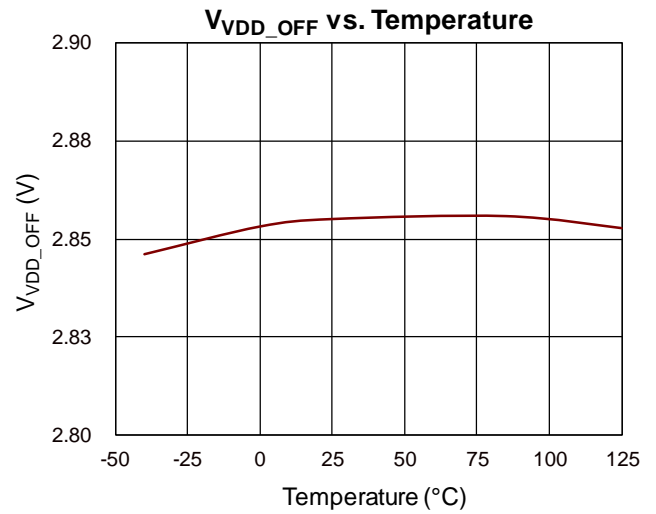
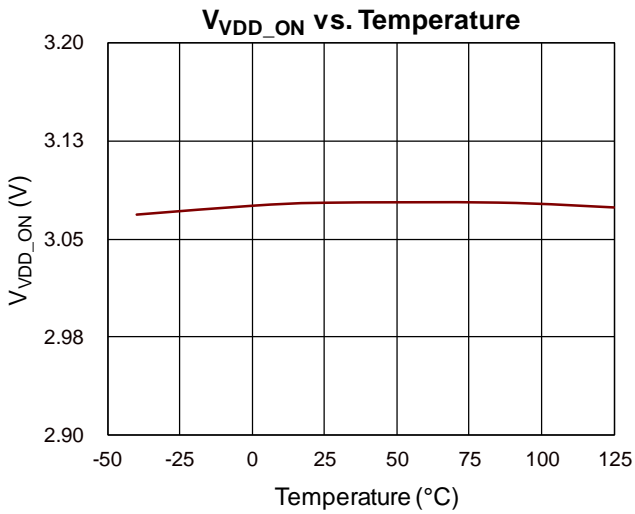
**Note 7.** Register option by OTP program.

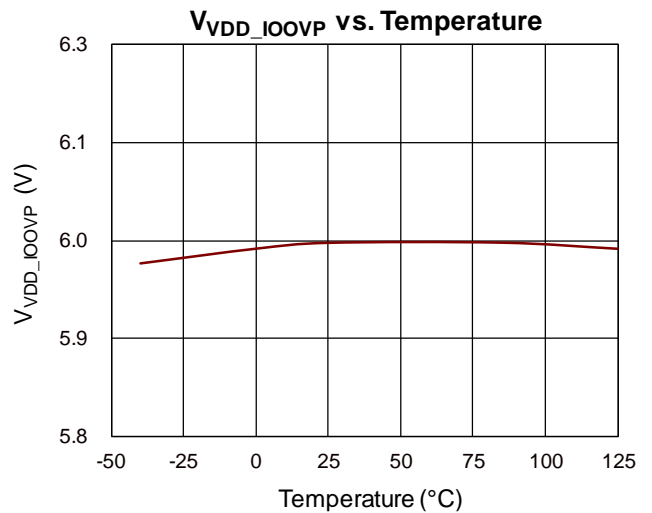
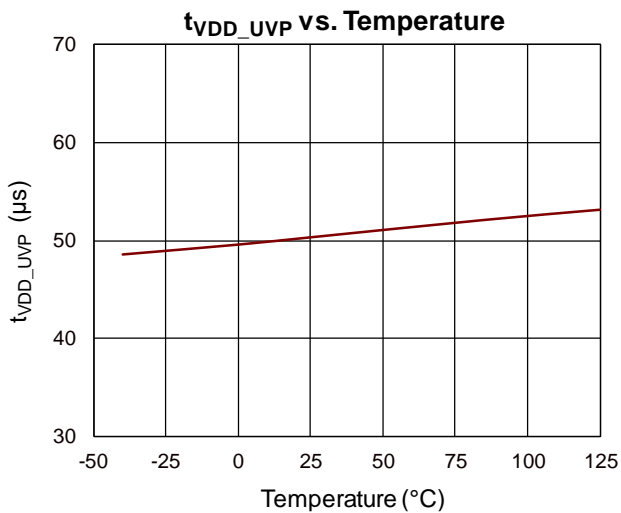
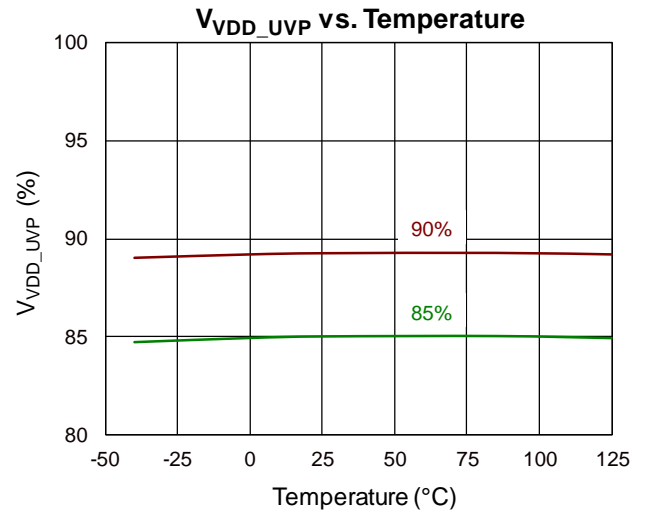
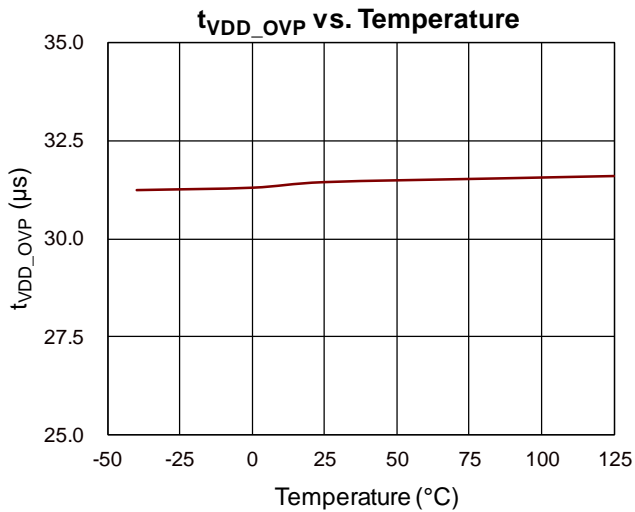
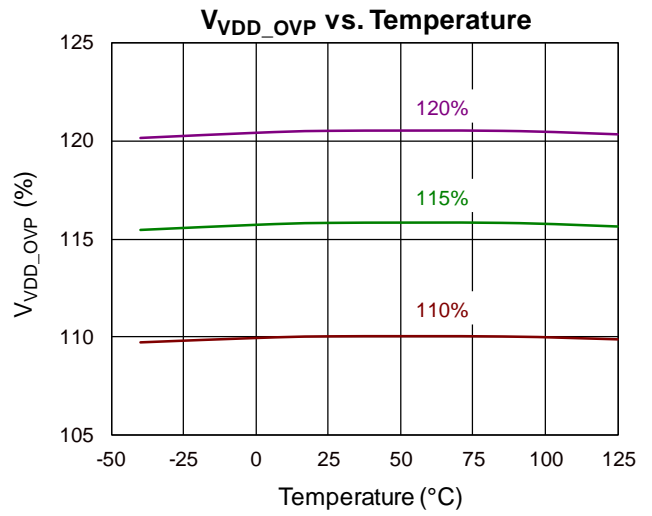
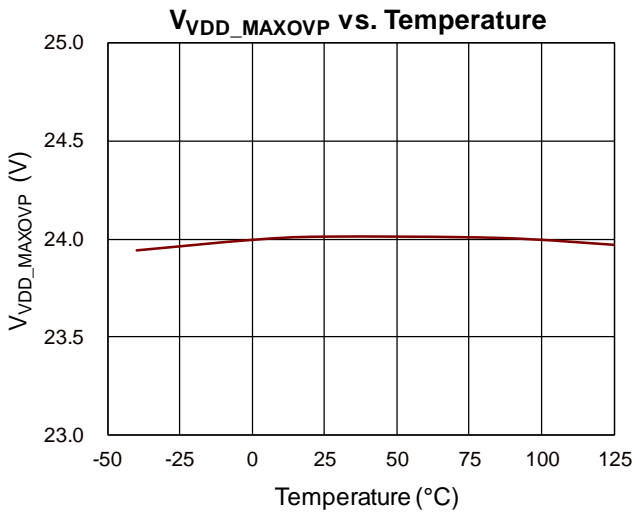


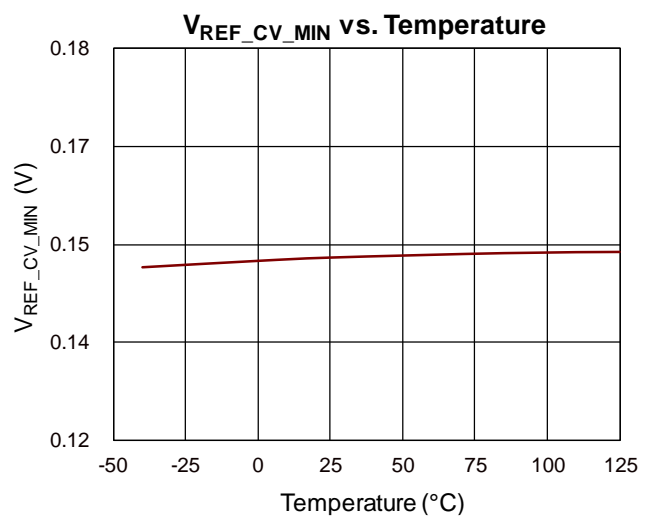
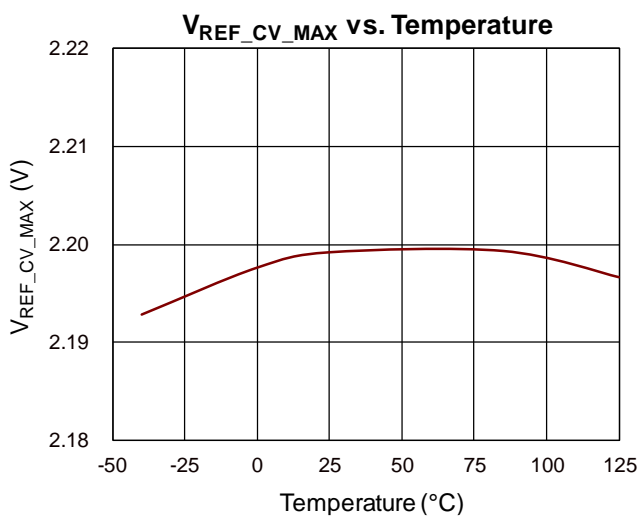
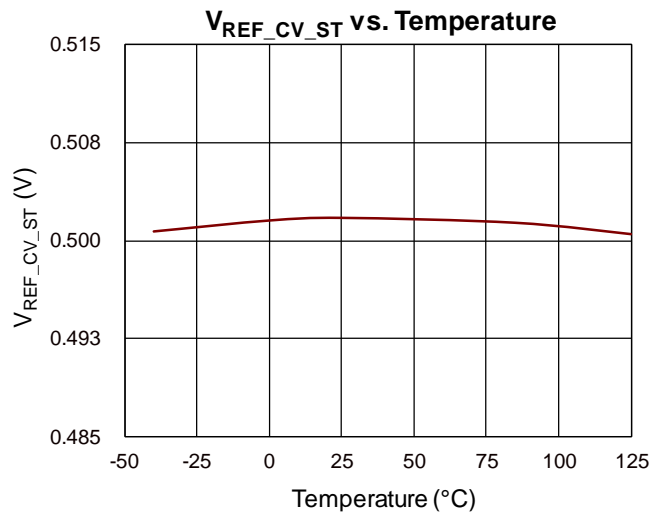
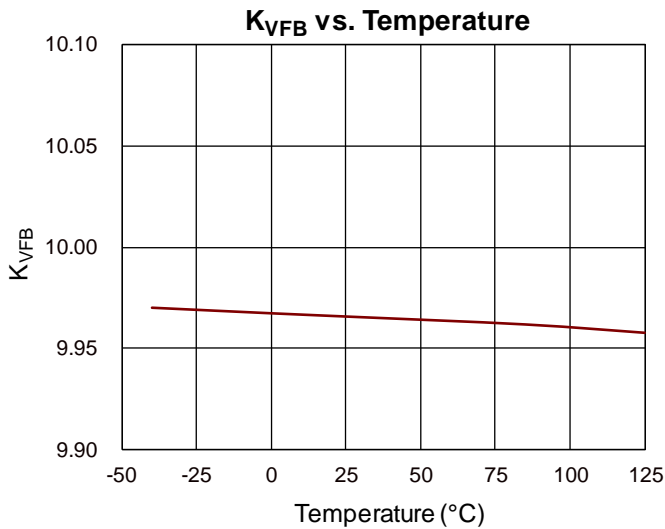
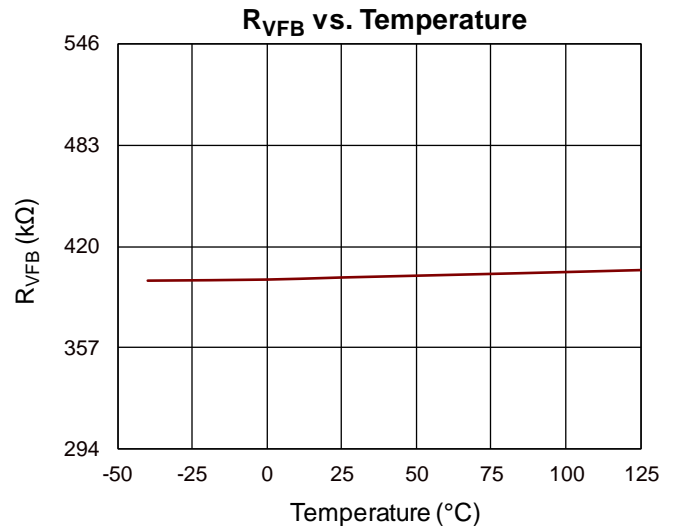
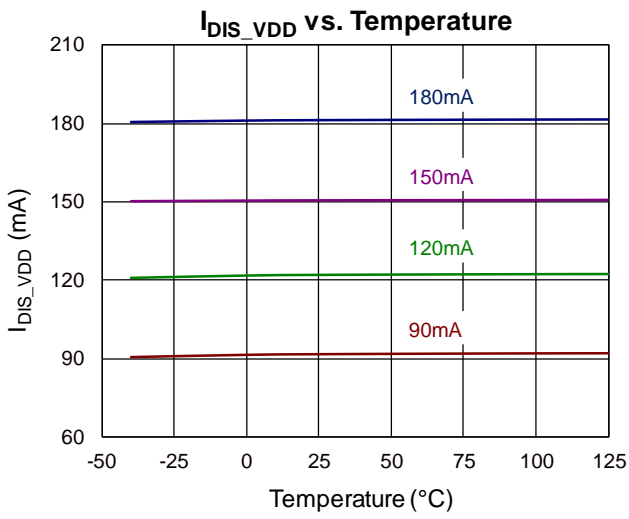
14.2 RT7206KNC Typical Application Circuit



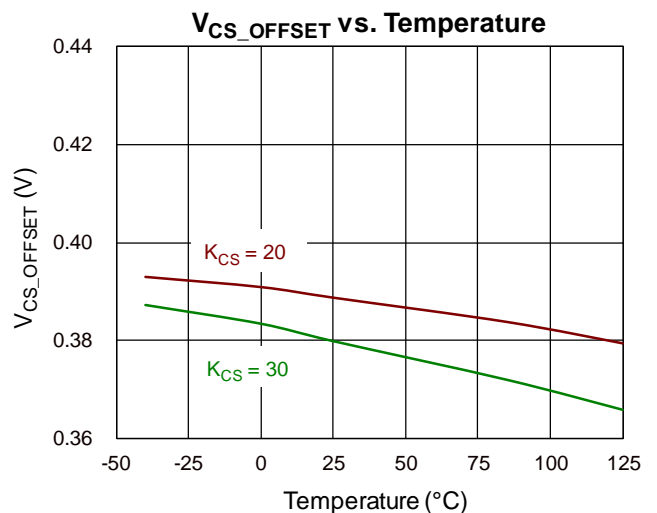
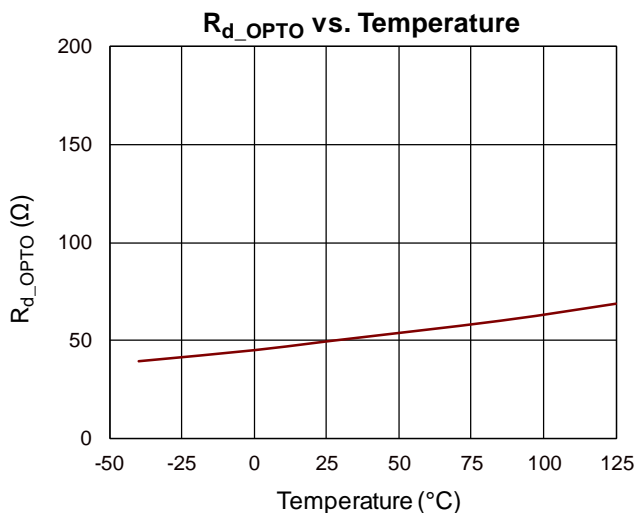
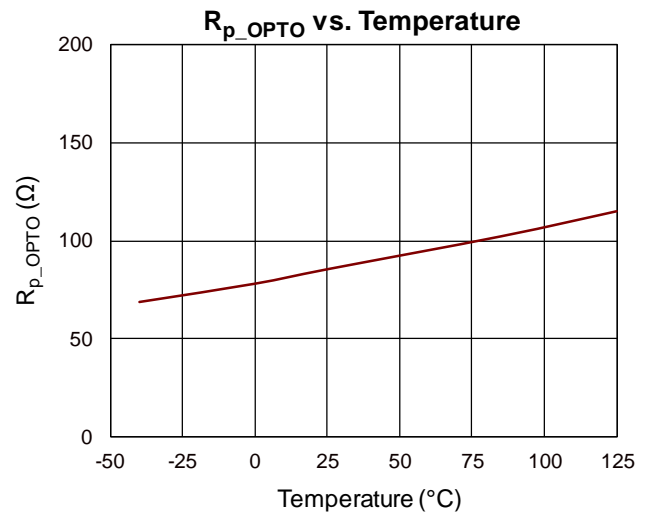
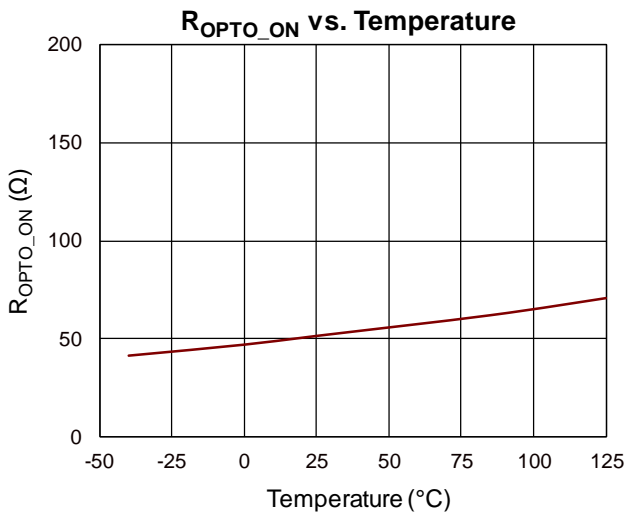
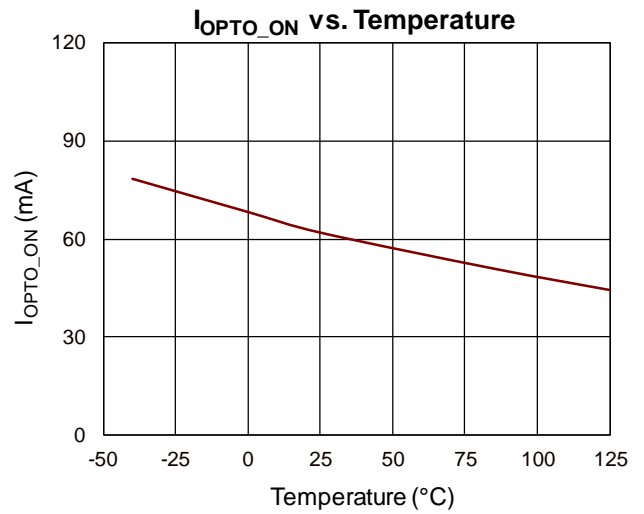
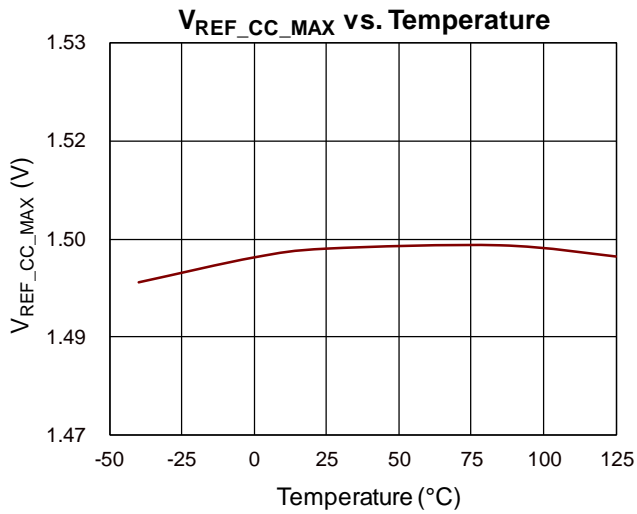
15 Typical Operating Characteristics

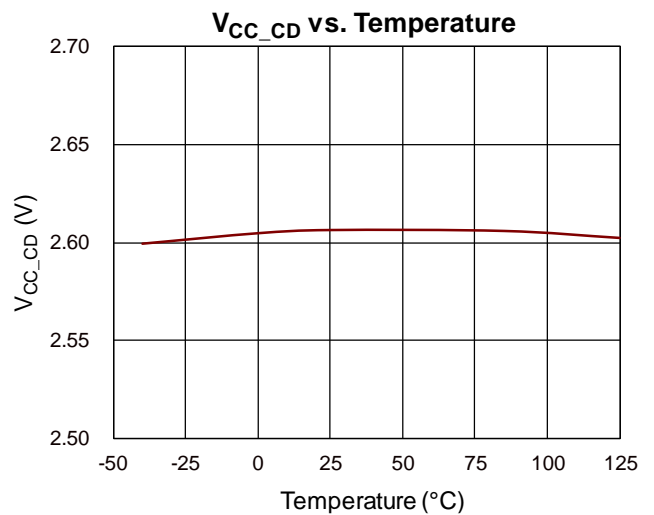
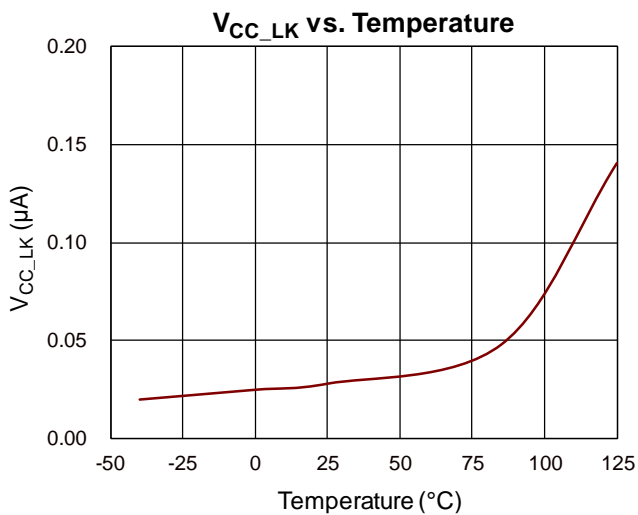
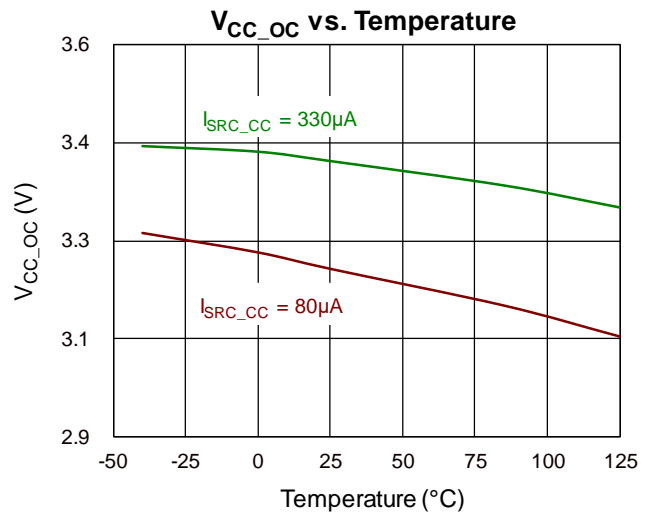
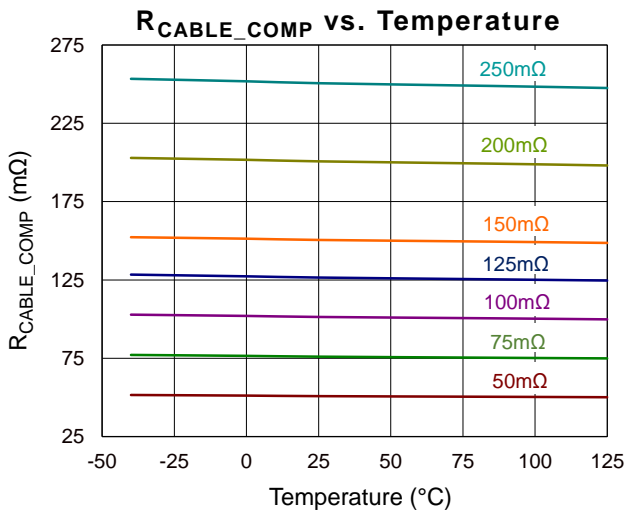
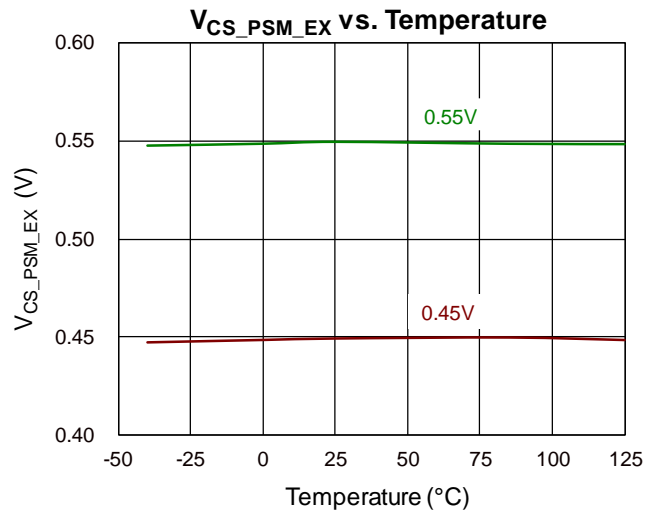
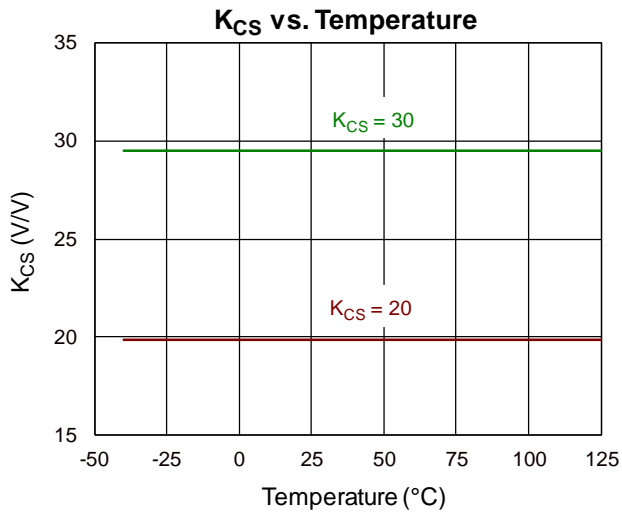


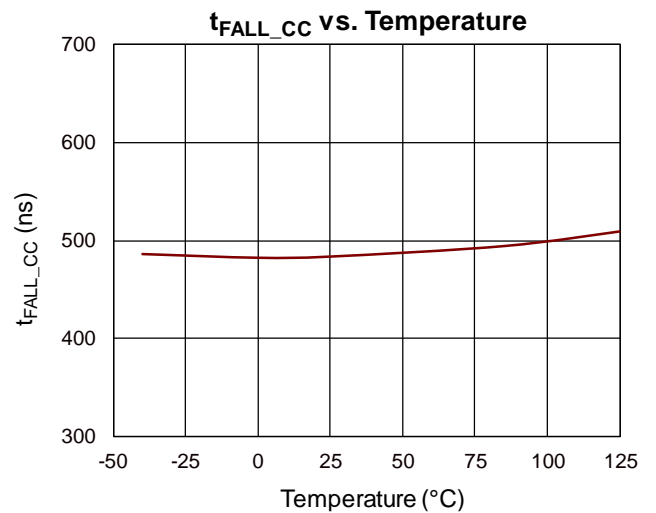
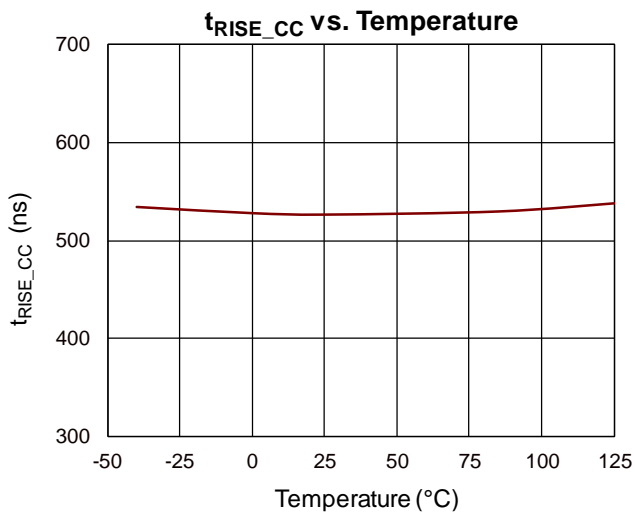
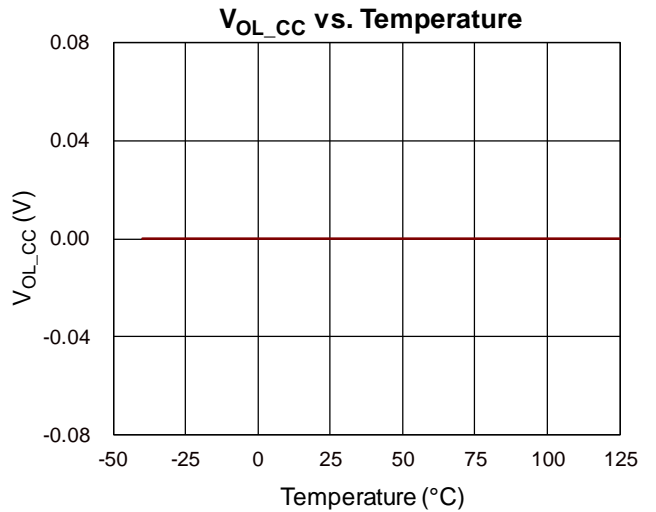
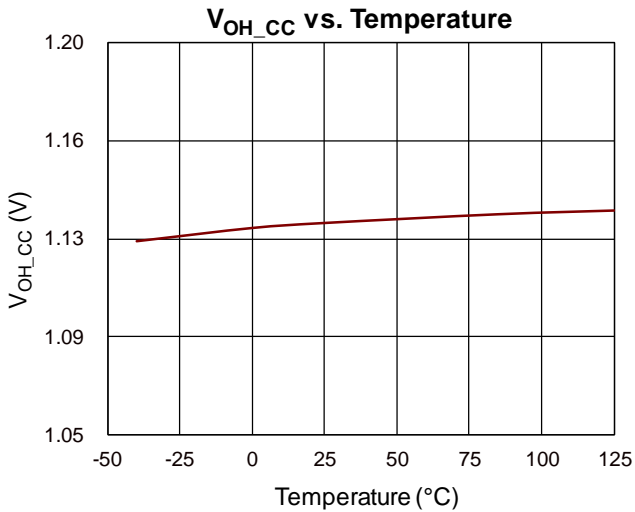
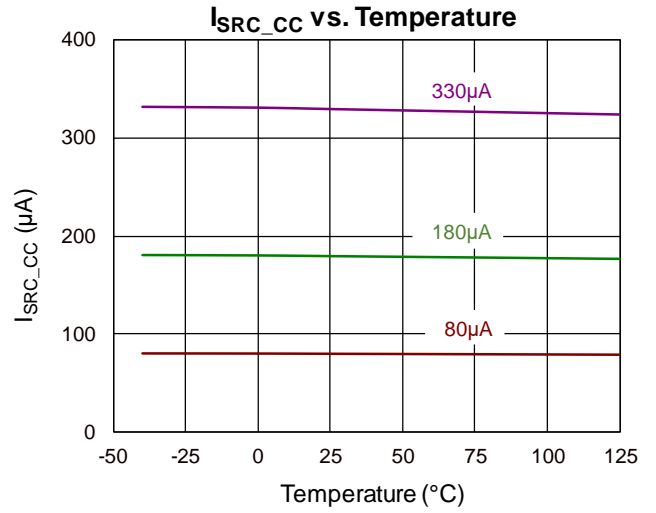
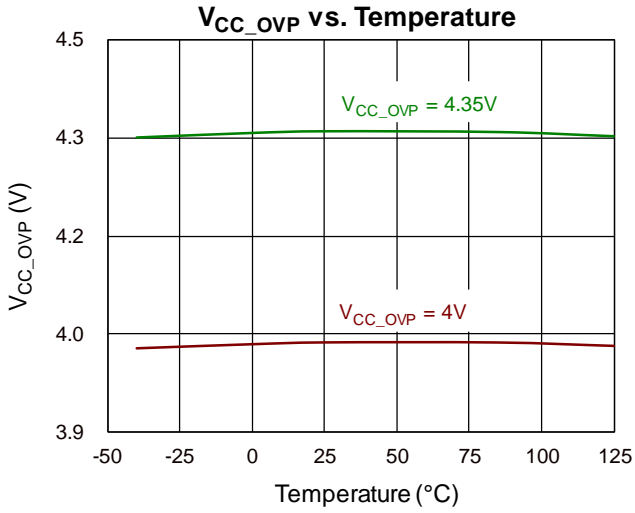


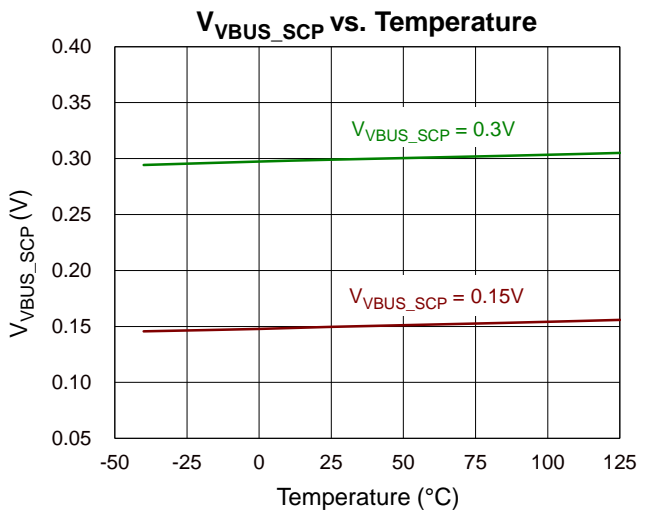
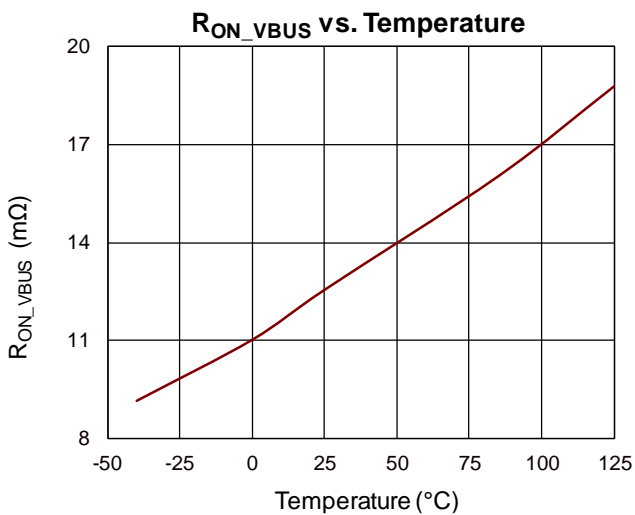
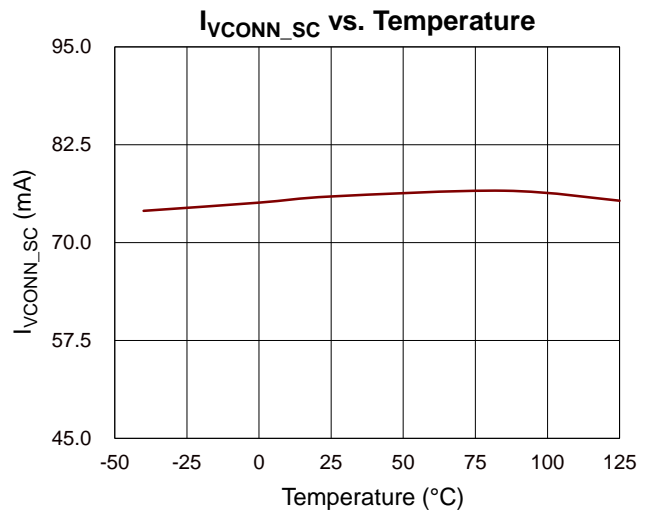
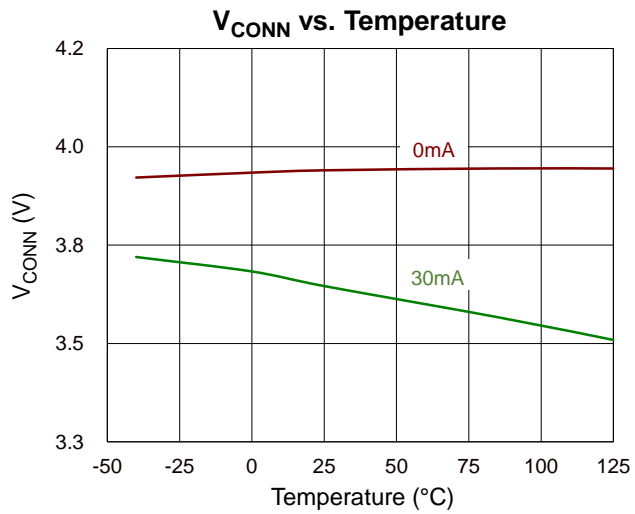
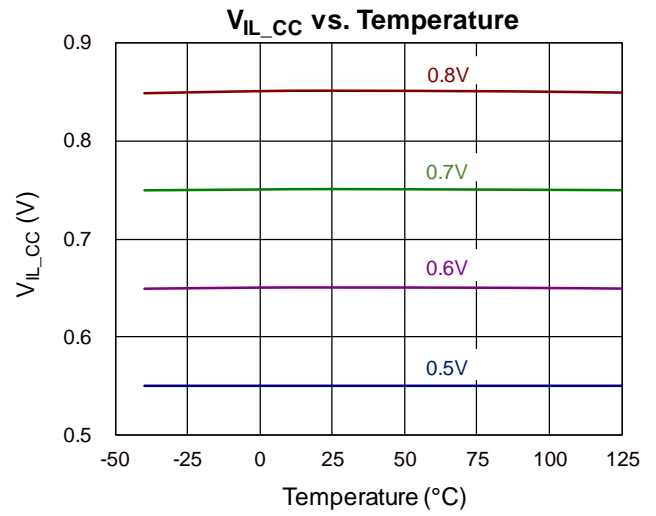
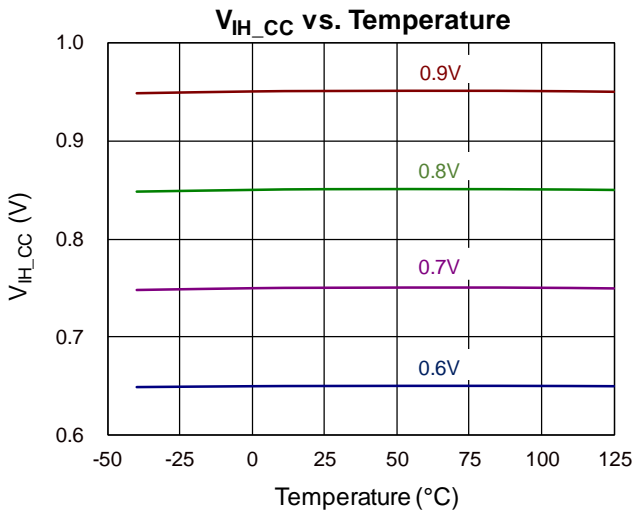


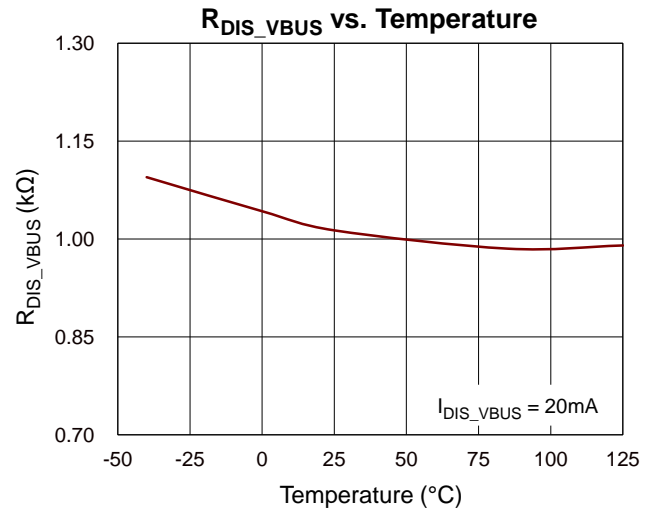
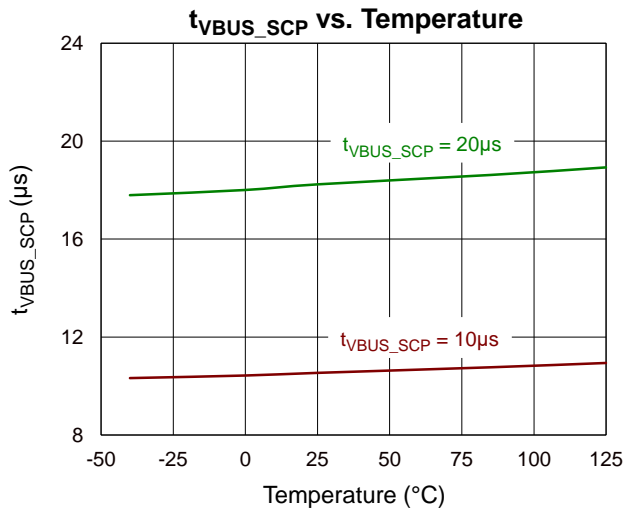












## 16 Operation

### 16.1 Constant-Voltage (CV) and Constant-Current (CC) Regulators in Source Application

The RT7206KNx series integrates a shunt regulator for CV and CC regulations. Both outputs of CV and CC regulators are connected to OPTO in parallel as the analog output. The operation of each feedback loop is similar to that of TL431-based regulator. However, the wider operating range of OPTO, from 0.3V to 25V, improves the design of power converters with a wider output range. If the voltage related to VDD, V<sub>DD</sub>, is still below the turn-on threshold, V<sub>VDD\_ON</sub>, OPTO will keep in high impedance to ensure a soft-start-up sequence. The reference voltages, V<sub>REF\_CV</sub> and V<sub>REF\_CC</sub>, are analog outputs from the embedded DACs which provide 10mV-resolution and 10mA-resolution for each CV and CC regulations.

### 16.2 Capability Selector in Sink Application

When the RT7206KNx series is utilized in a Sink port, OPTO will always keep in high impedance. The embedded ADC resolves the voltage related to OPTO, V<sub>OPTO</sub>, as the analog input. According to the voltage level of V<sub>OPTO</sub>, the RT7206KNx series, will send the request to a Source port to get the correspond capabilities.

### 16.3 Current-Sense Amplifier

The current in the power-ground bus can be sensed by an external current-sense resistor, R<sub>CS</sub>. In order to minimize the power loss of R<sub>CS</sub> and the noise, a differential amplifier with output gain, K<sub>CS</sub>, and output offset, V<sub>CS\_OFFSET</sub>, is integrated.

### 16.4 CC1/CC2 Interface

The specific I/O pins, CC1/CC2, are integrated to handle USB Type-C compliance and PD protocol. When the RT7206KNx series configured as a Source device, the optional current capabilities of 80μA, 180μA, and 330μA, provided by each of CC1 and CC2, will be advertised to a Sink device, implying the USB Type-C current of default, 1.5A, and 3.0A respectively.

## 17 Application Information

(Note 8)

### 17.1 AC-DC Source Port

#### 17.1.1 Voltage Sense and Current Sense

The RT7206KNx series integrates a resistor divider,  $R_{VFB}$ , for voltage feedback as shown in [Figure 1](#). The voltage related to  $V_{DD}$ ,  $V_{DD}$  is determined as:

$$V_{DD} = K_{VFB} \times V_{VFB}$$

$$K_{VFB} = (R_{VFB1} + R_{VFB2}) / R_{VFB2} = 10$$

The RT7206KNx series also integrates a differential amplifier so that the sensed current,  $I_{CS}$ , through the current-sense resistor,  $R_{CS}$ , is determined as:

$$I_{CS} = (V_{IFB} - V_{CS\_OFFSET}) / (R_{CS} \times K_{CS})$$

#### 17.1.2 Constant-Voltage (CV) and Constant-Current (CC) Regulations

For the CV loop,  $V_{DD}$  is determined by the reference voltage of CV regulator,  $V_{REF\_CV}$ . For the CC loop,  $I_{CS}$  is determined by the reference voltage of CC regulator,  $V_{REF\_CC}$ . Two loops incorporate an error amplifier respectively and both of them are connected to OPTO, driving the sinking current from the external circuit with an optocoupler and a resistor,  $R_D$ , in series to  $V_{DD}$ . The optocoupler transfers the compensation signal from the secondary side to the primary side. Note that for better linearity of the compensation range,  $R_D$  is suggested to be designed for satisfying the maximum COMP current of PWM controller,  $I_{COMP\_MAX}$ , at the minimum voltage related to  $V_{DD}$ ,  $V_{DD\_MIN}$ .

$$\frac{(V_{DD\_MIN} - V_F - 0.3V)}{R_D} \times CTR \geq I_{COMP\_MAX}$$

CTR: Current transfer ratio of the optocoupler

$V_F$ : Forward voltage of the optocoupler

0.3V: The threshold of OPTO voltage for driving the minimum OPTO sinking current

#### 17.1.3 Linear Cable Compensation

A transconductance amplifier is integrated for linear cable compensation. The compensation voltage,  $V_{CABLE\_COMP}$ , is determined as:

$$V_{CABLE\_COMP} = I_{CS} \times R_{CABLE\_COMP}$$

In addition, a programmable solution is reserved by ADC-measurement as a proprietary function.

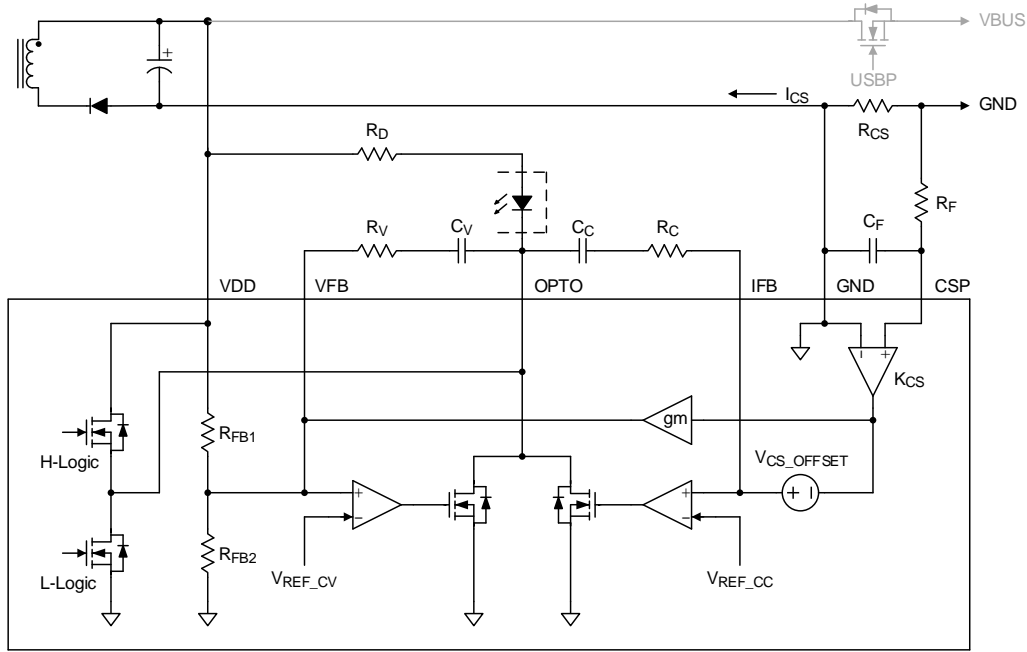


Figure 1. Application Circuit for CV and CC Regulations

**17.1.4 Power Sequence**

When start-up, VREF\_CV is set to the standby reference voltage, VREF\_CV\_ST, and then VDD is regulated to 5V. Once a Type-C cable attached, the Sink port will deliver power request back to the embedded MCU, changing VREF\_CV and regulating VDD to the correspond voltage level. In contrary, once the Type-C cable detached, the embedded MCU will enter power-saving mode and back to 5V.

**17.1.5 Rising and Falling Regulation**

As shown in [Figure 2](#), when PD protocol is detected, VREF\_CV can be set by the request of the Sink port. Both rise and fall time of VDD must meet PD compliance, defined as 275ms. The slope of VREF\_CV during rising interval, SRISE, can be determined as:

$$S_{RISE} \geq \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

VDD\_MAX: Maximum voltage request

VDD\_MIN: Minimum voltage request

275ms: Rise and fall time of PD compliance

25ms: Time margin from transient response of system

During the falling interval, the constant-discharge current, IDIS\_VDD, is enabled. The capability of IDIS\_VDD must take the output capacitors of system, COUT, in consideration. IDIS\_VDD can be determined as:

$$I_{DIS\_VDD} \geq C_{OUT} \times \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

The slope of VREF\_CV during falling interval, SFALL, can be determined as:

$$\frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms} \leq S_{FALL} \leq \frac{I_{DIS\_VDD}}{C_{OUT}}$$



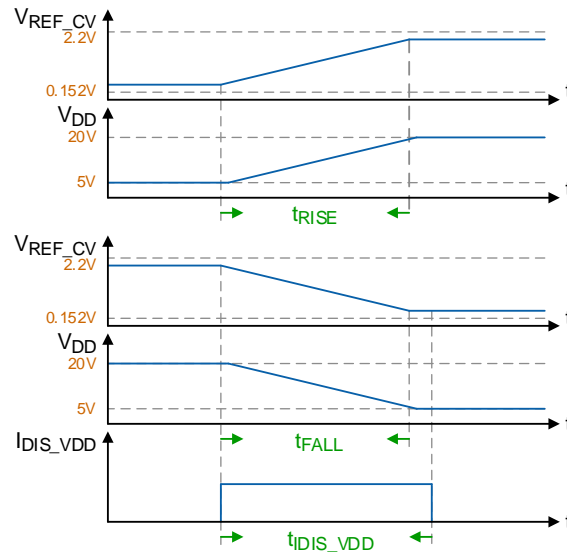


Figure 2. Rising and Falling Regulation

**17.1.6 Programmable Shutdown Flow from Protections**

The RT7206KNx series can achieve multiple behaviors for any abnormal condition occurs.

**17.1.6.1 Auto-Recovery**

Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously  $V_{DD}$  is forced down to  $V_{VDD\_OFF}$  by pulling  $V_{OPTO}$  down. After  $V_{DD}$  turned-off,  $V_{OPTO}$  is released and  $V_{DD}$  is powered up again.

**17.1.6.2 Output-Latch**

Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously  $V_{DD}$  is set back to 5V. To recover the system, the DC cable must be removed and then attached again.

**17.1.6.3 Power-Latch**

Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously  $V_{DD}$  is set back to 5V. After that,  $V_{OPTO}$  is pulled high to trigger the protection from the primary-side PWM controller, which is supposed to be a latch behavior. To recover the system, the AC cable must be removed and then attached again.

**17.1.6.4 Over/Undervoltage Protection (OVP/UVP)**

As shown in [Figure 3](#) and [Figure 4](#), the RT7206KNx series provides a quick-interruption solution to turn off the blocking N-MOSFET when either overvoltage or undervoltage condition occurs in  $V_{DD}$ , such as the malfunction of feedback loop due to aging of the optocoupler. Once  $V_{DD}$  is higher than the overvoltage protection threshold,  $V_{VDD\_OVP}$ , over the deglitch time,  $t_{VDD\_OVP}$ , or  $V_{DD}$  is lower than the undervoltage protection threshold,  $V_{VDD\_UVP}$ , over the deglitch time,  $t_{VDD\_UVP}$ , the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU. Besides, a programmable solution is reserved by ADC-measurement as a proprietary function.

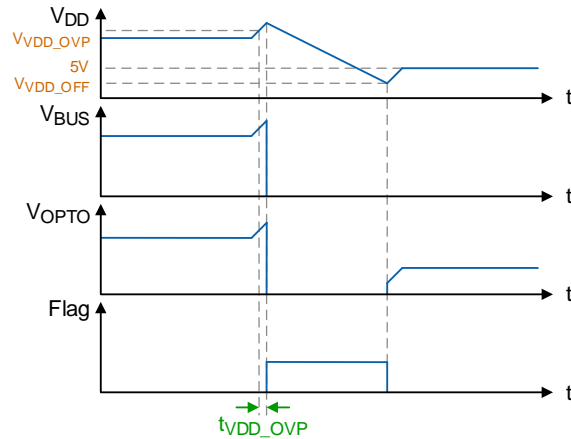


Figure 3. Timing Sequence of OVP with Auto-Recovery

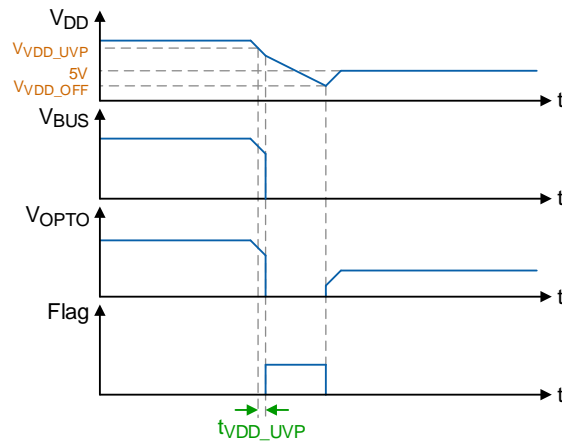


Figure 4. Timing Sequence of UVP with Auto-Recovery

**17.1.6.5 Short-Circuit Protection (SCP)**

As shown in [Figure 5](#), a quick-interruption solution is designed to preventing the damage from short-circuit condition in VBUS. When the situation happens, the voltage difference between VDD and VBUS,  $V_{ON\_VBUS}$ , will Instantaneously rise due to the huge current. Once  $V_{ON\_VBUS}$  is higher than the short-circuit protection threshold,  $V_{VBUS\_SCP}$ , over the deglitch time,  $t_{VBUS\_SCP}$ , the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU.

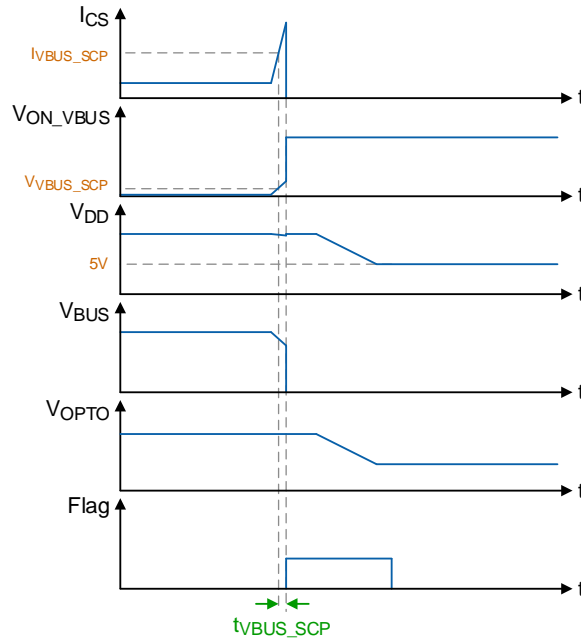


Figure 5. Timing Sequence of SCP with Output-Latch

**17.1.7 CC1/CC2 Overvoltage Protection (IO OVP)**

In order to prevent the damage of CC1/CC2 from the abnormal contact to VBUS at the USB Type-C receptacle, a quick-interruption solution is designed to turn off the blocking N-MOSFET as shown in [Figure 6](#). Once  $V_{DD}$  is higher than the threshold for CC1/CC2 overvoltage protection,  $V_{DD\_IOOVP}$ , and the voltage related to CC1/CC2,  $V_{CC}$  is higher than the CC1/CC2 overvoltage protection threshold,  $V_{CC\_OVP}$ , over the debounce time,  $t_{CC\_OVP}$ , the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU.

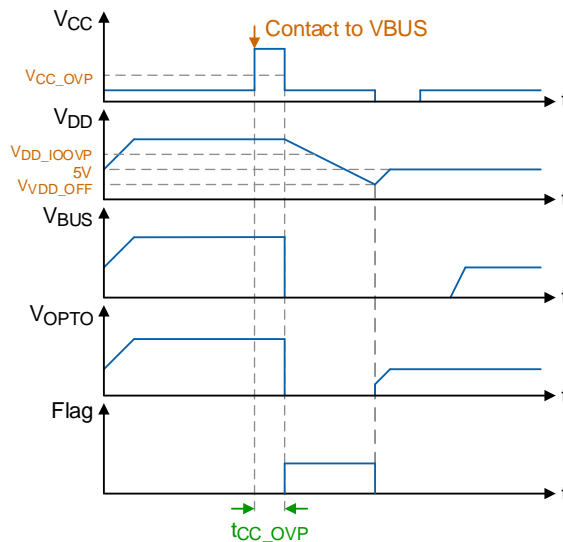


Figure 6. Timing Sequence of CC1/CC2 OVP with Auto-Recovery

17.1.8 Overcurrent Protection (OCP)

The RT7206KNx series provides a programmable solution by ADC-measurement to achieve overcurrent protection as shown in Figure 7. Once  $I_{CS}$  is higher than the programming threshold,  $I_{OCP\_ADC}$ , over a debounce time,  $t_{OCP\_ADC}$ , the programmable shutdown flow will be triggered.

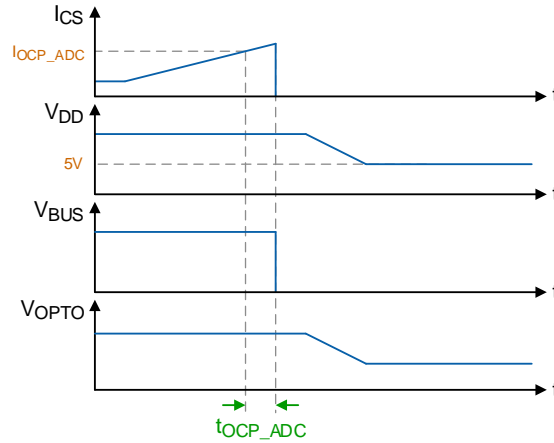


Figure 7. Timing Sequence of OCP with Output-Latch

17.1.9 Over-Temperature Protection (OTP)

A programmable solution by ADC-measurement to achieve over-temperature protection is designed as shown in Figure 8. If any of specific I/O pins, CC1/CC2, can be defined as general purpose I/O, the internal sourcing current source,  $I_{SRC\_CC}$ , will be set to  $80\mu A$ . By using an NTC/PTC connected between CC1/CC2 and GND, the ambient in the specific region can be monitored. Once the voltage related to CC1/CC2,  $V_{CC}$ , is lower than the over-temperature threshold,  $V_{OTP\_ADC}$ , over a debounce time,  $t_{OTP\_ADC}$ , the programmable shutdown flow will be triggered.

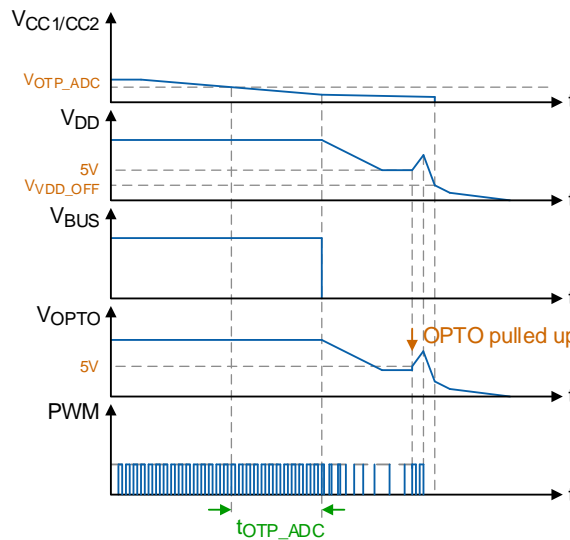


Figure 8. Timing Sequence of OTP with Power-Latch

**17.2 Sink Port (RT7206KN Only)**

**17.2.1 Power Sequence**

When a Type-C cable attached, VDD will be powered up by 5V from the Source port. After that, the embedded MCU will read the ADC voltage in OPTO, V<sub>ADC\_OPTO</sub>, to get the correspond power request. If Source Capabilities of the Source port is compatible, the request will be delivered to the Source port, changing 5V to the correspond voltage level. Once the ADC voltage in VDD, V<sub>ADC\_VDD</sub>, is recognized, the blocking N-MOSFET will be turned on for delivering power to the Host.

**17.2.2 Capability Selection**

The level of V<sub>OPTO</sub> can be easily designed by the resistors, R<sub>SEL1</sub> and R<sub>SEL2</sub>, with 1% tolerance between VDD and GND as shown in Figure 9.

Sink Capabilities		RSEL1	RSEL2
1	User Define	Open	Short
2	User Define	Open	11kΩ
3	User Define	Open	24.9kΩ
4	User Define	Open	56kΩ
5	User Define	Open	220kΩ
6	User Define	130kΩ	Open
7	User Define	19.6kΩ	Open
8	User Define	Short	Open

**17.2.3 Programmable Shutdown Flow from Protections**

As the Sink port, RT7206KN provides the solutions below once any abnormal condition occurs.

**17.2.3.1 Output-Latch**

Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off. To recover the system, the output cable must be removed and then attached again.

**17.2.4 Over/Undervoltage Protection (OVP/UVP)**

The RT7206KN series provides a programmable solution by ADC-measurement to achieve overvoltage or undervoltage protection. Once V<sub>DD</sub> is higher than the programming threshold, V<sub>OVP\_ADC</sub>, over a debounce time, t<sub>OVP\_ADC</sub>, or V<sub>DD</sub> is lower than the programming threshold, V<sub>UVP\_ADC</sub>, over a debounce time, t<sub>UVP\_ADC</sub>, the programmable shutdown flow will be triggered.

**17.2.5 Overcurrent Protection (OCP)**

The RT7206KN also provides a programmable solution by ADC-measurement to achieve overcurrent protection. Once I<sub>CS</sub> is higher than the programming threshold, I<sub>OCP\_ADC</sub>, over a debounce time, t<sub>OCP\_ADC</sub>, the programmable shutdown flow will be triggered.



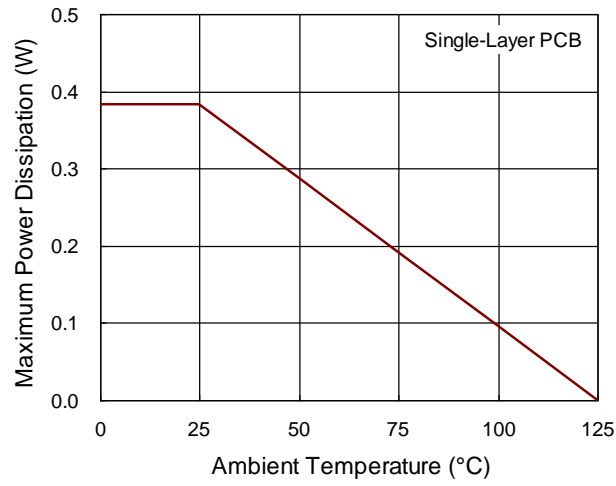
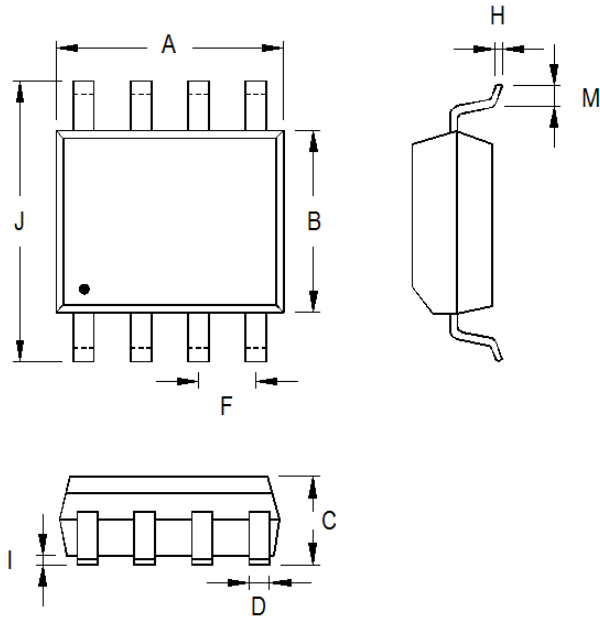


Figure 10. Derating Curve of Maximum Power Dissipation

**Note 8.** The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

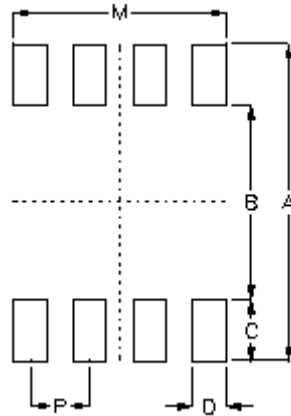


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package



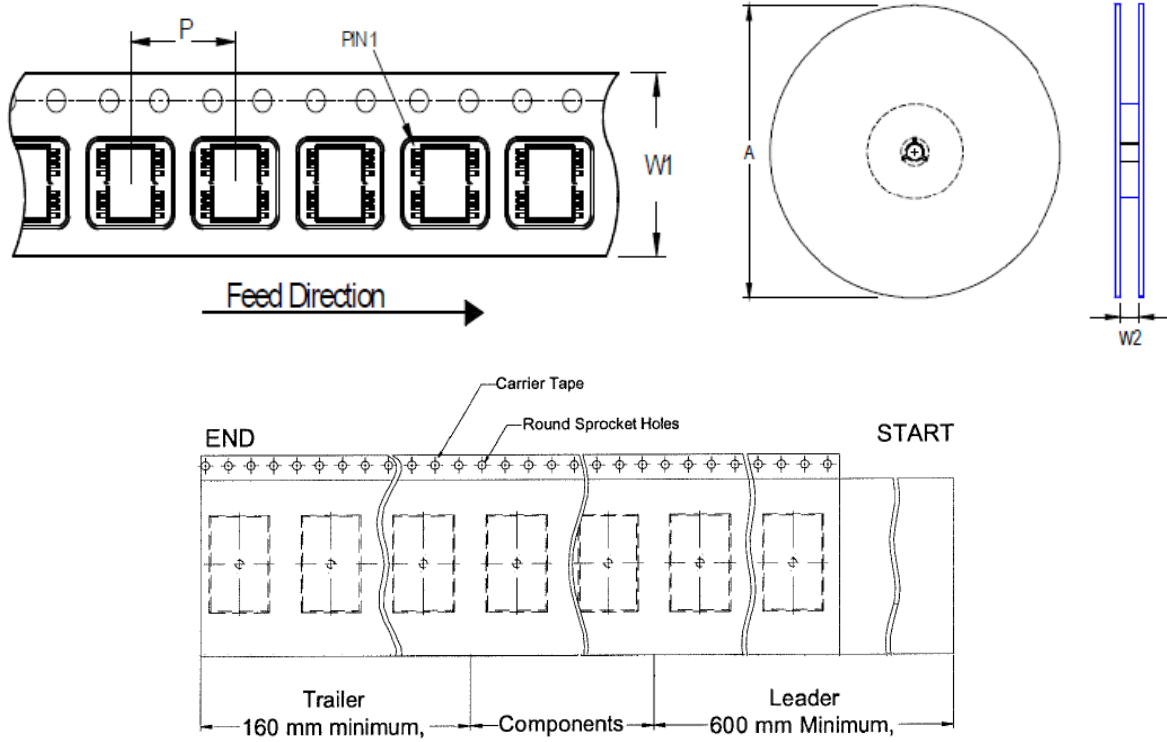
**19 Footprint Information**



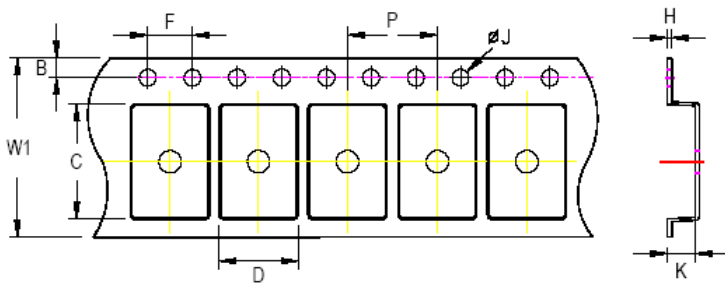
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8/SOP-8(FC)	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

20 Packing Information

20.1 Tape and Reel Data









Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOP-8	12	8	330	13	3,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:  
 - For 12mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

**20.2 Tape and Reel Packing**

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 13"</p>	4	 <p>1 reel per inner box <b>Box G</b></p>
2	 <p>HIC &amp; Desiccant (2 Unit) inside</p>	5	 <p>6 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box <b>Carton A</b></p>

Package	Container		Reel			Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units			
SOP-8	13"	3,500	Box G	1	3,500	Carton A	6	21,000			

**20.3 Packing Material Anti-ESD Property**

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
$\Omega/\text{cm}^2$	$10^4$ to $10^{11}$	$10^4$ to $10^{11}$	$10^4$ to $10^{11}$	$10^4$ to $10^{11}$	$10^4$ to $10^{11}$	$10^4$ to $10^{11}$

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**21 Datasheet Revision History**

Version	Date	Description	Item
01	2023/2/22	Modify	Simplified Application Circuit on P2, 3 Functional Pin Description on P4 Operation on P5 Recommended Operating Conditions on P6 Electrical Characteristics on P6 to P9 Typical Application Circuit on P10, 11 Typical Operating Characteristics on P16, 18, 19 Application Information on P20 to P25
02	2023/9/22	Modify	General Description on P1 Ordering Information on P1 Electrical Characteristics on P9 Application Information on P21
03	2024/7/3	Modify	Ordering Information on P1 Application Information on P31 Packing Information on P34, 35