High-Integration USB PD Controller with Internal Feedback Compensation and Synchronous Rectification for ZVS Control

General Description

The RT7208EB is a programmable USB PD controller with built-in functions of synchronous rectification, bi-direction control and internal feedback compensation. The controller MCU handles various proprietary protocols via the D+/D- interface and supports USB PD Type-C via the CC1/CC2 pins.

The RT7208EB provides the highly integrated solution for the off-line high power density AC-DC converter by utilizing the zero-voltage switching (ZVS) on main switch. This is accomplished by built-in compensation for feedback control to regulate output voltage and current. In order to reduce usage of external components, the controller is built-in with a synchronous rectification controller, and integrated with diverse functions and protections. These features improve the efficiency as well as the safety of a power converter.

In the IC, an internal synchronous rectifier controller can optimize efficiency and provide safe operation in both continuous-conduction mode (CCM) and discontinuous -conduction mode (DCM) under a wide output voltage range of 3.0V to 22V.

Moreover, a dual operational amplifier with the digital-to-analog converter (DAC) is embedded for voltage-loop and current-loop regulation when programming the constant-voltage (CV) and constant-current (CC) regulation in high precision.

Applications

- USB PD Type-C or Proprietary Protocols (e.g., FCP, SCP and AFC) Chargers/Adapters for Smart Phones, NBs, Tablets and All Other Electronics
- USB PD Extension Cores with Offline AC-DC Converters

Features

- **Protocol Support**
  - **USB PD2.0/PD3.0 and PPS**
  - **Proprietary Protocols**
- **Highly Integrated**
  - **Embedded MCU with an Mask ROM of 32KB, an OTP-ROM of 16KB, and an SRAM of 3KB**
  - **Built-in Synchronous Rectifier Controller and Driver**
  - **Built-in Charge Pump for a Wide V_{DD} Operation Range of 3V to 22V**
  - **Built-in Bi-direction Function for Programmable Constant-Voltage and Constant-Current Control**
  - **Built-in Internal Feedback Compensation**
  - **Built-in Dual Shunt Regulators with Respectively 11-bit and 10-bit DAC Programmable Reference Voltages for CV and CC Control**
  - **Built-in 10-bit Analog-to-Digital Converter (ADC)**
  - **Programmable Linear Cable Compensation**
  - **BLD Pin for Quick Discharge of Output Capacitor**
  - **VBUS Pin for Detection VBUS Voltage and Quick Discharge of VBUS Capacitor**
  - **USBP Pin for Direct Drive of External Blocking N-MOSFET**
  - **Power-Saving Mode in Standby Mode**
- **Protection**
  - **Adaptive Output Over-Voltage Protection**
  - **Adaptive Under-Voltage Protection**
  - **CC1/CC2/D+/D- Over-Voltage Protection**
  - **Firmware-Programmable Constant-Current Protection**
  - **Firmware-Programmable Over-Current Protection**
  - **Firmware-Programmable Over-Temperature Protection**

Ordering Information

RT7208EB □□-□

- Programmed Firmware Code AABBX
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- Package Type
  - QW : WQFN-28L 4x5 (W-Type) (Exposed Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

The products are :

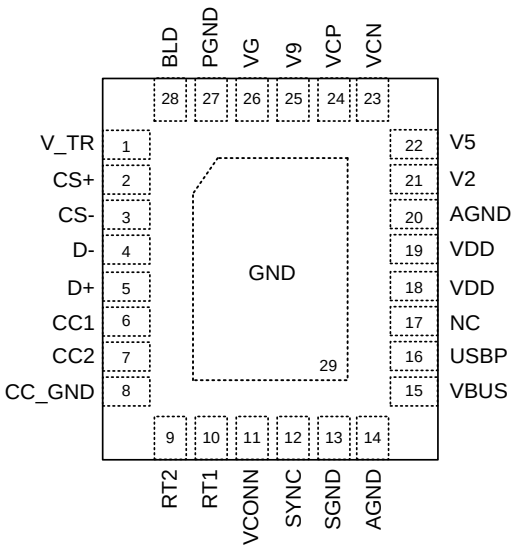
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

(TOP VIEW)

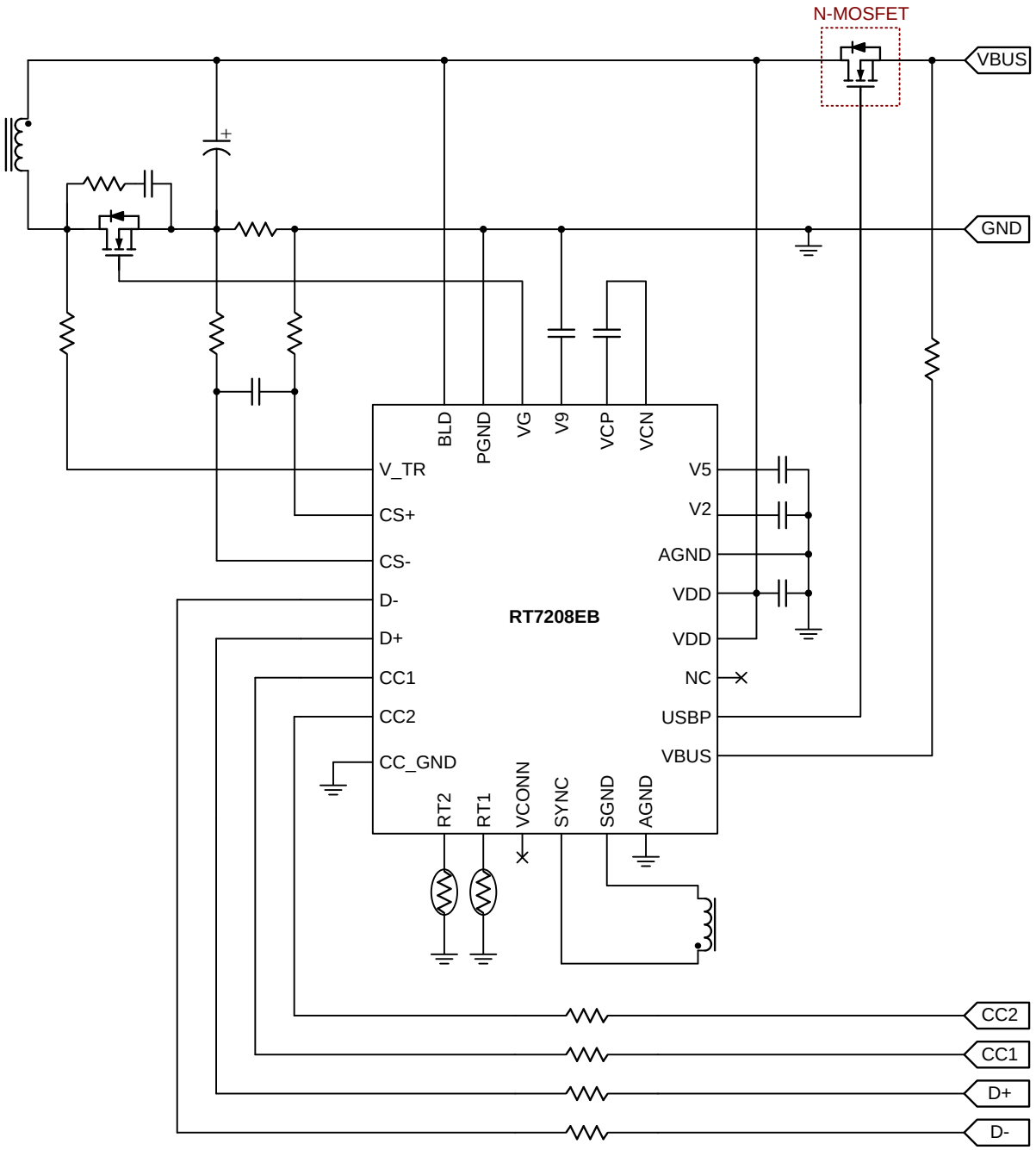


WQFN-28L 4x5

RT7208EB Functional Table

Version	RT7208EB
Output Voltage Supported	3V to 22V
SR MOSFET V_{DS} Scaling Factor R_{VDS2} / (R_{VDS1} + R_{VDS2})	1/50
VOUT Scaling Factor R_{FB2} / (R_{FB1} + R_{FB2})	1/10
Built-in FB Resistors	O
Blocking MOSFET Driver	N-MOSFET

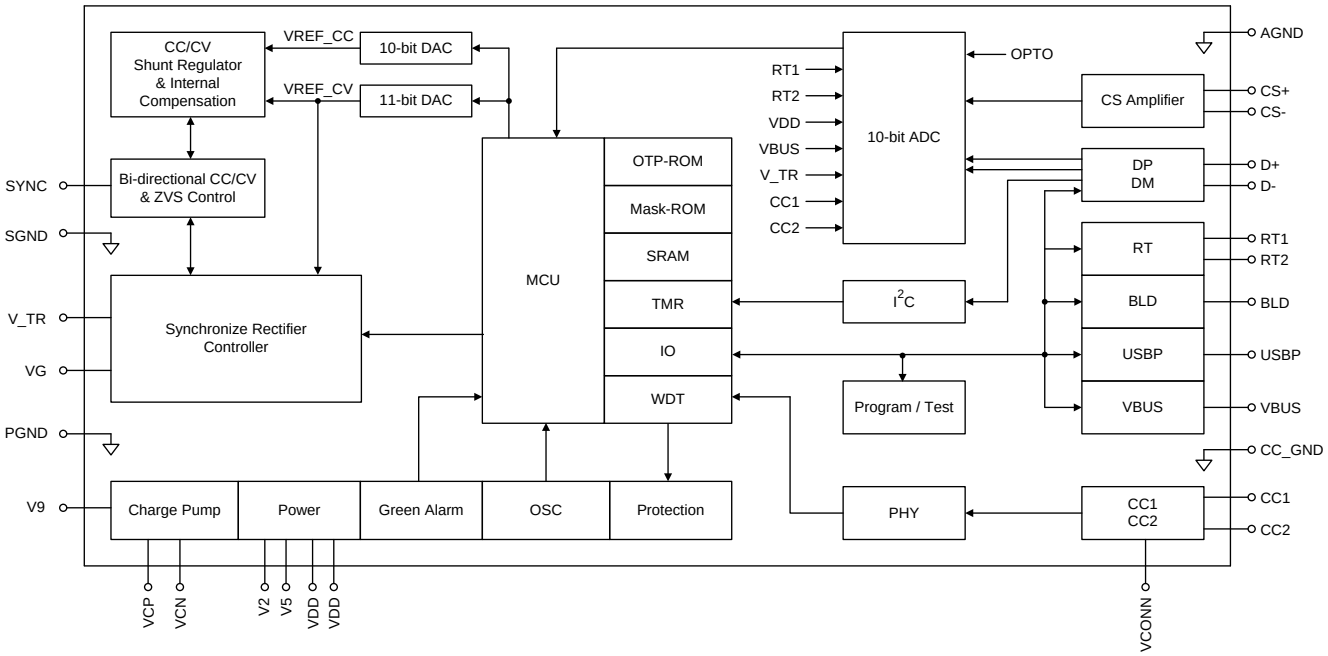
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	V_TR	AI	Transformer voltage sense node.
2	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
3	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
4	D-	A/D IO	USB D- channel.
5	D+	A/D IO	USB D+ channel.
6	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
7	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
8	CC_GND	GND	Alternative ground for CC1 and CC2.
9	RT2	A/D IO	Remote thermal sensor connection node 2 for over-temperature protection.
10	RT1	A/D IO	Remote thermal sensor connection node 1 for over-temperature protection.
11	VCONN	PWR	Supply VCONN power to CC1/CC2.
12	SYNC	A IO	Bi-direction control for pulse transformer connection.
13	SGND	GND	Alternative ground for SYNC.
14	AGND	GND	Analog ground.
15	VBUS	D IO	VBUS sensing and bleeder connection node to provide another path to discharge the VBUS capacitor.
16	USBP	D IO	Control signal of the blocking N-MOSFET
17	NC	NC	No internal connection.
18, 19	VDD	PWR	Supply input voltage.
20	AGND	GND	Analog ground.
21	V2	PWR	Regulated DC bias to supply for the MCU.
22	V5	PWR	Regulated DC bias to supply for internal circuitry.
23	VCN	AO	Charge pump driver CN output.
24	VCP	AO	Charge pump driver CP output.
25	V9	PWR	Regulated DC bias to supply for the synchronous rectifier driver.
26	VG	AO	Gate driver output for the SR MOSFET.
27	PGND	GND	Power ground.
28	BLD	D IO	Bleeder connection node to provide another path to discharge the output capacitor.
29 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram



Operation

The RT7208EB is a highly integrated secondary-side programmable SMPS and USB PD Type-C controller providing various functions and protections for off-line AC-DC converters.

Power Structure

Biased by the VDD pin, the RT7208EB has two regulated DC output voltages, V_5 and V_2, to supply its internal circuit and the microprocessor (MCU). The bypass capacitors at the V2 and V5 pins are required to improve stability of the internal LDO and to minimize regulated ripple voltages. The RT7208EB also integrates a charge pump to generate a boost voltage V_9 from V_5 with a capacitor between VCP and VCN pin connection so that the V9 voltage can be nearly 2 times of the V5 voltage and the VG pin can directly drive the SR MOSFET. Besides, the charge pump allows the controller to operate under low supply voltage condition as long as the output voltage is not below the programmed UVP level. In order to improve efficiency, the charge pump can be disabled by firmware and V_{DD} will supply power to V9 through the internal 9V LDO when V_{DD} is higher than firmware setting threshold.

Constant-Voltage and Constant-Current (CV/CC) Regulators

The RT7208EB has two transconductance amplifiers are connected in parallel to the feedback compensator which sends signal to SYNC pin to regulate output voltage and output current, respectively. The operation of each feedback loop is opposite to that of the traditional TL431 shunt regulator where the reference voltages of the voltage feedback loop and the current feedback loop (V_{REF_CV} and V_{REF_CC}) are analog output voltages from 11-bit DAC and 10-bit DAC, respectively. The analog output range of the 11-bit DAC is from V_{DAC_MIN} = 0.152V to V_{DAC_MAX} (typical 2.2V), which makes output voltage resolution as small as 10mV for the RT7208EB, to achieve high-precision CV regulation.

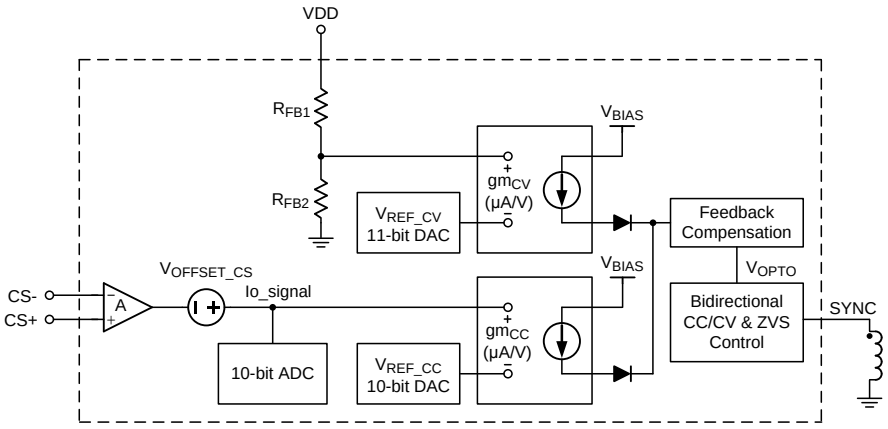


Figure 1. CV and CC Loops

Current-Sense Amplifier

To minimize power loss of the current sense resistor in the converter, the RT7208EB includes an amplifier with virtually zero input offset voltage and with a voltage gain of 20 or 40. The sensed output current is amplified by the current-sense amplifier, shown as "Io_signal" in Figure 1, which is then sent to the current-loop regulator for constant-current regulation and also sent to the MCU, by way of a 10-bit ADC for analog-to-digital conversion, to update the output current status for the MCU.

Bi-Direction Control

The RT7208EB provides the SYNC pin, as the bi-direction control transceiver between the primary side and the secondary side. The SYNC pin receives the PLS pulse from the primary side through a small pulse transformer, utilized to replace the photo-coupler. According to output load, the RT7208EB will internally generate the OPTO voltage to determine the transmitted time of SYNC pulse for feedback compensation. The primary side controller can detect the height and width of SYNC pulse to achieve output voltage and output current regulation. The SYNC pin can also detect the pulse width from the primary side and then turn on SR MOSFET to achieve ZVS on the main switch, if the pulse width from the primary side is larger than 120ns. By using the pulse transformer, bi-direction control delivers feedback compensation and possesses better transient response and phase margin.

External Temperature Sensing

The RT7208EB provides the RT1 and RT2 pin, as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC), as shown in Figure 2. If the RT voltage is below an over-temperature protection (OTP) threshold and the condition sustains for a programmed time delay, the OTP will be triggered.

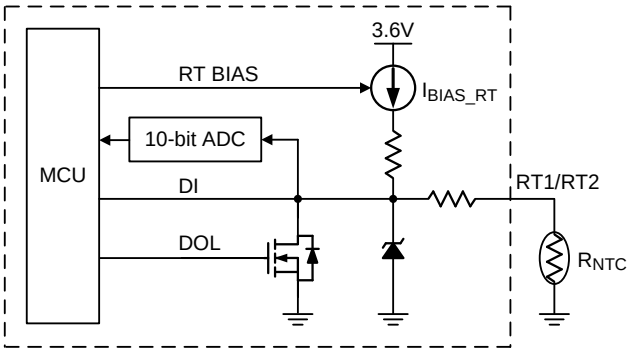


Figure 2. External Temperature Sensing

Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU via an ADC, can be reprogrammed for other purposes since they can be used as an analog/digital input or output, as shown in Figure 3.

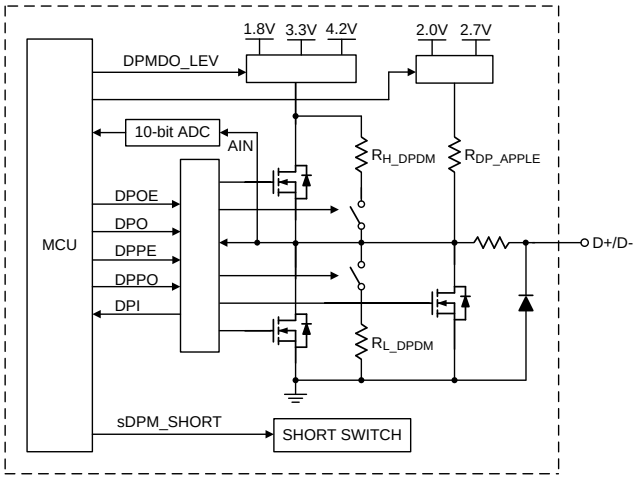


Figure 3. Interface of D+ and D-

Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with USB Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80μA, 180μA, and 330μA, provided by each of the CC pins, will be advertised to an Upstream Facing Port (UFP) as default USB current, 1.5A, and 3.0A, respectively, as shown in Figure 4.

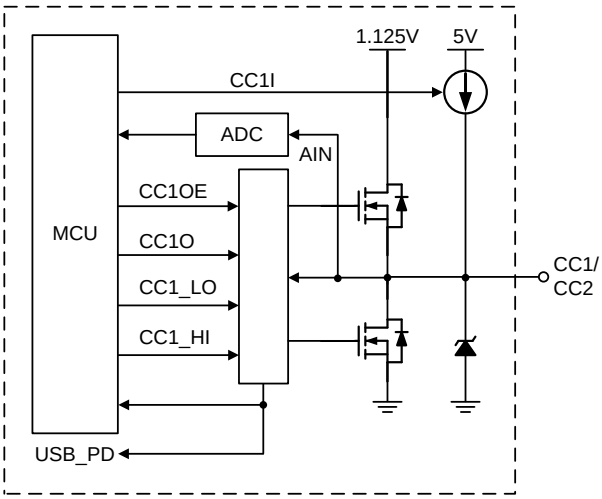


Figure 4. Interface of CC1 and CC2

Open-Drain Drivers for BLD and VBUS Pins

The BLD and VBUS pins with their specific functions are driven by open-drain drivers, as shown in Figure 5 and explained below.

The RT7208EB provides the BLD pin, driven by open-drain driver with a bleeder or a register-programmable discharge current to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 12V to 5V.

If the BLD pin is used as a bleeder, a resistor is connected between VOUT and the BLD pin and a power resistor can be used for better power dissipation capability. If the BLD pin is used as a register-programmable discharge current, there is unnecessary to connect a resistor between VOUT and the BLD pin.

The VBUS pin is used as a bleeder to help discharge the VBUS capacitor to V_{safe0V} upon the detachment of a connected device and provide real-time VBUS voltage detection by ADC.

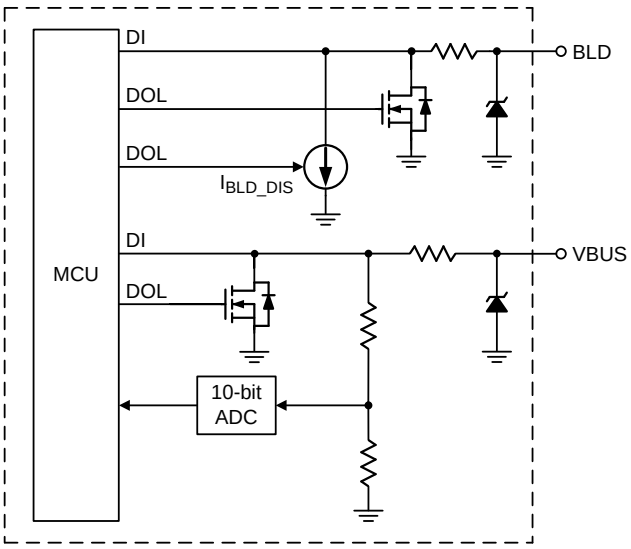


Figure 5. Interface of BLD and VBUS Pin

SR Control

To improve the AC-DC converter's efficiency, the RT7208EB includes an SR controller, which has proprietary auto-tracking function to minimize dead time between the conduction intervals of the SR MOSFET and the main switch MOSFET, while it can still ensure safe operation in both DCM and CCM conditions and even in a wide output range. To prevent the on-time overlap of the main switch MOSFET and the SR MOSFET, the SR controller will be temporarily turned off under conditions of load transition, output voltage transition, output short circuit, or low output or input voltages with programmable thresholds. At light load or no load condition, the SR controller will also be disabled to reduce power consumption.

Absolute Maximum Ratings (Note 1)

- USBP to GND ---------- –0.3V to 35V
- VDD, BLD, VBUS to GND ---------- –0.3V to 25V
- V9, VG, VCN to GND (Note 6) ---------- –0.3V to 14V
- V5, SYNC, V_TR, RT1, RT2, CC1, CC2, D+, D-, CS+, CS-, VCP, VCONN to GND (Note 6) ---------- –0.3V to 6.5V
- V2 to GND ---------- –0.3V to 2.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-28L 4x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)
  WQFN-28L 4x5, θ_{JA} ---------- 27.4°C/W
  WQFN-28L 4x5, θ_{JC} ---------- 2°C/W
- Junction Temperature (±15°C) (Note 5) ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range (150±15°C) (Note 5) ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 3V to 22V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		3.3	3.5	3.7	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.7	2.75	2.8	V
VDD Turn-On/Off Hysteresis	V_{VDD_HYS}		0.5	0.75	1	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.7V	--	120	240	μA
VDD Operating Current	I_{DD_OP}	V_{DD} = 5V, in normal mode, SR driver is disabled.	--	6	9	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	V_{DD} = 5V, in sleep mode, SR driver is disabled.	--	1.5	2.5	mA
VDD Green-Mode Current	I_{DD_GREEN}	V_{DD} = 5V	--	925	1250	μA
Maximum VDD Over-Voltage Protection Threshold	$V_{MAX\_VDD\_OVP}$		23	24	25	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Over-Voltage Protection Threshold	V_{VOUT_OVP}	With respect to V_{REF_CV}	00	106.7	110	113.3	%
			01	109.25	115	120.75	
			10	114	120	126	
			11	Disable			
VDD Over-Voltage Protection Threshold Voltage for Disable SR Driver	$V_{VDD\_OVP\_SR}$	With respect to V_{REF_CV}		104.5	110	115.5	%
VDD Over-Voltage Protection Deglitch Time	$t_{D\_VDD\_OVP}$	(Note 5)		24	30	36	µs
VDD Over-Voltage Protection Deglitch Time for Disable SR Driver	$t_{D\_VDD\_OVP\_SR}$			--	50	--	µs
Register-Programmable VDD Under-Voltage Wake-Up Threshold	$V_{DD\_UV\_WK}$	With respect to V_{REF_CV}. It can be disabled by register.	0	85.5	90	94.5	%
			1	80.75	85	89.25	
VDD Under-Voltage Deglitch Time	$t_{D\_VDD\_UV}$			75	115	155	µs
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} > 2.7V		20.5	21.6	22.7	MHz
Internal Bias							
V9 Bias	V_{BIAS_V9}	10V < V_{DD} < 25V It can disabled by register.		7.6	8	8.4	V
V9 Load Regulation		1mA < I_{BIAS_V9} < 30mA		--	--	300	mV
V9 Output Short-Circuit Current	I_{V9_SC}			45	70	95	mA
V5 Bias	V_{BIAS_V5}	6V < V_{DD} < 25V		4.75	5	5.25	V
V5 Load Regulation		1mA < I_{BIAS_V5} < 30mA		--	--	150	mV
V5 Output Short Circuit Current	I_{V5_SC}			50	90	130	mA
V5 Over-Voltage Protection Threshold Voltage	V_{V5_OVP}			5.7	6	6.3	V
V2 Bias	V_{BIAS_V2}	3V < V_{DD} < 25V		1.71	1.8	1.89	V
V2 Load Regulation		1mA < I_{BIAS_V2} < 20mA		--	--	20	mV
V2 Output Short Circuit Current	I_{V2_SC}			20	50	80	mA
V2 Over-Voltage Protection Threshold Voltage	V_{V2_OVP}			2.125	2.275	2.425	V
Over-Voltage Protection Deglitch Time	$t_{D\_BIASOVP}$			--	50	--	µs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Regulator Section							
VDD Divider Resistor for Feedback Loop and Cable Compensation	R_{FB_CV}	$R_{FB} = R_{FB1} + R_{FB2}$ R_{FB1} : V_{DD} to V_{FB1} R_{FB2} : V_{FB1} to GND		336	420	504	kΩ
V_{OUT} Scaling Factor	K_{FB}	(R_{FB1} + R_{FB2}) / R_{FB2} (Note 5)		9.9	10	10.1	--
VFB Capacitance	C_{F_VFB}	V_{FB} to GND capacitance (Note 5)		4	5	6	pF
Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$			0.485	0.5	0.515	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	11-bit Digital-to-Analog converter		--	0.152	--	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$			2.178	2.2	2.222	V
Minimum DAC Output Voltage for CC Regulators	$V_{DAC\_MIIN\_CC}$	10-bit Digital-to-Analog converter (Note 5)		--	0	--	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$			1.485	1.5	1.515	
Maximum ADC Sense Voltage	V_{ADC_MAX}	10-bit Analog-to-Digital converter		2.178	2.2	2.222	V
Register-Programmable High Level Trigger Level for FB Ramp Comparator	$V_{H\_TH\_RAMP}$		0	2	2.1	2.2	V
			1	1.6	1.7	1.8	
Low Level Trigger Level for FB Ramp Comparator	$V_{L\_TH\_RAMP}$			--	0	--	V
Register-Programmable FB Ramp Delay Time	t_{D_RAMP}		0	0.7	0.8	0.9	µs
			1	1.225	1.4	1.575	
Register-Programmable Low to High Charge Time for FB Ramp	t_{CHG_RAMP}	For 180kHz	0	2.7	3	3.3	µs
		For 130kHz	1	3.78	4.2	4.62	
Current-Sense Section							
Cut-Off Frequency for Current-Sense Amplifier Input Low Pass Filter	f_{C_CS}	(Note 5)		1	1.5	2	kHz
Current Sense Voltage Gain	K_{CS}		0	--	20	--	V/V
			1	--	40	--	
Input Offset Voltage	V_{OFFSET_CS}			--	0.6	--	V
Unit Gain Bandwidth		(Note 5)		1000	--	--	kHz

Parameter	Symbol	Test Conditions			Min	Typ	Max	Unit
Register-Programmable Transconductance Amplifier of Cable Compensation	gm_{COMP}	Without cable compensation		000	Disable			μA/V
		R_{CABLE} = 75mΩ	R_{CS} x K_{CS} = 100m	001	1.786	1.984	2.183	
			R_{CS} x K_{CS} = 200m		0.893	0.992	1.091	
		R_{CABLE} = 100mΩ	R_{CS} x K_{CS} = 100m	010	2.381	2.646	2.91	
			R_{CS} x K_{CS} = 200m		1.191	1.323	1.455	
		R_{CABLE} = 150mΩ	R_{CS} x K_{CS} = 100m	011	3.571	3.968	4.365	
			R_{CS} x K_{CS} = 200m		1.786	1.984	2.183	
		R_{CABLE} = 200mΩ	R_{CS} x K_{CS} = 100m	100	4.762	5.291	5.82	
			R_{CS} x K_{CS} = 200m		2.381	2.646	2.91	
		R_{CABLE} = 250mΩ	R_{CS} x K_{CS} = 100m	101	5.952	6.614	7.275	
			R_{CS} x K_{CS} = 200m		2.976	3.307	3.638	
Register-Programmable Exit Green Mode Threshold	V_{GREEN_ED}	(V_{CS+} - V_{CS-}) x K_{CS} + V_{OFFSET_CS}		0	--	0.65	--	V
				1	--	0.7	--	
Internal Compensation Section								
Register-Programmable R_Z for Zero Point	R_Z	(Note 5)		000	8	10	12	kΩ
				001	24	30	36	
				010	40	50	60	
				011	88	110	132	
				100	136	170	204	
				101	184	230	276	
				110	248	310	372	
				111	344	430	516	
Register-Programmable C_Z for Zero Point	C_Z	It can be programmed by register. (Note 5)			1.04	--	2127	nF
Register-Programmable Zero Point	f_{ZERO}	It can be programmed by register. (Note 5)			0.17	--	15318	Hz
Register-Programmable Middle Gain		It can be programmed by register. (Note 5)			–20	--	30.73	dB
Overshoot Clamping Comparator		Ratio of V_{REF_CV}			104.5	110	115.5	%
Debounce Time of Overshoot Clamping	t_{OVC}				24	30	36	μs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Maximum DAC Output Voltage for Internal Compensation	$V_{DAC\_COUNTER}$	With 11-bit digital to analog converter		2.178	2.2	2.222	V
Register-Programmable Overshoot Clamping for OPTO	$V_{DAC\_CLAMP\_HIGH}$	6-bit for the internal compensator counter to clamp DAC output voltage.		0	--	2.2	V
Register-Programmable Undershoot Clamping for OPTO	$V_{DAC\_CLAMP\_LOW}$	6-bit for the internal compensator counter to clamp DAC output voltage.		0	--	2.2	V
Register-Programmable Undershoot Clamping Comparator		1. Ratio of V_{REF_CV} 2. Default is disable 3. Disable at CC mode	0	85.5	90	94.5	µs
			1	87.875	92.5	97.125	
Register-Programmable Debounce Time of Disable Undershoot Clamping at CC Mode	$t_{DIS\_UVC\_CC}$	(Note 5)	0	5	10	15	µs
			1	15	20	25	
Undershoot Clamping Comparator Hysteresis		Ratio of V_{REF_CV} (Note 5)		--	5	10	mV
Register-Programmable Debounce Time of Undershoot Clamping	t_{UVC}	(Note 5)	0	5	10	15	µs
			1	25	30	35	
Charge Pump Section							
Charge Pump Diode Forward Voltage	V_{F_DCP}	I_{F_DCP} = 10mA		--	--	0.7	V
Charge Pump Operating Frequency	f_{CP}			150	170	190	kHz
Rising Time	t_{R_CP}	C_L = 6nF, V_5 = 5V, from 20% to 80%		70	140	210	ns
Falling Time	t_{F_CP}	C_L = 6nF, V_5 = 5V, from 80% to 20%		60	110	160	ns
Charge Pump Driver Impedance	R_{OUT_CP}	(Note 5)		--	--	10	Ω
Register-Programmable Charge Pump Enable Threshold	V_{V9_CP}	When V_9 < V_{V9_CP}, the charge pump is activated.	0	6.75	7	7.25	V
			1	5.75	6	6.25	
Charge Pump Enable Comparator Debounce Time	t_{V9_CP}	(Note 5)		--	15	--	µs
SR Driver Turn-On Threshold	V_{V9_SRON}			4.3	4.4	4.5	V
SR Driver Turn-Off Threshold	V_{V9_SROFF}	When V_9 < V_{V9_SROFF}, It will send an interrupt to MCU.		4	4.1	4.2	V
Debounce Time	t_{D_V9}	(Note 5)		--	50	--	µs
V9 Turn-On Threshold	V_{V9_ON}			3.55	3.65	3.75	V
V9 Turn-Off Threshold	V_{V9_OFF}	If V_9 < V_{V9_OFF}, the V9 internal circuit will be inactivated.		3.2	3.3	3.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
RT Section							
Open Loop Voltage	V_{RT_OP}	V_{DD} = 5V		3.2	3.6	4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}		00	95	100	105	µA
			01	18	20	22	
			10	3.6	4	4.4	
			11	Open			
VBUS Section							
Maximum VBUS Sinking Current	I_{VBUS_MAX}	(Note 5)		2	--	30	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_MAX} = 20mA		--	--	200	Ω
BLD Section							
Maximum BLD Sinking Current	I_{BLD_MAX}	V_{BLD} = 20V, in 300ms (Note 5)		0.2	--	0.7	A
Pull-Low Impedance	R_{L_BLD}	I_{BLD} = 50mA		--	--	30	Ω
Register-Programmable BLD Discharge Current	I_{BLD_DIS}	V_{DD} > 3V. It is necessary to gradually reduce the discharge current before closing I_{DD_DIS}.	000	7.5	15	22.5	mA
			001	15	30	45	
			010	42	60	78	
			011	63	90	117	
			100	84	120	156	
BLD Discharge Current Step Change Delay Time	t_{STEP_BLD}	When BLD is disabled.		80	100	120	µs
D+, D- Section							
Register-Programmable Pull-High Resistance	R_{H_DPDM}		0	Open			kΩ
			1	10	12.5	15	
Register-Programmable Pull-Low Resistance	R_{L_DPDM}		0	Open			kΩ
			1	16	20	24	
Register-Programmable Leakage Current	I_{LKG_DPDM}	(Note 5)	0	Open			µA
			1	0.5	1	1.5	
Register-Programmable Output High Voltage	V_{OH_OP}		00	Open Drain			V
	$V_{OH\_3.3V}$	V_{DD} = 5V, R_L = 15kΩ	01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.2V}$		11	3.78	4.2	4.62	
Pull-High Resistance for Apple Mode	$R_{H\_DPDM\_AM}$			25.6	32	38.4	kΩ
Register-Programmable Output High Voltage for Apple Mode	$V_{OH\_2.7V\_AM}$	V_{DD} = 5V, R_L = 15kΩ	0	2.565	2.7	2.835	V
	$V_{OH\_2V\_AM}$		1	1.88	2	2.12	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Low Voltage	V_{OL_OP}	R_L = 15kΩ		--	--	0.2	V
	$V_{OL\_3.3V}$						
	$V_{OL\_1.8V}$						
	$V_{OL\_4.2V}$						
	$V_{OL\_2.7V\_AM}$						
	$V_{OL\_2V\_AM}$						
Register-Programmable DP and DM Input Level	V_{IN_LEV}		0	--	0	--	V
			1	--	0.4	--	
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	0.7 + V_{IN_LEV}	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	V
			01	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	1.5 + V_{IN_LEV}	
			10	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2 + V_{IN_LEV}	
			11	2 + V_{IN_LEV}	2.1 + V_{IN_LEV}	2.2 + V_{IN_LEV}	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.5 + V_{IN_LEV}	0.6 + V_{IN_LEV}	0.7 + V_{IN_LEV}	V
			01	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	
			10	1.7 + V_{IN_LEV}	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	
			11	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2.0 + V_{IN_LEV}	
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
DP Comparison Threshold for Cable Detection	$V_{TH\_DP\_CD}$	Send an interrupt to MCU when cable detached.		0.2	0.3	0.4	V
Register-Programmable Input Debounce Time	t_{D_DPDMIN}	Debounce Time = t_{D_DPDMIN} x K_{tD_DPDMIN} (Note 5)	00	0.95	1	1.05	μs
			01	1.9	2	2.1	
			10	3.8	4	4.2	
			11	7.6	8	8.4	
Register-Programmable Input Debounce Time Scale	K_{tD_DPDMIN}	(Note 5)	00	--	1	--	--
			01	--	8	--	
			10	--	64	--	
			11	--	512	--	
DP/DM Over-Voltage Protection Threshold	V_{DPDM_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU.		4.5	4.75	5	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable DP/DM Over-Voltage Protection Debounce Time	t_{DPDM_OVP}	(Note 5)	0	95	100	105	µs
			1	475	500	525	
CC1, CC2 Section							
Output High Voltage	V_{OH_CC}			1.05	1.125	1.2	V
Output Low Voltage	V_{OL_CC}			0	0.0375	0.075	V
Register-Programmable Input High Trip Voltage	V_{IH_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Rising Time	t_{R_CC}	C_L = 470pF		300	--	700	ns
Falling Time	t_{F_CC}	C_L = 470pF		300	--	700	ns
Register-Programmable Open-Loop Voltage for CC1/CC2 Sourcing Current	V_{CC_OP}	V_{DD} = 5V	0	Disable			V
			1	2.9	3.25	3.6	
Register-Programmable Sourcing Current	I_{CC_SRC}		00	High Impedance			µA
			01	72	80	88	
			10	166	180	194	
			11	304	330	356	
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_CD}	Disable/Enable by register. Send a flag to MCU.		2.5	2.6	2.7	V
CC1/CC2 Over-Voltage Protection Threshold	V_{CC_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU.		4	4.5	5	V
Register-Programmable CC1/CC2 Cable Detection and Over-Voltage Protection Debounce Time	t_{CC_OVP}	(Note 5)	0	95	100	105	µs
			1	475	500	525	
VCONN Voltage	V_{VCONN}	V_{DD} = 5V, I_{VCONN} = 0mA		4.75	4.875	5	V
		V_{DD} = 5V, I_{VCONN} = 30mA		3.3	--	--	
VCONN Short-Circuit Current	I_{VCONN_SC}			50	70	90	mA
USBP Section							
Output High Voltage	V_{OH_USBP}			V_{DD} + 6.5V	V_{DD} + 8V	V_{DD} + 9.5V	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Gate Under-Voltage Protection Threshold	V_{GS_UVP}			V_{GS_TH} + 3.8V	V_{GS_TH} + 4.3V	V_{GS_TH} + 4.8V	V
Gate Under-Voltage Protection Debounce Time	t_{GS_UVP}	(Note 5)		33.75	--	55	μs
Register-Programmable Rise Time	t_{R_USBP}	C_L = 4nF, V_{DD} = 5V, from 20% to 80%	00	100	200	300	μs
			01	230	330	430	
			10	480	600	720	
			11	980	1200	1440	
Transition Delay Time for USBP Driver	t_{D_USBP}	If USBP driver capability set 330μs, 600μs or 1200μs, it will be changed to 200μs by HW after t_{D_USBP}.		45	50	55	ms
Falling Time	t_{F_USBP}	C_L = 4nF, V_{DD} = 5V, from 90% to 10%		--	--	2	μs
Output Low Voltage	V_{OL_USBP}	V_{DD} = 2V, I_{USBP} = 100μA before start-up.		--	--	1	V
SR Driver Section							
Output High Voltage	V_{OH_VG}	I_{SOURCE} = 50mA, V_9 = 9V		8.5	--	--	V
Output Low Voltage	V_{OL_VG}	I_{SINK} = 50mA, V_9 = 9V		--	--	0.5	V
Rising Time	t_{R_VG}	C_L = 6nF, V_9 = 9V, from 20% to 80%		--	75	125	ns
Falling Time	t_{F_VG}	C_L = 6nF, V_9 = 9V, from 80% to 20%		--	35	85	ns
Propagation Delay	t_P	(Note 5)		--	100	--	ns
Comparator Threshold for Gate Floating Detection	V_{TH_GF}	Disable/Enable by register. (Note 5)		0.2	0.3	0.4	V
Comparison Time for Gate Floating Detection	t_{GF}	(Note 5)		--	1.5	--	μs
Initial Output Low Clamping Voltage before Start-Up	$V_{OL\_VG\_INI}$	V_{DD} = 2.5V, I_{SINK} = 50mA		--	--	0.5	V
Internal Pull-Low Resistor	R_{GS_LOW}	(Note 5)		70	100	130	kΩ
V_TR Section							
V_TR Internal Resistance	R_{VDS2}			2.28	2.4	2.52	kΩ
V_TR Sample and Hold Error	E_{SH_VTR}	($\lvert V_{V\_TR\_HIGH} - V_{VTR\_SH} \rvert$ / $V_{V\_TR\_HIGH}$) x 100		--	--	5	%
V_TR Sample and Hold Threshold	K_{VTR_SH}	$V_{TH\_SH} = K_{VTR\_SH}$ x $V_{V\_TR\_HIGH}[n-1]$		0.831	0.875	0.919	--
Mask Time	t_{MASK}	$V_{V\_TR} > V_{VTR\_SH}$		170	320	470	ns

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable V_TR Blanking Time	t_{BLANK_VTR}	$V_{V\_TR} > V_{VTR\_SH}$ V_TR blanking time change limit is ±46ns per cycle. (Note 5)	000	0.15	0.25	0.35	µs
			001	0.35	0.45	0.55	
			010	0.55	0.65	0.75	
			011	0.75	0.85	0.95	
			100	0.95	1.05	1.15	
			101	1.15	1.25	1.35	
			110	1.35	1.45	1.55	
			111	1.55	1.65	1.75	
Register-Programmable V_TR Under-Voltage Threshold	$V_{TH\_VTR\_UV}$	If $V_{V\_TR\_HIGH}$ - (V_{OUT} x K_{VDS_SR}) > $V_{TH\_VTR\_UV}$, the SR driver is activated.	000	Disable			V
			001	0.35	0.45	0.55	
			010	0.3	0.4	0.5	
			011	0.25	0.35	0.45	
			100	0.2	0.3	0.4	
			101	0.15	0.25	0.35	
			110	0.1	0.2	0.3	
			111	0.05	0.15	0.25	
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When $V_{V\_TR} < K_{VIN\_LOW}$ x V_{OUT}, it will send an interrupt to MCU.		2.0	2.2	2.4	--
V_TR Over-Voltage Threshold	$V_{TH\_VTR\_OV}$	V_9 = 4.5V		2.8	3.0	3.2	V
Register-Programmable Low Level Threshold for V_TR Falling Edge Detection and Dead Time Comparison Threshold	$V_{TH\_LF\_V\_TR}$		00	0.05	0.10	0.15	V
			01	0.25	0.3	0.35	
			10	0.45	0.5	0.55	
			11	0	0.05	0.1	
Dead Time Comparator Delay		(Note 5)		--	--	40	ns
Dead Time Comparator Blanking Time	t_{BLANK_DT}	Disable dead time comparator on VG rising edge.		400	600	800	ns
Register-Programmable V_TR Falling Time Threshold	$t_{V\_TR\_FALLING}$	If V_TR falling time < $t_{V\_TR\_FALLING}$, VG will be triggered.	00	200	250	300	ns
			01	150	200	250	
			10	100	150	200	
			11	50	100	150	
Register-Programmable V_TR Falling Edge Debounce Time	t_{D_VTR}		0	0.05	0.15	0.25	µs
			1	Disable			
V_TR Rising Edge Threshold for AC OFF Detection	$V_{V\_TR\_EDGE}$			0.05	0.1	0.15	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_TR Rising Edge Debounce Time for AC OFF Detection	$t_{V\_TR\_EDGE}$	If V_{V_TR} in $t_{V\_TR\_EDGE}$ is lower than $V_{V\_TR\_EDGE}$, It will send an AC OFF interrupt to MCU. (Note 5)		90	100	110	ms
Register-Programmable Reset Voltage for V_TR Sample and Hold	V_{VTR_RST}		0	(1.25±25%) x K_{VDS_SR} x V_{DD} + 20m			V
			1	0.05	0.1	0.15	
Register-Programmable Debounce Time for V_TR Sample and Hold Reset	$t_{D\_VTR\_RST}$	If V_{VTR_SH} in $t_{D\_VTR\_RST}$ is higher than $V_{V\_TR\_HIGH}$, V_{VTR_SH} will reset to V_{VTR_RST}. (Note 5)	0	90	100	110	ms
			1	9	10	11	
SR Control Section							
Register-Programmable Charging Capacitance	C_T	65kHz	00	3.22	4.3	5.38	pF
		85kHz	01	2.47	3.3	4.13	
		140kHz	10	1.42	1.9	2.38	
		180kHz	11	0.98	1.4	1.82	
C_T Reset Time	t_{RST_CT}	From V_{V_TR} = K_{VTR_SH} x $V_{V\_TR\_HIGH}$[n-1] (Note 5)		--	--	200	ns
SR MOSFET VDS Scaling Factor	K_{VDS_SR}	R_{VDS2} / (R_{VDS1} + R_{VDS2}) (Note 5)		1/51	1/50	1/49	--
Register-Programmable gm_{V_TR} / gm_{VOUT}			0	3.65	3.97	4.29	--
			1	3.13	3.4	3.67	
Maximum VG Pulse Width Expansion Limit	t_{SRON_MAX}	t_{SR_ON}[n] < t_{SR_ON}[n-1] x t_{SRON_MAX} (Note 5)		105	106	107	%
Register-Programmable V_TR Pulse Width Expansion/Shrink Limit	t_{PWLMT_VTR}	If t_{V_TR}[n] > t_{V_TR}[n-1] + t_{PWLMT_VTR} or t_{V_TR}[n] < t_{V_TR}[n-1] - t_{PWLMT_VTR}, reset automatic tracking counter. (Note 5)	00	0.285	0.3	0.315	µs
			01	0.475	0.5	0.525	
			10	0.665	0.7	0.735	
			11	0.855	0.9	0.945	
Register-Programmable Minimum Period	t_{PERIOD_MIN}	Interval limit from V_TR rising edge to VG falling edge. The clock period is based on f_{OSC_MCU} and can be set by the 12-bit register. The full code is 190µs. (Note 5)		180.5	190	199.5	µs
Register-Programmable VG Inhibit Time	$t_{INHIBIT\_SR}$	Interval limit from VG rising edge to next VG rising edge. The clock period is based on f_{OSC_MCU} and can be set by the 9-bit register. The full code is 24µs. (Note 5)		22.8	24	25.2	µs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable VG Minimum OFF Time	t_{MINOFF_SR}	Interval limit from VG falling edge to next VG rising edge. The clock period is based on f_{OSC_MCU} and can be set by the 7-bit register. The full code is 5.9μs. (Note 5)		5.6	5.9	6.2	μs
PLL Function Section							
Register-Programmable PLL Dead Time	t_{DEAD_PLL}	If VG falling edge to $V_{TH\_VTR\_DT}$ interval < t_{DEAD_PLL}, reset automatic tracking counter. (Note 5)	00	380	400	420	ns
			01	190	200	210	
			10	95	100	105	
			11	Disable			
Register-Programmable Fault PLL Ratio	K_{FAULT_PLL}	If $t_{PWM}[n] > K_{FAULT\_PLL} \times t_{PWM}[n-1]$, VG will be skipped two cycles and reset automatic tracking counter. (Note 5)	0	1.4	1.5	1.6	--
			1	Disable			
Automatic Tracking Section							
Register-Programmable Auto-Tracking Dead Time	t_{DEAD_TRACK}	VG falling edge to $V_{TH\_VTR\_DT}$ interval. If $t_{CT\_DIS}[n] > t_{Lm\_DIS}[n-1] - t_{DEAD\_TRACK}$, VG will be turned-off by the digital circuit and decrement the automatic tracking counter. (Note 5)	00	720	800	880	ns
			01	540	600	660	
			10	360	400	440	
			11	180	200	220	
Maximum Step Limit for Tracking Up/Down		With respect to V_{REF_CV} and including 7-bit tracking control.		0.4	--	0.9	%
SYNC Section							
Register-Programmable SR Driver Turn-Off Delay	$t_{D\_SYNC\_VG}$	From SYNC trigger to VG falling edge.	00	--	0	50	ns
			01	0	50	100	
			10	50	100	150	
			11	100	150	200	
Register-Programmable CT Charge Delay	$t_{D\_CT\_CH}$	From SYNC trigger to CT charge enable.	00	Disable			ns
			01	60	110	160	
			10	170	220	270	
			11	255	330	405	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Positive Voltage Threshold for Pulse Signal Detection	V_{TH_POS}	Pulse signal detection can only be detected with positive voltage.	000	0.36	0.4	0.44	V
			001	0.16	0.2	0.24	
			010	0.76	0.8	0.84	
			011	0.56	0.6	0.64	
			100	1.116	1.2	1.284	
			101	0.93	1	1.07	
Register-Programmable Positive Voltage Detection Debounce Time	t_{D_POS}			12	17	22	ns
Output High Voltage	V_{OH_SYNC}	V_{DD} = 3V		1.6	2	2.4	V
		V_{DD} = 5V		1.88	2.35	2.82	
		V_{DD} = 20V		2.08	2.6	3.12	
Rising Time	t_{R_SYNC}	C_L = 50pF, V_{DD} = 2.7V, from 0.5V to 2V.		--	--	15	ns
Falling Time	t_{F_SYNC}	C_L = 50pF, V_{DD} = 2.7V, from 2V to 0.5V. (Note 5)		230	360	490	ns
SYNC Sourcing Current	I_{SYNC}	(Note 5)		50	75	100	mA
Register-Programmable Pulse Width	t_{PULSE_SYNC}		000	75	100	125	ns
			001	40	60	80	
			010	50	70	90	
			011	75	100	125	
			100	120	150	180	
			101	160	200	240	
SYNC Internal Pull-Low Resistor	R_{SYNC_LOW}			4	5	6	kΩ
SYNC Mask Time	t_{MASK_SYNC}			35	50	65	ns
SYNC Disable Time	t_{DIS_SYNC}			91	130	169	ns
ZVS Section							
SR MOSFET VDS Scaling Factor for Valley Detection	K_{VDS_DTVY}			1/25 x (100%±3%)			--
Register-Programmable Threshold Voltage of Valley Detection	V_{TH_DTVY}		0	V_{OUT} x K_{VTR} x (92%±5%)			V
			1	V_{OUT} x K_{VTR} x (81%±5%)			
Delay Time of Pulse Detection after VG Falling Edge	t_{D_DTPLS}			320	420	520	ns
Register-Programmable Threshold Width of Pulse ON Time Detection	t_{TH_DTPLS}		0	72	90	108	ns
			1	96	120	144	
Inhibit Time after ZVS Pulse	t_{INHBT_ZVS}			0.9	1.2	1.5	µs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Delay Time after SYNC Falling Edge for ZVS Pulse	t_{D_ZVS}		00	Disable			ns
			01	90	130	170	
			10	150	215	280	
			11	210	300	390	
Register-Programmable Pulse ON Time for ZVS	t_{PULSE_ZVS}	Interval limit from ZVS rising edge to ZVS falling edge. The clock period is based on f_{OSC_MCU} and can be set by the 6-bit register.		92	--	2346	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

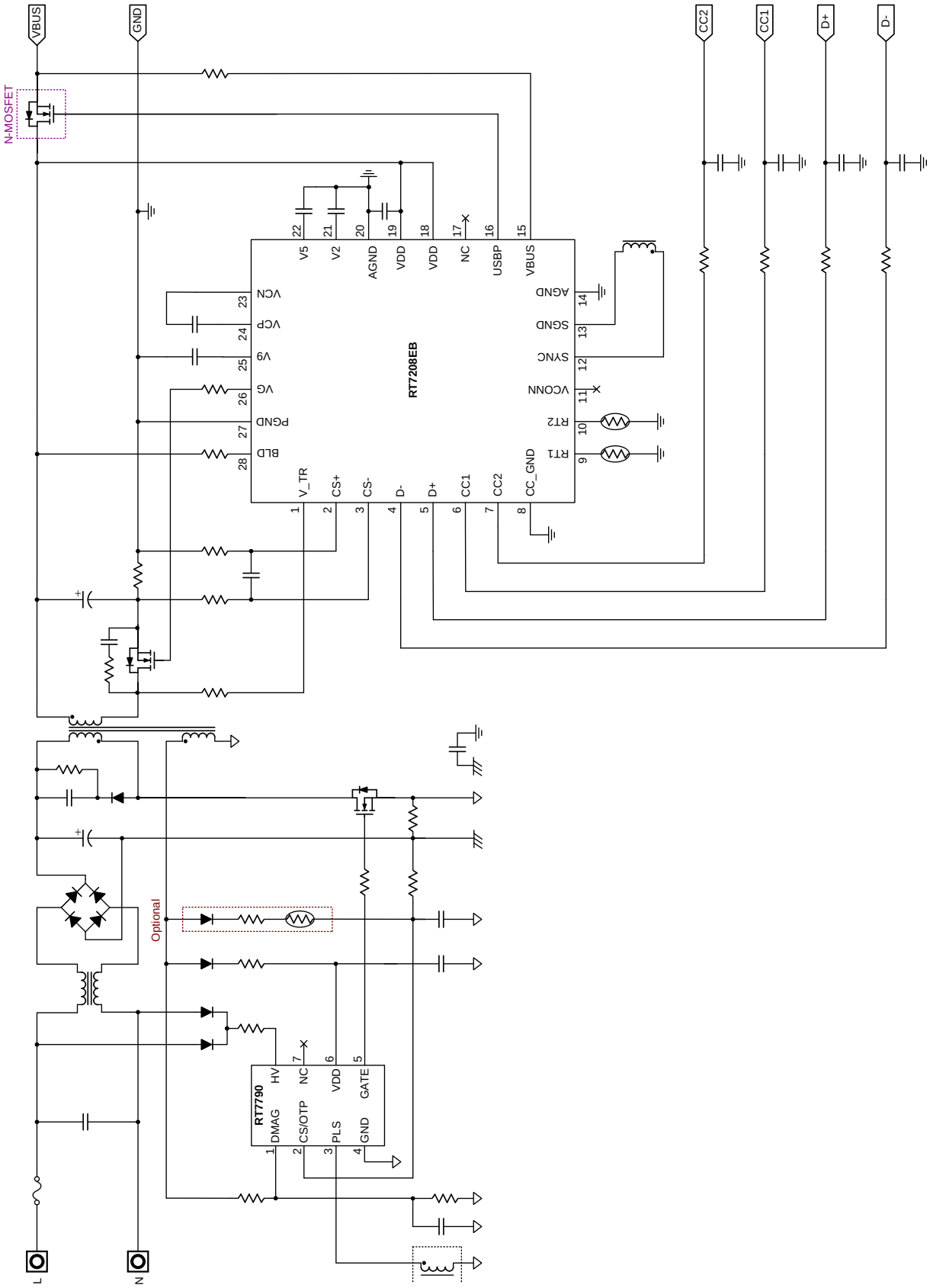
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

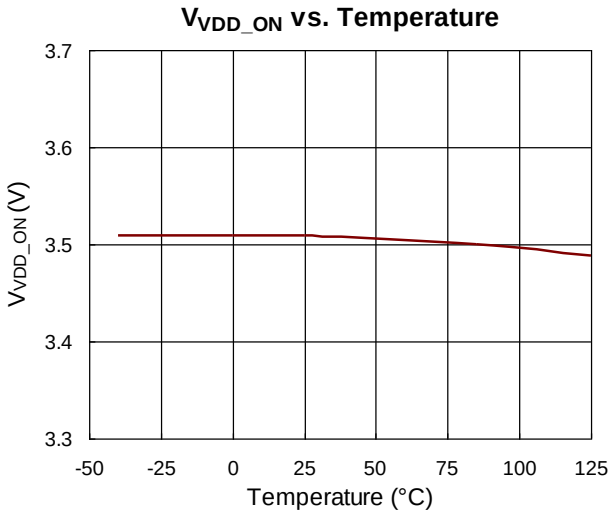
Note 5. Guaranteed by design.

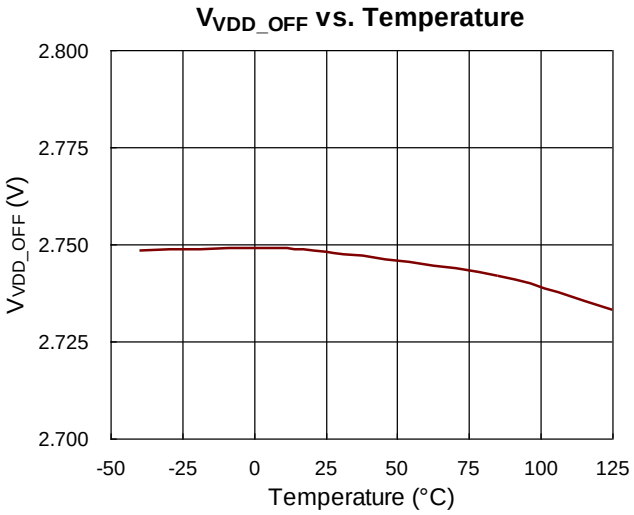
Note 6. For VG to GND, VG - V9 < 0.3V.
For VCP to GND, VCP- V5 < 0.3V.

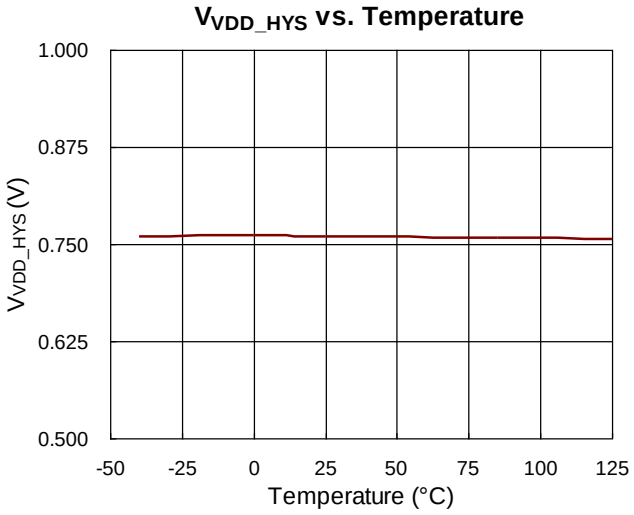
Typical Application Circuit

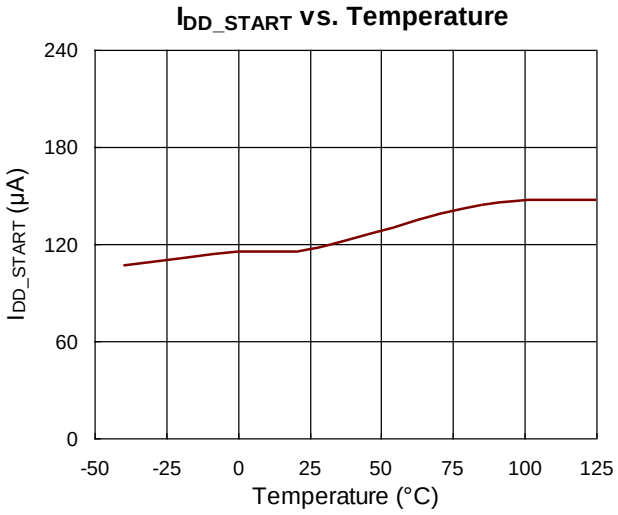


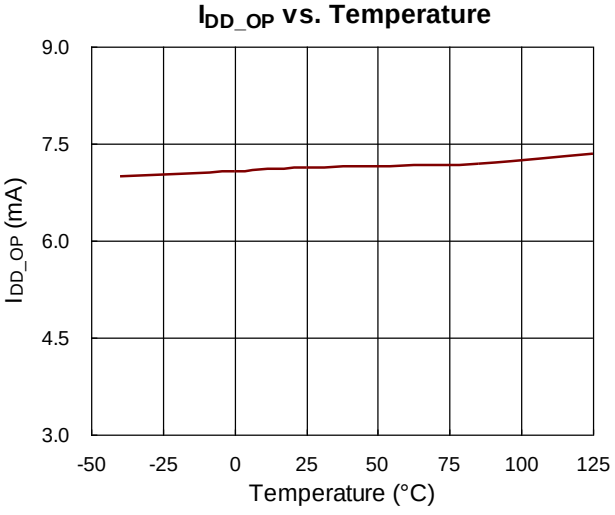
Typical Operating Characteristics

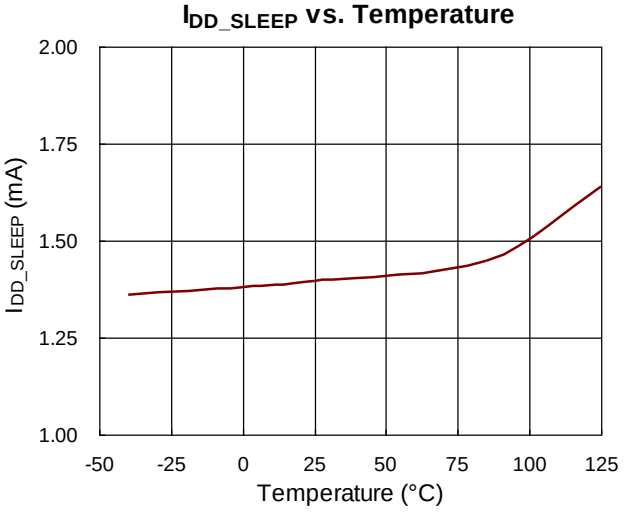


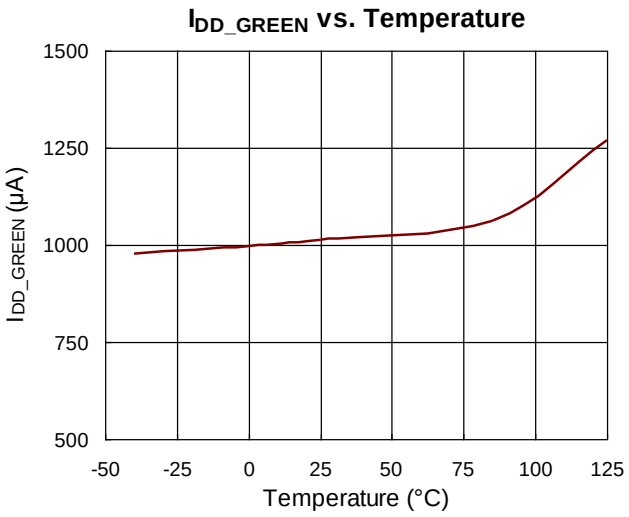


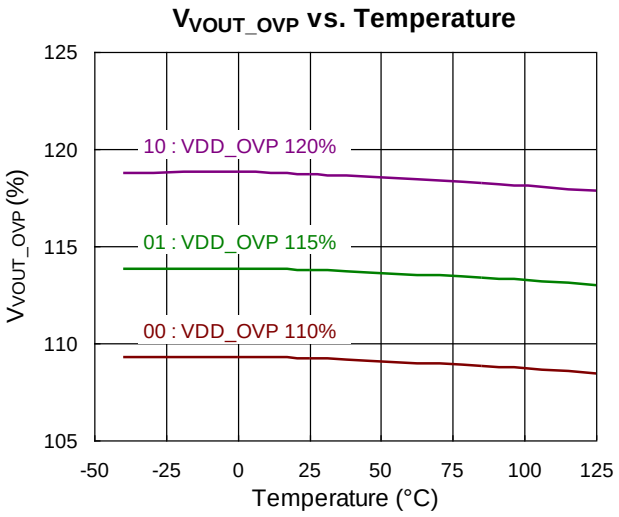


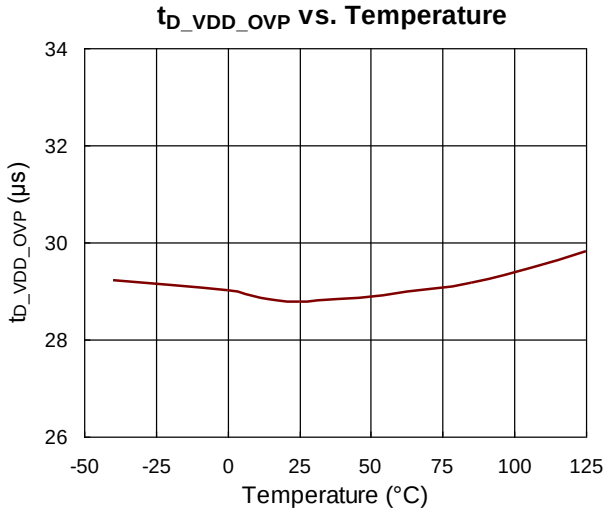


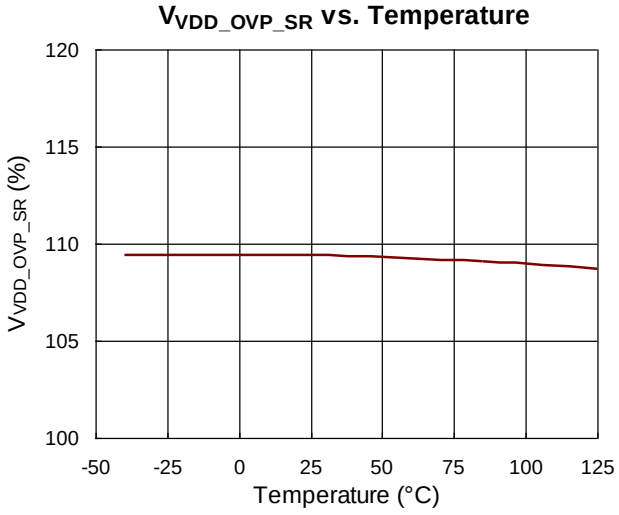


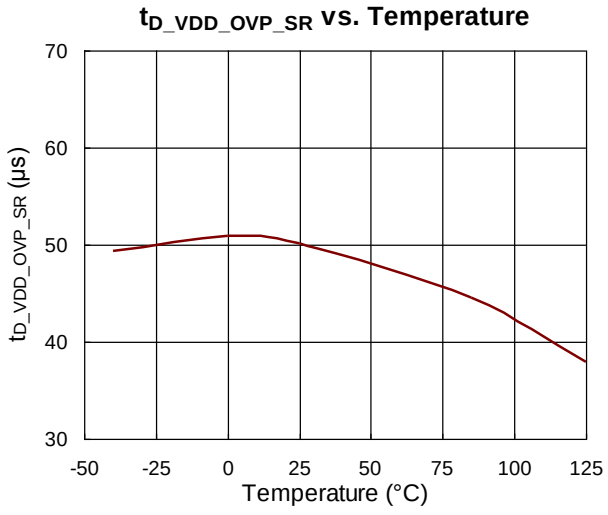


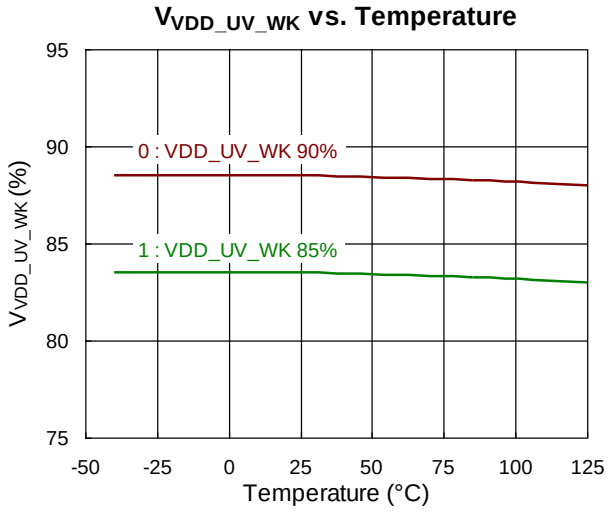


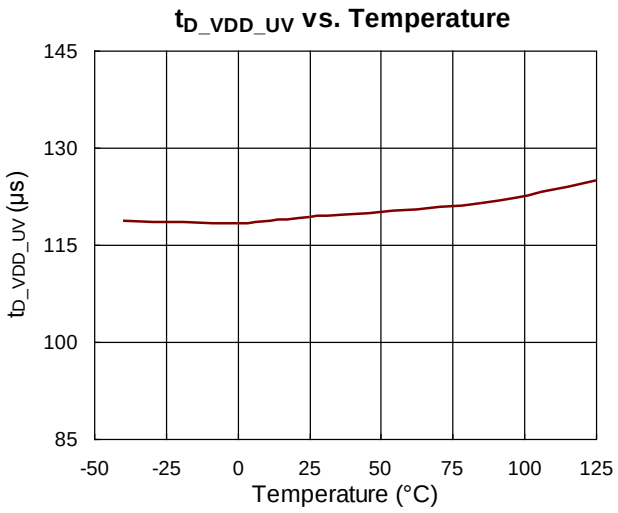


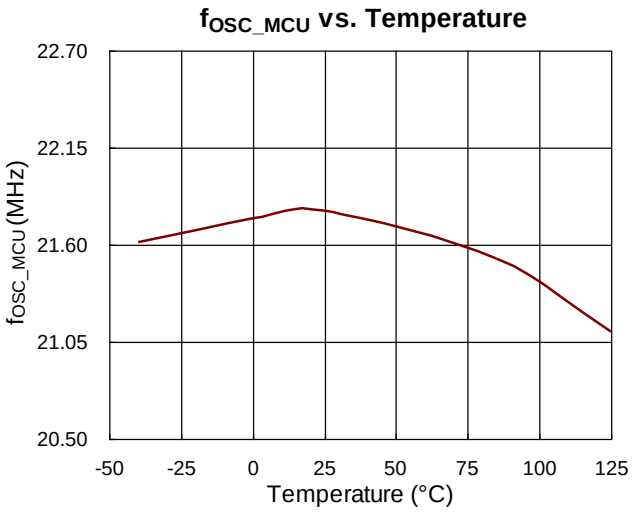


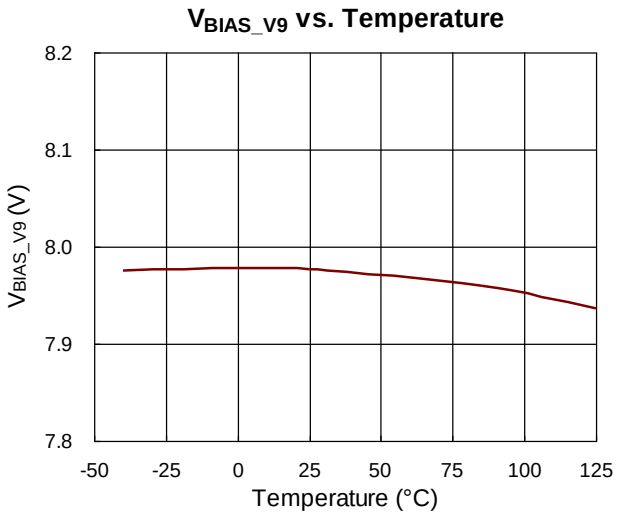


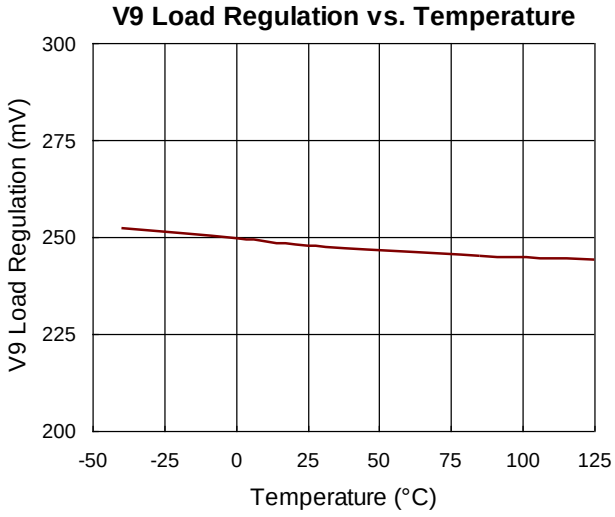


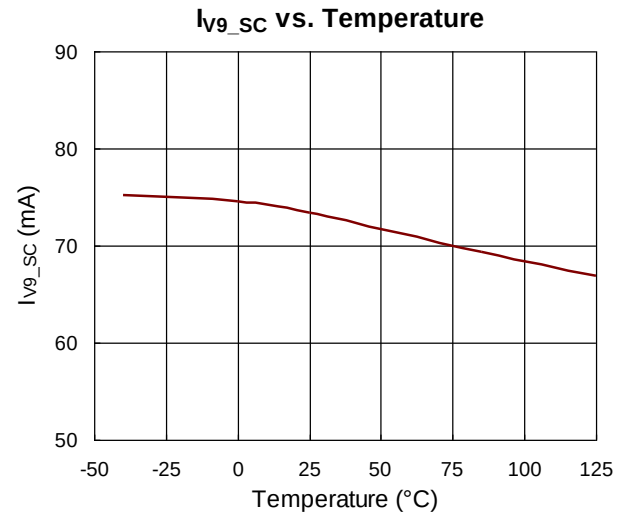


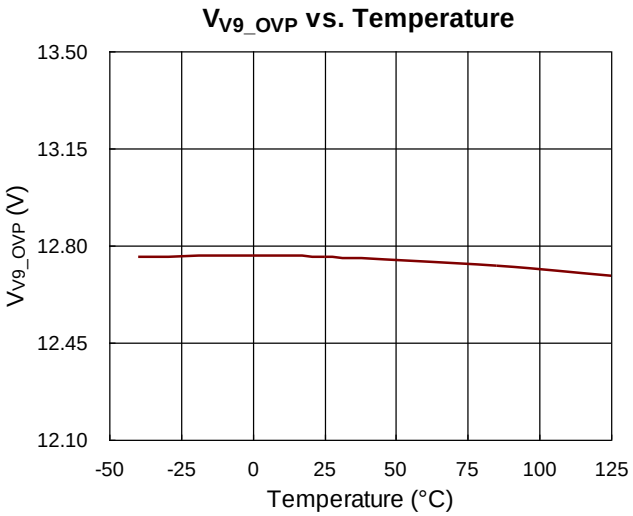


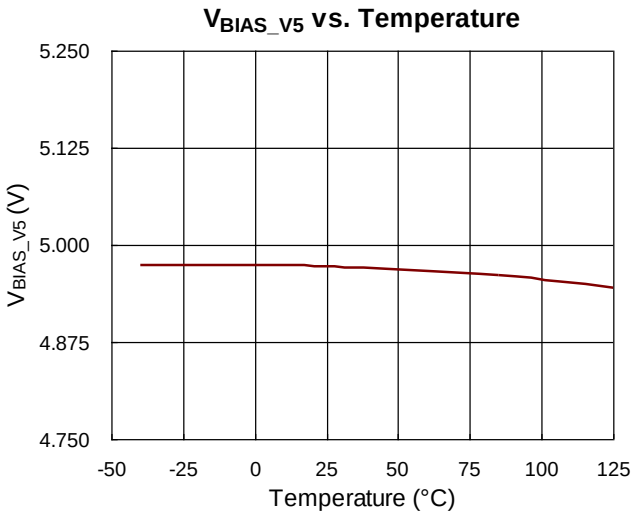


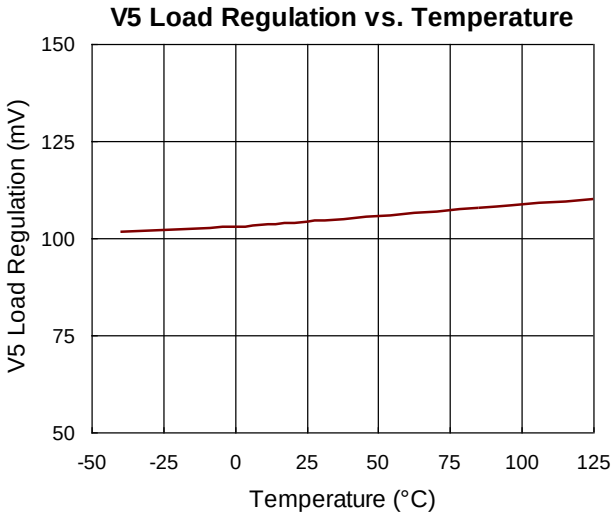


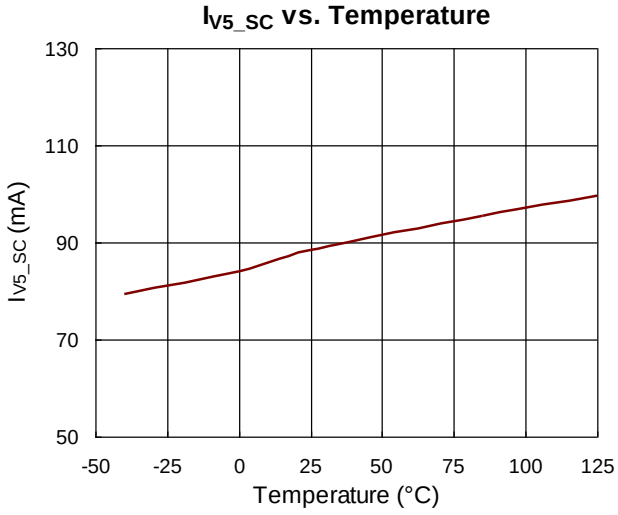


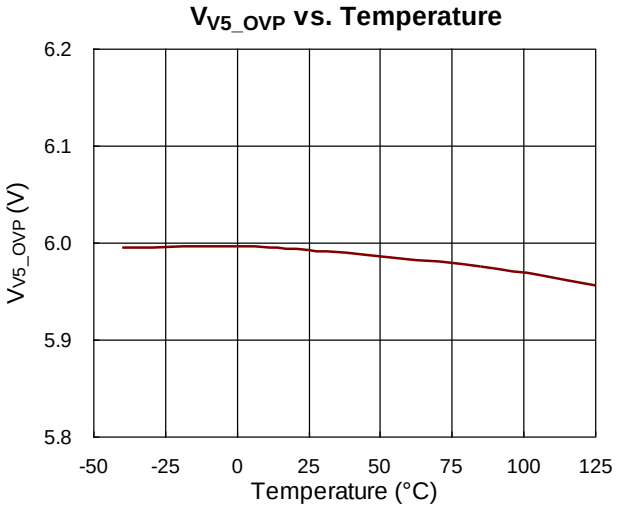


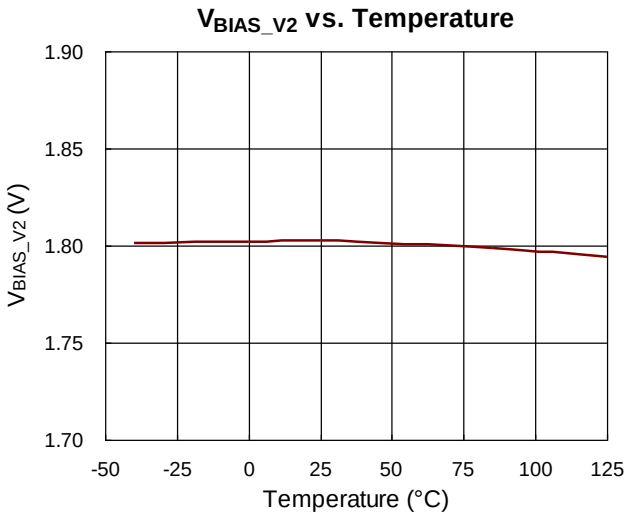


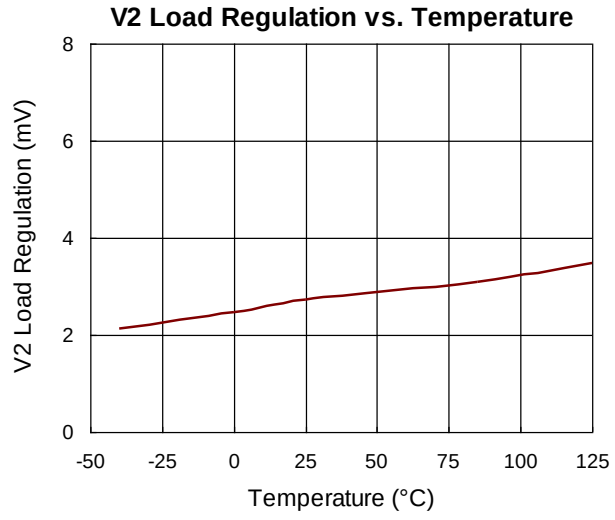




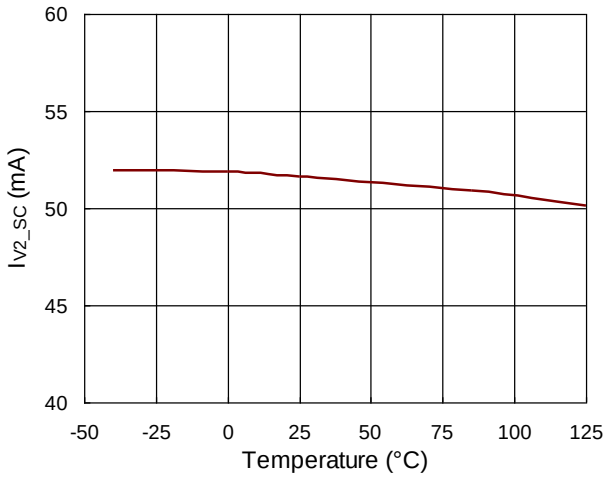




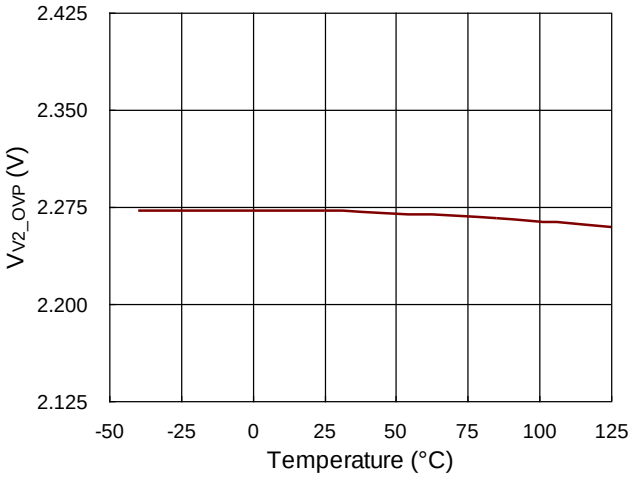




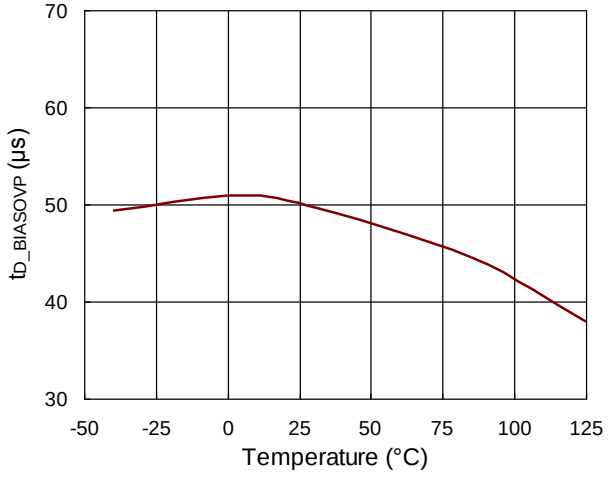
I_{V2_SC} vs. Temperature



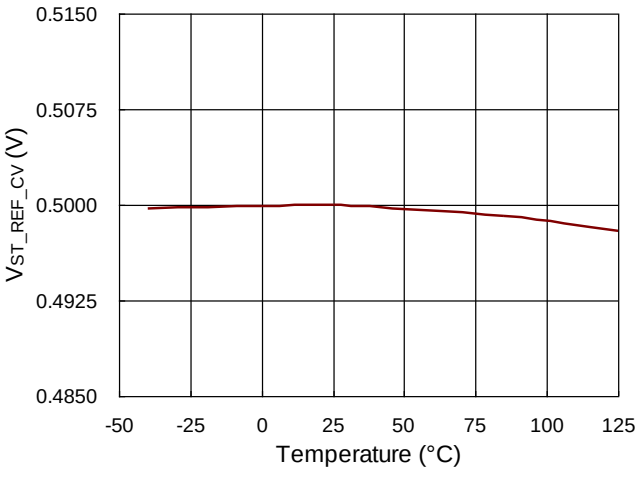
V_{V2_OVP} vs. Temperature



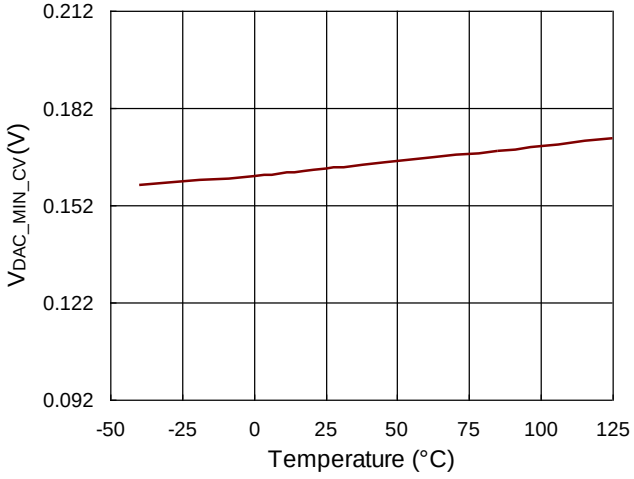
$t_{D\_BIASOVP}$ vs. Temperature



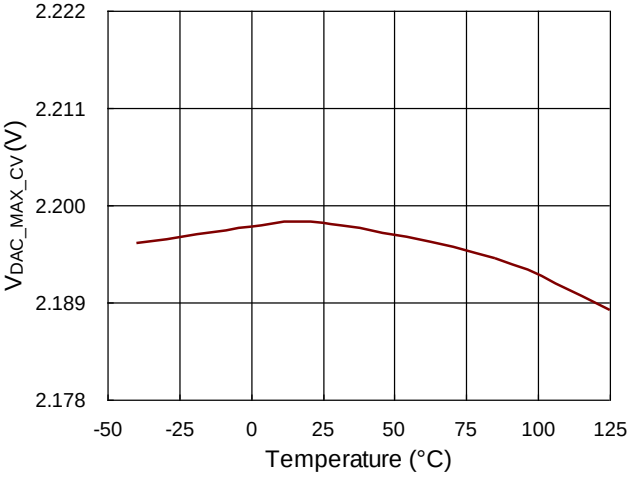
$V_{ST\_REF\_CV}$ vs. Temperature

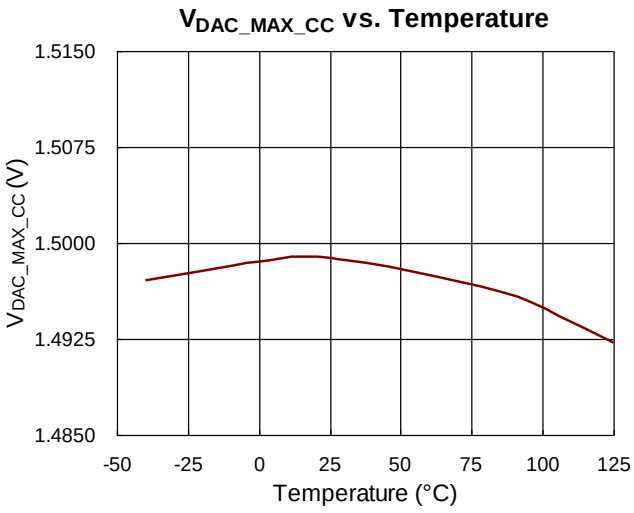


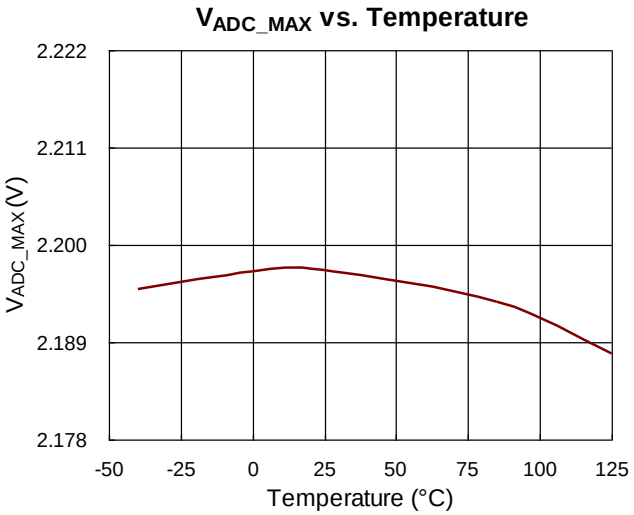
$V_{DAC\_MIN\_CV}$ vs. Temperature

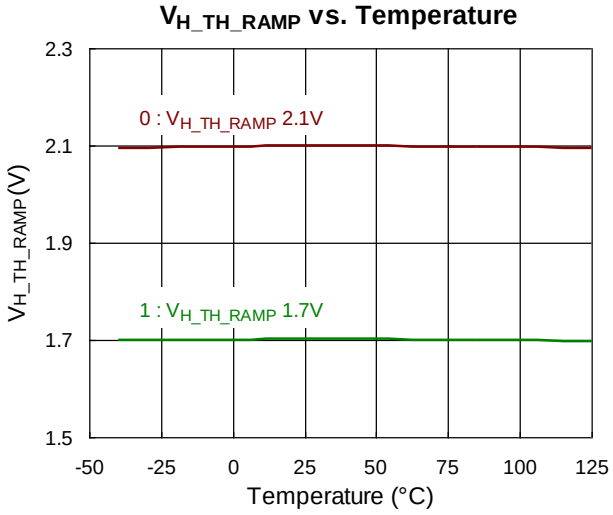


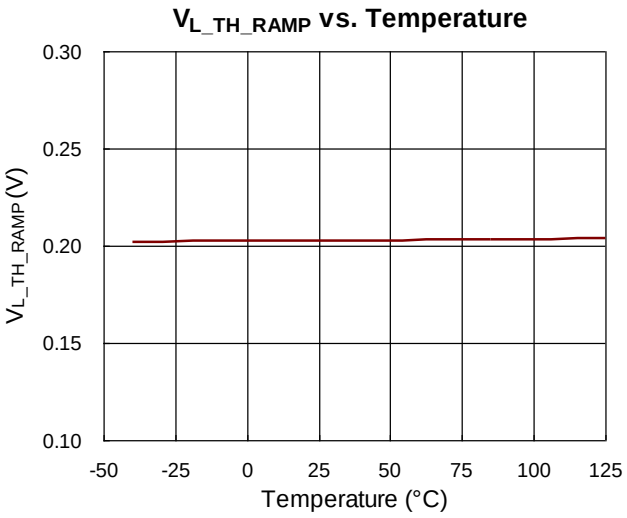
$V_{DAC\_MAX\_CV}$ vs. Temperature

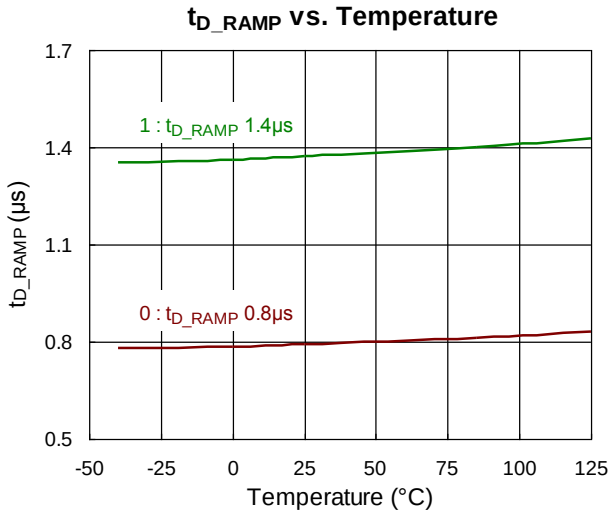


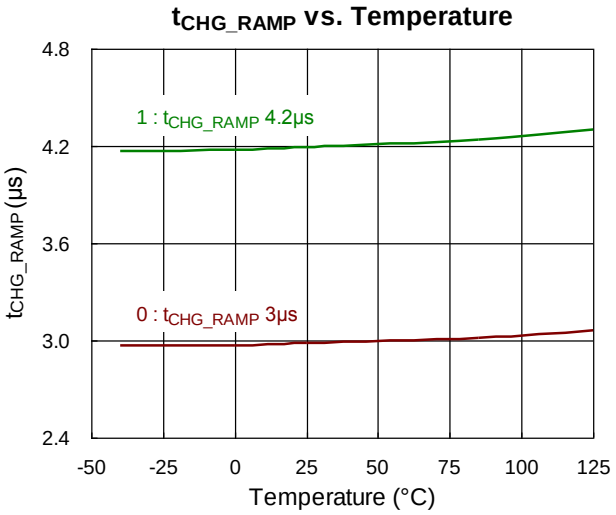


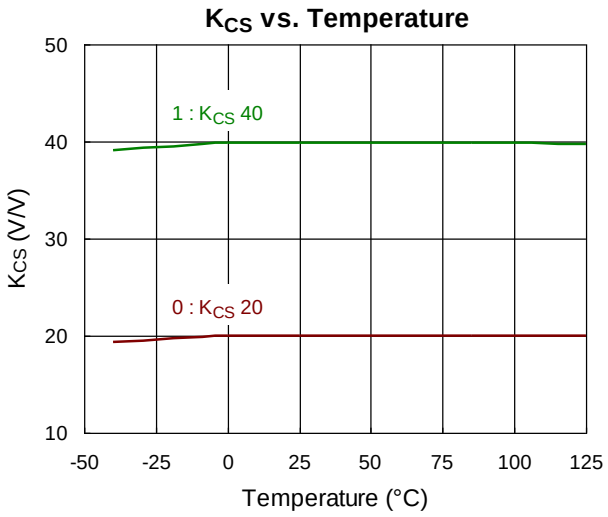


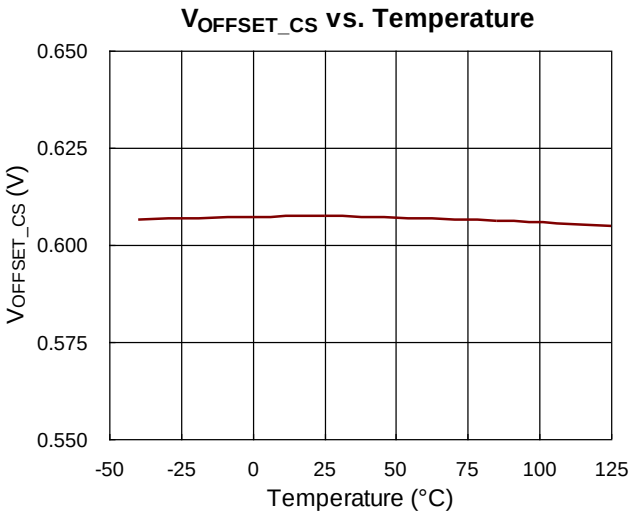


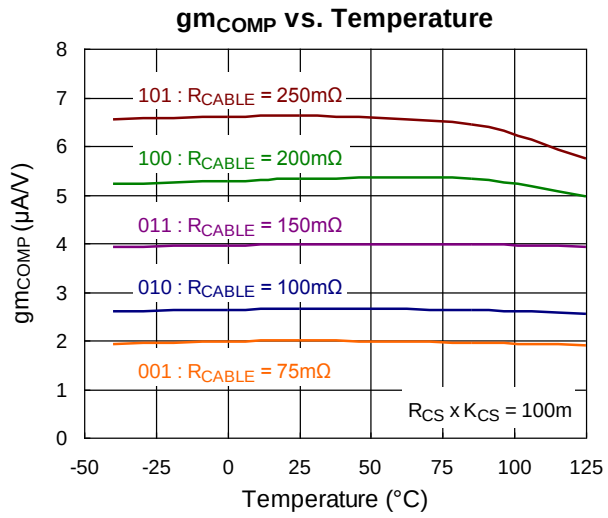


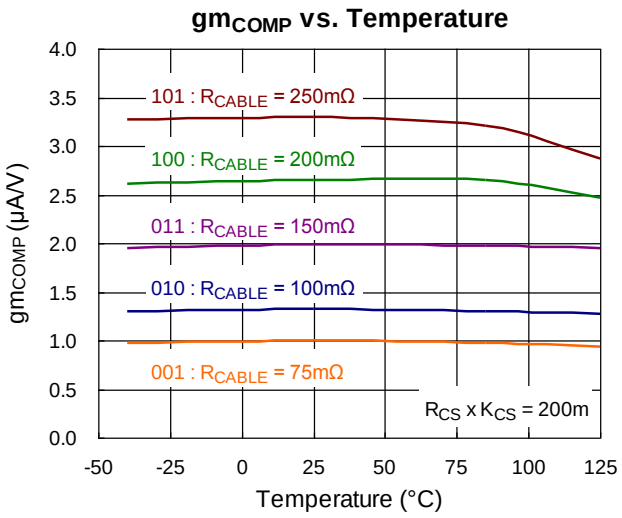


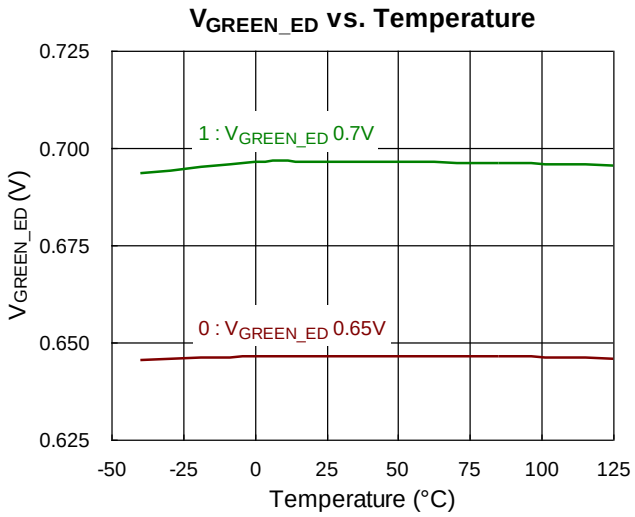


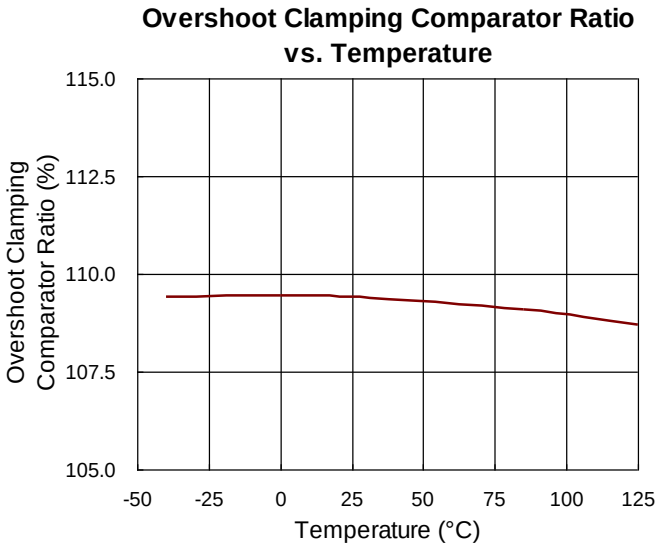




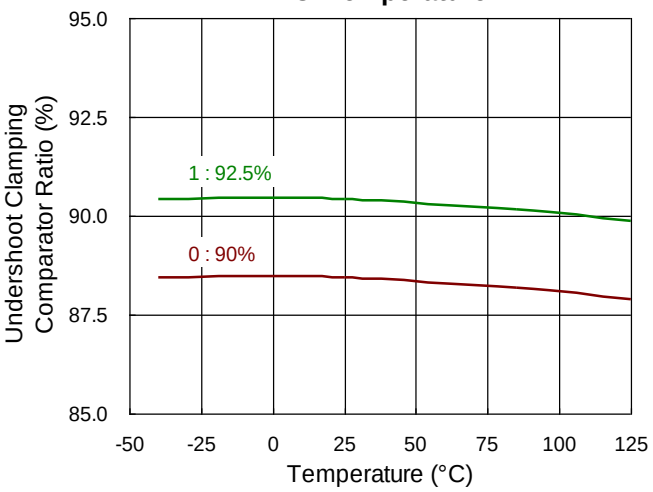




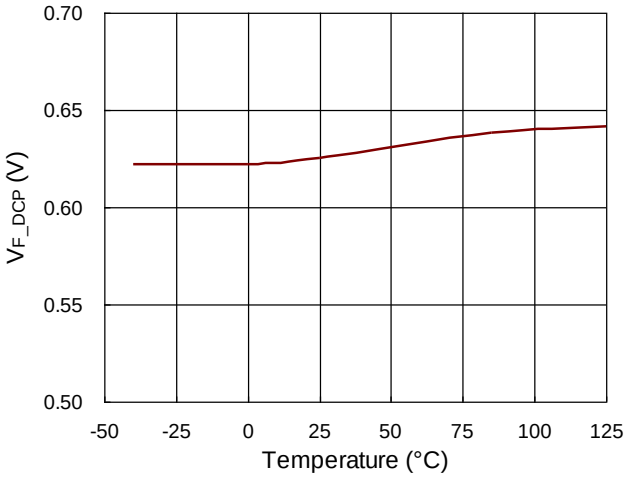




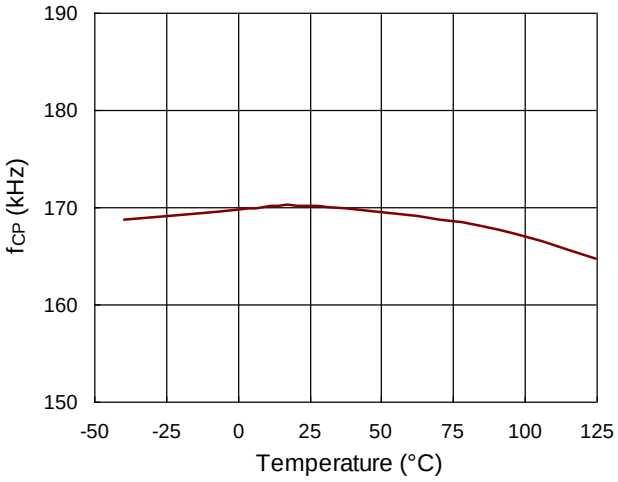
Undershoot Clamping Comparator Ratio vs. Temperature



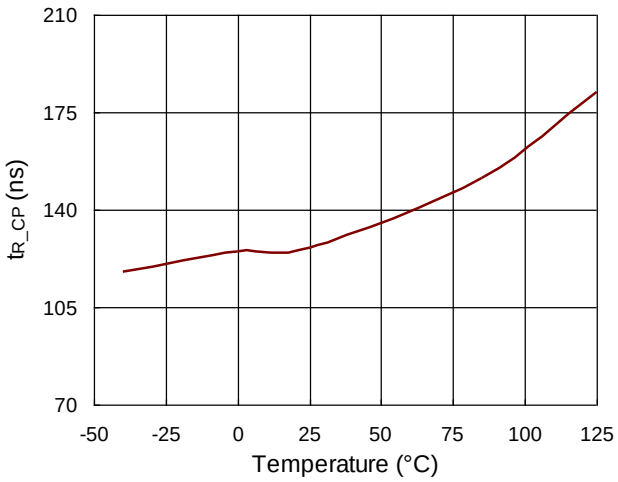
V_{F_DCP} vs. Temperature



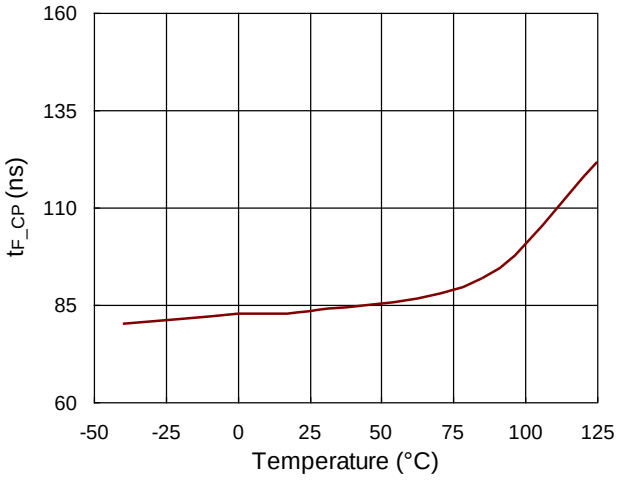
f_{CP} vs. Temperature



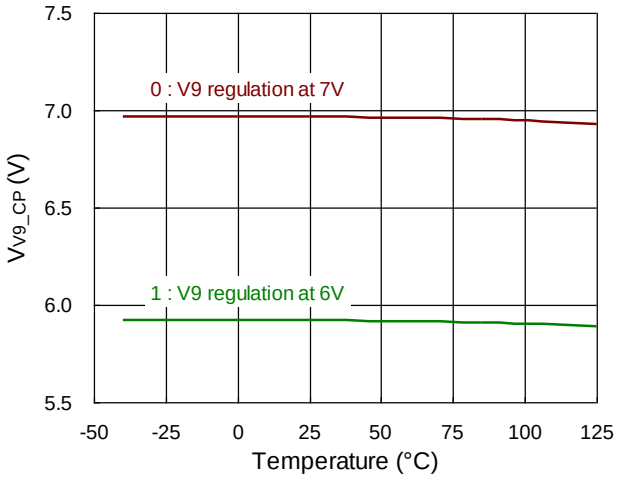
t_{R_CP} vs. Temperature

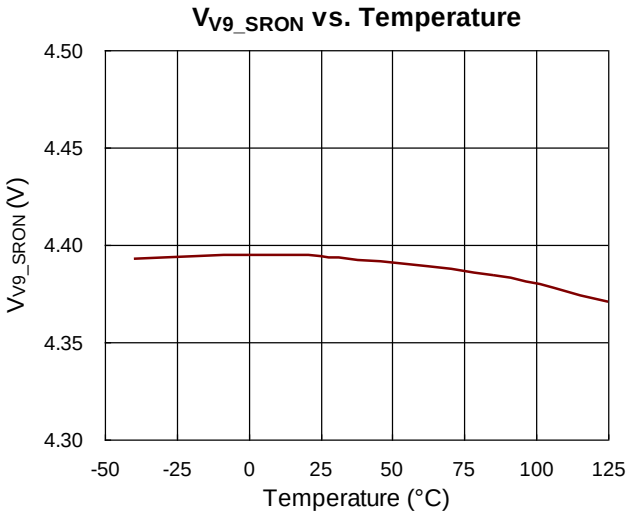


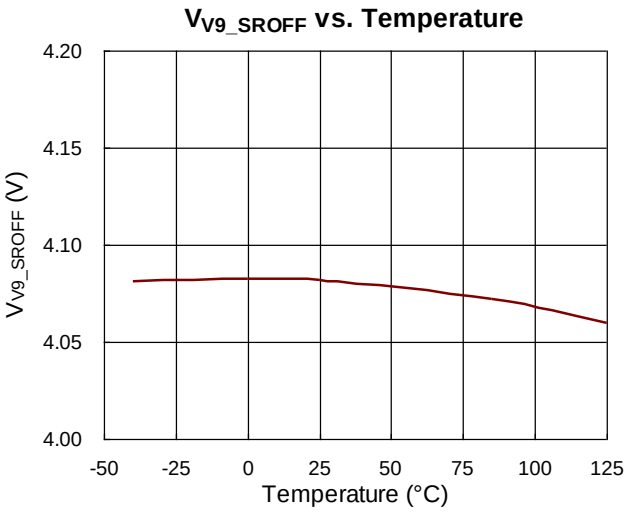
t_{F_CP} vs. Temperature

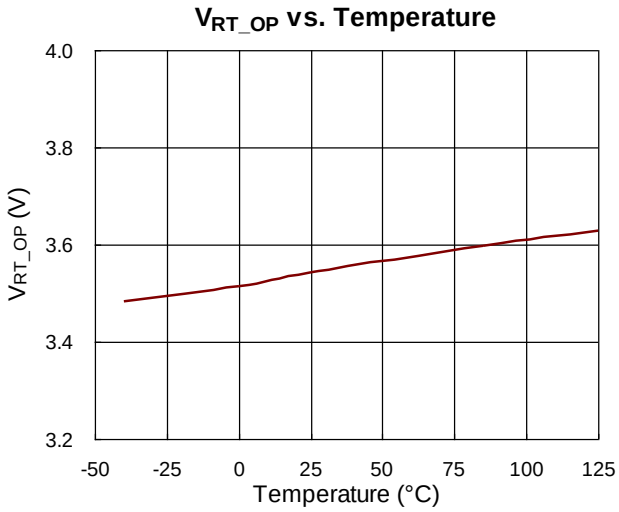


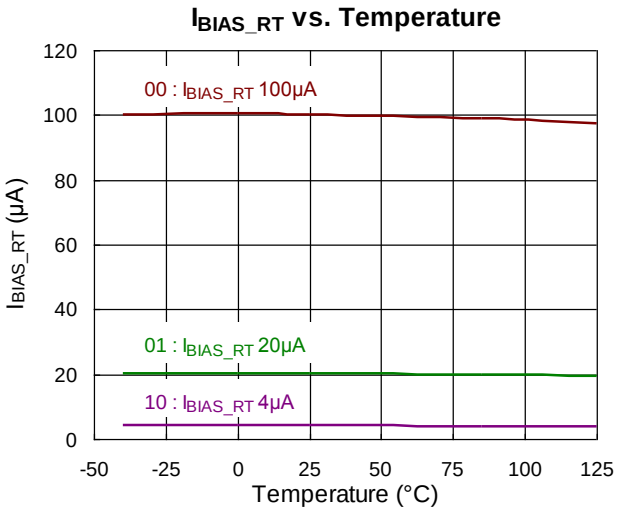
V_{V9_CP} vs. Temperature

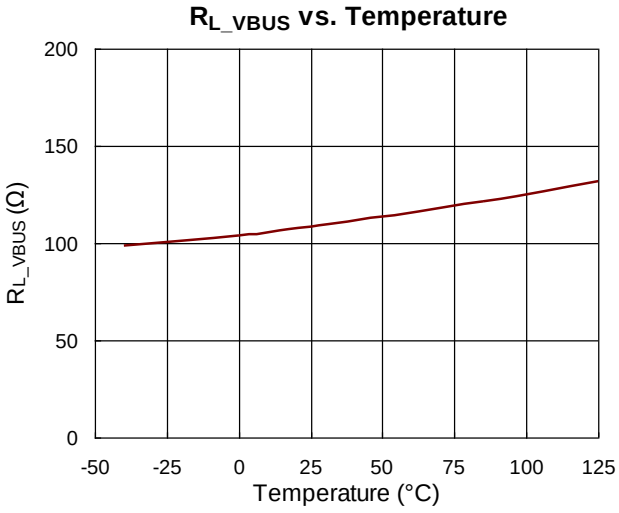


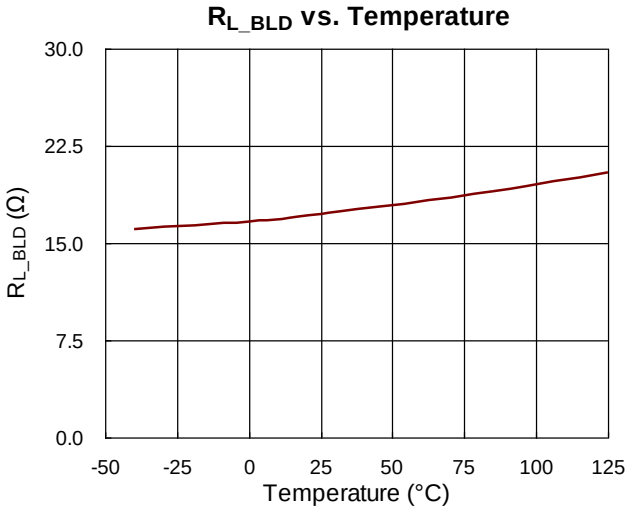


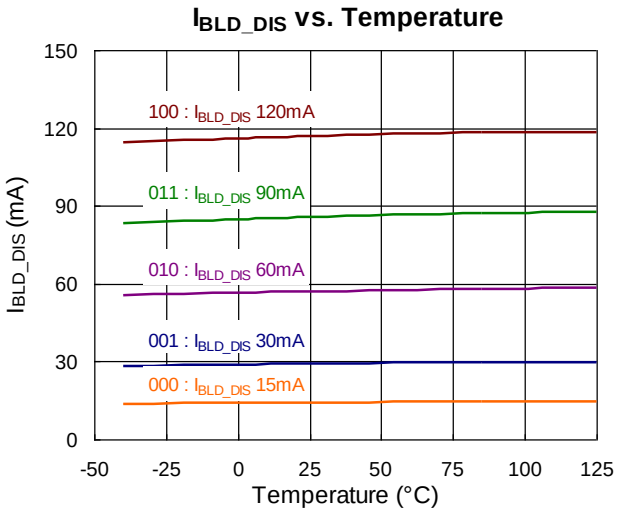


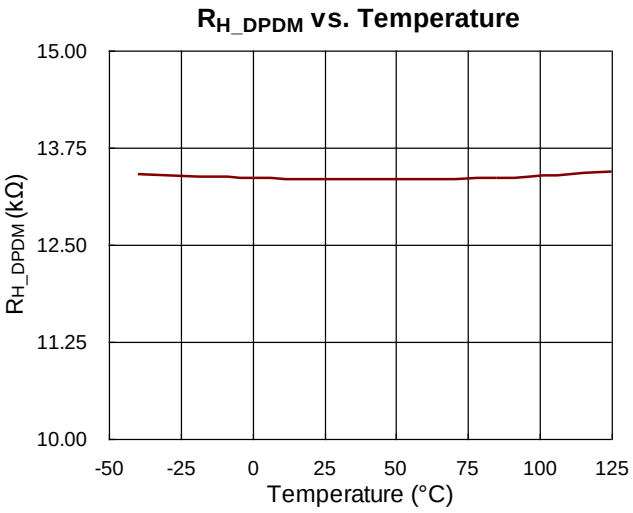


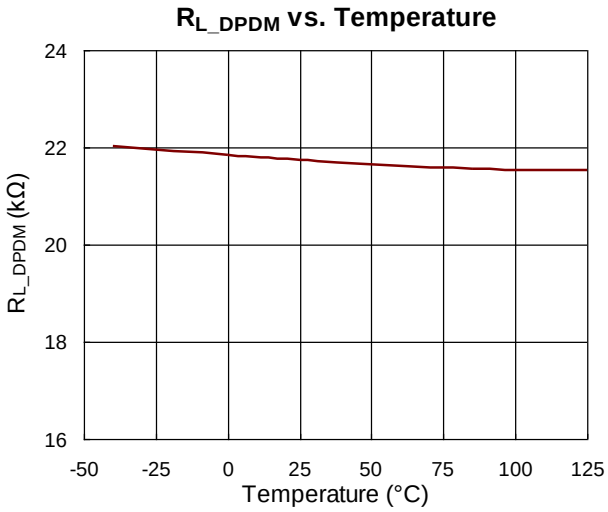


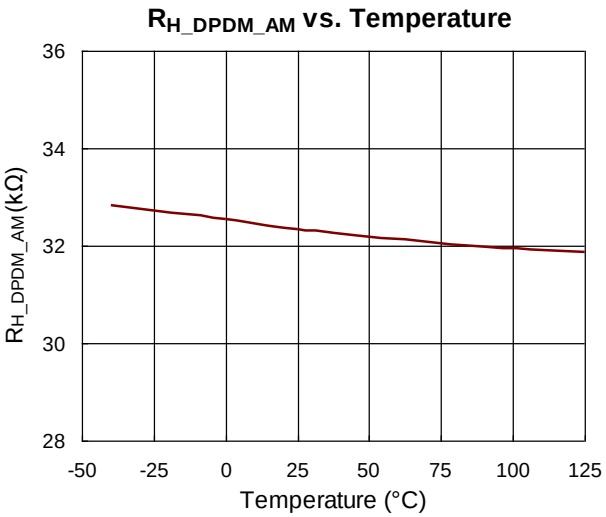


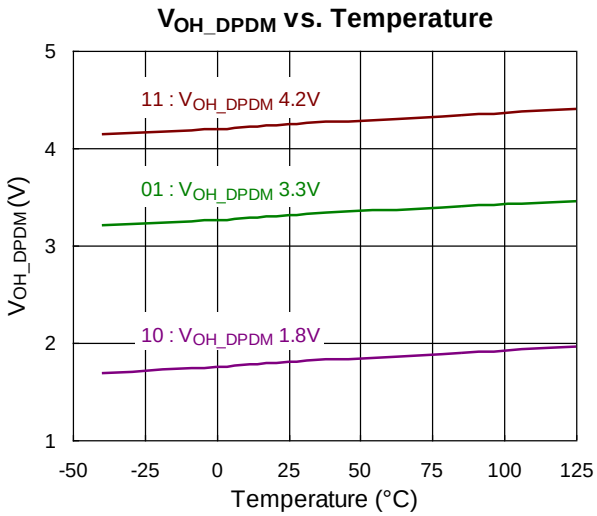


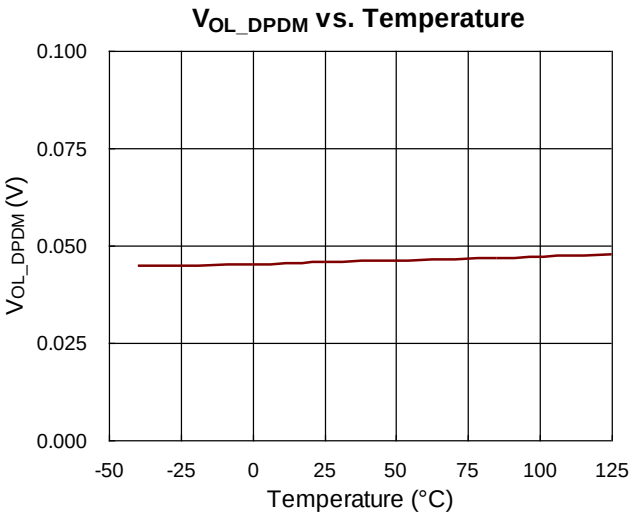


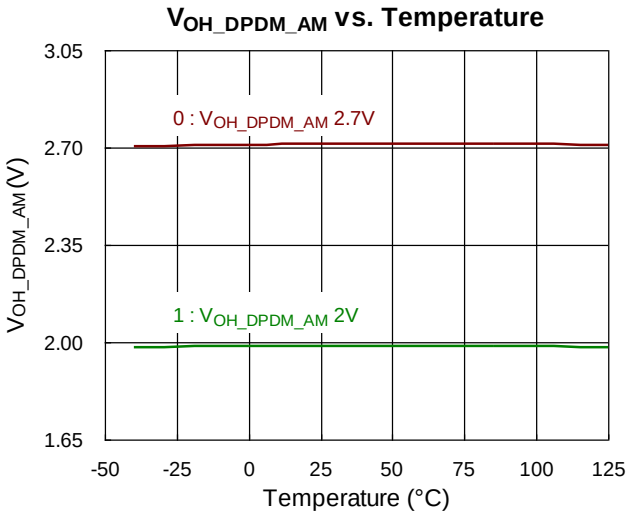


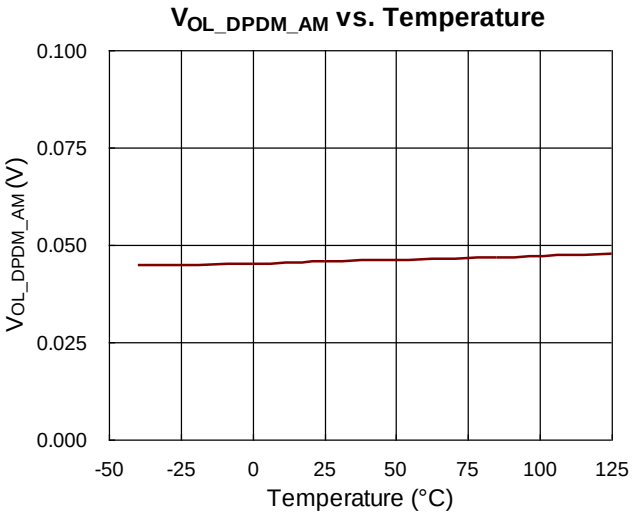


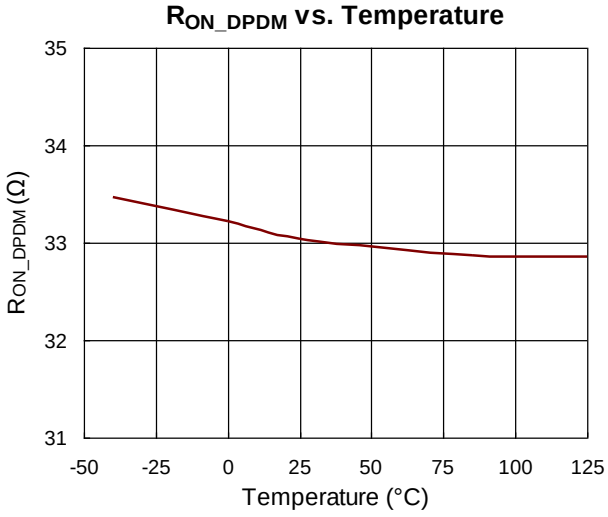


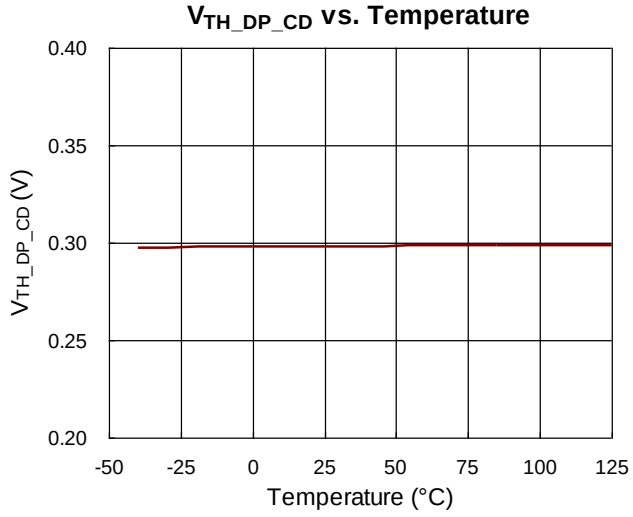


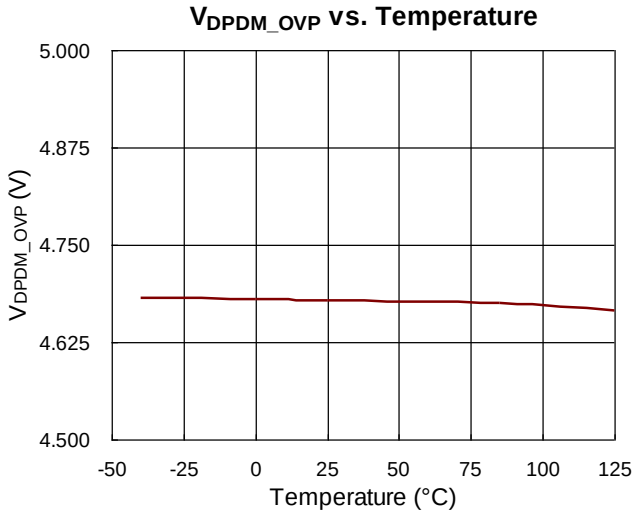


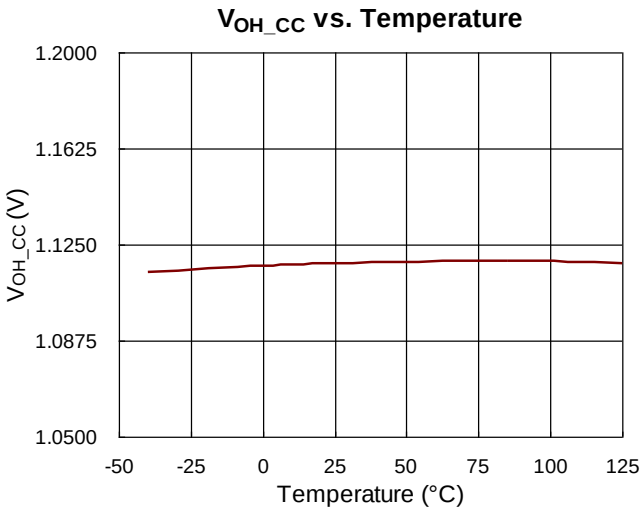


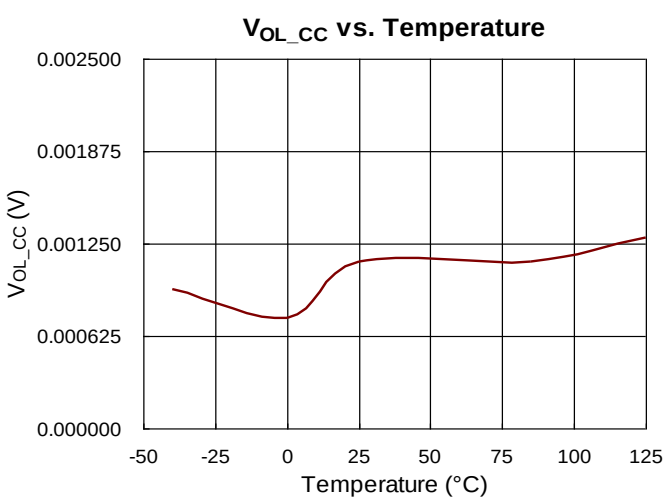


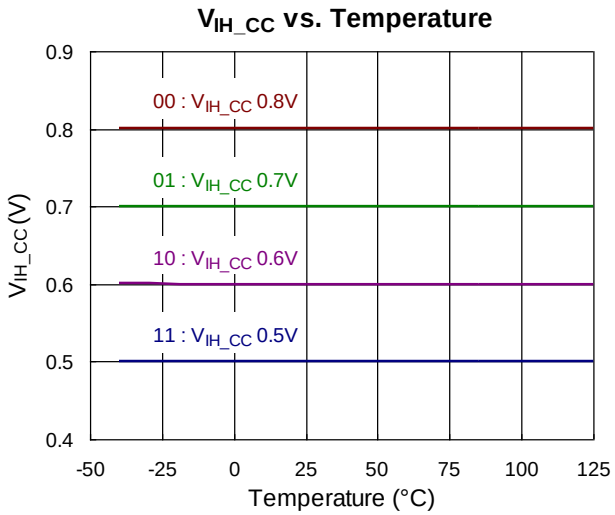


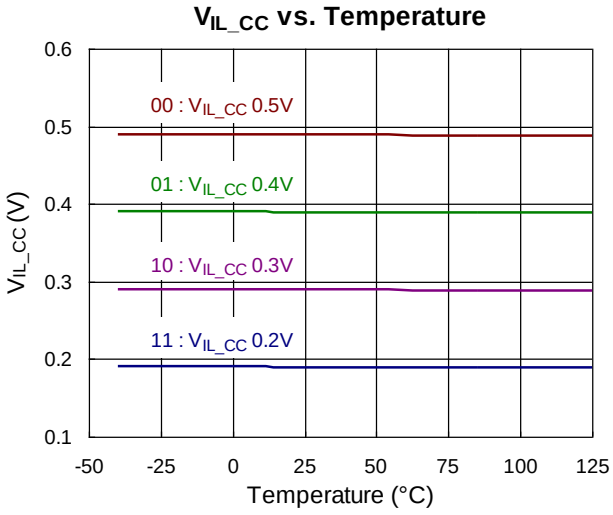


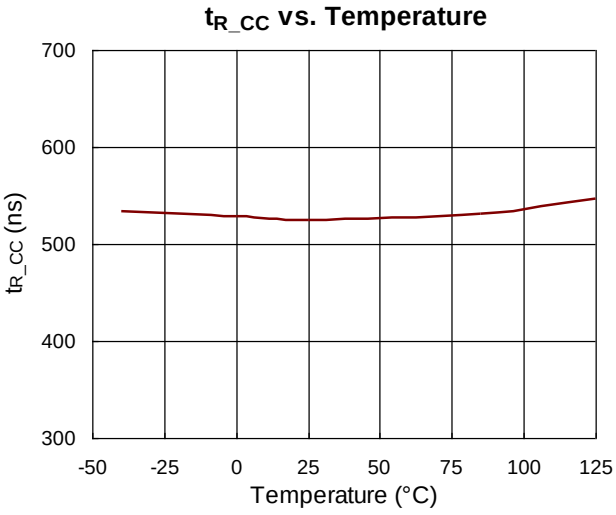


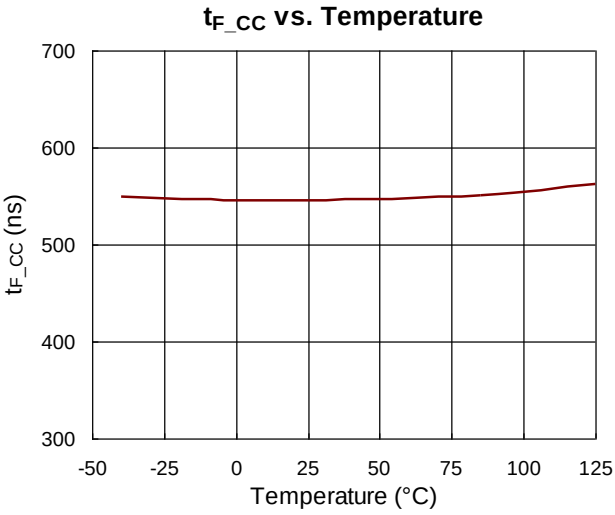


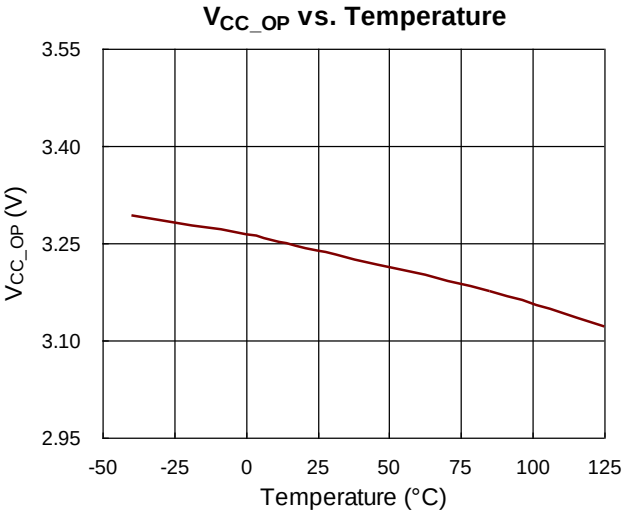


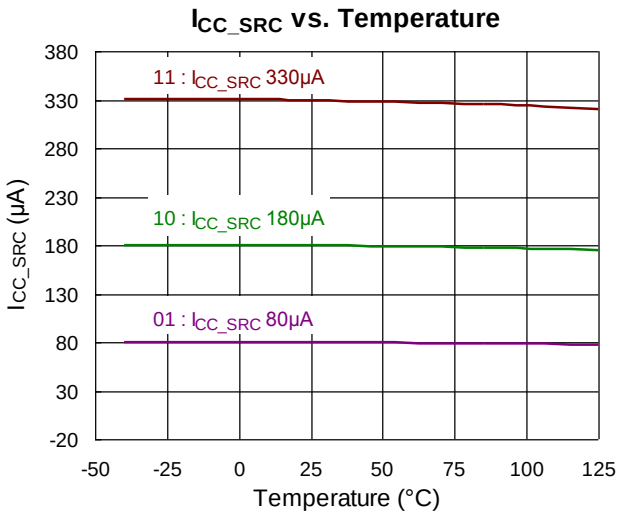


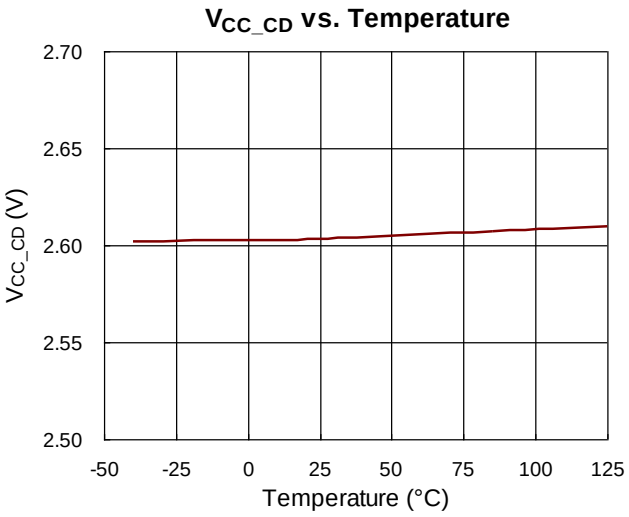


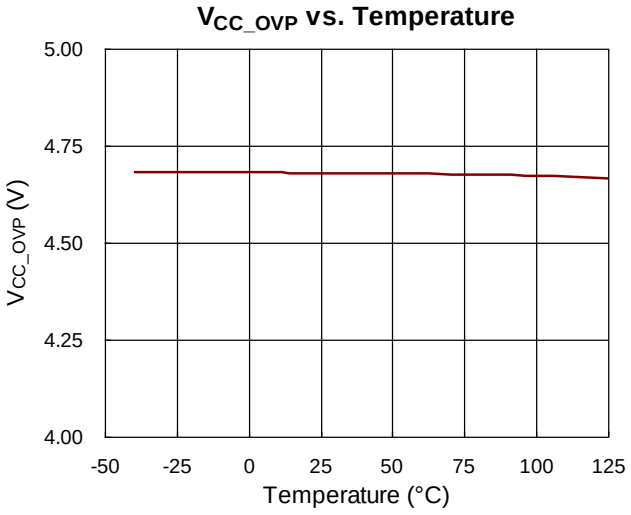


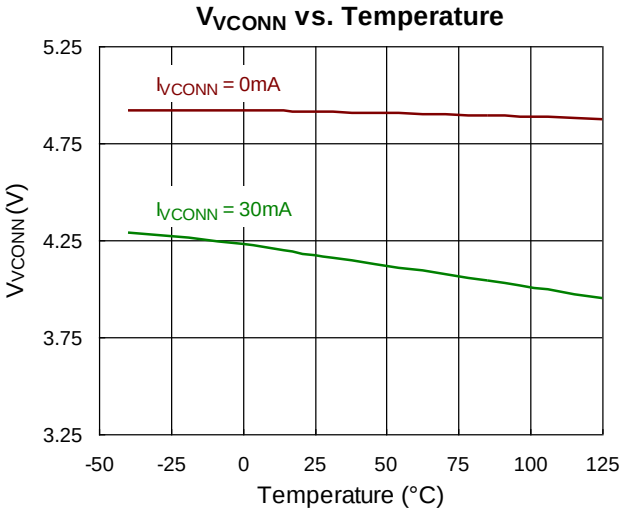


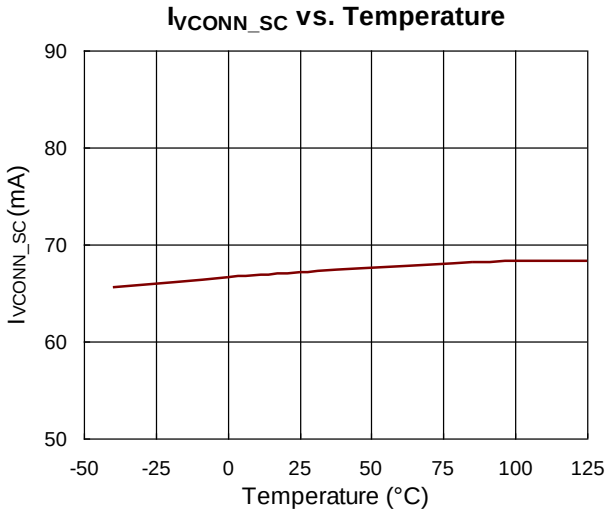


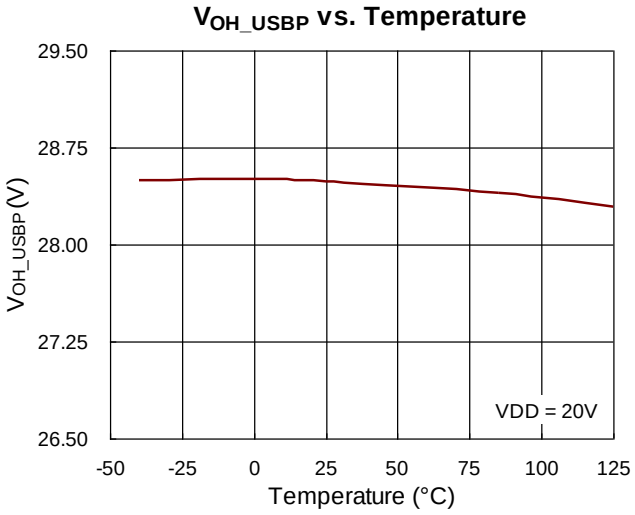


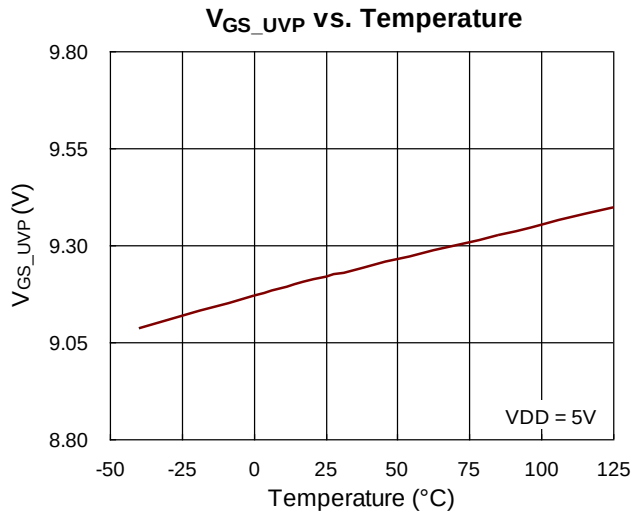


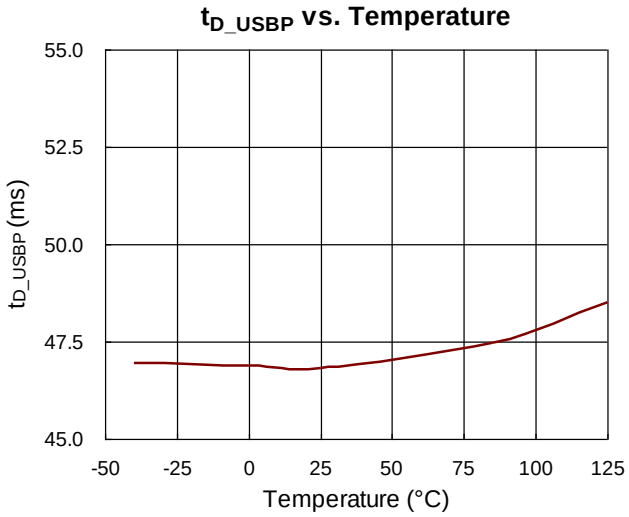


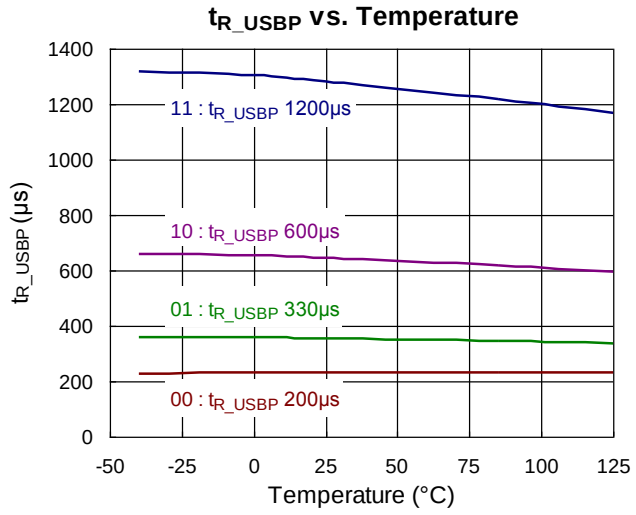


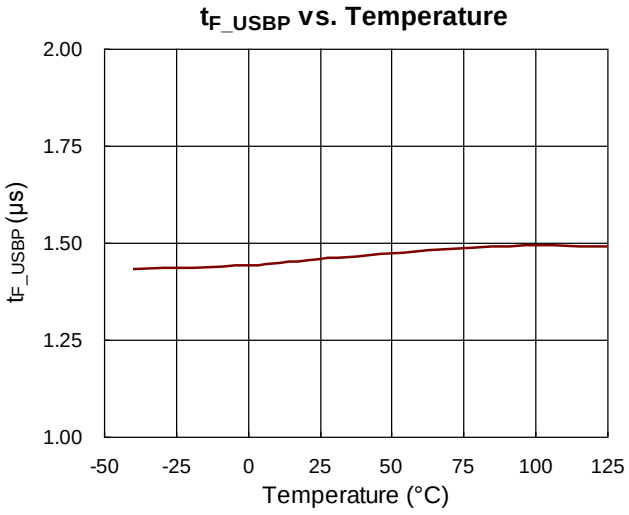


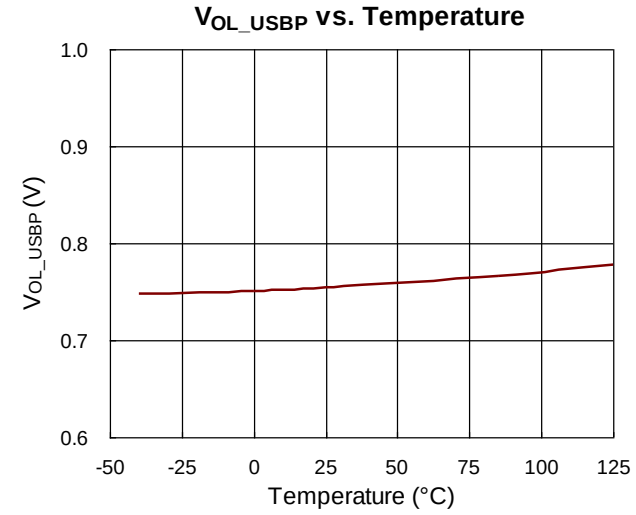


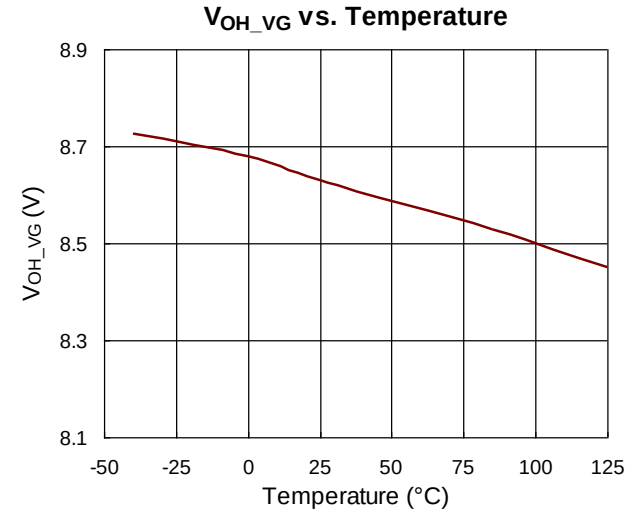




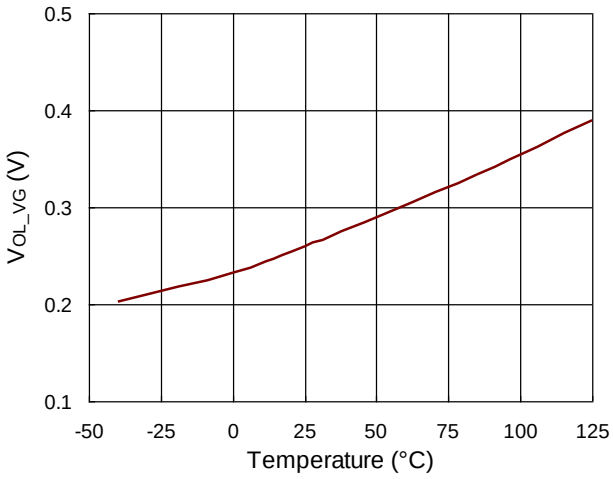




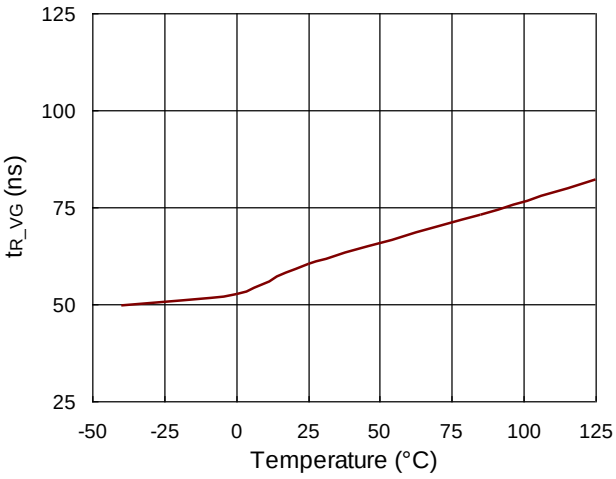




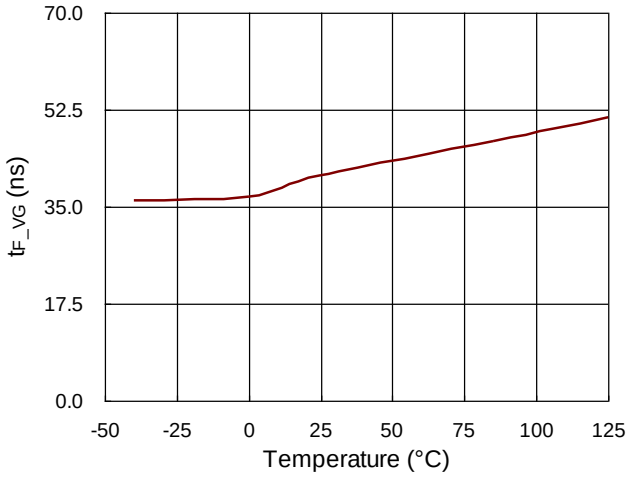
V_{OL_VG} vs. Temperature



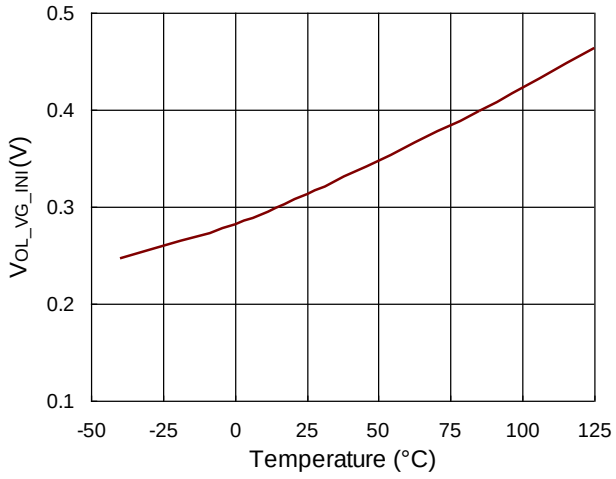
t_{R_VG} vs. Temperature



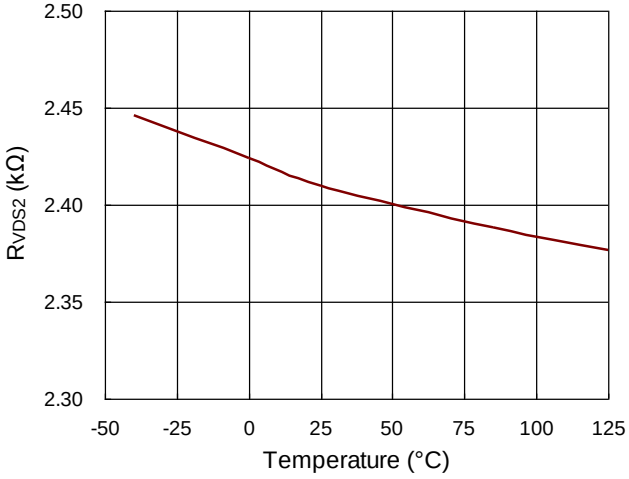
t_{F_VG} vs. Temperature



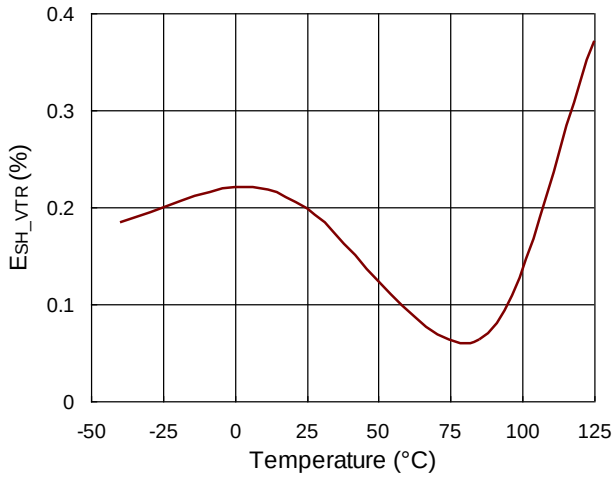
$V_{OL\_VG\_INI}$ vs. Temperature



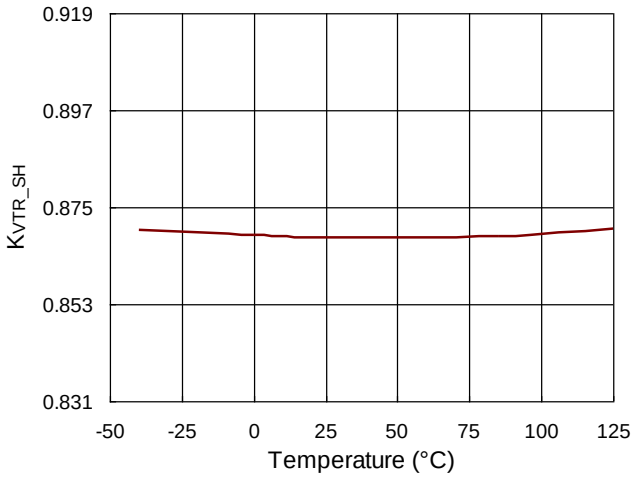
R_{VDS2} vs. Temperature



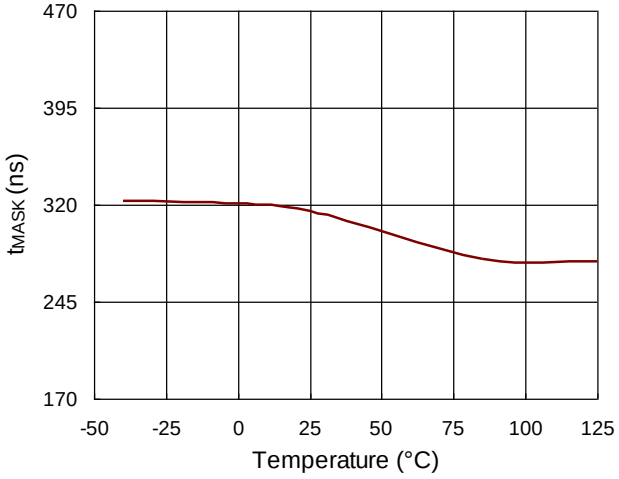
E_{SH_VTR} vs. Temperature



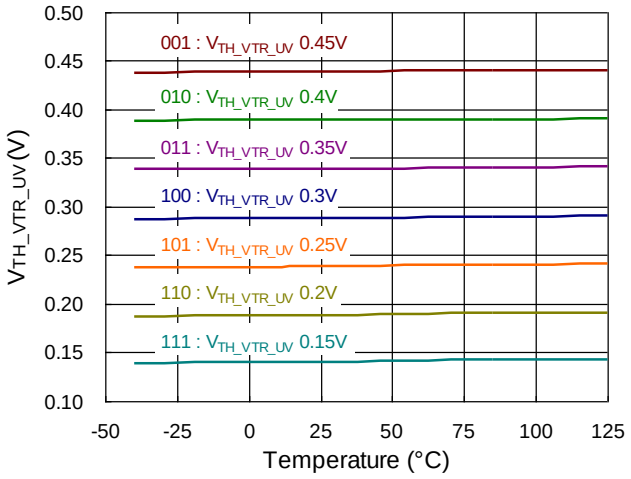
K_{VTR_SH} vs. Temperature



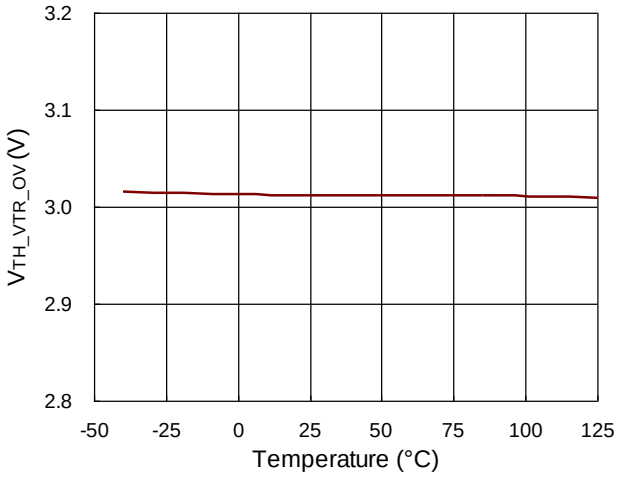
t_{MASK} vs. Temperature



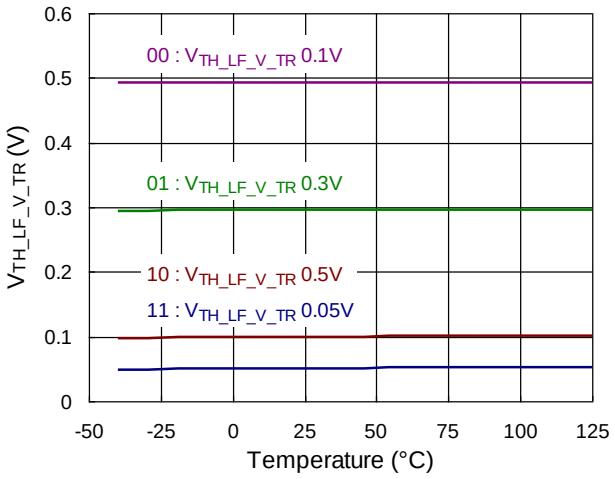
$V_{TH\_VTR\_UV}$ vs. Temperature



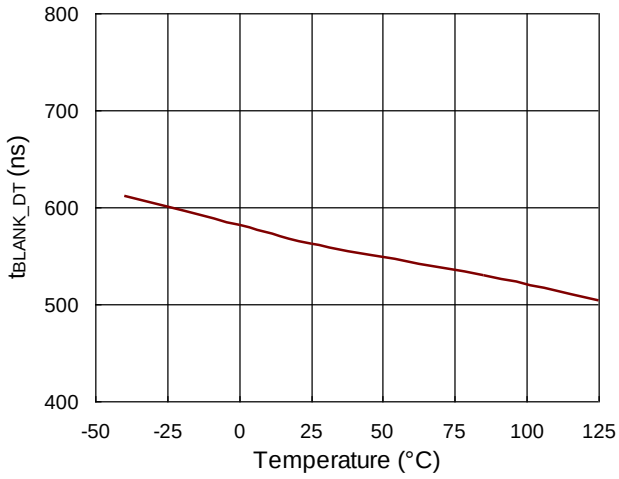
$V_{TH\_VTR\_OV}$ vs. Temperature

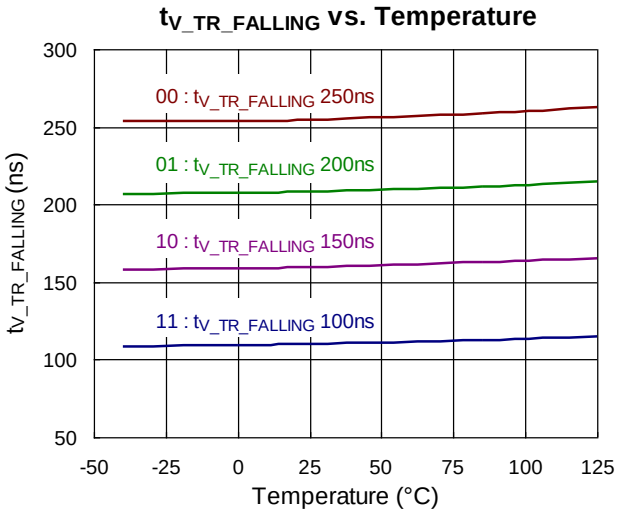


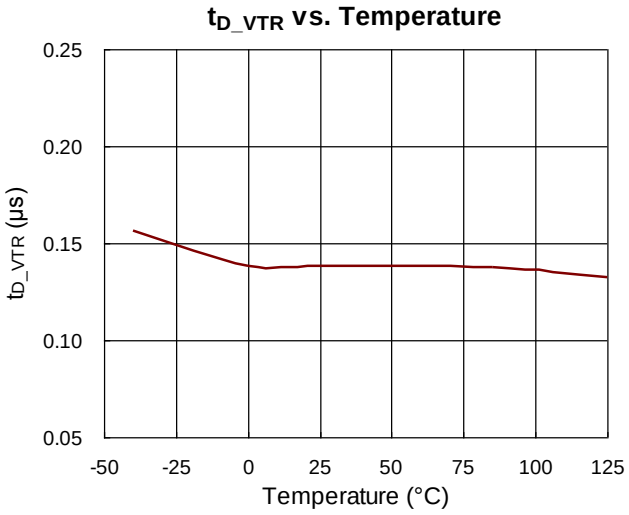
$V_{TH\_LF\_V\_TR}$ vs. Temperature

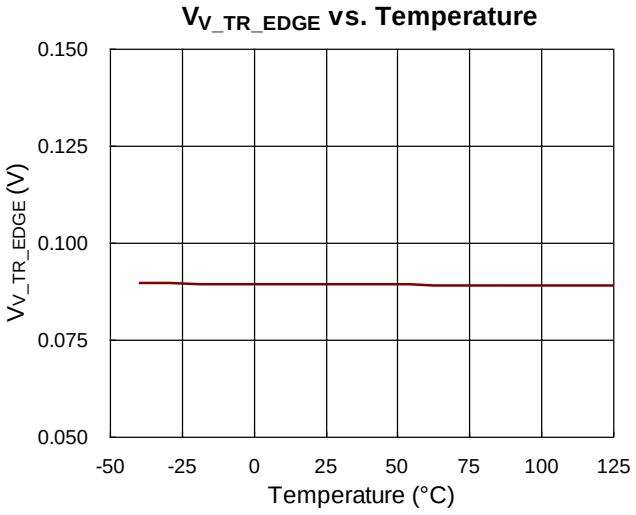


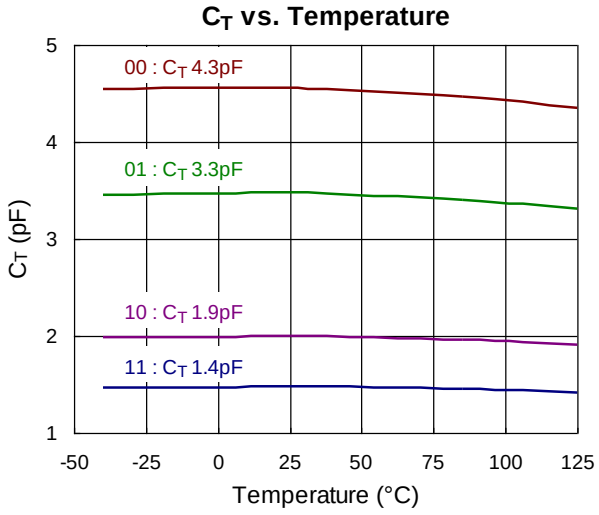
t_{BLANK_DT} vs. Temperature

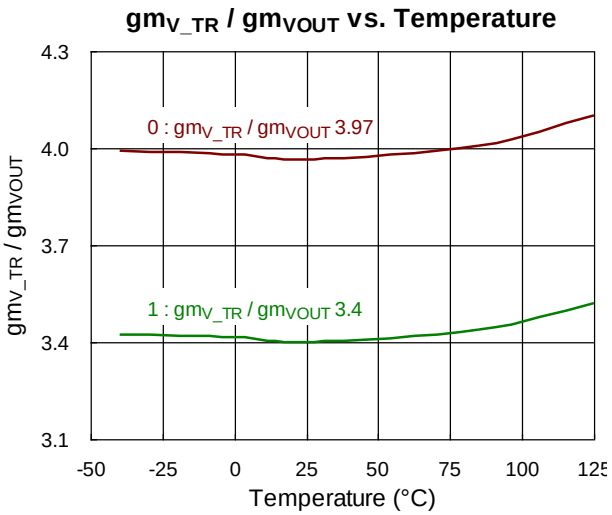


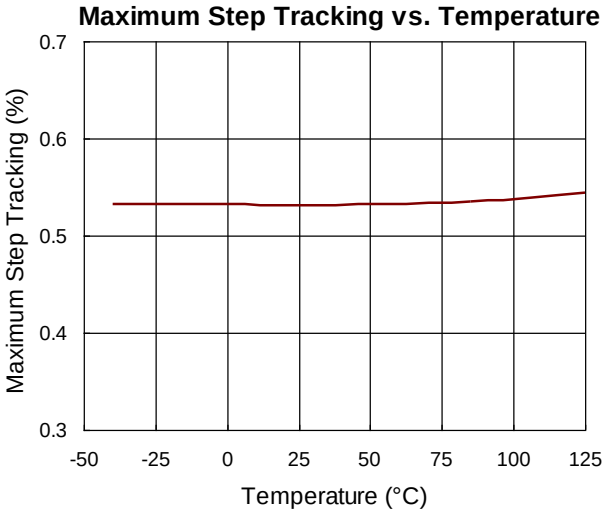


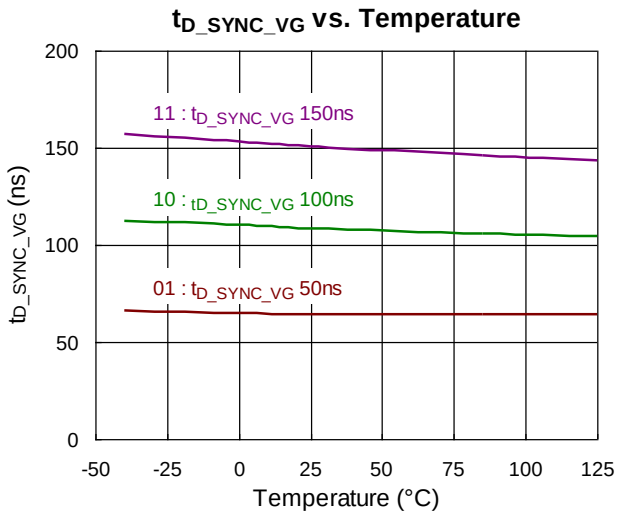


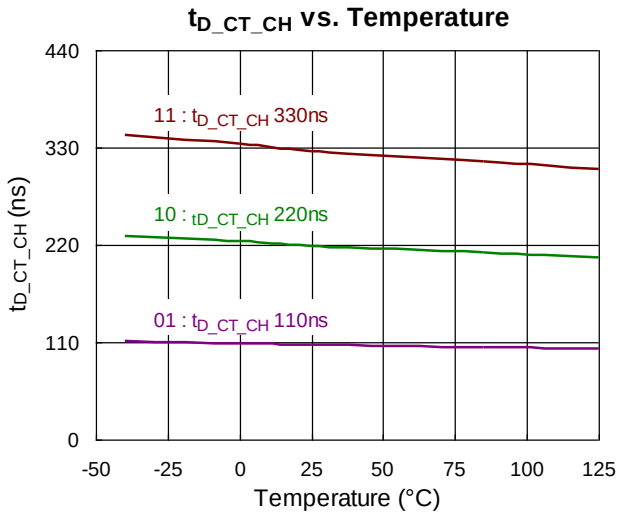


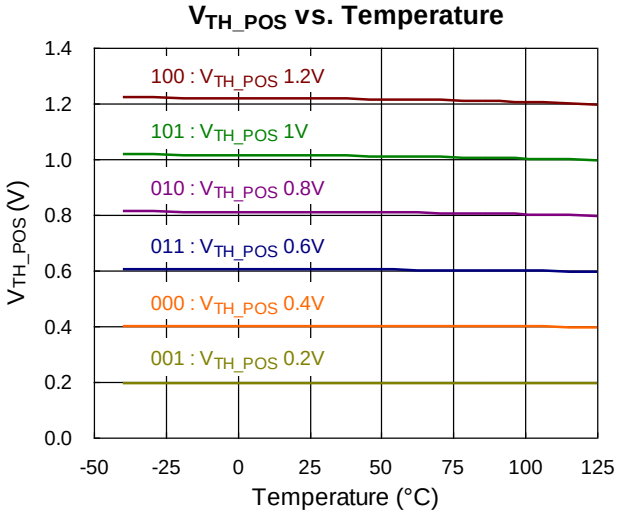


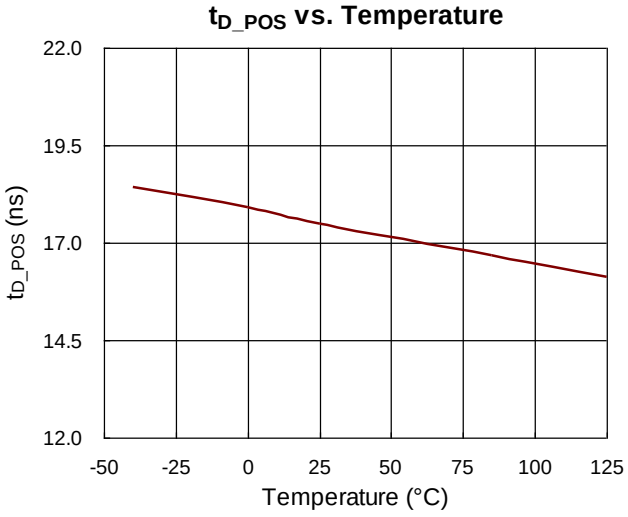


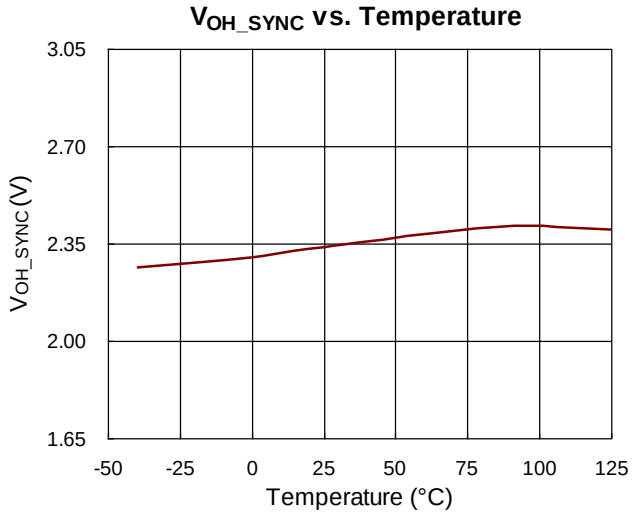


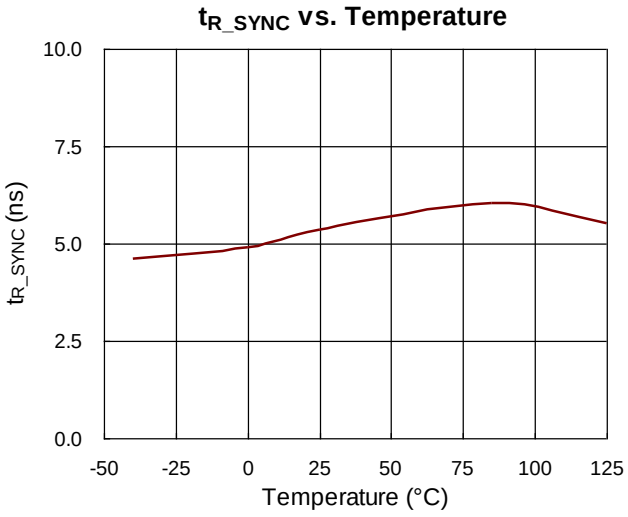


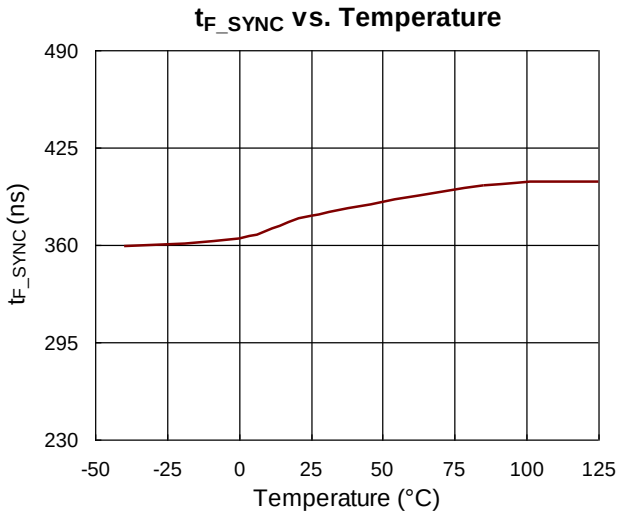


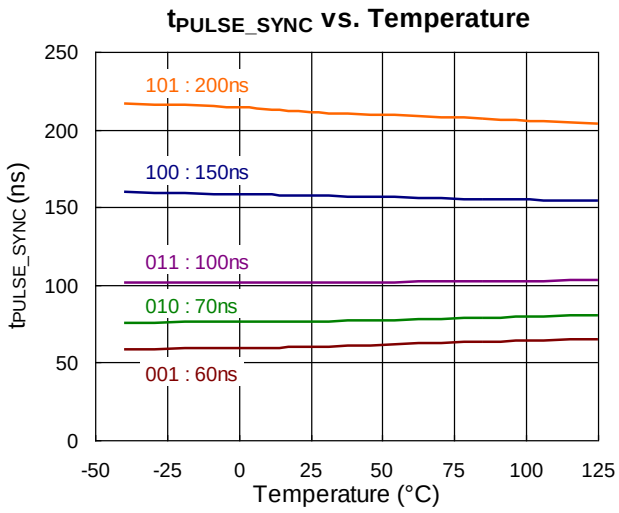


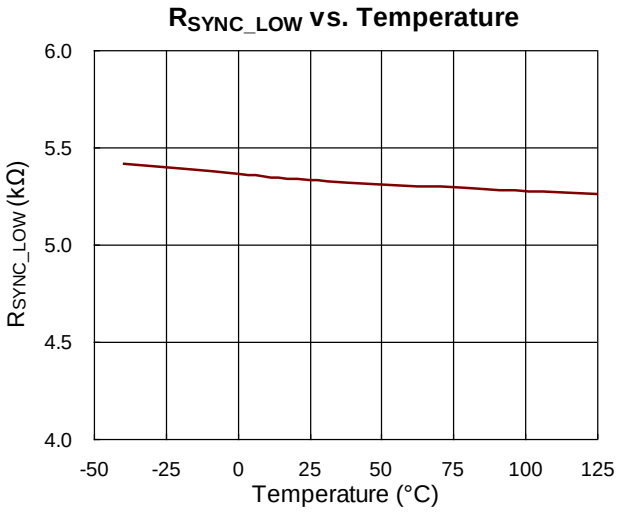


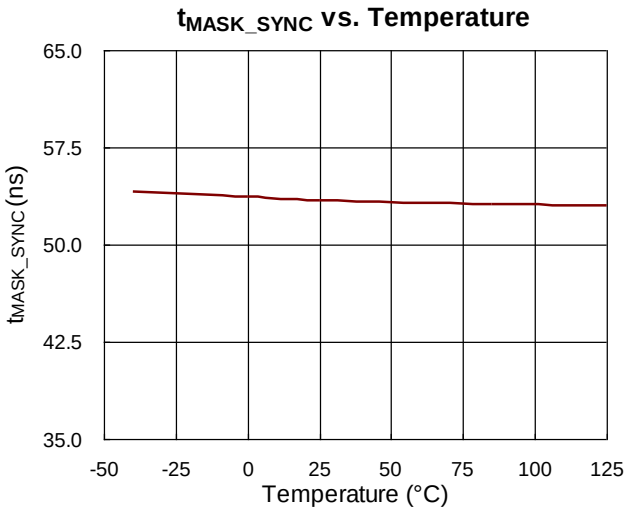


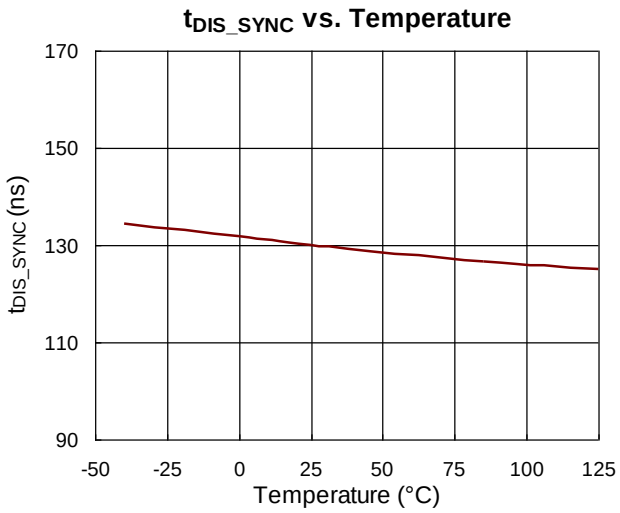


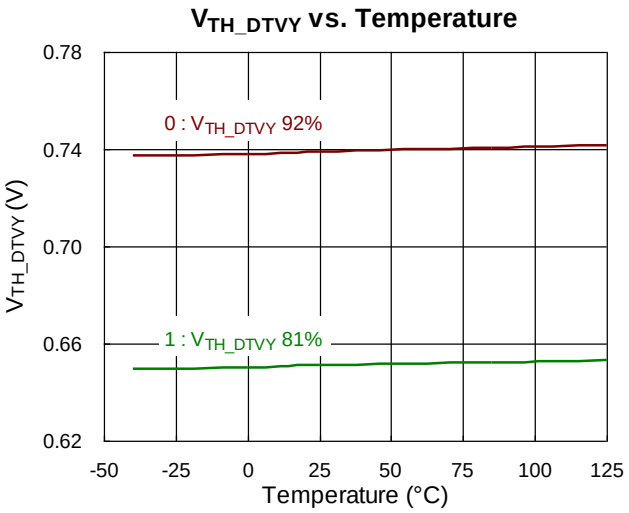


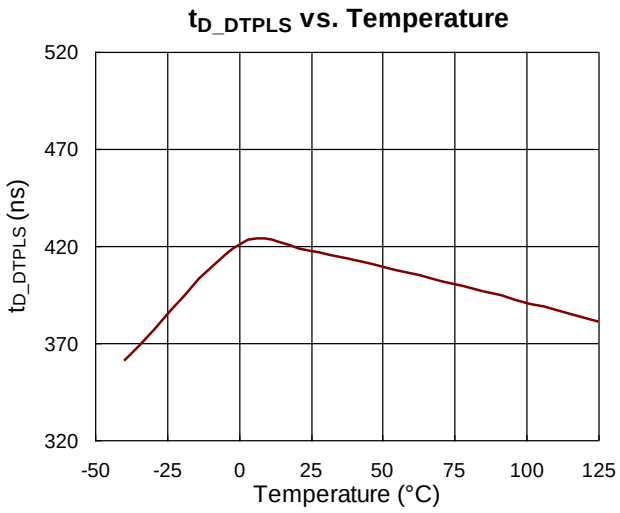


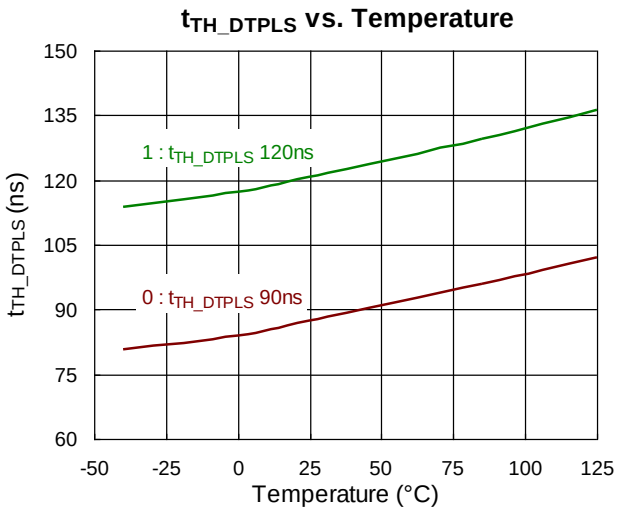


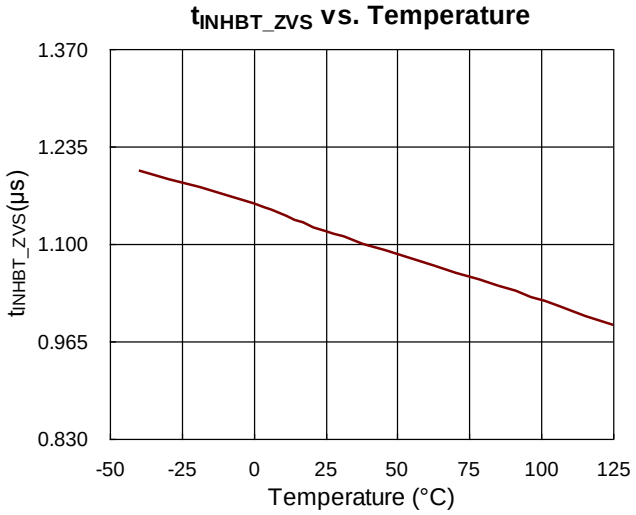












Application Information

Constant Voltage (CV) Loop

As shown in Figure 6, the RT7208EB incorporates 2 error amplifiers (EA) to regulate output voltage and current, respectively. The output voltage is determined as :

$V_{OUT} = K_{FB} \times V_{REF\_CV}$

Where

$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10$ (typ.)

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, and its digital counterpart, which is controlled by the MCU, as shown in Functional Block Diagram.

Constant-Current (CC) Loop and Current-Sense Amplifier

The RT7208EB integrates a virtually-zero input-offset-voltage current-sense amplifier with differential-mode inputs to minimize noise interference. The voltage gain of 20 or 40 can be set by the internal register. The amplified output current sense signal, sent to an ADC for A/D conversion, is monitored and processed by the MCU, and is also sent to the CC loop. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed by chargers' requirements.

Both the constant-voltage and constant-current compensation loops are connected to the feedback compensation. The output of feedback compensation, V_{OPTO}, has a lower level at light load and a higher level at heavy load. The V_{OPTO} decides the transmitted time and voltage level of SYNC signal through a pulse transformer, and the pulse transformer isolates the secondary side from the primary side. The primary side detects the height and width of feedback compensated signal from SYNC to achieve output voltage and output current regulation. Note that for better SYNC driver loss of the pulse transformer, the inductance of pulse transformer should be designed to cover

$$L_{PT} \geq \frac{V_{OH\_SYNC} \times t_{PULSE\_SYNC}}{I_{SYNC}}$$

L_{PT} : The inductance of pulse transformer

V_{OH_SYNC} : Output high voltage of SYNC

t_{PULSE_SYNC} : Pulse width of SYNC

I_{SYNC} : The minimum SYNC sourcing current

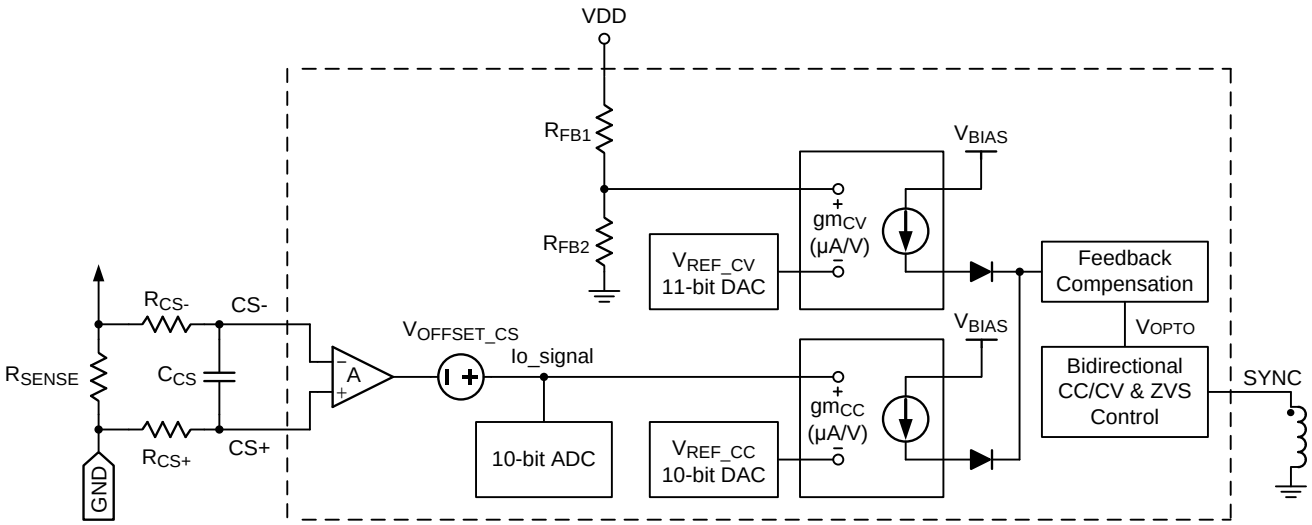


Figure 6. CV Loop and Current-Sense Amplifier

Internal Feedback Compensation

The RT7208EB has a built-in feedback compensator that optimizes system stability and response for different applications, and furthermore can reduce external components.

The feedback compensation design is based on the system operation mode and component parameters. An off-line flyback converter mostly uses a Type-II compensator to compensate for the feedback loop. It has a zero frequency pole, a low frequency zero and a high frequency pole. The feedback compensation design is to make the low frequency zero point of compensator to compensate the low frequency pole point of system and make the high frequency pole point to compensate the ESR zero point of output capacitor, by doing this the system can possess a better phase margin. In addition to phase margin, a proper middle gain of compensator is chosen to get the better transient response, and improve the system stability.

The RT7208EB provides a simple and flexible design for feedback compensation. The R_Z, C_Z and the middle gain of the compensator can be programmed according to different output conditions. With this feature, one can easily achieve a stable system by using this flexible design for compensation.

Power-Up Sequence

Figure 7 shows the timing diagram for the power-up sequence. When start-up, the default output voltage is set at 5V. Once a Type-C cable is attached, the UFP will deliver voltage and current settings to the RT7208EB for the MCU to decode and to program reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, the RT7208EB will enter power-saving mode, under which the RT7208EB operates at ultra-low operating current and thus the total input power can be saved. If the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7208EB will exit power-saving mode.

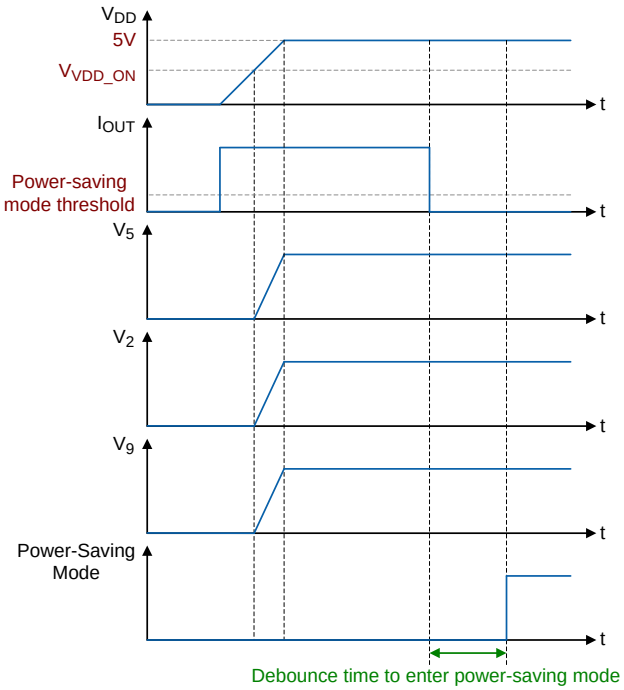


Figure 7. The Bias Voltages Sequence during Start-Up

Internal Biases and Charge Pump

The RT7208EB provides three regulated bias voltages, V_5, V_2, and V_9. The V_5 bias voltage is the output of a linear regulator powered by VDD, and supplies the internal analog circuit and the charge pump driver. The V_2 bias voltage is the output of a linear regulator powered by V_5, and supplies the MCU. As shown in Figure 8, the RT7208EB also integrates a charge pump circuit to generate V_9 to supply for the SR driver when V_{DD} is at lower levels, such as 3V to 5V. If the RT7208EB enters power-saving mode, the charge pump driver will be disabled.

The minimum source/sink capability of the charge pump driver is around 10mA at 170kHz of charge pump operating frequency f_{CP}. Bypass capacitors on the V5, V2 and V9 pins are required to minimize output ripples of the biases.

$$V_9 = V_5 \times 2 - V_{F\_DCP1} - V_{F\_DCP2} - I_{V9} \times R_{OUT\_CP}$$

When output voltage is set at lower levels (<5V), V_5 will be lower, following VDD by a voltage drop of a dropout voltage of the LDO. For higher V_9, a lower forward voltage for the Schottky diodes, D_{CP1} and D_{CP2}, is required.

When V_9 is higher, the internal circuit power consumption in V9 pin will also increase. In order to reduce the loss, the RT7208EB adds the power saving mode for the charge pump circuit. When V_9 is less than V_{V9_CP}, the charge pump circuit will be activated. So that the average voltage of V9 and charge pump switching loss can be reduced while maintaining enough voltage to drive the SR MOSFET.

If V_9 is powered from V_5 using a charge pump and V_{DD} is high (>8V), the linear regulator on the V5 pin will consume more power and affect the efficiency. Therefore, the RT7208EB builds an 8V linear regulator on the V9 pin to improve the efficiency. Once VDD is higher than firmware setting threshold, the charge pump can be disabled by firmware and VDD supplies power to V9 through the internal linear regulator.

The RT7208EB provides V5 short-circuit protection against the condition that the V5, V2, or VCP pin is shorted to GND, and also provides under-voltage protection for V9. If the V9 voltage is below V_{V9_SRON} (typical 4.5V), the SR driver will be turned off by firmware, that is, VG will be inactivated.

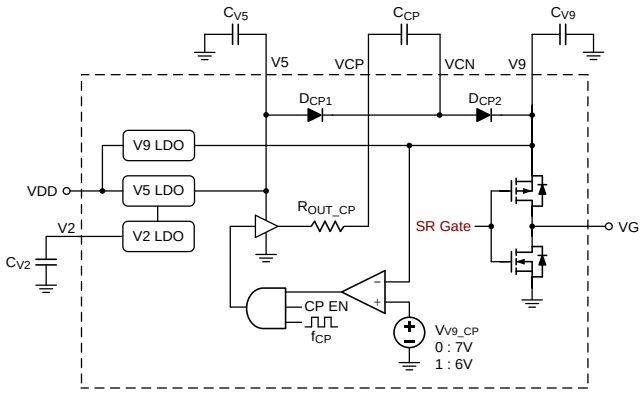
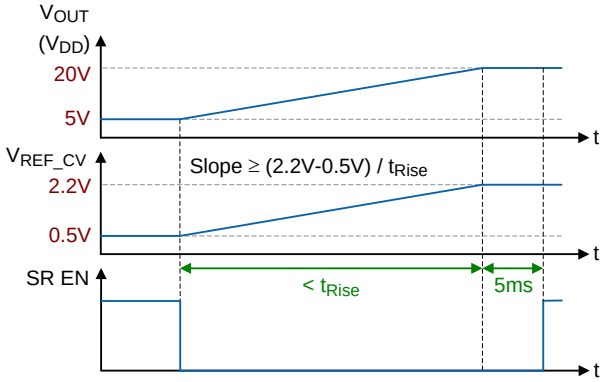


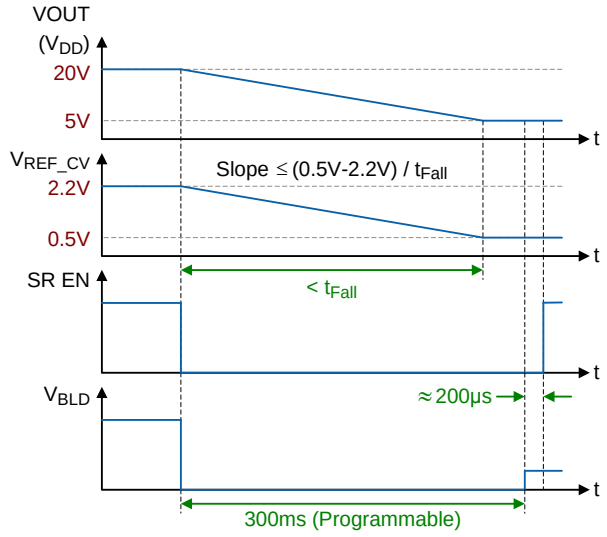
Figure 8. Internal Biases and Charge Pump Circuit

Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and the fall time of output voltages should be less than the defined specifications t_{Rise} and t_{Fall} respectively, as shown in Figure 9.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 9. Output Voltage Transient Waveforms

During the time of V_{OUT} falling, as shown in Figure 10, the BLD driver will be turned on as a dummy load to provide an extra discharging path for the output capacitor so that V_{OUT} can be settled in a shorter duration. The resistance of R_{DUMMY} can be calculated as below :

$C_{OUT} \times (R_{DUMMY} + R_{L\_BLD}) \times 2 < t_{Fall}$

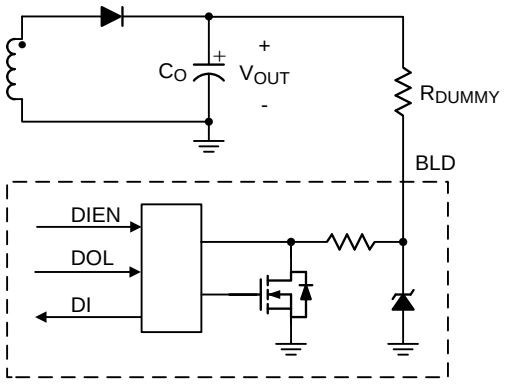


Figure 10. Application Circuit of an Active Dummy Load

During the time of V_{OUT} rising or falling, the SR driver will be turned off. After a firmware programmable delay time 300ms, the RT7208EB will sense the load condition and may reactivate the SR driver.

ZVS Control

In order to obtain zero-voltage switching on main switch of primary side, the power system needs to be operated in DCM mode. SYNC pin will detect the received pulse width (SYNC RX), larger than 120ns, from the primary side and then turn on SR MOSFET additionally according to the programmed t_{PULSE_ZVS}. As shown in Figure 11, the extra t_{PULSE_ZVS} of SR MOSFET turns on before main switch turn-on, meanwhile recycle and return the energy stored on the magnetizing inductance (Lm) of the transformer from the secondary side to the primary side. When the extra t_{PULSE_ZVS} of SR MOSFET turns off, the current of magnetizing inductance needs continuously flow and it will recycle and transfer the energy stored on the parasitic capacitor C_{DS} of main switch to the input side.

To achieve zero-voltage switching on main switch for optimizing the efficiency, the energy returned from SR MOSFET of the secondary side must be larger than the storage energy C_{DS} of the primary side. The t_{PULSE_ZVS} of SR MOSFET can be adjusted by the following equation :

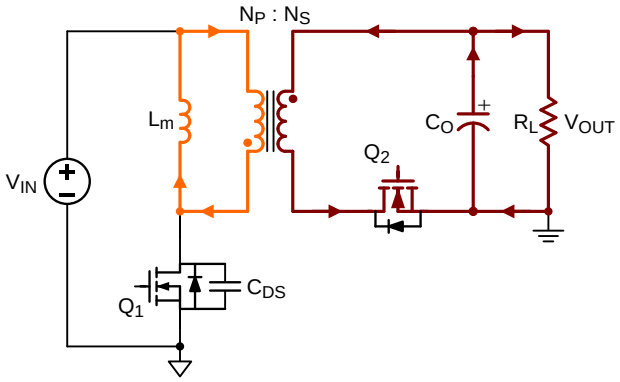
$$\frac{1}{2}\times Lm\times\left(\frac{\frac{N_P\times V_O}{N_S}}{Lm}\times t_{PULSE\_ZVS}\right)^2 \geq \frac{1}{2}\times C_{DS}\times\left(V_{IN}+\frac{N_P}{N_S}\times V_O\right)^2$$

$$t_{PULSE\_ZVS} \geq \sqrt{Lm\times C_{DS}}\times\left(\frac{N_S}{N_P}\times\frac{V_{IN}}{V_O}+1\right)$$

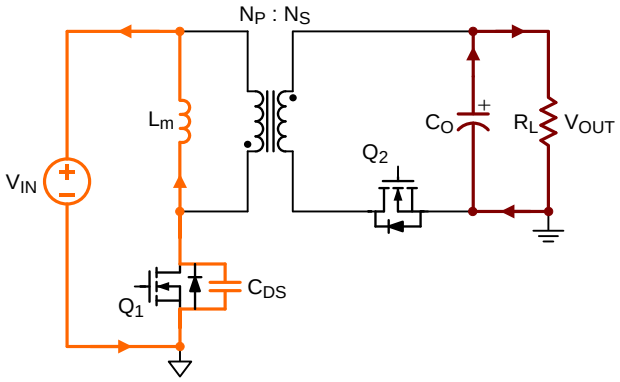
N_P : Turns of primary-side winding.

N_S : Turns of secondary-side winding.

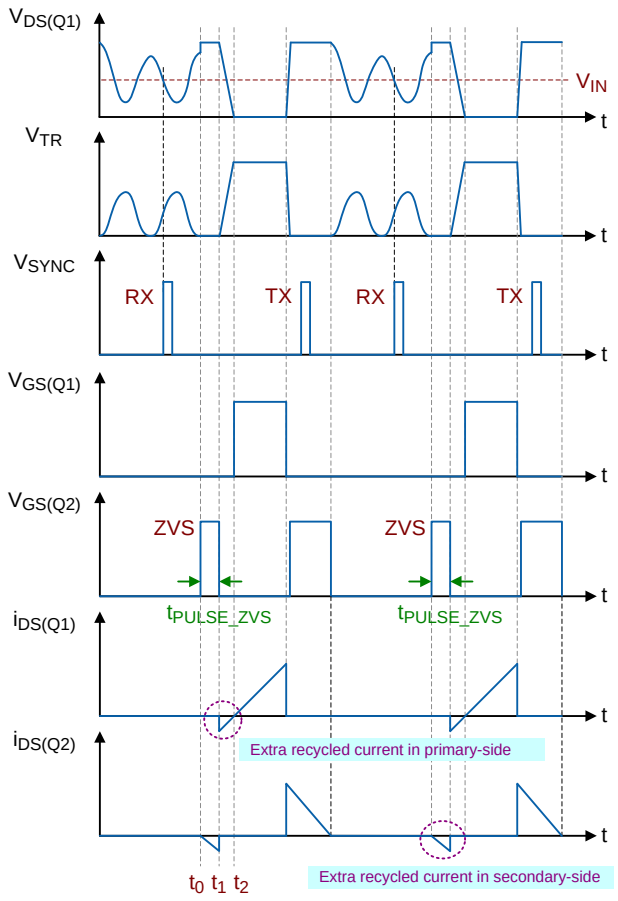
C_{DS} : The parasitic capacitance C_{DS} of main switch.



(a) t_0 to t_1 Equivalent Circuit



(b) t_1 to t_2 Equivalent Circuit



(c) Waveform

Figure 11. ZVS Control

Temperature Sensing and Thermal Protection

The RT7208EB provides the RT1 and RT2 pin for over-temperature protection or thermal monitoring. As shown in Figure 2, the RT1 and RT2 pin sources a constant bias current for a remote thermal sensor of an NTC thermistor, connected from the RT pin to GND, for temperature sensing. If the RT voltage is below a programmable threshold voltage and the condition sustains for a programmable deglitch time, over-temperature protection will be triggered.

The bias current through the RT1 and RT2 pin can be programmed as 100μA, 20μA, or 4μA by individually setting the internal register. With the appropriate bias current setting, linearity of temperature sensing over the temperature range of 25°C to 100°C can be improved. The RT7208EB can deliver the sensed RT voltage data back to the UFP via the protocol (Vendor Defined Message), if necessary. Figure 12 shows the RT voltages vary with temperature at three different bias currents with an NTC thermistor TTC104 as an example.

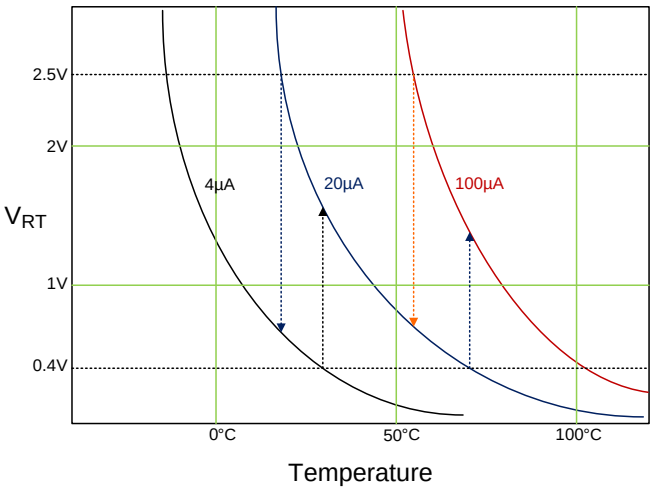


Figure 12. The RT Voltages vs. Temperature at Three Bias Currents

Linear Cable Compensation

The RT7208EB is based on output current value to adjust the feedback control voltage (V_{FB}) to implement a linear cable compensation, as shown in Figure 13. The transconductance amplifier gain (gm_{COMP}) can be set by the internal register.

$$V_{CABLE\_COMP} = I_{OUT} \times R_{CS} \times K_{CS} \times gm_{COMP} \times R_{FB1}$$

K_{CS} : Current sense gain

where

gm_{COMP} : Transconductance amplifier gain

R_{FB1} : V_{OUT} divider resistor

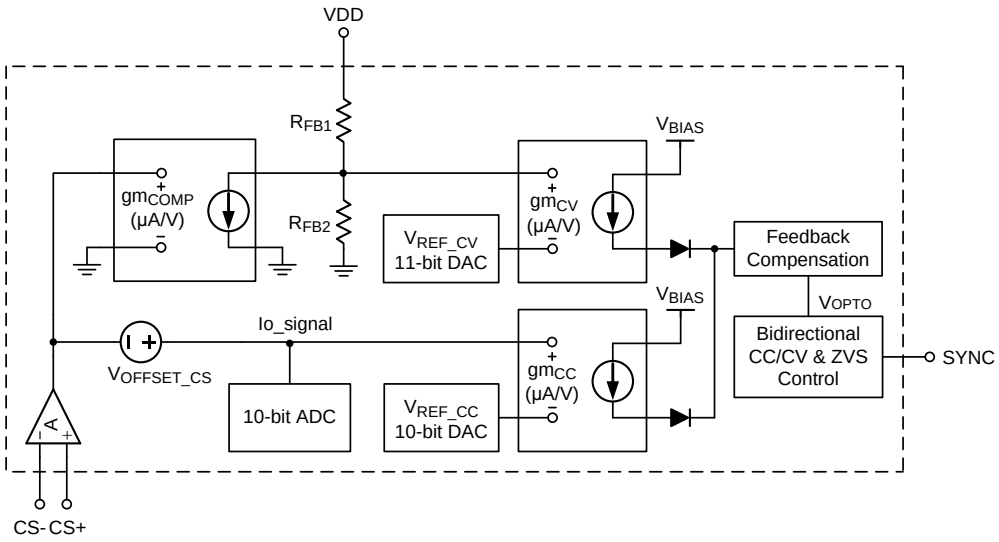


Figure 13. Linear Cable Compensation

Blocking N-MOSFET Control (USBP)

The RT7208EB provides a push-pull driver for controlling external blocking N-MOSFET as shown in the Figure 14. The push-pull driver not only can control N-MOSFET smooth turn-on to avoid VOUT drops in the capacitive load condition but also provide quickly turn-off in any fault condition.

Once the communication is set up with an UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector of the UFP is detected, the N-MOSFET will be turned-on. If VOUT over-voltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged by the VOUT over-voltage condition. When VOUT is shorted to GND, the N-MOSFET will be turned-off automatically and output power can be limited.

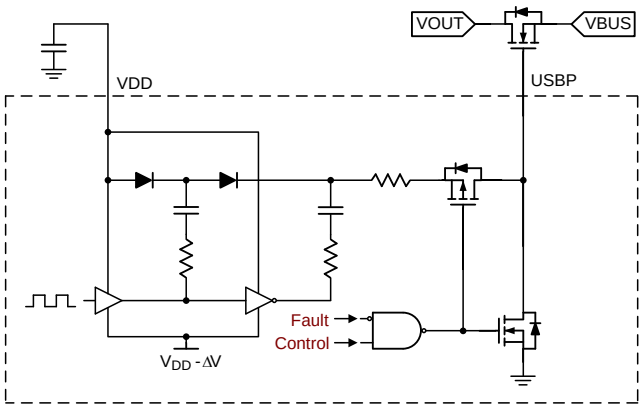


Figure 14. Blocking N-MOSFET Control

Output Over-Voltage Protection

As shown in the Figure 15 and Figure 16, the RT7208EB provides a fast turn-off blocking N-MOSFET as a backup VOUT over-voltage protection, in case the pulse transformer of the feedback loop is malfunction. If the internal voltage related to VDD is higher by the programmable threshold V_{VOUT_OVP}, the internal OPTO will be pulled low. The internal OPTO voltage will be latched low until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

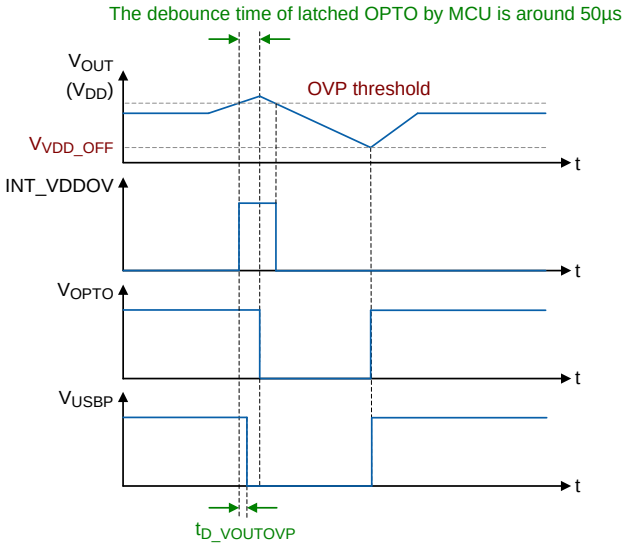


Figure 15. Timing Sequence of the OVP Function

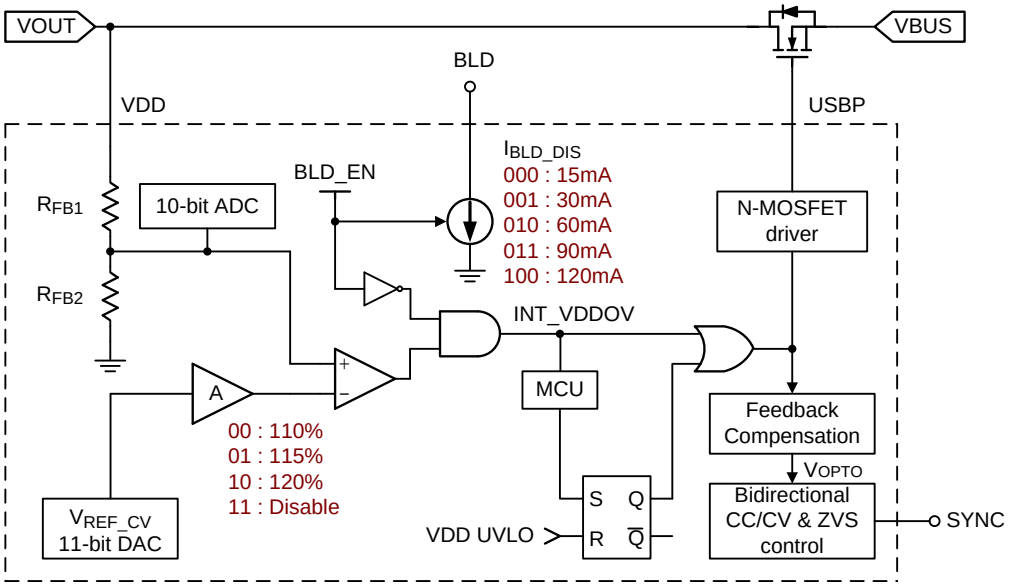


Figure 16. OVP Functional Diagram

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to – ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 4x5 package, the thermal resistance, θ_{JA}, is 27.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.4°C/W) = 3.64W for a WQFN-28L 4x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 17 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

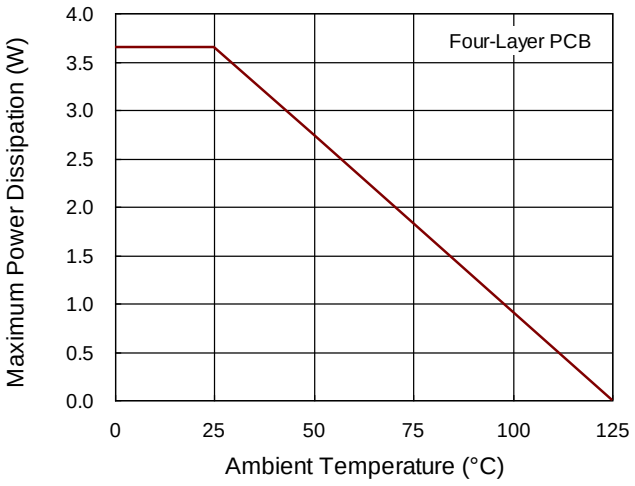
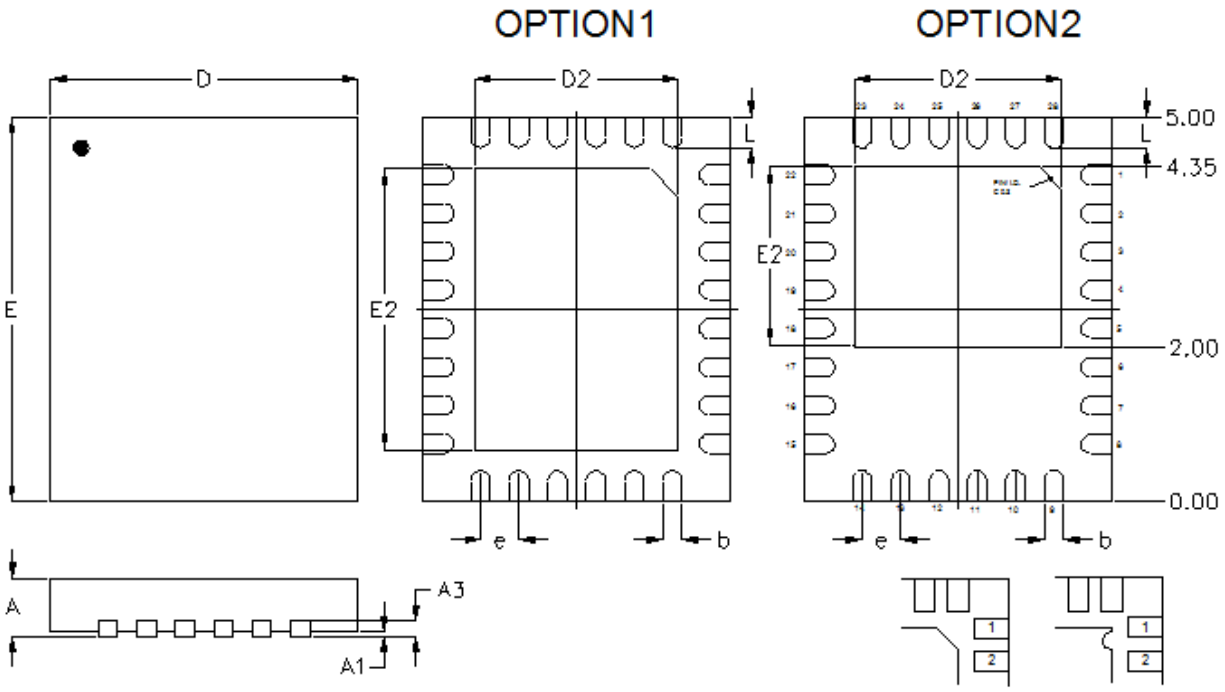


Figure 17. Derating Curve of Maximum Power Dissipation

Outline Dimension

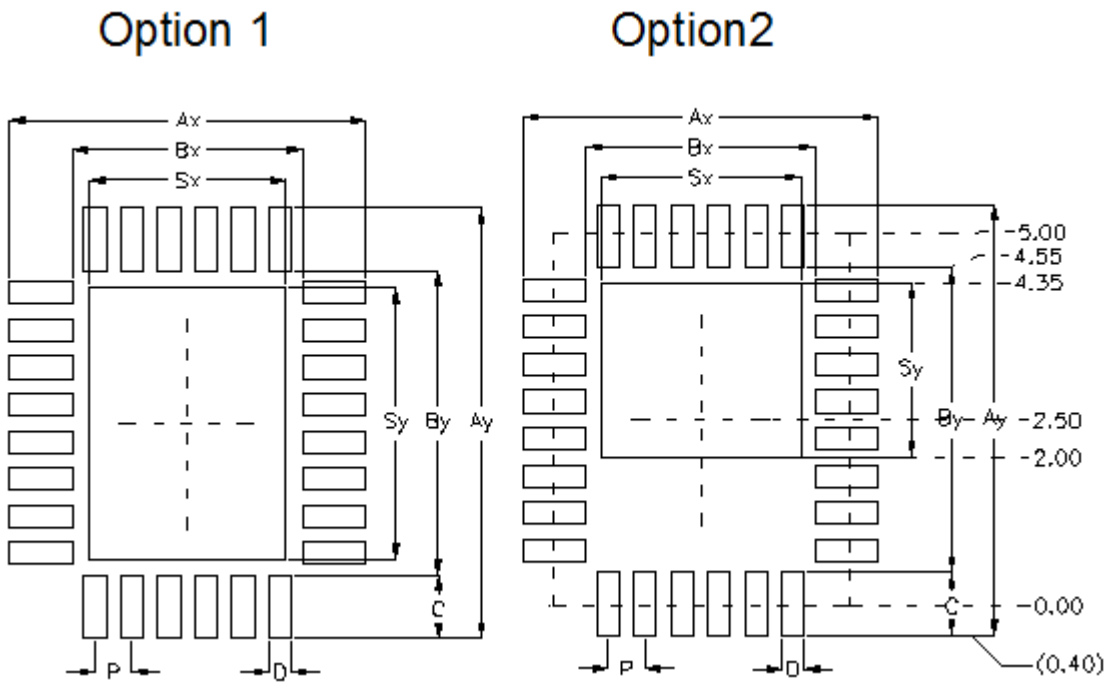


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.900	4.100	0.154	0.161
D2	Option1	2.600	2.700	0.102	0.106
	Option2	2.650	2.750	0.104	0.108
E		4.900	5.100	0.193	0.201
E2	Option1	3.600	3.700	0.142	0.146
	Option2	2.300	2.400	0.091	0.094
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 28L QFN 4x5 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4x5-28	Option1	28	0.50	4.80	5.80	3.10	4.10	0.85	0.30	2.65	3.65	±0.05
	Option2									2.70	2.35	

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