

# Low Quiescent Current USB Type-C Power Delivery Controller with Built-In Blocking N-MOSFET

## 1 General Description

The RT7216 is a low quiescent current USB Type-C Power Delivery (PD) controller designed for the secondary side of offline AC-DC power converters. Its high level of integration, including control regulators and a built-in blocking N-MOSFET, enables compact and energy-efficient designs. The embedded MCU and Bi-phase Mark Coding (BMC) transmitter manage PD protocol communication, while integrated DAC and ADC modules deliver precise voltage and current regulation. The RT7216 supports output voltages from 3.3V to 21V and output currents up to 5A. Comprehensive protection features, including Limited Power Source (LPS) and Over-Temperature Protection (OTP), ensure system safety and reliability. The recommended junction temperature range is  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and the ambient temperature range is  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .

## 2 Applications

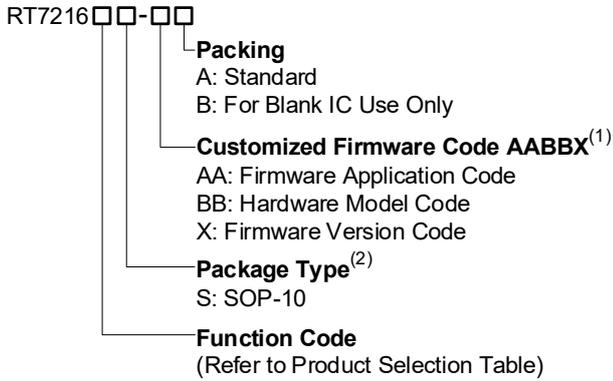
- USB Type-C PD Controller in Source Application for Chargers/Adapters of Smartphone, Tablet, Notebook, and Other Electronics
- USB Type-C PD Controller in Sink Application for IoT Devices of Power Over Ethernet, Smart Speaker, Projector, and Other Electronics

## 3 Features

- **Protocol Support**
  - USB PD3.2 PPS and SPR AVS
- **Operation**
  - Wide Voltage Range from 3.3V to 21V
  - $< 9\text{mA}$  Operating Current in Normal Mode
  - $< 0.5\text{mA}$  Operating Current in Sleep Mode
  - $< 0.35\text{mA}$  Operating Current in Green Mode
- **System Management**
  - ARM Cortex-M0 Microcontroller with 10.8MHz Oscillator and MTP-ROM of 16kB (Supports OTP via FT Trim)
  - 11-bit ADCs for Reading Information on Pins
  - 11-bit DACs for Constant-Voltage and 10-bit DACs Constant-Current Regulations
- **Power Management**
  - Linear Cable Compensation
  - VDD Pin Discharger for Output Capacitor
  - VBUS Pin Discharger for Vsafe0V
- **Port Management**
  - Built-In Blocking N-MOSFET
  - Built-in 8-bit DAC for Capacitive-Load Start-up
  - Built-in 100mW VCONN Power
  - Firmware Online-Update Supported
- **Protection**
  - VDD Adaptive Overvoltage Protection
  - VDD Adaptive Undervoltage Protection
  - VDD Drop for Short-Circuit Protection
  - Limited Power Source Protection
  - Programmable Overcurrent Protection
  - Programmable External and Internal Over-Temperature Protection

## 4 Ordering Information

### 4.1 Product Number Information



**Note 1.**

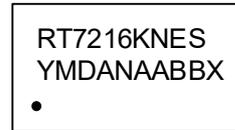
- Marked with <sup>(1)</sup> indicated: If the firmware code is empty, this field will be removed.
- Marked with <sup>(2)</sup> indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.

### 4.2 Production Selection Table

Function Code	KNE
Application Type	Source
Package	SOP-10
Constant Current	0
Differential Current Sensing	0
Max. Number of GPIOs	4

## 5 Marking Information

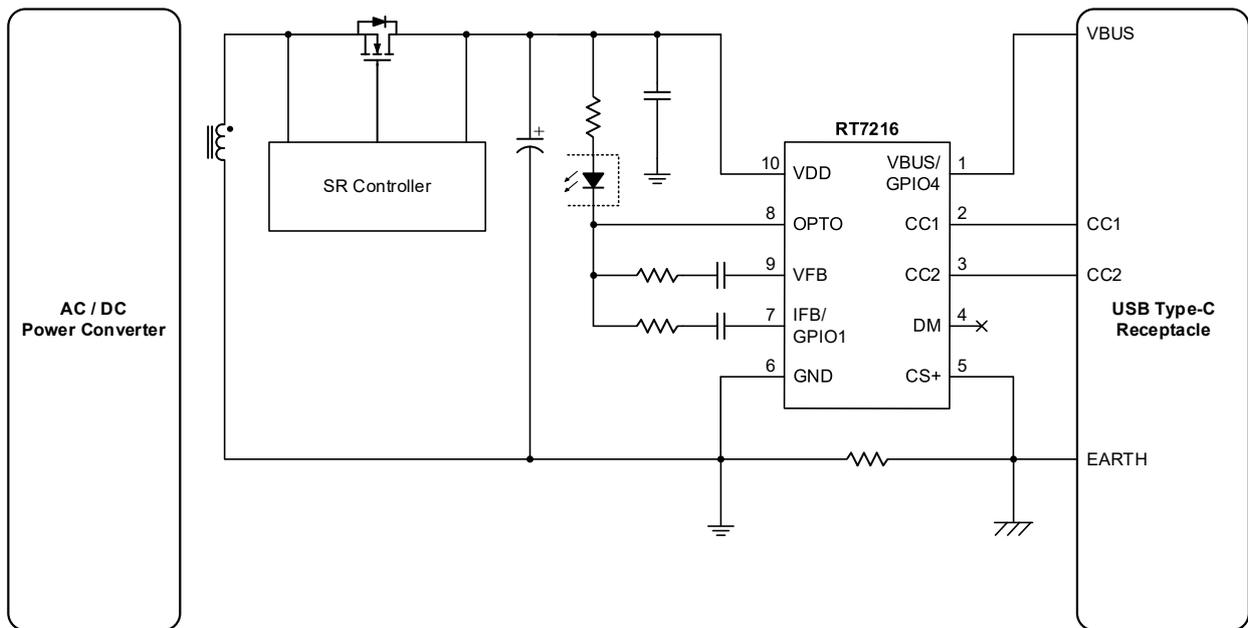
RT7216KNES-AABBX



RT7216KNES: Product Code  
YMDAN: Date Code  
AABBX: Customized Firmware Code

## 6 Simplified Application Circuit

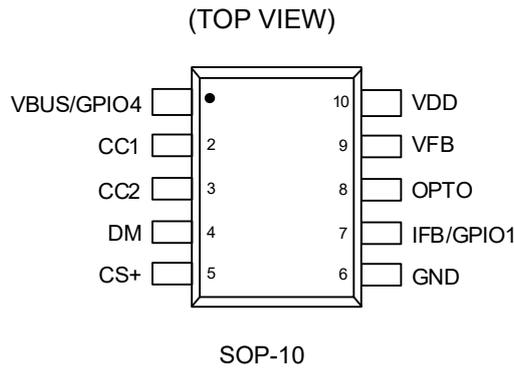
### 6.1 Simplified Circuit for Source Application



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7 Pin Configuration



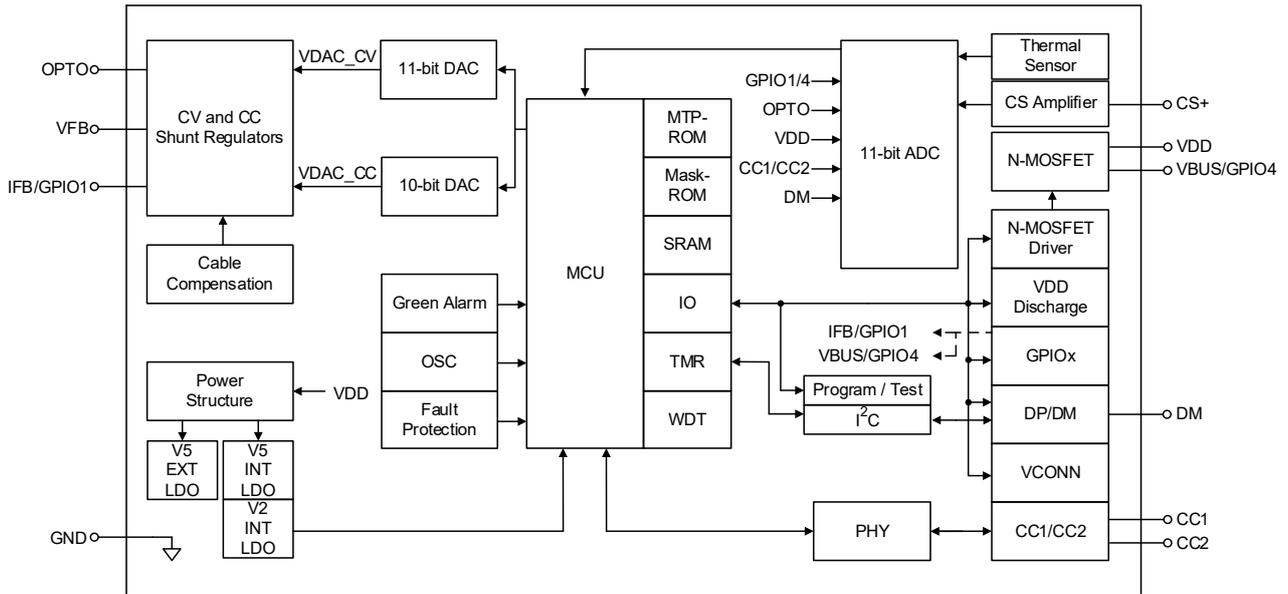
8 Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	VBUS/GPIO4	PWR A/D IO	The source terminal of the blocking N-MOSFET provides VBUS discharge functionality. Can be configured as sourcing current 20μA/100μA or sourcing voltage 4.5V with 3.1kΩ pull-up resistance, or as ADC input.
2	CC1	A/D IO	General purpose input and open-drain output. USB Type-C Configuration Channel 1: Built-in sourcing current for Source Advertisement, VCONN power, and BMC transceiver for USB PD. Can be configured as built-in sourcing current for rust detection.
3	CC2	A/D IO	General purpose input and open-drain output. USB Type-C Configuration Channel 2: Built-in sourcing current for Source Advertisement, VCONN power, and BMC transceiver for USB PD. Can be configured as built-in sourcing current for rust detection.
4	DM	A/D IO	General purpose input and open-drain output. Can be configured as sourcing current 20μA/100μA or sourcing voltage 4.5V with 3.1kΩ pull-up resistance, or as ADC input.
5	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
6	GND	GND	Ground.
7	IFB/GPIO1	A/D IO	General purpose input and open-drain output. Compensation for constant-current loop. Connect a compensation network to stabilize the control loop. Can be configured as sourcing current 20μA/100μA/1100μA or sourcing voltage 4.5V with 3.1kΩ pull-up resistance, or as ADC input.
8	OPTO	A/D IO	Current sink output for optocoupler connection. Can be configured as ADC input.
9	VFB	AI	Feedback input for constant-voltage loop
10	VDD	PWR	Supply input voltage

**8.1 IO Type Definition**

- PWR: Power Pin
- GND: Ground Pin
- A I: Analog Input Pin
- A/D IO: Analog/Digital Input/Output Pin

**9 Functional Block Diagram**



## 10 Absolute Maximum Ratings

(Note 2)

- VDD-----0.3V to 30V
- VBUS/GPIO4, CC1, CC2, DM, IFB/GPIO1, VFB, OPTO to GND-----0.3V to 28V
- CS+ to GND -----0.3V to 6.5V
- Power Dissipation, PD @ TA = 25°C  
 SOP-10-----0.72W
- Package Thermal Resistance (Note 3)  
 SOP-10,  $\theta_{JA}$ -----139.56°C/W  
 SOP-10,  $\theta_{JC}$  -----43.4°C/W
- Junction Temperature -----150°C
- Lead Temperature (Soldering, 10sec.)-----260°C
- Storage Temperature Range -----65°C to 150°C
- ESD Susceptibility (Note 4)  
 HBM (Human Body Model)-----2kV

**Note 2.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 3.**  $\theta_{JA}$  is simulated under natural convection (still air) at TA = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard.  $\theta_{JC}$  is simulated at the bottom of the package.

**Note 4.** Devices are ESD sensitive. Handling precautions are recommended.

## 11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD-----3.3V to 21V
- Supply Input Current, IDD (Based on TJ < 125°C) -----0A to 5A
- Junction Temperature Range-----40°C to 125°C
- Ambient Temperature Range -----40°C to 105°C

**Note 5.** The device is not guaranteed to function outside its operating conditions.

## 12 Electrical Characteristics

(TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>PMU Section</b>						
Oscillator Frequency for MCU	fOSC_MCU	VDD > 2.8V	10.26	10.80	11.34	MHz
<b>VDD Section</b>						
VDD Turn-On Threshold Voltage	VDD_ON		2.9	3.1	3.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Turn-Off Threshold Voltage	VDD_OFF		2.7	2.9	3.1	V
VDD Start-Up Current	I <sub>DD_STA</sub>	VDD = 2.5V	--	0.2	0.3	mA
VDD Normal-Mode Current	I <sub>DD_NOR</sub>	VDD = 3.3V to 21V Does not include I <sub>CC_SRC</sub> and GPIO bias current	--	7.6	9	mA
VDD Idle-Mode Current	I <sub>DD_IDLE</sub>	VDD = 3.3V to 21V Does not include I <sub>CC_SRC</sub> and GPIO bias current	--	0.35	0.5	mA
VDD Green-Mode Current	I <sub>DD_GREEN</sub>	VDD = 5V Does not include I <sub>CC_SRC</sub> and GPIO bias current	--	0.25	0.35	mA
VDD Sinking Current for Output Voltage Discharge	I <sub>VDD_DSCHG</sub>		21	30	39	mA
			42	60	78	
			63	90	117	
			84	120	156	
			105	150	195	
			126	180	234	
VDD Resistor Divider for Voltage Feedback	R <sub>VDD_FB</sub>	R <sub>VDD_FB</sub> = R <sub>FB1</sub> + R <sub>FB2</sub> R <sub>FB1</sub> = 378kΩ, R <sub>FB2</sub> = 42kΩ (Note 6)	294	420	546	kΩ
VDD Resistor Divider Scaling Factor for Voltage Feedback	K <sub>VDD_FB</sub>		9.9	10	10.1	--
VDD Resistor Divider for ADC and Protection	R <sub>VDD_ADC</sub>	(Note 6)	700	1000	1300	kΩ
VDD Resistor Divider Scaling Factor for ADC and Protection	K <sub>VDD_ADC</sub>		9.9	10	10.1	--
Standby Output Voltage by Initial Reference	V <sub>VDD_ST</sub>		0.485	0.5	0.515	V
VDD Threshold Voltage for Maximum Overvoltage Protection	V <sub>VDD_MOVP</sub>		23	24	25	V
VDD Maximum Overvoltage Protection Deglitch Time	t <sub>VDD_MOVP</sub>	(Note 6)	25	30	35	μs
VDD Threshold Voltage for Adaptive Overvoltage Protection	V <sub>VDD_OVP</sub>	110% (min) to 160% (max), adjustable in 2.5% steps	104.50	110.00	115.50	%
			152.00	160.00	168.00	
VDD Adaptive Overvoltage Protection Deglitch Time	t <sub>VDD_OVP</sub>	8.5μs (min) to 53.5μs (max), adjustable in 3μs steps (Note 6)	7.14	8.50	9.86	μs
			44.94	53.50	62.06	
VDD Threshold Voltage for Adaptive Undervoltage	V <sub>VDD_UVP</sub>	52.5% (min) to 90% (max), adjustable in 2.5% steps	85.50	90.00	94.50	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection			49.88	52.50	55.13	
VDD Adaptive Undervoltage Protection Deglitch Time	tvDD_UVP	8.5μs (min) to 53.5μs (max), adjustable in 3μs steps (Note 6)	7.14	8.50	9.86	μs
			44.94	53.50	62.06	
<b>DAC/ADC Section</b>						
Maximum DAC Output Voltage for Constant-Voltage Regulator	VDAC_CV_MAX	11-bit digital-to-analog converter	2.156	2.2	2.244	V
Minimum DAC Output Voltage for Constant-Voltage Regulator	VDAC_CV_MIN		--	0.152	--	V
Maximum DAC Output Voltage for Constant-Current Regulator	VDAC_CC_MAX	10-bit digital-to-analog converter	0.147	1.5	1.53	V
Minimum DAC Output Voltage for Constant-Current Regulator	VDAC_CC_MIN		--	0	--	V
Maximum ADC Sense Voltage	VADC_MAX	11-bit analog to digital converter	2.178	2.2	2.222	V
<b>Current Sense Amplifier Section</b>						
Current-Sense Amplifier Gain	Kcs		19.4	20	20.6	V/V
			29.2	30	30.8	
Current-Sense Amplifier Output Offset Voltage	VCS_OFFSET		0.35	0.4	0.45	V
Cable-Compensation Resistance	RCABLE		20	25	30	mΩ
			40	50	60	
			63	75	85	
			90	100	110	
			105	125	145	
			130	150	170	
			180	200	220	
			230	250	270	
Current-Sense Amplifier Input Threshold Voltage for Current Wake-Up	VCS_WK	$V_{CS\_WK} = (V_{CS+} - V_{CS-}) \times K_{cs} + V_{CS\_OFFSET}$	0.51	0.55	0.59	V
			0.7117	0.75	0.7883	
			0.7508	0.7875	0.8242	
			0.7775	0.8125	0.8475	
			0.8042	0.8375	0.8708	
			0.8683	0.9	0.9317	
			0.8825	0.9125	0.9425	
			0.9217	0.95	0.9783	
			0.9483	0.975	1.0017	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
			0.975	1	1.025	
			1.0142	1.0375	1.0608	
			1.0533	1.075	1.0967	
			1.08	1.1	1.12	
			1.1317	1.15	1.1683	
			1.1833	1.2	1.2167	
			1.235	1.25	1.265	
<b>OPTO Section</b>						
OPTO Pull-Up Resistance	ROPTO_PU	Pulled up to VDD	35.7	51	66.3	kΩ
OPTO Pull-Down Resistance	ROPTO_PD	Pulled down to GND	42	60	78	kΩ
OPTO Sinking Current	LOPTO_SINK		18.75	25	31.25	μA
OPTO Output-Low Resistance	ROPTO_OL	Shorted to GND	--	25	200	Ω
<b>CC1/CC2 Section</b>						
CC1/CC2 Sourcing Current	ICC_SRC	VDD > 3V (For precise bias current application)	18	20	22	μA
			72	80	88	
			169	180	191	
			304	330	356	
CC1/CC2 Sourcing Current Clamping Voltage	VCC_CLP		4	4.5	5	V
			2.9	3.25	3.6	
CC1/CC2 Input-High Threshold Voltage	VCC_IH		2.5	2.6	2.7	V
			1.5	1.6	1.7	
			1.9	2	2.1	
			0.9	1	1.1	
CC1/CC2 Threshold Voltage for Overvoltage Protection	VCC_OVP		5.75	6	6.25	V
CC1/CC2 Overvoltage Protection Deglitch Time	tCC_OVP	(Note 6)	0.09	0.1	0.11	ms
<b>VCONN Section</b>						
VCONN Voltage	VCONN	VDD = 5V, ICONN = 0mA	4.6	4.8	5	V
		VDD = 5V, ICONN = 33mA	3.8	--	--	
VCONN Short-Circuit Current	ICONN_SC	Short to 2V	45	70	95	mA
<b>PD PHY Section</b>						
BMC Transmitter Output-High Voltage	VOH_BMC		1.05	1.125	1.2	V
BMC Transmitter Output-Low Voltage	VOL_BMC		0	0.0375	0.075	V
BMC Transmitter Output On-Resistance	RON_BMC		15	35	55	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BMC Transmitter Output Voltage Rise Time	t <sub>R_BMC</sub>		300	--	700	ns
BMC Transmitter Output Voltage Fall Time	t <sub>F_BMC</sub>		300	--	700	ns
<b>DM Section</b>						
DM Sourcing Current	I <sub>DM_SRC</sub>	V <sub>DD</sub> > 3V (For precise bias current application)	18	20	22	μA
			95	100	105	
DM Sourcing Current Clamping Voltage	V <sub>DM_CLP</sub>	V <sub>DD</sub> = 5V, I <sub>DM_BIAS</sub> = 95μA	3.6	4	5	V
		V <sub>DD</sub> = 5V, I <sub>DM_BIAS</sub> = 0μA	--	--	5	
DM Sourcing Voltage	V <sub>DM_SRC</sub>	V <sub>DD</sub> = 5V, I <sub>LOAD</sub> = 1mA	1.2	2.1	3	V
		V <sub>DD</sub> = 5V, I <sub>LOAD</sub> = 10μA	4	4.5	5	
DM Pull-Up Resistance	R <sub>DM_PU</sub>		1.65	3.1	4.65	kΩ
DM Pull-Down Resistance	R <sub>DM_PD</sub>		16	20	24	kΩ
DM Output-Low Voltage	V <sub>DM_OL</sub>		--	--	0.2	V
DM Input-High Threshold Voltage	V <sub>DM_IH</sub>		0.9	1	1.1	V
			1.9	2	2.1	
DM Input-Low Threshold Voltage	V <sub>DM_IL</sub>		0.86	0.955	1.05	V
			1.86	1.96	2.06	
DM Input Comparator Debounce Time	t <sub>DPDM_I</sub>	(Note 6)	0.95	1	1.05	μs
			142.5	150	157.5	
			475	500	525	
			950	1000	1050	
DM Threshold Voltage for Overvoltage Protection	V <sub>DM_OVP</sub>		5.75	6	6.25	V
DM Overvoltage Protection Deglitch Time	t <sub>DM_OVP</sub>	(Note 6)	0.09	0.1	0.11	ms
<b>GPIO Section</b>						
GPIO Sourcing Current	I <sub>GPIO_BIAS</sub>	V <sub>DD</sub> > 3V (For high bias current application)	18	20	22	μA
			95	100	105	
GPIO Sourcing Current Clamping Voltage	V <sub>GPIO_CLP</sub>	V <sub>DD</sub> = 5V, I <sub>GPIO1_BIAS</sub> = 95μA	3.6	4	5	V
		V <sub>DD</sub> = 5V, I <sub>GPIO1_BIAS</sub> = 0μA	--	--	5	
GPIO Sourcing Voltage	V <sub>GPIO_SRC</sub>	V <sub>DD</sub> = 5V, I <sub>LOAD</sub> = 1mA	1.2	2.1	3	V
		V <sub>DD</sub> = 5V, I <sub>LOAD</sub> = 10μA	4	4.5	5	
GPIO Pull-Up Resistance	R <sub>GPIO_PU</sub>		1.65	3.1	4.65	kΩ
GPIO Pull-Down Resistance	R <sub>GPIO_PD</sub>		30	65	100	Ω
GPIO Pull-Down Current Capability	I <sub>GPIO_PD</sub>	(Note 6)	30	--	--	mA

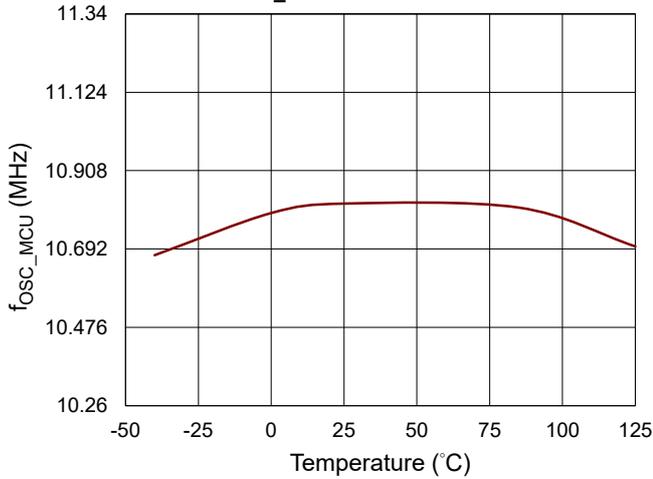
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GPIO Input-High Threshold Voltage	VGPI01_IH		0.9	1	1.1	V
			1.9	2	2.1	
GPIO Input-Low Threshold Voltage	VGPI01_IL		0.86	0.955	1.05	V
			1.86	1.96	2.06	
<b>GPIO1 Section</b>						
GPIO1 Sourcing Current	IGPI01_BIAS	VDD > 3V (For high bias current application)	18	20	22	μA
			95	100	105	
			850	1100	1350	
GPIO1 Sourcing Current Clamping Voltage	VGPI01_CLP	VDD = 5V, IGPI01_BIAS = 850μA	1.4	2.6	3.8	V
		VDD = 5V, IGPI01_BIAS = 0μA	--	--	5	
<b>VBUS/GPI04 Section</b>						
VDD Pin to VBUS Pin Turn-On Resistance	RON	VGS = 10V, IDS = 4A@25°C Measured between VDD and VBUS	6.4	9.3	12.2	mΩ
		VGS = 10V, IDS = 4A@125°C Measured between VDD and VBUS ( <a href="#">Note 6</a> )	7.1	--	14.5	
Drain-Source Current Threshold for Limit Power Source Protection	IDS_LPS	TA = -40°C to 125°C	1.25	2.5	4.29	A
		TA = 25°C	2	2.5	3	
<b>Accuracy Section</b>						
Thermal Sensor Error	ETS	25°C to 105°C ( <a href="#">Note 6</a> )	-7	--	7	°C

**Note 6.** Guaranteed by design.

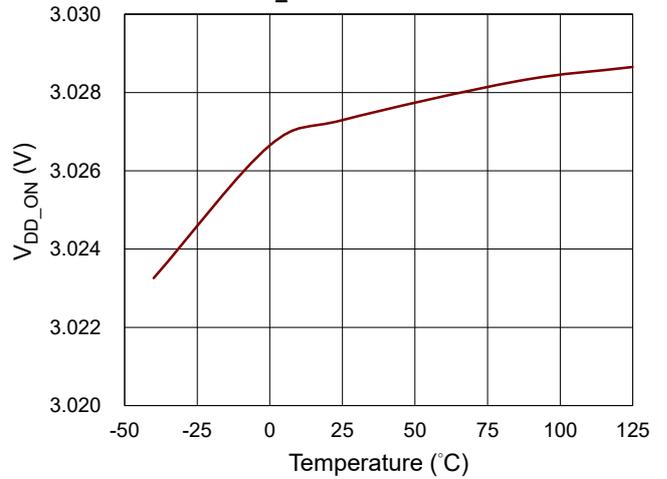


**14 Typical Operating Characteristics**

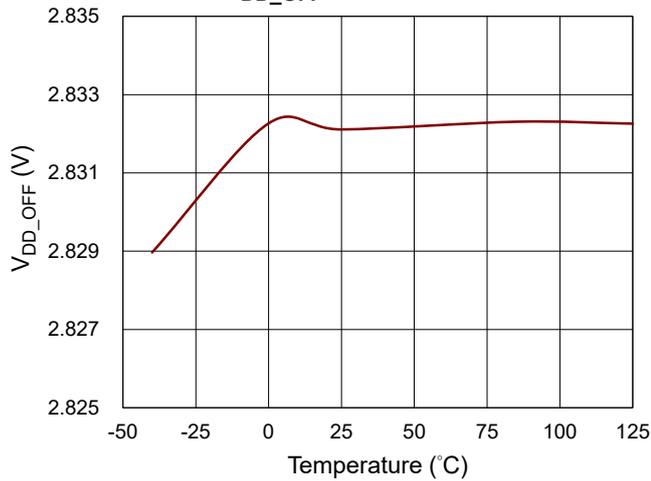
**f<sub>OSC\_MCU</sub> vs. Temperature**



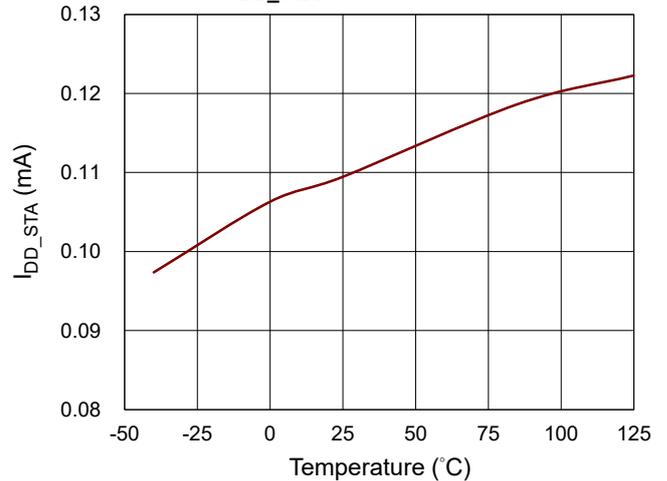
**V<sub>DD\_ON</sub> vs. Temperature**



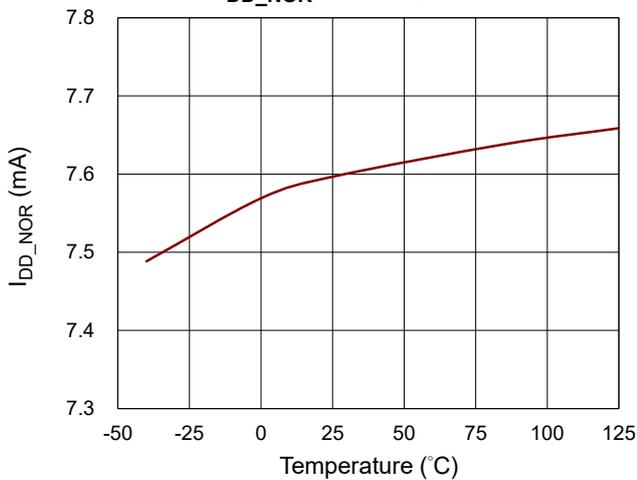
**V<sub>DD\_OFF</sub> vs. Temperature**



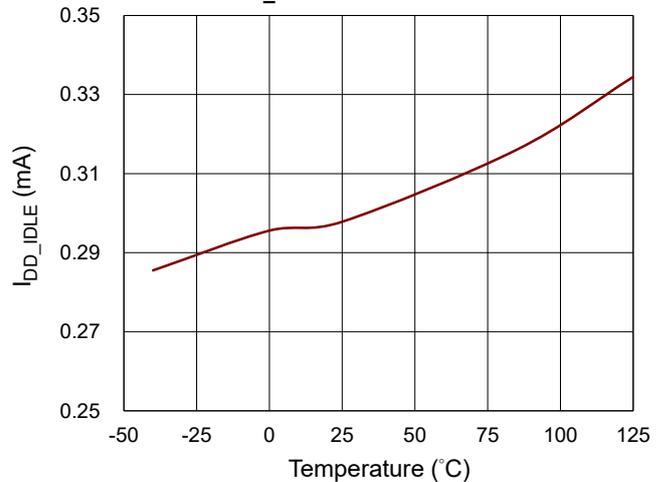
**I<sub>DD\_STA</sub> vs. Temperature**



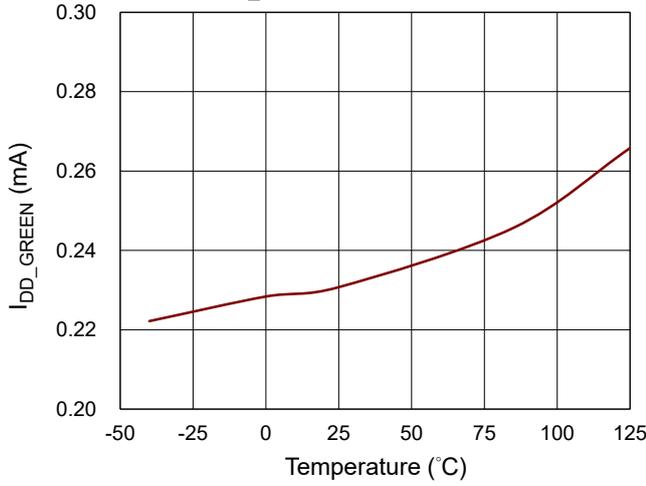
**I<sub>DD\_NOR</sub> vs. Temperature**



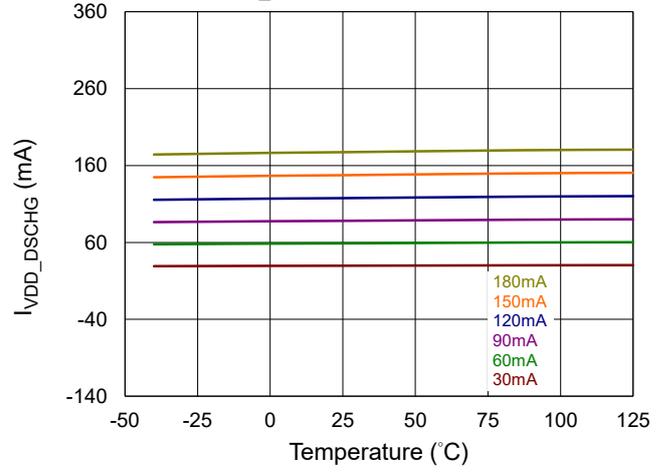
**I<sub>DD\_IDLE</sub> vs. Temperature**



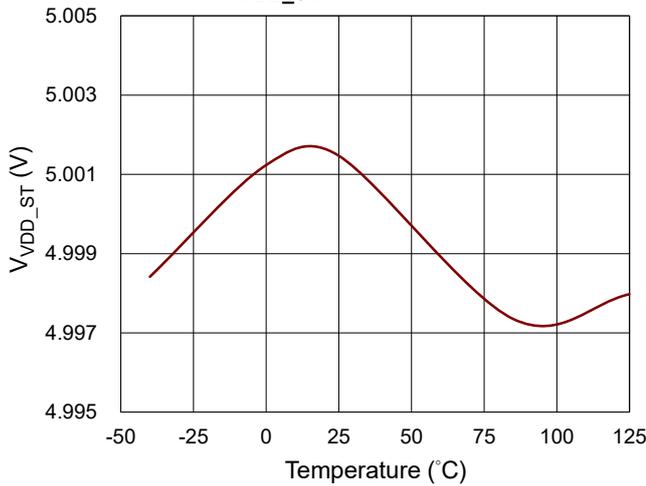
**I<sub>DD\_GREEN</sub> vs. Temperature**



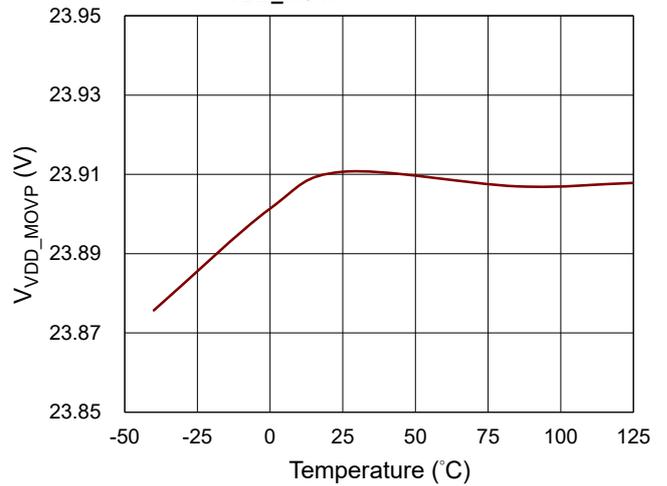
**I<sub>VDD\_DSCHG</sub> vs. Temperature**



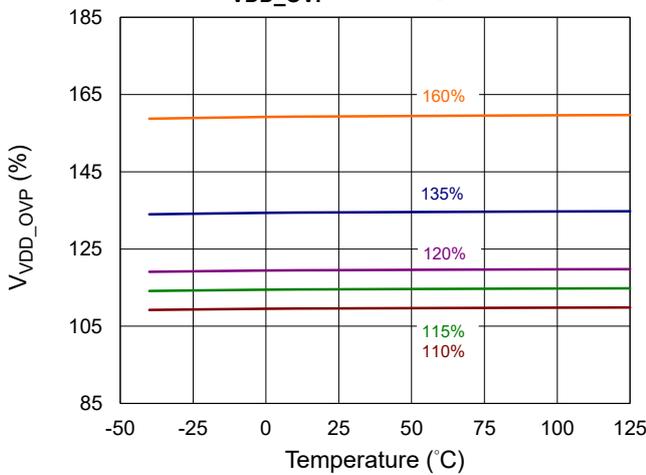
**V<sub>VDD\_ST</sub> vs. Temperature**



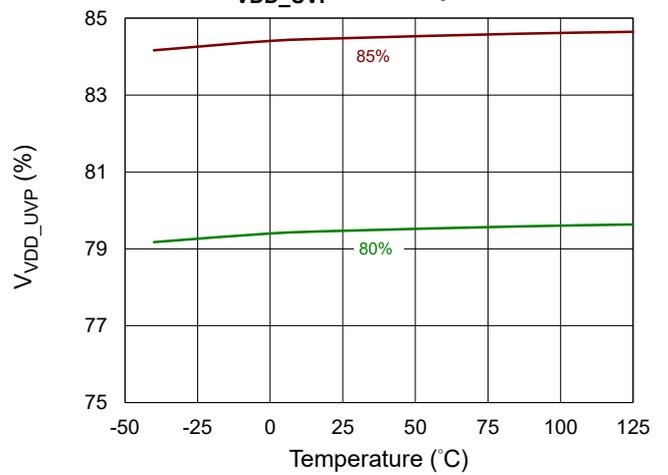
**V<sub>VDD\_MOVP</sub> vs. Temperature**

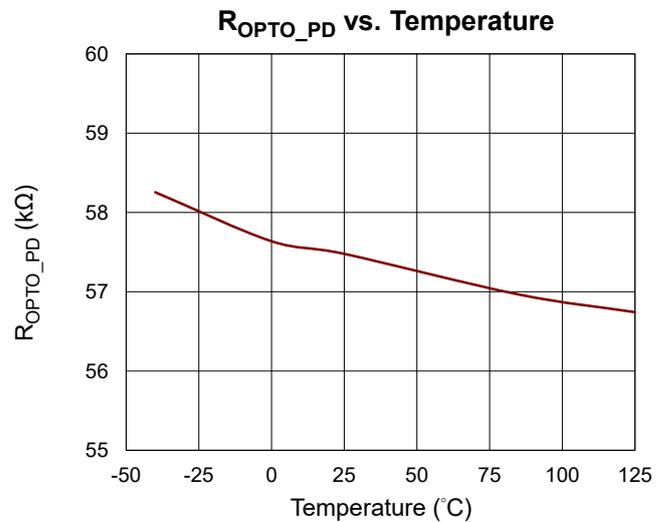
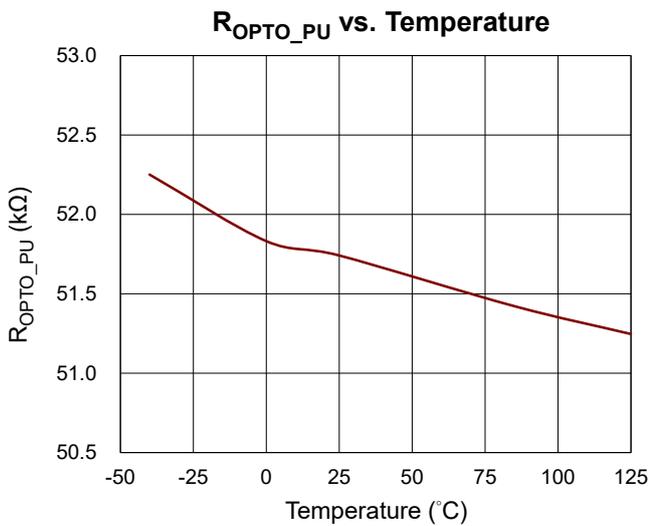
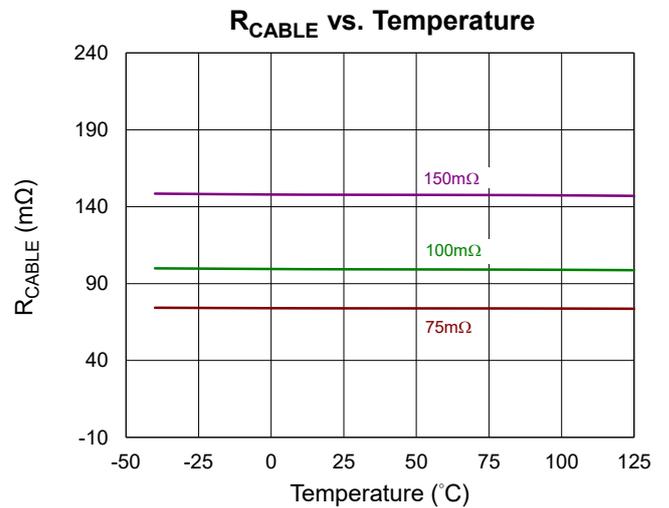
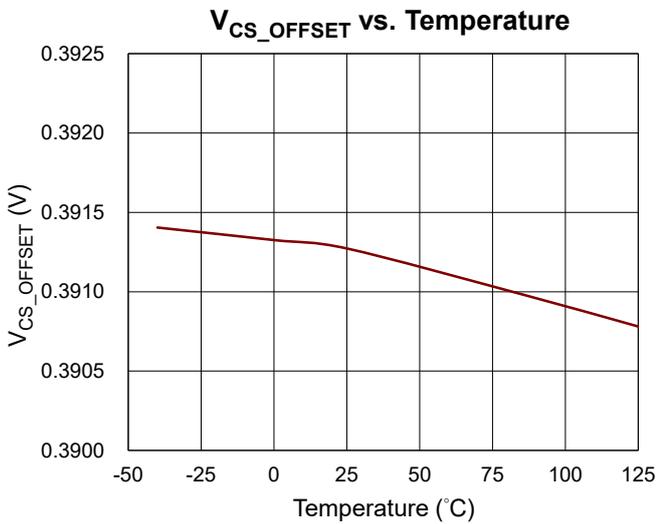
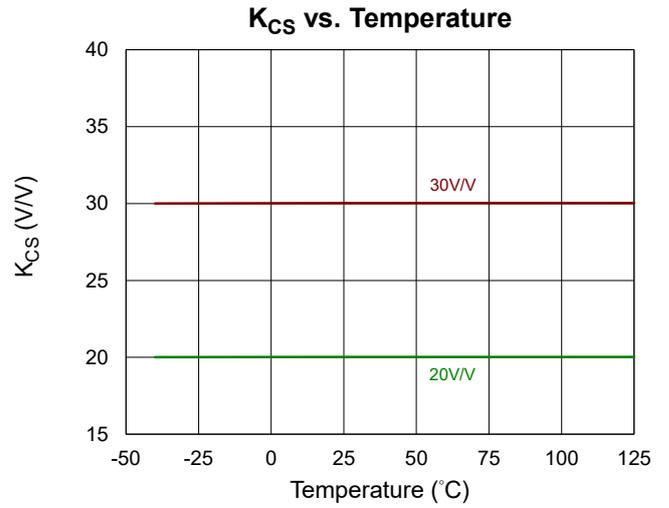
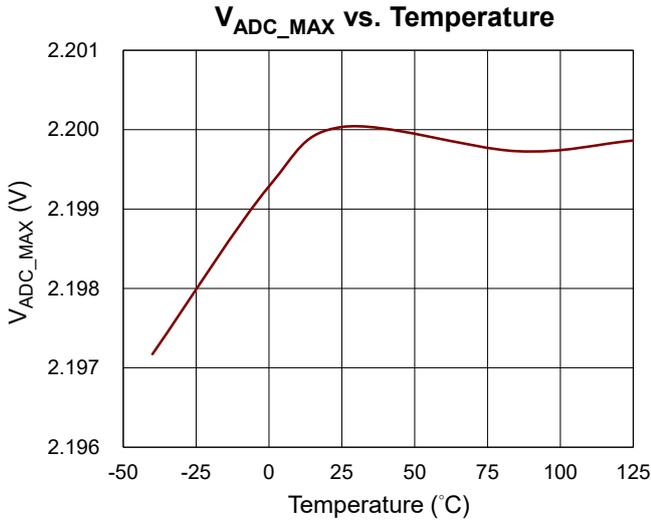


**V<sub>VDD\_OVP</sub> vs. Temperature**

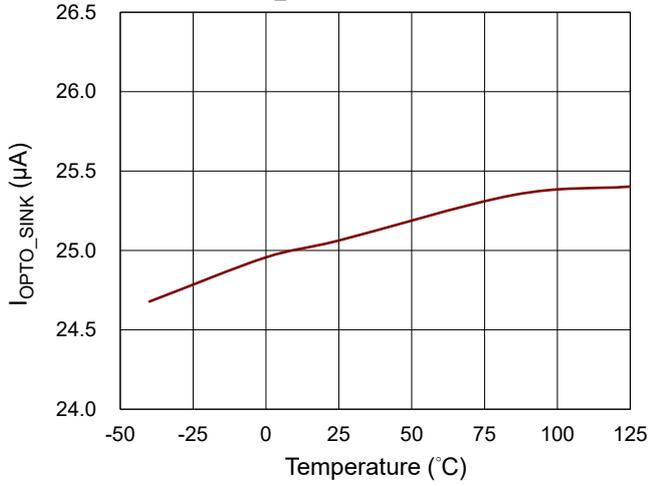


**V<sub>VDD\_UVP</sub> vs. Temperature**

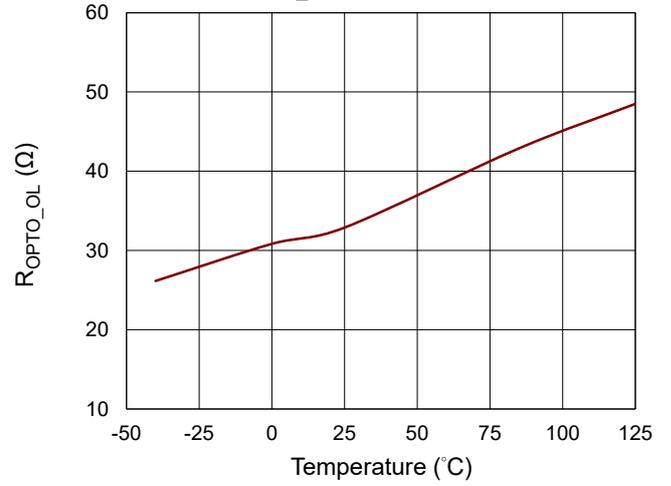




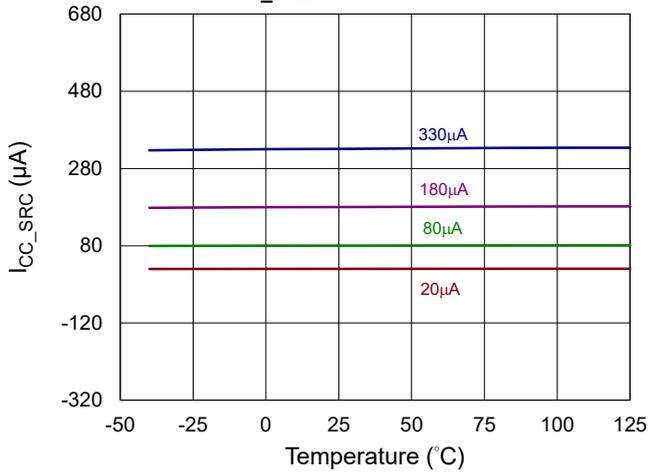
**$I_{OPTO\_SINK}$  vs. Temperature**



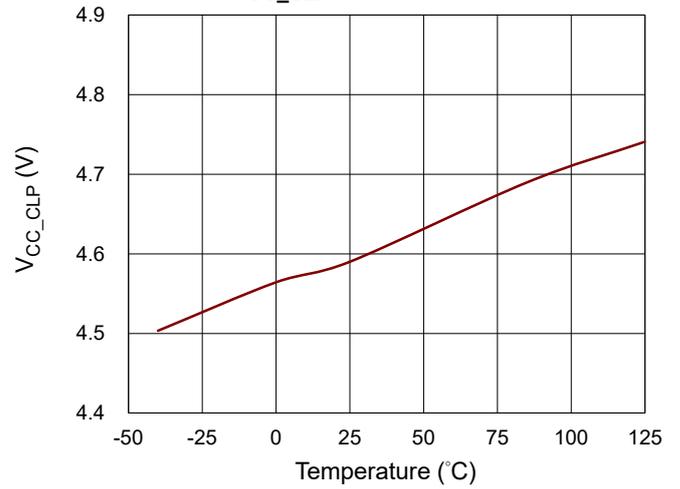
**$R_{OPTO\_OL}$  vs. Temperature**



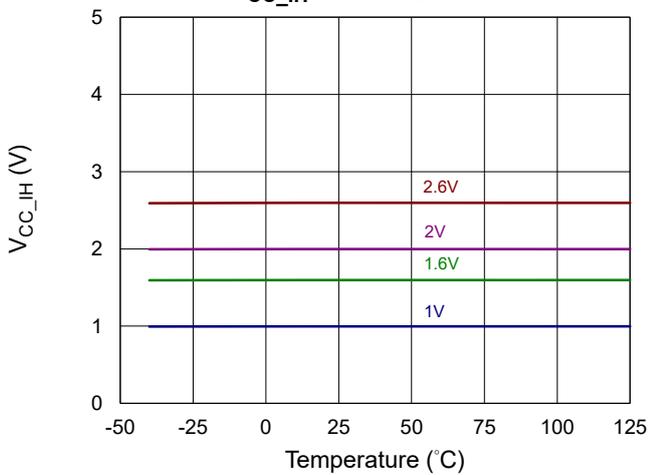
**$I_{CC\_SRC}$  vs. Temperature**



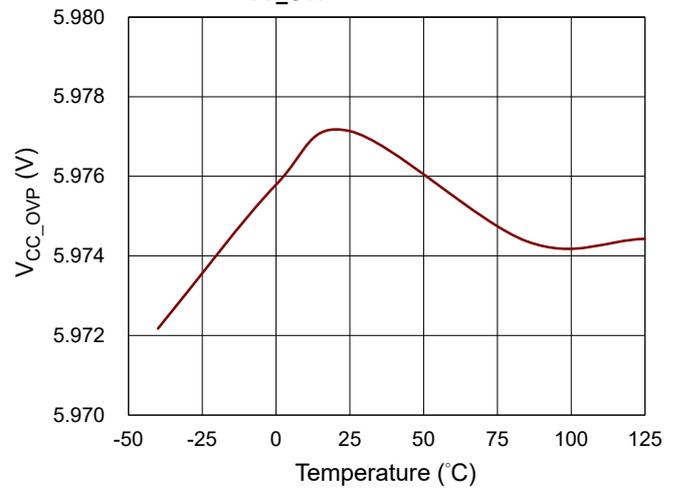
**$V_{CC\_CLP}$  vs. Temperature**

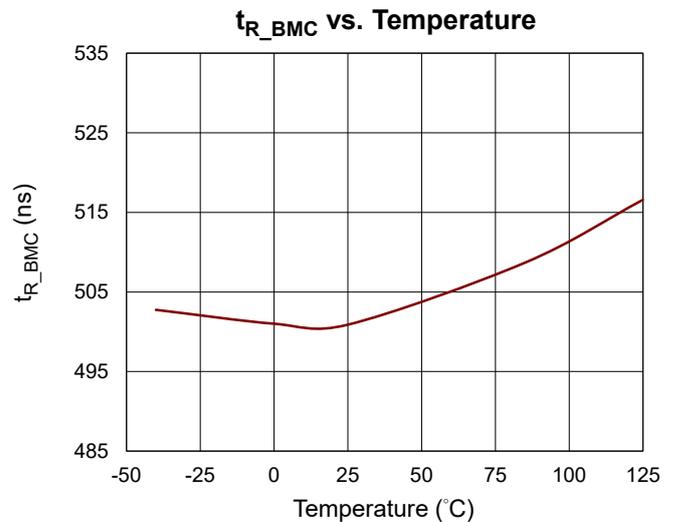
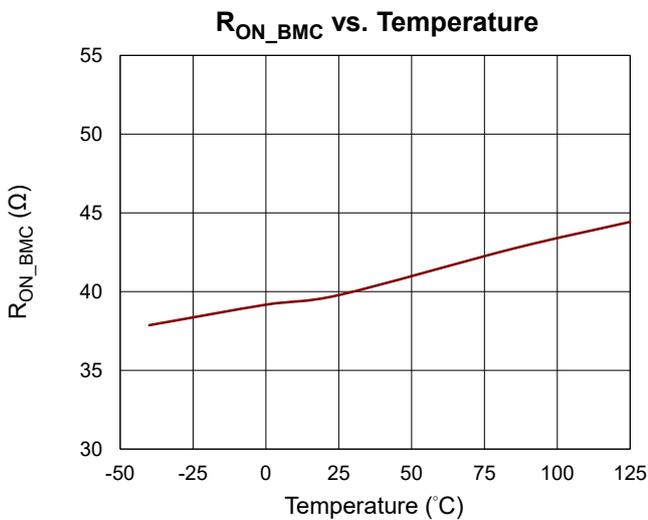
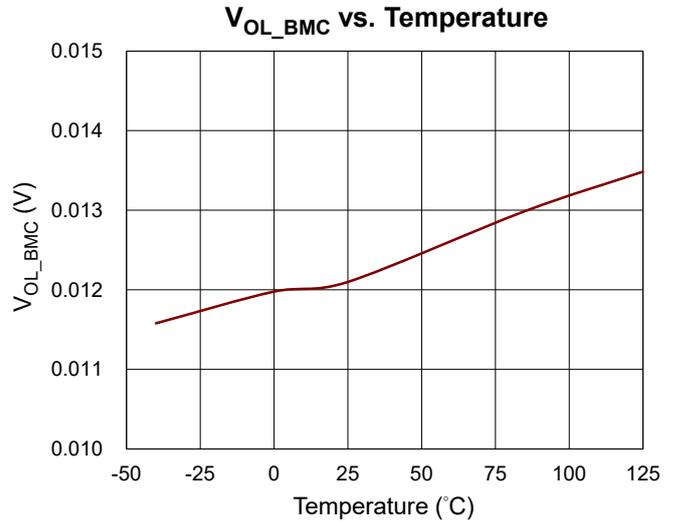
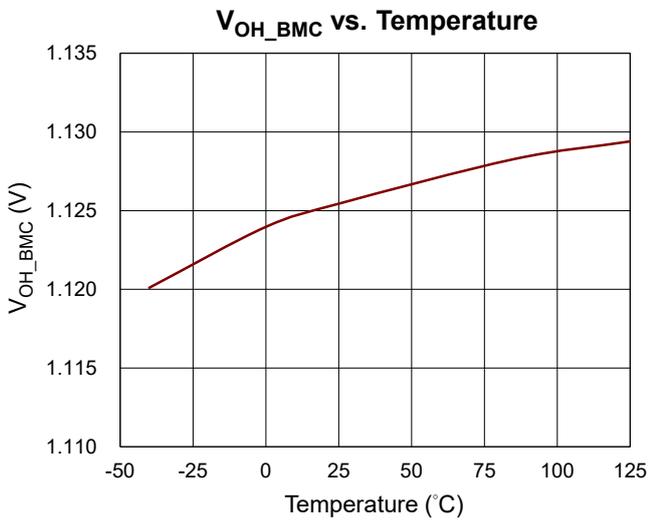
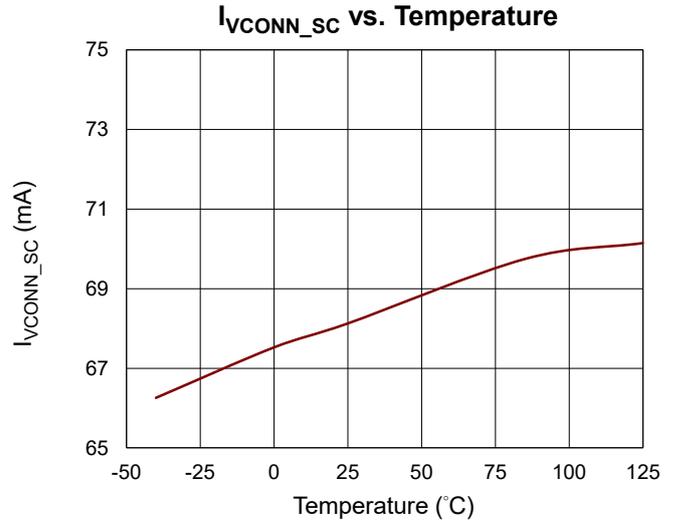
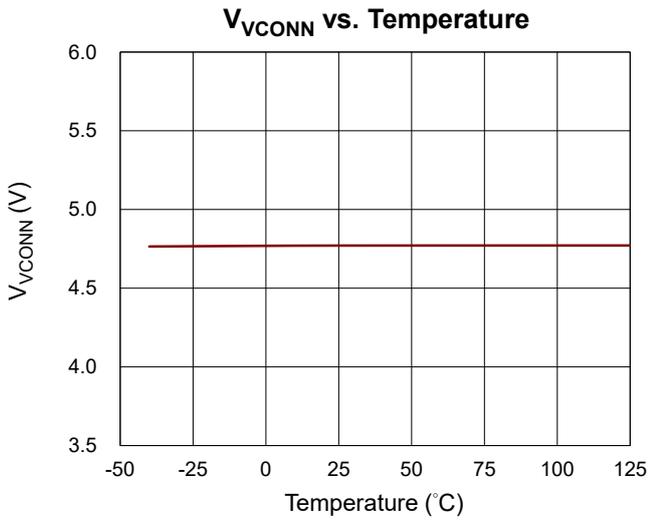


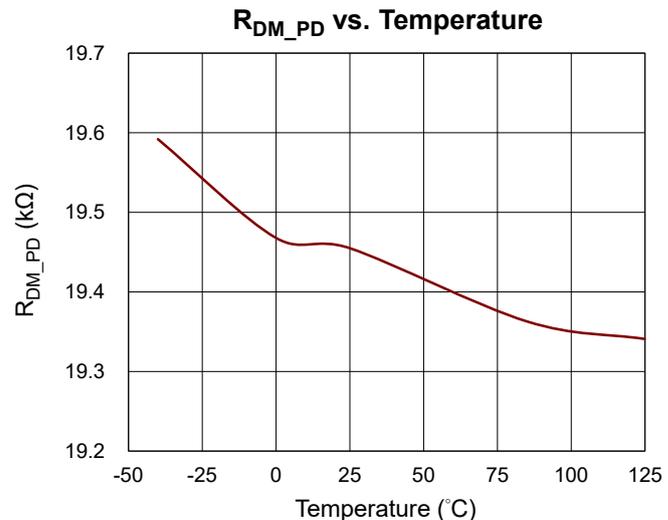
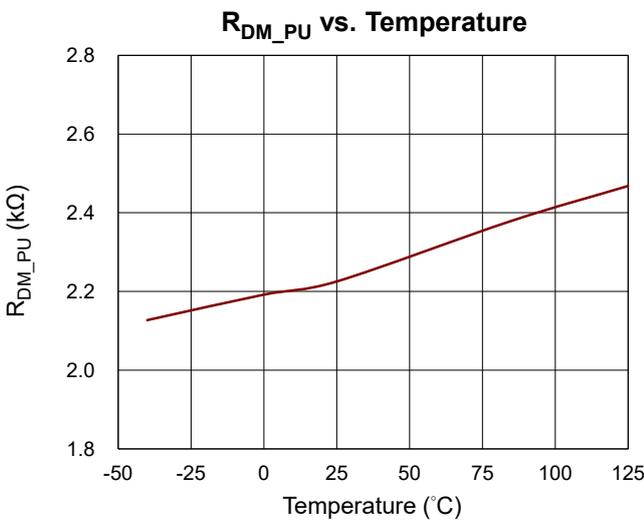
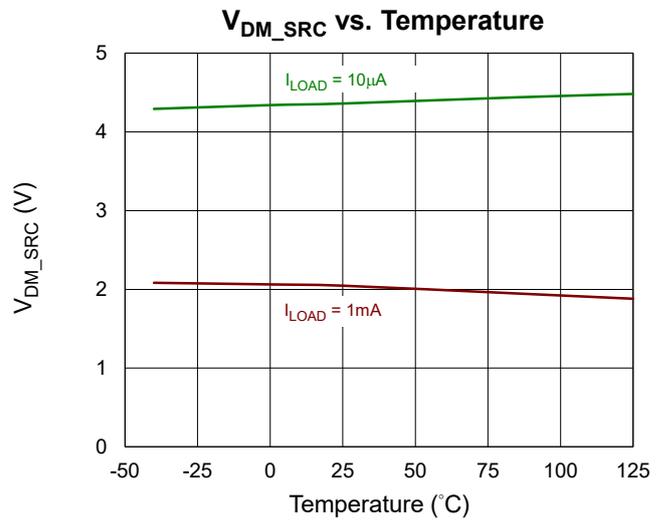
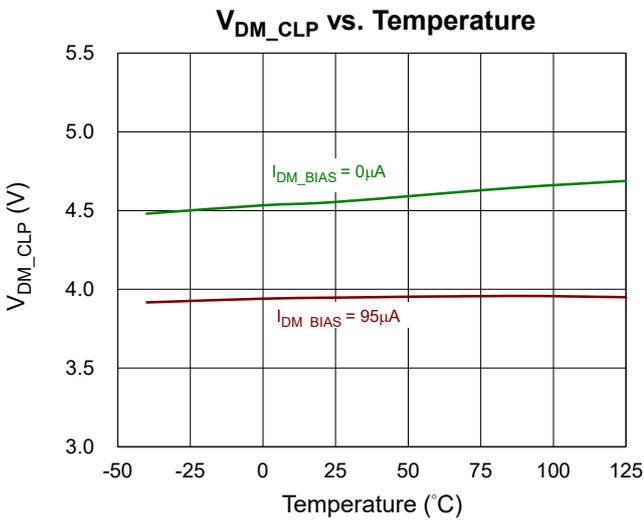
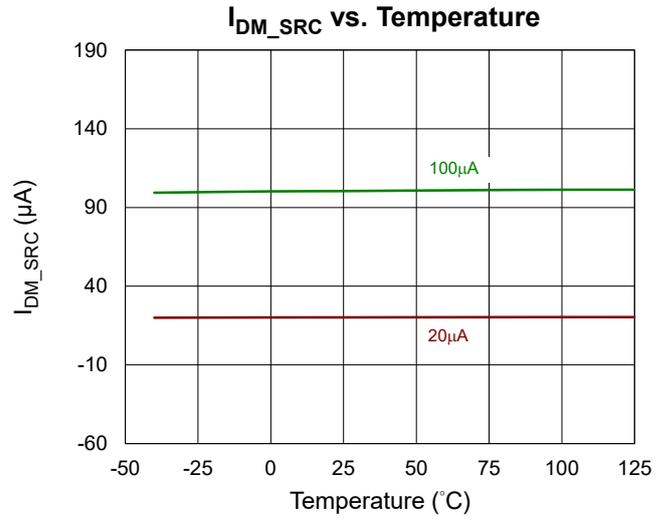
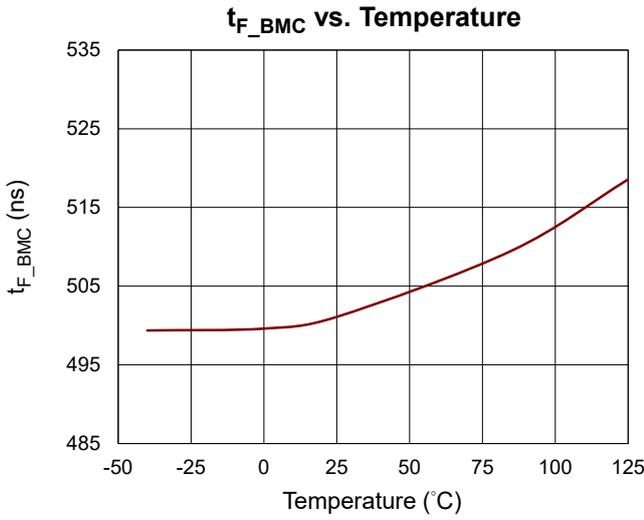
**$V_{CC\_IH}$  vs. Temperature**

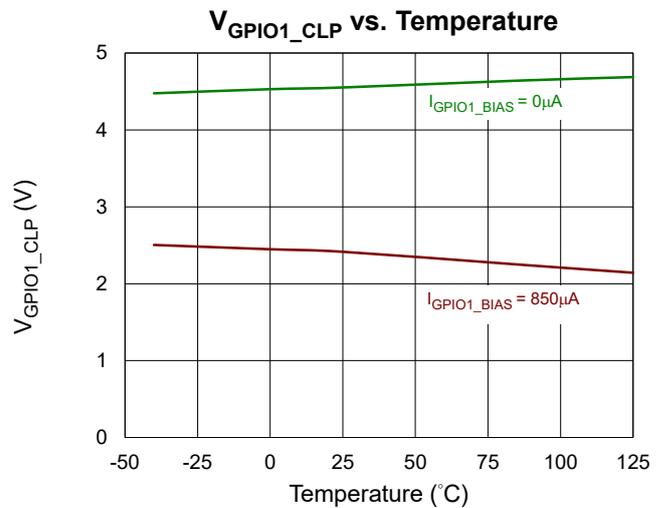
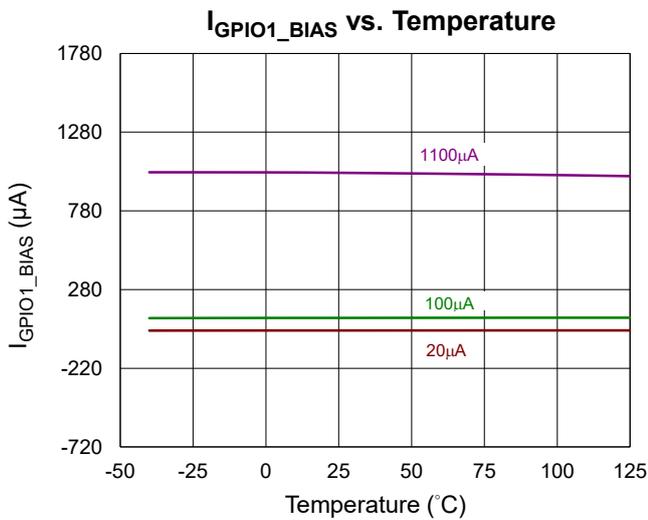
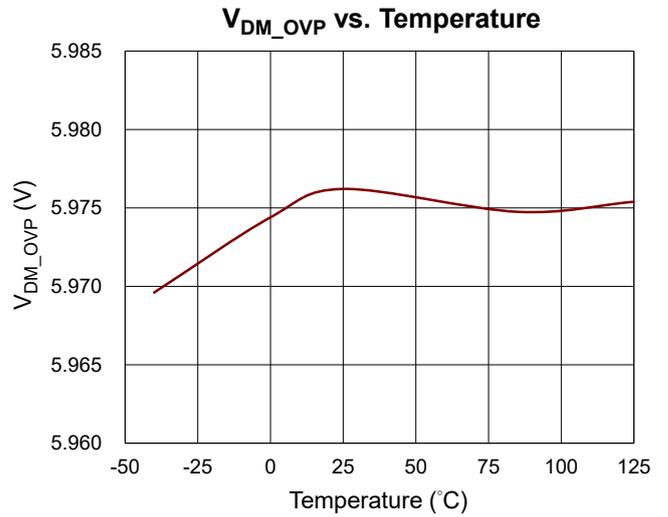
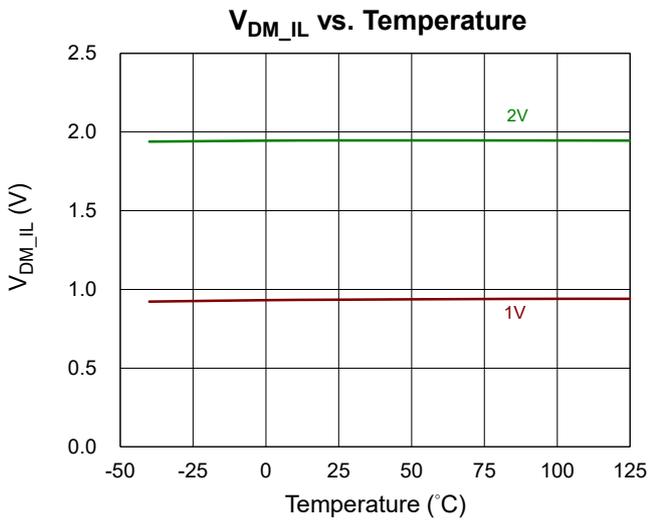
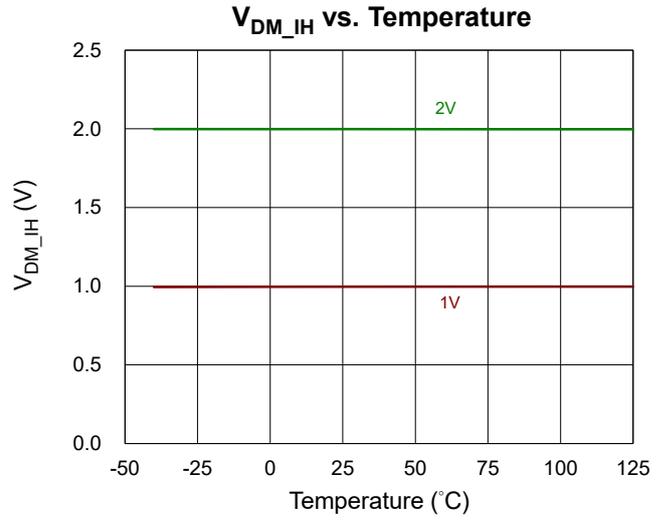
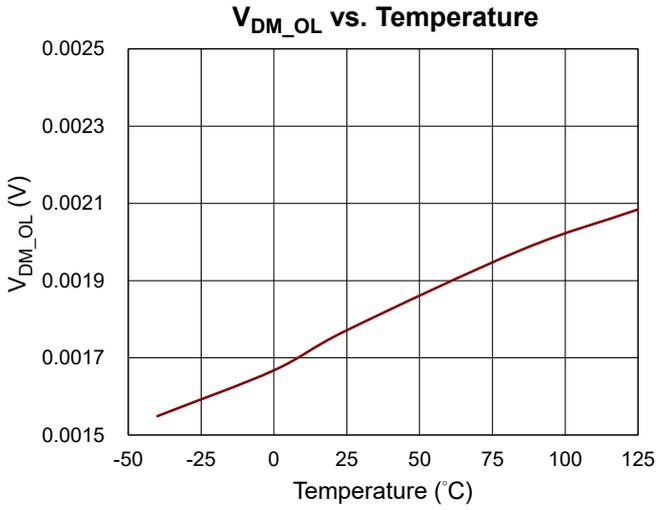


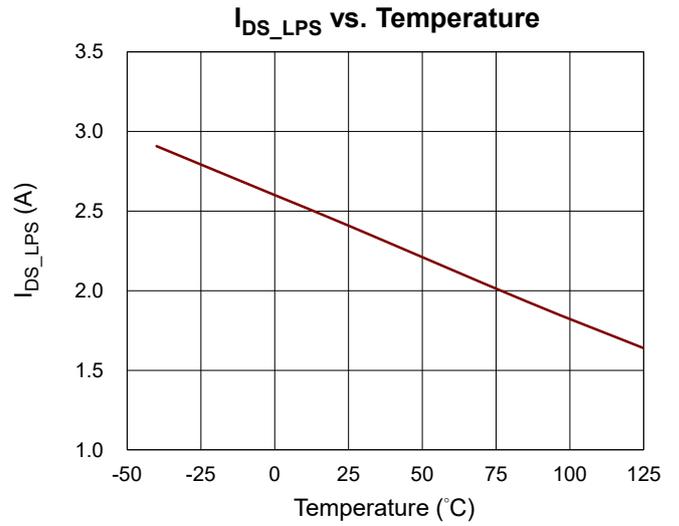
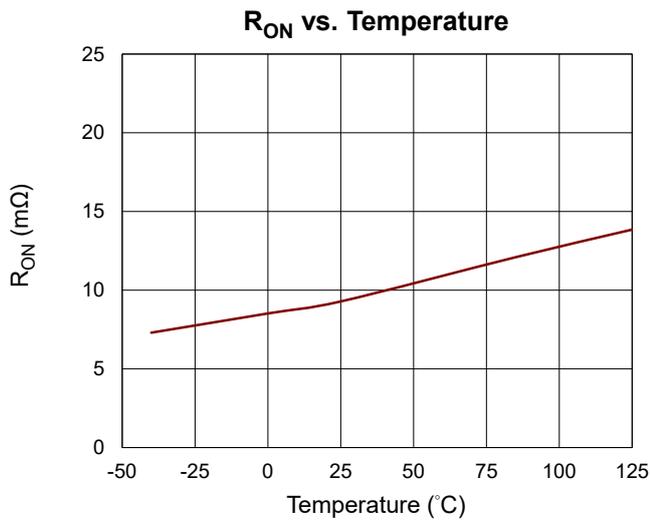
**$V_{CC\_OVP}$  vs. Temperature**













15.3 N-MOSFET Driver

The charge pump drives the integrated blocking N-MOSFET. The soft-start function is implemented using an 8-bit DAC to prevent voltage droop during startup conditions with capacitive loads.

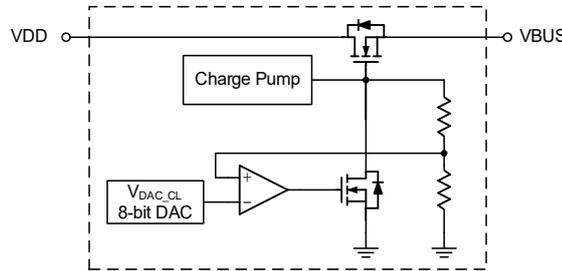


Figure 2. Soft-Start Function

15.4 Discharge

15.4.1 VDD Pin Discharger for Output Capacitor

The VDD pin provides discharge current control, acting as a bleeder to discharge the output capacitor when a device is detached or when a lower output voltage is requested, such as reducing VOUT from 20V to 5V. The I\_VDD\_DISCHG capability should consider both the operating voltage and output capacitance. The discharge current is programmable via the internal register based on power dissipation.

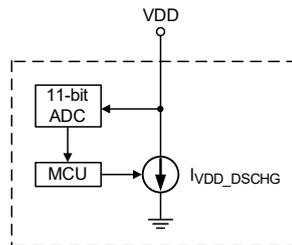


Figure 3. Discharge Current Control of the VDD Pin

15.4.2 VBUS Pin Discharger for Vsafe0V

The VBUS pin uses an open-drain driver to discharge the VBUS capacitor when a device is detached. The pin voltage is continuously monitored by the ADC, enabling the IC to determine compliance with the Vsafe0V specification.

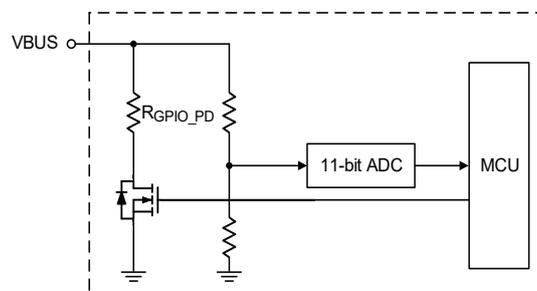


Figure 4. Open-Drain Driver of the VBUS Pin

**15.5 DM and GPIO Pins Functional Description**

The DM and GPIO pins support multiple functions, including general-purpose input and open-drain output. They can also be configured as current or voltage sources, and serve as ADC inputs for voltage monitoring. A hardware comparator enables voltage change detection and allows the device to wake up from power-saving mode.

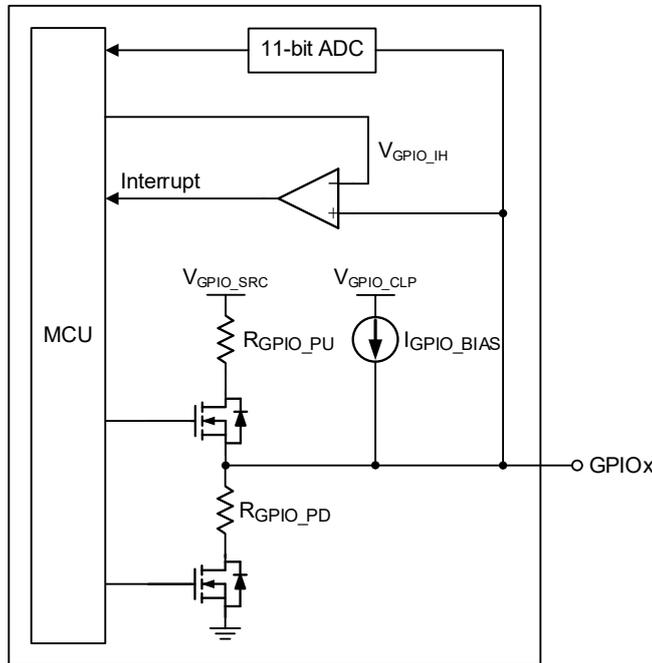


Figure 5. Internal Circuit Diagram of the DM and GPIO Pins

**15.6 CC1 and CC2 Pins Functional Description**

**15.6.1 CC Pin Attach/Detach Detection**

The CC pin supports attach/detach detection and current advertisement in accordance with the USB Type-C specification. Hardware comparators detect attach and detach events by instantly responding to voltage changes on the CC pin, allowing the system to quickly identify cable insertion or removal.

**15.6.2 PD PHY**

The USB PD PHY implements a BMC transceiver for communication over the CC channel. It supports packet encoding and decoding, CRC generation and checking, SOP/EOP detection, and clock recovery, ensuring robust and reliable data exchange between the protocol layer and the CC line.

**15.6.3 VCONN**

The device integrates a VCONN switch to supply power (up to 100mW) to active or electronically marked (e-marked) cables through the unused CC pin. The VCONN path features overcurrent protection to ensure safe operation.

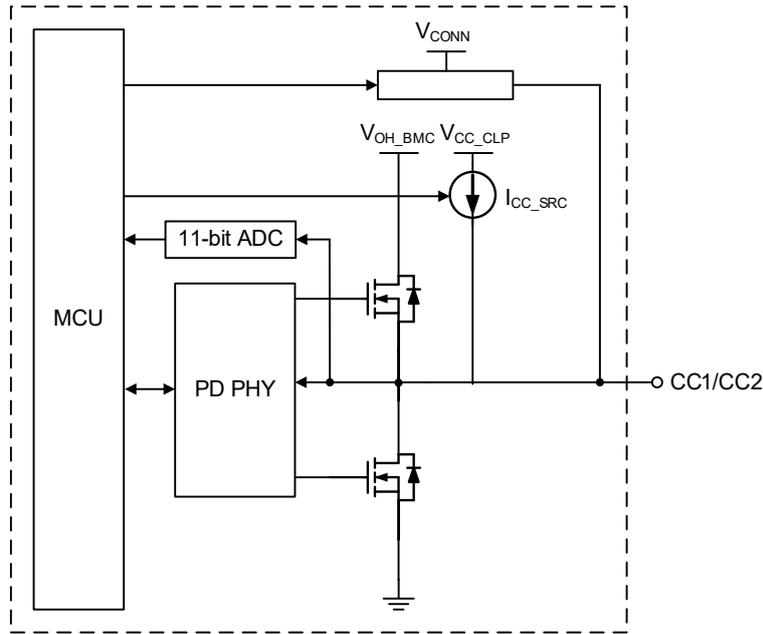


Figure 6. Internal Circuit Diagram of the CC1 and CC2 Pins

## 15.7 Temperature Sensing

### 15.7.1 Internal

A built-in temperature sensor supports temperature reporting and provides over-temperature protection (OTP).

### 15.7.2 External

The current source of the CC1, CC2, DM, and GPIO pins can source current to a thermistor, enabling the ADC to measure the resulting voltage. Temperature is calculated by converting this value according to the thermistor's characteristic table, supporting temperature reporting and over-temperature protection (OTP).

## 16 Application Information

(Note 7)

### 16.1 VDD Adaptive Overvoltage Protection

A fast turn-off blocking N-MOSFET provides VOUT overvoltage protection. When the internal voltage related to VDD exceeds the programmable threshold ( $V_{VDD\_OVP}$ ), the blocking N-MOSFET is immediately turned off and a fault flag is sent to the embedded MCU for customized protection actions. This mechanism safeguards against malfunctions such as optocoupler aging in the feedback loop.

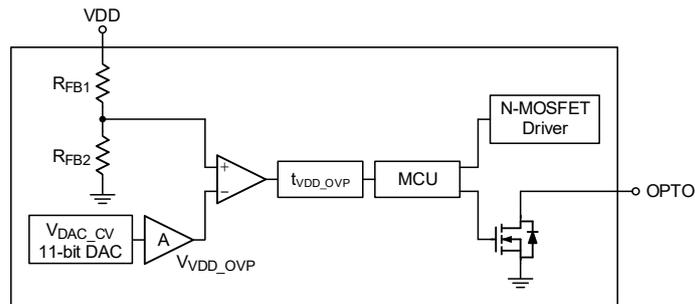


Figure 7. OVP Functional Diagram

### 16.2 VDD Adaptive Undervoltage Protection

A fast turn-off blocking N-MOSFET provides VOUT undervoltage protection. When the internal voltage related to VDD drops below the programmable threshold ( $V_{VDD\_UVP}$ ), the blocking N-MOSFET is immediately turned off and a fault flag is sent to the embedded MCU for customized protection actions. This mechanism safeguards against feedback failure and output short-circuit events.

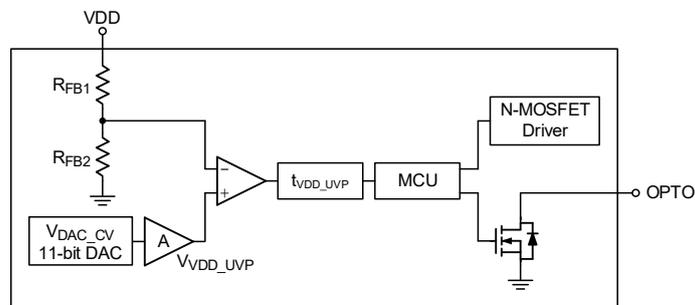


Figure 8. UVP Functional Diagram

16.3 Limited Power Source Protection

Limited Power Source (LPS) protection is implemented by monitoring both the drain-source voltage across the blocking MOSFET and the voltage across the current sense resistor. When the drain-source voltage exceeds the threshold corresponding to  $I_{DS\_LPS}$ , but the current sense voltage remains below the firmware-defined value, this indicates a mismatch between the actual current through the blocking MOSFET and the current sense reading. Under these conditions, LPS protection is triggered to ensure system safety.

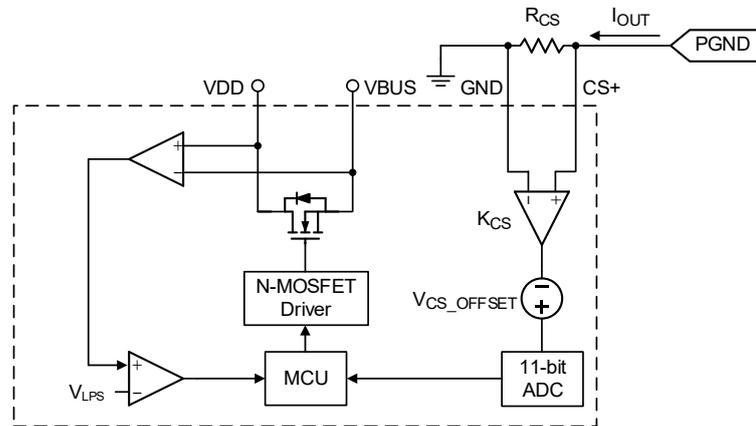


Figure 9. LPS Functional Diagram

16.4 Programmable Overcurrent Protection

Programmable overcurrent protection (OCP) is achieved by amplifying the voltage across the current sense resistor, adding an offset voltage, and converting the result with the ADC for current calculation. When the measured current exceeds the user-defined protection threshold, OCP is triggered to prevent damage and ensure system reliability.

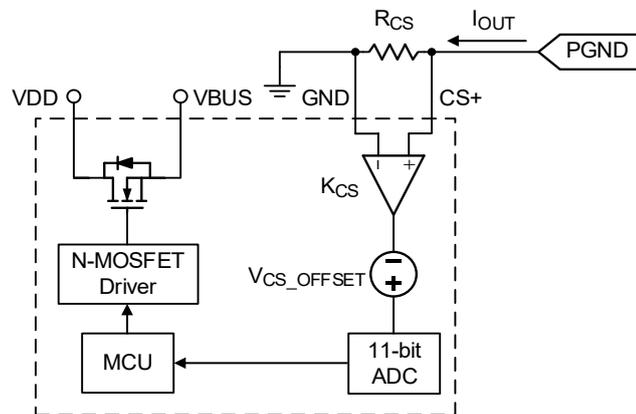


Figure 10. OCP Functional Diagram

**16.5 Programmable External and Internal Over-Temperature Protection**

Programmable external and internal over-temperature protection (OTP) is provided through real-time monitoring by an internal temperature sensor and by sourcing current to a thermistor via CC1, CC2, DM, or GPIO pins for external sensing. The MCU calculates the temperature from the ADC reading, and OTP is triggered when the measured value exceeds the set threshold.

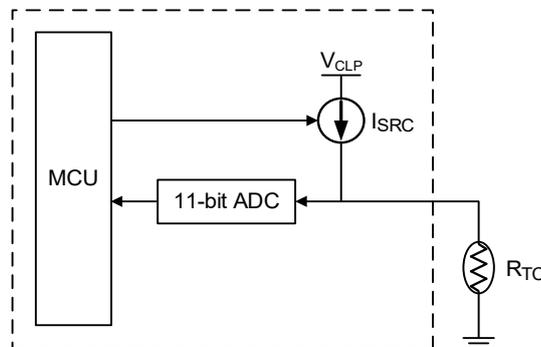


Figure 11. External OTP Functional Diagram

**16.6 Thermal Considerations**

The junction temperature should never exceed the absolute maximum junction temperature  $T_{J(MAX)}$ , listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance,  $\theta_{JA}$ , is highly package dependent. For a SOP-10 package, the thermal resistance,  $\theta_{JA}$ , is 139.56°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated as below:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (139.56^\circ\text{C/W}) = 0.72\text{W for a SOP-10 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed  $T_{J(MAX)}$  and the thermal resistance,  $\theta_{JA}$ . The derating curve in [Figure 12](#) allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

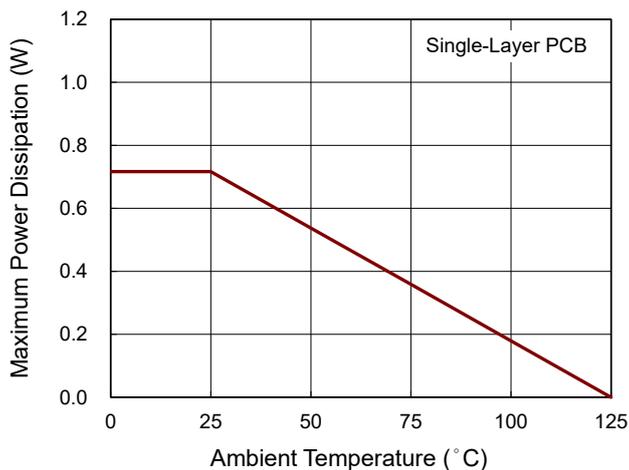
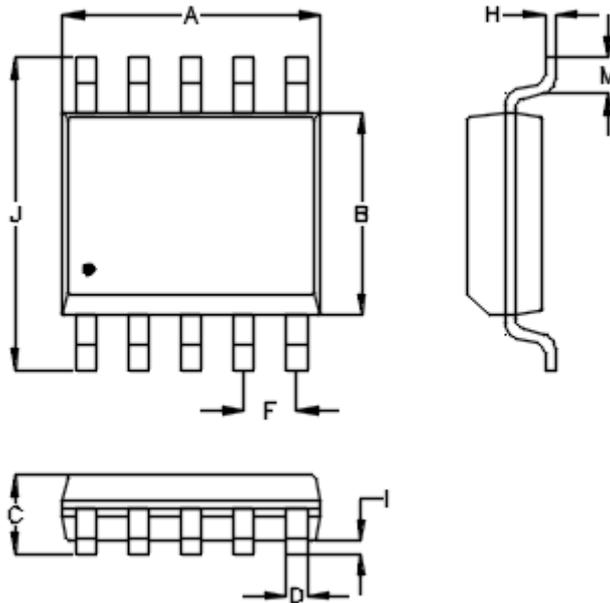


Figure 12. Derating Curve of Maximum Power Dissipation

**Note 7.** The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

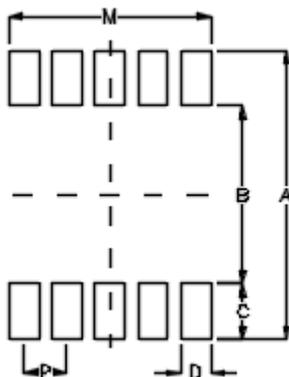
**17 Outline Dimension**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.800	5.000	0.189	0.197
B	3.800	4.000	0.150	0.157
C	1.300	1.750	0.051	0.069
D	0.300	0.500	0.012	0.020
F	1.000		0.039	
H	0.100	0.250	0.004	0.010
I	0.050	0.250	0.002	0.010
J	5.800	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

**10-Lead SOP Plastic Package**

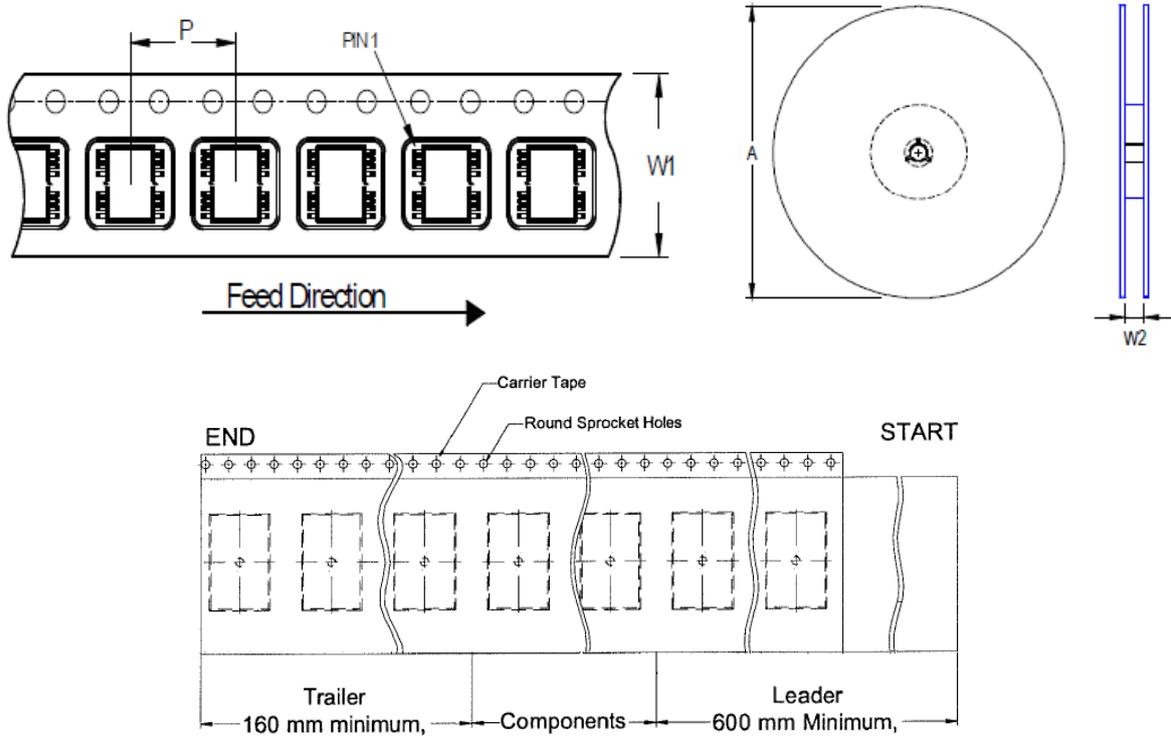
## 18 Footprint Information



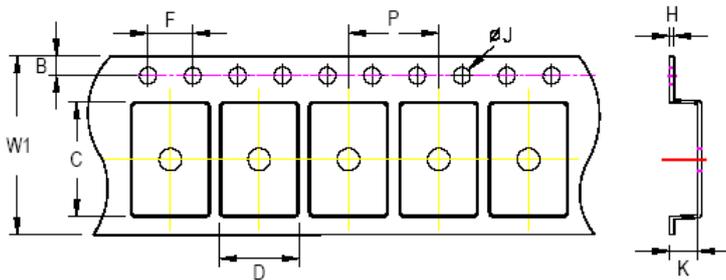
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-10	10	1.00	6.80	4.20	1.30	0.70	4.70	±0.10

**19 Packing Information**

**19.1 Tape and Reel Data**



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOP-10	12	8	330	13	2,500	160	600	12.4/14.4



**C, D, and K are determined by component size.**  
**The clearance between the components and the cavity is as follows:**  
**- For 12mm carrier tape: 0.5mm max.**

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.2mm	0.6mm

## 19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 13"</p>	4	 <p>1 reel per inner box <b>Box G</b></p>
2	 <p>HIC &amp; Desiccant (2 Unit) inside</p>	5	 <p>6 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box <b>Carton A</b></p>

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-10	13"	2,500	Box G	1	2,500	Carton A	6	15,000

**19.3 Packing Material Anti-ESD Property**

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
$\Omega/\text{cm}^2$	$10^4$ to $10^{11}$					

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## 20 Datasheet Revision History

Version	Date	Description
00	2025/12/24	First Edition