RICHTEK®

RT7220E

Synchronous Rectifier Controller for Asymmetrical Half-Bridge Converters with a Wide Output Voltage Operating Range

1 General Description

The RT7220E is a Synchronous Rectifier (SR) controller for Asymmetrical Half-Bridge (AHB) converters operating in Critical Conduction Mode (CRM), Cycle Skipping Mode (CSM), and Burst Mode (BM). The RT7220E detects the drain voltage of the MOSFET to control the on/off state of the SR gate. This functionality is intended to minimize turn-off dead-time and deliver sine-wave energy through the SR gate pulses, enhancing efficiency.

The RT7220E supports a wide output voltage range from 5V to 48V, and a HV LDO is built-in for the MOSFET gate driver at low output voltage. When used with the AHB controller RT7795, the double pulses function can be enabled to optimize efficiency at heavy load/low output voltage.

Furthermore, the RT7220E provides green mode operation under light load conditions, reducing operation current to below 160μA.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

2 Ordering Information

RT7220E □-□□□□

Packing
A: Standard

Trim Code
(Refer to Version Table)

Package Type(1)
S: SOP-8

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Features

- **Suitable for Low-Side SR Control of AHB in CRM, CSM, and BM**
- **Suitable for 5V to 48V V_{OUT} Range**
- **Double Pulses Function to Optimize Efficiency (Works with the AHB Controller RT7795)**
- **<1.2mA Operating Current in Normal Mode**
- **<160μA Operating Current in Green Mode**
- **Built-In HV LDO to Supply SR Driver when V_{VDD} is Lower than 4.5V**
- **Automatic Dead-Time Tracking Control to Optimize Efficiency**
- **Protection**
  - **SR Gate Driver with V_{BIAS} Clamp**
  - **SR Gate Initial Pull-Low before Start-Up**
  - **SR Minimum On-Time**

4 Applications

- USB PD Power Converters
- Fast-Charger Power Adapters
- General Purpose High-Efficiency and/or Compact-Size AHB Power Converters

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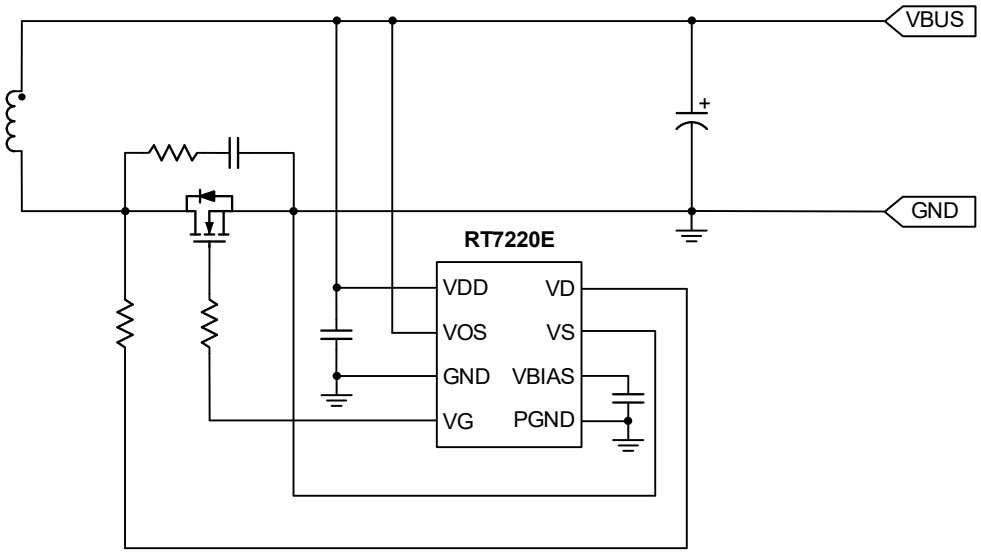
5 Simplified Application Circuit



6 Marking Information

RT7220ES-EDCA

RT7220
ESEDC
•YMDAN

RT7220ESEDC: Product Code
YMDAN: Date Code

RT7220ES-EEAA

RT7220
ESEEA
•YMDAN

RT7220ESEEA: Product Code
YMDAN: Date Code

RT7220ES-SDAA

RT7220
ESSDA
•YMDAN

RT7220ESSDA: Product Code
YMDAN: Date Code

7 RT7220E Version Table

Part Number	RT7220ES-EDCA	RT7220ES-SDAA	RT7220ES-EEAA
VD Voltage Supported	160V	160V	160V
Output Voltage Supported	5V to 48V	5V to 48V	5V to 48V
Maximum Operation Frequency	250kHz	250kHz	250kHz
HV LDO	160V/77mA	160V/77mA	160V/77mA
VBIAS Output Voltage	8V	6V	8V
Debounce Time of Diode On for VG	350ns	200ns	200ns
Falling Time Threshold for VG Trigger	100ns	100ns	150ns

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Table of Contents

1 General Description 1
2 Ordering Information 1
3 Features 1
4 Applications 1
5 Simplified Application Circuit 2
6 Marking Information 2
7 RT7220E Version Table 2
8 Pin Configuration 4
9 Functional Pin Description 4
10 Functional Block Diagram 4
11 Absolute Maximum Ratings 5
12 Recommended Operating Conditions 5
13 Electrical Characteristics 6
14 Typical Application Circuit 10
15 Operation 11
15.1 Power Structure 17
15.2 Drain Voltage Sense 17
15.3 Gate Driver 17
15.4 Source Voltage Sense 17
15.5 Double Pulses Function 17
16 Application Information 18
16.1 Power Selection 18
16.2 VG Turn-On 18
16.3 VG Turn-Off 19
16.4 VG Minimum On-Time 19
16.5 Green Mode Operation 19
16.6 Output Voltage Sense for VD Blanking Time 20
16.7 VD Undervoltage Protection 21
16.8 VG Double Pulses Function 21
16.9 Thermal Considerations 22
16.10 Design Considerations and PCB Layout Guide 22
17 Outline Dimension 24
18 Footprint Information 25
19 Packing Information 26
19.1 Tape and Reel Data 26
19.2 Tape and Reel Packing 27
19.3 Packing Material Anti-ESD Property 28
20 Datasheet Revision History 29

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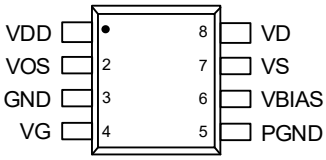
8 Pin Configuration

(TOP VIEW)

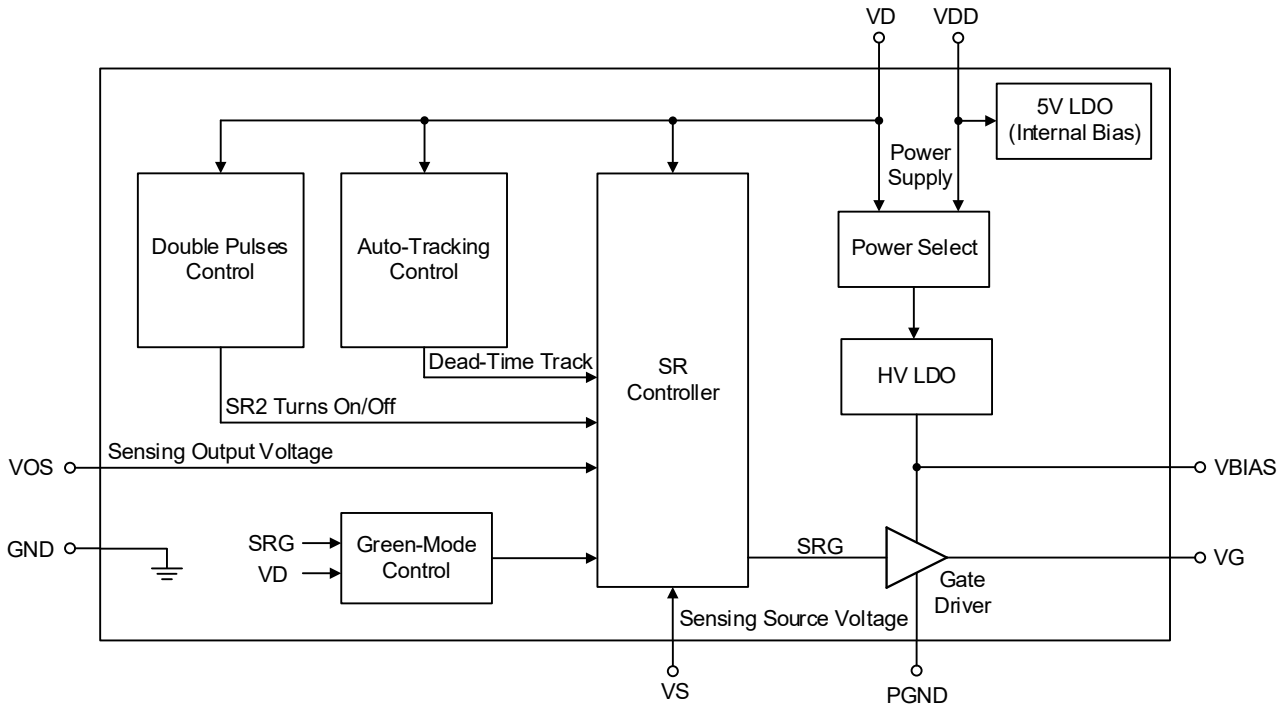


SOP-8

9 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD	Supply voltage.
2	VOS	Output voltage sensing node.
3	GND	Ground.
4	VG	Gate driver output for the SR MOSFET.
5	PGND	Ground of gate driver.
6	VBIAS	Regulated DC bias.
7	VS	Source voltage sensing node for the SR MOSFET.
8	VD	Drain voltage sensing node for the SR MOSFET.

10 Functional Block Diagram



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11 Absolute Maximum Ratings

(Note 2)

- VD to GND ---------- –1V (Pulse width 500ns) to 180V
- VOS to GND ---------- –0.3V to 60V
- VDD to GND ---------- –0.3V to 60V
- VBIAS to GND ---------- –0.3V to 10V
- VG to GND ---------- –0.3V to V_{VBIAS} + 0.3V
- VS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 ---------- 0.53W
- Package Thermal Resistance (Note 3)

  SOP-8, θ_{JA} ---------- 188°C/W

  SOP-8, θ_{JC} ---------- 47°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VD ---------- –1V (Pulse width 500ns) to 160V
- Supply Input Voltage, VDD ---------- 5V to 48V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

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13 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD Section							
VDD Turn-On Threshold Voltage	V_{VDD_ON}			3.1	3.25	3.4	V
VDD Turn-Off Threshold Voltage	V_{VDD_OFF}			2.7	2.8	2.9	V
Hysteresis Voltage between VDD Turn-On and Turn-Off Threshold	V_{VDD_HYS}			0.35	0.45	0.55	V
VDD Start-Up Current	I_{DD_ST}	Rising V_{VDD} = V_{VDD_ON} - 0.1V		--	--	200	μA
VDD Operating Current	I_{DD_OP}	V_{VDD} = 5V, the VG pin is open.		--	0.9	1.2	mA
VDD Green-Mode Current	I_{DD_GREEN}	In green mode. V_{VDD} = 5V		--	120	160	μA
VOS Section							
VOS Threshold Voltage to Disable the Second VG Pulse	$V_{TH_DIS_VG2}$			13.5	14.5	15.5	V
VOS Threshold Voltage to Enable the Second VG Pulse	$V_{TH_EN_VG2}$			$V_{TH_EN_VG2}$ – 1V	$V_{TH_EN_VG2}$ – 0.5V	$V_{TH_EN_VG2}$ – 0.2V	
VBIAS Section							
VBIAS Output Voltage	V_{VBIAS}	I_{LOAD} = 30mA, 55V ≥ V_{VDD} ≥ 9V	RT7220ES-EDC, RT7220ES-EEA	7.6	8	8.4	V
		I_{LOAD} = 25mA, 55V ≥ V_{VDD} ≥ 6.9V	RT7220ES-SDA	5.5	6	6.5	
		I_{LOAD} = 30mA, 4.7V < V_{VDD} < 8V	RT7220ES-EDC, RT7220ES-EEA	V_{VDD} – 0.55	--	V_{VDD}	
		I_{LOAD} = 30mA, 4.7V < V_{VDD} < 6V	RT7220ES-SDA	V_{VDD} – 0.63	--	V_{VDD}	
		V_{VDD} < 4.5V. The power path for the SR driver is from the V_{VD} and it detects V_{VDD} cycle by cycle to change the power source.		4.6	4.8	5	
VBIAS Current-Limit Level	I_{VBIAS_CL}			60	77	94	mA

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
SR Driver Section							
Output High Voltage	V_{OH_VG}	Sourcing I_{VG} = 100mA, V_{VBIAS} = V_{VDD} = 8V	RT7220ES-EDC, RT7220ES-EEA	7.06	7.25	7.46	V
		Sourcing I_{VG} = 100mA, V_{VBIAS} = V_{VDD} = 6V	RT7220ES-SDA	5	5.25	5.5	
Output Low Voltage	V_{OL_VG}	Sinking I_{VG} = 100mA, V_{VBIAS} = V_{VDD} = 8V	RT7220ES-EDC, RT7220ES-EEA	0.04	0.1	0.16	V
		Sourcing I_{VG} = 100mA, V_{VBIAS} = V_{VDD} = 6V	RT7220ES-SDA	0.04	0.1	0.16	
Rise Time	t_{R_VG}	C_{VG} = 10nF, V_{VG} = 1V to V_{VBIAS} - 1V	RT7220ES-EDC RT7220ES-EEA	78	142	240	ns
			RT7220ES-SDA	50	108	200	
Turn-On Propagation Time	t_{P_ON}	From V_{VD} falling edge and the end of the $t_{DB_DON_NM}$ to V_G = 1V, C_{VG} = 0nF (Note 6)		--	--	50	ns
Fall Time	t_{F_VG}	C_{VG} = 10nF, V_{VG} = V_{VBIAS} - 1V to 1V	RT7220ES-EDC, RT7220ES-EEA	--	24	62	ns
			RT7220ES-SDA	--	17	50	
Turn-Off Propagation Time	t_{P_OFF}	(Note 6)		--	--	30	ns
Initial Output Low Clamping Voltage before Start-up	$V_{OL_VG_INI}$	C_{GD} = 330pF, C_{GS} = 27pF, V_{VD} is from 0V to 40V, t_R = 50ns, pulse width = 1μs (Note 6)		--	--	1	V
Internal Pull-Low Resistor	R_{PL_SR}			70	100	130	kΩ
VD Section							
Ratio of VD to GND Resistor Divider	K_{VD}	(Note 6)		1.64	1.67	1.69	%
Ratio of VD Sample and Hold at VD Voltage Rising	$K_{TH_VDH_R}$	$V_{TH_SH_R}[n]$ = $K_{TH_VDH_R}$ x $V_{VD_SH}[n-1]$		80.7	85	89.3	%
Ratio of VD Sample and Hold at VD Voltage Falling	$K_{TH_VDH_F}$	$V_{TH_SH_F}[n]$ = $K_{TH_VDH_F}$ x $V_{VD_SH}[n-1]$		66.5	70	73.5	%
Debounce Time before Sampling VD Voltage	t_{DB_VDSH}	V_{VD} > $V_{TH_SH_R}$ (Note 6)		50	100	130	ns

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Initial VD Blanking Time	$t_{BLK_VD_L}$	V_{VD} blanking time is counted after t_{DB_VDSH} when V_{VD} > K_{VIN_LOW} x V_{VOS}		0.188	0.25	0.313	μs
V_{IN} Low VD Blanking Time	$t_{BLK_VD_H}$	V_{VD} blanking time is counted after t_{DB_VDSH} when V_{VD} < K_{VIN_LOW} x V_{VOS}		1.2	1.5	1.8	μs
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When V_{VD} < K_{VIN_LOW} x V_{VDD}, V_{VD} blanking time will be changed to V_{IN} low blanking time.		200	220	240	%
Voltage Threshold of Lower VD Voltage-Level Detection at VD Voltage Rising	$V_{TH_VDL_R}$			2.85	3.0	3.15	V
Voltage Threshold of Lower VD Voltage-Level Detection at VD Voltage Falling	$V_{TH_VDL_F}$			2.55	2.8	3.05	V
Threshold Voltage of SR MOSFET Body Diode Turn-On Detection	V_{TH_DON}			–0.4	–0.3	–0.2	V
Threshold Voltage of SR MOSFET Body Diode Turn-Off Detection	V_{TH_DOFF}			–0.36	–0.25	–0.13	V
VG Fast Turn-Off Initial Threshold	$V_{TH_ZCD_MIN}$	(Note 6)		–12.1	–10.5	–9	mV
Maximum VG Fast Turn-Off Limit for Tracking Up/Down	$V_{TH_ZCD_MAX}$	With 5-bit tracking control.		0	5	10	mV
VG Fast Turn-Off Step Limit for Tracking Up/Down	ΔV_{TH_ZCD}	$V_{TH_ZCD}[n] = V_{TH_ZCD}[n-1] \pm \Delta V_{TH_ZCD}$		0.45	0.5	0.55	mV
Falling Time Threshold for VG Trigger	t_{VD_FALL}	V_{VD} falling edge is from $V_{TH_SH_F}$ to $V_{TH_VDL_F}$.	RT7220ES-EDC, RT7220ES-SDA	75	100	125	ns
			RT7220ES-EEA	100	150	200	
Mode Detection Period of Exit/Enter Green Mode Detection	t_{MCD}			8.5	10	11.5	ms
Debounce Time of SR Diode Turn-On Detection in Green-Mode	$t_{DB_DON_GM}$			--	1	--	μs
Number of VD Cycles Required to Enter Green Mode	N_{TH_F}	The number of VG pulses in t_{MCD} is less than N_{TH_F}. (Note 6)		--	32	--	Puses
Number of VD Cycles Required to Exit Green Mode	N_{TH_R}	The number of diode_on pulses in t_{MCD} is greater than N_{TH_R}.		--	64	--	Pulses
SR Control Section							
Number of VG Pulse in One PWM Switching Period	N_{VG}			--	1	2	Pulses

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Wide Second Diode Conduction Duration	$t_{ON_WIDE_DON2}$	From 2nd diode's turn-on edge to turn off edge.	1.6	2	2.4	μs
Width Threshold of Wide Second VG Pulse	$t_{ON_WIDE_SR2}$	From second VG pulse rising edge to second VG pulse falling edge.	1.6	2	2.4	μs
Longer ZCD Blanking Time	$t_{BLK_ZCD_L}$	When "VG pulls low at the end of the $t_{BLK_ZCD_S}$" and "a 2nd VG pulse comes or a Wide-Second-Diode-Conduction-Duration event is detected", the next ZCD blanking time (of the present phase) will be changed to the longer ZCD blanking time $t_{BLK_ZCD_L}$.	1.6	2	2.4	μs
Shorter ZCD Blanking Time	$t_{BLK_ZCD_S}$	When the VG pulls low at the end of the $t_{BLK_ZCD_L}$, the next ZCD blanking time (of the present phase) will be changed to the $t_{BLK_ZCD_S}$.	0.4	0.5	0.6	μs
Threshold Voltage of Middle VD Voltage-Level Detection at VD Voltage Rising	V_{TH_VDM}	When V_{VD} < V_{TH_VDM}, VG will be disabled. (Note 6)	V_{OUT} + 0.4	V_{OUT} + 1.6	V_{OUT} + 2.8	V
Debounce Time of Diode Turn-On Detection before Turning On SR MOSFET	$t_{DB_DON_NM}$	The debounce time starts when falling V_{VD} < V_{TH_DON} and after the end of the t_{VD_FALL}. At the end of the time, the VG pulls high to turn on the SR MOSFET. — RT7220ES-EDCA — VOS < $V_{TH_EN_VG2}$	280	350	420	ns
		RT7220ES-EDCA — VOS > $V_{TH_DIS_VG2}$	150	200	250	
		RT7220ES-SDA, RT7220ES-EEA	150	200	250	
Leading Edge Blanking Time of Reverse-Current-Limit	t_{BLK_RCL}	The time starts at V_{VD} rising edge.	210	300	390	ns
Reverse-Current-Limit Threshold Voltage	V_{TH_RCL}	Between the end of the t_{BK_RCL} and the end of the t_{BLK_ZCD}, the SR MOSFET is turned off when rising V_{VD} > V_{TH_RCL}.	24	30	36	mV
Automatic Tracking Section						
Auto-Tracking Dead Time	t_{DEAD_TRACK}	From VG falling edge to V_{VD} = V_{TH_DOFF}	80	100	120	ns

Note 6. Guaranteed by design.

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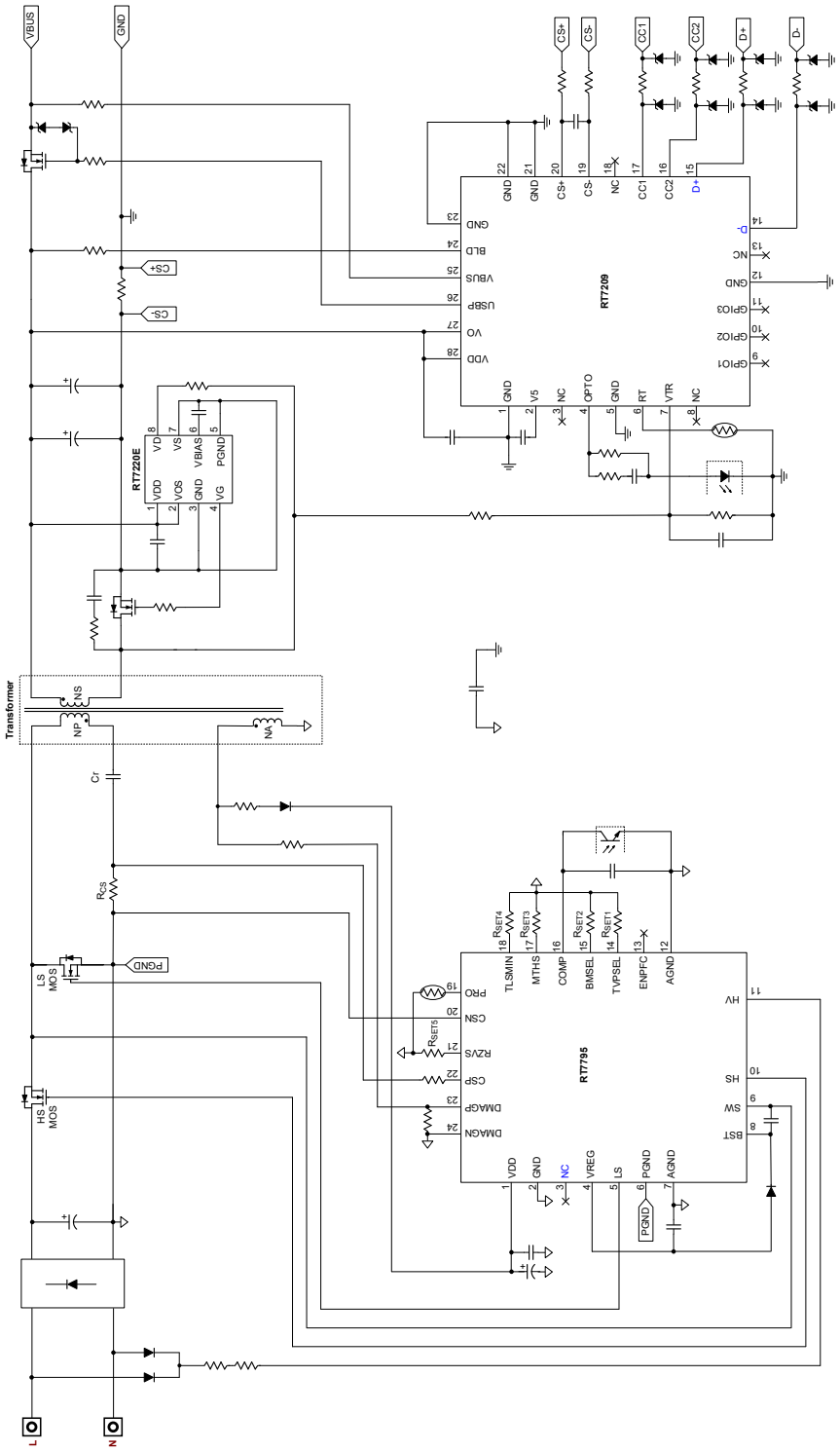
14 Typical Application Circuit



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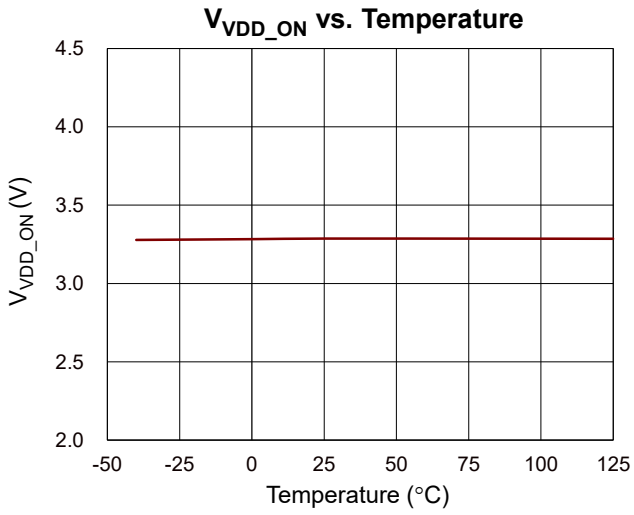
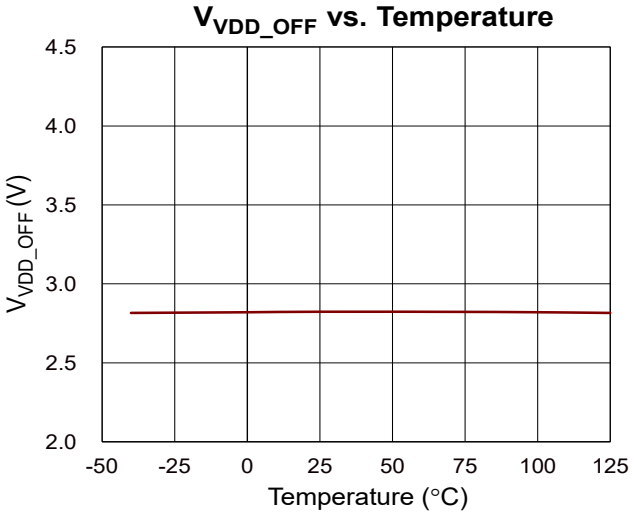
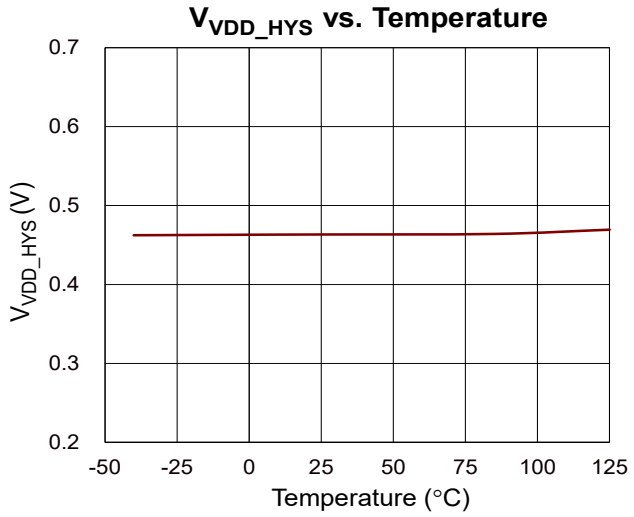
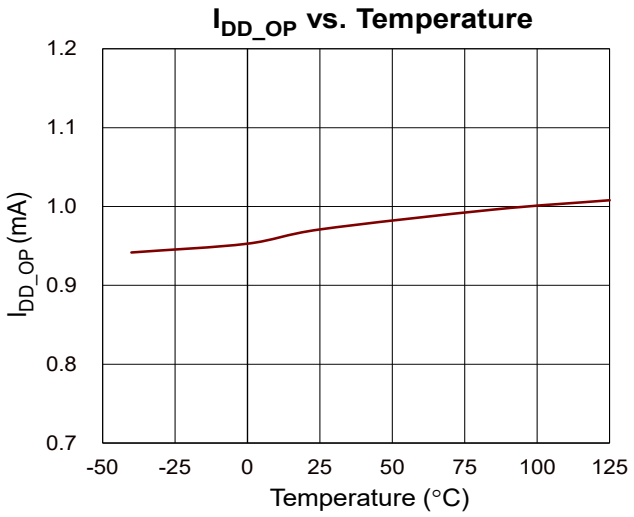
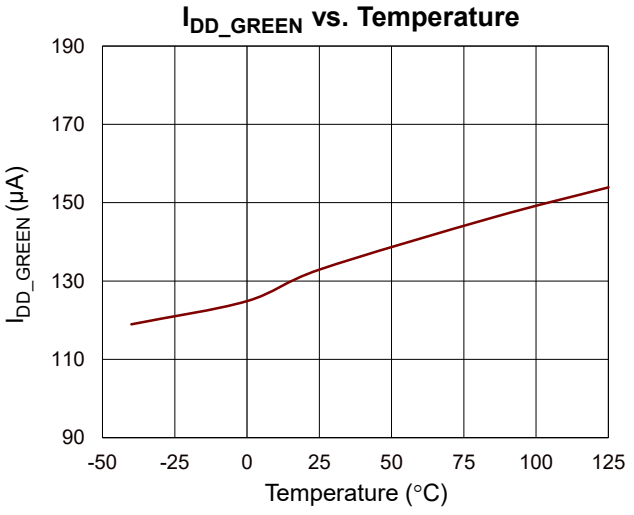
15 Typical Operating Characteristics

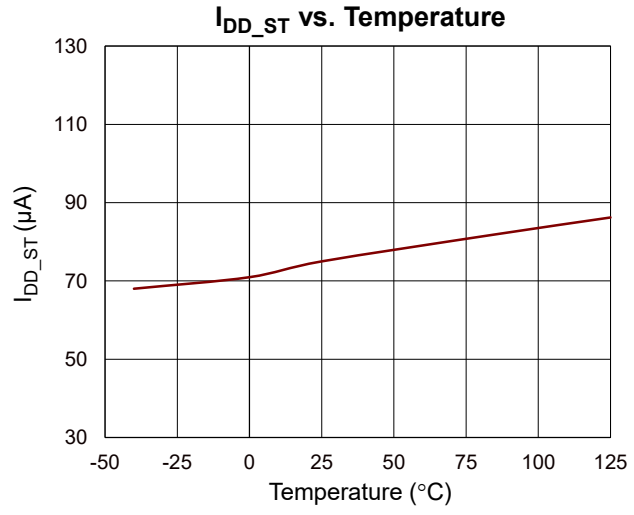












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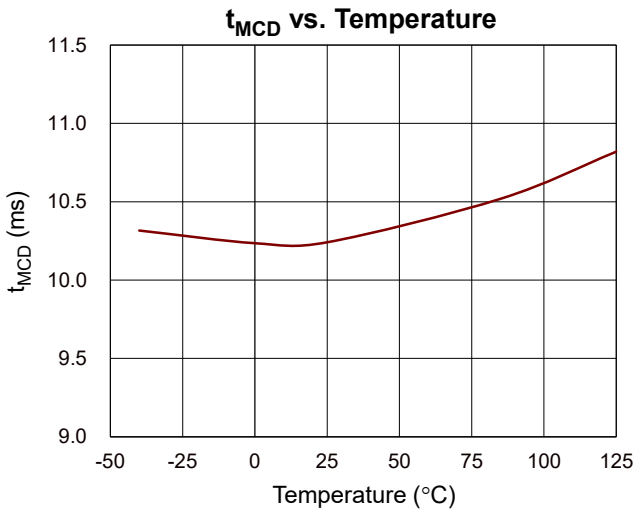

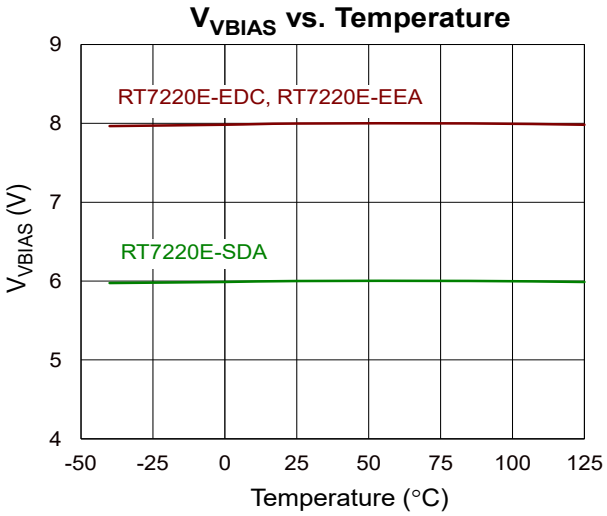

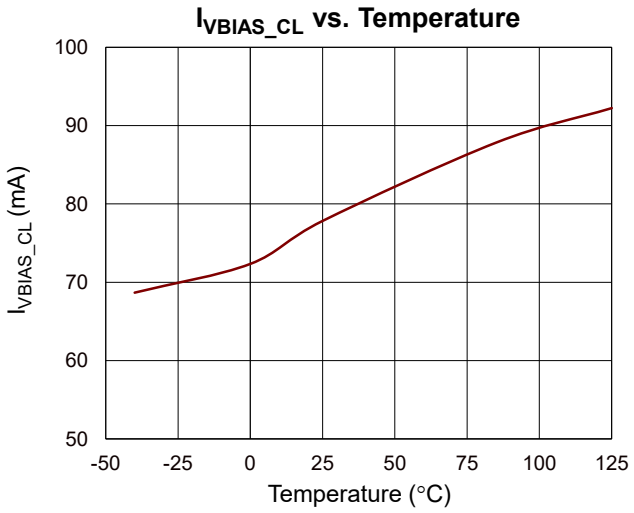

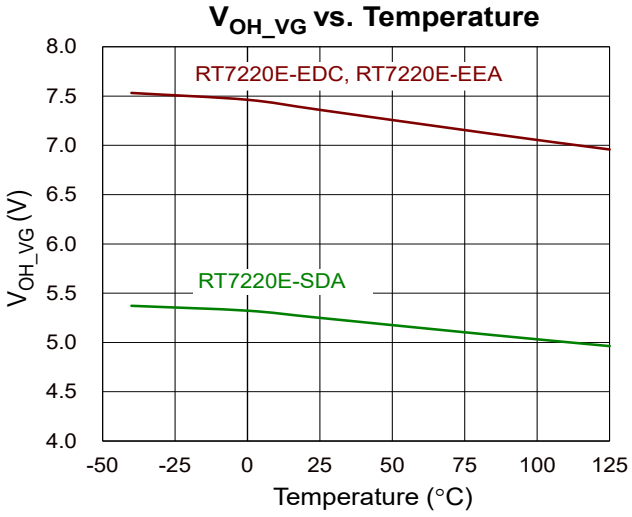

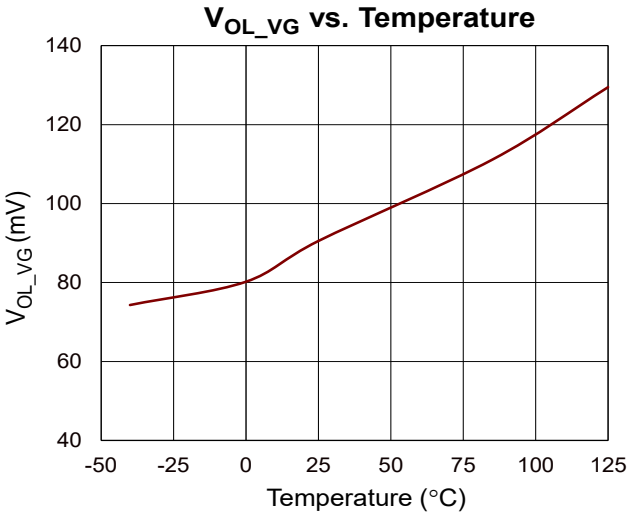

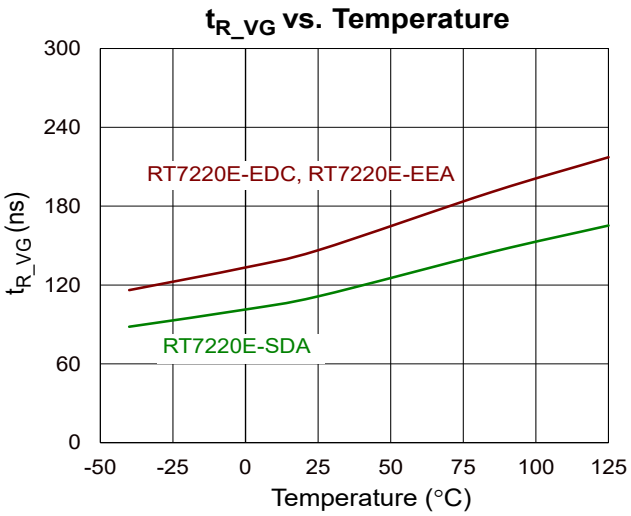

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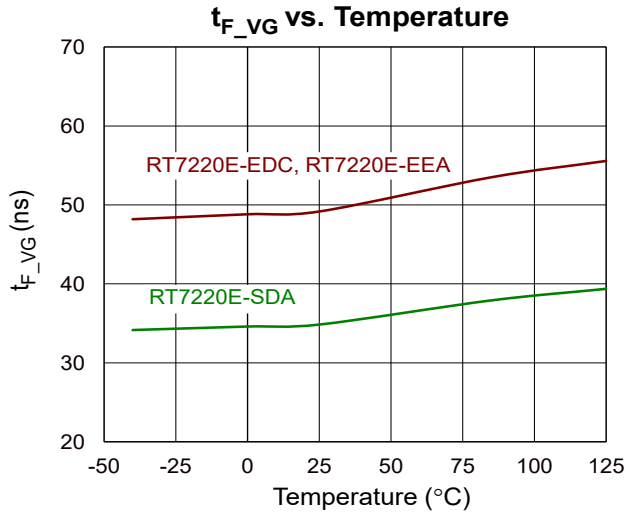

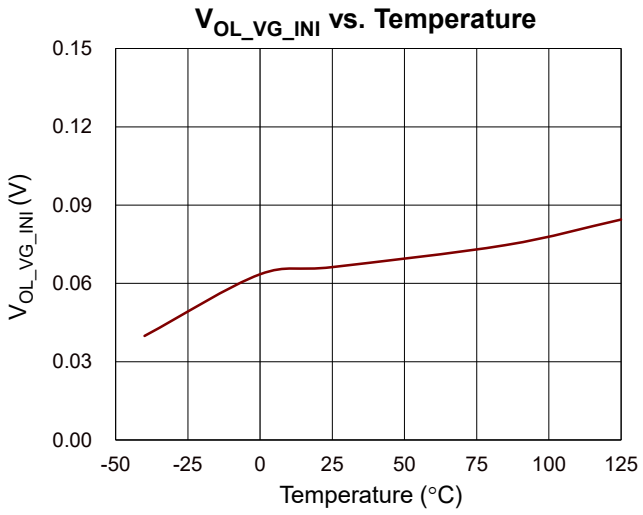

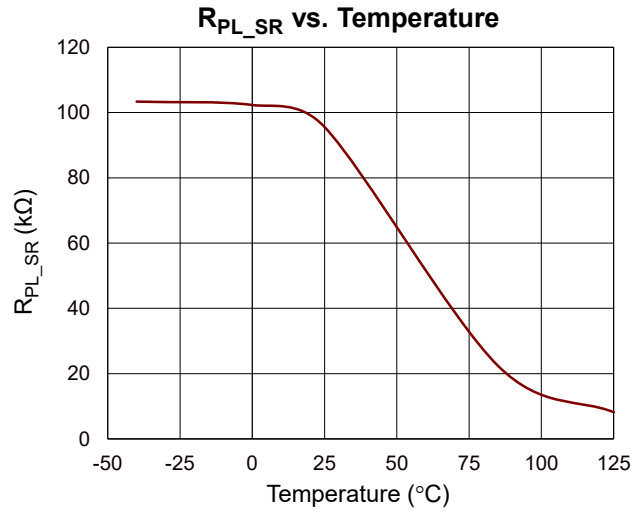

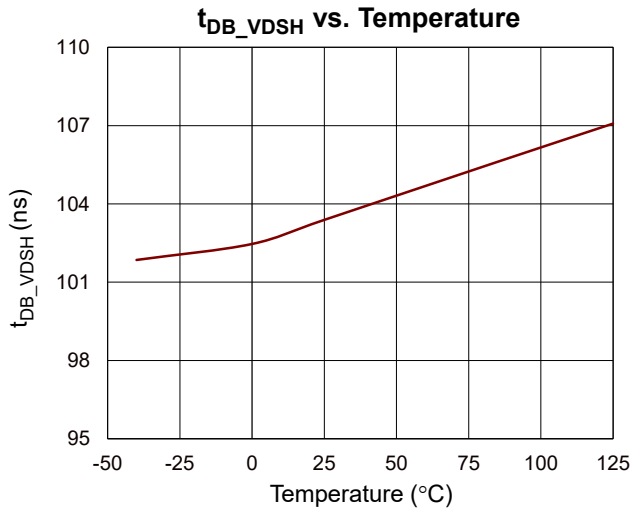

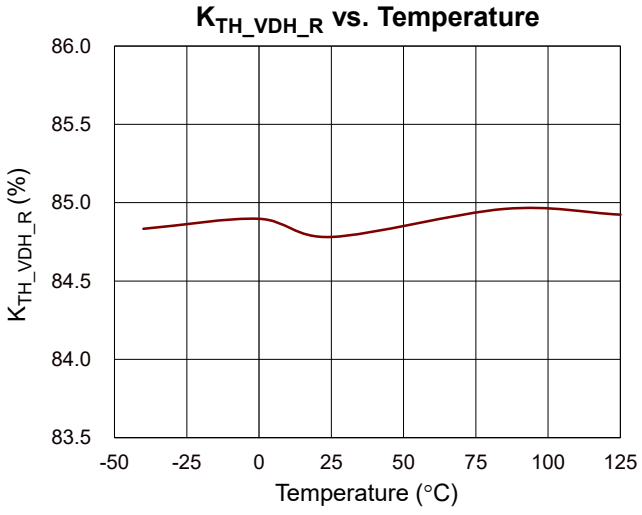

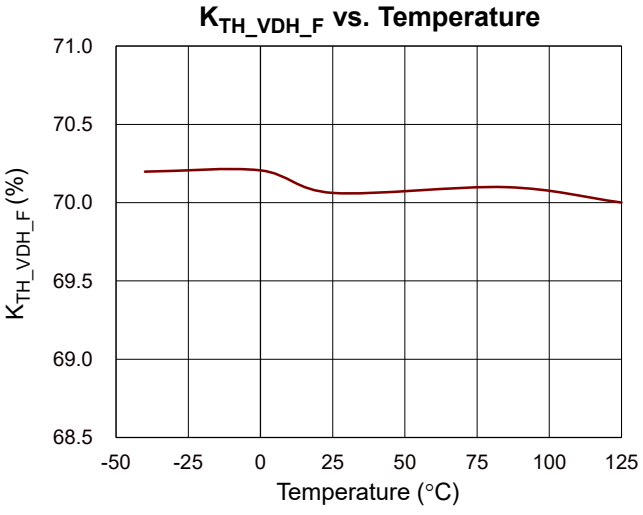

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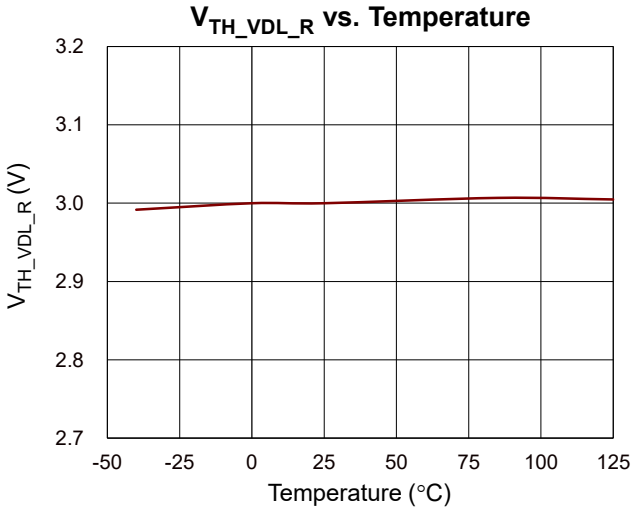

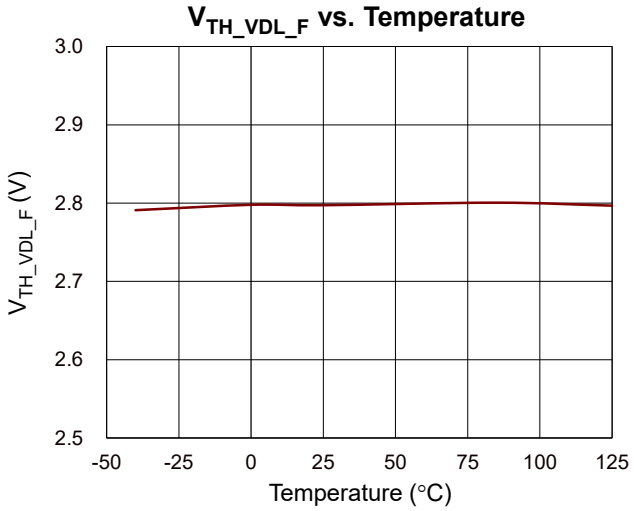

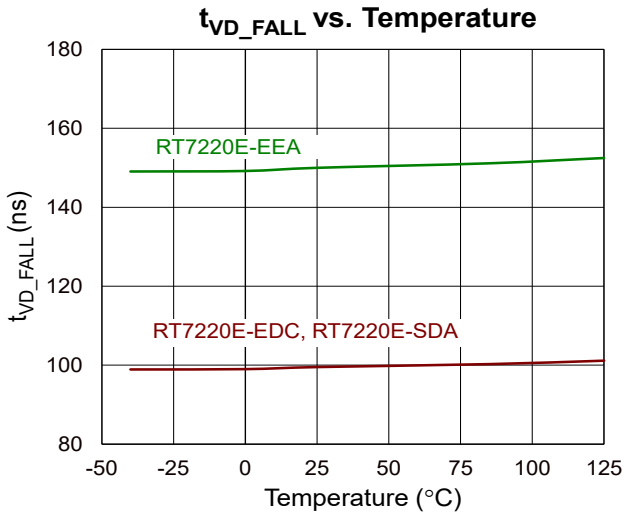

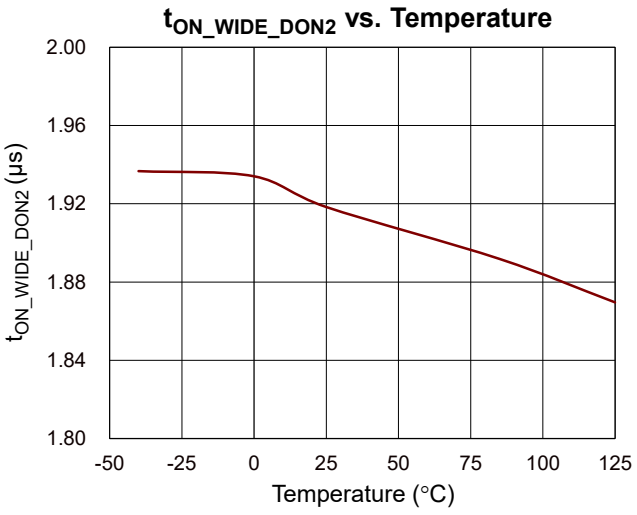

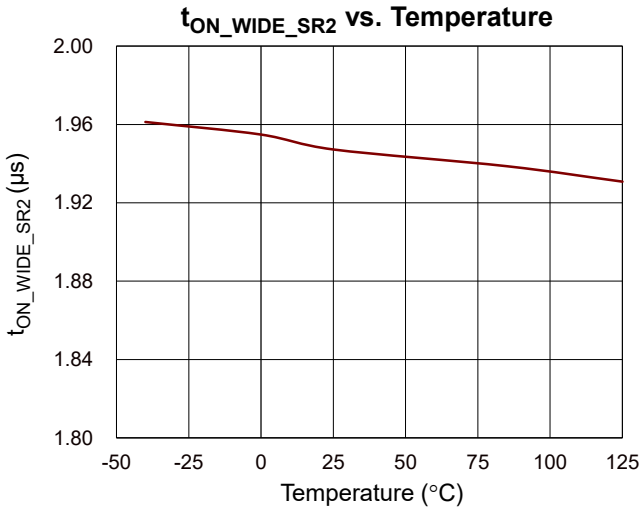

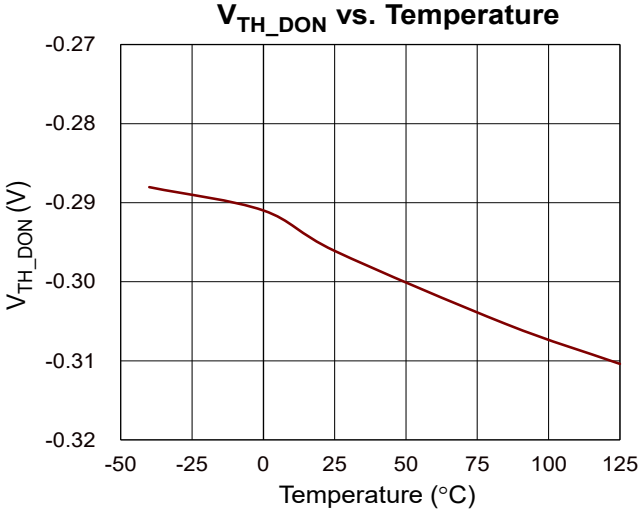

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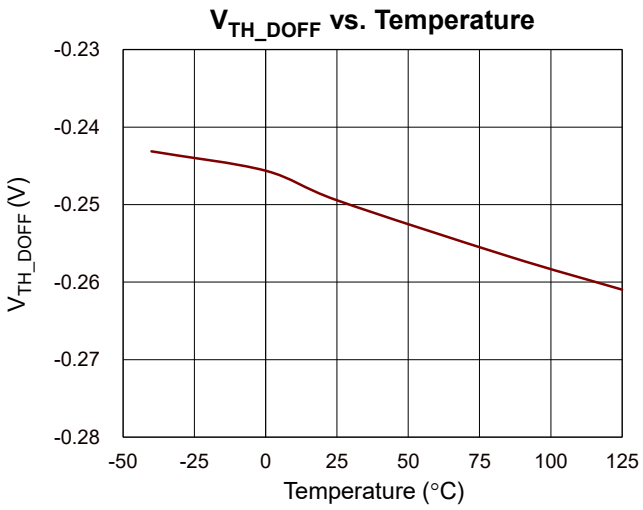

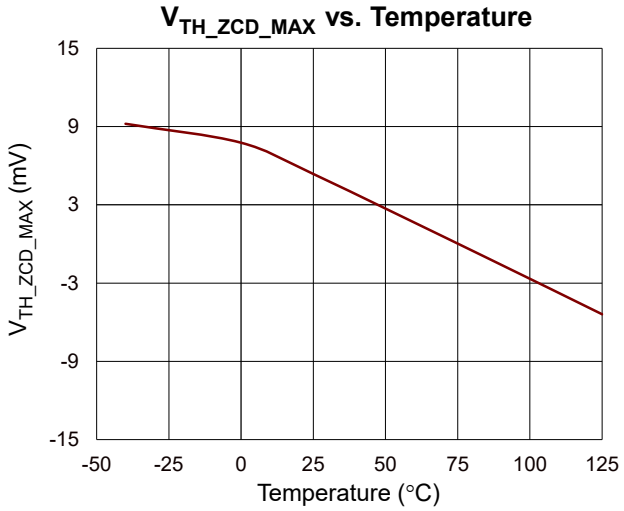

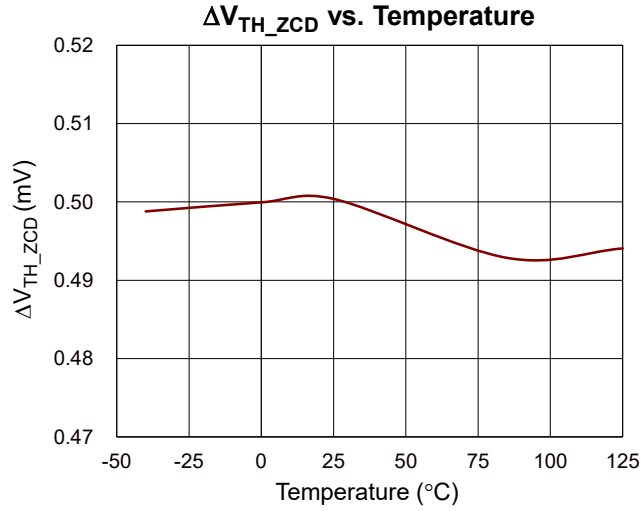

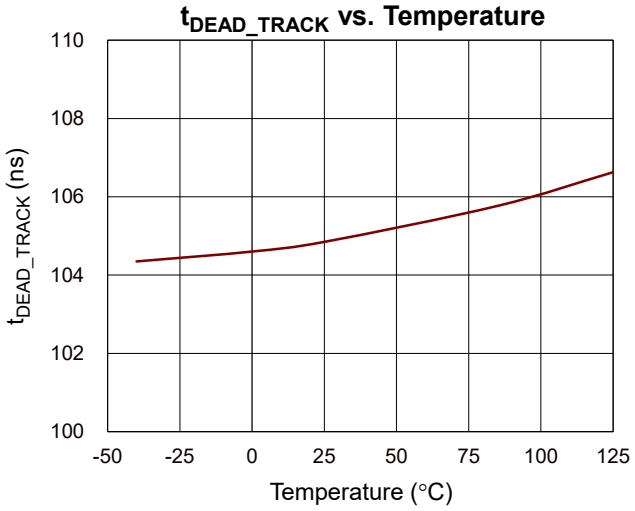

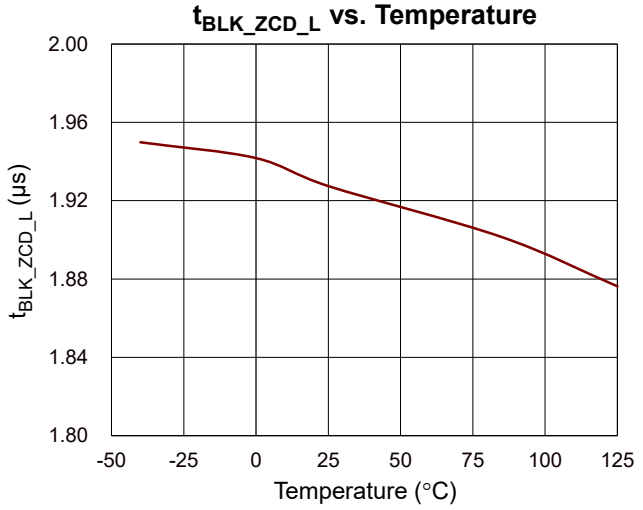

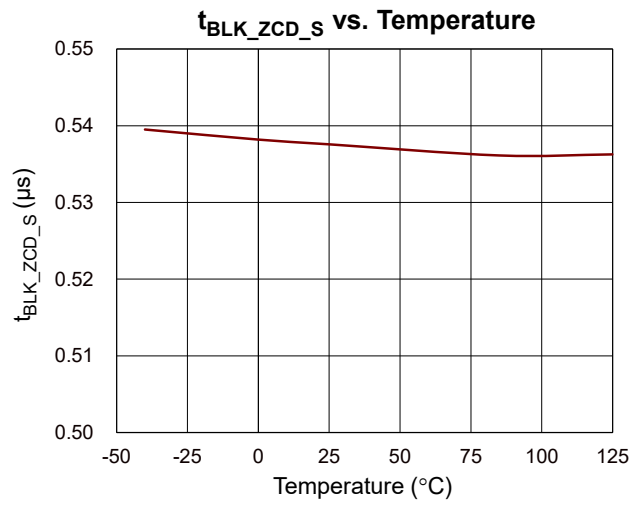

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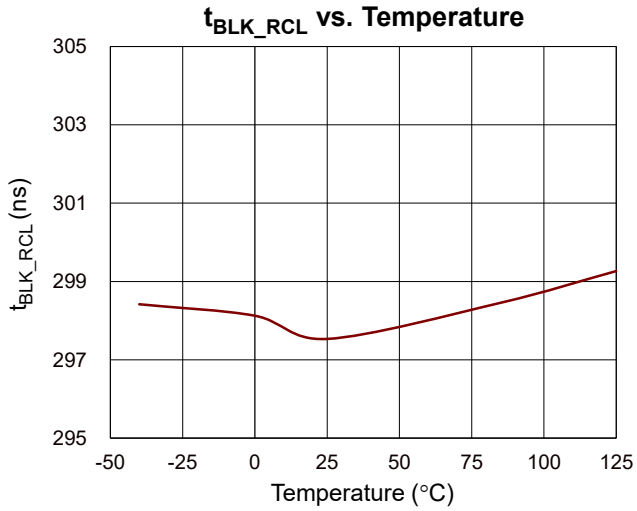

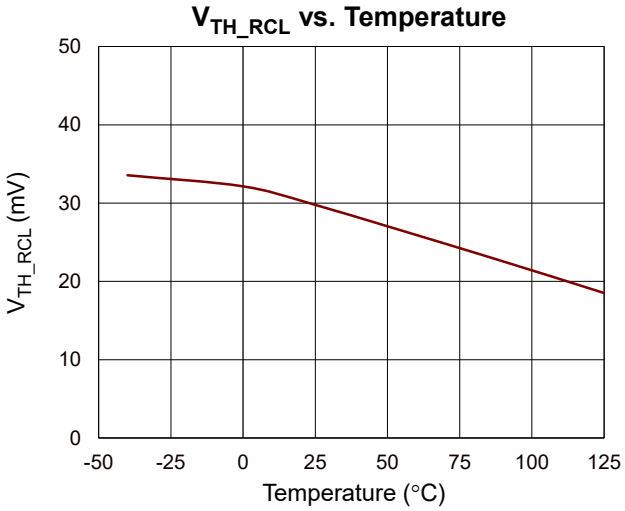

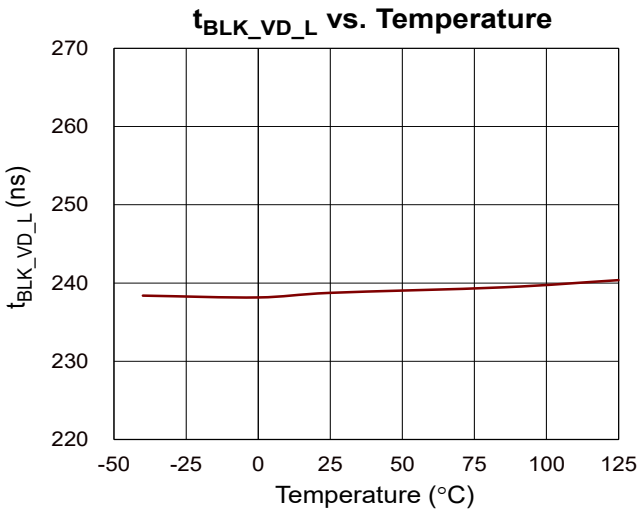

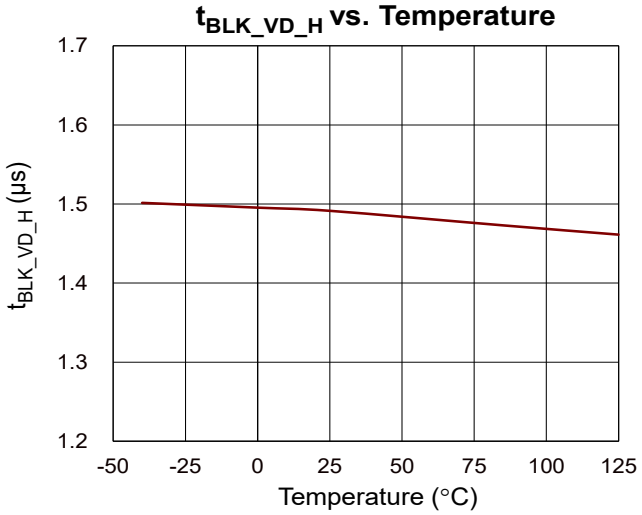

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16 Operation

The RT7220E is a secondary-side synchronous rectifier controller for AHB converters operating in CRM, CSM and BM modes. The RT7220E senses the MOSFET drain voltage to determine VG turn-on/off and modulates VG pulse width cycle-by-cycle to minimize turn-off dead time, and thereby optimizing efficiency.

16.1 Power Structure

The VDD pin supplies power for the IC and needs to be connected to the power supply output capacitor directly. The VDD pin supports a wide operating range, and the VBIAS is regulated from the LDO to supply the gate driver.

16.2 Drain Voltage Sense

The VD pin connected to the MOSFET drain pin is used to detect the VD signal as the VG turn-on/off criterion. The DC voltage is supplied from VD to VBIAS via a built-in HV LDO.

16.3 Gate Driver

The VG pin is a synchronous rectifier MOSFET driver, with power supplied from either VDD or VBIAS to ensure MOSFET can be fully turned on. In addition, the gate fast turn-off function provides reliable operation.

16.4 Source Voltage Sense

The source pin of the MOSFET is connected to the input of the source voltage sensing VS pin. To ensure correct drain-sense voltage sensing, it is strongly recommended that the sense node should be directly connected to the source of the MOSFET.

16.5 Double Pulses Function

When the power converter operates at heavy load/low output voltage, the RT7220E enables the double pulses function to optimize efficiency. The double pulses function delivers a second sine-wave energy to enhance efficiency. To enable the double pulses function, the RT7220E needs to work with the AHB converter.

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17 Application Information

(Note 7)

17.1 Power Selection

The RT7220E supports a wide output voltage range, with the VDD pin directly connected to the power output of a converter. In addition, a built-in HV LDO is used to supply the gate driver VG for the MOSFET. When VDD is less than 4.5V, the VG voltage powered by VBIAS will be clamped at 4.7V. When VDD is greater than 4.7V, the VG voltage will be proportional to VDD. Once VDD is greater than VBIAS, the VG voltage will be clamped at VBIAS to ensure fast turn-off time. The power selection circuit is shown in Figure 1.

Moreover, the RT7220E provides an initial pull-low function to prevent the gate of the SR MOSFET from being falsely turned on by the parasitic capacitance during start-up.

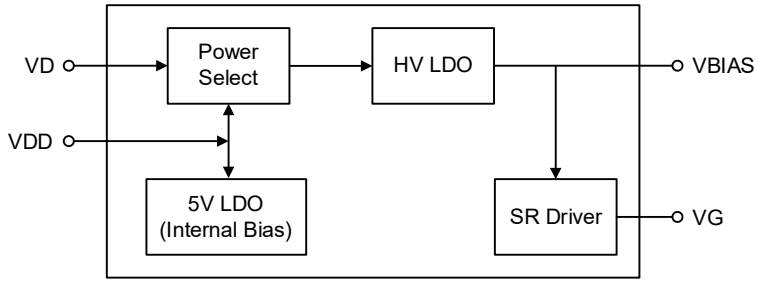

Figure 1. Power Selection Circuit

17.2 VG Turn-On

As shown in Figure 2, when the VD voltage is larger than V_{TH_VDM} and $V_{TH_SH_R}$, and after t_{DB_VDSH} and t_{TH_SRON}, if the VD falling time (from $K_{TH_VDH_F}$ x V_{VD_SH} to $V_{TH_VDL_F}$) < t_{VD_FALL}, VG will be triggered immediately at the end of $t_{DB_DON_NM}$.

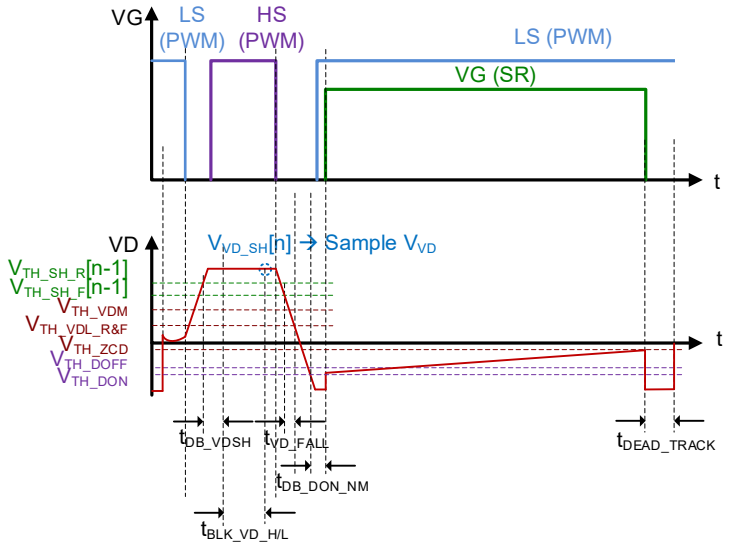

Figure 2. SR Turn-On/Off

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17.3 VG Turn-Off

As shown in Figure 2, VG will be turned off as the VD voltage rises to V_{TH_ZCD}. The RT7220E modulates and optimizes the turn-off dead-time t_{DEAD_TRACK} cycle-by-cycle to ensure reliable and high-efficiency operation. For the corrected dead-time modulation, the turn-off delay time of the MOSFET t_{OFF_DELAY}, as shown in Figure 3, should be smaller than t_{F_VG}.

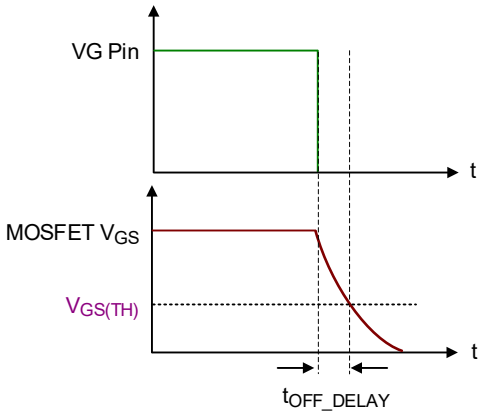

Figure 3. VG Turn-Off Delay Time

17.4 VG Minimum On-Time

The RT7220E provides the minimum on-time function to prevent incorrect turn-off due to ringing or voltage spike. When reverse current occurs in the secondary SR MOSFET from drain to source, VD will reach V_{TH_RCL}, causing VG to turn off immediately. The VG turn-off threshold is blanked during t_{BLK_ZCD}, unless VD reaches V_{TH_RCL}, as shown in Figure 4.

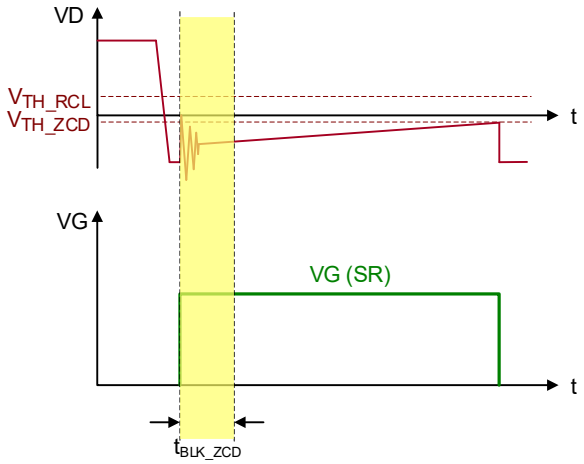

Figure 4. VG Minimum On-Time

17.5 Green Mode Operation

To improve efficiency under light load conditions, the RT7220E features a green mode operation that disables the SR MOSFET and reduces the device's operating current. Green mode is determined by detecting the number of VD and VG pulses, respectively. If VG pulses are fewer than 32 cycles within the period of t_{MCD}, the RT7220E disables the VG output and enters green mode, as shown in Figure 5.

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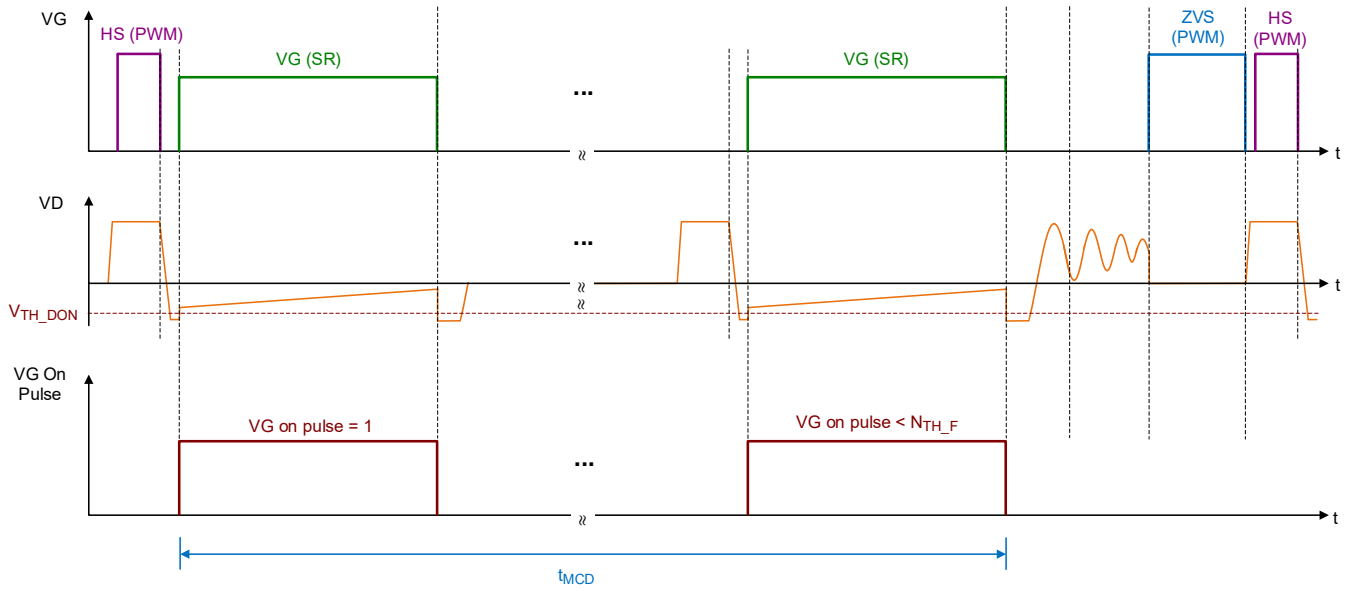

Figure 5. Enter Green Mode

Once Diode_on pulses are greater than 64 cycles within the period of t_{MCD}, the RT7220E exits green mode and resumes normal operation immediately, as shown in Figure 6.

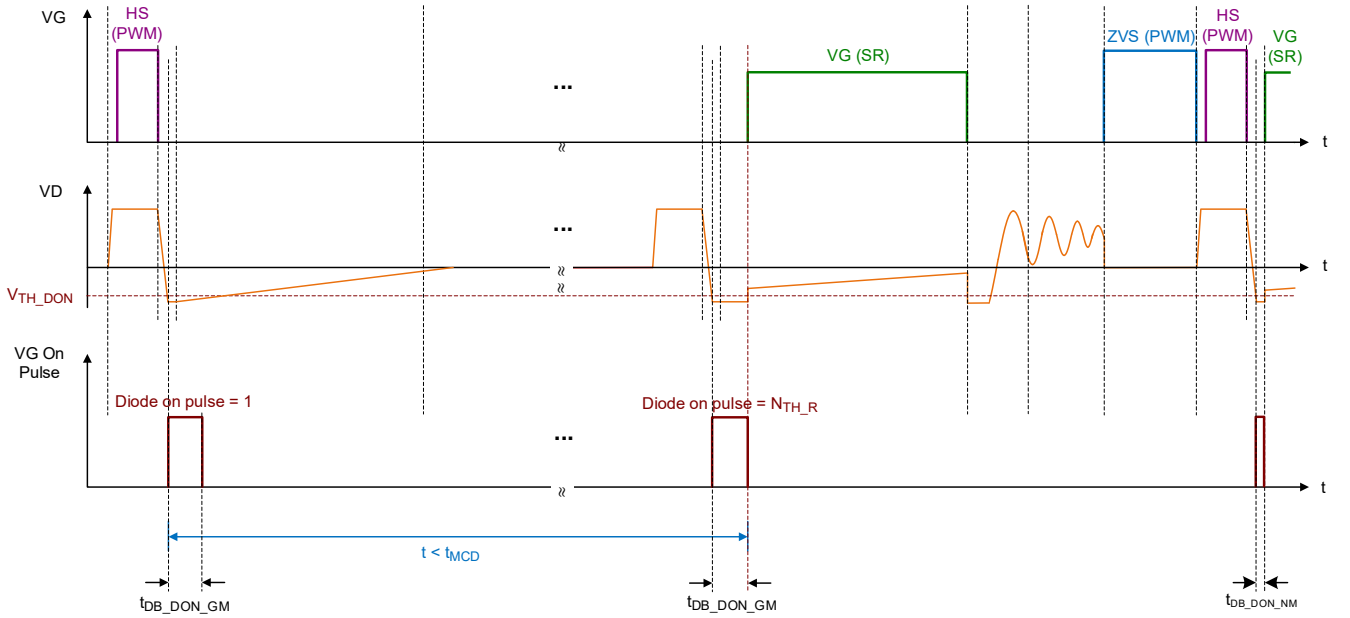

Figure 6. Exit Green Mode

17.6 Output Voltage Sense for VD Blanking Time

For AHB converter applications, since the RT7220E GND and the power converter's GND are not the same, the VDD pin cannot sense the output voltage. Therefore, the VOS pin is used to detect the output voltage.

When VIN is low, the VD falling edge detection may be incorrect, as the C_{OSS} of PWM MOSFET is inversely proportional to the input voltage. To protect the system under this condition, the RT7220E provides a V_{IN_LOW} threshold voltage in the VD to adjust the VD blanking time.

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The VD blanking time (t_{BLK_VD}) can be determined by the following equations:

$V_{VD} < K_{VIN_LOW} \times V_{VOS} = V_{IN_LOW}$

→ t_{BLK_VD} increases from $t_{BLK_VD_L}$ to $t_{BLK_VD_H}$

17.7 VD Undervoltage Protection

To avoid mis-triggering VG during the AC OFF period, the RT7220E will disable the SR function when V_{VD} is lower than V_{TH_VDM}. Since V_{VD} is equal to V_{IN} / N_{PS}, the boundary V_{IN} of V_{VD} undervoltage protection ($V_{IN_BOUNDARY}$) can be obtained according to the following equation:

$V_{IN_BOUNDARY} = N_{PS} \times V_{TH_VDM}$

where N_{PS} is the primary to secondary turn ratio.

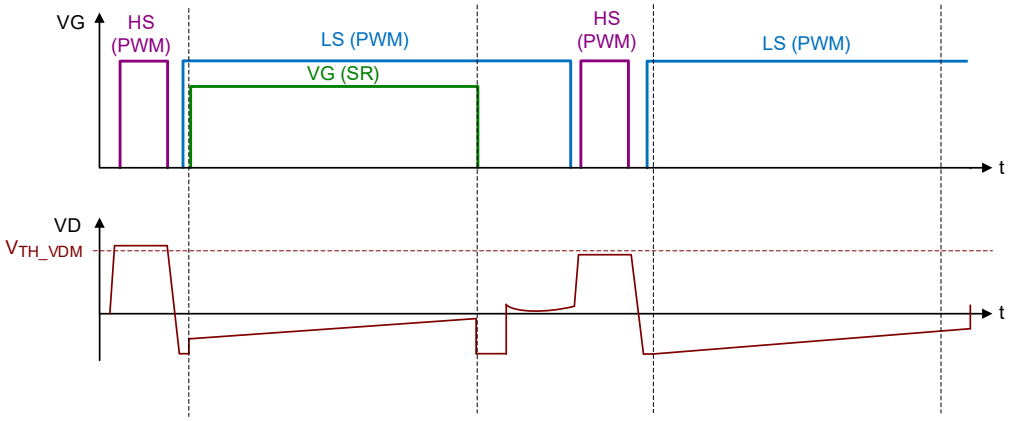

Figure 7. VD Undervoltage Protection

17.8 VG Double Pulses Function

For AHB applications, there are two sine waves in the secondary current during power delivery, especially under heavy load or low output voltage conditions. The VG double pulses function can turn on the SR MOSFET instead of the second diode when 2 sine waves appear in the secondary current.

The maximum number of VG pulses in one PWM switching period is two pulses. The second VG pulse is enabled when the present second diode's on-time is larger than $t_{ON_WIDE_DON2}$ for four consecutive pulses (debounce). The second VG pulse is disabled when the second VG's on-time is smaller than $t_{ON_WIDE_SR2}$.

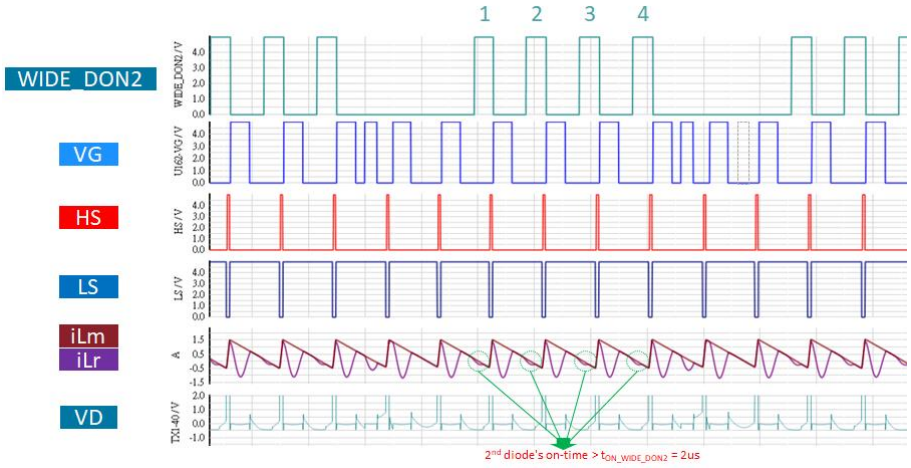

Figure 8. VG Double Pulses Function

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17.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA}, is 188°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (188°C/W) = 0.53W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} the derating curve in Figure 9 allows the designer to inspect the effect of rising ambient temperature on the maximum power dissipation.

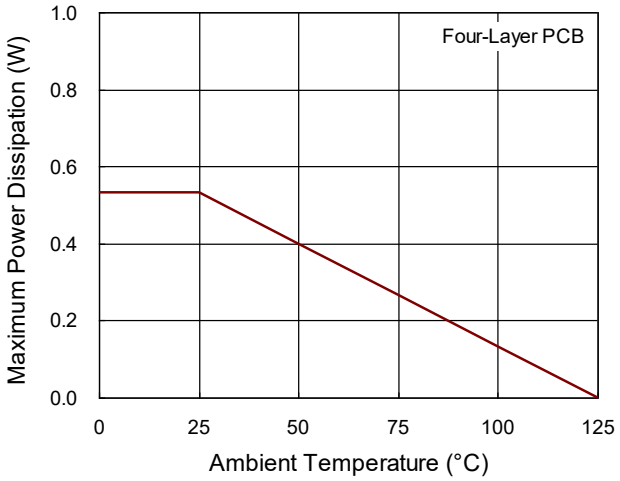

Figure 9. Derating Curve of Maximum Power Dissipation

17.10 Design Considerations and PCB Layout Guide

- The bypass capacitor of VDD and VBIAS should be as close as possible to the RT7220E. It is recommended to use a low ESR MLCC capacitor of 1μF or more to reduce ripple, as shown in Figure 10.
- A resistor between the VD pin and the drain of the SR MOSFET is necessary. It is recommended to use a 47Ω resistor with a package size larger than 0603.
- To avoid IR voltage drop affecting the output voltage detection, the VDD pin must be connected to the output capacitor independently.
- To detect VD accurately, the VS, GND and PGND pins must be connected to the source of the SR MOSFET independently.
- The SR MOSFET drive loop should be as short as possible to reduce EMI.

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- Keep the IC out of the power loop to prevent abnormal operation due to noise coupling. For a four-layer PCB layout, the power loop should not pass through the 2nd and 3rd PCB layers under the RT7220E chip.

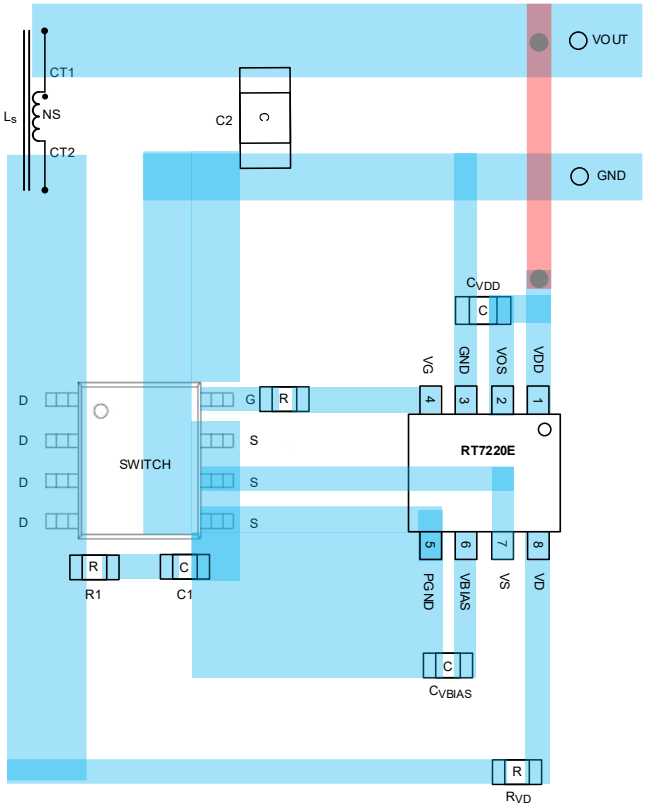

Figure 10. Design PCB Layout

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

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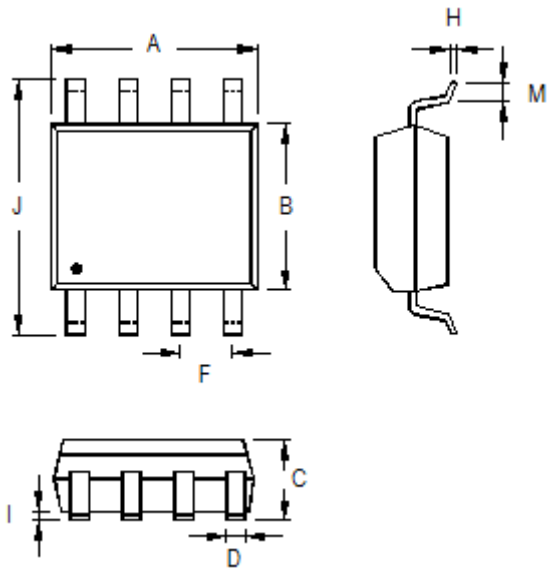
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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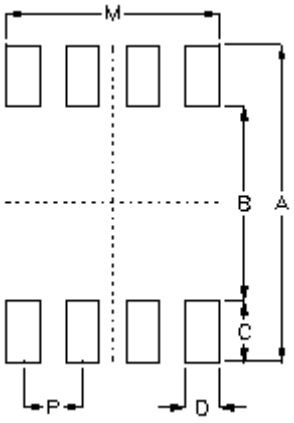
19 Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8/SOP-8(FC)	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

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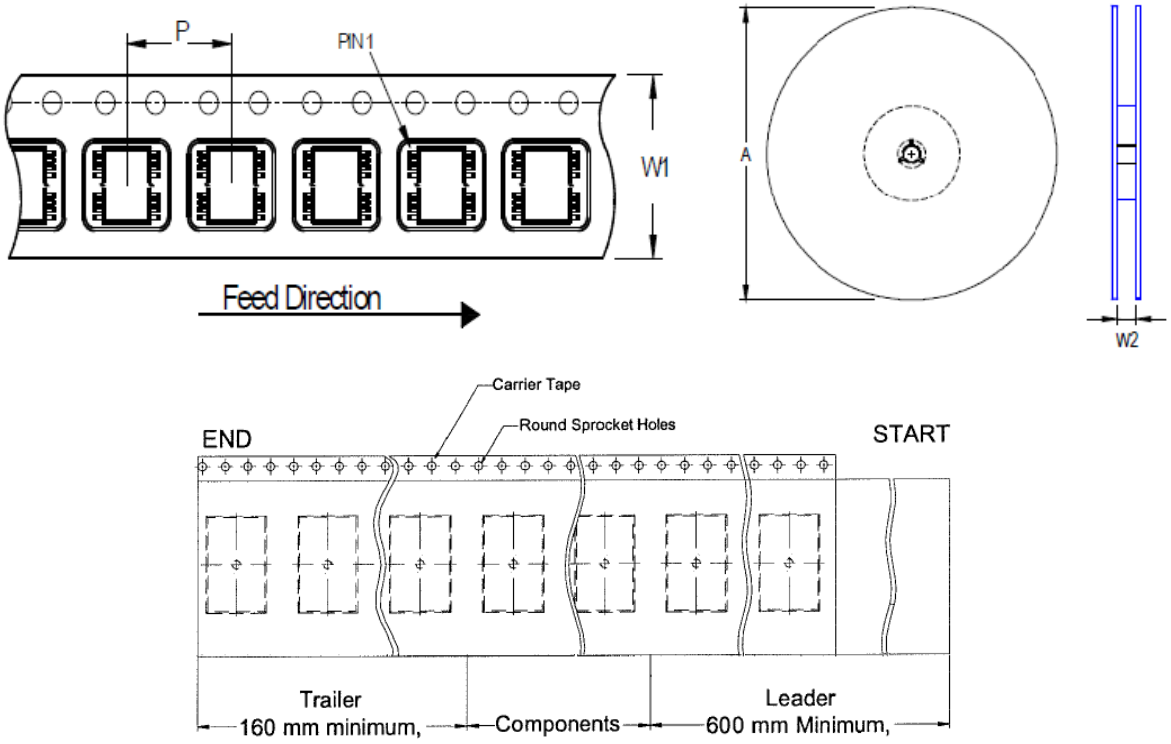
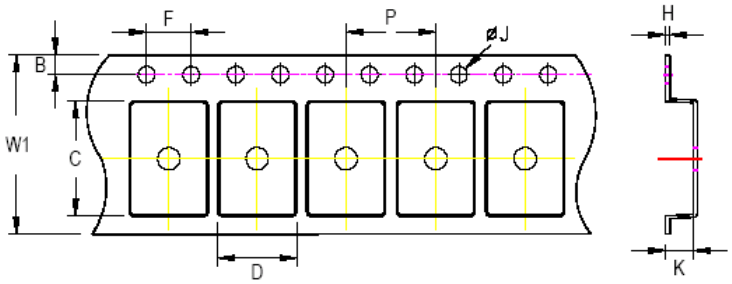
20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
SOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.2mm	0.6mm

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20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 13”	4	1 reel per inner box **Box G**
2	HIC & Desiccant (2 Unit) inside	5	6 inner boxes per outer box
3	Caution label is on backside of Al bag	6	Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

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20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/23	Final	Typical Operating Characteristics on P10 to 16
01	2024/11/14	Modify	*Marking Information on page 2* - Updated marking information *RT7220E Version Table on page 2* - Added RT7220ES-EDAA, RT7220ES-SDAA, and RT7220ES-EEAA *Packing Information on page 26* - Updated packing information
02	2025/4/17	Modify (Removed RT7220ES-EDAA)	*Features on page 1* - Modified protection *Marking Information page 2* - Removed RT7220ES-EDAA *RT7220E Version Table page 2* - Removed RT7220ES-EDAA *Electrical Characteristics on page 6, 7, 8, 9* - Modified the specification of V_{VBIAS}, V_{OH_VG}, V_{OL_VG}, t_{R_VG}, t_{F_VG}, t_{VD_FALL}, N_{TH_R}, $t_{DB_DON_NM}$ *Typical Application Circuit on page 10* - Updated circuit *Typical Operating Characteristics on page 11 to 16* - Modified I_{DD_GREEN}, I_{DD_ST}, V_{VBIAS}, V_{OH_VG}, t_{R_VG}, t_{F_VG}, R_{PL_SR}, $K_{TH_VDH_R}$, $K_{TH_VDH_F}$, $V_{TH_VDL_R}$, $V_{TH_VDL_F}$, t_{DEAD_TRACK}, $t_{BLK_ZCD_L}$, $t_{BLK_ZCD_S}$, t_{BLK_RCL} - Removed I_{DD_ST}, t_{MCD}, V_{REG_VD}, V_{DROP_LDO}, $t_{TH_SRON_L}$, $t_{TH_SRON_H}$, $V_{TH_TTH_SEL}$, t_{BK_DONDET} *Application Information on page 18, 20, 21* - Modified Figure 1, Figure 2, Figure 5, Figure 6, Figure 7, Section 17.6, and Section 17.7

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