RICHTEK®

RT7251A/RT7251B

17V, 1.5A, 340/800kHz Synchronous Buck Converter

1 General Description

The RT7251A/RT7251B is a high-efficiency, monolithic synchronous buck converter that can operate at 340kHz/800kHz, while delivering up to 1.5A output current from a 4V to 17V input supply. The current mode architecture of the RT7251A/RT7251B allows for optimized transient response. The cycle-by-cycle current limit provides protection against shorted outputs, and the soft-start feature eliminates input current surge during start-up. Fault conditions also include output undervoltage protection, output overvoltage protection, and over-temperature protection. The low current (<5μA) shutdown mode provides output disconnection, enabling easy power management in battery-powered systems. The RT7251A/RT7251B is available in a WDFN-8L 2x2 package.

2 Ordering Information

RT7251A/B □□

Package Type(1)
QW: WDFN-8L 2x2 (W-Type)

Lead Plating System
Z: ECO (Ecological Element with Halogen Free and Pb free)(2)

A: 340kHz
B: 800kHz

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Suitable for use in SnPb or Pb-free soldering processes.

3 Features

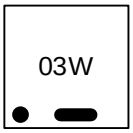
- **4V to 17V Input Voltage Range**
- **1.5A Output Current**
- **Internal N-MOSFETs**
- **Current Mode Control**
- **Power Saving Mode at Light Load**
- **Frequency Operation: 340kHz (RT7251A)/800kHz (RT7251B)**
- **Output Adjustable from 0.8V to 12V**
- **Up to 95% Efficiency**
- **Internal Compensation**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Overcurrent Protection**
- **Input Undervoltage-Lockout**
- **Output Undervoltage Protection**
- **Output Overvoltage Protection**
- **Power-Good Indicator**
- **Over-Temperature Protection**

4 Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

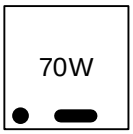
5 Marking Information

RT7251AZQW



03 : Product Code
W : Date Code

RT7251BZQW



70 : Product Code
W : Date Code

6 Simplified Application Circuit

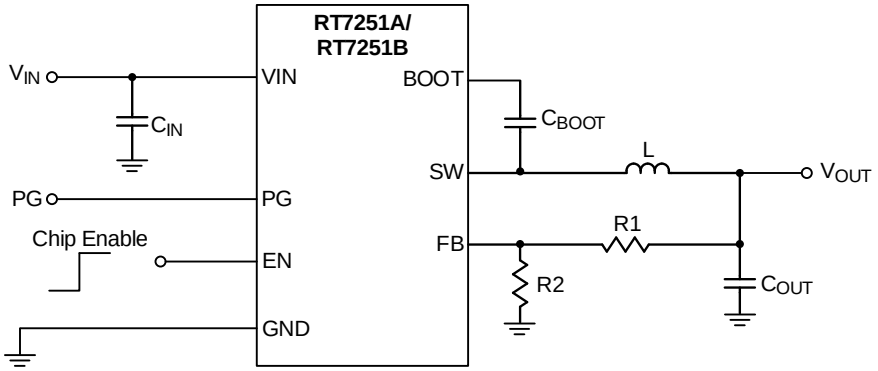
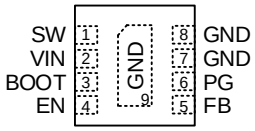


Table of Contents

7 Pin Configuration

(TOP VIEW)

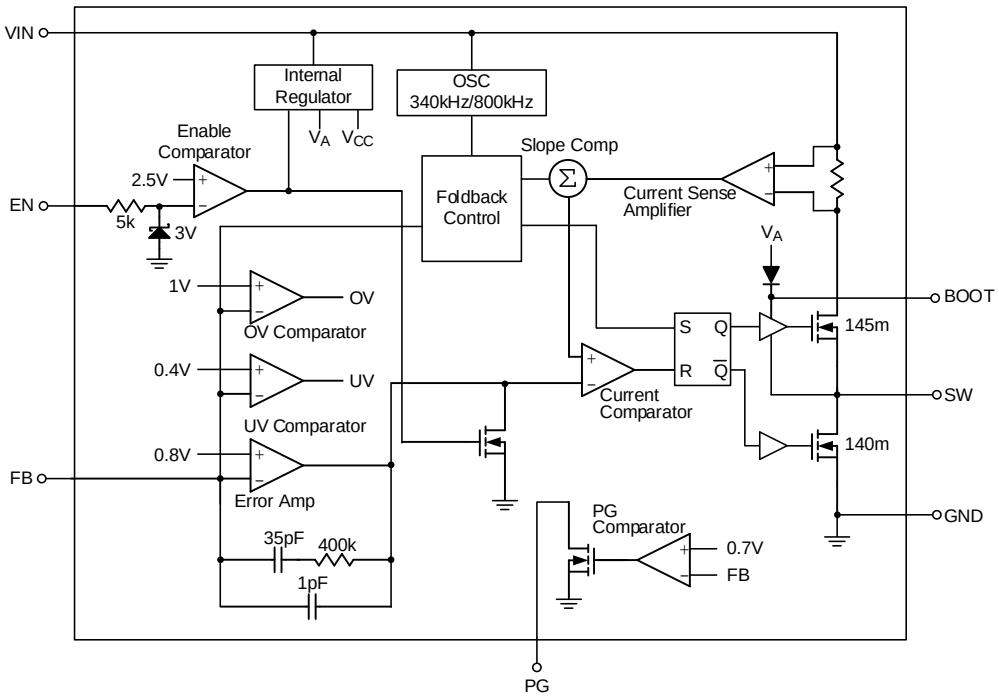


WDFN-8L 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. The output switching state between the high-side MOSFET and the low-side MOSFET of the power converter. Connect the SW pin to the external inductor and the bootstrap capacitor.
2	VIN	Power input voltage. Support 4V to 17V input voltage. It is suggested to place decoupling input capacitors as close to the VIN and GND pins as possible.
3	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.01μF ceramic capacitor between this pin and SW pin.
4	EN	Chip enable. A logic-high enables the converter; a logic-low forces the RT7251A/RT7251B into shutdown mode, reducing the supply current to less than 5μA. Attach this pin to VIN with a 100kΩ pull-up resistor for automatic startup.
5	FB	Feedback voltage input. The pin is used to set the output voltage of the converter via a resistor divider. It is suggested to place the FB resistor divider as close to the FB pin as possible.
6	PG	Power-good indicator. The output of this pin is low if the output voltage is 12.5% less than the nominal voltage. Otherwise, it is an open-drain.
7, 8, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 19.3V
- VIN to SW ---------- –0.3V to 19.3V
- VIN to SW (t ≤ 10ns) ---------- –3V to 25V
- SW ---------- –1.5V to 19.3V
- SW (t ≤ 10ns) ---------- –5V to 25V
- BOOT to SW ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-8L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 3)

  WDFN-8L 2x2, θ_{JA} ---------- 120°C/W

  WDFN-8L 2x2, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 4V to 17V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	1	5	μA
Supply Current	I_Q	V_{EN} = 3V, V_{FB} = 0.9V	--	0.6	1	mA
Feedback Voltage	V_{FB}	4V ≤ V_{IN} ≤ 17V	0.788	0.8	0.812	V
FB Pin Current	I_{FB}	V_{FB} = 0.8V	--	10	--	nA
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	145	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	140	--	mΩ
High-Side Switch Current Limit	I_{LIM_H}	Min. duty cycle, V_{BOOT} – V_{SW} = 4.8V maximum loading = 1.5A	--	3	--	A
Low-Side Switch Current Limit	I_{LIM_L}	From drain to source	--	1	--	A
Oscillation Frequency	f_{OSC1}	For RT7251A	300	340	380	kHz
		For RT7251B	700	800	900	
Short-Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V, For RT7251A	--	95	--	kHz
		V_{FB} = 0V, For RT7251B	--	170	--	
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V, For RT7251A	--	93	--	%
		V_{FB} = 0.7V, For RT7251B	--	84	--	
Minimum On-Time	t_{ON}		--	100	--	ns
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}		--	3.5	--	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	200	--	mV
EN Input Voltage Rising Threshold	V_{EN_R}		2.7	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	
EN Pull Low Current		V_{EN} = 2V, V_{FB} = 1V	--	1	--	μA
Soft-Start Time	t_{SS}		--	1	--	ms
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C
Power-Good Voltage Threshold	V_{PG}		--	0.7	--	V
Power-Good Voltage Hysteresis	V_{PG_HYS}		--	130	--	mV
Power-Good Pull Down Resistance			--	12	--	Ω
Output Overvoltage Rising Threshold	V_{OVP_R}		--	125	--	%V_{REF}
Output OVP Propagation Delay			--	10	--	μs

13 Typical Application Circuit

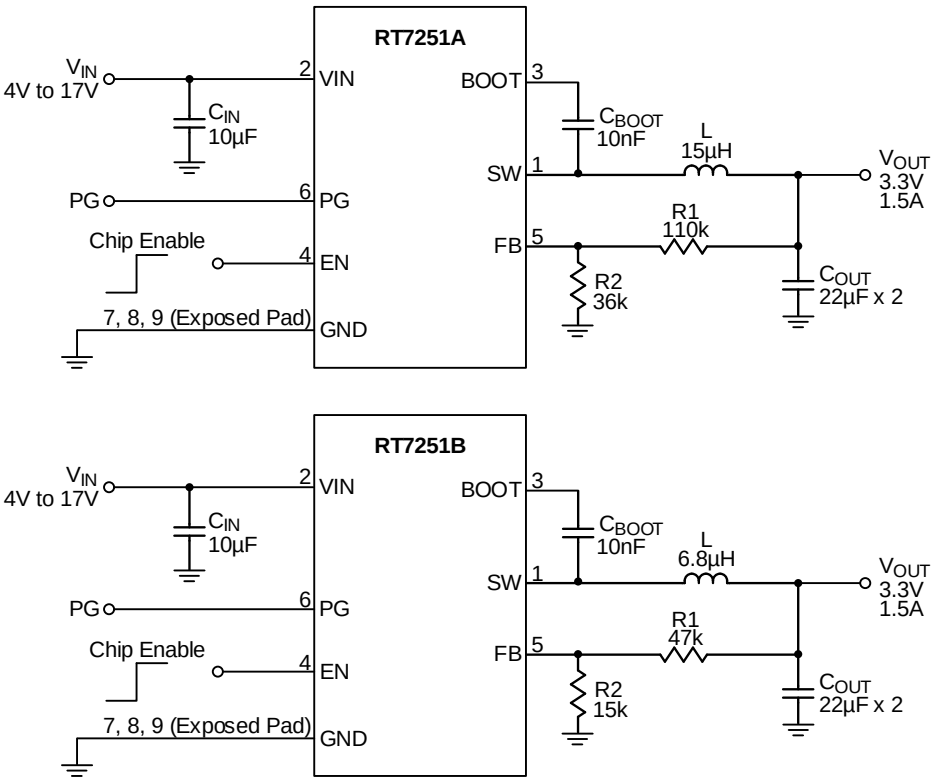


Table 1. Recommended Component Selection

RT7251A

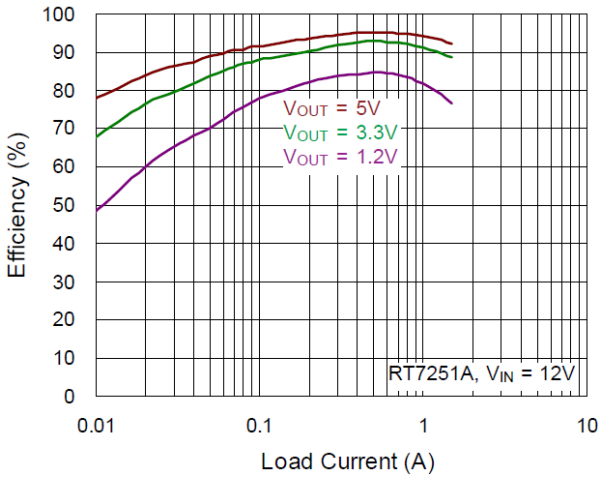
VOUT (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	COUT (µF)
1.2	4.7	110	220	22 x 2
2.5	10	110	51	22 x 2
3.3	15	110	36	22 x 2
5	22	120	22	22 x 2

RT7251B

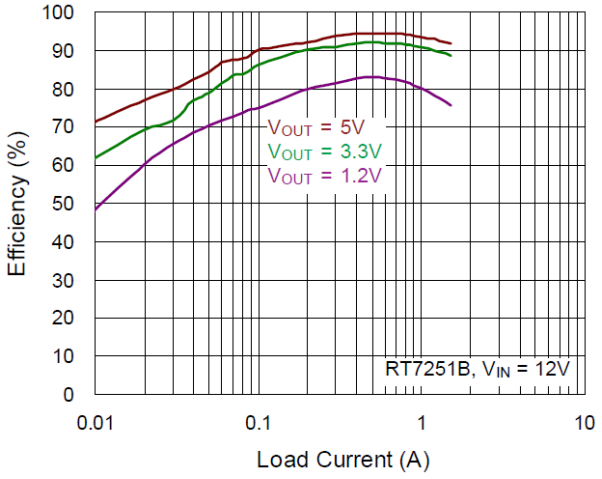
VOUT (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	COUT (µF)
1.2	3.6	47	91	22 x 2
2.5	4.7	47	22	22 x 2
3.3	6.8	47	15	22 x 2
5	10	62	12	22 x 2

14 Typical Operating Characteristics

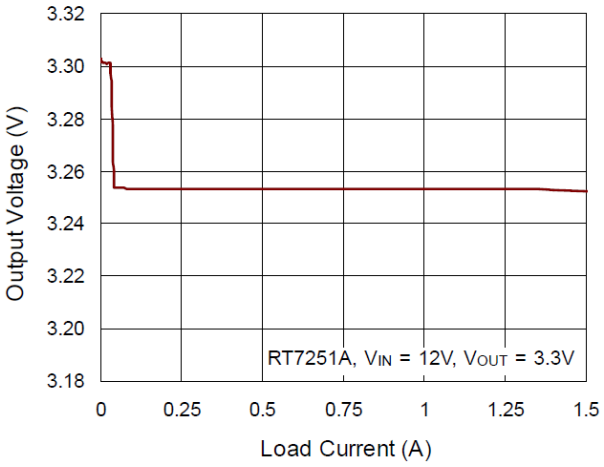
Efficiency vs. Load Current



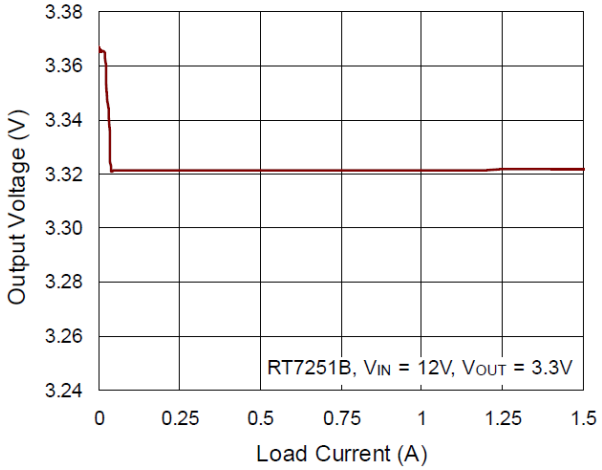
Efficiency vs. Load Current



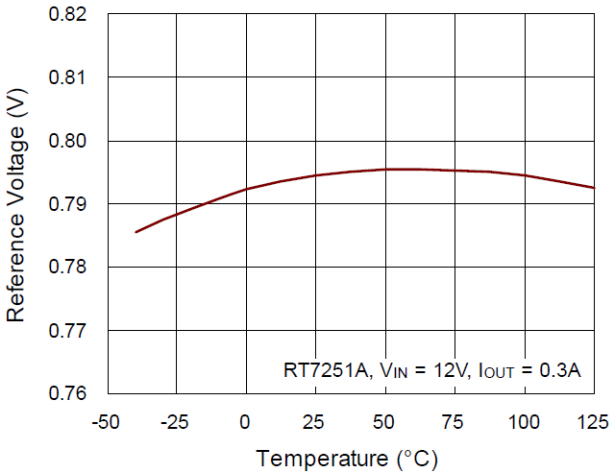
Output Voltage vs. Load Current



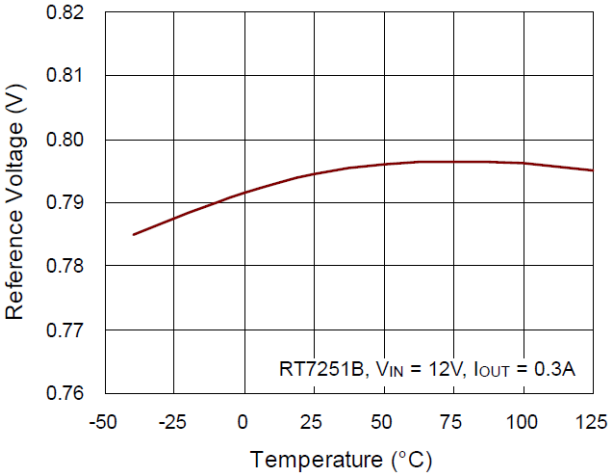
Output Voltage vs. Load Current



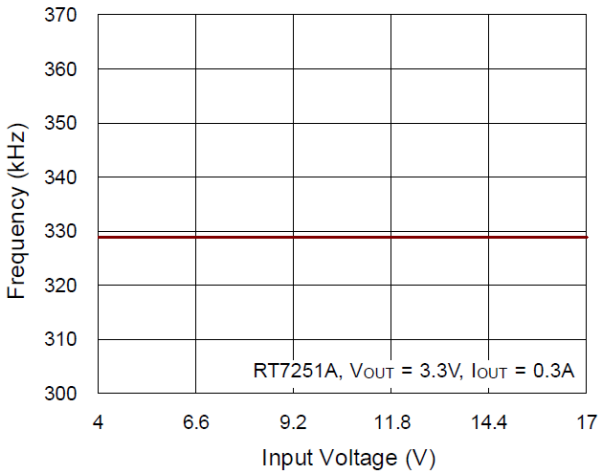
Reference Voltage vs. Temperature



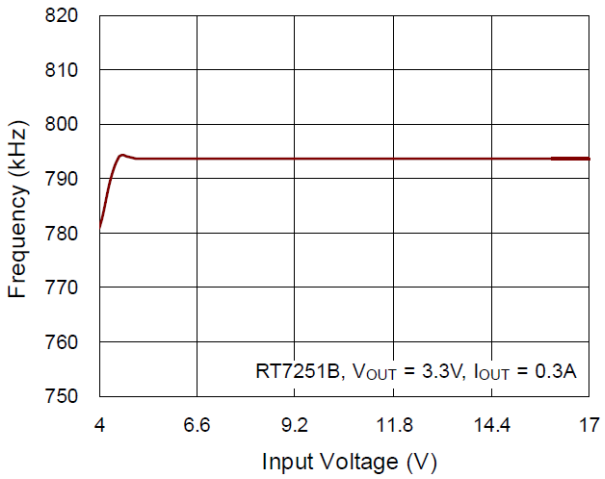
Reference Voltage vs. Temperature



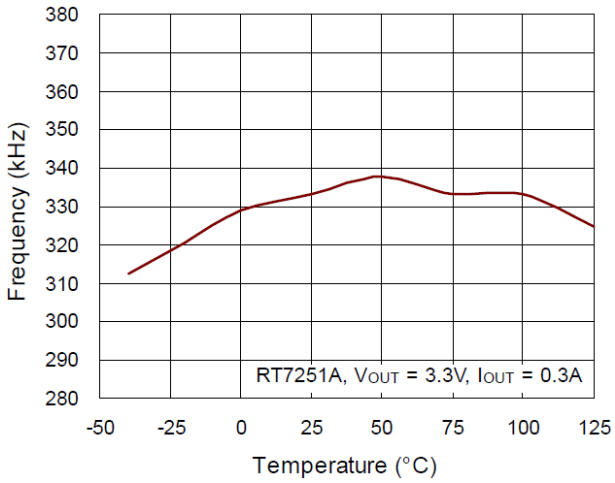
Frequency vs. Input Voltage



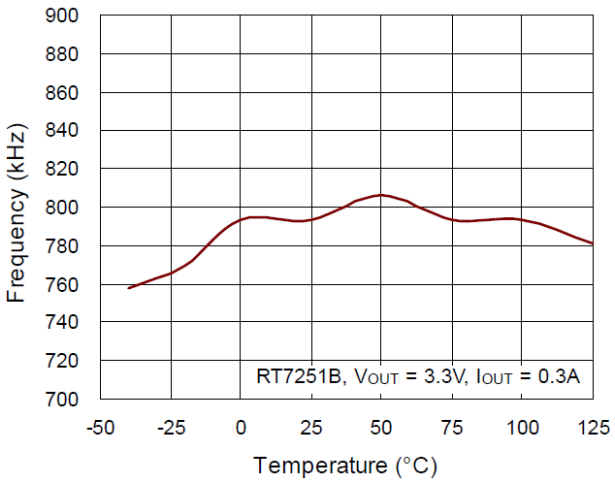
Frequency vs. Input Voltage



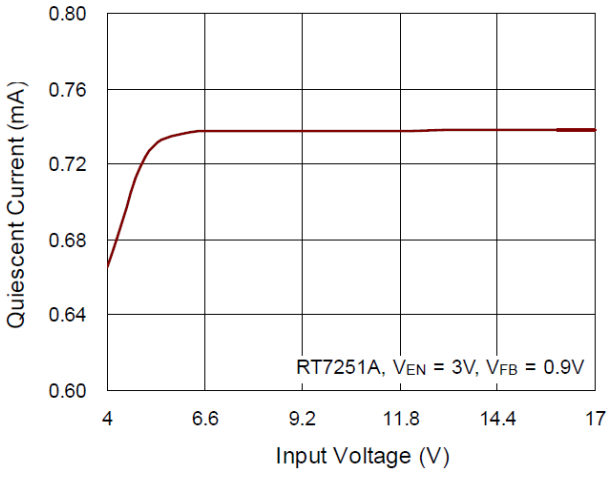
Frequency vs. Temperature



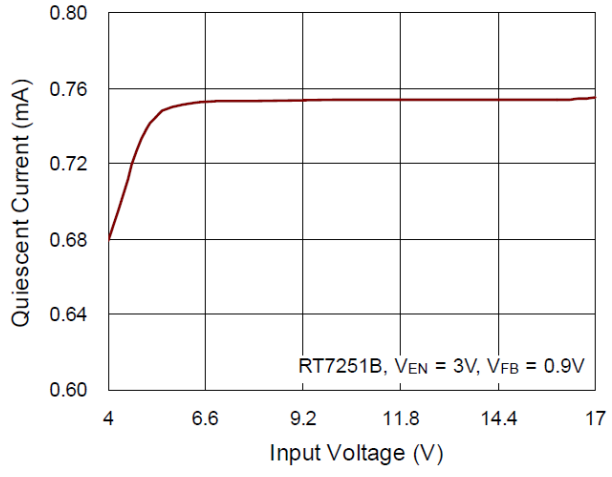
Frequency vs. Temperature

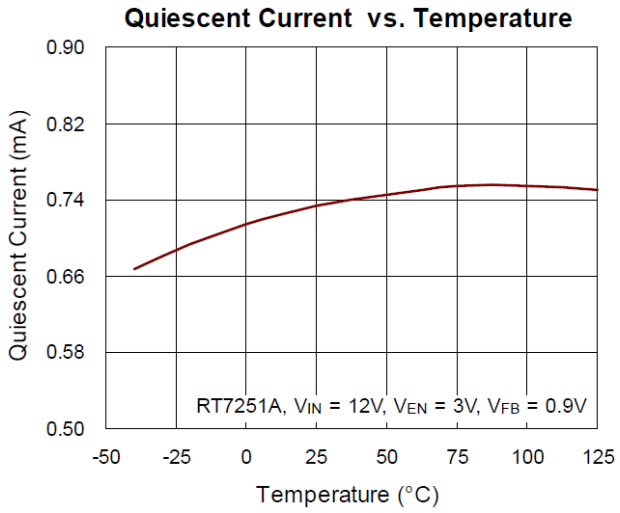


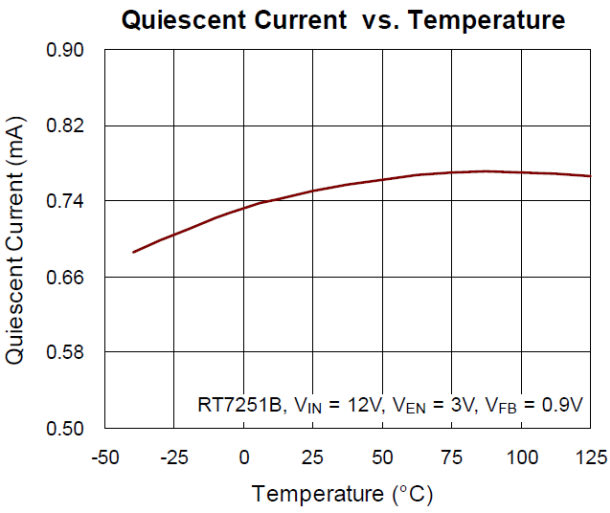
Quiescent Current vs. Input Voltage

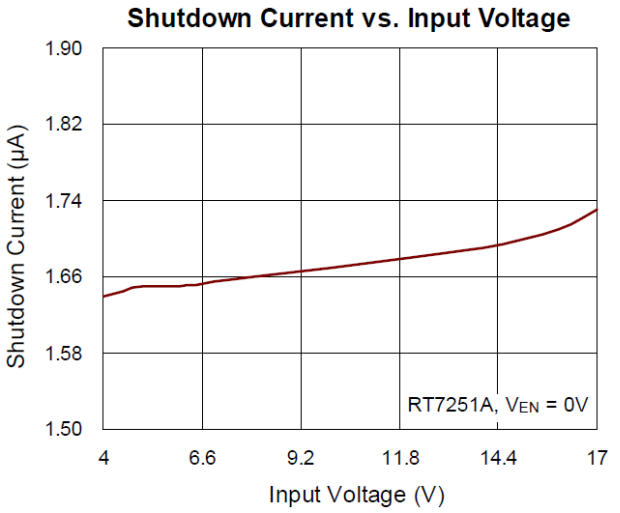


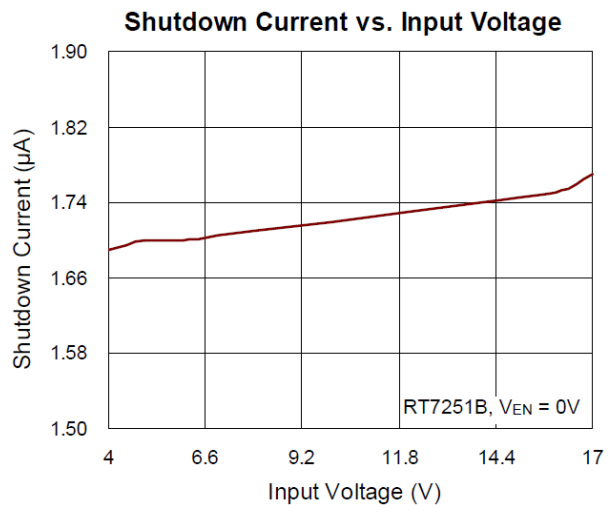
Quiescent Current vs. Input Voltage

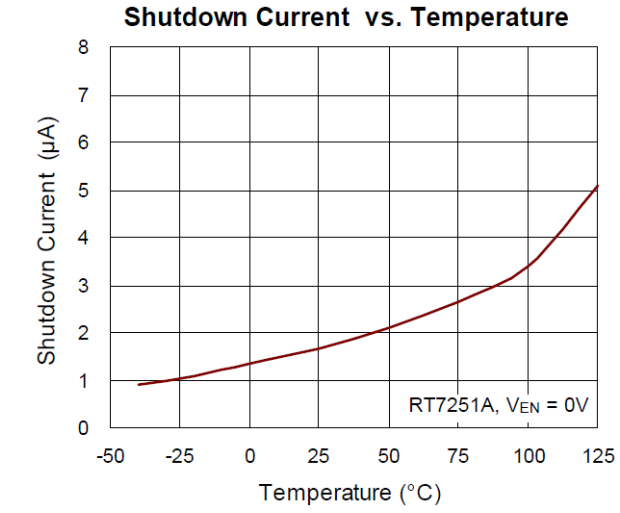


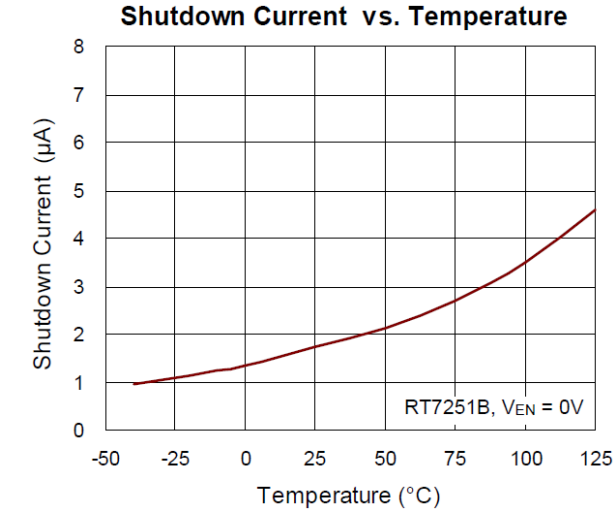




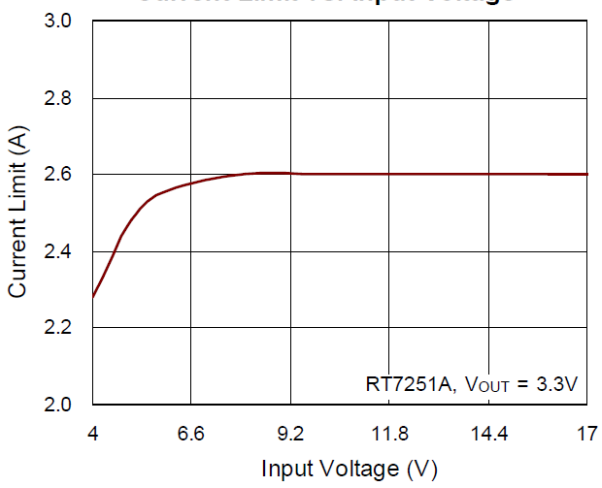




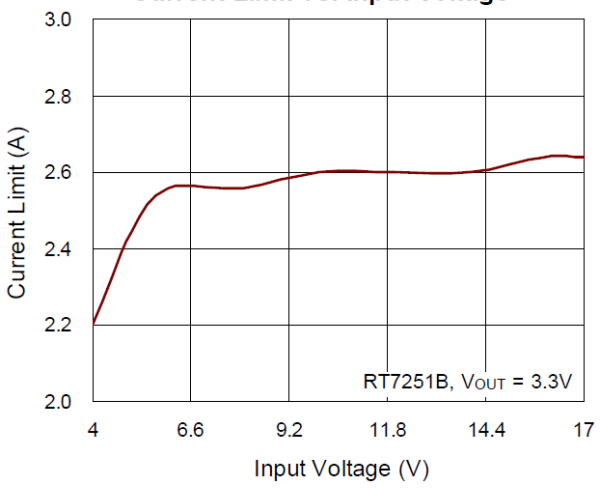




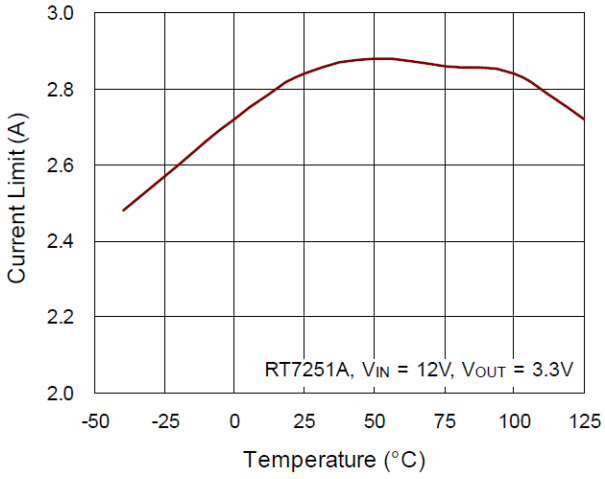
Current Limit vs. Input Voltage



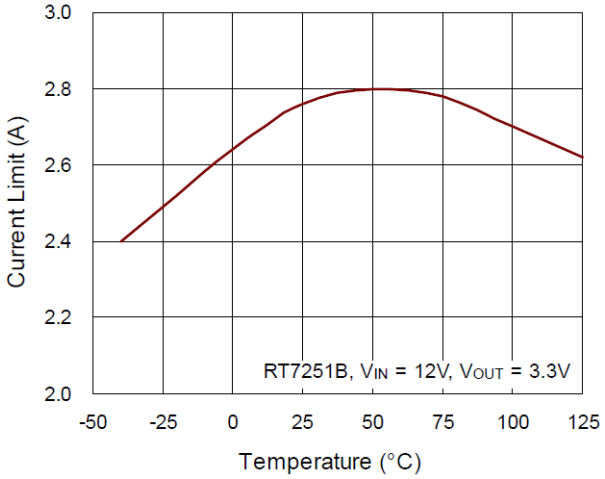
Current Limit vs. Input Voltage



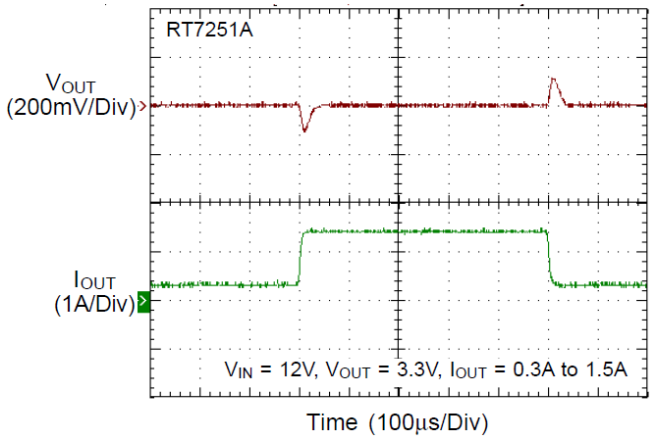
Current Limit vs. Temperature



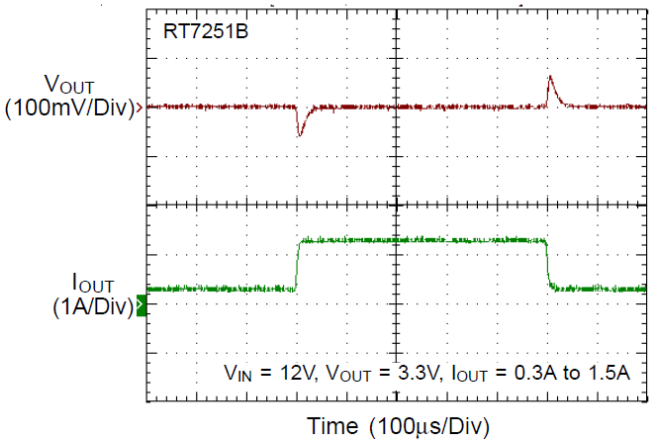
Current Limit vs. Temperature



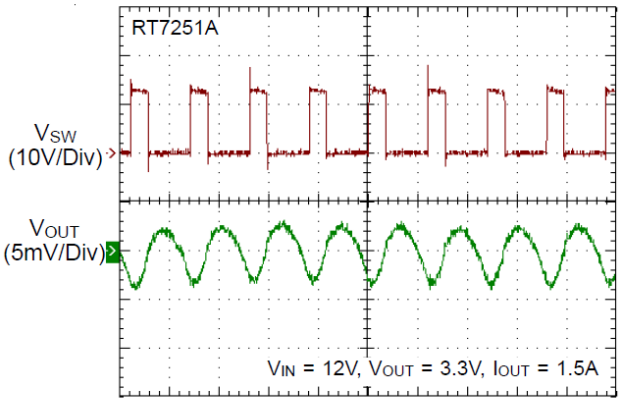
Load Transient Response



Load Transient Response

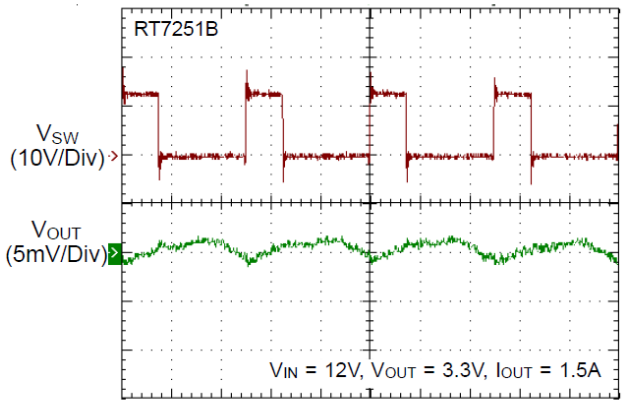


Switching



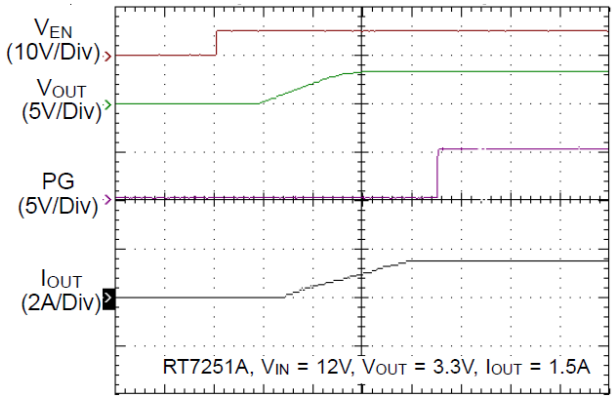
Time (2.5µs/Div)

Switching



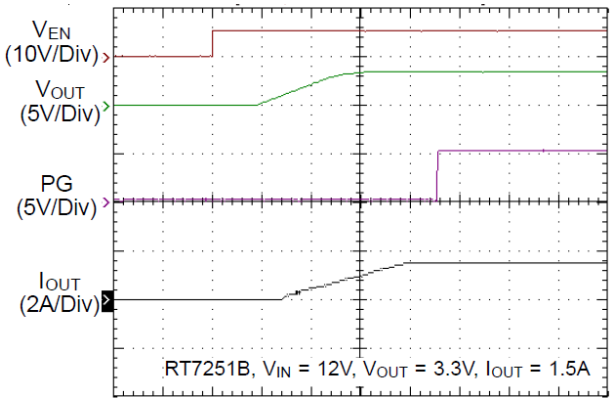
Time (500ns/Div)

Power On from EN



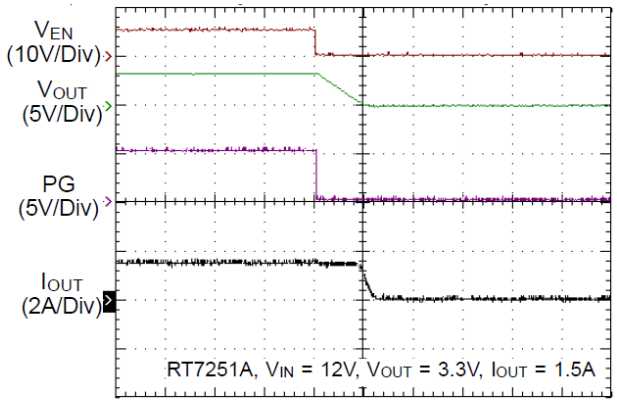
Time (500µs/Div)

Power On from EN



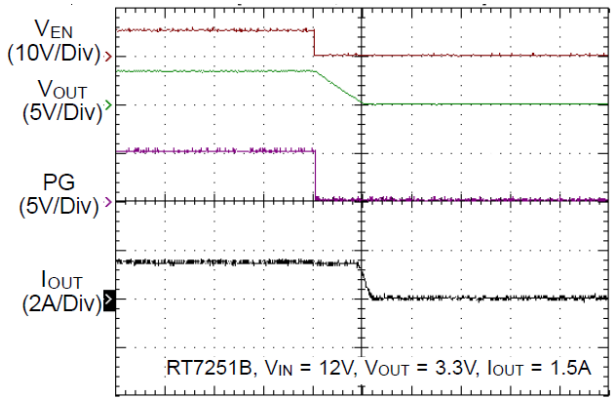
Time (500µs/Div)

Power Off from EN



Time (100µs/Div)

Power Off from EN



Time (100µs/Div)

15 Application Information

(Note 6)

The RT7251A/RT7251B is a synchronous high-voltage buck converter that supports an input voltage range from 4V to 17V, and an output current of up to 1.5A.

15.1 Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage, as shown in Figure 1.

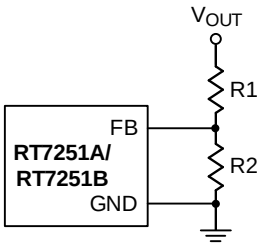


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation:

$$V_{FB} = (1 + \frac{R1}{R2})$$

where V_{FB} is the feedback voltage (0.8V typical).

15.2 External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and the SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. It is recommended to add an external bootstrap diode between an external 5V supply and the BOOT pin for efficiency improvement when the input voltage is lower than 5.5V, or the duty ratio is higher than 65%. The bootstrap diode can be a low-cost one such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from the system or a 5V output of the RT7251A/RT7251B. Note that the external boot voltage must be lower than 5.5V.

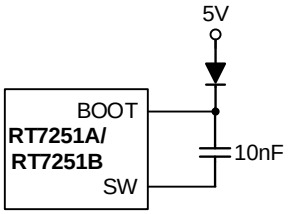


Figure 2. External Bootstrap Diode

15.3 Overvoltage Protection (OVP)

The RT7251A/RT7251B provides overvoltage protection when the output voltage exceeds 125%. The internal MOSFET will be turned off. The control will return to normal operation once the overvoltage condition is removed.

15.4 Undervoltage Protection (UVP)

The RT7251A/RT7251B provides Hiccup Mode Undervoltage Protection (UVP). When the FB voltage drops below 50% of the feedback voltage, the UVP function will be triggered, causing the RT7251A/RT7251B to shut down for a period of time and then recover automatically. The Hiccup Mode UVP can reduce input current in short-circuit conditions.

15.5 Inductor Selection

The inductor value and operating frequency determine the ripple current according to specific input and output voltages. The ripple current (ΔI_L) increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = [\frac{V_{OUT}}{f \times L}] \times [1 - \frac{V_{OUT}}{V_{IN}}]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For ripple current selection, a value of $\Delta I_L = 0.2 \times I_{MAX}$ is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}] \times [1 - \frac{V_{OUT}}{V_{IN(MAX)}}]$$

The selection of the inductor can refer to Table 2.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

15.6 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor with a higher temperature rating than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10μF low ESR ceramic capacitor is recommended. For the recommended capacitor, refer to Table 3 for more details. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response, as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \times [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR values. However, they provide lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use

types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, they can be used in cost-sensitive applications for ripple current rating and long-term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors, combined with trace inductance, can also lead to significant ringing.

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken for loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	MURATA	GRM31CR61E106K	10	1206
C_{IN}	TDK	C3225X5R1E106K	10	1206
C_{IN}	TAIYO YUDEN	TMK316BJ106ML	10	1206
C_{OUT}	MURATA	GRM32ER61E226M	22	1210
C_{OUT}	MURATA	GRM21BR60J226M	22	0805
C_{OUT}	TDK	C3225X5R0J226M	22	1210
C_{OUT}	TAIYO YUDEN	EMK325BJ226MM	22	1210

15.7 Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}(ESR). This also begins to charge or discharge C_{OUT}, generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that will indicate a stability problem.

15.8 Thermal Considerations

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and the difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is layout dependent. For the WDFN-8L 2x2 package, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A =25ºC can be calculated by the following formula:

$P_{D(MAX)} = (125°C - 25°C) / (120°C/W) = 0.833W$ for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for a fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

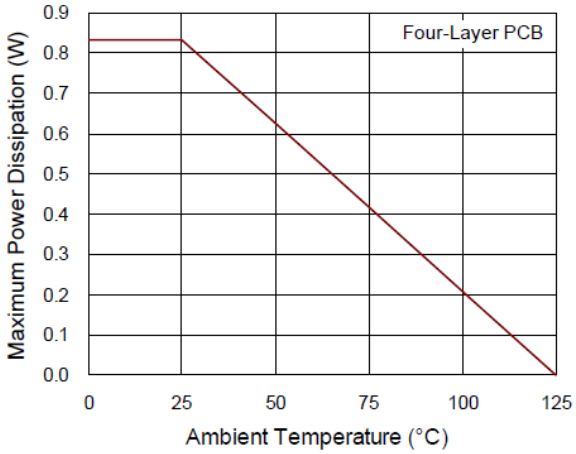


Figure 3. Derating Curve of Maximum Power Dissipation

15.9 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT7251A/RT7251B.

- Keep the traces of the main current paths as short and wide as possible.
- Place the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- Place the feedback components as close as possible to the FB pin.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

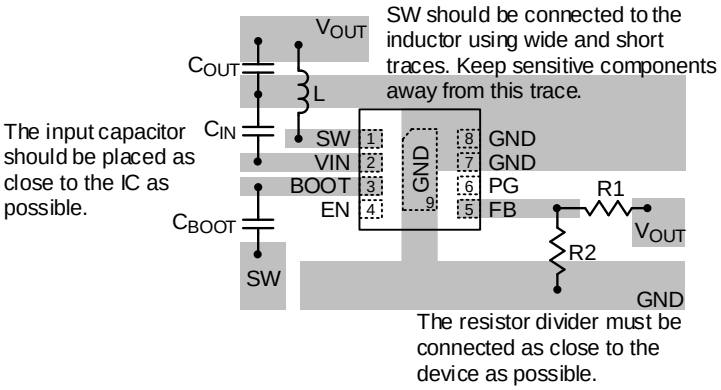
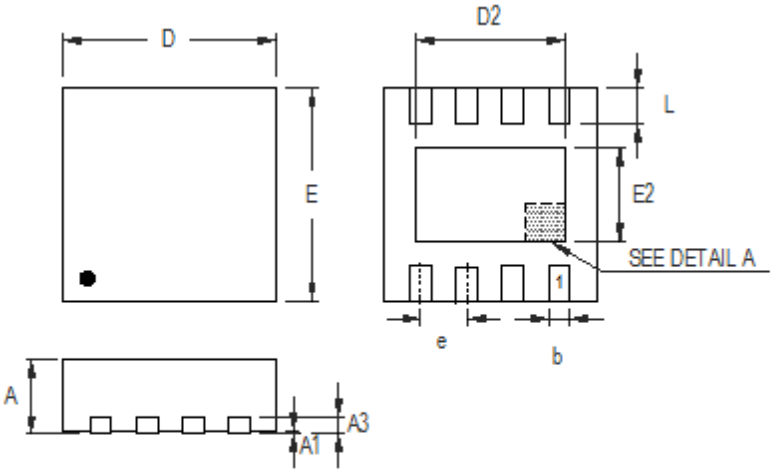
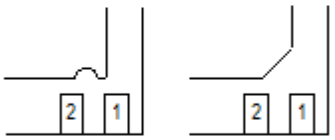


Figure 4. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

16 Outline Dimension





DETAIL A

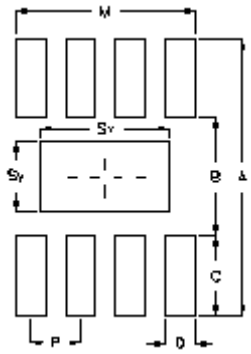
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

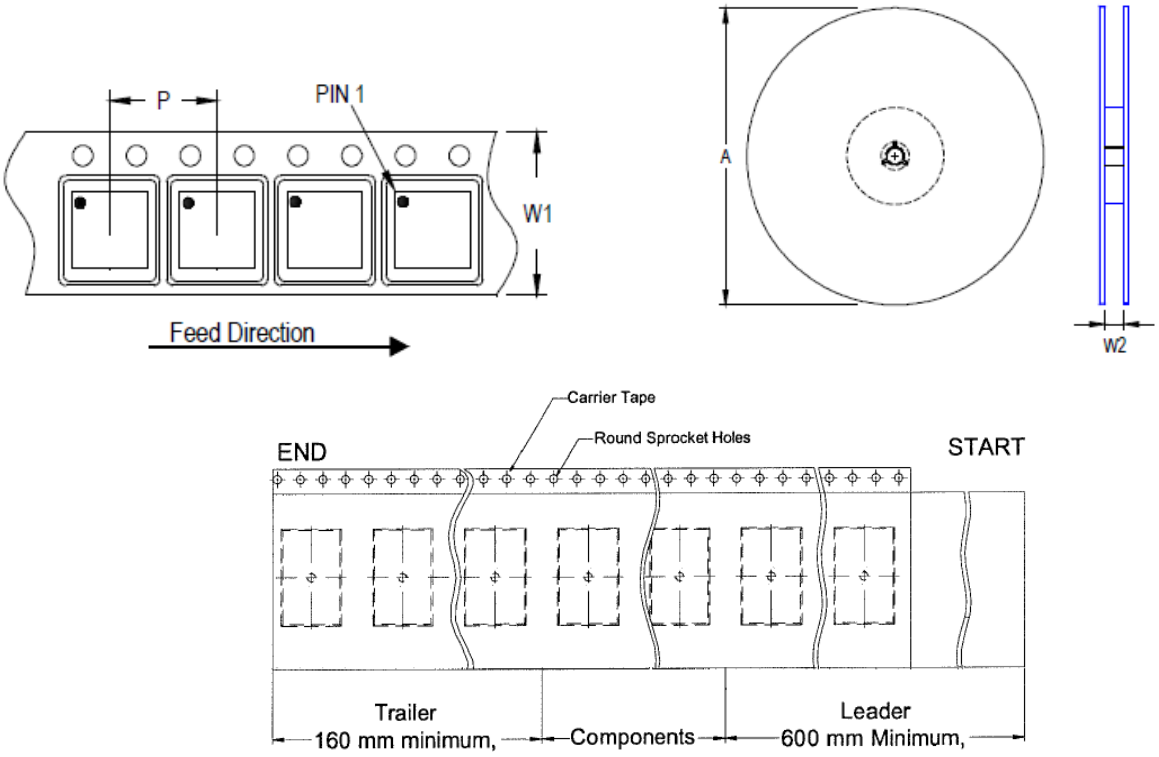
17 Footprint Information



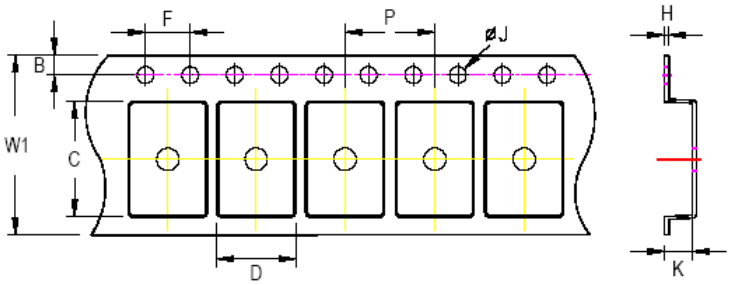
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05

18 Packing Information

18.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

19 Datasheet Revision History

Version	Date	Description	Item
00	2011/11/13	Final	
01	2012/04/13	Modify	*Application Information on page 11*
02	2018/06/05	Modify	*Electrical Characteristics on page 5*
03	2022/03/17	Modify	*Absolute Maximum Ratings on page 4*
04	2023/4/20	Modify	*Application Information on page 11 Datasheet Revision History on page 16*
05	2025/3/4	Modify	*Changed the name of pin 6 to PG.* *General Description on page 1* *Features on page 1* *Simplified Application Circuit on page 2* *Ordering Information on page 1* *Electrical Characteristics on page 6* *Footprint Information on page 19* *- Added Footprint Information* *Packing Information on page 20, 21, 22* *- Added packing information*