Primary-Side Regulation LED Driver Controller with Active-PFC and Integrated Power MOSFET

General Description
The RT7305 consists of a high voltage power MOSFET and a high-performance constant current LED driver with active power factor correction. It supports high power factor across a wide range of line voltages, and it drives the converter in the Quasi-Resonant (QR) mode to achieve higher efficiency. By using Primary Side Regulation (PSR), RT7305 controls the output current accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component count, the cost, and the volume of the driver board.

RT7305 embeds comprehensive protection functions for robust designs, including LED open circuit protection, LED short circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (OVP), Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

Applications
- AC/DC LED Lighting Driver

Features
- Integrated 620V Power MOSFET
- Tight LED Current Regulation
- No Opto-Coupler and TL431 Required
- Power Factor Correction (PFC)
- Quasi-Resonant
- Maximum/Minimum Switching Frequency Clamping
- Maximum/Minimum on-Time Limitation
- Wide VDD Range (up to 25V)
- Multiple Protection Features
  - LED Open-Circuit Protection
  - LED Short-Circuit Protection
  - Output Diode Short-Circuit Protection
  - VDD Under-Voltage Lockout
  - VDD Over-Voltage Protection
  - Over-Temperature Protection
  - Cycle-by-Cycle Current Limitation
- RoHS Compliant and Halogen Free

Simplified Application Circuit

Flyback Application Circuit

Buck-Boost Application Circuit
Ordering Information

RT7305

Package Type
S : SOP-7

Lead Plating System
G : Green (Halogen Free and Pb Free)

Marking Information

RT7305GS : Product Number
YMDNN : Date Code

Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

Functional Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Supply Voltage (VDD) input. The controller will be enabled when VDD exceeds VTH_ON and disabled when VDD is lower than VTH_OFF.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground of the Controller.</td>
</tr>
<tr>
<td>3</td>
<td>ZCD</td>
<td>Zero Current Detection Input. This pin is used to sense the voltage at auxiliary winding of the transformer.</td>
</tr>
<tr>
<td>4</td>
<td>COMP</td>
<td>Compensation Node. Output of the internal trans-conductance amplifier.</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Current Sense Input. Connect this pin to the current sense resistor.</td>
</tr>
<tr>
<td>6</td>
<td>SOURCE</td>
<td>Source terminal of the integrated power MOSFET.</td>
</tr>
<tr>
<td>7</td>
<td>DRAIN</td>
<td>Drain terminal of the integrated power MOSFET.</td>
</tr>
</tbody>
</table>

Function Block Diagram
**Operation**

**Critical-Conduction Mode (CRM) with Constant On-Time Control**

Figure 1 shows a typical flyback converter with input voltage ($V_{IN}$). When main switch $Q_1$ is turned on with a fixed on-time ($t_{ON}$), the peak current ($I_{L_PK}$) of the magnetic inductor ($L_m$) can be calculated by the following equation:

$$I_{L_PK} = \frac{V_{IN}}{L_m} \times t_{ON}$$

![Figure 1. Typical Flyback Converter](image)

If the input voltage is the output voltage of the full-bridge rectifier with sinusoidal input voltage ($V_{IN_PK} \sin(\theta)$), the inductor peak current ($I_{L_PK}$) can be expressed as the following equation:

$$I_{L_PK} = \frac{V_{IN_PK} \sin(\theta)}{L_m} \times t_{ON}$$

When the converter operates in CRM with constant on-time control, the envelope of the peak inductor current will follow the input voltage waveform with in-phase. Thus, high power factor can be achieved, as shown in Figure 2.

**Primary-Side Constant-Current Regulation**

RT7305 needs no shunt regulator and opto-coupler at the secondary side to achieve the output current regulation. Figure 3 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which $V_{AUX}$ is the voltage on the auxiliary winding of the transformer.

![Figure 2. Inductor Current of CRM with Constant On-Time Control](image)

![Figure 3. Key Waveforms of a Flyback Converter](image)

**Voltage Clamping Circuit**

RT7305 provides a voltage clamping circuit at ZCD pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on ZCD pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile,
the sourcing ZCD current (I_{ZCD_SH}), flowing through the upper resistor (R_{ZCD1}), is sampled and held to be a line-voltage-related signal for propagation delay compensation. RT7305 embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to \text{I}_{ZCD_SH} \times K_{PC}) applies a voltage offset (I_{CS} \times R_{PC}) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the total power limit or output current can be equal at high and low line voltage.

**Quasi-Resonant Operation**

For improving converter’s efficiency, RT7305 detects valleys of the Drain-to-Source voltage (V_{DS}) of main switch and turns it on near the selected valley. For the valley detections, a pulse of the “valley signal” is generated after a 500ns (typ.) delay time which starts at which the voltage (V_{ZCD}) on ZCD pin goes down and reaches the voltage threshold (V_{ZCDT}, 0.4V typ.). During the rising of the V_{ZCD}, the V_{ZCD} must reach the voltage threshold (V_{ZCDA}, 0.5V typ.). Otherwise, no pulse of the “valley signal” is generated. Moreover, if the timing when the falling V_{ZCD} reaches V_{ZCDT} is not later than a mask time (t_{MASK}, 2\mu s typ.) then the valley signal will be masked and regards as no valley, as shown in Figure 4.

![Figure 4. Valley Signal Generating Method](image)

Figure 5 illustrating how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at end of the interval (t_{START}, 130\mu s typ.) which starts at the rising edge of the previous PWM signal. A blanking time (t_{S(MIN)}, 8.5\mu s typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the t_{S(MIN)} interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the t_{S(MIN)} interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the t_{S(MIN)} interval and no valley is detected after the end of the t_{S(MIN)} interval, the next PWM signal will be triggered automatically at end of the t_{S(MIN)} + 5\mu s (typ.).

**Figure 5. PWM Triggered Method**

### Protections

#### LED Open-Circuit Protection

In an event of output open circuit, the converter will be shut down to prevent being damaged, and it will be auto-restarted when the output is recovered. Once the LED is open-circuit, the output voltage and V_{ZCD} will rise. When the sample-and-hold ZCD voltage (V_{ZCD_SH}) exceeds its OV threshold (V_{ZCD_OVP}, 3.1V typ.), output OVP will be activated and the PWM output (GD pin) will be forced low to turn off the main switch. If the output is still open-circuit when the converter restarts, the converter will be shut down again.

#### LED Short-Circuit Protection

LED short-circuit protection can be achieved by VDD UVLO and cycle-by-cycle current limitation. Once LED
short-circuit failure occurs, VDD drops related to the output voltage. When the VDD is lower than falling UVLO threshold (VTH_OFF, 9V typ.), the converter will be shut down and it will be auto-restarted when the output is recovered.

**Output Diode Short-Circuit Protection**

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage VCS exceeds the threshold (VCS_SD 1.5 typ.) of the output diode short-circuit protection, RT7305 will shut down the PWM output (GD pin) in few cycles to prevent the converter from damage. It will be auto-restarted when the failure condition is recovered.

**VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)**

RT7305 will be enabled when VDD voltage (VDD) exceeds rising UVLO threshold (VTH_ON, 16V typ.) and disabled when VDD is lower than falling UVLO threshold (VTH_OFF, 9V typ.). When VDD exceeds its over-voltage threshold (VOVP, 27V typ.), the PWM output of RT7305 is shut down. It will be auto-restarted when the VDD is recovered to a normal level.

**Over-Temperature Protection (OTP)**

The RT7305 provides an internal OTP function to protect the controller itself from suffering thermal stress and permanent damage. It is not suggested to use the function as precise control of over temperature. Once the junction temperature is higher than the OTP threshold (TSD, 150°C typ.), the controller will shut down until the temperature cools down by 30°C (typ.). Meanwhile, if VDD reaches falling UVLO threshold voltage (VTH_OFF), the controller will hiccup till the over temperature condition is removed.
Absolute Maximum Ratings  (Note 1)
- DRAIN to GND Voltage, $V_{DRAIN}$ $\leq -0.3V$ to 620V
- VDD Supply Voltage, $V_{DD}$ $\leq -0.3V$ to 30V
- SOURCE, CS, ZCD, COMP to GND Voltage $\leq -0.3V$ to 6V
- Power Dissipation, $P_D$ @ $T_A = 25^\circ$C $\leq 1.246$W
- Package Thermal Resistance (Note 2) $\theta_{JA} \leq 80.25$°C/W
- Lead Temperature (Soldering, 10 sec.) $\leq 260^\circ$C
- Junction Temperature $\leq 150^\circ$C
- Storage Temperature Range $\leq -65^\circ$C to 150°C
- ESD Susceptibility (Note 3) HBM (Human Body Model) $\leq 2kV$
  MM (Machine Model) $\leq 200V$

Recommended Operating Conditions  (Note 4)
- Supply Input Voltage, $V_{DD}$ $\leq 12$V to 25V
- COMP Voltage, $V_{COMP}$ $\leq 0.7$V to 4.3V
- Junction Temperature Range $\leq -40^\circ$C to 125°C

Electrical Characteristics
($V_{DD} = 15V$, $T_A = 25^\circ$C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>VDD Supply Current and Protections</td>
<td></td>
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<tr>
<td>VDD OVP Threshold Voltage</td>
<td>$V_{OVP}$</td>
<td></td>
<td>25.5</td>
<td>27</td>
<td>28.5</td>
<td>V</td>
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<tr>
<td>VDD OVP De-bounce Time</td>
<td></td>
<td>(Note 5)</td>
<td>--</td>
<td>10</td>
<td>--</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Rising UVLO Threshold Voltage</td>
<td>$V_{TH_ON}$</td>
<td></td>
<td>15</td>
<td>16</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>Falling UVLO Threshold Voltage</td>
<td>$V_{TH_OFF}$</td>
<td></td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>V</td>
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<tr>
<td>Operating Supply Current</td>
<td>$I_{DD_OP}$</td>
<td>$I_{ZCD} = 0$</td>
<td>--</td>
<td>--</td>
<td>3.5</td>
<td>mA</td>
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<tr>
<td>Start-up Current</td>
<td>$V_{DD} = V_{TH_ON} - 1V$</td>
<td></td>
<td>--</td>
<td>--</td>
<td>30</td>
<td>$\mu$A</td>
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<tr>
<td>ZCD Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower Clamp Voltage</td>
<td>$I_{ZCD} = 0$ to $-2.5mA$</td>
<td></td>
<td>--</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>ZCD OVP Threshold Voltage</td>
<td>$V_{ZCD_OVP}$</td>
<td>At the knee point (Note 5)</td>
<td>2.8</td>
<td>3.1</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td>Constant Current Control Section</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Regulated factor for Constant-Current Control</td>
<td>$K_{CC}$</td>
<td></td>
<td>0.245</td>
<td>0.25</td>
<td>0.255</td>
<td>V</td>
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<tr>
<td>Maximum COMP Voltage</td>
<td>$I_{COMP} &lt; 30\mu$A</td>
<td></td>
<td>4.5</td>
<td>--</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>Maximum COMP Sourcing Current</td>
<td>$I_{COMP(MAX)}$</td>
<td>$V_{COMP} &lt; 3.5V$</td>
<td>--</td>
<td>62.5</td>
<td>--</td>
<td>$\mu$A</td>
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<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
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<td><strong>Timing Control Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Ramp Slope of the Ramp Generator Output</td>
<td>$S_{ramp}$</td>
<td></td>
<td>228</td>
<td>270</td>
<td>312</td>
<td>mV/μs</td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>$I_{ON(MIN)}$</td>
<td>$I_{ZCD} = -150 \mu A$</td>
<td>1.8</td>
<td>2.5</td>
<td>3.1</td>
<td>μs</td>
</tr>
<tr>
<td>Maximum On-Time</td>
<td>$I_{ON(MAX)}$</td>
<td></td>
<td>29</td>
<td>47</td>
<td>65</td>
<td>μs</td>
</tr>
<tr>
<td>Minimum Switching Period</td>
<td>$t_{S(MIN)}$</td>
<td></td>
<td>7</td>
<td>8.5</td>
<td>10</td>
<td>μs</td>
</tr>
<tr>
<td>Duration of Starter</td>
<td>$t_{START}$</td>
<td>At no valley detected</td>
<td>75</td>
<td>130</td>
<td>300</td>
<td>μs</td>
</tr>
<tr>
<td><strong>Current Sense Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blanking Time</td>
<td>$t_{LEB}$</td>
<td>$LEB + Propagation Delay$ (Note 5)</td>
<td>--</td>
<td>470</td>
<td>--</td>
<td>ns</td>
</tr>
<tr>
<td>Output Diode Short-Circuit Protection Voltage Threshold at CS</td>
<td>$V_{CS,SD}$</td>
<td>Shutdown when $V_{CS} &gt; V_{CS,SD}$ in 7 cycles.</td>
<td>--</td>
<td>1.5</td>
<td>--</td>
<td>V</td>
</tr>
<tr>
<td>CS Voltage Threshold for Peak Current Limitation</td>
<td>$V_{CS,CL}$</td>
<td></td>
<td>0.93</td>
<td>1.03</td>
<td>1.13</td>
<td>V</td>
</tr>
<tr>
<td>Propagation Delay Compensation factor</td>
<td>$K_{PC}$</td>
<td>Sourcing $I_{CS} = I_{ZCD} \times K_{PC}$, $I_{ZCD} = -150 \mu A$</td>
<td>--</td>
<td>0.02</td>
<td>--</td>
<td>A/A</td>
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<tr>
<td><strong>Over-Temperature Protection Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-Temperature Threshold</td>
<td>$T_{SD}$</td>
<td>(Note 5)</td>
<td>--</td>
<td>150</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td>Over-Temperature Threshold Hysteresis</td>
<td>$T_{SD,HYS}$</td>
<td>(Note 5)</td>
<td>--</td>
<td>30</td>
<td>--</td>
<td>°C</td>
</tr>
<tr>
<td><strong>Power MOSFET Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-to-Source Leakage Current</td>
<td>$I_{DSS}$</td>
<td>$V_{DS} = 620V, V_{DD} = 0V$</td>
<td>--</td>
<td>--</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>Static Drain-Source On-Resistance</td>
<td>$R_{DS(ON)}$</td>
<td>$I_{D} = 100mA$</td>
<td>--</td>
<td>--</td>
<td>6.5</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Guarantee by design.
Typical Application Circuit

Flyback Application Circuit

Buck-Boost Application Circuit

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Table 1. Suggested Component Values

<table>
<thead>
<tr>
<th>C_{VDD} (µF)</th>
<th>C_{COMP} (µF)</th>
<th>C_{ZCD} (pF)</th>
<th>C_{CS} (pF)</th>
<th>R_{ST} (MΩ)</th>
<th>R_{AUX} (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>2.2</td>
<td>22 (optional)</td>
<td>10 (optional)</td>
<td>1</td>
<td>10</td>
</tr>
</tbody>
</table>
Typical Operating Characteristics

**V\text{OVP} vs. Junction Temperature**

![Graph showing V\text{OVP} vs. Junction Temperature](image1)

**V\text{TH\_ON} vs. Junction Temperature**

![Graph showing V\text{TH\_ON} vs. Junction Temperature](image2)

**V\text{TH\_OFF} vs. Junction Temperature**

![Graph showing V\text{TH\_OFF} vs. Junction Temperature](image3)

**I\text{DD\_OP} vs. Junction Temperature**

![Graph showing I\text{DD\_OP} vs. Junction Temperature](image4)

**K\text{CC} vs. Junction Temperature**

![Graph showing K\text{CC} vs. Junction Temperature](image5)

**I\text{COMP\(\text{max}\)} vs. Junction Temperature**

![Graph showing I\text{COMP\(\text{max}\)} vs. Junction Temperature](image6)
**Sramp vs. Junction Temperature**

![Graph](image)

**t\text{ON(min)} vs. Junction Temperature**

![Graph](image)

**t\text{START vs. Junction Temperature**

![Graph](image)

**V\text{CS_SD vs. Junction Temperature**

![Graph](image)

**V\text{CS_CL vs. Junction Temperature**

![Graph](image)

**K\text{PC vs. Junction Temperature**

![Graph](image)
Application Information

Output Current Setting

Considering the conversion efficiency, the programmed DC level of the average output current ($I_{OUT}(t)$) can be derived as:

$$I_{OUT\_CC} = \frac{1}{2} \times K \times \frac{N_P}{N_S} \times K_{CC} \times CTR_{TX1}$$

$$CTR_{TX1} = \frac{I_{SEC\_PK}}{I_{PRI\_PK}} \times \frac{N_S}{N_P}$$

In which $CTR_{TX1}$ is the current transfer ratio of the transformer $TX1$, $I_{SEC\_PK}$ is the peak current of secondary side, and $I_{PRI\_PK}$ is the peak current of the primary side. $CTR_{TX1}$ can be estimated to be 0.9. According to the above parameters, current sense resistor $R_{CS}$ can be determined as the following equation:

$$R_{CS} = \frac{1}{2} \times K \times \frac{N_P}{N_S} \times \frac{K_{CC}}{I_{OUT\_CC}} \times CTR_{TX1}$$

Propagation Delay Compensation Design

The $V_{CS}$ deviation ($\Delta V_{CS}$) caused by propagation delay effect can be derived as:

$$\Delta V_{CS} = \frac{V_{IN} \cdot t_D \cdot R_{CS}}{L_m}$$

In which $t_D$ is the delay period which includes the propagation delay of RT7305 and the turn-off transition of the main MOSFET. The sourcing current from CS pin of RT7305 ($I_{CS}$) can be expressed as:

$$I_{CS} = K_{PC} \cdot \frac{V_{IN} \cdot N_A}{N_P} \cdot \frac{1}{R_{ZCD1}}$$

where $N_A$ is the turns number of auxiliary winding.

$R_{PC}$ can be designed by:

$$R_{PC} = \frac{\Delta V_{CS}}{I_{CS}} = \frac{t_D \cdot R_{CS} \cdot R_{ZCD1}}{L_m \cdot K_{PC}} \times \frac{N_P}{N_A}$$

Minimum On-Time Setting

RT7305 limits a minimum on-time ($t_{ON\_MIN}$) for each switching cycle. The $t_{ON\_MIN}$ is a function of the sample-and-hold ZCD current ($I_{ZCD\_SH}$) as following:

$$t_{ON\_MIN} \cdot I_{ZCD\_SH} = 375p \cdot sec \cdot A \text{ (typ.)}$$

Thus, $R_{ZCD1}$ can be determined by:

$$R_{ZCD1} = \frac{t_{ON\_MIN} \cdot V_{IN}}{375p} \cdot \frac{N_A}{N_P} \text{ (typ.)}$$

In addition, the current flowing out of ZCD pin must be lower than 2.5mA (typ.). Thus, the $R_{ZCD1}$ is also determined by:

$$R_{ZCD1} > \frac{\sqrt{2} \cdot V_{AC\_MAX}}{2.5m} \cdot \frac{N_A}{N_P}$$

where the $V_{AC\_MAX}$ is maximum input AC voltage.

Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the knee voltage on the auxiliary winging. It is recommended that output OV level ($V_{O\_OUT}$) is set at 120% of nominal output voltage ($V_{OUT}$). Thus, $R_{ZCD1}$ and $R_{ZCD2}$ can be determined by the equation as:

$$V_{OUT} \cdot \frac{N_A}{N_S} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} \cdot 120\% = 3.1V \text{ (typ.)}$$

Table 2. Suggested Component Values Range

<table>
<thead>
<tr>
<th>Component</th>
<th>Range of Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{VDD}$</td>
<td>10μF to 33μF</td>
</tr>
<tr>
<td>$C_{COMP}$</td>
<td>1μF to 4.7μF</td>
</tr>
<tr>
<td>$C_{ZCD}$</td>
<td>NC to 22pF</td>
</tr>
<tr>
<td>$C_{CS}$</td>
<td>NC to 10pF</td>
</tr>
<tr>
<td>$R_{ST}$</td>
<td>0.6MΩ to 2MΩ</td>
</tr>
<tr>
<td>$R_{AUX}$</td>
<td>10Ω to 100Ω</td>
</tr>
</tbody>
</table>
Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

\[ P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \]

where \( T_{J(MAX)} \) is the maximum junction temperature, \( T_A \) is the ambient temperature, and \( \theta_{JA} \) is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, \( \theta_{JA} \), is layout dependent. For SOP-7 package, the thermal resistance, \( \theta_{JA} \), is 80.25°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at \( T_A = 25°C \) can be calculated by the following formula:

\[ P_{D(MAX)} = \frac{(125°C - 25°C)}{(80.25°C/W)} = 1.246W \] for SOP-7 package

The maximum power dissipation depends on the operating ambient temperature for fixed \( T_{J(MAX)} \) and thermal resistance, \( \theta_{JA} \). The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Figure 6. Derating Curve of Maximum Power Dissipation

Layout Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply:

- The current path(1) from input capacitor, transformer, RT7305, current sense resistor return to input capacitor is a high frequency current loop. It must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially.

- The path(2) for the RCD snubber circuit is a high frequency switching loop. Keep it as small as possible.

- It is good for reducing noise, output ripple and EMI issue to separate ground traces of input capacitor(a), current sense resistor(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together on input capacitor ground(a). The areas of these ground traces should be kept large.

- Placing bypass capacitor for abating noise on IC is highly recommended. The capacitors \( C_{COMP} \), \( C_{ZCD} \), and \( C_{CS} \) should be placed as close to controller as possible.

- To minimize parasitic trace inductance and EMI, minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.
Figure 7. PCB Layout Guide
### Outline Dimension

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions In Millimeters</th>
<th>Dimensions In Inches</th>
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</thead>
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<td>Min.</td>
<td>Max.</td>
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<tr>
<td>B</td>
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<td>C</td>
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<td>1.753</td>
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</tr>
</tbody>
</table>

7-Lead SOP Plastic Package