

High-Efficiency PFC Controller

1 General Description

The RT7333M is a Power Factor Correction (PFC) controller incorporates advanced technologies such as tracking boost, valley switching, and frequency reduction. It operates in both Critical Conduction Mode (CRM) and Discontinuous Conduction Mode (DCM).

The feed-forward schemes and THD optimizer ensure a near-unity power factor across a wide range of input voltages and output power levels.

The totem-pole gate driver features an 800mA source current and a 1000mA sink current driving capability. The RT7333M includes a disabled function with an extremely low quiescent current ($<17\mu\text{A}$) to reduce power consumption in standby mode. The controller integrates comprehensive safety protection features, such as input undervoltage-lockout, output overvoltage protection, undervoltage protection, and cycle-by-cycle current limit.

The RT7333M is a highly integrated solution with a built-in programmable loop-compensation circuit to minimize the need for external components.

The RT7333M is available in a SOP-8 package. The recommended junction temperature range is -40°C to 125°C , and the ambient temperature range is -40°C to 85°C .

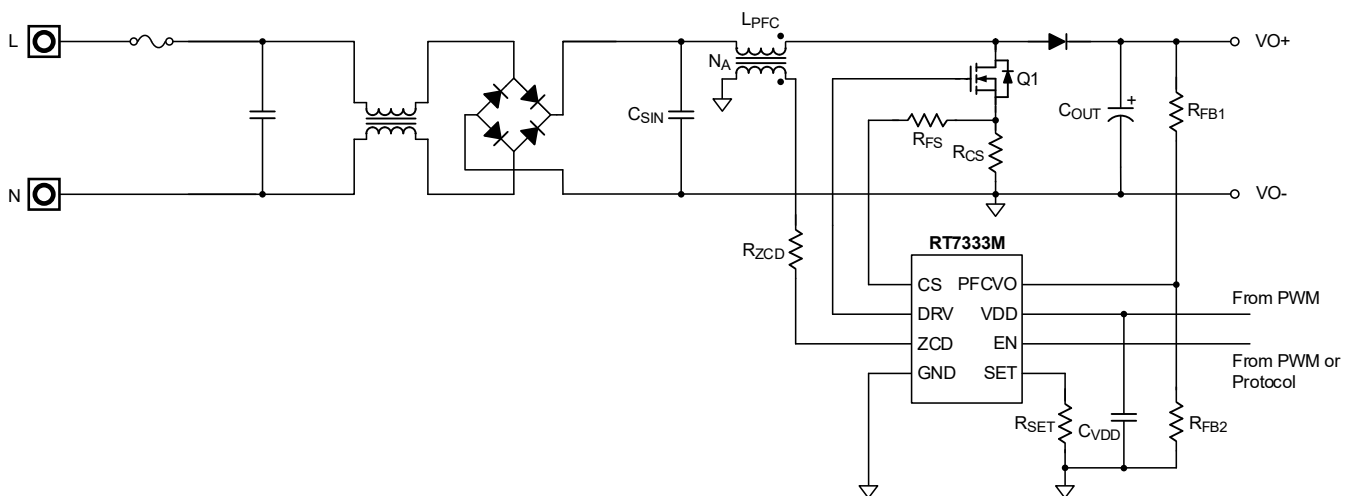
2 Features

- CRM/DCM Operation
- Constant On-Time Control (Voltage Mode)
- Built-In Loop-Compensation Circuit
- High Efficiency
 - Tracking Boost
 - Valley Switching in Both CRM and DCM
 - Frequency Reduction at Middle Load and Light Load
- Disable Function
 - Low Quiescent Current ($<17\mu\text{A}$)
- Ultra-Low Start-Up Current ($<5\mu\text{A}$)
- Maximum Switching Frequency Clamping (130kHz/176kHz/246kHz/397kHz)
- Burst Mode Operation at Light Load
- Maximum/Minimum On-Time Limit
- Cycle-by-Cycle Current Limit
- Output Overvoltage Protection (OVP)
- Undervoltage-Lockout (UVLO)

3 Applications

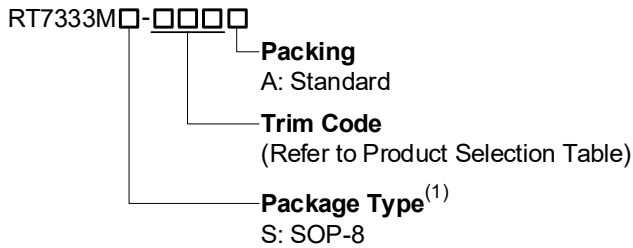
- USB-PD
- PCs, NBs, TVs, Monitors
- General Power Supplies

4 Simplified Application Circuit



5 Ordering Information

5.1 Product Number Information



Note 1.

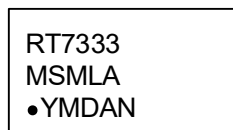
Richtek products are Richtek Green Policy compliant and marked with ⁽¹⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5.2 Product Selection Table

Product Number	RT7333MS-MLAA	RT7333MS-MTAA	RT7333MS-MTBA	RT7333MS-MTCA	RT7333MS-MTDA
Driver Voltage	10.5V	10.5V	10.5V	10.5V	10.5V
Tracking Boost	Linear	Two Stage	Two Stage	Two Stage	Two Stage
Overcurrent Limit (OCL)	Cycle-by-Cycle Limit	Cycle-by-Cycle Limit	Cycle-by-Cycle Limit	Cycle-by-Cycle Limit	Cycle-by-Cycle Limit
Overcurrent Protection (OCP)	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery
PFCVO OVP	Gate OFF	Gate OFF	Gate OFF	Gate OFF	Gate OFF
PFCVO UVP	Auto-Recovery	Auto-Recovery	Gate OFF	Gate OFF	Auto-Recovery
ZCD Short Protection	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery
VDD OVP	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery
BNI/BNO	Disable	Disable	Disable	Disable	Disable
Soft Start	Enable	Enable	Disable	Enable	Enable
gm _{ramp}	5μA/V	5μA/V	5μA/V	3μA/V	5μA/V

6 Marking Information

RT7333MS-MLAA



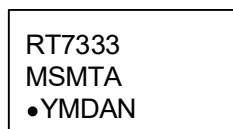
RT7333MSMLA: Product Code
YMDAN: Date Code

RT7333MS-MTCA



RT7333MSMTC: Product Code
YMDAN: Date Code

RT7333MS-MTAA



RT7333MSMTA: Product Code
YMDAN: Date Code

RT7333MS-MTDA



RT7333MSMTD: Product Code
YMDAN: Date Code

RT7333MS-MTBA



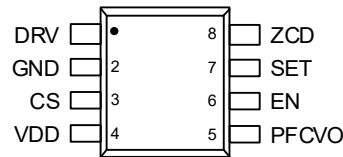
RT7333MSMTB: Product Code
YMDAN: Date Code

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7 Pin Configuration

(TOP VIEW)

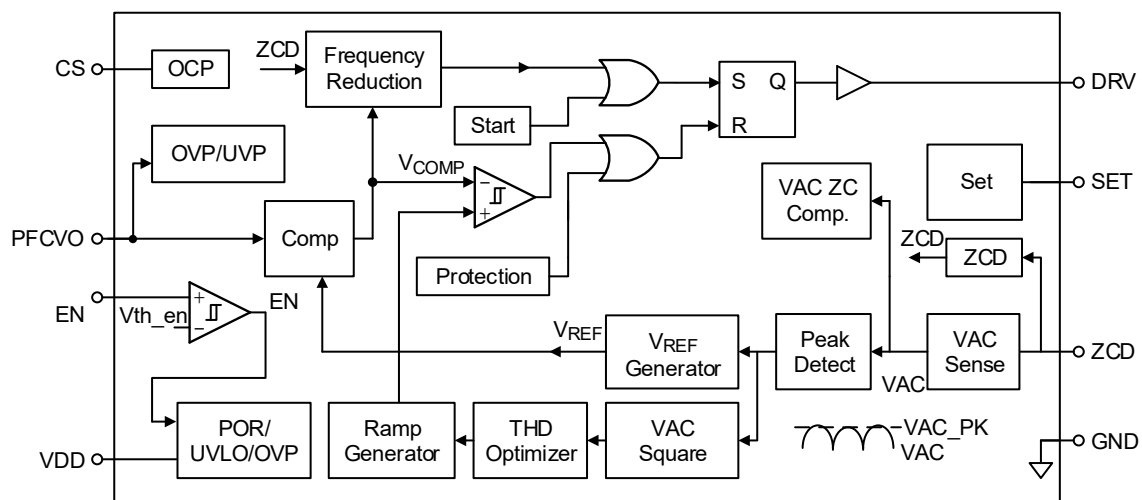


SOP-8

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	DRV	Gate driver output.
2	GND	Ground of the controller.
3	CS	Current sense input and maximum frequency setting. A current-sense resistor R_{CS} is connected between the source terminal of MOSFET and GND to determine the current limit. A resistor R_{FS} connected from the CS pin to the source terminal of MOSFET is used for the maximum switching frequency.
4	VDD	Supply voltage input. The controller will be enabled when the VDD voltage exceeds V_{TH_ON} (8V typical) and disabled when the VDD voltage drops below V_{TH_OFF} (5.5V typical).
5	PFCVO	Inverting input of the internal error amplifier. Connect a resistive divider from the output voltage to PFCVO for output voltage feedback. It is also used for OVP and UVP detections.
6	EN	Enable/disable PFC.
7	SET	The lowest voltage setting for the Tracking Boost.
8	ZCD	VIN feed-forward and zero current detection input. It is connected to an auxiliary winding of the PFC inductor to detect the demagnetization time.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VDD to GND ----- -0.3 to 40V
- EN to GND ----- -0.3 to 40V
- Gate Driver Output, DRV to GND ----- -0.3V to 20V
- CS, PFCVO, SET, ZCD to GND ----- -0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
 - SOP-8 ----- 0.53W
- Package Thermal Resistance (Note 3)
 - SOP-8, θ_{JA} ----- 188°C/W
 - SOP-8, θ_{JC} ----- 47°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
- HBM (Human Body Model) ----- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VDD ----- 7V to 34V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD OVP Threshold Voltage	VDD_OVP		35	37	39	V
VDD On Threshold	VTH_ON		6	8	10	V
VDD Off Threshold	VTH_OFF		5	5.5	6	V
VDD Start-Up Current	IDD_ST	VDD = VTH_ON – 0.1V	--	2.5	5	μA

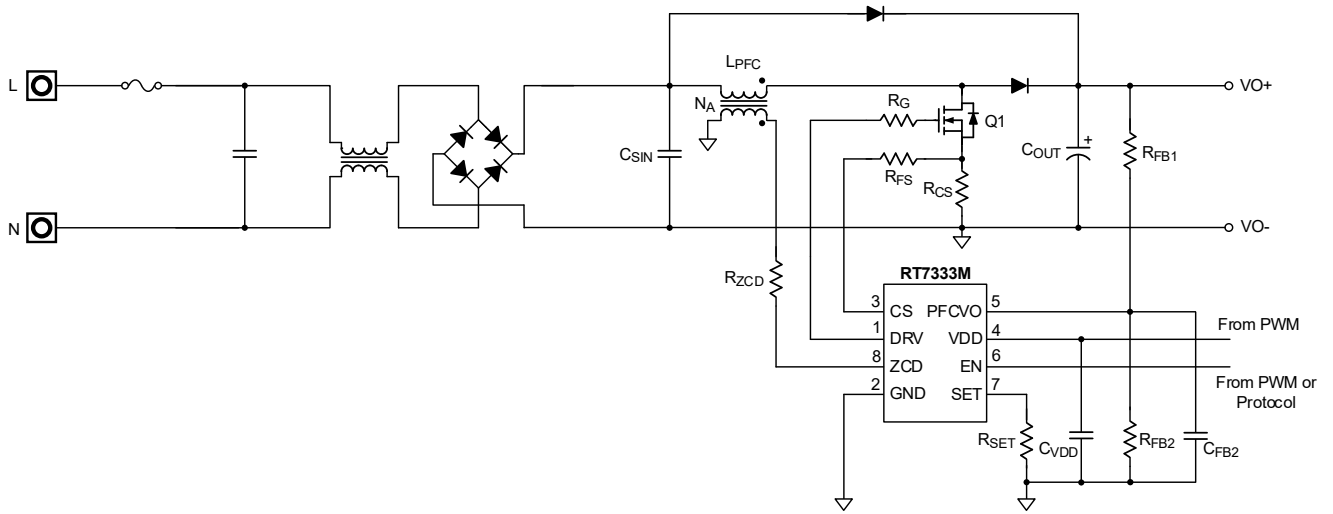
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Quiescent Current	I _{DD_QEN}	EN low disable, DRV pin floating	--	12	17	μA
VDD Operating Supply Current	I _{DD_OP}	f _s = 130kHz, DRV pin floating	--	2	3	mA
VDD Operating Current, Burst Mode	I _{DD_BT}	Burst mode, DRV pin floating	--	240	380	μA
Debounce Time for Exit Auto-Recovery Protection	t _{D_AUTO}	Enter auto-recovery protection mode	800	1000	1200	ms
PFCVO Section						
PFCVO Maximum Reference Voltage	V _{REF_MAX}		2.475	2.5	2.525	V
PFCVO OVP Threshold Voltage	V _{PFCVO_OVP}		2.64	2.72	2.8	V
PFCVO Hysteresis for Output OVP	V _{PFCVO_OVP_HYS}		0.04	0.1	0.16	V
PFCVO UVP Threshold Voltage (Output Short Protection)	V _{PFCVO_UVP}	For RT7333MS-MLAA, MTAA, and MTDA	0.36	0.4	0.44	V
		For RT7333MS-MTBA and MTCA	0.27	0.3	0.33	
PFCVO Hysteresis for Output UVP	V _{PFCVO_UVP_HYS}		0.07	0.1	0.13	V
Burst Mode Section						
Burst Mode Level	V _{COMP_BURST}		120	150	180	mV
Debounce Time of Burst Mode	t _{D_BURST}		14.4	18	21.6	ms
PFCVO Threshold for PFC Wake-Up	V _{PFCVO_WKP}		V _{REF} – 0.1V	V _{REF} – 0.07V	V _{REF} – 0.04V	V
ZCD Section						
Arming Voltage	V _{ZC_DA}		0.56	0.7	0.84	V
Trigger Voltage	V _{ZC_DT}		0.32	0.4	0.48	V
Delay Time of Forcing GATE ON If Without Detect Valley (DCM)	t _{ZC_TOUT_DCM}	If ZCD appears before f _{s_MAX} , counting from f _{s_MAX} , and no valley is detected within t _{ZC_TOUT_DCM} , the gate will turn on	3.2	4	4.8	μs
1 st ZCD Delay Time of Forcing GATE ON If Without Detect Valley (BCM)	t _{ZC_TOUT_BCM}	Counting from the gate turn-on, if no ZCD is detected within t _{ZC_TOUT_BCM} , the gate will turn on	60	70	82	μs
Sourcing Current Capability	I _{ZC_SOURCE}		1.1	--	--	mA
Sinking Current Capability	I _{ZC_SINK}		1.4	--	--	mA
Two Stage Low Line to High Line	I _{ZC_TWOH}	(Note 6)	--	297	--	μA
Two Stage High Line to Low Line	I _{ZC_TWOL}	(Note 6)	--	265	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ZCD Short Protection	I _{ZC_OC}		0.45	0.5	0.55	mA
Debounce Time of I _{ZC_OC}	t _{D_ZC_OC}		--	7	--	Clks
Internal Compensator Section						
R _Z for Zero Point	R _Z	(Note 6)	--	100	--	kΩ
C _Z for Zero Point	C _Z	(Note 6)	--	266	--	pF
Enhanced Transient Response (ETR) Section						
ETR Trigger Threshold High	V _{ETR_H_TH}		140	200	260	mV
ETR Trigger Threshold Low	V _{ETR_L_TH}		−260	−200	−140	mV
ETR Trigger Hysteresis	V _{ETR_HYS}		20	50	80	mV
Frequency Reduction (FR) Section						
FR_ET	V _{FR_ET}		1.28	1.35	1.4	V
FR_EX	V _{FR_EX}		0.3	0.35	0.42	V
Current Sense Section						
Leading Edge Blanking Time OC Limit	t _{LEB_OCL}		210	300	390	ns
OC Limit	V _{OCL}		0.36	0.4	0.44	V
Leading Edge Blanking Time OCP	t _{LEB_OCP}		140	200	280	ns
OCP	V _{OCP}		1.1	1.2	1.3	V
OCP Debounce Time	t _{D_OCP}		--	7	--	Clks
Gate Driver Section						
Gate Output Clamping Voltage	V _{CLAMP}	V _{DD} = 15V For RT7333MS-MLAA, MTAA, MTCA, and MTDA	9.5	10.5	11.5	V
		V _{DD} = 15V For RT7333MS-MTBA		10.5		V
Timing Control Section						
Maximum Switching Frequency	f _{S_MAX}	R _{FS} = 1kΩ±1%	117	130	143	kHz
		R _{FS} = 620Ω±1%	158	176	194	
		R _{FS} = 330Ω±1%	221	246	271	
		R _{FS} = 100Ω±1%	357	397	437	
Minimum On-Time	t _{ON_MIN}		230	300	370	ns
Maximum On-Time	t _{ON_MAX}		16	20	25	μs
EN Section						
V _{TH1} VIH Voltage	V _{EN_TH1_VIH}		0.55	1.16	1.7	V
V _{TH1} VIL Voltage	V _{EN_TH1_VIL}		0.4	0.75	1	V
V _{TH2} VIH Voltage	V _{EN_TH2_VIH}		2.6	2.7	2.8	V
Hysteresis Voltage of V _{TH2}	V _{EN_TH2_HYS}		10	50	90	mV
EN Pull-Low Resistor	R _{EN_PULL_L}		175	250	325	kΩ

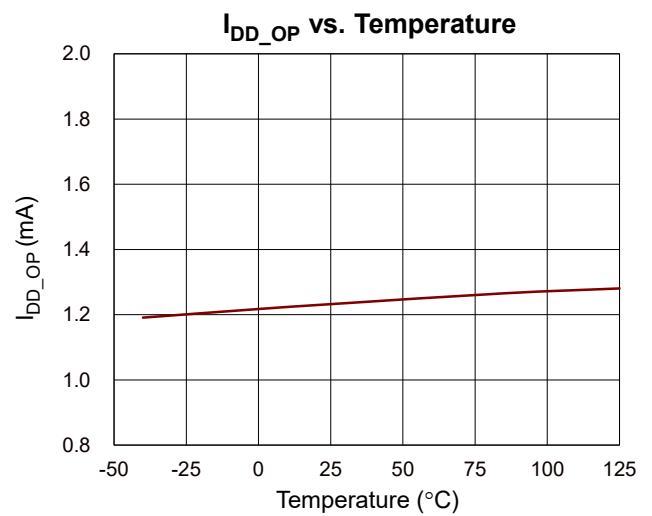
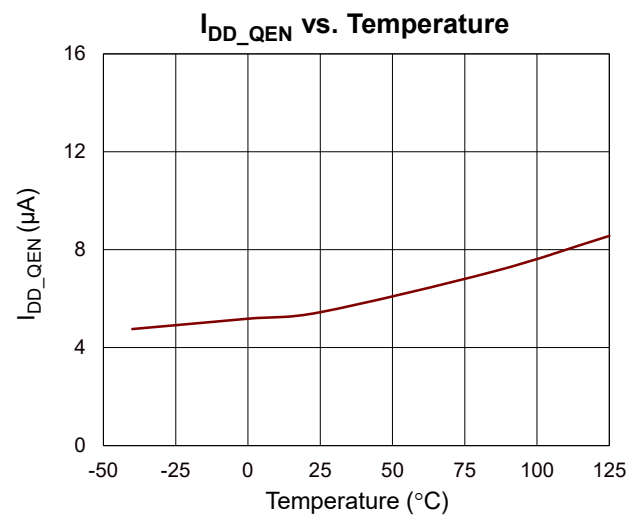
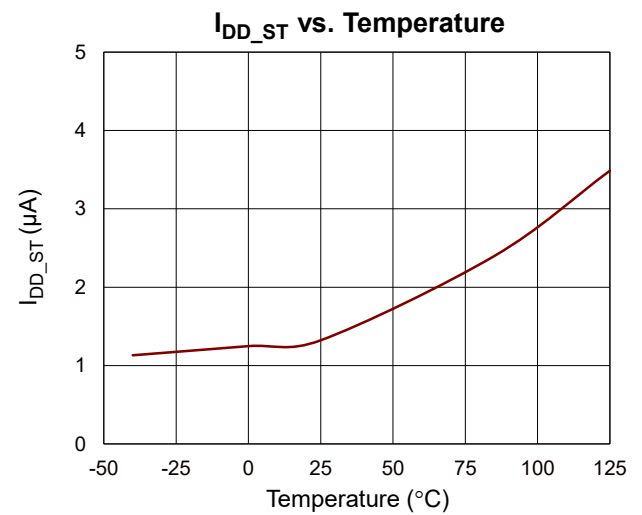
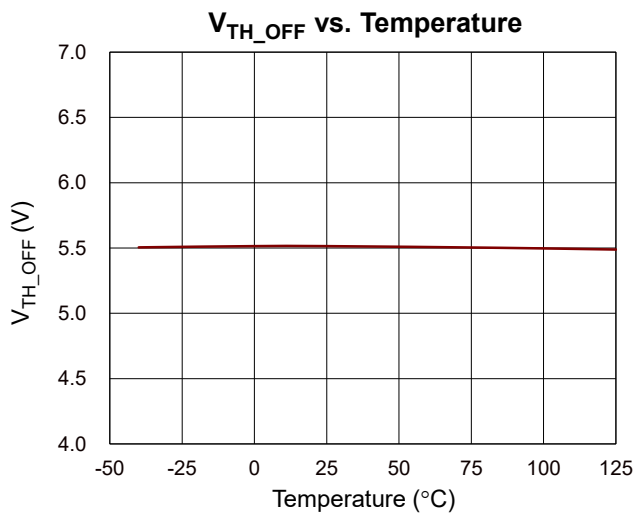
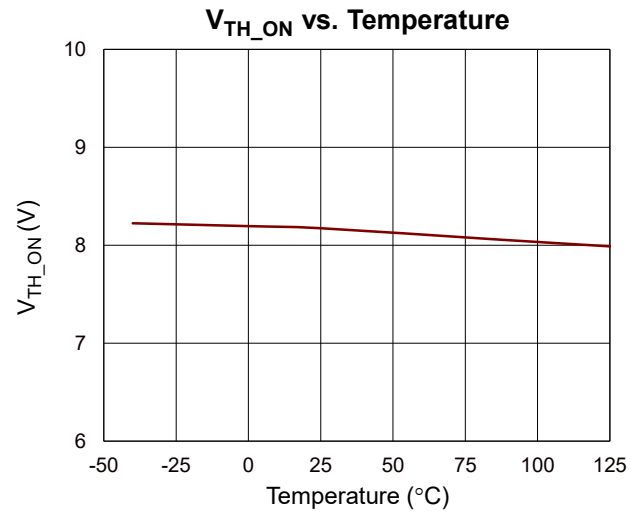
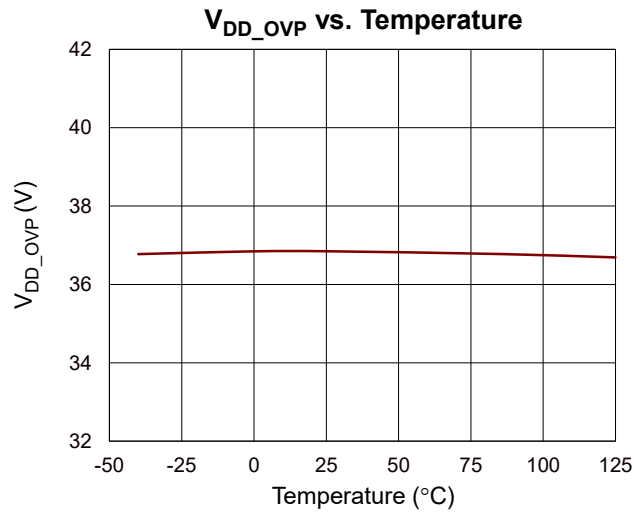
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SET Section						
Tracking Boost Lowest Voltage Initial Setting	VREF_MIN	SET pin open, VO_PFC = 390V	2.475	2.5	2.525	V
		SET pin short, VO_PFC_MIN = 250V	1.52	1.6	1.68	V
		RSET = 100kΩ±1%, VO_PFC_MIN = 200V	1.21	1.28	1.35	V
		RSET = 330kΩ±1%, VO_PFC_MIN = 300V	1.82	1.92	2.02	V
Over-Temperature Protection (OTP) Section						
Initial Over-Temperature Protection Threshold	TOTP_INTH	(Note 6)	--	150	--	°C
Over-Temperature Protection Threshold After Start-Up	TOTP_STTH	(Note 6)	--	160	--	°C

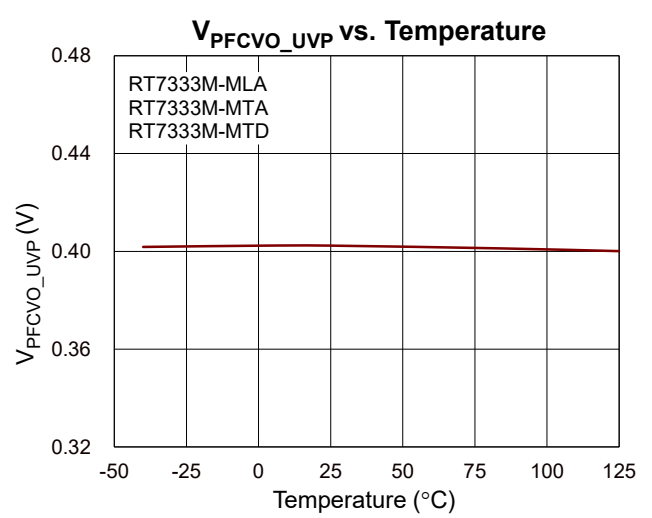
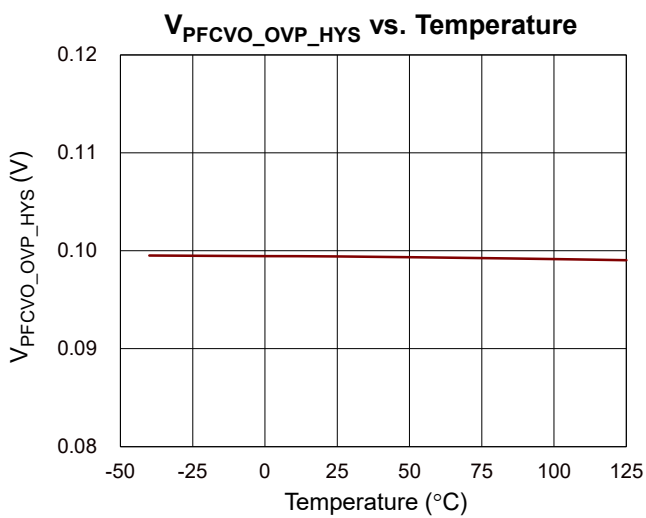
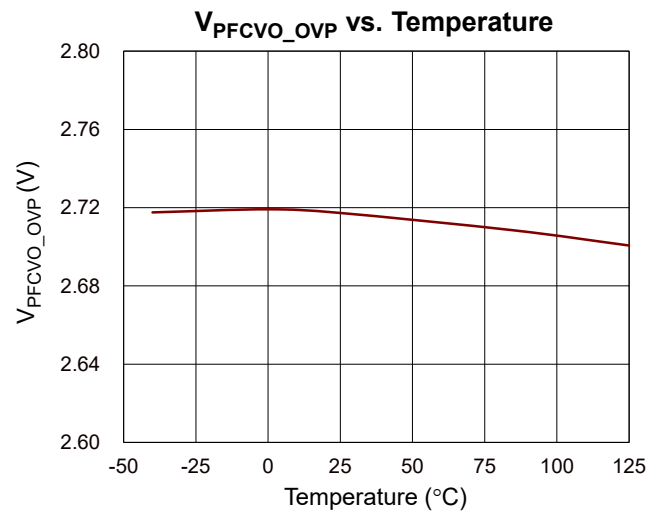
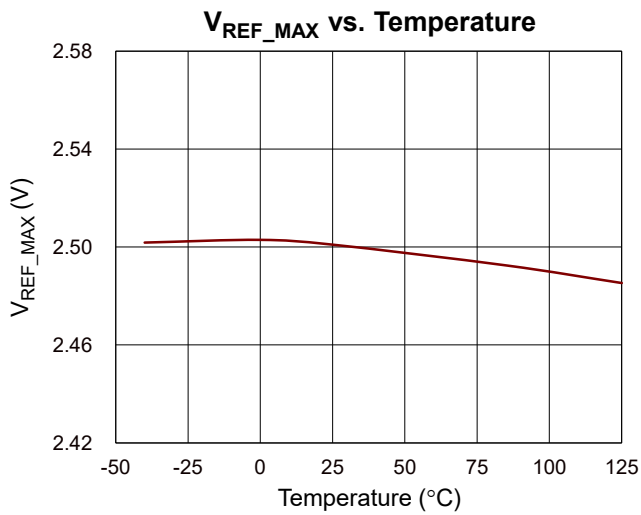
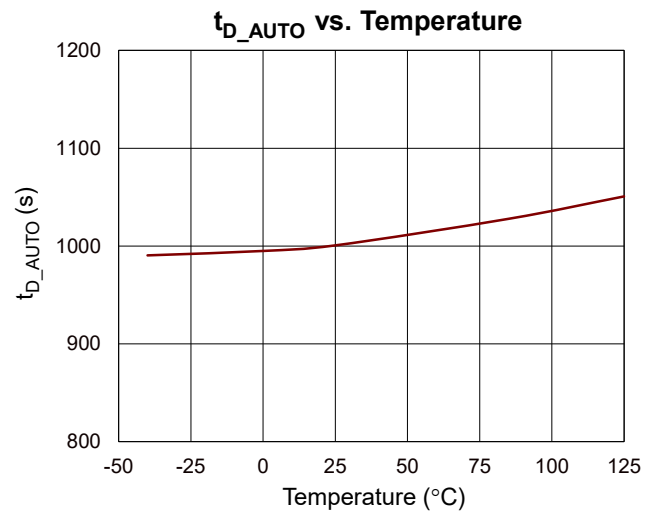
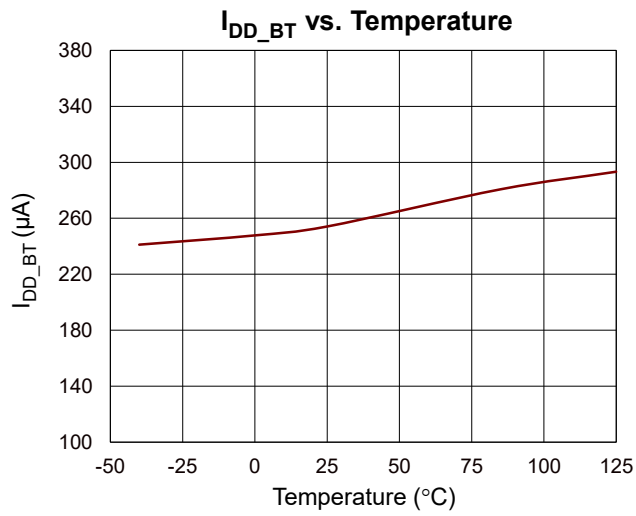
Note 6. Guaranteed by design.

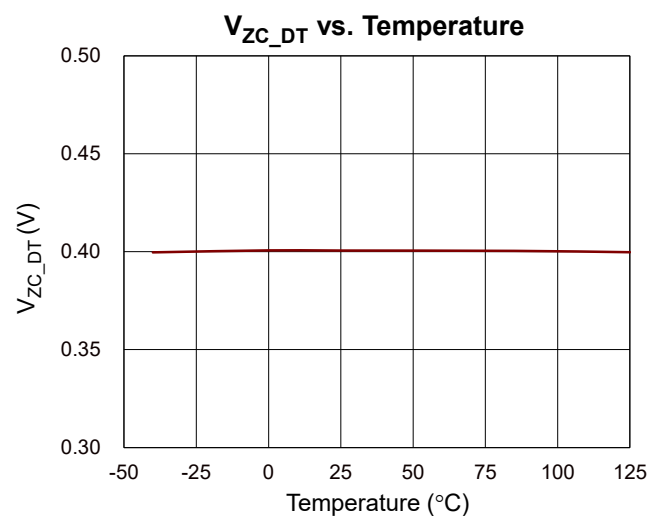
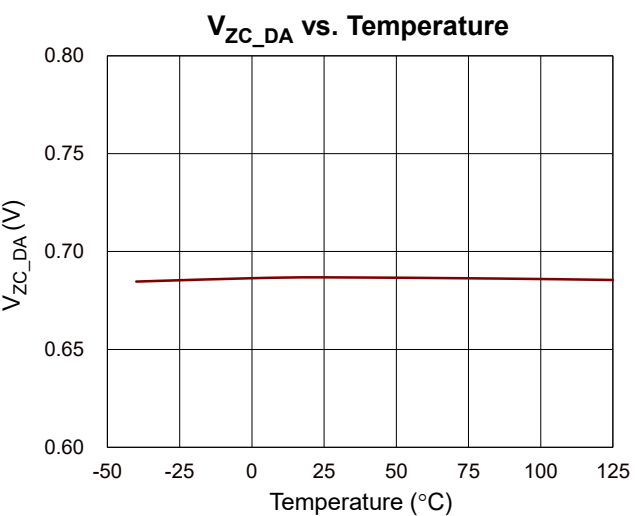
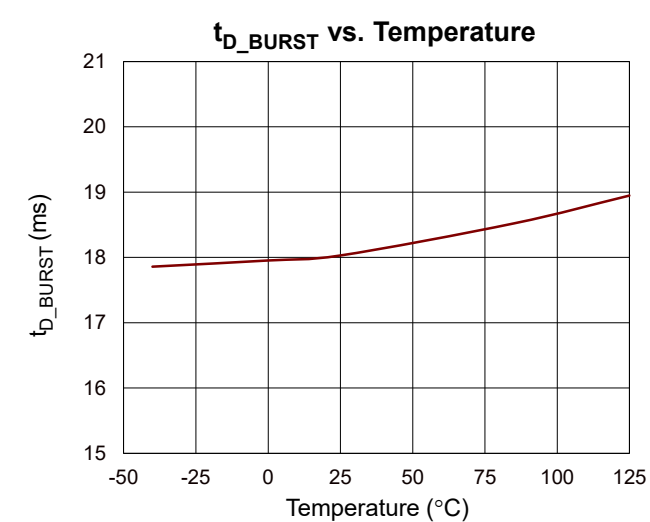
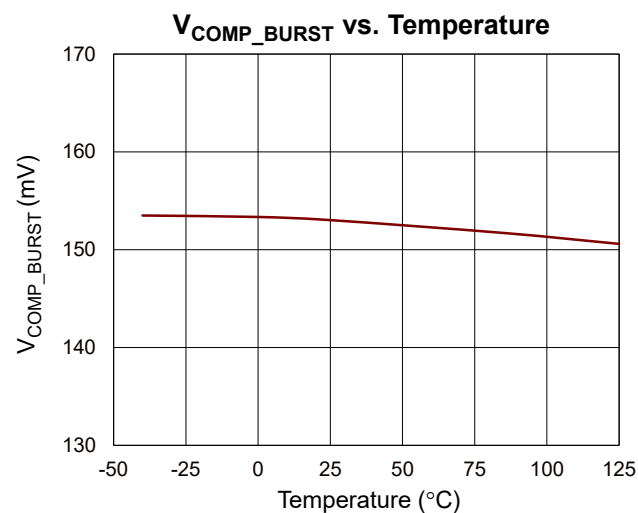
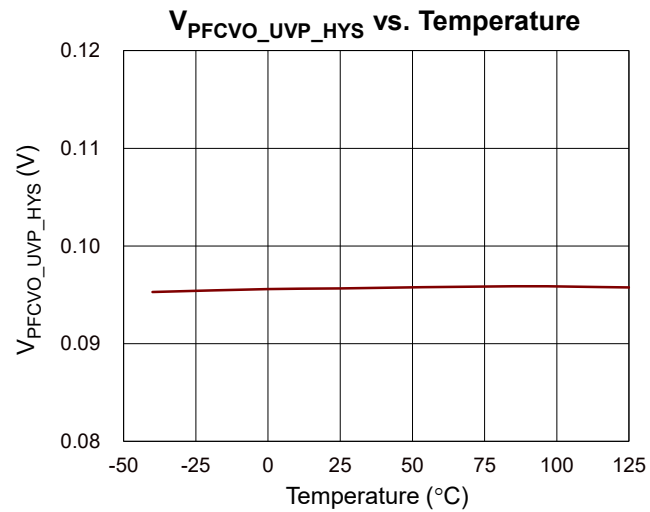
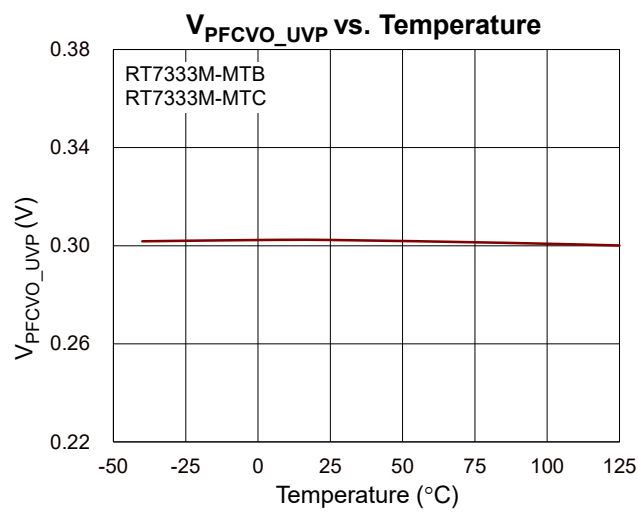
13 Typical Application Circuit

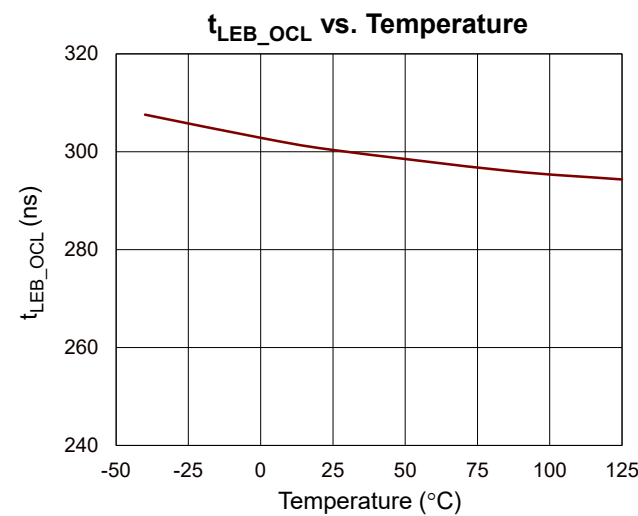
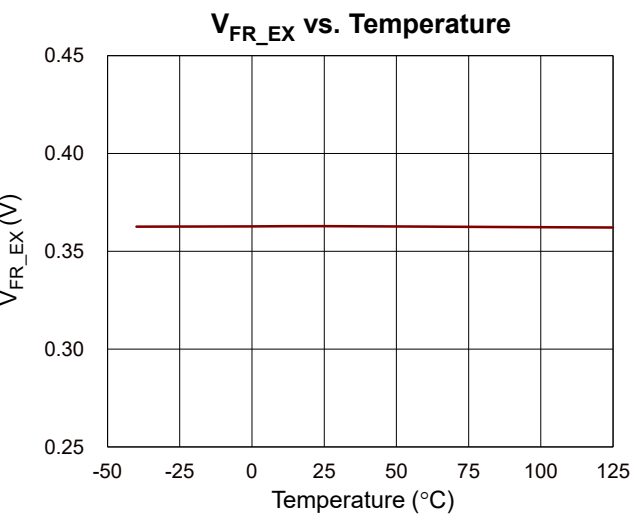
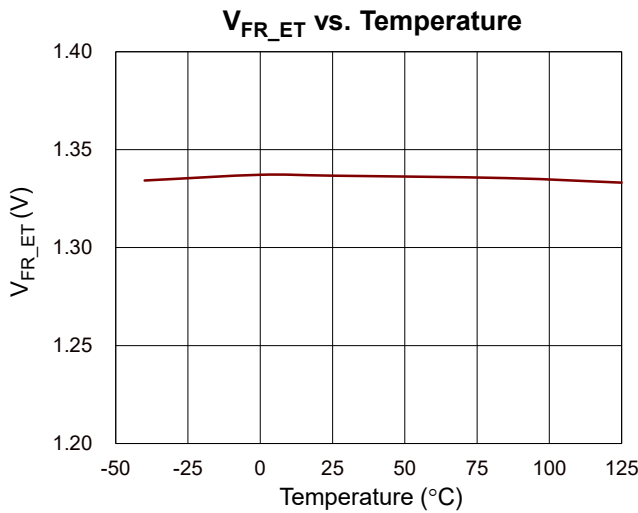
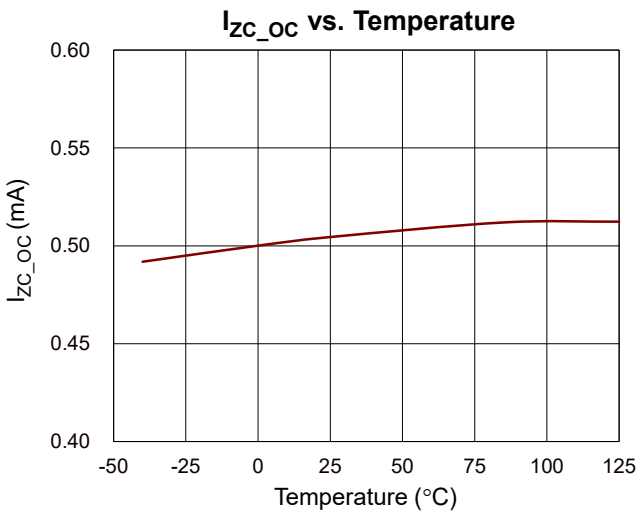
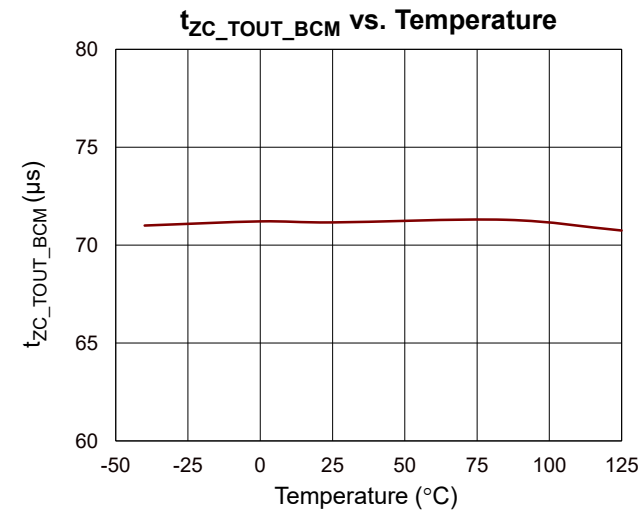
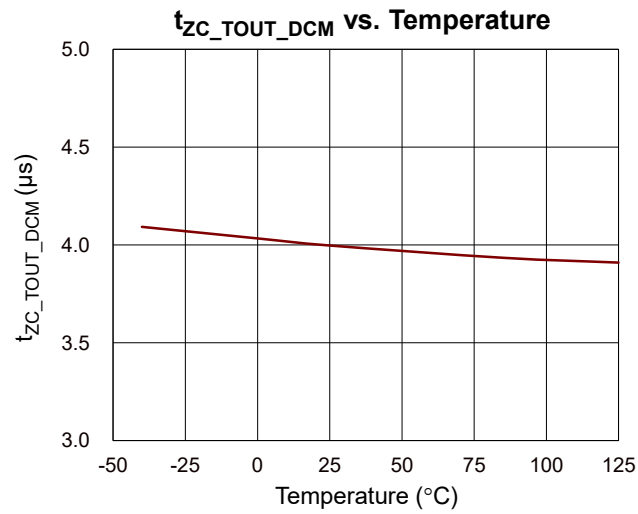


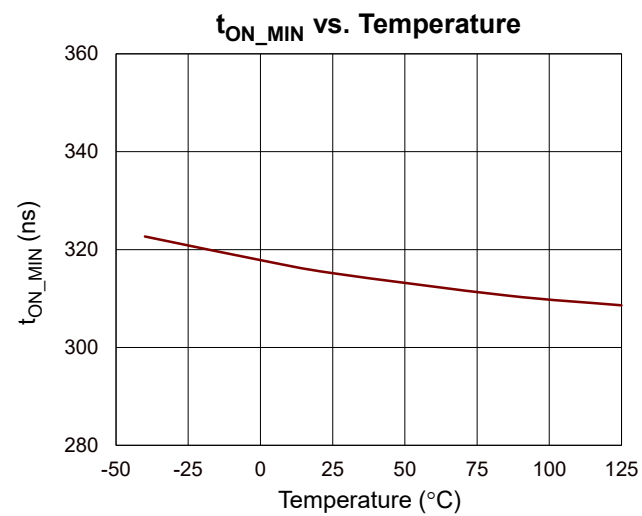
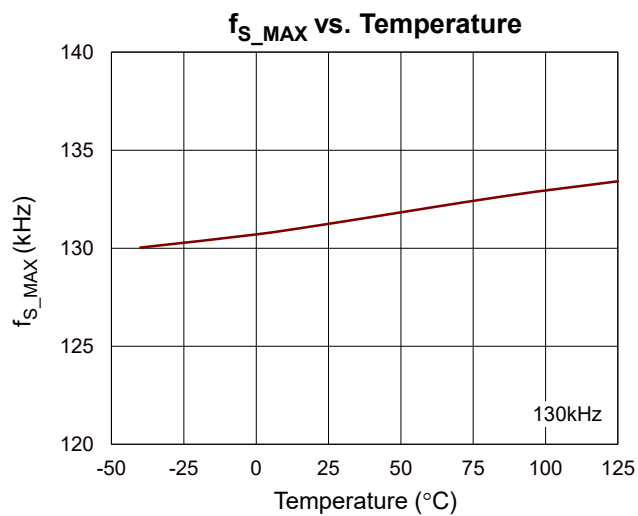
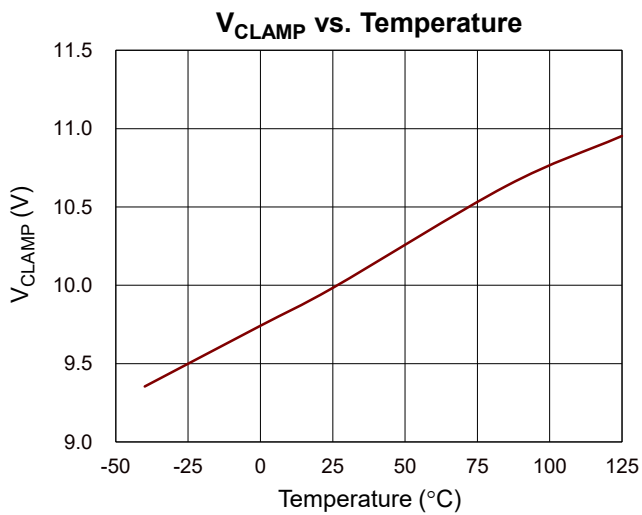
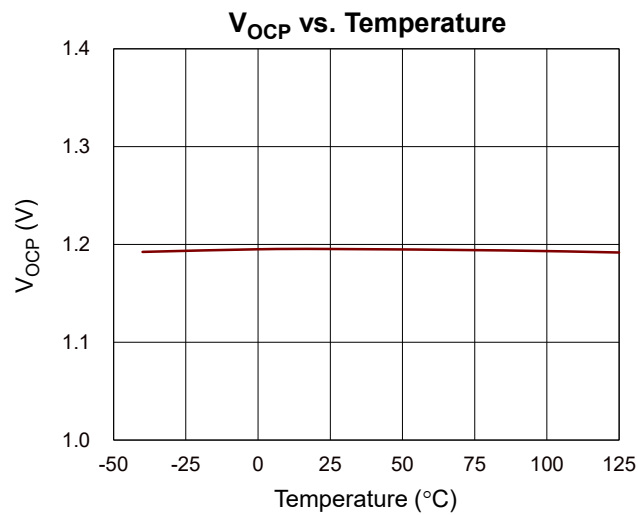
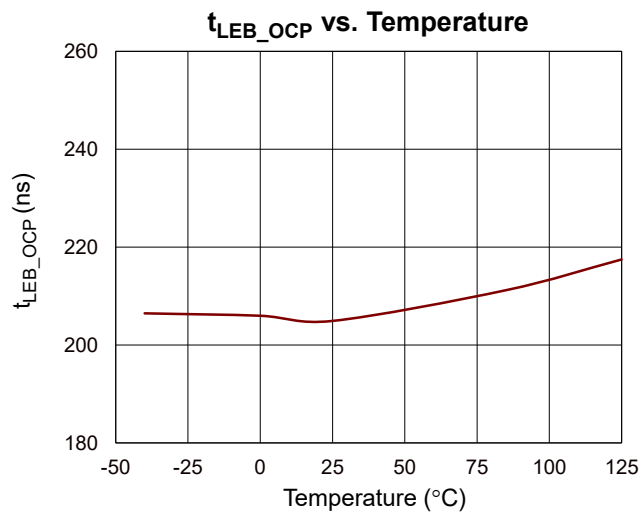
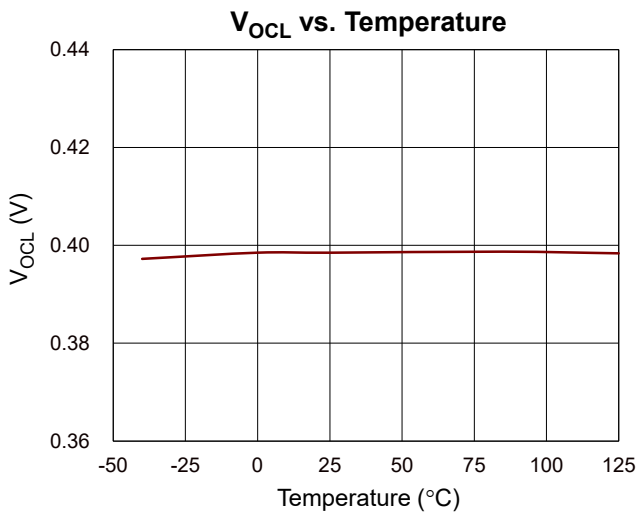
14 Typical Operating Characteristics

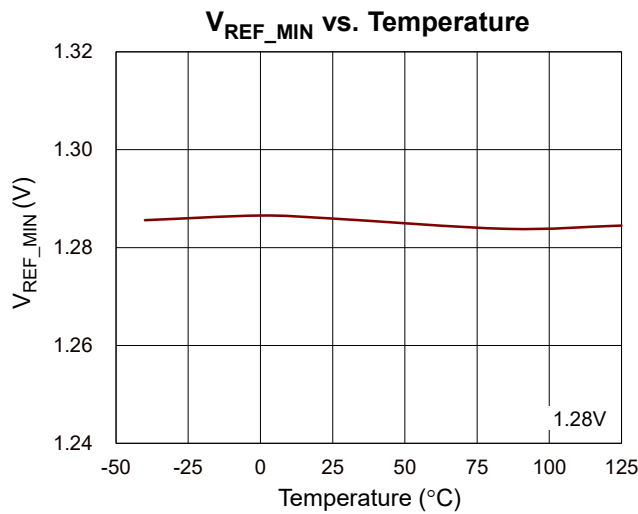
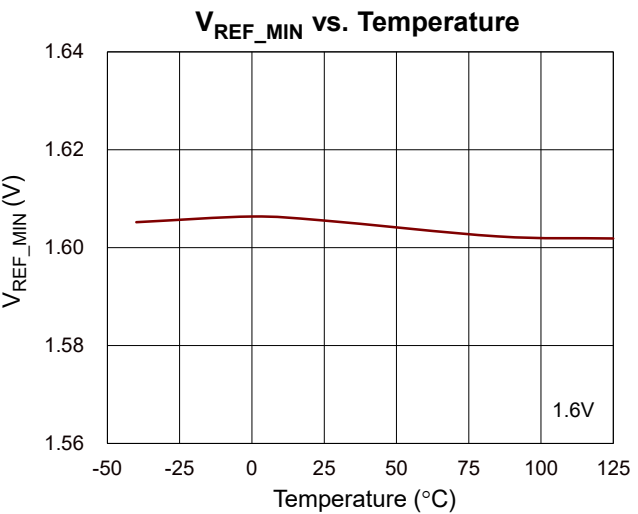
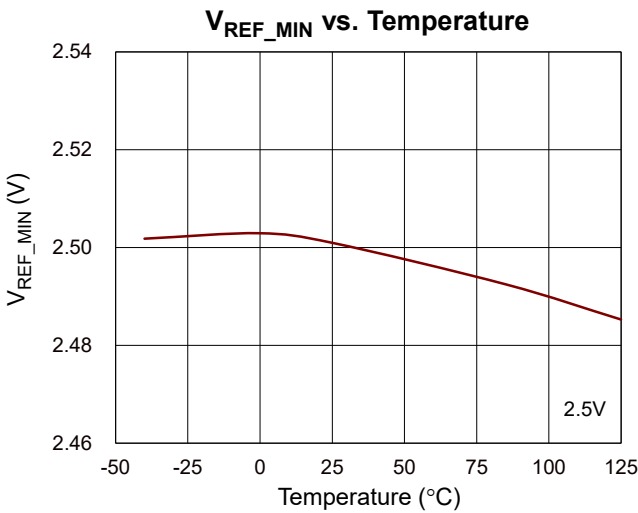
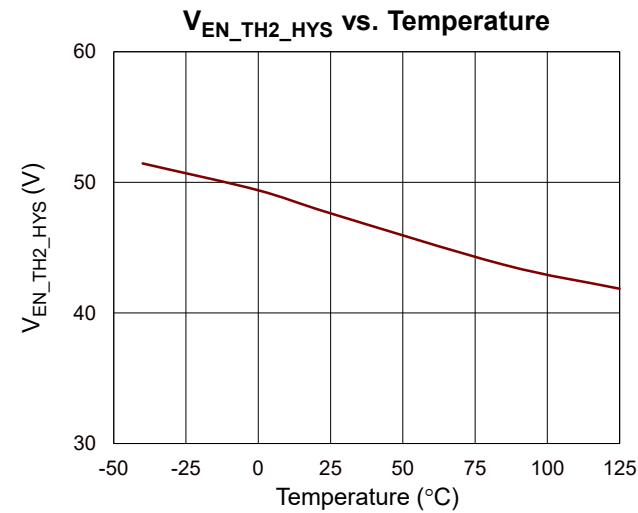
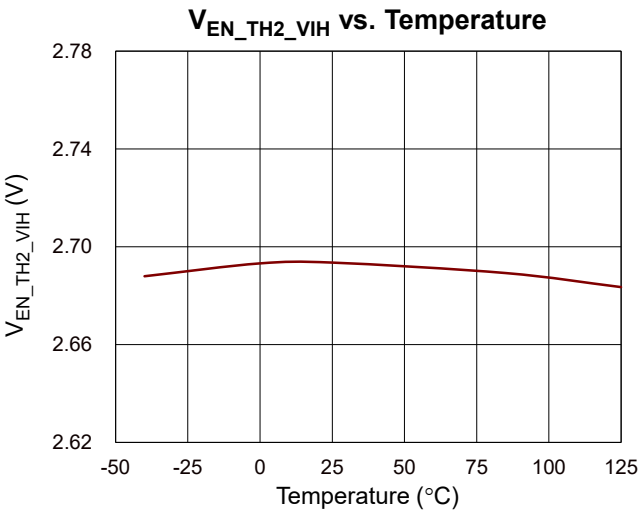
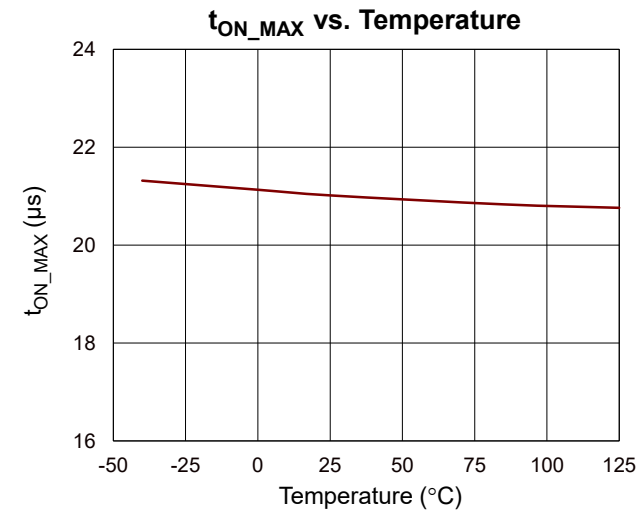


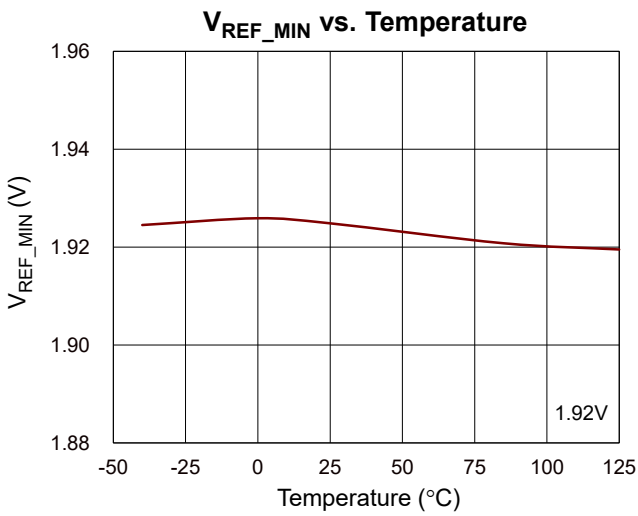












15 Operation

15.1 Critical Conduction Mode (CRM)

Figure 1 shows that CRM operates at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

In CRM, the power switch is turned on immediately after the inductor current decreases to zero. CRM is the preferred control method for medium power (<300W) applications due to its features of zero current switching and a lower peak current compared to DCM.

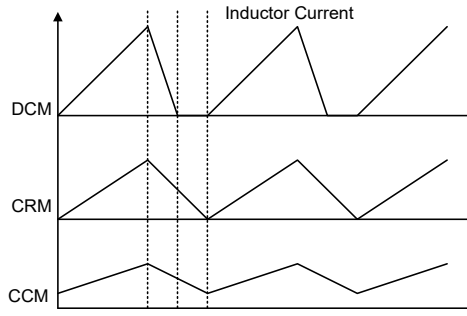


Figure 1. Inductor Current of DCM, CRM, and CCM

15.2 Constant On-Time Voltage Mode Control

Figure 2 shows a typical boost converter. When the MOSFET turns on with a fixed on-time (t_{ON}), the inductor current can be calculated using equation (1).

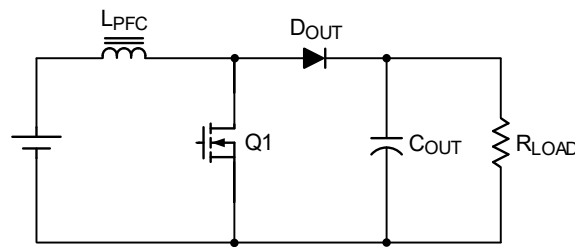


Figure 2. Typical Boost Converter

$$I_{L_PK} = \frac{V_{IN}}{L_{PFC}} \times t_{ON} \quad (1)$$

If the input voltage is a sinusoidal waveform and rectified by a bridge rectifier, the inductor current can be expressed using equation (2). When the converter operates in CRM with constant on-time voltage mode control, the envelope of the inductor peak current will follow (in phase) the input voltage waveform. The average inductor current will be half of the peak current, as shown in Figure 3. Therefore, the near unity power factor can be achieved with this control scheme.

$$I_{L_PK} \times |\sin\theta| = \frac{V_{IN_PK} \times |\sin\theta| \times t_{ON}}{L_{PFC}} \quad (2)$$

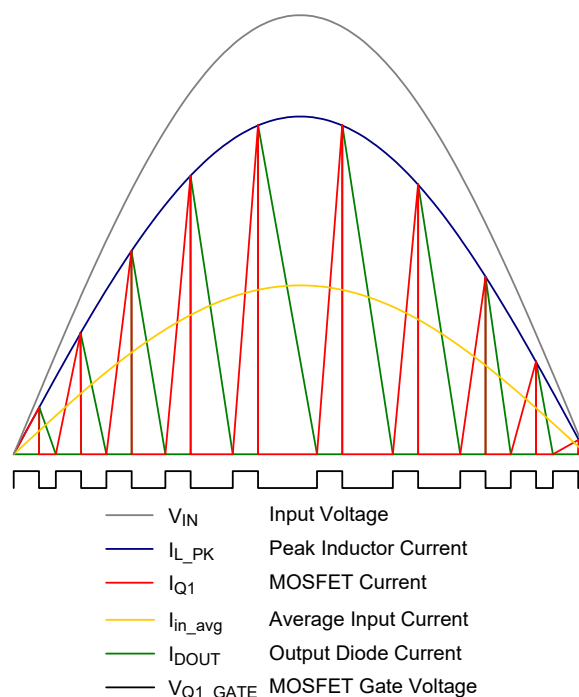


Figure 3. Inductor Current of CRM with Constant On-Time Voltage Mode Control

15.3 Undervoltage-Lockout

The controller will be enabled when VDD exceeds V_{TH_ON} (8V typical) and disabled when VDD drops below V_{TH_OFF} (5.5V typical).

The maximum VDD voltage is set at 37V for overvoltage protection, as shown in [Figure 4](#).

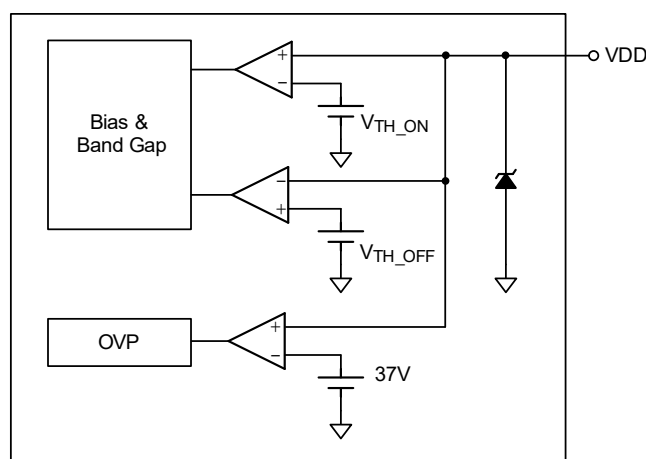


Figure 4. VDD and UVLO

15.4 Output Voltage Detection

Figure 5 shows the output voltage detection circuit. The PFCVO pin is utilized to detect the output voltage for the feedback loop. Overvoltage protection is provided with a threshold voltage of 2.72V. If the PFCVO voltage exceeds 2.72V, the gate driver will be disabled to prevent the output voltage from reaching an overvoltage condition or a feedback open-loop condition. The maximum rated voltage of the bulk capacitor is suggested to be 450V. The PFCVO pin is internally connected to a 2.55MΩ resistor to ground.

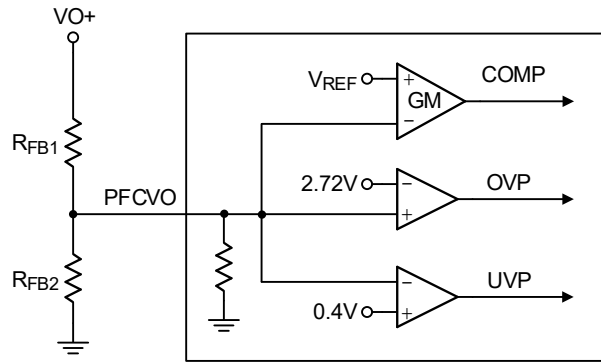


Figure 5. Feedback Voltage Detection

15.5 Transconductance Error Amplifier

The RT7333M incorporates a transconductance error amplifier featuring a non-linear GM design intended to regulate the output voltage and provide a swift response. The transconductance value is 10μA/V under typical operating conditions. When the PFCVO voltage exceeds $V_{REF} + 0.2V$ or drops below $V_{REF} - 0.2V$, the error amplifier's output at the COMP terminal (as depicted in Figure 6) will either source or sink a higher current. This non-linear GM design facilitates a rapid response to dynamic load changes in the PFC converter, even when the feedback loop's bandwidth is lower than the AC line frequency (the frequency compensation is integrated into this IC).

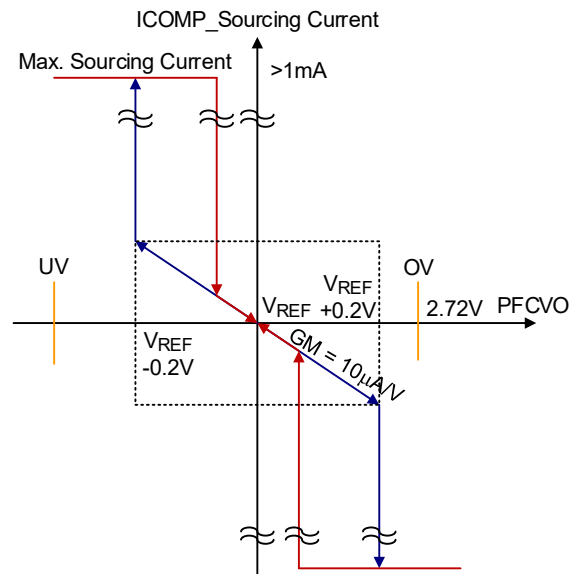


Figure 6. Non-Linear GM

15.6 Feed-Forward Compensation

The ZCD pin is a multifunctional pin. [Figure 7](#) shows the ZCD block diagram. The ZCD block diagram provides VIN feed-forward, zero-current detection, and voltage clamp functions.

The input voltage detector provides a feed-forward signal to compensate for the loop bandwidth.

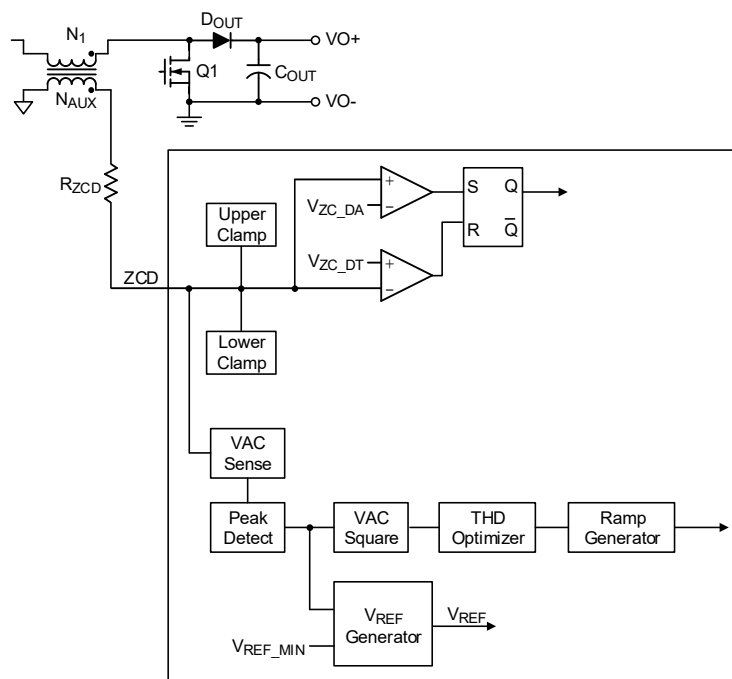


Figure 7. ZCD Detection Circuit

15.7 Valley Switching and Frequency Reduction

When the power switch is turned on, the inductor current will increase linearly to the peak value, as shown in [Figure 8](#). When the power switch is turned off, the inductor current will decrease linearly to zero. The zero current can be detected by the ZCD pin and the auxiliary winding of the inductor.

When the inductor current decreases to zero, the auxiliary winding voltage will change from high to low. Once the ZCD voltage decreases to the V_{ZC_DT} (0.4V) threshold, a valley signal is generated. To protect the ZCD pin from overvoltage, the ZCD pin is clamped to an upper clamp voltage V_{ZC_DH} (4.8V) and a lower clamp voltage V_{ZC_DL} (0.1V).

The RT7333M also provides a ZCD time-out detection function. If the controller operates at a high frequency and no ZCD signal is detected after a 4 μ s delay time, the PWM will be turned on.

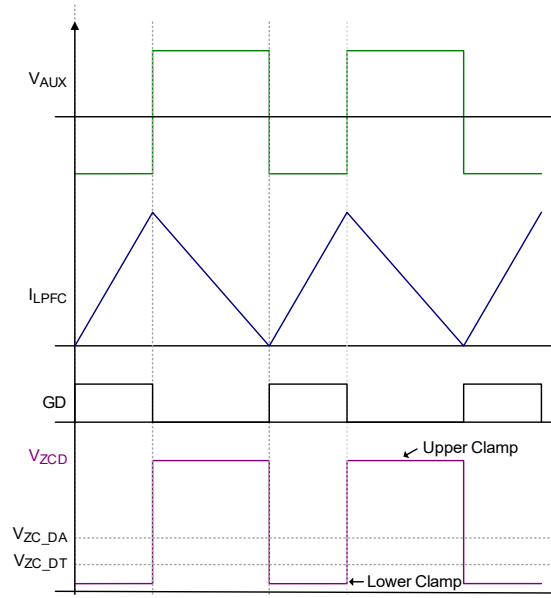


Figure 8. ZCD Related Waveforms

15.8 Ramp Generator

The RT7333M provides constant on-time voltage mode control to achieve a near unity power factor for the PFC.

[Figure 7](#) shows the Ramp Generator with Feed-Forward compensation and THD optimization circuit for constant on-time operation.

15.9 Disable Function

The EN pin provides a disabled function to save power consumption in standby mode. When the EN pin is pulled lower than 750mV, the gate driver will be turned off and operate in standby mode with a low quiescent current of less than 15μA (maximum). Once the EN pin is pulled higher than 2.7V, the controller will be activated. The EN pin is internally connected to a 250kΩ resistor (REN_PULL_L) to ground. A 3ms soft start function is embedded in RT7333M when the VDD and EN voltages exceed their threshold on voltages.

15.10 Tracking Boost

The tracking boost technique is used to optimize efficiency and reduce inductor size. The tracking boost is divided into two types: linear, as shown in [Figure 9 \(a\)](#), and two-stage, as shown in [Figure 9 \(b\)](#). The input voltage is continuously detected, and VREF is updated through the ZCD pin with an update period of 13ms.

In the linear curve, VREF linearly increases in proportion to the input voltage from 90Vac to 265Vac. In the two-stage curve, VREF separates the low line and high line at the IZC_TWO point.

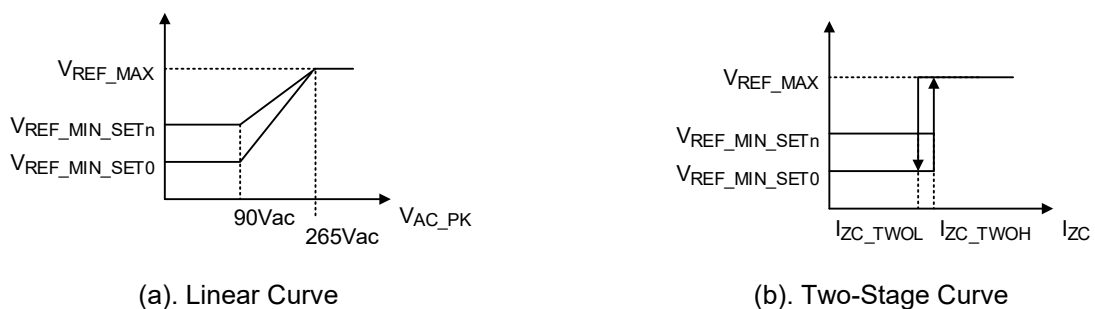


Figure 9.

16 Application Information

(Note 7)

16.1 Multi-Mode PFC

The RT7333M is a multi-mode PFC boost controller, designed to achieve high efficiency by tracking boost and valley switching. In addition, the RT7333M can automatically switch among control modes to optimize efficiency for the system operating under various load conditions, as shown in [Figure 10](#).

As the load decreases, the controller may enter different modes, such as the frequency reduction mode or burst mode.

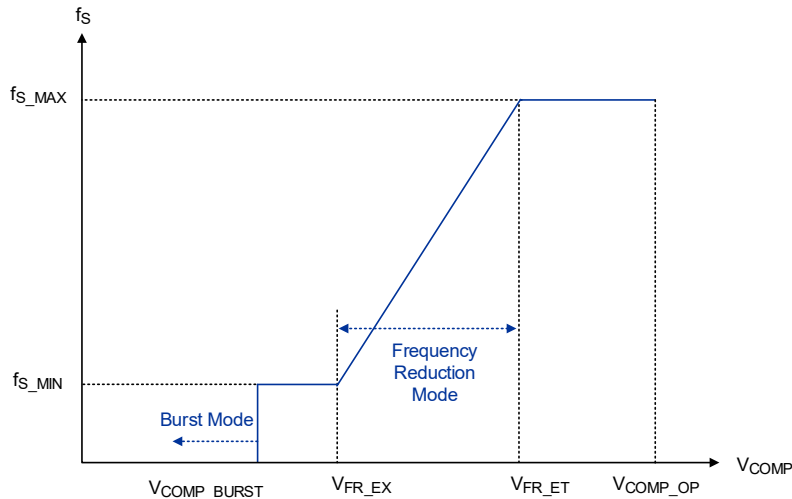


Figure 10. Operating Mode

16.2 LPFC Setting

The boost inductor LPFC can be calculated as shown in Equation (3):

$$L_{PFC} \leq \frac{V_{COMP_SET}}{R_{N_MAX} \times g_{m_{ramp}} \times K_A} \quad (3)$$

where

$$V_{COMP_SET} = 2.1V$$

$$g_{m_{ramp}} = 5\mu A/V \text{ (RT7333MS-MLAA, MTAA, MTBA, and MTDA); } 3\mu A/V \text{ (RT7333MS-MTCA)}$$

$$K_A = 25.2M$$

16.3 Feed-Forward Setting and Input Voltage Detection

The input voltage is detected through the ZCD pin. The R_{ZCD} can be calculated as shown in Equation (4):

$$R_{ZCD} = K \times N_{AUX} / N_1 \quad (4)$$

where

$$K = 781.25k$$

$$N_{AUX} / N_1 > 1.5V / (V_{O_MAX} - V_{IN_MAX})$$

The N_{AUX} / N_1 ratio is used for the detection of the zero current cross signal.

The ZCD current I_{ZC} can be calculated as follows:

$$I_{ZC} = (V_{IN} \times N_{AUX} / N_1 + 0.1) / R_{ZCD}$$

16.4 Tracking Boost Setting

The tracking boost voltage is set by the SET pin, as shown in [Figure 11](#). The RSET is used to select the minimum reference voltage (VREF_MIN) level, as shown in [Table 1](#). There are four levels to choose from.

A 1% resistor tolerance for RSET is recommended.

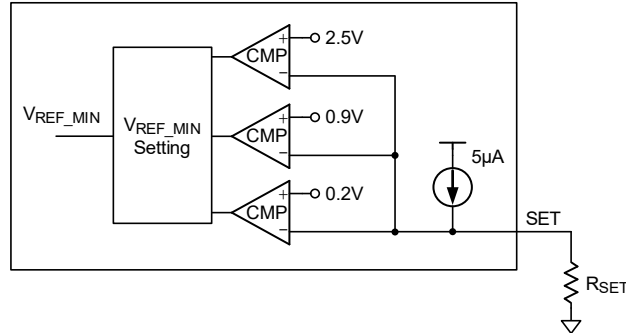


Figure 11. Tracking Boost Selector

Table 1. Programmable Tracking Boost Minimum Reference Voltage Level Setting

RSET (Ω)	VSET (V)	VREF_MIN (V)	VO_MIN (V)
Open	>2.5	2.5	390
Short	<0.2	1.6	250
330k	0.9 < VSET < 2.5	1.92	300
100k	0.2 < VSET < 0.9	1.28	200

16.5 Maximum Frequency Setting

The CS pin is applied to set the maximum current limit and maximum frequency respectively, by RCS and RFS. The threshold voltage at the CS pin is typically 0.4V. The current sense resistor can be calculated using equation (5) with the peak current of the MOSFET.

$$R_{CS} = \frac{0.4V \times OCP\%}{I_{L_PK}} \quad (5)$$

The maximum frequency setting function is shown in [Figure 12](#). The RT7333M provides a sourcing current from the CS pin, and the voltage can be calculated as the current value multiplied by the resistance. When the setting voltage is higher, the maximum switching frequency is lower; when the setting voltage is lower, the maximum switching frequency is higher. The RT7333M has four maximum switching frequency levels, as shown in [Table 2](#). A 1% resistor tolerance for RFS is recommended for setting the maximum switching frequency.

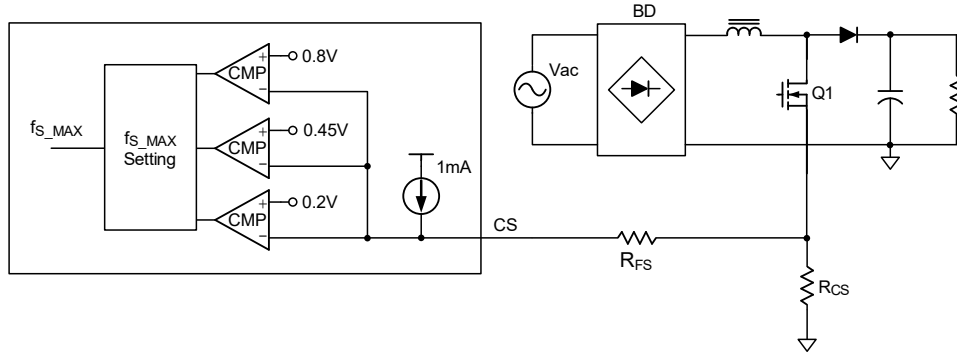


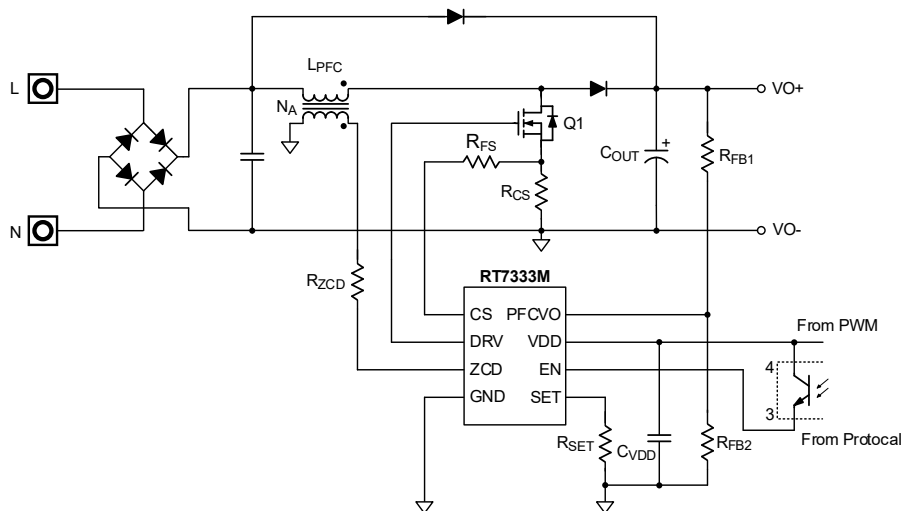
Figure 12. Maximum Switching Frequency Setting

Table 2. Programmable Maximum Switching Frequency Level Setting

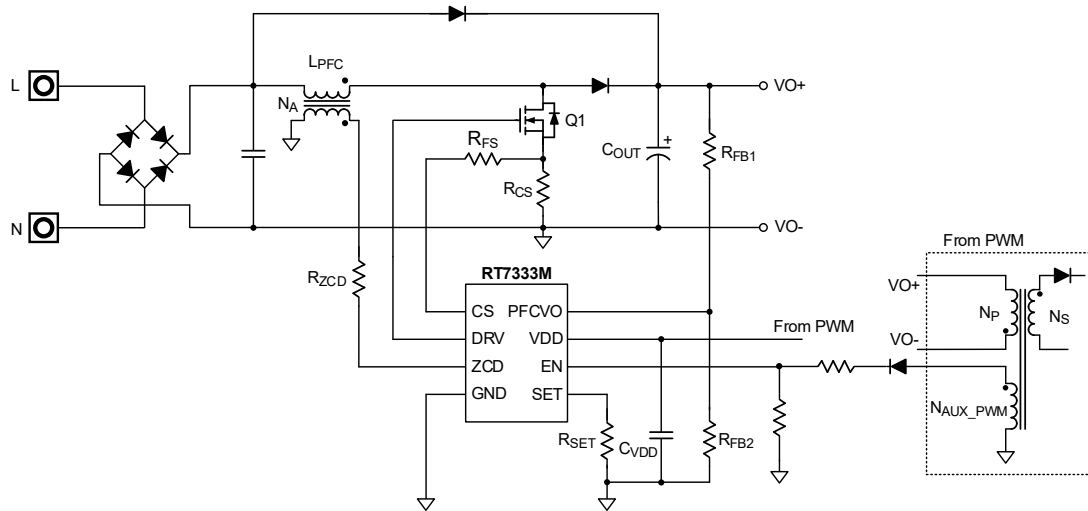
$R_{FS} (\Omega)$	$V_{CS} (V)$	$f_{S_MAX} (kHz)$	$f_{S_MIN} (kHz)$
$1k \pm 1\%$	> 0.8	130	30
$620 \pm 1\%$	$0.45 < V_{CS} < 0.8$	176	76
$330 \pm 1\%$	$0.2 < V_{CS} < 0.45$	246	46
$100 \pm 1\%$	$V_{CS} < 0.2$	397	197

16.6 Disable Function Setting

The disabled function is utilized to disable the PFC. It includes two thresholds: V_{EN_TH1} and V_{EN_TH2} . When the EN pin is set lower than V_{EN_TH2} , the RT7333M will stop switching and operate in standby mode. When the EN pin is set lower than V_{EN_TH1} , the RT7333M will be turned off for further power saving. The application circuits are shown in [Figure 13 \(a\)](#) and [Figure 13 \(b\)](#).



(a) EN Enable by Protocol IC



(b) EN Enable by PWM AUX. Winding Voltage

Figure 13.

16.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA} , is 188°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as follows:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (188^\circ\text{C/W}) = 0.53\text{W for a SOP-8 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in [Figure 14](#) allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

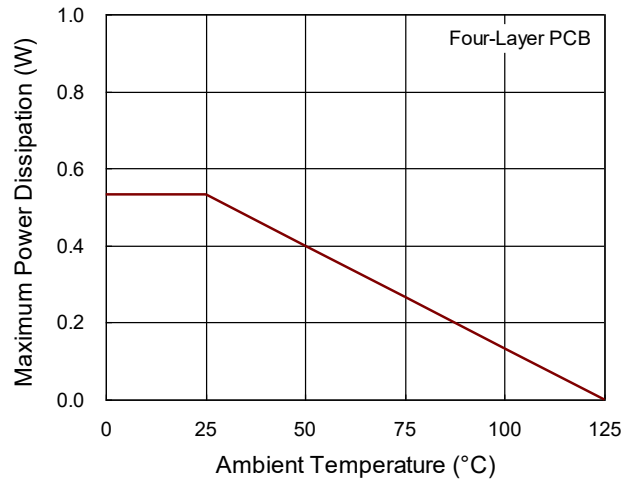


Figure 14. Derating Curve of Maximum Power Dissipation

16.8 Layout Considerations

A proper PCB layout can mitigate unknown noise interference and EMI issues in the switching power supply. Refer to the following guidelines when designing a PCB layout for a switching power supply.

- The current path (1) from input capacitor, inductor, MOSFET, and Rcs, returning to the input capacitor, and the current path (2) from input capacitor, inductor, output diode, and output filter capacitor, returning to the input capacitor are high-frequency current loops. The path (3) from the DRV pin, through the MOSFET, Rcs to ground, is also a high frequency-current loop. They must be as short as possible to decrease noise coupling and should be kept separate from other low voltage traces, such as IC control circuit paths. Additionally, the path between MOSFET ground (b) and IC ground (d) is recommended to be as short as possible.
- It is beneficial for reducing noise, output ripple, and EMI issues to separate ground traces of the input capacitor (a), MOSFET (b), auxiliary winding (c), IC control circuit (d), and bulk (e). Auxiliary winding ground (c) should be individually connected to the bulk ground (e). Connect the MOSFET ground (b) and IC control circuit ground (d) to the bulk ground (e). Finally, connect bulk ground (e) to the input capacitor ground (a). The areas of these ground traces should be kept large.

In addition, apply sufficient copper area at the anode and cathode terminals of the diode for heat-sinking. It is recommended to apply a larger area at the quiet cathode terminal. A large anode area will induce high-frequency radiated EMI.

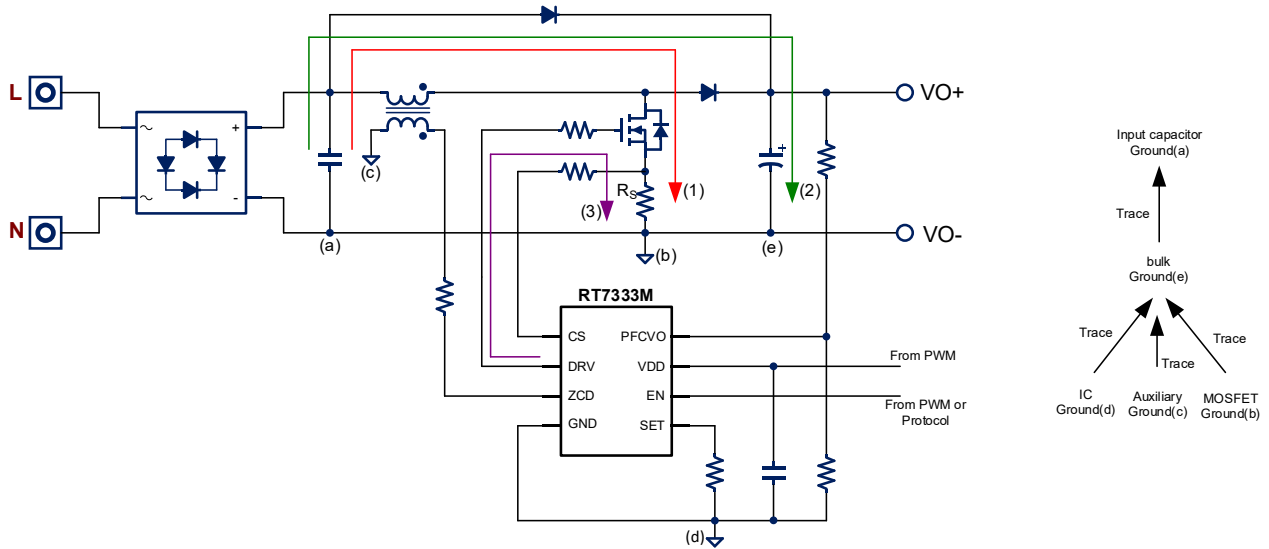
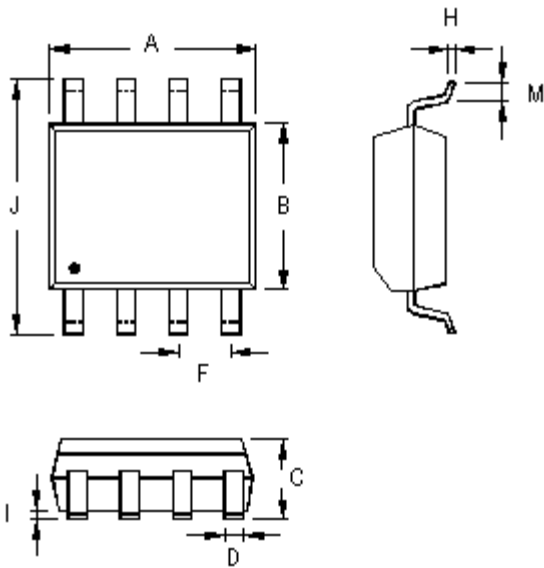


Figure 15. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

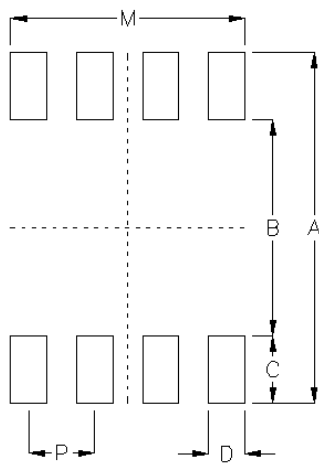
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

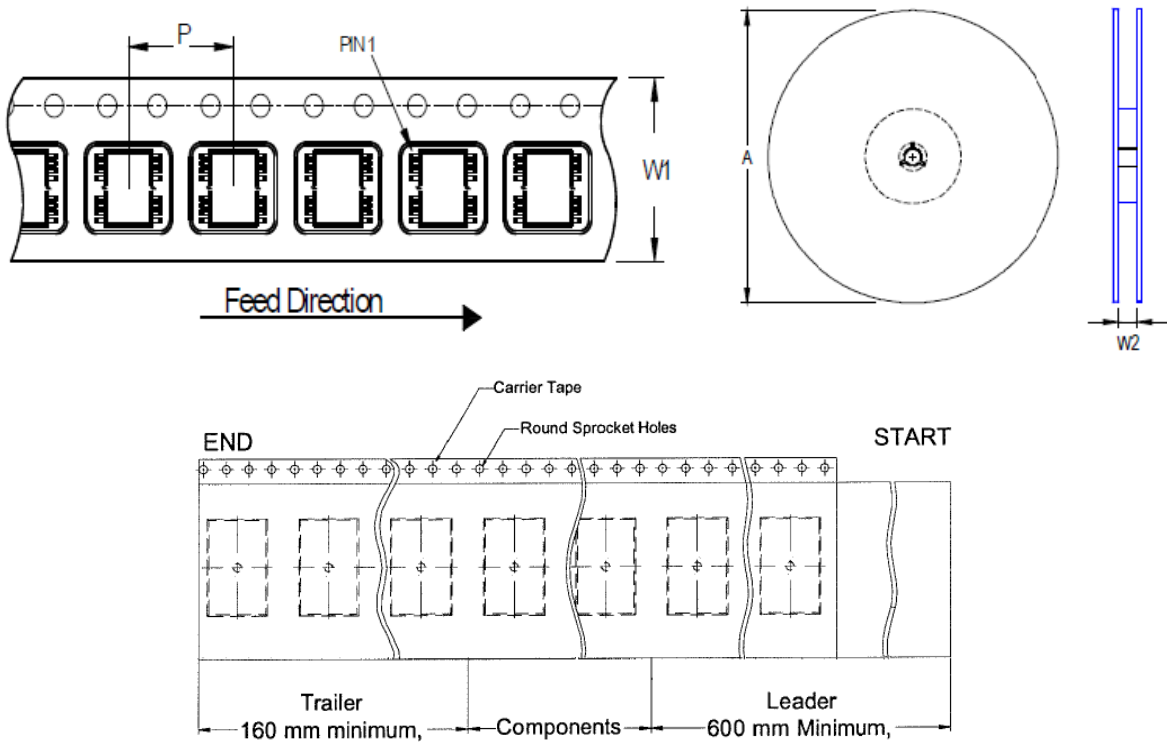
18 Footprint Information



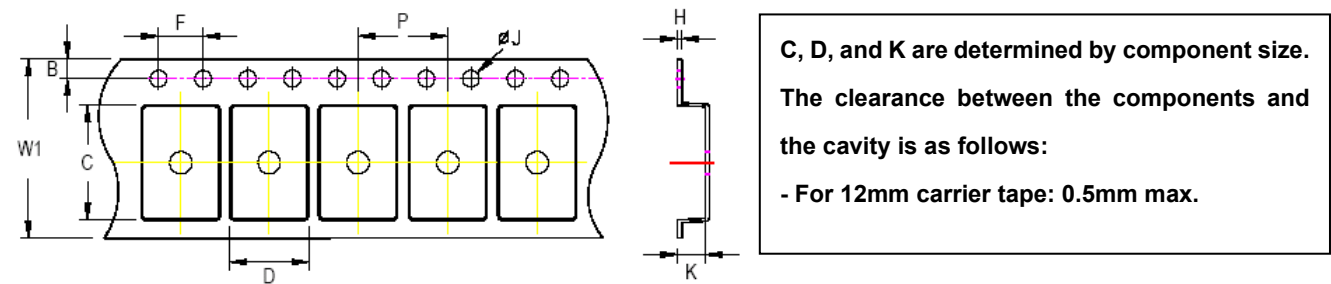
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8/SOP-8(FC)	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
SOP-8	12	8	330	13	2,500	160	600	12.4/14.4



Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.2mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13"	4	 1 reel per inner box Box G
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box Carton A

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-8	13"	2,500	Box G	1	2,500	Carton A	6	15,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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20 Datasheet Revision History

Version	Date	Description
00	2025/2/27	First Edition
01	2025/3/18	Modify (Added RT7333M-MTB) <i>RT7333M Version Table on page 2</i> - Added RT7333M-MTB <i>Electrical Characteristics on page 6</i> - Modified the specification of VPFCVO_UVP - Updated the test condition of VPFCVO_UVP_HYS <i>Typical Operating Characteristics on page 12</i> - Added VPFCVO_UVP curve for RT7333M-MTB <i>Application Information on page 22</i> - Added section 17.2
02	2026/8/14	Ordering Information Marking Information - Added product number RT7333MS-MTCA and RT7333MS-MTDA Electrical Characteristics - Added RT7333MS-MTCA and RT7333MS-MTDA to PFCVO UVP Threshold Voltage (Output Short Protection) for different test conditions - Added RT7333MS-MTCA and RT7333MS-MTDA to Gate Output Clamping Voltage for certain test condition Typical Operating Characteristics - Added RT7333M-MTC and RT7333M-MTD to VPFCVO_UVP VS. Temperature for different test conditions LPFC Setting - Distinguished RT7333MS-MLAA, MTAA, MTBA, and MTDA for 5μA/V and RT7333MS-MTCA for 3μA/V Layout Considerations - Updated descriptions and the figure Tape and Reel Data - Modified maximum carrier tape