Programmable Burst Switching Green Mode/Burst Mode Level Flyback Controller

General Description

The RT7737 series are enhanced high efficient PWM flyback controller with proprietary SmartJitter™ technology. The innovative SmartJitter™ technology not only reduces the EMI emissions of SMPS when the system enters burst switching green mode, but also eliminates the output jittering ripple. Also, the RT7737 series feature programmable burst switching green mode and burst mode level for adopting different application requirements to optimize the product performance. To meet the stringent trend toward performance, the RT7737 series are the best choice for product designers.

The RT7737 is available in SOT-23-6 package. It is a current mode PWM controller providing comprehensive protection functions, including an input Under-Voltage Lockout (UVLO), a VDD Over-Voltage Protection (OVP), an Over-Load Protection (OLP), a Secondary Rectifier Sort Protection (SRSP), a CS pin open protection and a cycle-by-cycle current limit. With the above features, the RT7737 is a cost-effective and compact solution for AC/DC products.

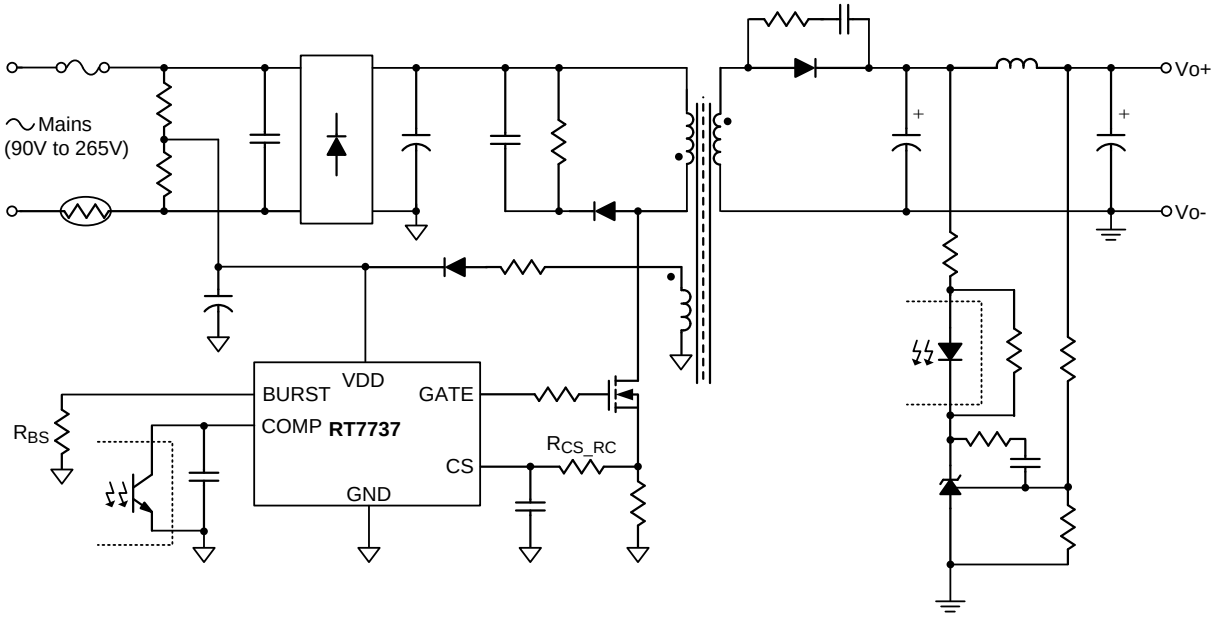
Features

- **Proprietary SmartJitter™ Technology**
  - **Reducing EMI Emissions of SMPS**
  - **Output Jittering Ripple Elimination**
- **Programmable Burst Switching Green Mode Level**
- **Programmable Burst Mode Level**
- **Accurate Over Load Protection**
- **Driver Capability : 200mA/–300mA**
- **High Noise Immunity**

Applications

- Switching AC/DC Adaptor
- DVD Open Frame Power Supply
- Set-Top Box (STB)
- ATX Standby Power
- TV/Monitor Standby Power
- PC Peripherals
- NB Adaptor

Simplified Application Circuit



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Ordering Information

RT7737□□□

- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- RT7737 Version (Refer to Version Table)

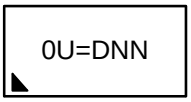
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT7737GGE



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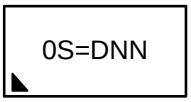
DNN : Date Code

RT7737LGE



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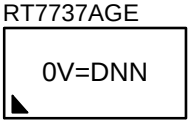
RT7737AGE



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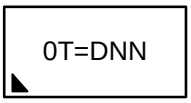
RT7737HGE



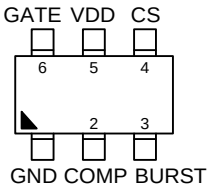
0T= : Product Code
DNN : Date Code

RT7737 Version Table

Version	RT7737G	RT7737L	RT7737A	RT7737H
Frequency (f_{OSC})	65kHz	65kHz	65kHz	100kHz
OLP Delay Time @ f_{OSC}	55ms	55ms	28ms	36ms
Internal OVP	Auto Recovery	Latch	Latch	Auto Recovery
OLP & SRSP	Auto Recovery	Auto Recovery	Latch	Auto Recovery
BURST Pin High	Latch	Latch	Latch	Latch
BURST Pin Low	Auto Recovery	Auto Recovery	Latch	Auto Recovery

Pin Configurations

(TOP VIEW)



SOT-23-6

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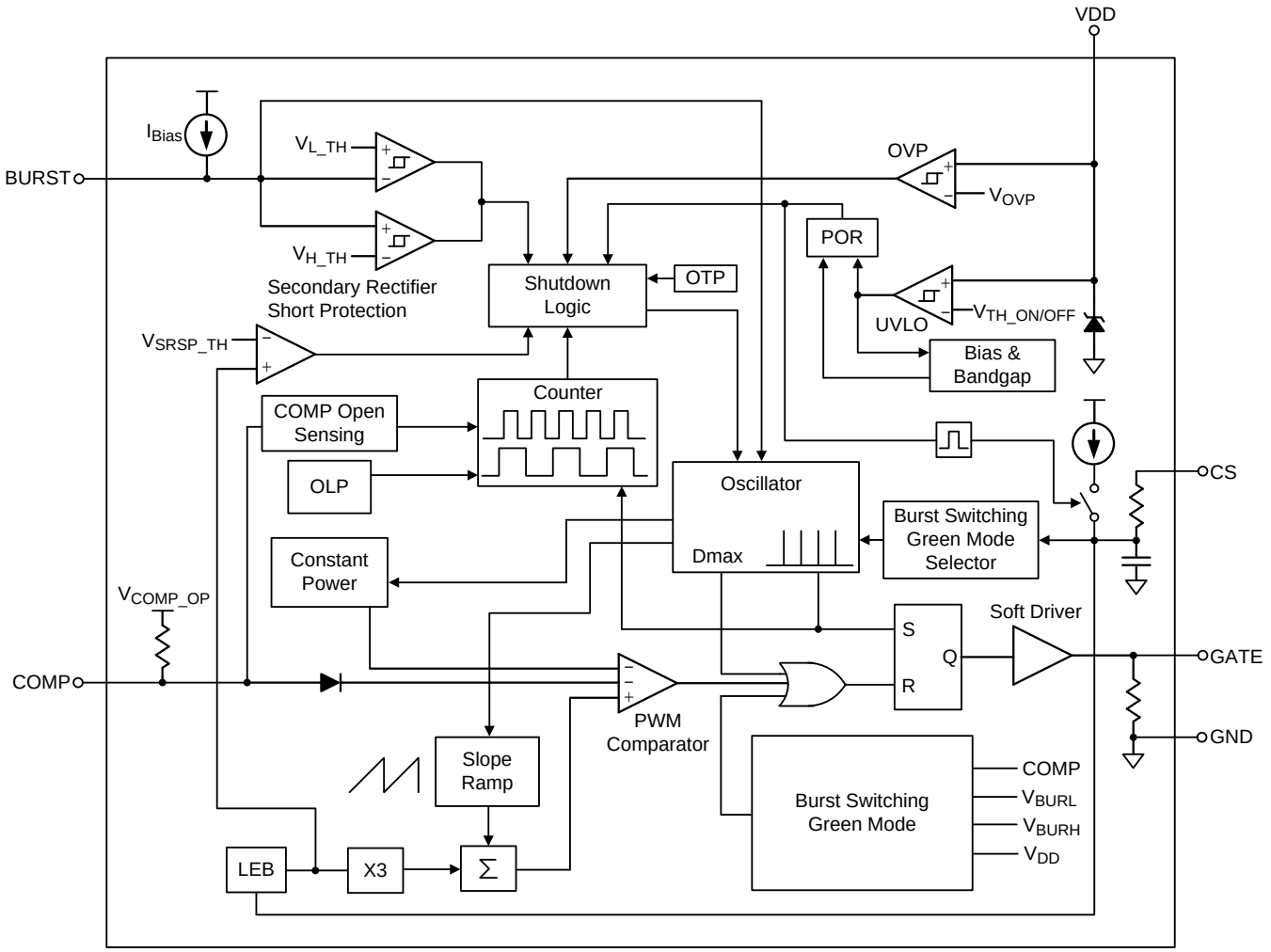
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground of the Controller.
2	COMP	Feedback Voltage Input. Connect an opto-coupler to close the control loop and achieve output voltage regulation.
3	BURST	Burst Mode Level Setting.
4	CS	Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting.
5	VDD	Supply Voltage Input. The controller will be enabled when VDD exceeds V_{TH_ON} and disabled when VDD decreases lower than V_{TH_OFF}.
6	GATE	Gate Driver Output for External Power MOSFET.

Function Block Diagram



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Operation

Burst Switching Green Mode

The burst mode is designed to reduce switching loss at light load condition. When the output load gets light, the COMP voltage drops and reaches V_{BURL}, the controller will cease switching. After the output voltage drops and the COMP voltage goes up to V_{BURH}, the controller will resume switching.

VDD Holdup Mode

The RT7737 provides a unique operation mode at almost no load condition named VDD holdup mode. Under the VDD holdup mode, the RT7737 forces PWM switching to maintain V_{DD} voltage between V_{DD_ET} and V_{DD_ED}. The benefit of the VDD holdup mode is to avoid the V_{DD} drops to V_{TH_OFF} due to the long burst mode period at no load or load transient moment. Therefore, this function makes bias winging design and transient design easier and compacter.

Oscillator

The oscillator runs at 65kHz and features frequency jittering function. The saw-tooth slope compensation, maximum duty cycle pulse and over-load protection slope are built-in. Its jitter depth is proportion of oscillator frequency where Δf is frequency jittering range, and T_{JIT} is frequency jittering period.

Leading Edge Blanking (LEB)

To prevent unexpectedly gate switching interruption from the initial spike on CS pin, the LEB delay is designed to block this spike at the beginning of gate switching.

Gate Driver

A totem pole gate driver is designed to meet both EMI and efficiency requirements in low power applications. An internal pull-low circuit is activated after pretty low V_{DD} to prevent external MOSFET from accidentally turning on during UVLO.

Programmable Burst Switching Green Mode Level

The burst switching green mode level can be set by connecting a recommended resistor between the CS pin and the current sense resistor.

BURST Pin – Programmable Burst Mode Level

The burst mode level can be set by connecting a recommended resistor on the BURST pin and GND to decide the burst mode threshold.

Over-Load Protection

In over-load conditions, current limit for a long time will lead to system thermal stress problem. To further protect the system, the RT7737 is designed with a proprietary prolonged turn-off period during hiccup. The power loss and temperature during OLP are averaged to an acceptable level over the ON/OFF cycle.

CS Pin Open Protection

When the CS pin is opened, the controller will shut down after a few cycles.

Internal VDD Over-Voltage Protection

Output voltage can be roughly sensed by the VDD pin. If the sensed voltage reaches V_{OVP} threshold, the controller shuts down after deglitch delay.

Feedback Open or Opto-Coupler Short

If the output voltage feedback loop is open or the opto-coupler is shorted, the OVP/OLP function will be triggered depending on which one occurs first.

Secondary Rectifier Short Protection

The current spike during secondary rectifier short test is extremely high because of the saturated main transformer. Meanwhile, the transformer acts like a leakage inductance. During high line, the current in power MOSFET is sometimes too high in OLP delay time. To offer better and easier protection design, the RT7737 shuts down after a few of cycles before fuse is impacted.

Output Short Protection

The RT7737 implements output short protection by detecting GATE width and delay time. It can minimize the power loss and temperature during output short, especially at high line input voltage.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 30V
- GATE to GND ---------- –0.3V to 16.5V
- BURST, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2.5kV
  MM (Machine Model) ---------- 250V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 12V to 25V
- Recommended Resistance on the BURST Pin ---------- 10kΩ to 60kΩ
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
V_{DD} Over-Voltage Protection Level	V_{OVP}		26	27	28	V
V_{DD} Zener Clamp	V_Z		29	--	--	V
On Threshold Voltage	V_{TH_ON}	RT7737G/L/H	12.5	13.5	14.5	V
		RT7737A	14.5	15.5	16.5	
Off Threshold Voltage	V_{TH_OFF}		8.5	9	9.5	V
V_{DD} Holdup Mode Entry Point	V_{DD_ET}	V_{COMP} < 1.3V	9.5	10	10.5	V
V_{DD} Holdup Mode Ending Point	V_{DD_ED}	V_{COMP} < 1.3V	10	10.5	11	V
Latch-off Clamping Voltage	V_{DD_LH}		--	6	--	V
Threshold Voltage for Latch-off Release	V_{LH_OFF}		--	5.5	--	V

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Start-up Current	I_{DD_ST}	V_{DD} < V_{TH_ON} – 0.1V, T_A = –40°C to 85°C	RT7737G/L/H	--	5	10	μA
			RT7737A	--	5	12	
Latch-off Operating Current	I_{DD_LH}	T_A = –40°C to 85°C	RT7737G/L/H	--	--	10	μA
			RT7737A	--	--	12	
Operating Supply Current	I_{DD_OP1}	GATE pin open, V_{COMP} = 2.5V		--	1	--	mA
	I_{DD_OP2}	GATE pin open, V_{COMP} = 1.7V		--	0.9	--	
I_{DD} Sinking Current	I_{DD_ARP}	During entering auto recovery protection, T_A = –40°C to 85°C		350	550	750	μA
Oscillator Section							
Normal PWM Frequency	f_{OSC}	V_{COMP} > V_{BS_ET}	RT7737G/L/A	60	65	70	kHz
			RT7737H	92	100	108	
Maximum Duty Cycle	DCY_{max}			70	75	80	%
Minimum Burst Switching Frequency	f_{BS_MIN}	V_{COMP} < V_{BS_ED}	RT7737G/L/A	18.5	22	25.5	kHz
			RT7737H	20	25	30	
PWM Frequency Jittering Range	Δf			--	±6	--	%
PWM Frequency Jittering Period	T_{JIT}	f_{OSC} = 65kHz		--	16	--	ms
		f_{OSC} = 100kHz		--	10.4	--	
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 9V to 23V		--	--	2	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = –30°C to 105°C		--	--	5	%
COMP Input Section							
Open Loop Voltage	V_{COMP_OP}	COMP pin open		5	5.2	5.4	V
Short Circuit Current of COMP	I_{ZERO}	V_{COMP} = 0V		0.24	0.29	0.34	mA
Delay Time of COMP Open-loop Protection	T_{OLP}	f_{OSC} = 65kHz	RT7737G/L	--	55	--	ms
		f_{OSC} = 65kHz	RT7737A	--	28	--	
		f_{OSC} = 100kHz	RT7737H	--	36	--	
Burst Switching Green Mode Entry Voltage	V_{BS_ET}	R_{CS_RC} = 750Ω		--	2.75	--	V
		R_{CS_RC} = 510Ω		--	2.65	--	
		R_{CS_RC} = 330Ω		--	2.55	--	
		R_{CS_RC} = 200Ω		--	2.45	--	
		R_{CS_RC} = 100Ω		--	2.35	--	
Burst Switching Green Mode Ending Voltage	V_{BS_ED}	R_{CS_RC} = 750Ω		--	2.35	--	V
		R_{CS_RC} = 510Ω		--	2.25	--	
		R_{CS_RC} = 330Ω		--	2.15	--	
		R_{CS_RC} = 200Ω		--	2.05	--	
		R_{CS_RC} = 100Ω		--	1.95	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Delay Time of Output Short Protection	T_{D_OSP}	RT7737G/L/A; f_{OSC} = 65kHz	--	8	--	ms
		RT7737H; f_{OSC} = 100kHz	--	5.2	--	
Current Sense Section						
Maximum Current Limit	V_{CS_MAX}	(Note 6)	1.05	1.1	1.15	V
Leading Edge Blanking Time	T_{LEB}	(Note 5)	250	400	550	ns
Internal Propagation Delay Time	T_{PD}	(Note 5)	--	100	--	ns
Minimum On-Time	T_{ON_MIN}		350	500	650	ns
SRSP Threshold Voltage	V_{SRSP_TH}	RT7737G/L/A (Note 6)	1.9	2	2.1	V
		RT7737H (Note 6)	2.5	2.6	2.7	
Detection On-Time of Output Short Protection	T_{ON_OSP}	f_{OSC} = 65kHz	0.9	1.1	1.3	μs
		f_{OSC} = 100kHz	0.5	0.65	0.8	
GATE Section						
Rising Time	T_R	C_L = 1nF	--	250	--	ns
Falling Time	T_F	C_L = 1nF	--	40	--	ns
Gate Output Clamping Voltage	V_{CLAMP}	V_{DD} = 23V	--	14	--	V
BURST Pin						
High-Level Threshold Voltage	V_{H_TH}		2.95	3	3.05	V
Low-Level Threshold Voltage	V_{L_TH}		0.25	0.3	0.35	V
Burst Mode Entry Voltage	V_{BURST_ET}	R_{BS} = 60kΩ	--	1.65	--	V
		R_{BS} = 10kΩ	--	1.15	--	
Burst Mode Ending Voltage	V_{BURST_ED}	R_{BS} = 60kΩ, V_{BURST_ED} = V_{BURST_ET} + 0.2V	--	1.85	--	V
		R_{BS} = 10kΩ, V_{BURST_ED} = V_{BURST_ET} + 0.2V	--	1.35	--	
Over-Temperature Protection (OTP) Section						
OTP Before Turn On	T_{OTP_INTH}	Built-in OTP (Note 6)	--	120	--	°C
OTP After Turn On	T_{OTP_STTH}	Built-in OTP (Note 6)	--	140	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in natural convection (still air) at T_A = 25°C with the component mounted on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Leading edge blanking time and internal propagation delay time are guaranteed by design.

Note 6. Guaranteed by design.

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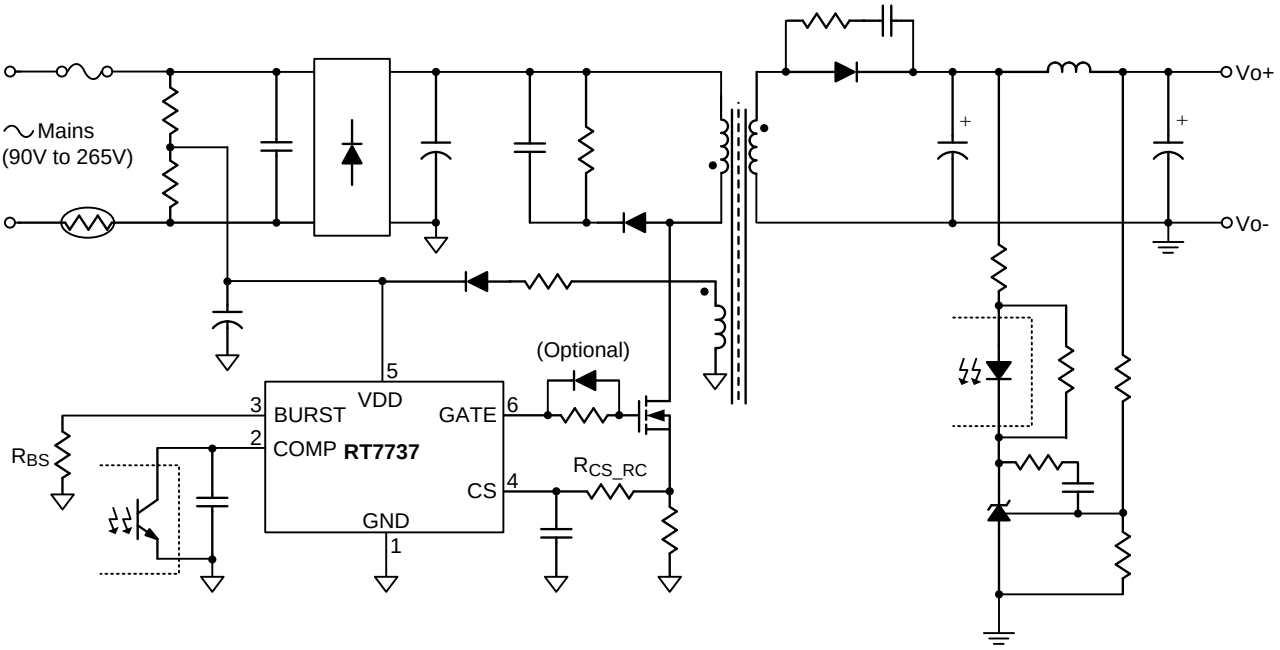
Typical Application Circuit



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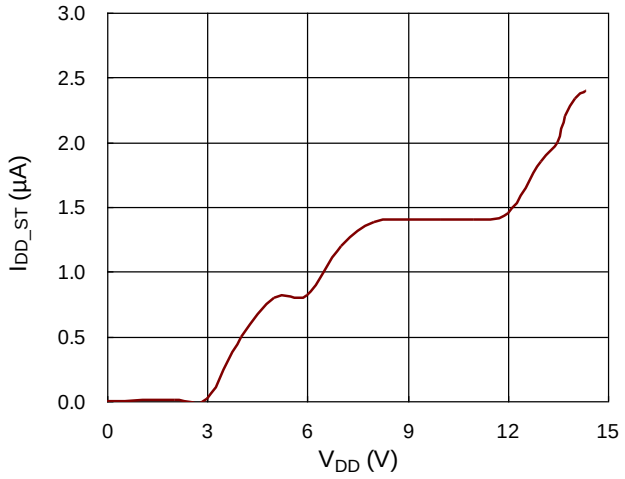
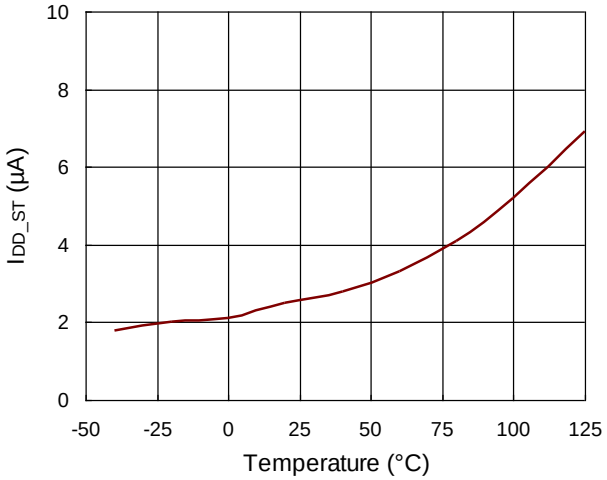
Typical Operating Characteristics

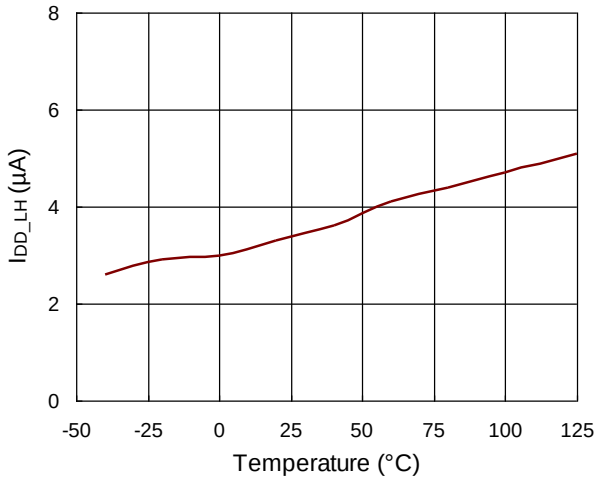
I_{DD_ST} vs. V_{DD}



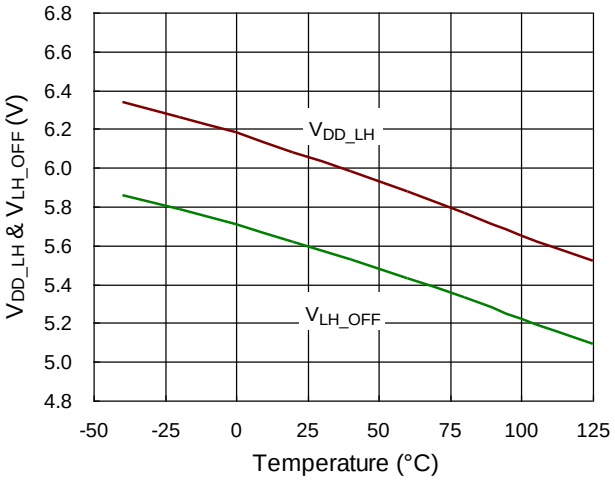
I_{DD_ST} vs. Temperature



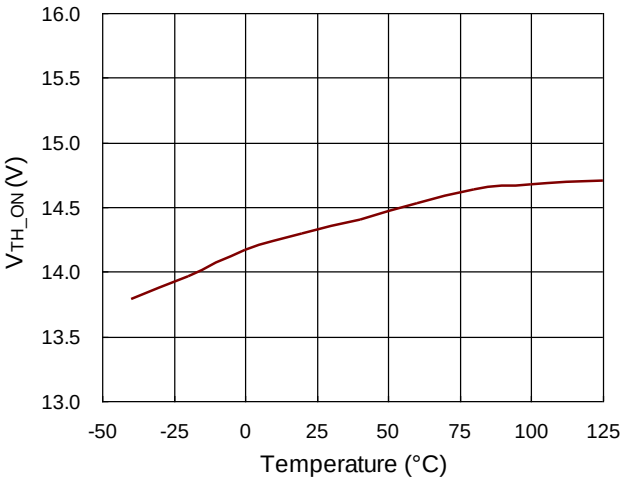
I_{DD_LH} vs. Temperature



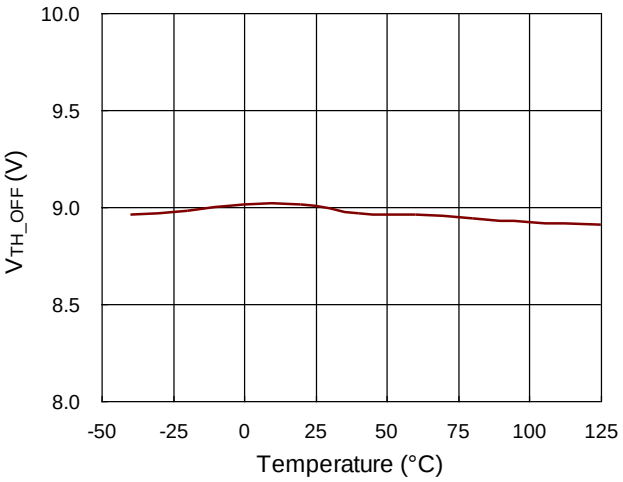
V_{DD_LH} & V_{LH_OFF} vs. Temperature



V_{TH_ON} vs. Temperature



V_{TH_OFF} vs. Temperature



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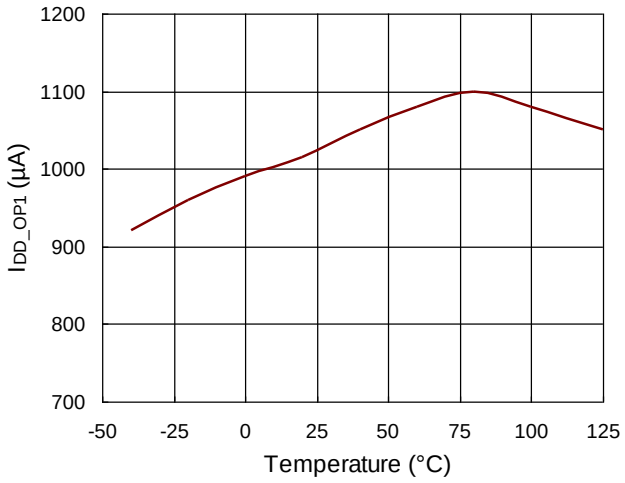
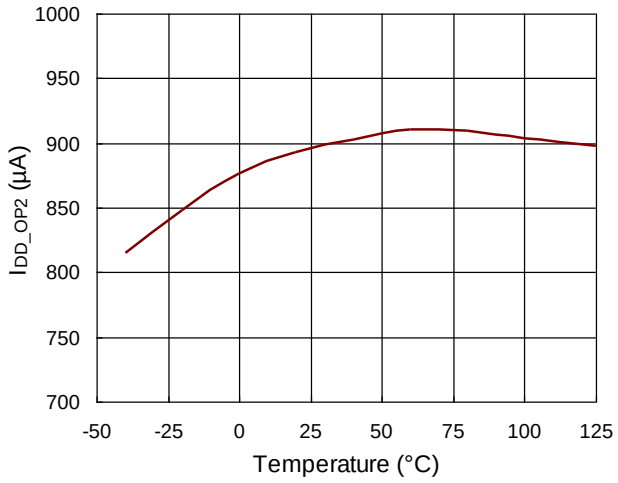
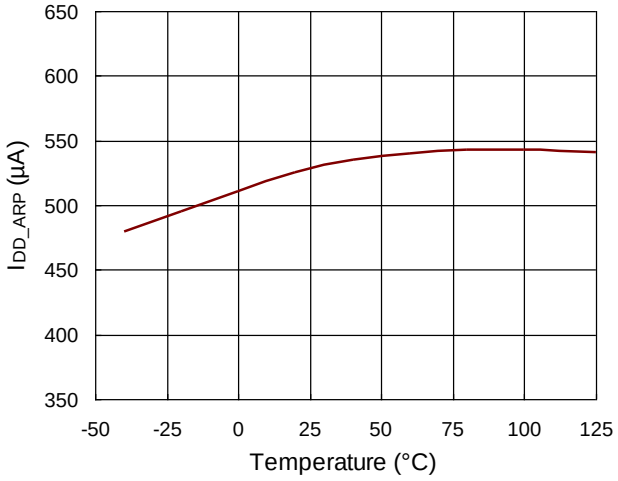
I_{DD_OP1} vs. Temperature



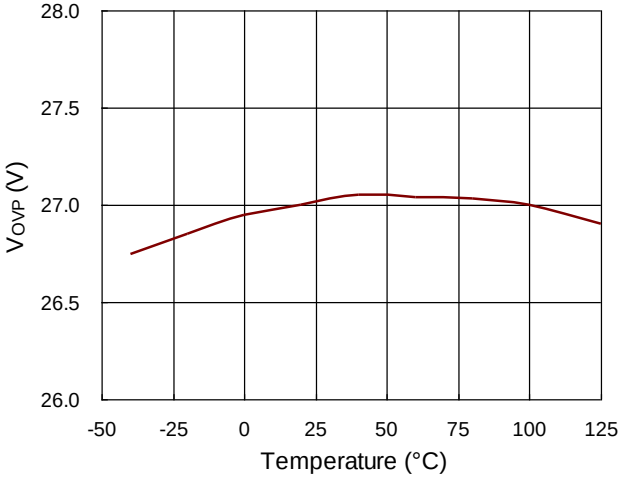
I_{DD_OP2} vs. Temperature



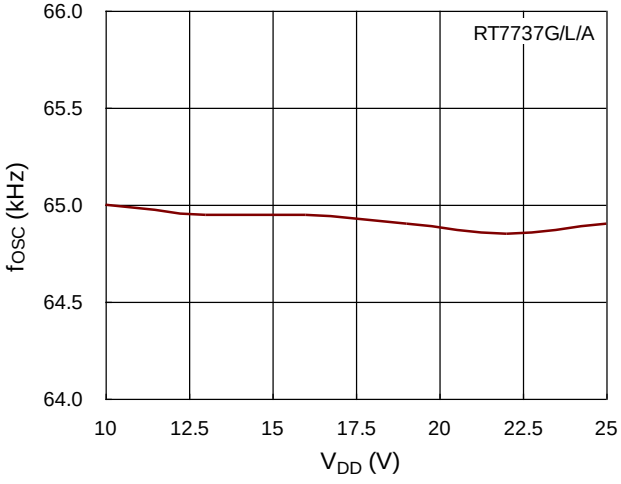
I_{DD_ARP} vs. Temperature



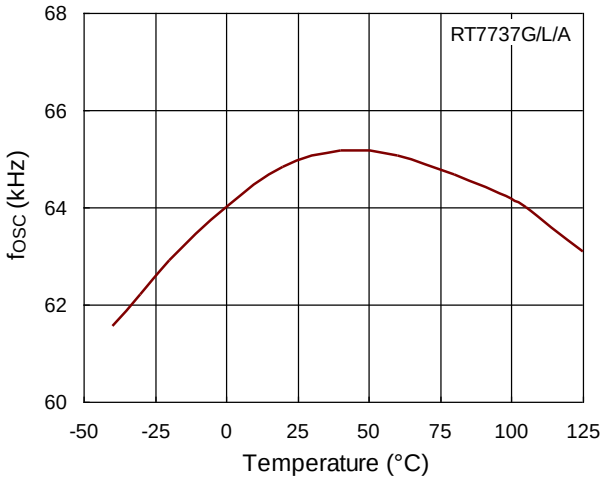
V_{OVP} vs. Temperature



f_{OSC} vs. V_{DD}



f_{OSC} vs. Temperature



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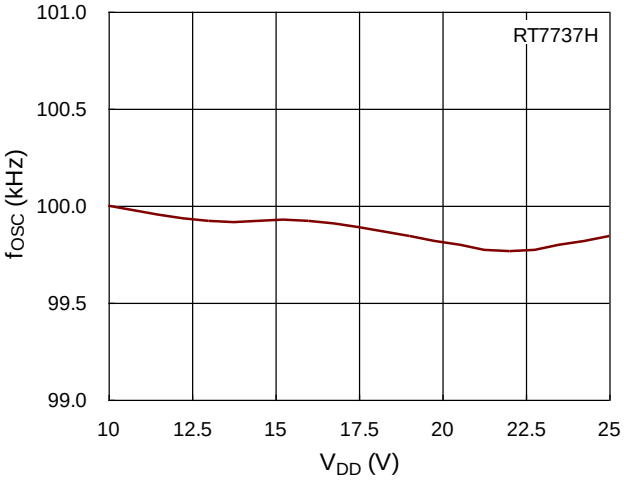
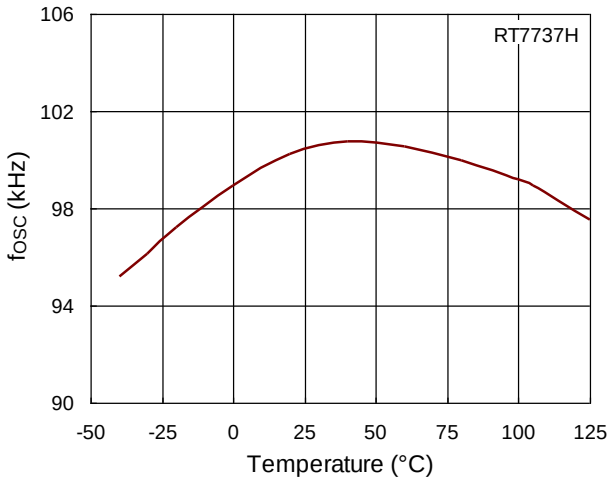
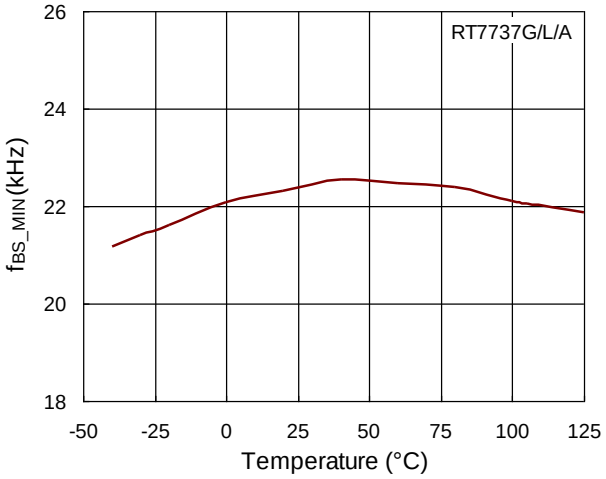
f_{OSC} vs. V_{DD}



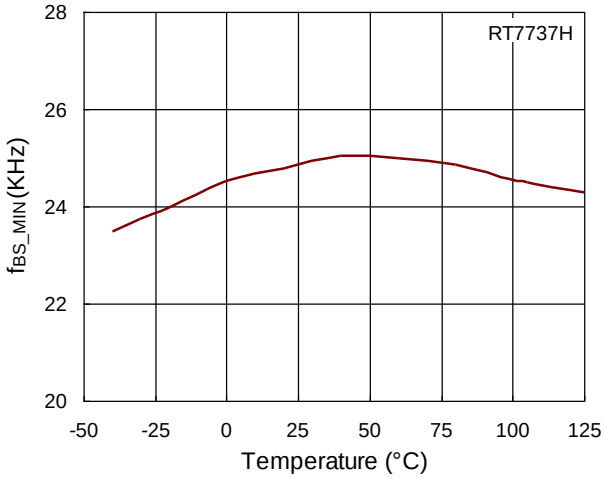
f_{OSC} vs. Temperature



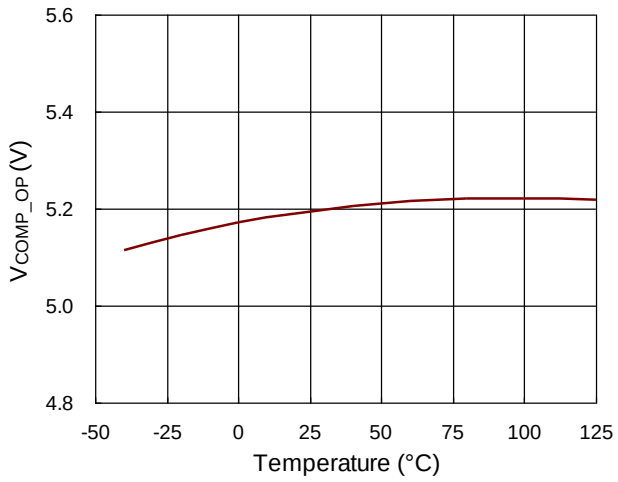
f_{BS_MIN} vs. Temperature



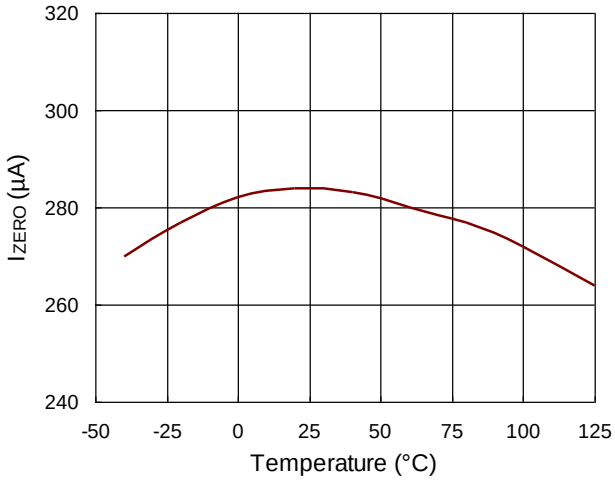
f_{BS_MIN} vs. Temperature



V_{COMP_OP} vs. Temperature



I_{ZERO} vs. Temperature



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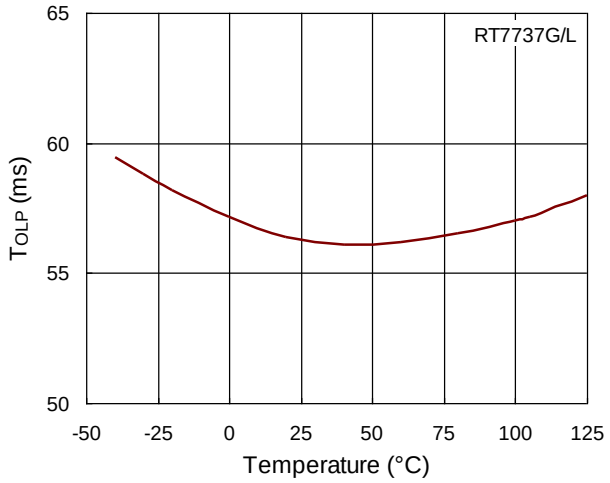
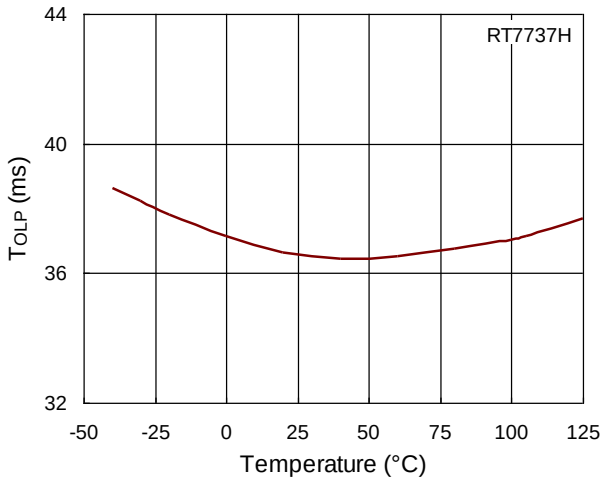
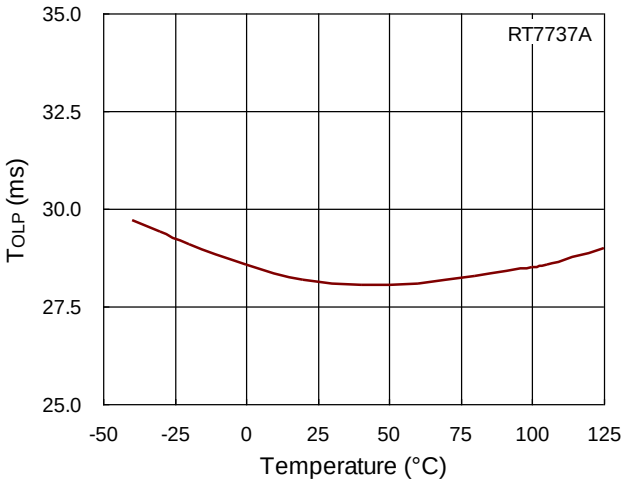
T_{OLP} vs. Temperature



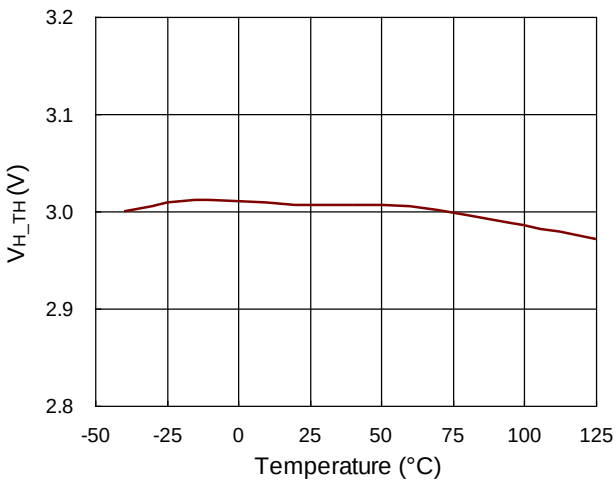
T_{OLP} vs. Temperature



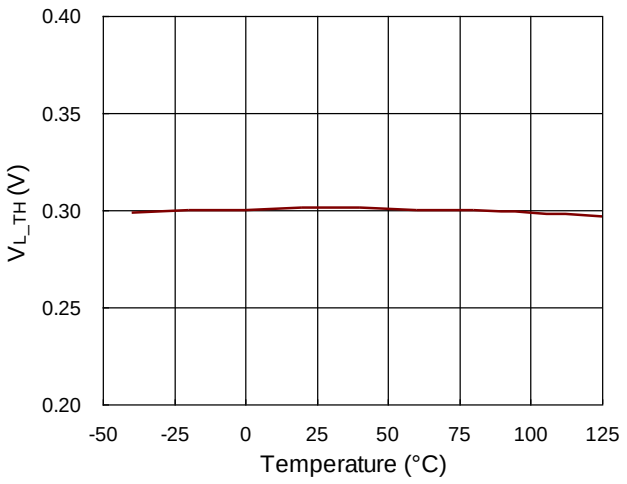
T_{OLP} vs. Temperature



V_{H_TH} vs. Temperature



V_{L_TH} vs. Temperature



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Application Information

SmartJitter™ Technology

The RT7737 series applies RICHTEK proprietary SmartJitter™ technology.

In order to reduce switching loss for lower power consumption during light load or no load, general PWM controllers have green mode function.

The output power equation is :

$$P_{O_DCM}(V_{COMP}) = \frac{1}{2} \times L_p \times \left(\frac{x_1 \times V_{COMP}}{R_{CS}}\right)^2 \times f_S(V_{COMP}) \times \eta$$

Where L_P is the magnetizing inductance of the transformer, R_{CS} is the current sense resistor, V_{COMP} is the feedback voltage of the COMP pin. f_S is the switching frequency of the power switch, η is the conversion efficiency, and x_1 is a constant coefficient.

Output power is a function of feedback voltage V_{COMP}. Frequency jittering technique is typically used to improve EMI problems in general PWM controllers, and the frequency jittering period is based on PWM switching frequency.

When the system enters green mode, a output power relationship is formed between the feedback voltage V_{COMP} and the PWM switching frequency, and a new stable equilibrium point is eventually reached after back-and-forth adjustments. It is mutually-affected by V_{COMP} and PWM switching frequency and limits the frequency jittering. As a result, EMI improvement function worsens, as show in Figure 1.

The innovative SmartJitter™ technology not only helps reduce EMI emissions of SMPS when the system enters green mode, but also eliminates output jittering ripple.

Accurate Over-Load Protection and Tight Current Limit Tolerance

Generally, the saw current limit is applied to low cost flyback controllers because of simple design. The RT7737 series applies RICHTEK proprietary technology through well foundry control, design and test/trim mode in final test to make the current limit tolerance tight enough to make design and mass production easier, and it provides accurate over-load protection.

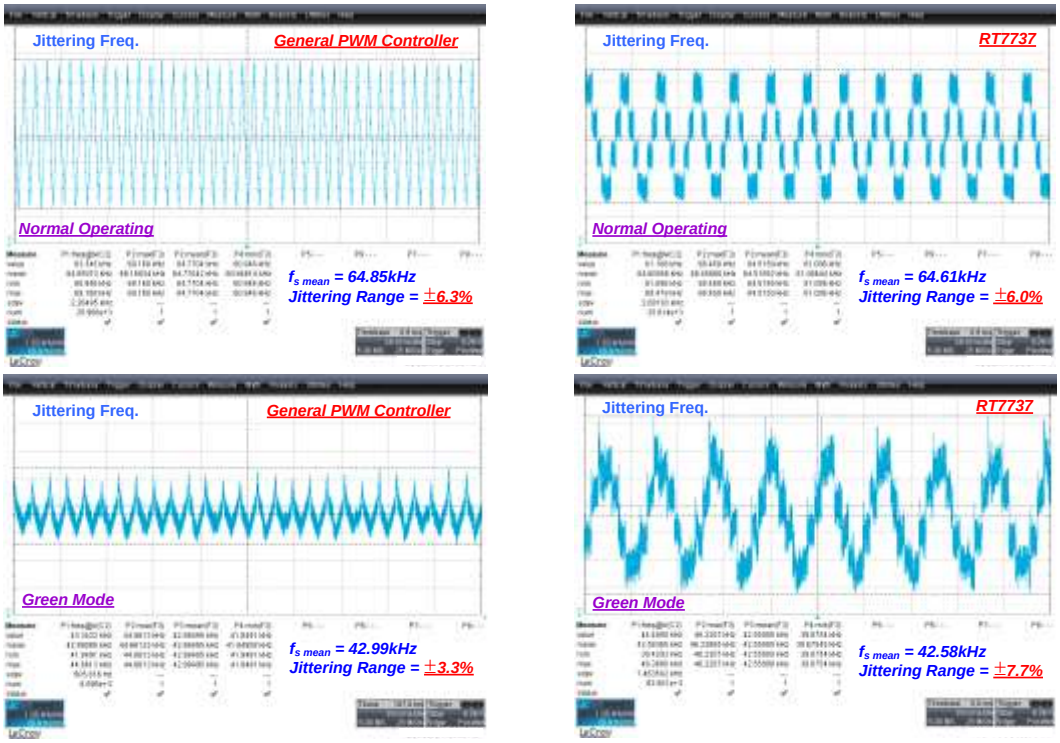

Figure 1. Frequency Jittering Range During Green Mode : General PWM Controller vs. RT7737

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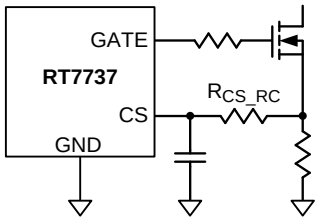
CS Pin - Programmable Burst Switching Green Mode Level

When the VDD reaches the threshold voltage V_{TH_ON}, the RT7737 starts to operate. Before the GATE starts to operate, the RT7737 sets the burst switching green mode thresholds (V_{BS_ET} and V_{BS_ED}) first. The IC provides a sourcing current from CS pin, and the voltage can be calculated as current value times resistance. When the setting voltage is higher, the burst switching green mode entry threshold is higher; when the setting voltage is lower, the burst switching green mode entry threshold voltage is lower. The RT7737 has five burst switching green mode levels as shown in Table 1.

The 1% or 5% R_{CS_RC} tolerance should be chosen for burst switching green mode level setting. Designers can use R_{CS_RC} = 330Ω as initial burst switching green mode level setting, and find the resistance value which make operating frequency most close to f_{BS_MIN} under highest input voltage and 25% nominal load. The better four loads (100%/75%/50%/25% nominal load) average frequency can be achieved by this design.

Besides achieving optimized average efficiency, for strict limit audio frequency product applications, the programmable burst switching green mode provides five levels for designers to avoid some specific frequencies under specific loads to fulfill product application requirements.

Table 1. Programmable Burst Switching Green Mode Level Setting

Burst Switching Green Mode Setting		
		
R_{CS_RC} (Ω)	**V_{BS_ET} (V)**	**V_{BS_ED} (V)**
750	2.75	2.35
510	2.65	2.25
330	2.55	2.15
200	2.45	2.05
100	2.35	1.95

BURST Pin - Programmable Burst Mode Level

The RT7737 provides a BURST pin to program the burst mode level by connecting a resistor, R_{BS}, with a range of 10kΩ to 60kΩ between the BURST pin and ground. The voltage on the BURST pin should be between V_{L_TH} and V_{H_TH} for normal operating as shown in Figure 2. Designers can program the burst mode entry voltage V_{BURST_ET} according to Figure 3, and the burst mode ending voltage V_{BURST_ED} = V_{BURST_ET} + 0.2V.

The 1% or 5% R_{BS_RC} tolerance should be chosen for burst mode level setting. Designers should use R_{BS_RC} = 33kΩ as initial burst mode level setting, and adjust burst mode level setting according to power consumption requirement under highest input voltage and no load.

When the R_{BS_RC} is larger, the quicker the IC enters burst mode which means the current is also larger. It turns out that the average frequency decreases under burst mode and the same load conditions. It decreases the switching losses under high input voltage, light load or no load conditions and further decreases power consumption efficiently. On the contrary, When the R_{BS_RC} is smaller, the slower the IC enters burst mode which means the current is also smaller. As a result, the average frequency increases under burst mode and the same load conditions, and it increases the switching losses under high input voltage, light load or no load conditions.

Audio noise is related to frequency and sound intensity, and the human ear can't hear a sound below 17kHz. The minimum frequency, f_{BS_MIN}, of the RT7737 is 22kHz which may not be heard by the human ear. Because of stricter energy regulations and pursuit of green performance, the requirements of light load and no load power consumption are lower and stricter. The RT7737 uses the control method to enter burst mode under light load or no load condition to efficiently decrease the switching losses to lower power consumption. However, the higher R_{BS} resistance is not the better. Although it can decrease the average frequency in burst mode, it also increases the cycle-by-cycle current which means the sound intensity is relatively larger. Also, the difference

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frequency of burst mode low frequency and the minimum frequency of the RT7737 falls to frequency that is available to human ear, ant it may cause audio noise problem.

As a result, designers should be aware of product audio noise while pursuing lower power consumption.

The advantages of programmable burst mode are that it can not only decreases power consumption under light load and no load conditions but also provides linear entry level setting for those applications which strict frequency limitations have to choose from, or avoid some specific frequencies.

The BURST pin can be used for programmable burst mode level setting and can also act as over-voltage protection or IC on/off control application with external application circuits, as shown in Figure 4 to 6. The application circuit design concept is shown in Figure 2. If the BURST voltage is lower than V_{L_TH} after deglitch time (30μs, typ.), the controller shuts down and stops switching. The BURST pin features an internal bias current (30μA, typ.). Bypassing the bias current can decrease the voltage on the BURST pin.

The range of the BURST pin series resistance is from 10kΩ to 60kΩ. Providing supply current from 260μA to 10μA from application circuit can raise the voltage on the BUSRT pin. The selection of application circuit components should take component leakage and thermal effect into account.

The programmable burst mode voltage should be between V_{L_TH} and V_{H_TH} for normal operation, so the BURST pin cannot be open. If designers want to connect a bypass capacitor to the BURST pin, the capacitance should be less than 1nF.

The difference between the burst switching green mode ending voltage (V_{BS_ED}) and the burst mode ending voltage (V_{BURST_ED}) should be more than 50mV to prevent the burst switching green mode from suddenly dropping to burst mode, causing audio noise.

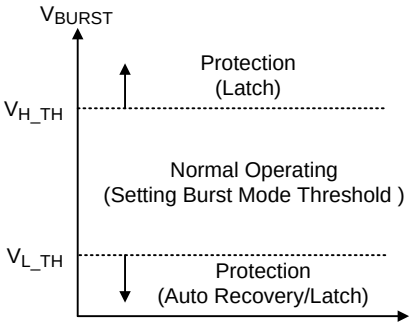

Figure 2. BURST Pin Operation

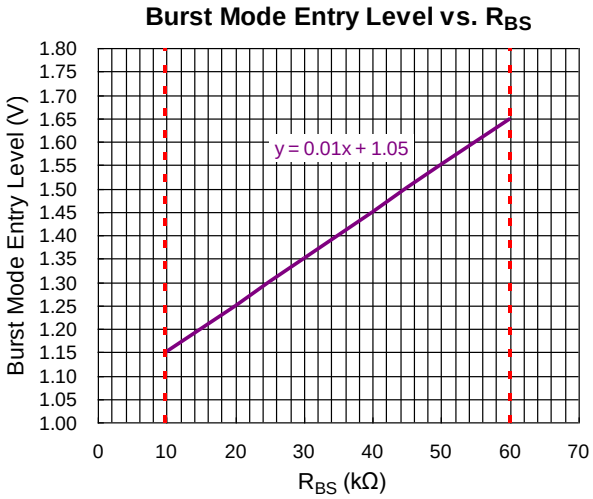

Figure 3. Burst Mode Entry Level vs. R_{BS}

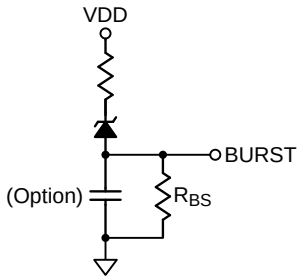

Figure 4. VDD OVP Application Circuit

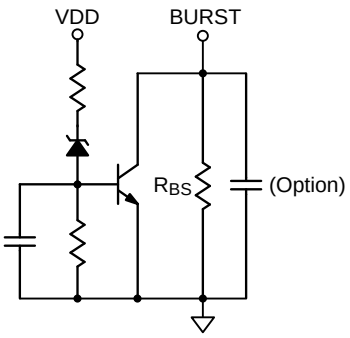

Figure 5. VDD OVP Application Circuit

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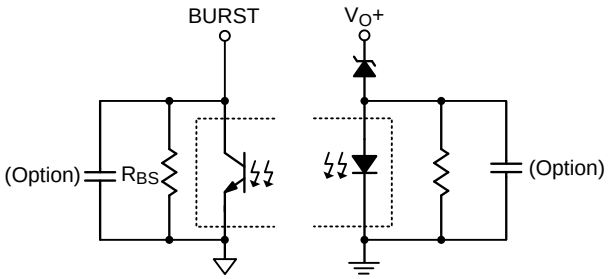

Figure 6. Output OVP Application Circuit

Start-Up Circuit

To minimize power loss, it's recommended to connect the start-up circuit to the bleeding resistors. It's power saving and also could reset latch mode protection quickly. Figure 7 shows I_{DD_Avg} vs. $R_{Bleeding}$ curve. Users can apply this curve to design the adequate bleeding resistors.

In order to prolong turn-off period and minimize the power loss and thermal rising during hiccup, the controller is designed to have smaller sinking current during entering auto-recovery protection, I_{DD_ARP}. Therefore, the start-up current at maximum AC line input voltage must be smaller than I_{DD_ARP} ($I_{DD_ARP(min)}$ = 350μA). Otherwise, when the controller enters auto-recovery protection, the VDD capacitor won't be dropped down to V_{TH_OFF} by IC's sinking current and then restart. The controller behaves like latch protection or triggers the SCR of VDD.

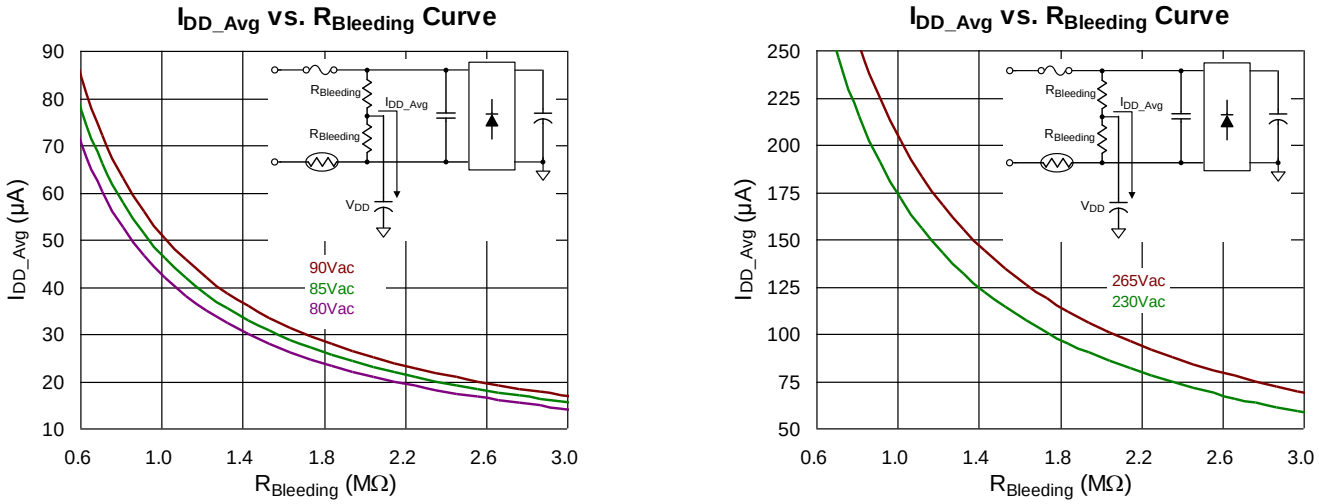

Figure 7. I_{DD_Avg} vs. $R_{Bleeding}$ Curve

VDD Discharge Time in Auto Recovery Mode

Figure 8 shows the V_{DD} and V_{GATE} waveforms during an auto recovery protection (e.g., OLP). In this mode, the start-up resistors, VDD sinking current and VDD decoupling capacitor will affect the restart time. The VDD voltage discharge time $t_{D_Discharge}$ can be calculated by the following equation :

$$t_{D_Discharge} = \frac{C_{VDD} \times (V_{DD_DIS} - V_{TH_OFF})}{I_{DD_ARP} - I_{ST}}$$

Where the C_{VDD} is the VDD decoupling capacitor, the V_{DD_DIS} is the initial VDD voltage after entering the auto recovery mode, the V_{TH_OFF} (9V typ.) is the falling UVLO voltage threshold of the controller, the I_{DD_ARP} (550μA typ.) is the sinking current of the VDD pin in the auto recovery mode, and I_{ST} is the start-up current of the power system.

Please note that the start-up current at high input voltage must be smaller than the I_{DD_ARP}. Otherwise, the VDD voltage can't reach the V_{TH_OFF} to activate the next start-up process after an auto recovery protection. Therefore, the system behavior resembles the behavior of latch mode.

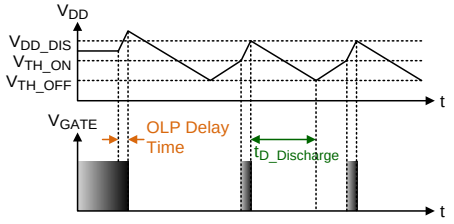

Figure 8. Auto Recovery Mode (e.g., OLP)

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VDD Holdup Mode

The VDD holdup mode is only designed to prevent VDD from decreasing to the turn-off threshold voltage, V_{TH_OFF}, under light load or load transient. Compare to burst mode, the VDD holdup mode brings higher switching. Hence, it is highly recommended that the system should avoid operating at this mode during light load or no load conditions.

Output Short Protection

The RT7737 implements output short protection by detecting GATE width T_{ON_OSP} and delay time T_{D_OSP}. It can minimize the power loss during output short, especially at high line input voltage.

Because it is hard to distinguish the difference between output short and big capacitance load, circuit design must be careful to make sure GATE width is larger than T_{ON_OSP} (T_{ON} > $T_{ON_OSP(MAX)}$) after delay time T_{D_OSP} during start-up.

Resistors on GATE Pin

In Figure 9, R_G is applied to alleviate ringing spike of gate drive loop in typical application circuits. The value of R_G must be considered carefully with respect to EMI and efficiency for the system.

The built-in internal discharge resistor R_{ID} in parallel with GATE pin prevents the MOSFET from any uncertain condition. If the connection between the GATE pin and the Gate of the MOSFET is disconnected, the MOSFET will be false triggered by the residual energy through the Gate-to-Drain parasitic capacitor C_{GD} of the MOSFET and the system will be damaged. Therefore, it's highly recommended to add an external discharge-resistor R_{ED} connected between the Gate of MOSFET and GND terminals. The energy through the C_{GD} is discharged by the external discharge-resistor to avoid MOSFET false triggering.

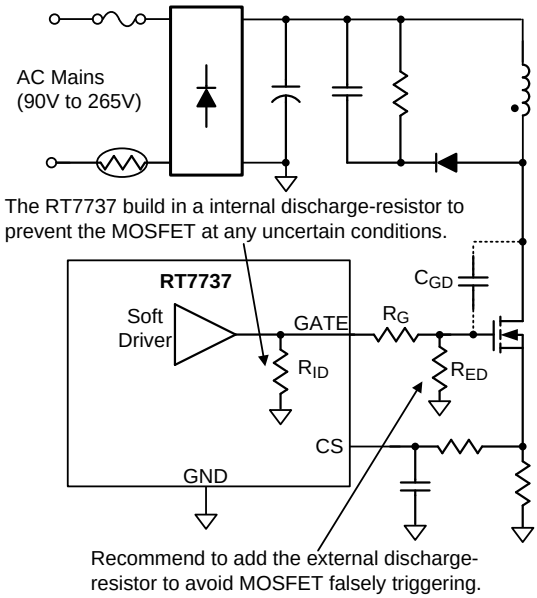

Figure 9. Resistors on Gate Pin

Feedback Resistor

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced, as shown in Figure 10. Due to small feedback resistor current, shunt regulator selection (e.g. TL-431) and minimum regulation current design must be considered carefully to make sure it's able to regulate under low cathode current.

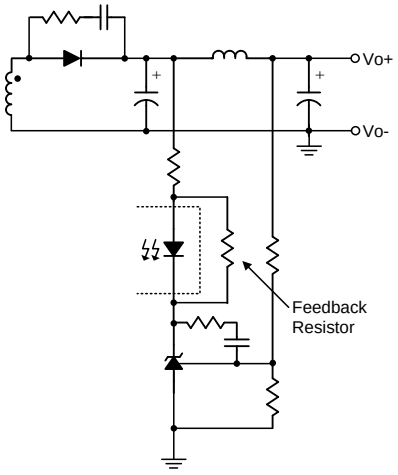

Figure 10. Feedback Resistor

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Negative Voltage Spike on Each Pin

Negative voltage (< −0.3V) to the controller pins will cause substrate injection and lead to controller damage or circuit false triggering. For example, the negative spike voltage at the CS pin may come from improper PCB layout or inductive current sense resistor. Therefore, it is highly recommended to add an R-C filter to avoid the CS pin damage, as shown in Figure 11. Proper PCB layout and component selection should be considered during circuit design.

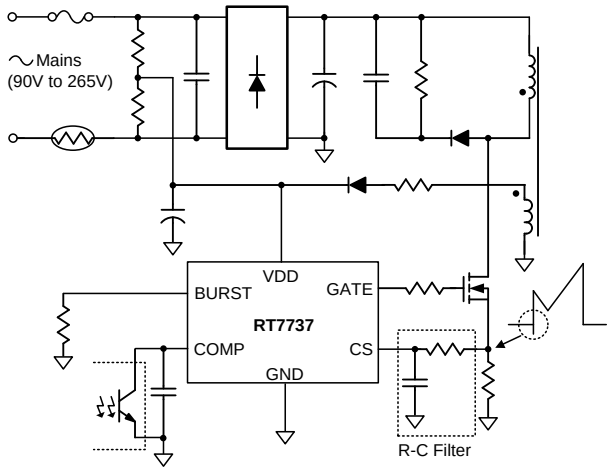

Figure 11. R-C Filter on CS Pin

Over-Temperature Protection (OTP)

The RT7737 provides OTP function to prevent permanent damage. It is not recommended to apply this function to accurate temperature control.

When the IC turns on, the controller detects around temperature before it starts switching. If the temperature is higher than T_{OTP_INTH} (typ. 120°C), the controller triggers OTP, and there is no output signal. If the temperature is lower than T_{OTP_INTH}, the controller starts operation and the OTP threshold is automatically set to T_{OTP_STTH} (typ. 140°C), which means when the controller starts switching, the OTP threshold is T_{OTP_STTH}.

When the controller triggers OTP, the controller will be shut down and cease switching. At the same time, V_{DD} drops below V_{DD} off threshold V_{TH_OFF}, the controller enters hiccup mode. Until the OTP is released, the controller resumes operation.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (260.7°C/W) = 0.38W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 12 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

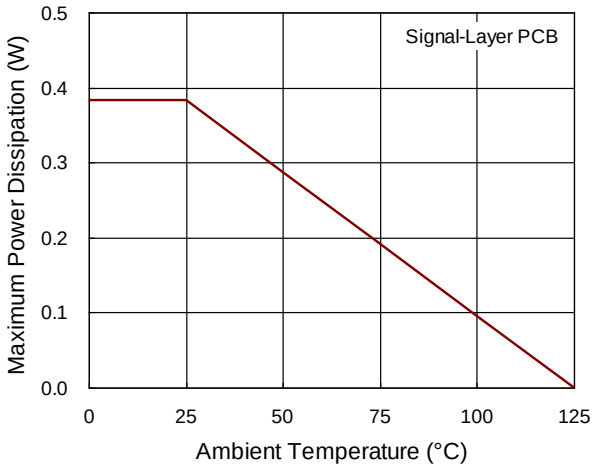

Figure 12. Derating Curve of Maximum Power Dissipation

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Layout Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply :

- The current path (1) through bulk capacitor, transformer, MOSFET, R_{CS} returns to bulk capacitor is a high frequency current loop. It must be as short as possible to decrease noise coupling and keep away from other low voltage traces, such as IC control circuit paths, especially.
- The path (2) of the RCD snubber circuit is also a high switching loop. Keep it as small as possible.
- Separate the ground traces of bulk capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d) for reducing noise, output ripple and EMI issue. Connect these ground traces together at bulk capacitor ground (a). The areas of these ground traces should be large enough.
- Place the bypass capacitor as close to the controller as possible.
- In order to reduce reflected trace inductance and EMI, minimize the area of the loop connecting the secondary winding, output diode and output filter capacitor. In additional, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking.

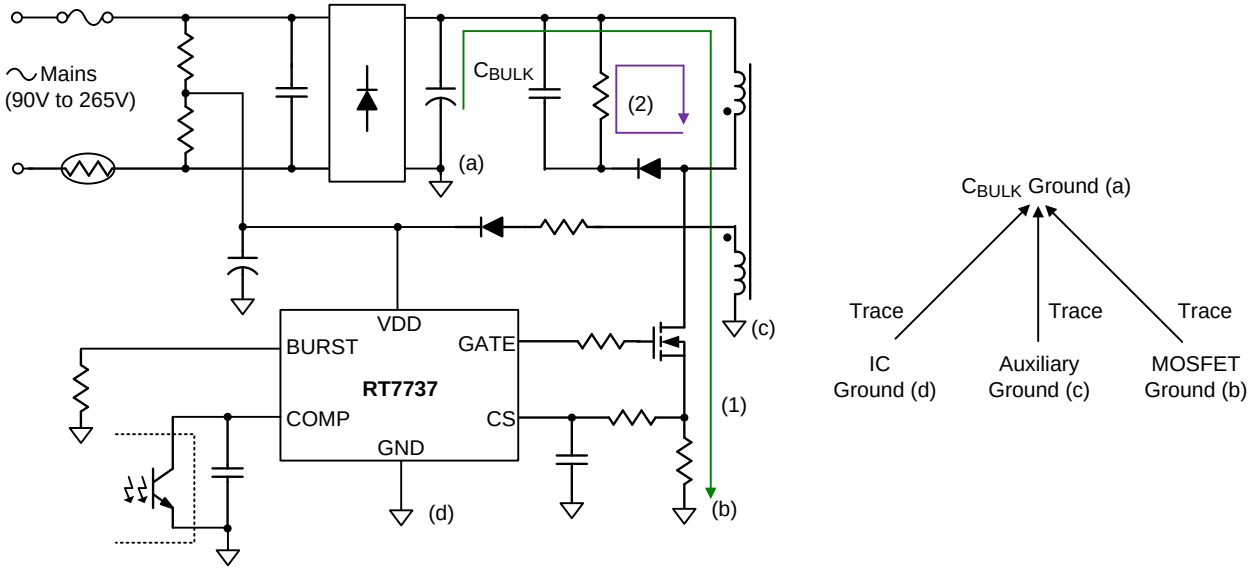

Figure 13. PCB Layout Guide

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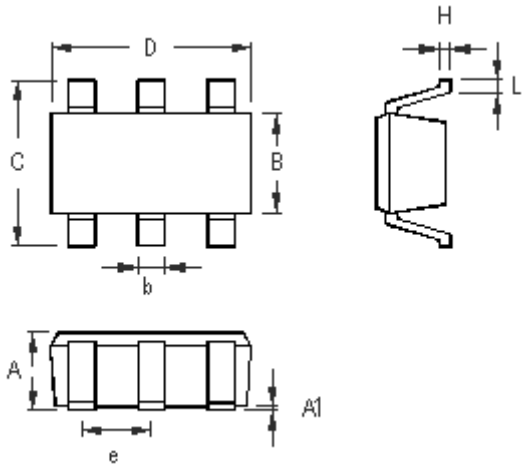
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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