RICHTEK®

RT7758M

PWM Controller for Programmable Power Converter (USB PD)

1 General Description

The RT7758M series, operating with Continuous Conduction Mode (CCM) or Quasi-Resonant Mode (QR Mode), is specifically designed to work with controllers, such as the RT7216KNE to provide a comprehensive solution for USB PD or programmable power adapters. This RT7758M not only offers a high power efficiency control scheme, but also achieves very low standby power consumption of 50mW under 5V standby conditions.

The RT7758M is specifically design to achieve a wide range of output voltages by utilizing several innovations, including (1) By way of the DMAG pin, the RT7758M senses the output voltage to adjust loop gain for system stability, adjust the output overvoltage protection threshold voltage to protect external devices, and adjust the current limit to meet Limited Power Source (LPS) safety requirements; (2) The RT7758M is equipped with comprehensive protection features, including bulk-capacitor brown-in/brown-out protection, VDD Overvoltage Protection (VDD OVP), output Overvoltage/Undervoltage Protection (output OVP/UVP), Secondary Rectifier Short-Circuit Protection (SRSP), and external Over-Temperature protection (external OTP); (3) For constant output power regulation, a resistor connected to the CS pin can be used to achieve accurate line compensation across the universal input voltage range; and (4) The RT7758M also provides various features to protect against any failures occurring at the secondary-side component, such as the RT7216KNE or a shunt regulator.

In applications, it is suggested that the RT7758M be used with a secondary controller, the RT7216KNE. To realize a robust and safe design that prevents all potential fault conditions due to misconnection of various devices, cables, plugs and receptacles.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Features

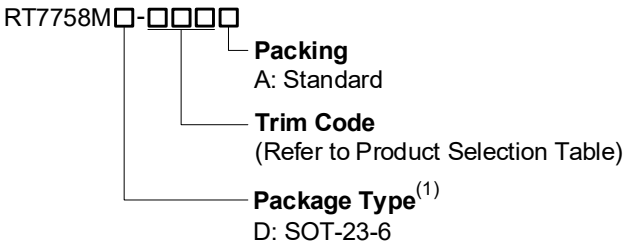
- **Optimized for Adaptive Output Power**
  - **Wide VDD Range: 9V to 64V**
  - **Adaptive Loop Gain Control for Loop Stability**
- **High Efficiency**
  - **Green Mode Operation at Light Load and No Load**
- **Comprehensive Protection Features**
  - **Bulk-Capacitor Brown-In and Brown-Out Protection**
  - **VDD Overvoltage Protection**
  - **Output Overvoltage and Undervoltage Protection**
  - **External Over-Temperature Protection**
  - **Secondary Rectifier Short-Circuit Protection**
  - **Programmable Line Compensation**
- **Others**
  - **<50mW in 5V Standby Mode for Power Saving**
  - **Driver Capability: 250mA/–400mA**
  - **SmartJitter Technology**

3 Applications

- USB PD and Programmable Power Adapters

4 Ordering Information

4.1 Product Number Information



Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

4.2 Product Selection Table

Product Number		RT7758MD-LQTA	RT7758MD-AQTA	RT7758MD-AQPA	RT7758MD-AQCA	RT7758MD-AQDA	RT7758MD-AEMA	RT7758MD-LQAA
Operation Mode		QR Mode	CCM Mode	CCM Mode	CCM Mode	CCM Mode	CCM Mode	CCM Mode
Constant Power Application (V_{DMAG} > $V_{DMAG\_HYSMIDPD}$)		X	X	X	X	X	X	O
Normal Mode PWM Frequency, f_{NOR}		85kHz	65kHz	65kHz	65kHz	65kHz	65kHz	65kHz
Maximum PWM Frequency for Frequency Increased Peak Load, f_{MAX}		X	130kHz	130kHz	130kHz	130kHz	X	130kHz
Minimum QR Mode Frequency, f_{QR_MIN}		61.5 kHz	X	X	X	X	X	X
Valley Switching Mode		O	O	O	O	O	O	O
Valley Jitter Function		O	O	O	O	O	O	O
Peak Load	Frequency Increased Mode	X	O	O	O	O	X	O
	V_{CS_OCP2} (I_{DMAG} > I_{DMAG_HVSW})	X	0.5V	0.4V	0.5V	0.5V	X	0.5V
	V_{CS_OCP2} (I_{DMAG} < I_{DMAG_HVSW})	X	0.55V	0.4V	0.5V	0.5V	X	0.55V
Zero-Duty Entry Voltage (I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} > 2.7V) (Note 7)		0.75V	0.8V	0.7V	0.8V	0.9V	0.9V	1V
Deep Burst Mode Function		X	O	O	X	X	X	X

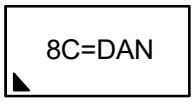
Product Number	RT7758MD-LQTA	RT7758MD-AQTA	RT7758MD-AQPA	RT7758MD-AQCA	RT7758MD-AQDA	RT7758MD-AEMA	RT7758MD-LQAA
Disable Line Compensation (V_{COMPD} < V_{GM_ED1}, V_{DMAG} > 1.15V) (Note 7)	O	O	X	X	O	O	O
VDD OVP	Auto-Recovery	Latch	Latch	Latch	Latch	Latch	Latch
Output OVP	Auto-Recovery	Latch	Latch	Latch	Latch	Latch	Latch
Output UVP	Auto-Recovery	Latch	Latch	Latch	Latch	Latch	Auto-Recovery
OCP (Level – I)	Auto-Recovery	Latch	Latch	Latch	Latch	Latch	Auto-Recovery
OCP (Level – II)	X	Latch	Latch	Latch	Latch	X	Auto-Recovery
OCP (Level – I) Delay Time	192.8ms @ f_{NOR}	252ms @ f_{NOR}	252ms @ f_{NOR}	252ms @ f_{NOR}	252ms @ f_{NOR}	63ms @ f_{NOR}	252ms @ f_{NOR}
OCP (Level – II) Delay Time	X	126ms @ f_{MAX}	126ms @ f_{MAX}	126ms @ f_{MAX}	126ms @ f_{MAX}	X	126ms @ f_{MAX}
SRSP	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery
External OTP	Auto-Recovery	Latch	Latch	Latch	Latch	Latch	Auto-Recovery

5 Marking Information

RT7758MD-LQTA

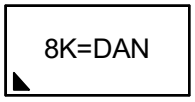
8G=: Product Code
DAN: Date Code

RT7758MD-AQTA



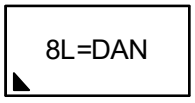
8C=: Product Code
DAN: Date Code

RT7758MD-AQPA



8K=: Product Code
DAN: Date Code

RT7758MD-AQCA

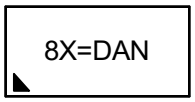


8L=: Product Code
DAN: Date Code

RT7758MD-AQDA

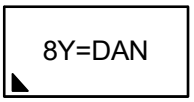
8T=: Product Code
DAN: Date Code

RT7758MD-AEMA



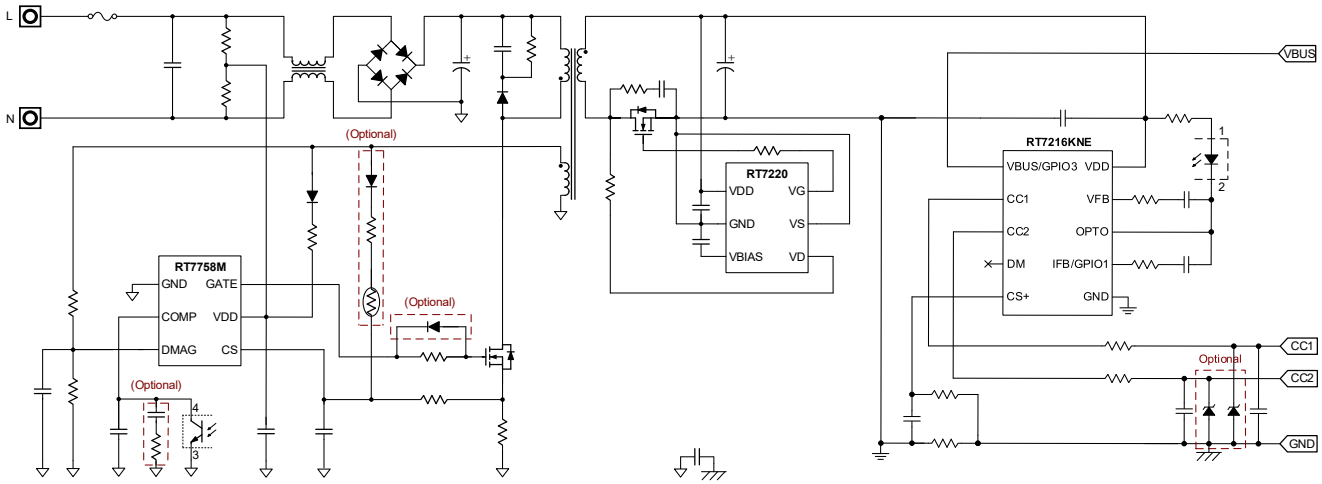
8X=: Product Code
DAN: Date Code

RT7758MD-LQAA



8Y=: Product Code
DAN: Date Code

6 Simplified Application Circuit



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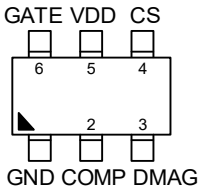
7 Pin Configuration

(TOP VIEW)

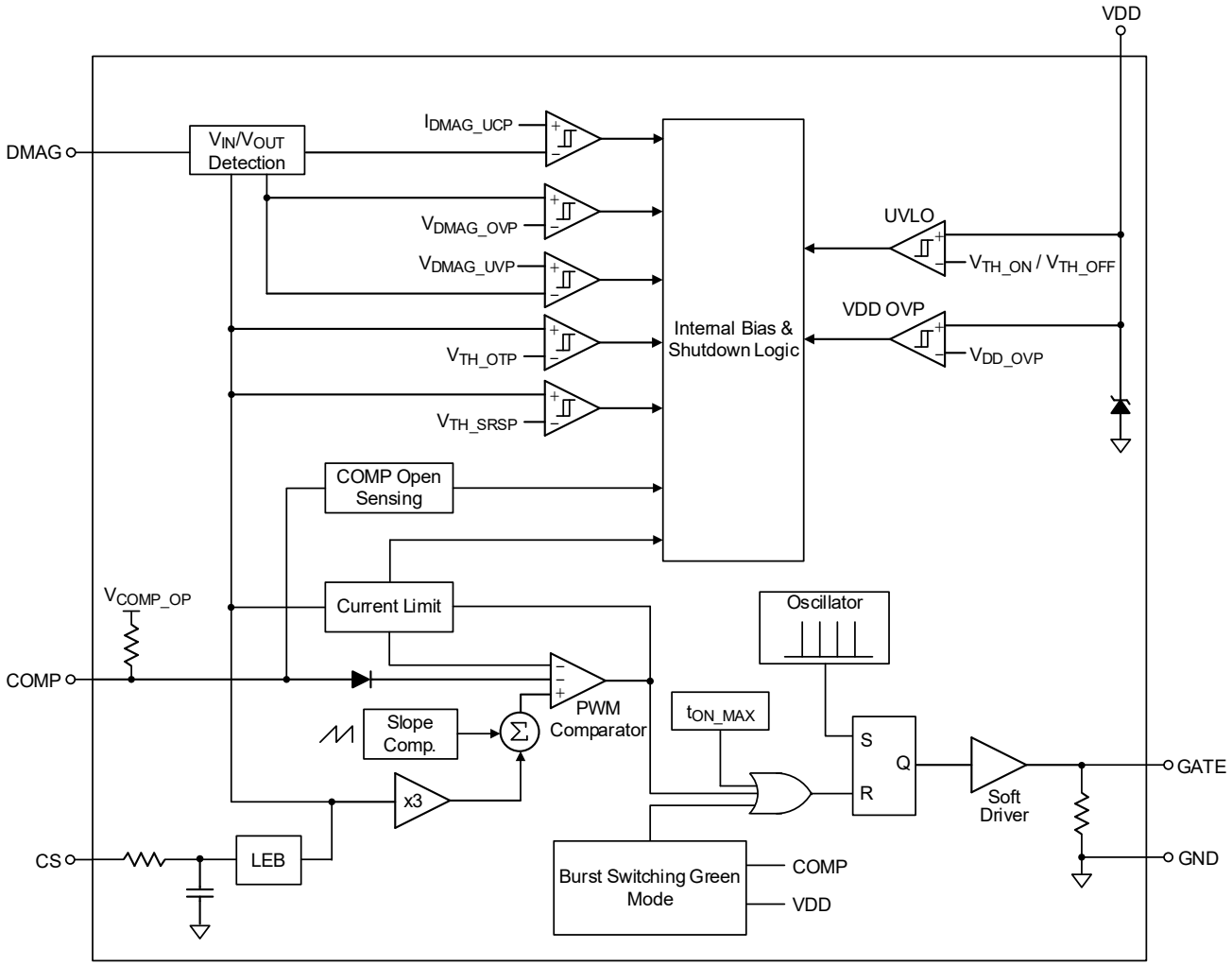


SOT-23-6

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground of the controller.
2	COMP	Feedback input. Connect an opto-coupler from the COMP pin to GND to close the control loop to achieve output voltage regulation.
3	DMAG	Demagnetization input. Input and output voltages are sensed from the auxiliary winding.
4	CS	Current sense input. The current sense resistor, connected from the CS pin to GND, is used to set the current limit for the power system.
5	VDD	Supply input voltage. The controller is enabled when the VDD voltage exceeds V_{TH_ON} and is disabled when the VDD voltage drops below V_{TH_OFF}.
6	GATE	Gate driver output.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 70V
- GATE to GND ---------- –0.3V to 16.5V
- COMP, CS to GND ---------- –0.3V to 6.5V
- DMAG to GND (DC Continue) ---------- –0.3V to 6.5V
- DMAG to GND (Pulse width 0.1ms and negative current -5mA) ---------- –1V to 6.5V
- Power Dissipation, P_D@ T_A = 25°C

  SOT-23-6 ---------- 0.39W
- Package Thermal Resistance (Note 3)

  SOT-23-6, θ_{JA} ---------- 254.2°C/W

  SOT-23-6, $\theta_{JC(top)}$ ---------- 83.7°C/W

  SOT-23-6, $\theta_{JC(bot)}$ ---------- 42°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under ”Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD ---------- 9V to 64V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Overvoltage Protection Threshold Voltage	V_{DD_OVP}		65	67	69	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD Undervoltage Protection Threshold Voltage	V_{DD_UVP}	$V_{COMP} > V_{COMP\_OP} - 0.35V$ and $V_{DMAG} < V_{DMAG\_UVP}$		7	7.5	8	V
Turn-On Threshold Voltage	V_{TH_ON}			15	17	19	V
Turn-Off Threshold Voltage	V_{TH_OFF}			6.5	7	7.5	V
VDD Holdup Mode Entry Point	V_{DD_ET}	$V_{COMPD} < V_{ZD\_ET}$, VDD falling (Note 7)		7	7.5	8	V
VDD Holdup Mode Ending Point	V_{DD_ED}	$V_{COMPD} < V_{ZD\_ET}$, VDD rising (Note 7)		V_{DD_ET} + 0.1	V_{DD_ET} + 0.5	V_{DD_ET} + 0.9	V
Delta Voltage between V_{DD_ET} and V_{TH_OFF}	ΔV_{ED_OFF}			0.2	0.5	0.8	V
Latch-Off Clamp Voltage	V_{DD_LH}			4.35	4.85	5.35	V
Latch-Off Release Threshold Voltage	V_{DD_RST}			V_{DD_LH} – 0.9	V_{DD_LH} – 0.35	V_{DD_LH} – 0.1	V
Start-Up Current	I_{DD_ST}	$V_{DD} < V_{TH\_ON} - 0.1V$		--	1.5	4	µA
Operating Supply Current	I_{DD_OP}	V_{DD} = 15V, V_{COMP} = 0V		295	345	395	µA
			RT7758M-AEM RT7758M-LQT	265	315	365	
I_{DD} Sinking Current for Auto-Recovery Mode	I_{DD_ARP}	During entering auto-recovery mode		770	960	1180	µA
Latch-Off Operating Current	I_{DD_LH}	T_A = –40°C to 85°C		1	--	10	µA
Oscillator Section							
Normal Mode PWM Frequency	f_{NOR}	$V_{GM\_ET2} > V_{COMPD} > V_{GM\_ET1}$ (Note 7)		60	65	70	kHz
			RT7758M-LQT	80	85	90	
Maximum PWM Frequency for Frequency Increased Peak Load	f_{MAX}	$V_{COMPD} > V_{GM\_ED2}$ (Note 7)	RT7758M-AQP	120	130	140	kHz
		$V_{COMPD} > V_{GM\_ED2}$, $I_{DMAG} < I_{DMAG\_HVSW}$ (Note 7)	RT7758M-AQT RT7758M-AQC RT7758M-AQD RT7758M-LQA	120	130	140	
Minimum Green Mode Frequency	f_{GM_MIN}	$V_{COMPD} < V_{GM\_ED1}$ (Note 7)		20	25	30	kHz
Minimum QR Mode Frequency	f_{QR_MIN}		RT7758M-LQT	53	61.5	70	kHz
Maximum Duty for CCM	D_{MAX_CCM}	During CCM mode		70	75	80	%
Maximum Duty for QR	D_{MAX_QR}	Operating at f_{QR_MIN}	RT7758M-LQT	71	78	85	%
PWM Frequency Jittering Range	Δf			±3	±6	±9	%

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PWM Frequency Jittering Period	t_{JIT}	f_{OSC} = 65kHz (Note 6)		12.6	15.8	19	ms
		f_{OSC} = 85kHz (Note 6)	RT7758M-LQT	9.6	12	14.4	
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 9V to 67V at f_{OSC} = f_{NOR}		--	--	2	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = –30°C to 105°C (Note 6)		--	--	5	%
COMP Input Section							
Open-Loop Voltage	V_{COMP_OP}	Comp pin open-circuited		4	4.2	4.4	V
			RT7758M-AEM RT7758M-LQT	3.4	3.6	3.8	
COMP Short-Circuit Current	I_{ZERO}	V_{COMP} = 0V		150	210	270	µA
			RT7758M-AEM RT7758M-LQT	120	180	240	
COMP Open-Loop Protection Delay Time	$t_{DLY\_COMP\_OP}$	f_{OSC} = 65kHz		220	252	284	ms
			RT7758M-AEM	50.4	63	75.6	
		f_{OSC} = 85kHz	RT7758M-LQT	162.8	192.8	222.8	
Green Mode Entry Voltage (Level – I)	V_{GM_ET1}	I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} > 2.7V, (Note 7)		1.1	1.15	1.2	V
			RT7758M-LQT	1	1.05	1.1	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} < 0.9V, (Note 7)		0.8	0.85	0.9	
			RT7758M-LQT	0.7	0.75	0.8	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} > 2.7V, (Note 7)		1	1.05	1.1	
			RT7758M-LQT	0.9	0.95	1	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} < 0.9V, (Note 7)		0.7	0.75	0.8	
			RT7758M-LQT	0.6	0.65	0.7	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Green Mode Ending Voltage (Level – I)	V_{GM_ED1}	I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} > 2.7V, (Note 7)		0.95	1	1.05	V
			RT7758M-LQT	0.8	0.85	0.9	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} < 0.9V, (Note 7)		0.65	0.7	0.75	
			RT7758M-LQT	0.5	0.55	0.6	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} > 2.7V, (Note 7)		0.85	0.9	0.95	
			RT7758M-LQT	0.7	0.75	0.8	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} < 0.9V, (Note 7)		0.55	0.6	0.65	
			RT7758M-LQT	0.4	0.45	0.5	
Green Mode Entry Voltage (Level – II)	V_{GM_ET2}	I_{DMAG} < I_{DMAG_HVSW} (Note 7)		1.7	1.8	1.9	V
Green Mode Ending Voltage (Level – II)	V_{GM_ED2}	I_{DMAG} < I_{DMAG_HVSW} (Note 7)		1.9	2	2.1	V
Zero-Duty Entry Voltage	V_{ZD_ET}	I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} > 2.7V (Note 7)	RT7758M-LQA	0.85	0.9	0.95	V
			RT7758M-AQD RT7758M-AEM	0.75	0.8	0.85	
			RT7758M-AQC RT7758M-AQT	0.65	0.7	0.75	
			RT7758M-LQT	0.6	0.65	0.7	
			RT7758M-AQP	0.55	0.6	0.65	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} < 0.9V (Note 7)	RT7758M-LQA	0.55	0.6	0.65	
			RT7758M-AQD RT7758M-AEM	0.45	0.5	0.55	
			RT7758M-AQC RT7758M-AQT	0.35	0.4	0.45	
			RT7758M-LQT	0.3	0.35	0.4	
			RT7758M-AQP	0.25	0.3	0.35	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} > 2.7V (Note 7)	RT7758M-LQA	0.95	1	1.05	
			RT7758M-AQD RT7758M-AEM	0.85	0.9	0.95	
			RT7758M-AQC RT7758M-AQT	0.75	0.8	0.85	
			RT7758M-LQT	0.7	0.75	0.8	
			RT7758M-AQP	0.65	0.7	0.75	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} < 0.9V (Note 7)	RT7758M-LQA	0.65	0.7	0.75	
			RT7758M-AQD RT7758M-AEM	0.55	0.6	0.65	
			RT7758M-AQC RT7758M-AQT	0.45	0.5	0.55	
			RT7758M-LQT	0.4	0.45	0.5	
			RT7758M-AQP	0.35	0.4	0.45	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Zero-Duty Ending Voltage	V_{ZD_ED}	I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} > 2.7V (Note 7)	RT7758M-LQA	0.875	0.925	0.975	V
			RT7758M-AQD RT7758M-AEM	0.775	0.825	0.875	
			RT7758M-AQC RT7758M-AQT	0.675	0.725	0.775	
			RT7758M-LQT	0.625	0.675	0.725	
			RT7758M-AQP	0.575	0.625	0.675	
		I_{DMAG} < I_{DMAG_HVSW}, V_{DMAG} < 0.9V (Note 7)	RT7758M-LQA	0.575	0.625	0.675	
			RT7758M-AQD RT7758M-AEM	0.475	0.525	0.575	
			RT7758M-AQC RT7758M-AQT	0.375	0.425	0.475	
			RT7758M-LQT	0.325	0.375	0.425	
			RT7758M-AQP	0.275	0.325	0.375	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} > 2.7V (Note 7)	RT7758M-LQA	0.975	1.025	1.075	
			RT7758M-AQD RT7758M-AEM	0.875	0.925	0.975	
			RT7758M-AQC RT7758M-AQT	0.775	0.825	0.875	
			RT7758M-LQT	0.725	0.775	0.825	
			RT7758M-AQP	0.675	0.725	0.775	
		I_{DMAG} > I_{DMAG_HVSW}, V_{DMAG} < 0.9V (Note 7)	RT7758M-LQA	0.675	0.725	0.775	
			RT7758M-AQD RT7758M-AEM	0.575	0.625	0.675	
			RT7758M-AQC RT7758M-AQT	0.475	0.525	0.575	
			RT7758M-LQT	0.425	0.475	0.525	
			RT7758M-AQP	0.375	0.425	0.475	
Current Sense Section							
Overcurrent Protection Threshold Voltage for OCP (Level – I)	V_{CS_OCP1}	V_{DMAG} > 2.7V		0.38	0.4	0.42	V
		V_{DMAG} < 0.9V		0.26	0.28	0.3	
Maximum Overcurrent Protection Threshold Voltage for OCP (Level – II)	V_{CS_OCP2}	V_{DMAG} > 2.7V, I_{DMAG} > I_{DMAG_HVSW} (Note 6)	RT7758M-AQT RT7758M-LQA	0.475	0.5	0.525	V
		V_{DMAG} > 2.7V, I_{DMAG} < I_{DMAG_HVSW}	RT7758M-AQT RT7758M-LQA	0.5	0.55	0.6	
		V_{DMAG} > 2.7V	RT7758M-AQC RT7758M-AQD	0.475	0.5	0.525	
		V_{DMAG} > 2.7V	RT7758M-AQP	0.38	0.4	0.42	

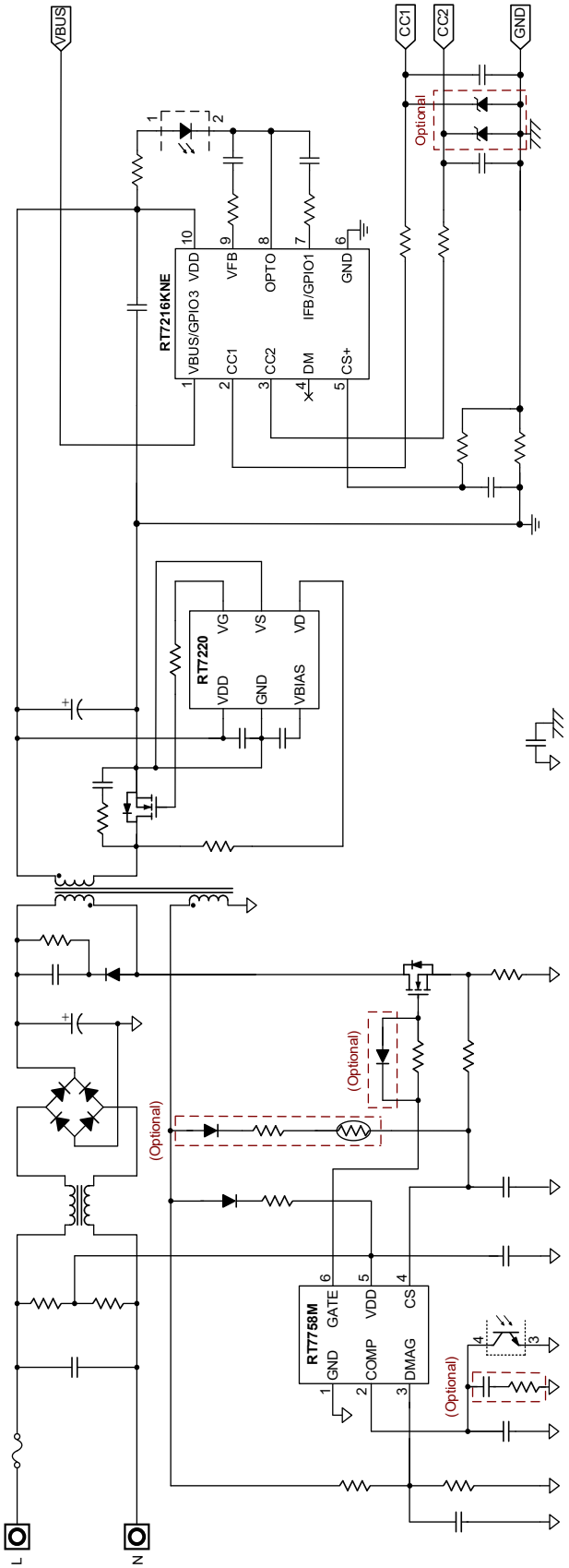
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Overcurrent Protection Delay Time (Level – I)	t_{DLY_OCP1}	f_{OSC} = 65kHz		220	252	284	ms
			RT7758M-AEM	50.4	63	75.6	
		f_{OSC} = 85kHz	RT7758M-LQT	162.8	192.8	222.8	
Overcurrent Protection Delay Time (Level – II)	t_{DLY_OCP2}	I_{DMAG} > I_{DMAG_HVSW}, f_{OSC} = 65kHz	RT7758M-AQT RT7758M-AQC RT7758M-AQD RT7758M-LQA	220	252	284	ms
		I_{DMAG} < I_{DMAG_HVSW}, f_{OSC} = 130kHz	RT7758M-AQT RT7758M-AQC RT7758M-AQD RT7758M-LQA	106	126	146	
		f_{OSC} = 130kHz	RT7758M-AQP	106	126	146	
Leading-Edge Blanking Time	t_{LEB}			400	475	550	ns
Secondary Rectifier Short-Circuited Protection Threshold Voltage	V_{TH_SRSP}			0.9	1.0	1.1	V
External Over-Temperature Protection Threshold Voltage	V_{TH_OTP}	V_{DMAG} = 3V		0.79	0.81	0.83	V
External Over-Temperature Protection Delay Time	t_{DLY_OTP}	f_{OSC} = 65kHz		53	63	73	ms
		f_{OSC} = 85kHz		38.6	48.2	57.8	
GATE Section							
Rising Time	t_R	C_L = 1nF	RT7758M-LQT	80	180	280	ns
				160	340	520	
Falling Time	t_F	C_L = 1nF		5	30	80	ns
GATE Output Clamp Voltage	V_{CLAMP}	V_{DD} = 23V		10	11.5	13	V
DMAG Section							
Output Overvoltage Protection Threshold Voltage	V_{DMAG_OVP}			3.5	3.6	3.7	V
Output Undervoltage Protection Threshold Voltage	V_{DMAG_UVP}			0.3	0.35	0.4	V
Output Undervoltage Protection Delay time	$t_{DLY\_DMAGUVP}$	f_{OSC} = 65kHz		12.6	15.8	19	ms
		f_{OSC} = 85kHz	RT7758M-LQT	18.2	22.7	27.2	
Blanking Time of the DMAG Pin	t_{BLK}	V_{CS_PK} = 0V		1.5	1.8	2.1	µs
		V_{CS_PK} = 0.4V		2.1	2.5	2.9	
Brown-In Protection Threshold Current	I_{DMAG_BNI}			300	320	340	µA
Brown-Out Protection Threshold Current	I_{DMAG_BNO}			270	290	310	µA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Brown-Out Protection Delay Time	t_{DLY_BNO}	f_{OSC} = 65kHz		53	63	73	ms
		f_{OSC} = 85kHz	RT7758M-LQT	38.6	48.2	57.8	
High VIN Entry Level	I_{DMAG_HVSW}			578	680	782	μA
Hysteresis of High VIN Entry	I_{DMAG_HVHYS}			5	20	40	μA
Enable Valley Switching Threshold Voltage	V_{EN_VALLEY}			1.1	1.15	1.2	V
Disable Valley Switching Threshold Voltage	V_{DIS_VALLEY}			1	1.05	1.1	V
Enable Constant Current Threshold Voltage	V_{DMAG_MIDPD}		RT7758M-LQA	1.45	1.5	1.55	V
Enable Constant Power Threshold Voltage	$V_{DMAG\_HYSMIDPD}$		RT7758M-LQA	1.55	1.6	1.65	V
Debounce Time of High Line to Low Line	t_{DLY_HTOL}	f_{OSC} = 65kHz (Note 6)		230	252	274	ms
		f_{OSC} = 85kHz (Note 6)	RT7758M-LQT	162.8	192.8	222.8	
Maximum DMAG Sourcing Current	I_{DMAG_MAX}			2500	--	--	μA
DMAG Undercurrent Protection Threshold Current	I_{DMAG_UCP}			25	50	75	μA

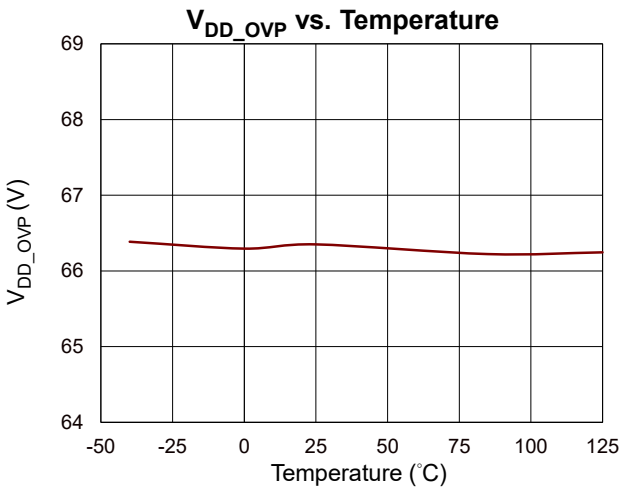
Note 6. Guaranteed by design.

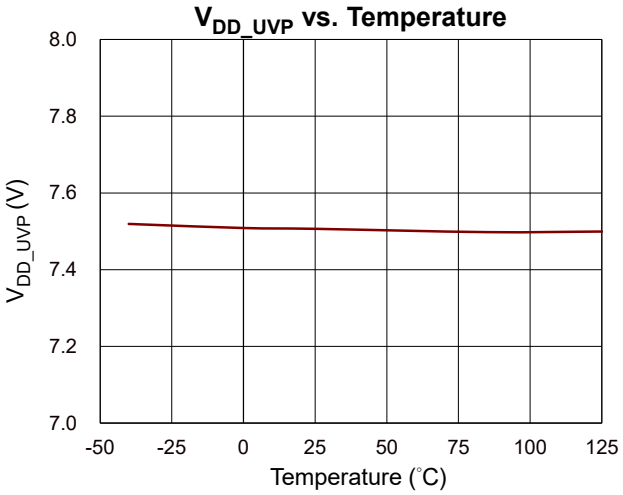
Note 7. The electrical characteristics of COMP input section are based on internal COMP signal (V_{COMPD}). $V_{COMPD} = V_{COMP} - V_F$, V_F = 0.9V when T_A = 25°C.

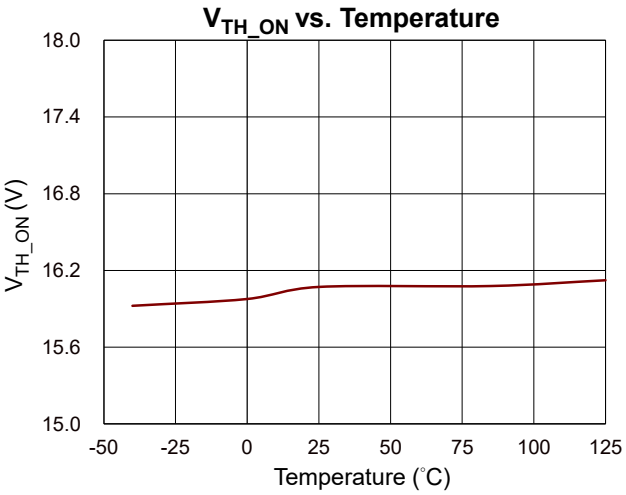
13 Typical Application Circuit

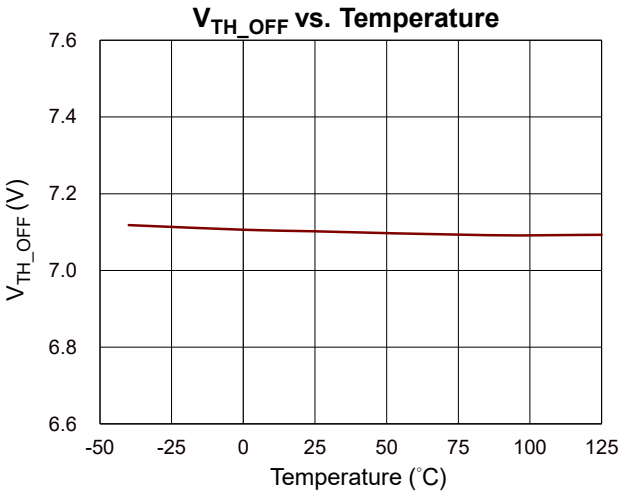


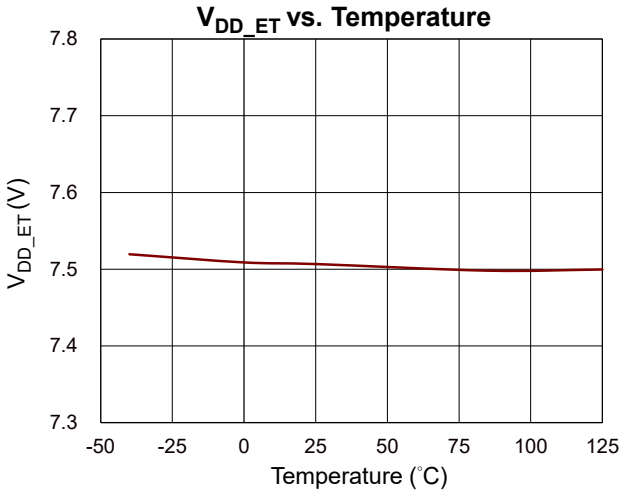
14 Typical Operating Characteristics

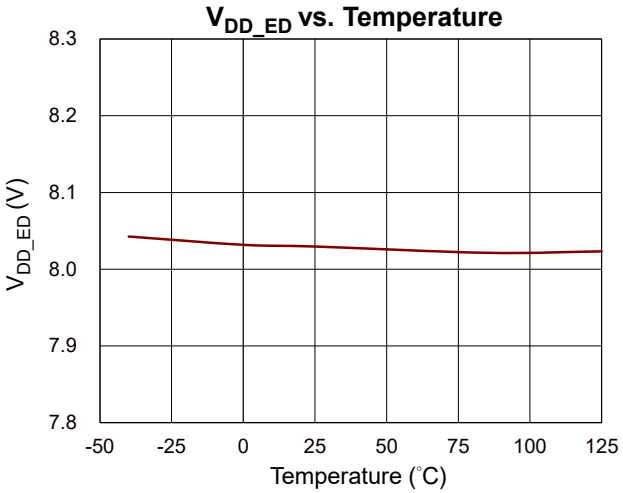


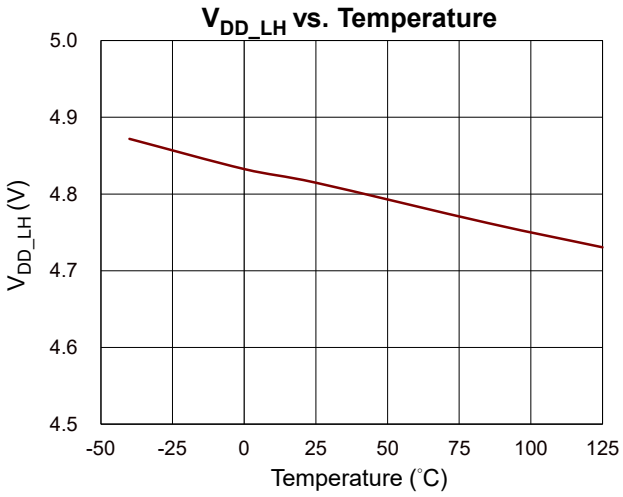


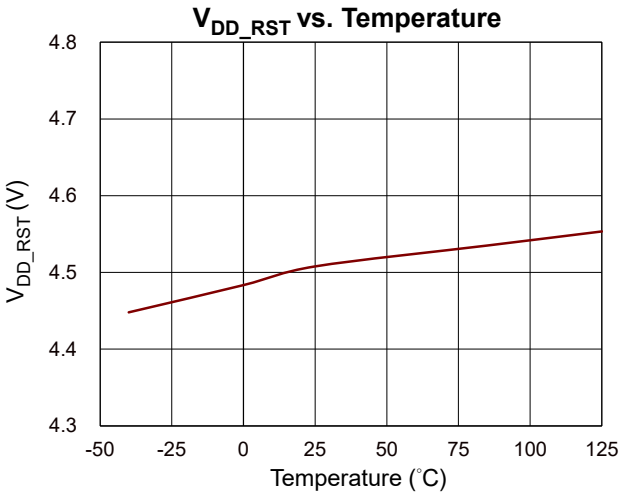


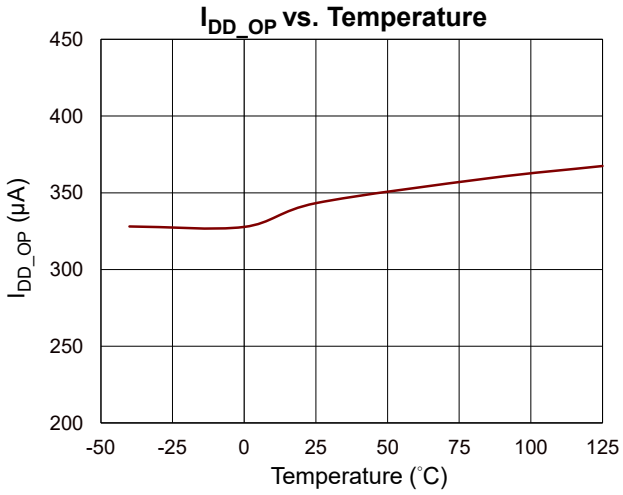


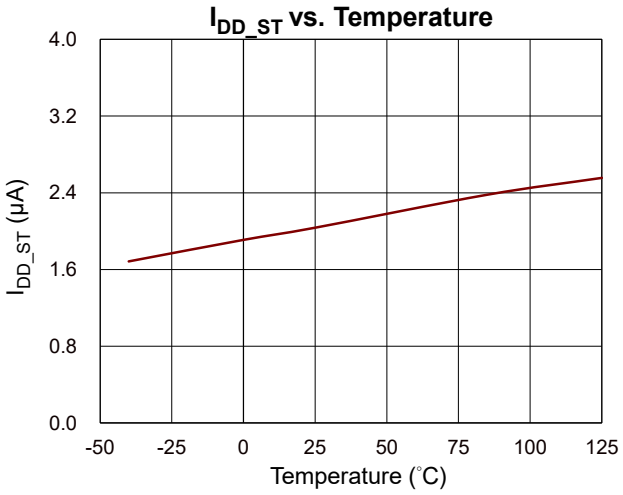


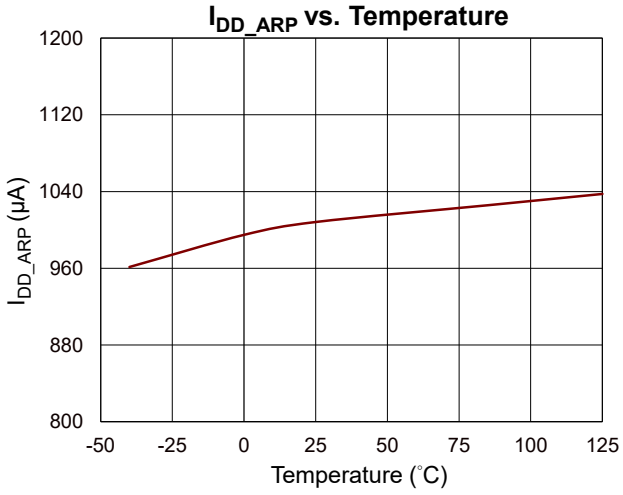


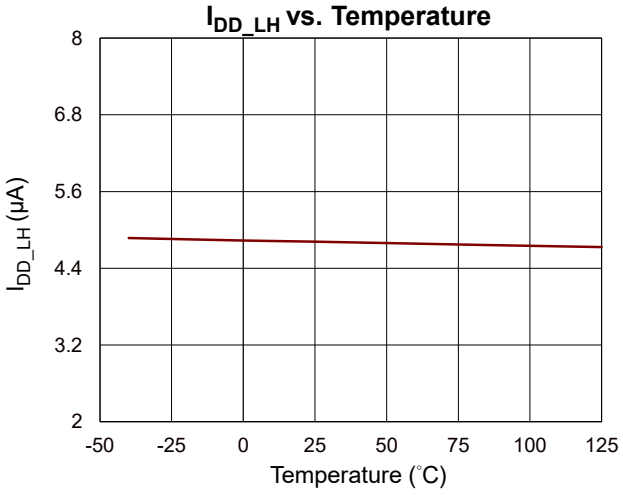


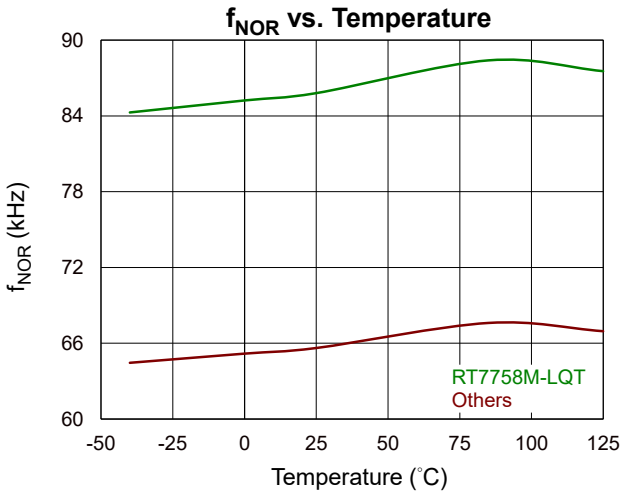


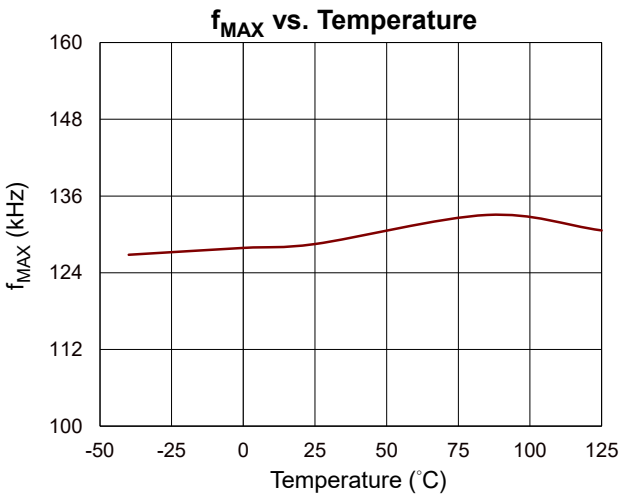


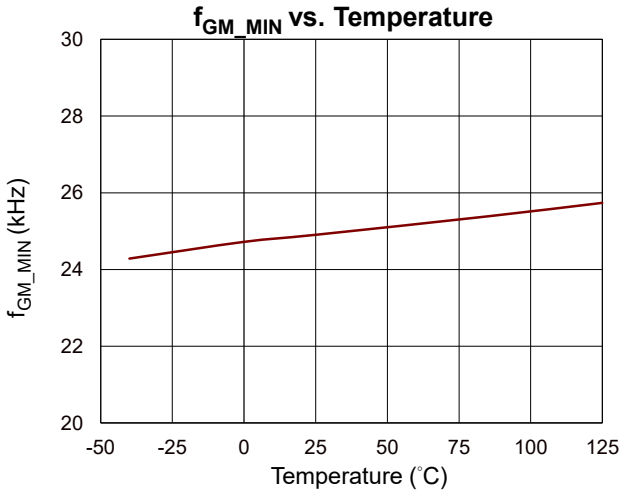


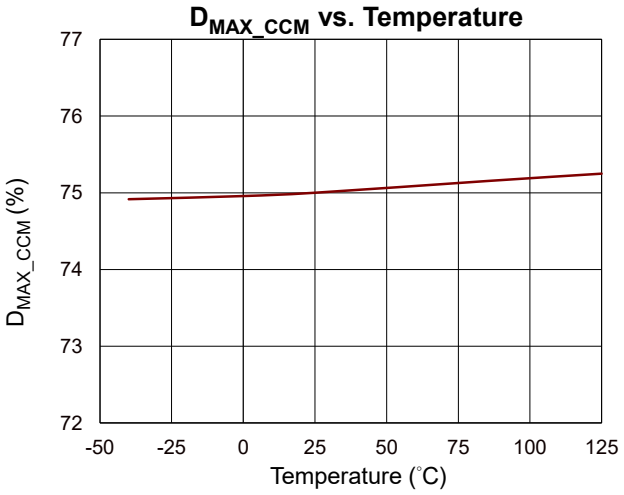


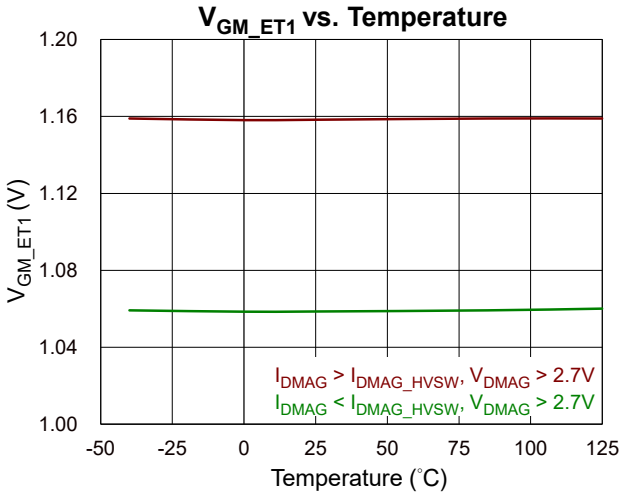


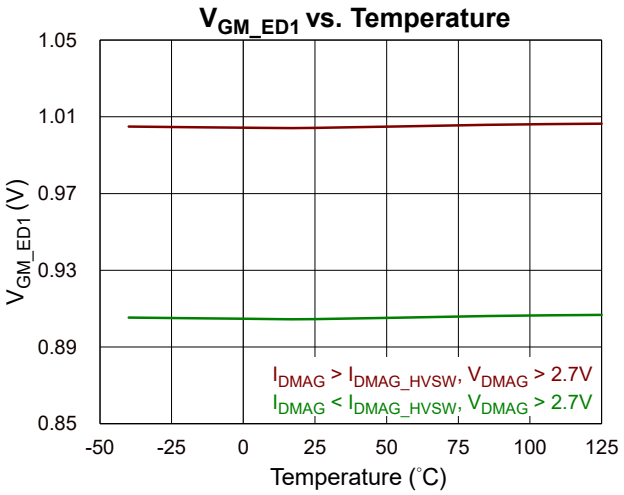


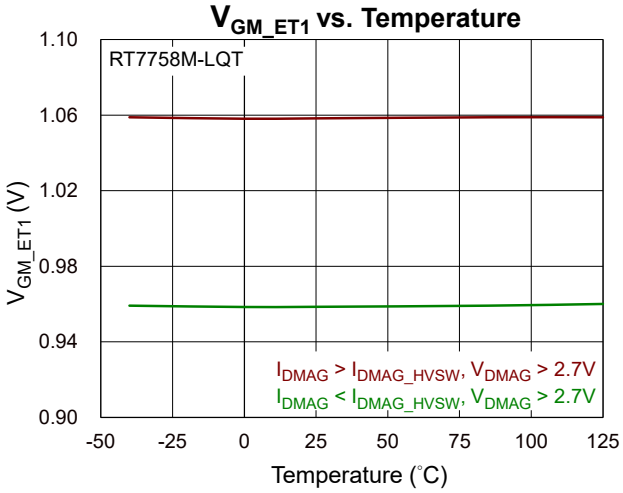


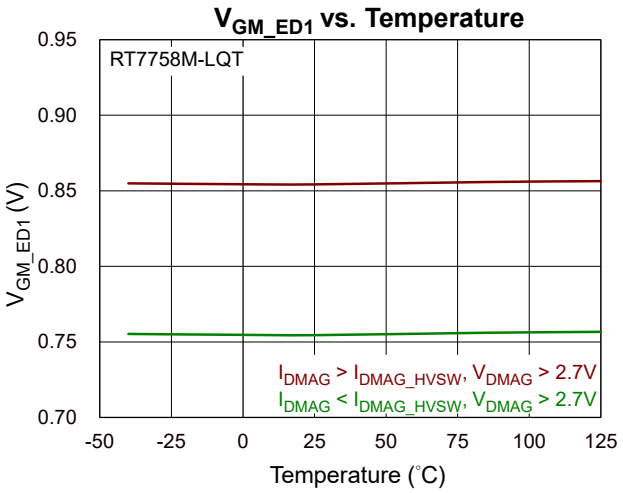


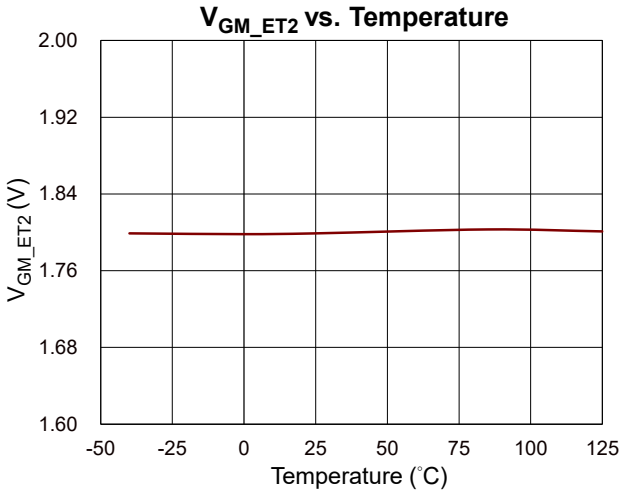


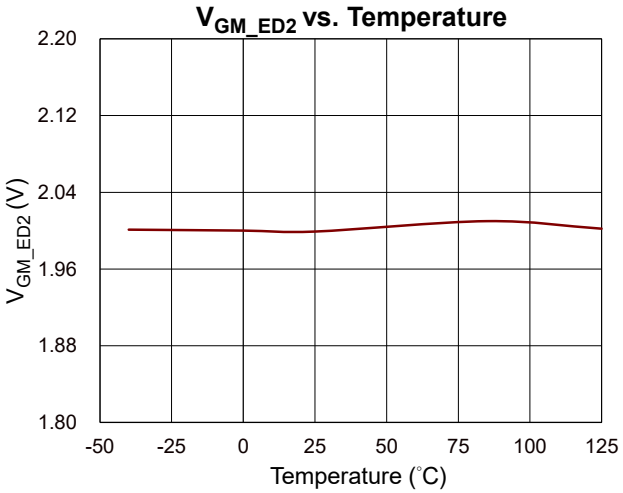


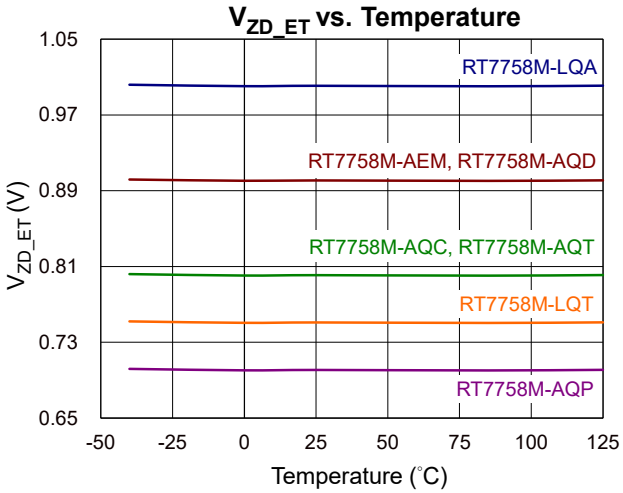


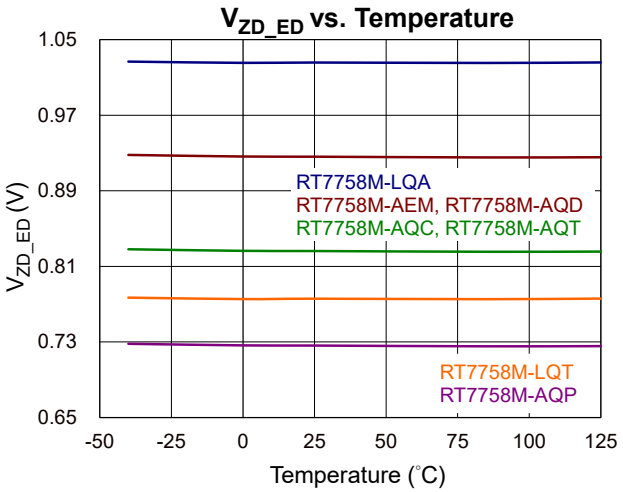


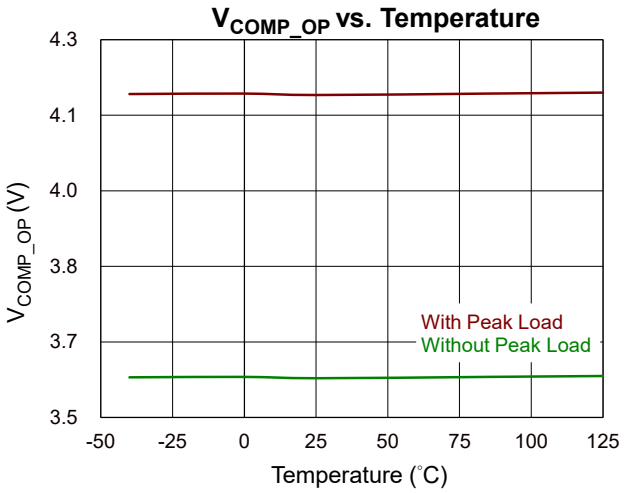


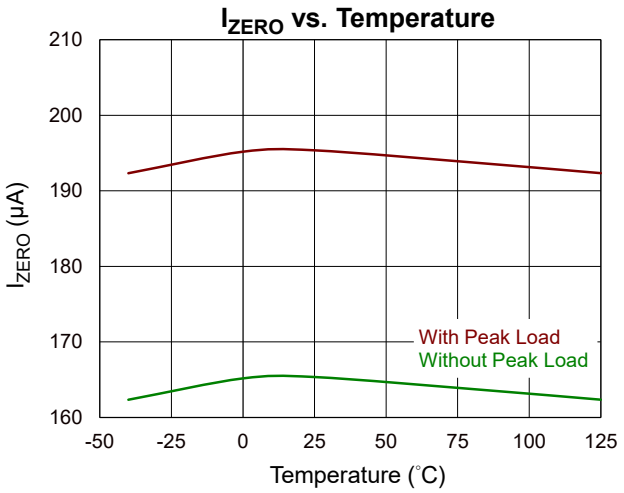


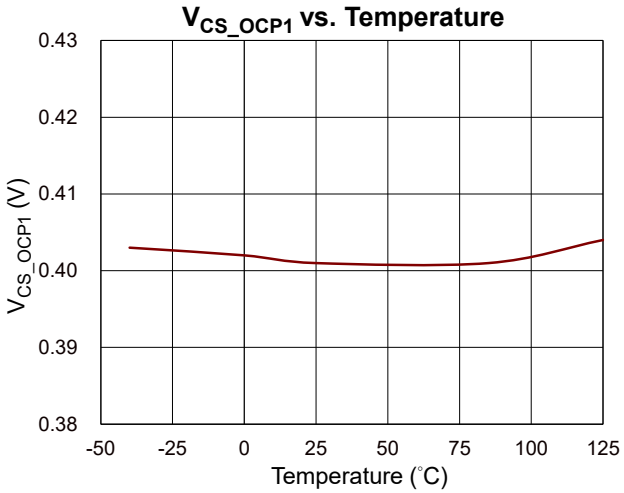


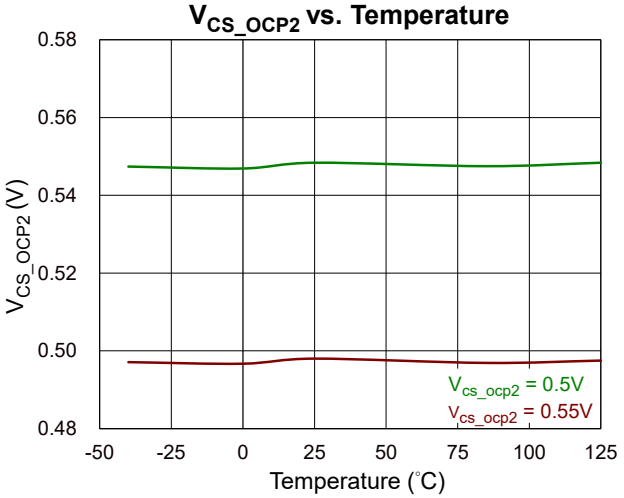


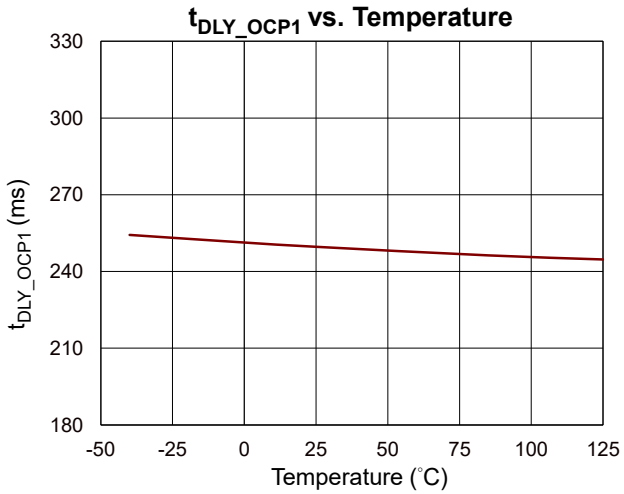


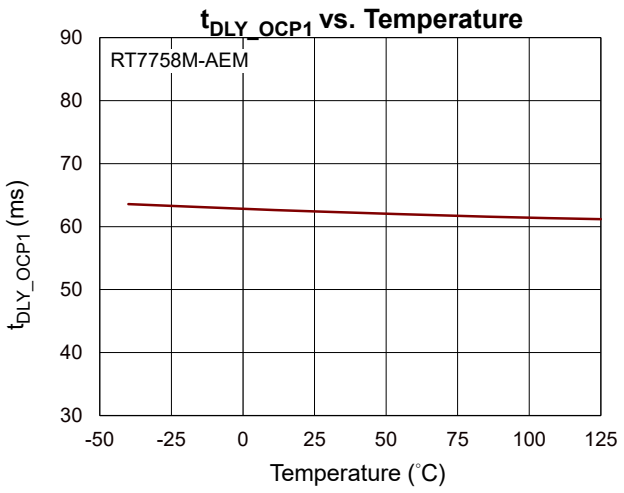


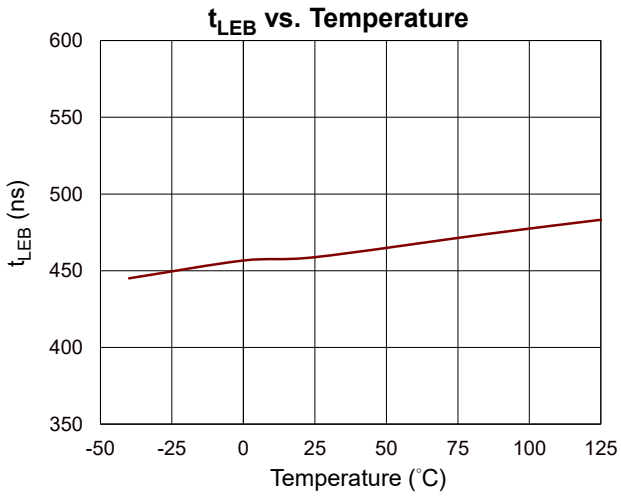


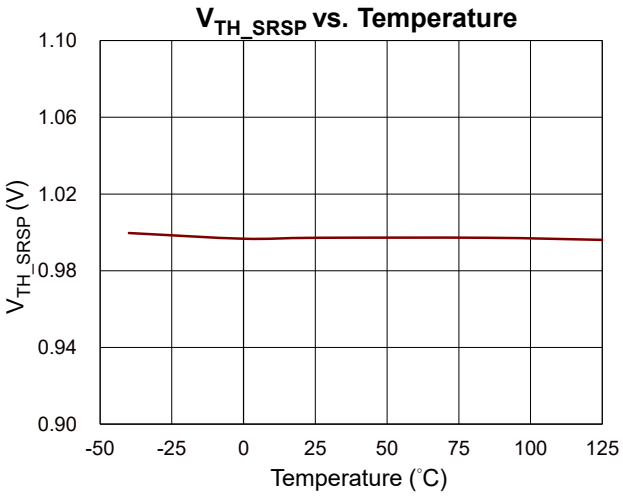


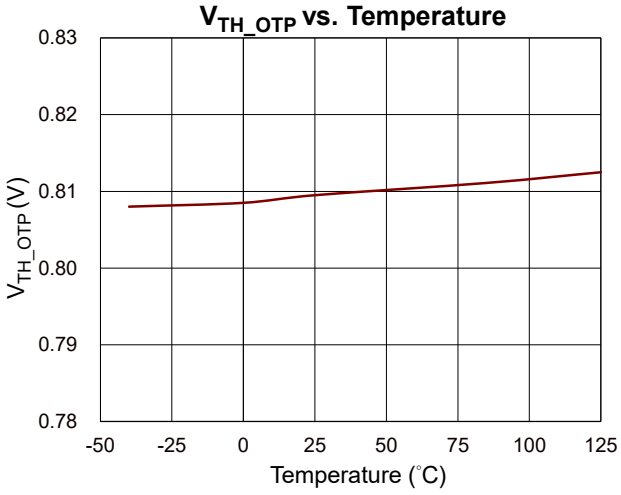


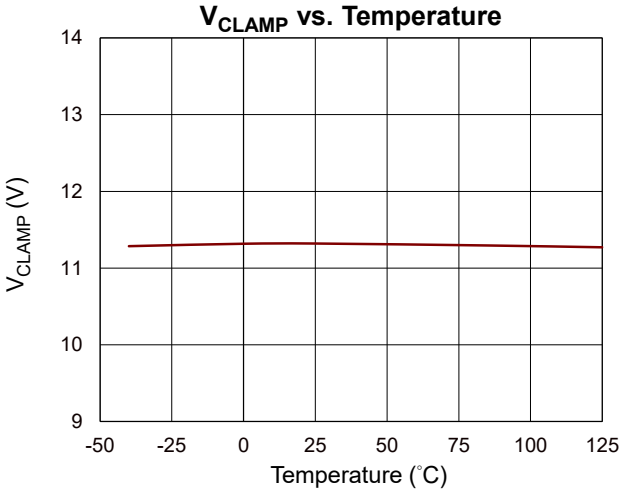


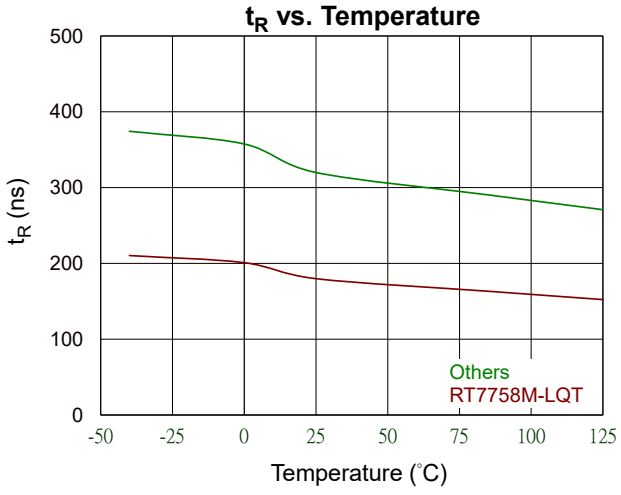


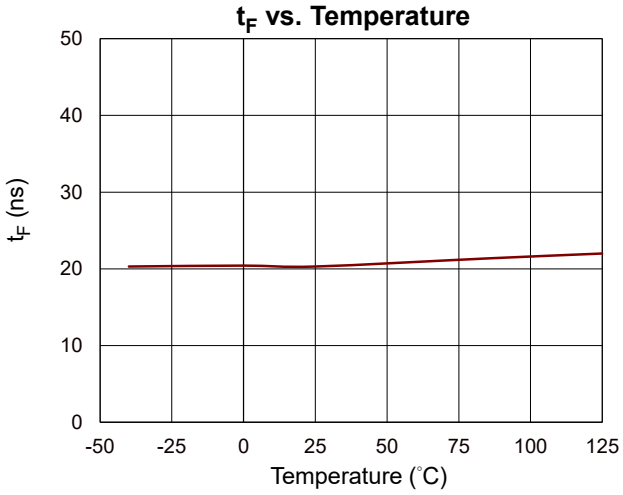


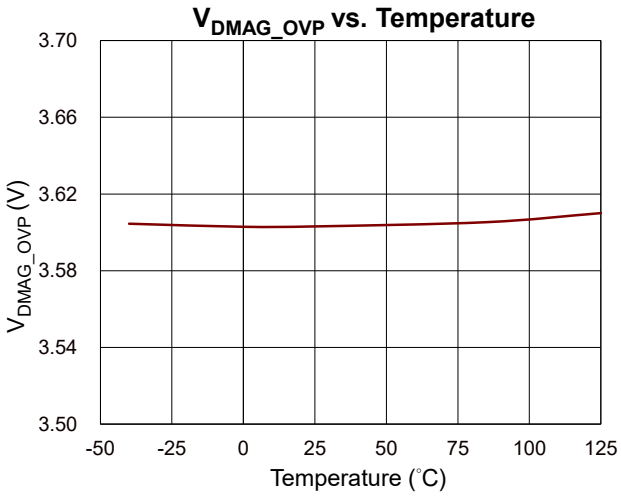


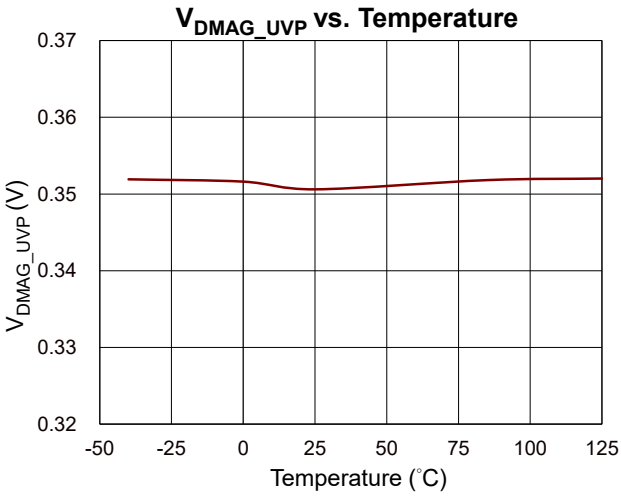


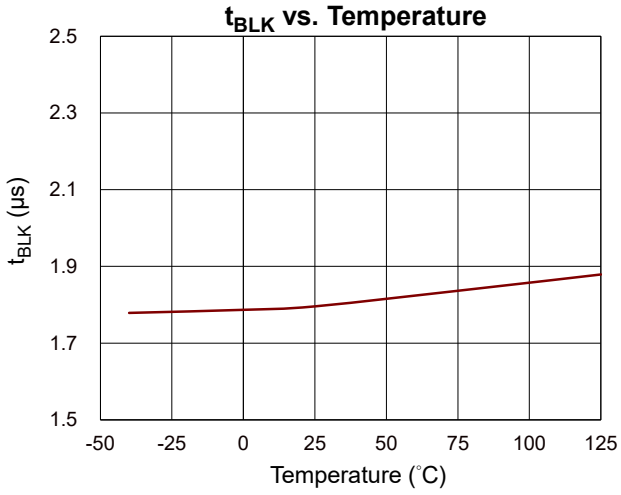


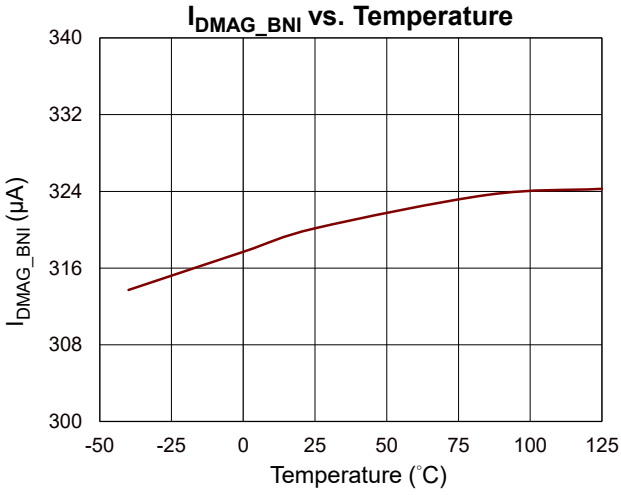


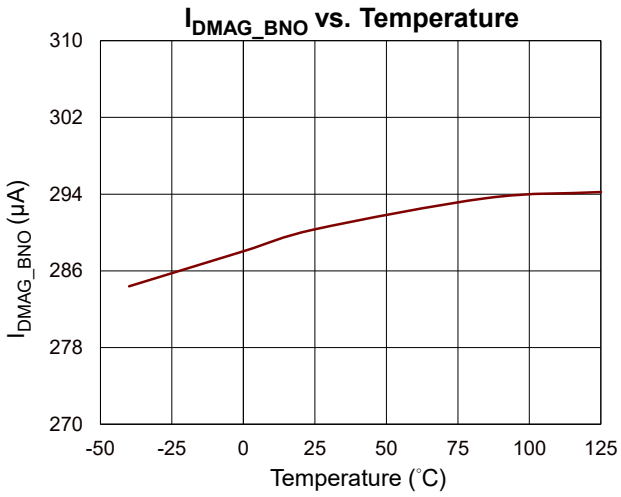


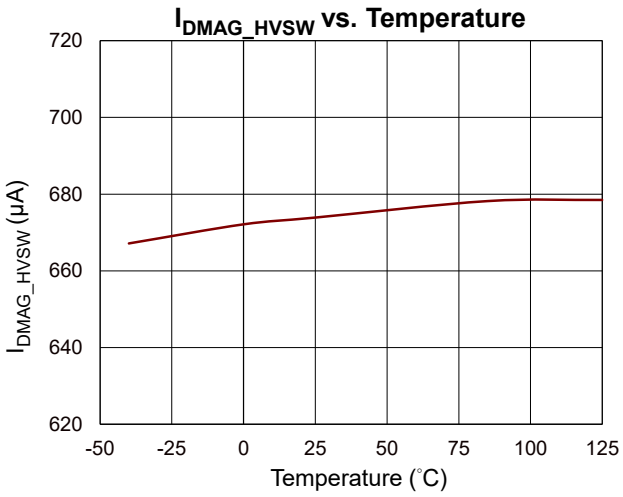


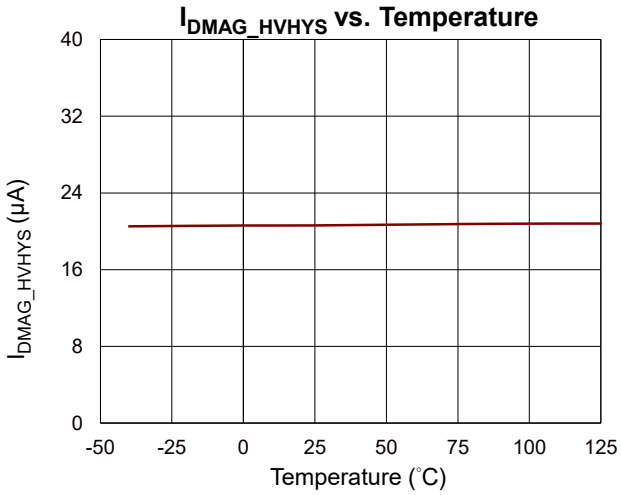


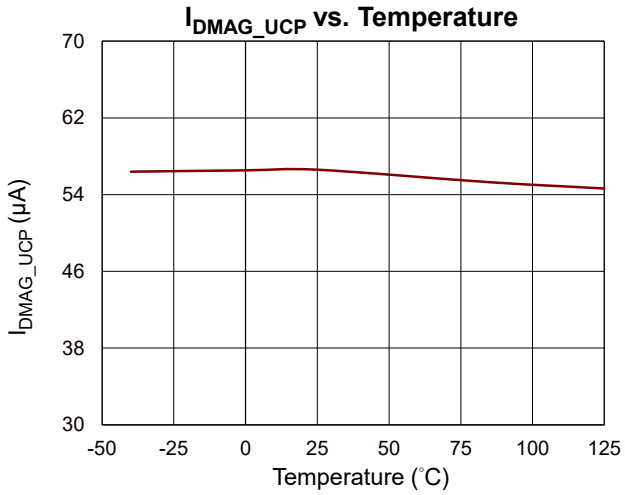












15 Operation

The RT7758M series is specifically designed to work with a USB PD controller or a programmable power adapter controller as a total solution. For applications with a wide output voltage range, the RT7758M features many innovations, including adaptive output overvoltage protection, adaptive overcurrent protection and adaptive loop stability control.

15.1 Multi-Mode PWM

The RT7758M is a PWM controller that provides a multi-mode control to optimize performance under different load conditions. With an internal oscillator to provide a PWM frequency for the system to operate in continuous conduction mode (CCM) or quasi-resonant mode (QR mode), this controller will automatically enter green mode under light load or no-load conditions.

15.2 Gate Driver

A totem-pole gate driver is designed to meet the requirements for both EMI and efficiency in low-power applications. An internal pull-down circuit is included to prevent the external MOSFET from being falsely turned on when VDD is too low and an undervoltage lockout (UVLO) event is triggered.

15.3 SmartJitter Technology

In general PWM controllers, a frequency jittering scheme is usually adopted to spread frequency spectrum in order to alleviate EMI problems. However, due to the inherent operating characteristics of the valley switching mode and the green mode, the frequency spectrum in high line conditions or in deeper extended valley switching conditions cannot be spread wide enough as expected, which degrades the suppression of EMI emissions.

The RT7758M employs RICHTEK's proprietary SmartJitter technology to optimize the frequency jittering range. This innovative technology can reduce EMI emissions of a switch-mode power supply as well as output ripple as a consequence of frequency jittering in all operation conditions.

15.4 Adaptive Loop Stability Control

The system loop gains can be different for applications with a wide range of output voltage. The RT7758M features proprietary adaptive loop stability control to adjust loop gain automatically, ensuring system stability across the wide range of output voltage.

15.5 Adaptive Overcurrent Protection

In general, a power system designed for 20V/3A may output a current of 12A when the output voltage decreases to 5V, for a constant output power condition. This may violate the LPS safety requirements for maximum output current, and cause damage to connected devices, such as the secondary USB PD controller RT7216KNE. To solve this, the RT7758M adopts a cycle-by-cycle current limit feature, which can automatically lower the current limit and maximum output current if the output voltage (V_{OUT}) is too low or the output current is too high. The protection mode is entered if the fault condition sustains for an overcurrent protection delay time (t_{DLY_OCP}).

15.6 Secondary Rectifier Short Protection (SRSP)

When a secondary rectifier or secondary MOSFET short-circuit condition occurs during the primary MOSFET on-time, the main transformer becomes saturated, and the rising rate of the primary-side current is then limited only by the leakage inductance of the transformer, which is about a few percentage of the primary magnetizing inductance. Therefore, the current slope is much higher than that in normal operation. In high line conditions, peak current through the primary MOSFET will become extremely high after the overcurrent protection delay time

elapses. To provide reliable protection, the RT7758M is designed to shut down in a few cycles once a secondary rectifier short-circuit condition is detected.

15.7 Deep Burst Mode

When the output is at light load, the system enters burst mode to reduce switching loss. During burst mode, the break time between switching cycles is naturally controlled by the feedback voltage. As the output load decreases, the burst mode frequency may fall within the range sensitive to human hearing. To reduce audible noise, the deep burst mode function ensures that the system frequency remains outside the sensitive range.

16 Application Information

(Note 8)

The RT7758M is a multi-mode PWM flyback controller providing different operational modes, such as green mode, and burst mode. The RT7758M can automatically switch among several control modes to optimize efficiency for the power system when operating under various load conditions.

16.1 Start-Up Circuit

To optimize power efficiency, bleeder resistors can be added to the start-up circuit. These resistors not only can reduce power loss but can reset latched-mode protections faster. Figure 1 shows the curve for IDD average current (I_{DD_Avg}) vs. bleeder resistance ($R_{Bleeder}$). The curve can be used to design appropriate bleeder resistance values.

During hiccup mode, the off-time duration is extended to minimize power loss and heat dissipation. During auto-recovery protection mode, the controller sinks a very small current, I_{DD_ARP}. The start-up current at maximum AC line input voltage must be smaller than the minimum I_{DD_ARP}. Otherwise, when the controller enters an auto-recovery protection mode, the VDD capacitor cannot be discharged to V_{TH_OFF} by the sinking current I_{DD_ARP} to restart the controller. The controller will then behave as in latched-protection mode or even trigger the silicon controlled rectifier (SCR) of VDD.

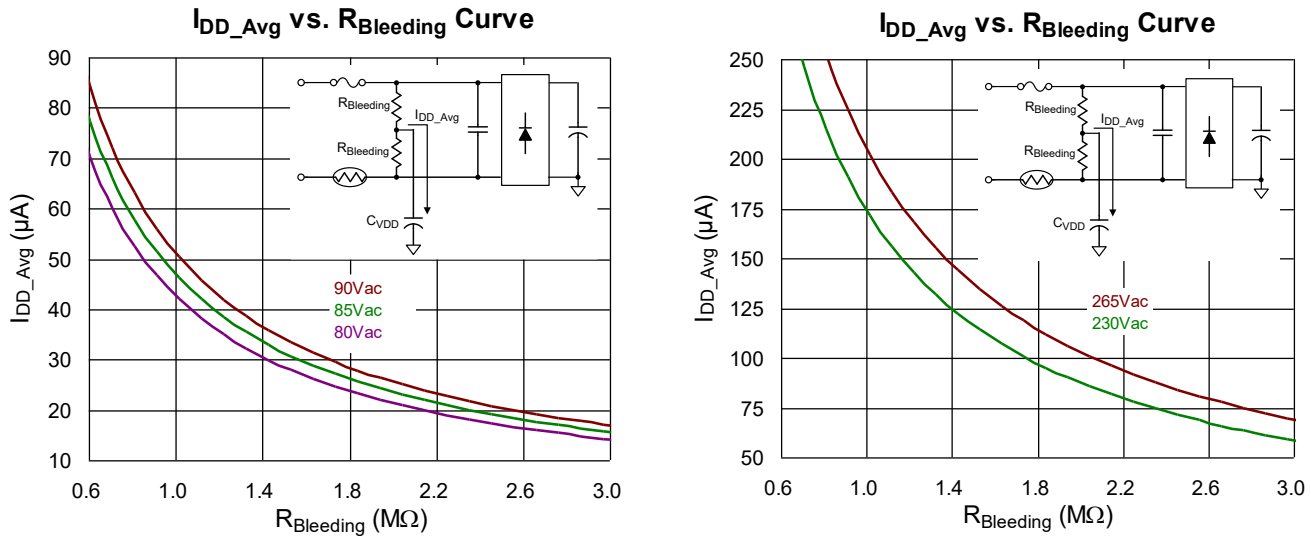


Figure 1. Start-Up Circuit

16.2 VDD Discharge Time in Auto Recovery Mode

Figure 2 shows the V_{DD} and V_{GATE} waveforms during an auto-recovery protection (for example, OCP). In this mode, the start-up resistors, the VDD sinking current, and the VDD decoupling capacitor affect the restart time. The VDD voltage discharge time ($t_{D\_Discharge}$) can be calculated using the following equation:

$$t_{D\_Discharge} = \frac{C_{DD} x (V_{DD\_DIS} - V_{TH\_OFF})}{I_{DD\_ARP} - I_{ST}}$$

where the C_{VDD} is the VDD decoupling capacitor, the V_{DD_DIS} is the initial VDD voltage after entering auto-recovery mode, the V_{TH_OFF} (typical) is the falling UVLO voltage threshold of the controller, the I_{DD_ARP} (typical) is the sinking current of the VDD pin in auto-recovery mode, and I_{ST} is the start-up current of the power system.

Note that the start-up current at high input voltage must be smaller than the I_{DD_ARP}. Otherwise, the VDD voltage cannot reach the V_{TH_OFF} to activate the next start-up process after an auto recovery protection event. Therefore, the system behavior will resemble that of latch mode.

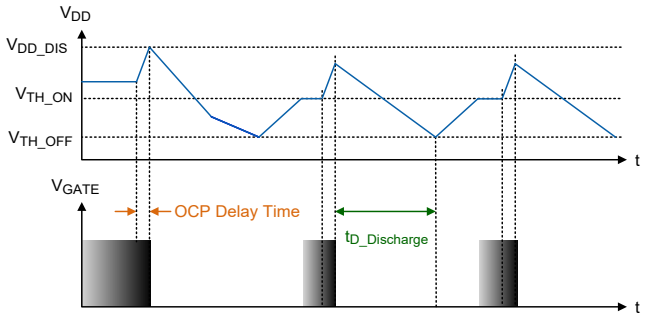


Figure 2. Auto-Recovery Mode (For Example, OCP)

16.3 VDD Holdup Mode

VDD holdup mode is implemented to prevent VDD from dropping below the turn-off threshold voltage (V_{TH_OFF}) when the system operates under light load, no load, or fast load transient conditions. VDD holdup mode can help reduce the power loss caused by the start-up resistor and meet the requirement for the start time. However, compared to burst mode, VDD holdup mode consumes more switching power loss. Hence, it is highly recommended that the system will not be designed to operate in this mode under light load or no-load conditions. If the system operates in VDD holdup mode and exceeds the VDD holdup mode delay time (256 cycles), the system will restart.

16.4 DMAG Pin

During the MOSFET on-time, the auxiliary winding voltage is negative, and the RT7758M outputs a clamp current, proportional to the input line voltage, to clamp the DMAG voltage at 0.1V. The RT7758M has defined two characteristics for the DMAG pin: the DMAG brown-in protection threshold current (I_{DMAG_BNI}) and the DMAG brown-out protection threshold current (I_{DMAG_BNO}). The bulk-capacitor brown-in and brown-out threshold voltages, V_{BULK_BNI} and V_{BULK_BNO}, can be programmed by adjusting R_{DMAG1} and R_{DMAG2} respectively at the DMAG pin, as shown in Figure 3.

Once one of the brown-in and brown-out threshold voltages is set, the other one can be determined accordingly. The bulk-capacitor brown-out threshold voltage V_{BULK_BNO} can be obtained according to the following equations:

$$V_{BULK\_BNO} = \frac{V_{BULK\_BNI} \times I_{DMAG\_BNO}}{I_{DMAG\_BNI}}$$

When the MOSFET turns off, the DMAG pin senses the output voltage of the power stage across the auxiliary winding, with a ratio equal to the turns ratio of the auxiliary and secondary windings, and then scales it with the resistive divider R_{DMAG2} / R_{DMAG1}, as shown in Figure 3. The voltage divider can be calculated using the following equation:

$$\begin{cases} \dfrac{\dfrac{V_{BULK\_BNI} \times N_A}{N_P} + 0.1}{R_{DMAG2}} + \dfrac{0.1}{R_{DMAG1}} = I_{DMAG\_BNI} \\ \dfrac{R_{DMAG2}}{\dfrac{(V_{O\_OVP} + V_F)}{V_{DMAG\_OVP}} \times \dfrac{N_A}{N_S} - 1} = R_{DMAG1} \end{cases}$$

where V_{O_OVP} is the output OVP threshold voltage.

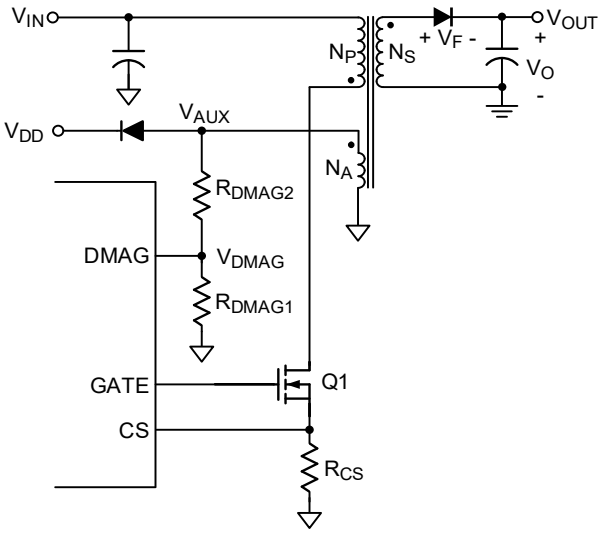


Figure 3. DMAG Pin Resistor

When the secondary-side current reduces to zero during the MOSFET turn-off period, the magnetic inductance (L_P) of the transformer and the equivalent parasitic capacitance (C_{DS}) of the MOSFET induce resonant oscillations on the DMAG pin, as shown in Figure 4.

The RT7758M with valley switching version provides a valley switching function to save switching loss and improve power supply unit (PSU) efficiency. The valley switching function only works when the resonance period (t_{DCM}) is longer than 0.8μs and the DMAG voltage is higher than 0.25V. Otherwise, the DMAG pin cannot detect the valley signal and the system will become hard-switching. During the circuit design stage, tolerances of magnetic inductance (L_P) and the equivalent parasitic capacitance (C_{DS}) must be considered.

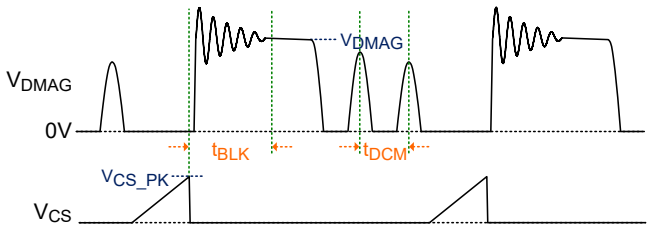


Figure 4. Resonant Oscillations on the DMAG Pin

16.5 Adaptive Blanking Time

When the MOSFET just turns off, the leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induces resonant oscillations on the DMAG pin, as shown in Figure 4. The resonant oscillations may cause the controller to falsely trigger DMAG overvoltage protection ($V_{DMAG} > V_{DMAG\_OVP}$), which fails to reflect the actual output overvoltage fault condition ($V_O > V_{O\_OVP}$), causing the controller to malfunction. As the load increases, the duration of the resonant oscillation may also increase. It is recommended to add a small bypass capacitor, sized from 10pF to 22pF and placed as close to the DMAG pin as possible, to suppress such noise. A larger bypass capacitor may cause the DMAG voltage to phase-shift too much, preventing the MOSFET from switching on at the exact valley points.

To address this, the RT7758M provides an adaptive blanking time to prevent the DMAG overvoltage protection from being falsely triggered. The built-in blanking time for the overvoltage protection (t_{BLK}) varies with the system peak current limit (V_{CS_PK}), and can be calculated by using the following equation:

$t_{BLK} = 1.8\mu s + 1.75\ (\mu s/V) \times V_{CS\_PK}$.

16.6 Line Compensation

The RT7758M provides line compensation to ensure a constant output current limit (I_{O_MAX}) over a wide range of AC line input voltages, as shown in Figure 5.

For different power stage designs, the propagation delay may vary with the transformer inductances, parasitic capacitances of the MOSFET, or series resistances at the gate of the MOSFET. However, with the same design, the current overshoot caused by the propagation delay may become significant at high line, where the inductor current di/dt is higher. There is a significant difference between the overshoot at high input voltage and that at low input voltage, affecting the actual peak current.

To compensate for this difference and achieve accurate overcurrent protection under different input line voltages, the RT7758M outputs a line compensation current on the CS pin to add an offset voltage proportional to the input voltage by adding a propagation delay resistor (R_{PDC}). The propagation delay differences due to different input line voltages can be compensated by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to keep the output current limit constant across different line voltages.

As a starting point, $R_{PDC} = 470\Omega$ and $C_{RC} = 100pF$ can be used as reasonable initial settings for line compensation. In Figure 6, curve (1) represents an ideal output current limit curve for overcurrent protection, which remains constant from low line to high line input voltages. If the output current limit curve is like curve (2), the resistance R_{PDC} should be increased. However, if the output current limit curve is like curve (3), the capacitance C_{RC} should be increased. The output current limit (I_{O_MAX}) under different line voltages can be optimized by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to achieve accurate overcurrent protection.

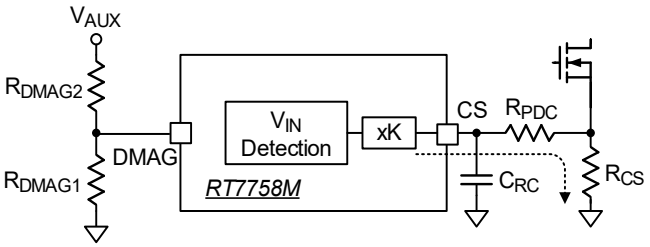


Figure 5. Functional Block Diagram of Line Compensation

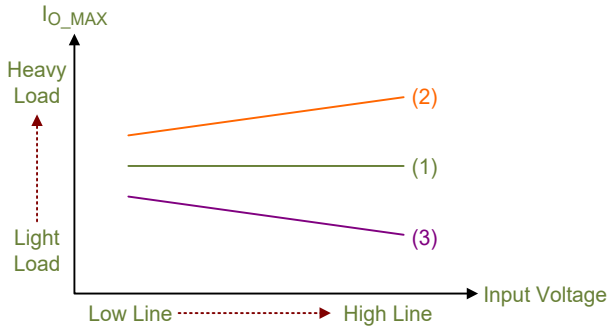


Figure 6. Output Current Limits for Overcurrent Protection

16.7 External Over-Temperature Protection (Ext-OTP)

The RT7758M includes a programmable external over-temperature protection (External OTP), implemented with a fast diode, a resistive voltage divider, and an external NTC resistor (R_{NTC}) to sense the power system temperature, as shown in Figure 7. During the MOSFET off-time, the auxiliary winding voltage (V_{AUX}) is constant, and the CS voltage, sampled as a fraction of the clamped voltage (V_{AUX_Clamp}) and compared with the internal reference voltage to set the over-temperature protection threshold voltage. When the system temperature rises, the resistance of the NTC resistor decreases. By adjusting the value of the setting resistor (R_{SET}), the threshold temperature for over-temperature protection can be programmed. During the off-time, if the sampled CS voltage exceeds the external OTP threshold voltage (V_{TH_OTP}) and sustains for the external OTP delay time (t_{D_OTP}), the controller will shut down and the switching will stop. Once the OTP condition is removed, the controller with the auto-recovery option will automatically resume its operation. The design equation for the external OTP threshold voltage is expressed as below:

$$V_{TH\_OTP} = \left[\left(V_{O\_NOR\_MAX} + V_F \right) \times \frac{N_A}{N_S} - V_{F\_OTP} \right] \times \frac{R_{PDC} + R_{CS}}{R_{NTC\_OTP} + R_{SET} + R_{PDC} + R_{CS}}$$

where $V_{O\_NOR\_MAX}$ is the maximum normal output voltage, and R_{NTC_OTP} is the NTC resistance at the threshold temperature for external OTP.

It is highly recommended to use a fast diode ($C_T \leq 5pF$ and $t_{rr} \leq 50ns$), such as, the 1N4148 or BAV21 series, for external OTP applications. This helps prevent the CS pin from incorrect regulation or damage caused by negative voltage spikes.

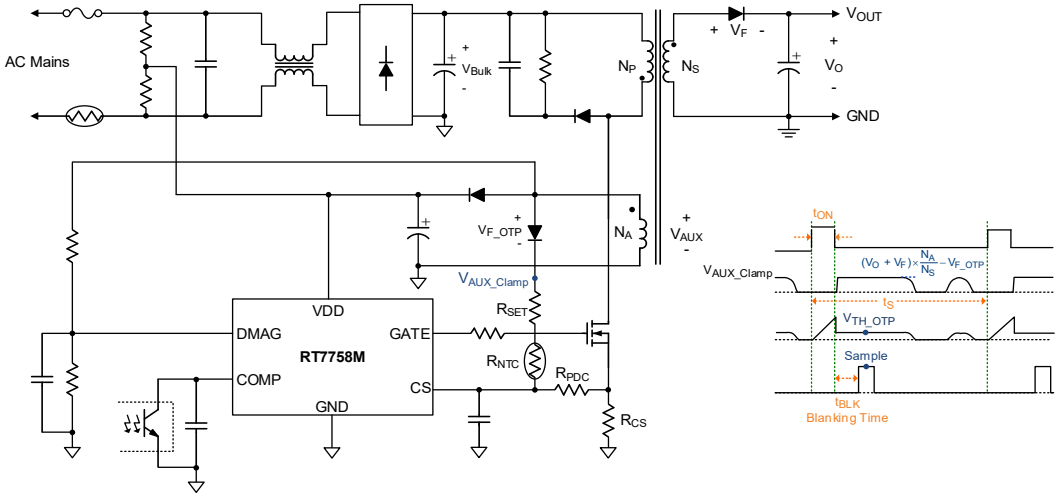


Figure 7. Application Circuit of External Over-Temperature Protection

16.8 Resistors at the GATE Pin

As shown in the typical application circuit in Figure 8, a resistor (R_G) can be applied to mitigate ringing spikes induced by the gate drive loop. Therefore, the value of the resistor (R_G) should be chosen carefully to meet the requirements for both EMI and efficiency in applications.

The RT7758M has a built-in discharge resistor (R_{ID}), internally connected from the GATE pin to GND, to prevent the MOSFET from suffering any uncertain conditions. However, if the GATE pin is open-circuited to the gate of the MOSFET, the MOSFET may be falsely triggered by the stored charge on the gate-to-drain parasitic capacitor (C_{GD}) of the MOSFET and then be damaged. Therefore, it is recommended to add an external discharge resistor (R_{ED}) between the gate of the MOSFET and GND so that the charge stored on the parasitic capacitor (C_{GD}) can be discharged by this external discharge resistor. This ensures that the MOSFET is protected from being falsely triggered even if the RT7758M is not in place or the GATE pin is open-circuited.

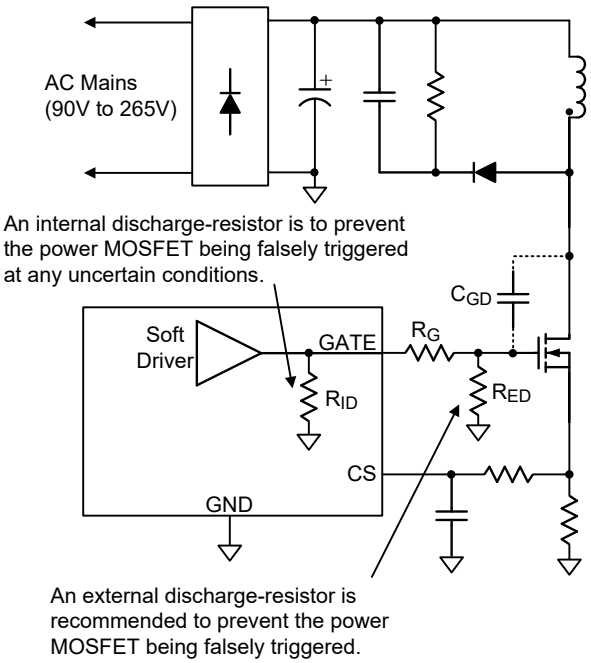


Figure 8. Resistors at the GATE Pin

16.9 Feedback Resistor

To enhance efficiency at light load, the power loss caused by the feedback resistor, as shown in Figure 9, must be reduced. Since the current through the feedback resistor is very small, a shunt regulator (such as the TL431), especially with its minimum regulated current, should be carefully chosen to ensure that the shunt regulator can still regulate the output voltage at such a small cathode current.

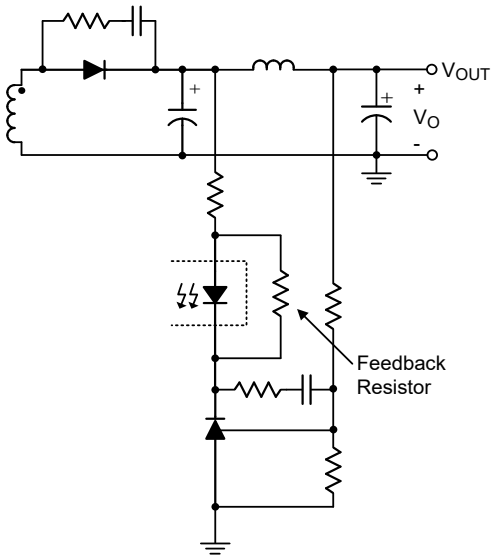


Figure 9. Feedback Resistor

16.10 Negative Voltage Spike on Each Pin

Any negative voltage less than −0.3V on each controller pin may cause a large injection current into the substrate, potentially damaging the controller or falsely triggering the circuit. For example, the negative voltage spikes at the CS pin may result from a poor PCB layout or the inductance of the current sense resistor. Therefore, an R-C filter, as shown in Figure 10, is recommended to prevent the CS pin from being damaged by the negative voltage spikes. During the circuit design stage, proper PCB layout and component selection must be carefully considered.

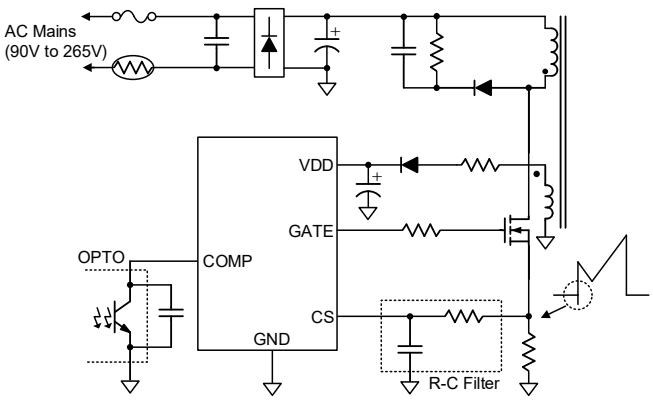


Figure 10. R-C Filter on the CS Pin

16.11 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 254.2°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (254.2°C/W) = 0.39W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 11 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

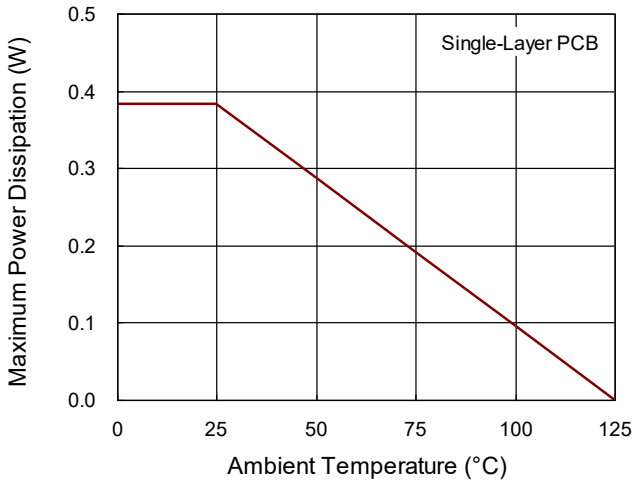


Figure 11. Derating Curve of Maximum Power Dissipation

16.12 Layout Considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch-mode power supply (SMPS). It is recommended to follow the following PCB layout guidelines when designing a switch-mode power supply:

- The current path (1), starting from the bulk capacitor, through the transformer, the MOSFET, the resistor R_{CS} and back to the bulk capacitor, is a high-frequency and high-current loop. Another high-frequency and high-current loop is the current path (2), which is from the GATE pin, through the MOSFET, the resistor R_{CS}, and back to the IC ground. These two paths should be kept as small as possible to decrease noise coupling and should be kept away from other low-voltage traces, such as IC control circuit paths.
- The path (3), starting from the auxiliary winding, through the resistor, the diode, and the VDD capacitor to the VDD pin, is also recommended to be as short as possible.

  Additionally, the VDD capacitor should be placed as close to the VDD pin as possible.
- The path (4) from the RCD snubber circuit to the MOSFET should also be kept short as it is a loop with high switching frequency.
- The ground traces of the bulk capacitor (a), the MOSFET (b), the VDD capacitor (c), the auxiliary winding (d) and the IC control circuit (e) should be separated to reduce noise, output ripple and EMI emission. The ground traces of the auxiliary winding (d) and the IC control circuit (e) are connected at the VDD capacitor ground (c). Then the connected ground trace goes through the VDD capacitor ground (c), the MOSFET ground (b), and to the bulk capacitor ground (a) in turn. The area of the bulk capacitor ground trace should be large enough.
- The bypass capacitor should be placed as close to the controller as possible.

- In order to reduce the reflected trace inductance and EMI emissions, the trace connecting the secondary winding, the output diode, and the output filter capacitor should be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to facilitate heat dissipation from the diode.

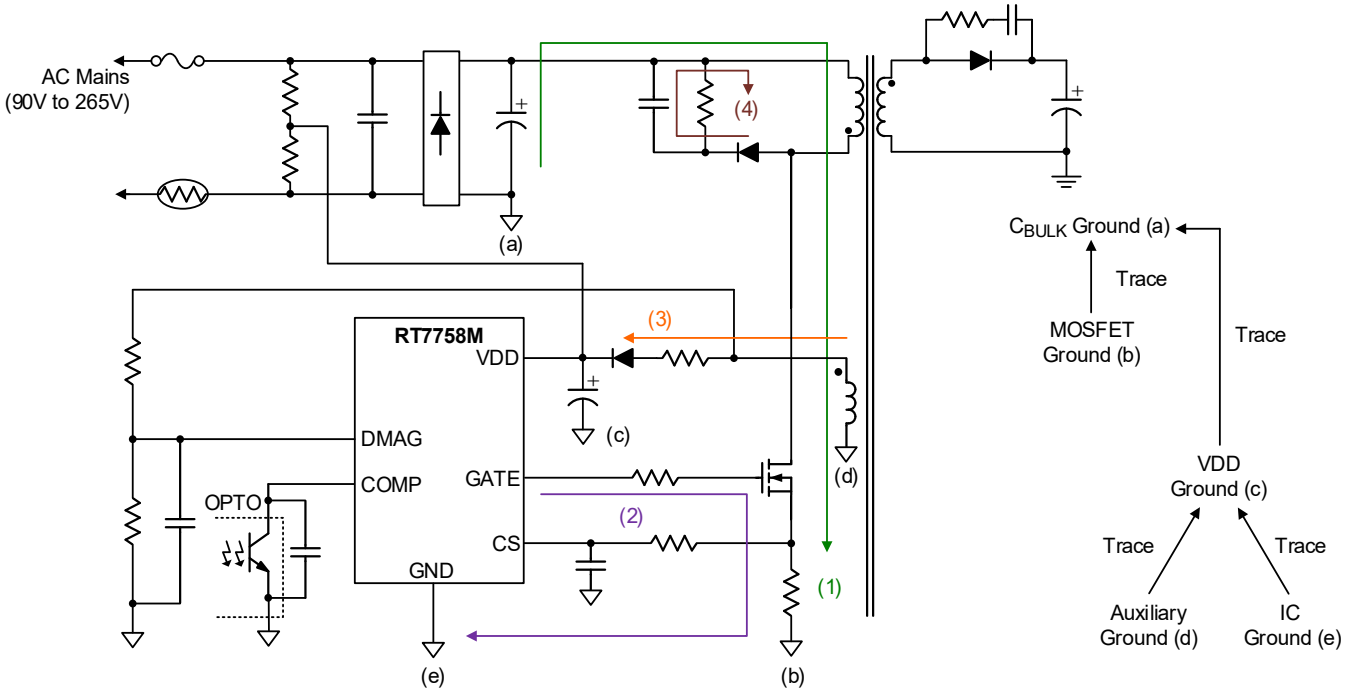
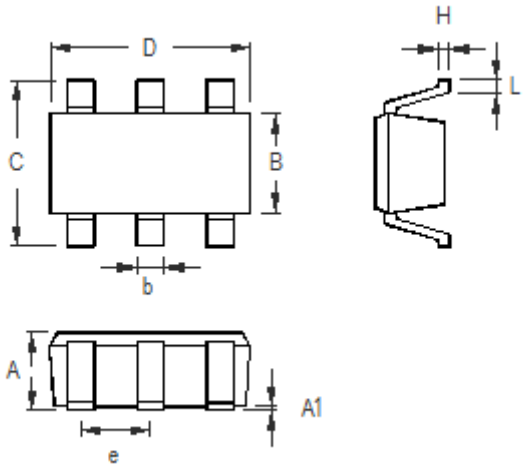


Figure 12. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

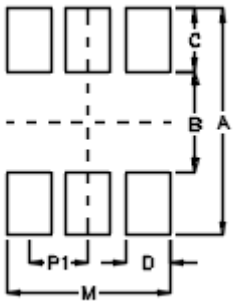
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

18 Footprint Information

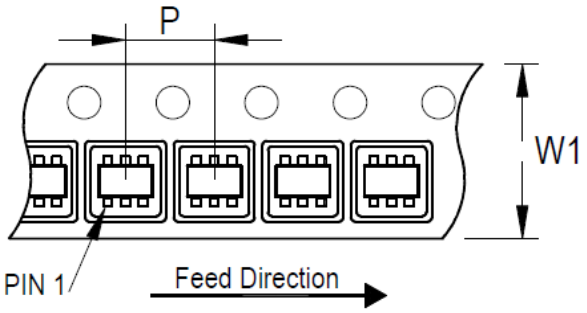


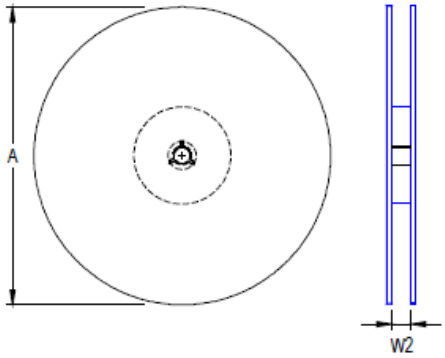
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

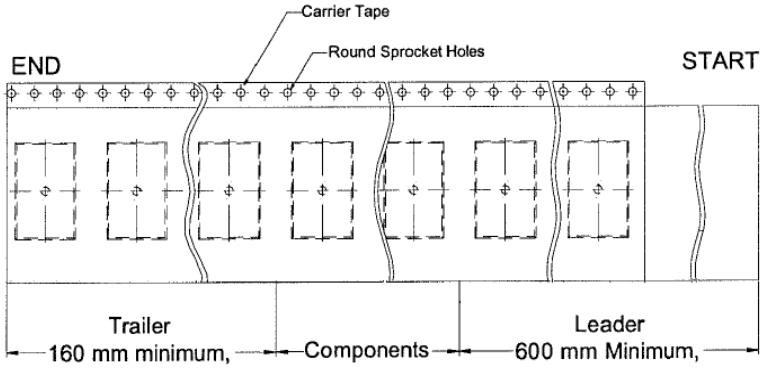
19 Packing Information

19.1 Tape and Reel Data

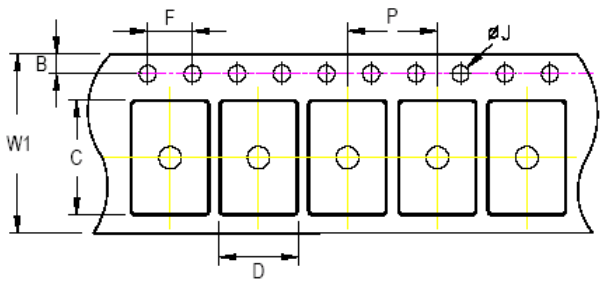
SOT/TSOT-23-6/8:

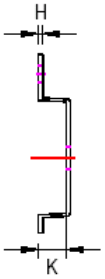






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
SOT-23-6	8	4	180	7	3,000	160	600	8.4/9.9





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-6	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description
00	2026/4/16	First Edition