PowerZero™ Series PWM Flyback Controller

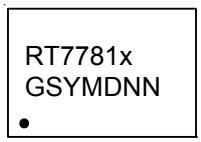
General Description

The RT7781 is a series of high-performance current mode PWM controllers with Richtek proprietary PowerZero™ technology. The PowerZero™ provides an excellent green power solution, especially under light-load and no-load conditions. The integrated high-voltage device provides fast start-up function without external start-up resistors. It also features brown-in and brown-out detection.

The RT7781 offers complete protection functions such as internal Over-Temperature Protection (OTP), Over-Load Protection (OLP) and VDD Over-Voltage Protection (OVP). It also features Secondary Rectifier Short-circuit Protection (SRSP) and Current Sensing pin (CS) open-circuit protection. Due to these protections, design of power supply unit becomes simple and reliable.

The RT7781 provides several versions, shown in the RT7781 version table, for various applications. It is targeted for cost-effective and compact power supply units such as NB adaptors.

Marking Information



RT7781xGS : Product Number

x : G/L/A/T/C

YMDNN : Date Code

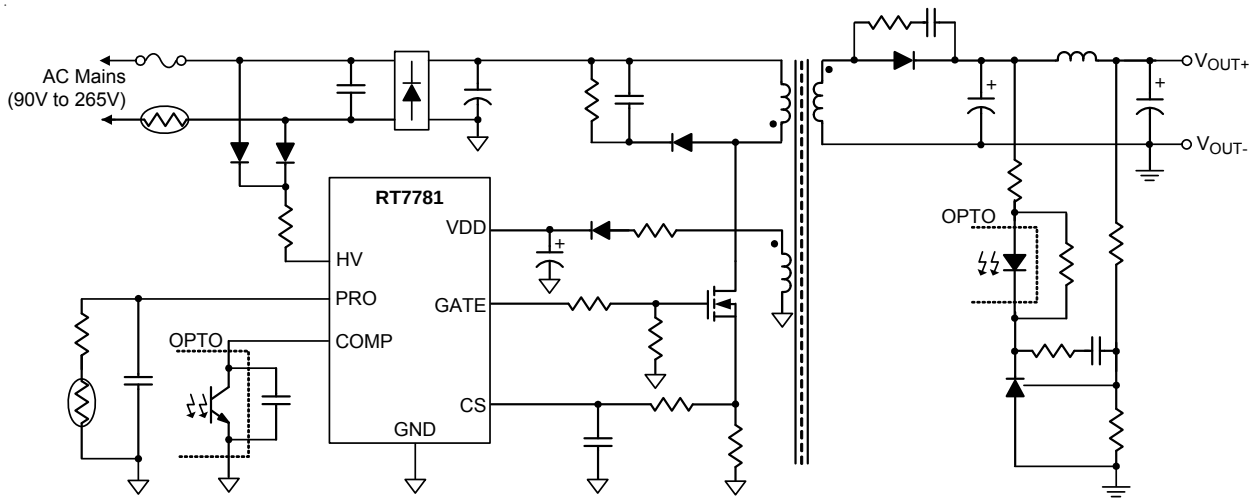
Features

- **PowerZero™ Technology**
  - **Integrated 700V Start-Up Device**
  - **Brown-In and Brown-Out**
- **Low No-Load Input Power (<50mW) (RT7781G/L/A/C)**
- **Low No-Load Input Power (<30mW) (RT7781T)**
- **Accurate Over Load Protection**
- **Driver Capability : 400mA/–400mA**
- **PRO Pin for Arbitrary External Protection (RT7781G/L/A/T)**
- **ACD Pin for TV Application (RT7781C)**
- **Disable Mode for 30mW Solution (RT7781T)**
- **Jittering Frequency**
- **Soft Driving for Reducing EMI Noise**
- **VDD Over Voltage Protection**
- **Internal Over Temperature Protection**
- **Secondary Rectifier Short Protection**
- **CS Pin Open Protection**
- **RoHS Compliant and Halogen Free**

Applications

- NB Adaptor
- Switching AC/DC Adaptor with Low No-Load Input Power
- TV and Monitor Applications
- Open Frame Power Supply

Simplified Application Circuit



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Ordering Information

RT7781□□□

- Package Type
  S : SOP-7
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- RT7781 Version (Refer to Version Table)

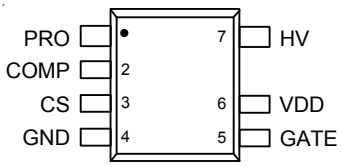
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

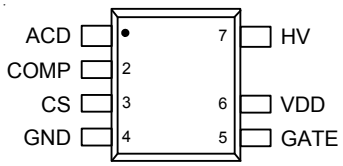
Pin Configurations

(TOP VIEW)



RT7781G/L/A/T

SOP-7



RT7781C

SOP-7

RT7781 Version Table

Version	RT7781G	RT7781L	RT7781A	RT7781T	RT7781C
Frequency	65kHz	65kHz	65kHz	65kHz	65kHz
OLP and SRSP	Auto Recovery	Auto Recovery	Latch	Auto Recovery	Auto Recovery
OLP Delay Time	56ms	56ms	56ms	56ms	56ms
VDD OVP (27V)	Auto Recovery	Latch	Latch	Latch	Auto Recovery
V_{PRO} > 1.8V	Latch	Latch	Latch	Latch	X
0.5V > V_{PRO} > 0.3V	Auto Recovery	Latch	Latch	Latch	X
V_{PRO} < 0.3V	Auto Recovery	Auto Recovery	Latch	Auto Recovery	X
ACD Pin	X	X	X	X	Yes
Disable Mode	X	X	X	Yes	X

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Functional Pin Description

Pin No.	Pin Name	Pin Description
1	PRO	External Protection Input for OVP or OTP. (RT7781G/L/A/T)
	ACD	Output for AC Voltage Brown-Out Detection. (RT7781C)
2	COMP	Feedback Voltage Input. Connect an opto-coupler to close the control loop and achieve output voltage regulation.
3	CS	Current Sense Input. The current sense resistor between this pin and GND is used for current limit setting.
4	GND	Ground of the Controller.
5	GATE	Gate Driver Output for the External MOSFET.
6	VDD	Supply Voltage Input. The controller will be enabled when VDD exceeds V_{TH_ON} and disabled when VDD decreases lower than V_{TH_OFF}.
7	HV	High Voltage Input for Start-Up. This pin can withstand high voltage up to 700V.

Function Block Diagram

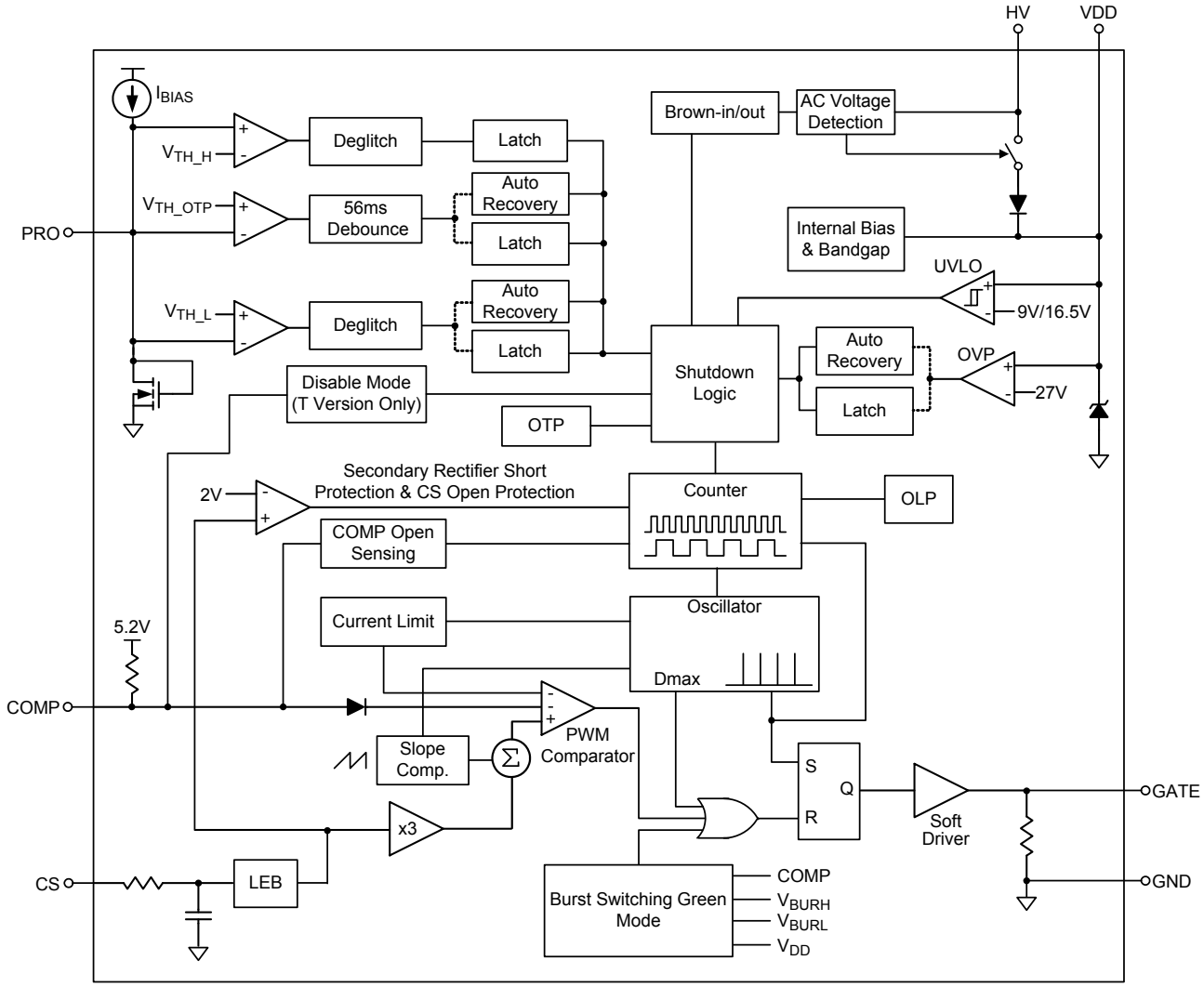

Figure 1. RT7781G/L/A/T Block Diagram

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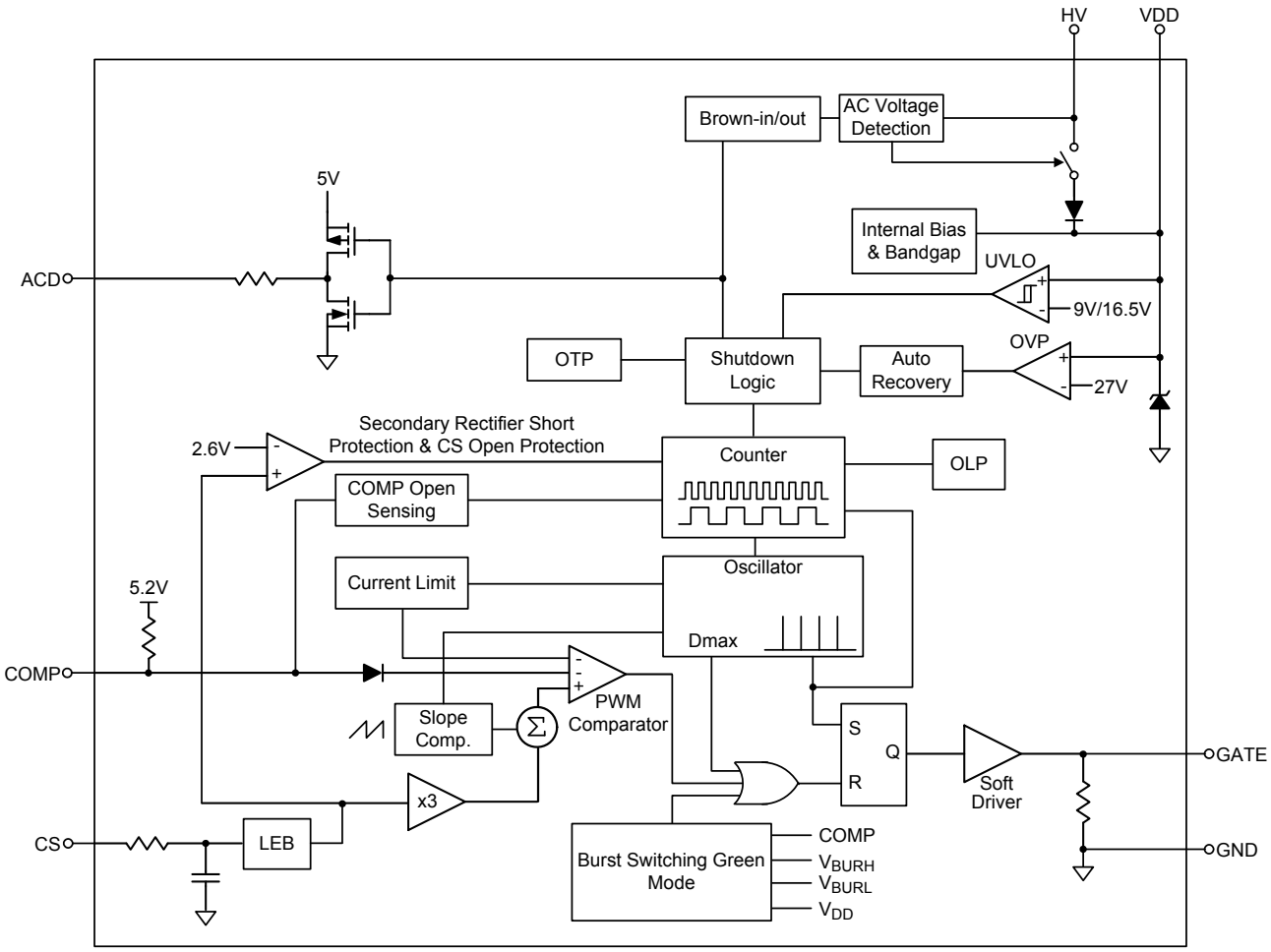

Figure 2. RT7781C Block Diagram

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Operation

HV pin Detection

The RT7781 provides a 700V high voltage pin to detect the AC input voltage and supports startup.

Brown-In and Brown-Out

The brown-in and brown-out functions are designed in this controller. Therefore, the components and power loss of external brown-in and brown-out circuits can be eliminated.

When the HV voltage rises above the brown-in voltage threshold (V_{TH_BI} = 113V typ.) for more than the brown-in deglitch time, the IC enters brown-in condition and starts PWM switching. When the HV voltage keeps under the brown-out voltage threshold (V_{TH_BO} = 96V typ.) for more than the brown-out debounce time (t_{D_BO}), the IC enters brown-out condition and stops PWM switching.

Burst Switching Green Mode

The burst mode is designed to reduce switching loss at light load condition. When the output load gets light, the COMP voltage drops and reaches V_{BURL}, the controller will cease switching. After the output voltage drops and the COMP voltage goes up to V_{BURH}, the controller will resume switching.

VDD Holdup Mode

The RT7781 provides a unique operation mode at almost no load condition named VDD holdup mode. Under the VDD holdup mode, the RT7781 forces PWM switching to maintain V_{DD} voltage between V_{DD_ET} and V_{DD_ED}. The benefit of the VDD holdup mode is to avoid the V_{DD} drops to V_{TH_OFF} due to the long burst mode period at no load or load transient moment. Therefore, this function makes bias winging design and transient design easier and compacter.

Disable Mode (T Version Only)

The RT7781T, designed to cooperate with the specific secondary-side voltage regulator RT7205, provides an outstanding solution with ultra low no-load input power (<30mW). The RT7781T features the disable mode to minimize the power consumption at very light-load or no-load conditions.

Oscillator

The oscillator runs at 65kHz and features frequency jittering function. Its jittering depth is 6% with about 4ms envelope frequency at 65kHz. It also generates slope compensation saw-tooth, 75% maximum duty cycle pulse and over-load protection slope.

Leading Edge Blanking (LEB)

Due to the device parasitic capacitors, an initial current spike appears on the current sense resistor at the beginning of the power MOSFET on-state. The spike of the CS voltage may incorrectly trigger the peak current comparator to turn off the power MOSFET, resulting in running failure of the Flyback converter. Thus, the LEB time used to mask the initial voltage spike on the CS pin, is a necessary design for a successful PWM operation.

Gate Driver

A totem pole gate driver is designed to meet both of low EMI and high efficiency application requirements. The driver integrates a voltage clamping circuit to limit the max. GATE output voltage at high VDD supply voltage condition(V_{DD} > 15V). An internal pull low circuit is activated to prevent the external MOSFET from accidental turning-on when the V_{DD} is pretty low during a start-up process.

Cycle-by-Cycle Current Limit & Constant Power

This is a basic but very useful function and it can be implemented easily in current mode controller. The entry points of current limit are different for low line and high line AC inputs because of the effect from different peak currents with the same propagation delay time. The RT7781 provides a unique calibration mechanism to reduce the variation and achieves constant output power between 90Vac and 265Vac.

COMP Pin Open Protection

If the COMP voltage reaches the open voltage V_{COMP_OP}, the controller will shut down after about t_{OLP} and enter auto recovery mode.

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Accurate Over-Load Protection Over AC Input Voltage Range

In normal operation, the CS peak voltage is controlled by the COMP voltage. In output over-load conditions, the CS peak voltage must be limited (regardless of the COMP voltage) to protect the load device and converter. This operation is called cycle-by-cycle current limit. When the duration of the current-limit operation reaches the Over-Load Protection (OLP) debounce time, the OLP shuts down the converter.

In over load conditions, long time operation of the cycle-by-cycle current limit will lead to system thermal stress problem. To further protect the system, the RT7781 is designed with a proprietary function to prolong the turn-off period during hiccup operation. Thus, the average power loss and the temperature of each component in the converter will be reduced to an acceptable level during long-time output over-load conditions.

In general, the OLP trip level is a function of the AC input voltage. For improving the accuracy of the OLP level over the full range of AC input voltage, the RT7781 is equipped with an OLP level compensation function. This function is that the maximum CS voltage threshold in the cycle-by-cycle current limit operation is modulated by the GATE on-time. It means that smaller GATE on-time gets smaller maximum CS voltage threshold. Therefore, the total variation of the OLP trip level over the full range of AC input voltage is minimized.

Over Voltage Protection

Output voltage can be roughly sensed by VDD pin. If the sensed voltage reaches V_{OVP} threshold, the controller will shut down after the OVP deglitch time.

CS Pin Open Protection

When CS pin is opened, the controller will shut down after a couple of cycles and enter auto recovery mode.

Secondary Rectifier Short Protection (SRSP)

The RT7781 is equipped with the SRSP against the secondary rectifier short-circuit condition in a flyback converter. As the output rectifier is damaged as short-circuit and the power MOSFET is turned on, inrush currents which flow through the power MOSFET, primary and secondary windings are very huge and may cause magnetic saturation of the transformer. Due the huge current stress, the power components can not sustain the stress until the end of the OLP debounce time. The SRSP function is a necessary design for protecting the power components. When CS voltage reaches the SRSP voltage threshold, the RT7781 shuts down the converter after the debounce time of few switching cycles.

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Absolute Maximum Ratings (Note 1)

- HV to GND ---------- –0.3V to 700V (DC)
- Supply Input Voltage, VDD to GND ---------- –0.3V to 30V
- GATE to GND ---------- –0.3V to 16.5V
- PRO, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-7 ---------- 0.36W
- Package Thermal Resistance (Note 2)
  SOP-7, θ_{JA} ---------- 276.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model)
  (Except HV pin) ---------- 5kV
  (HV to GND) ---------- 1kV
  MM (Machine Model) ---------- 300V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, HV ---------- 0V to 500V (DC)
- Supply Input Voltage, VDD ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HV Section						
HV Start-Up Current	I_{JEFT_ST}	$V_{DD} < V_{TH_ON}$, V_{HV} = 500V	1	3.5	--	mA
Off State Leakage Current	I_{HV_LK}	$V_{DD} > V_{TH_ON}$, V_{HV} = 500V	--	--	25	μA
Brown-In Threshold	V_{TH_BI}	DC Input Voltage	106	113	120	V
Brown-Out Threshold	V_{TH_BO}	DC Input Voltage	86	96	106	V
Brown-In/Out Hysteresis	ΔV_{BIO}	$\Delta V_{BIO} = V_{TH_BI} - V_{TH_BO}$	10	17	27	V
De-Bounce Time of Brown-Out	t_{D_BO}	f_{OSC} = 65kHz	--	60	--	ms
		f_{OSC} = 22kHz	--	180	--	
VDD Section						
Under Voltage Lockout (UVLO) Voltage Threshold (On)	V_{TH_ON}		15.5	16.5	17.5	V
Under Voltage Lockout (UVLO) Voltage Threshold (Off)	V_{TH_OFF}	RT7781G/L/A/C	8.5	9	9.5	V
		RT7781T	6.5	7	7.5	

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
HV Restart Voltage Threshold	V_{HV_ON}			--	5.5	--	V
VDD Holdup Mode Ending Point	V_{DD_ED}	V_{COMP} < 1.35V		--	V_{DD_ET} + 0.5	--	V
VDD Holdup Mode Entry Point	V_{DD_ET}	V_{COMP} < 1.35V	RT7781G/L/A/C	9.5	10	10.5	V
			RT7781T	7.5	8	8.5	
VDD Over-Voltage Protection Level	V_{OVP}			26	27	28	V
VDD Zener Clamp Voltage	V_Z			29	--	--	V
Operating Current	I_{DD_OP}	f_{OSC} = 65kHz COMP = GATE = Open		--	0.7	1.4	mA
VDD Clamping Voltage after a Latch-off Protection	V_{LH}			--	6.5	--	V
VDD Reset Voltage Threshold of the Latch-off Protection	V_{LH_RST}			--	5.5	--	V
Oscillator Section							
PWM Frequency	f_{PWM}	Average Frequency		60	65	70	kHz
Minimum Burst Switching Frequency	f_{BS_MIN}	Average Frequency		18	22	--	kHz
Maximum Duty Cycle	D_{MAX}			70	75	80	%
Frequency Jittering Range	Δf			--	±6	--	%
Frequency Jittering Period	t_{JIT}	f_{OSC} = 65kHz		--	4	--	ms
Max. Frequency Variation over Operating VDD Range	f_{DV}	(max. frequency variation over V_{DD} = 12V to 25V) / f_{PWM}		--	--	2	%
Max. Frequency Variation over Ambient Temperature Range	f_{DT}	(max. frequency variation over T_A = −30°C to 105°C) (Note 5)		--	--	5	%
COMP Input Section							
COMP Open Voltage	V_{COMP_OP}	COMP = Open		5	5.2	5.4	V
COMP Open Protection Delay Time	t_{OLP}	f_{OSC} = 65kHz		--	56	--	ms
Short Circuit COMP Current	I_{ZERO}	V_{COMP} = 0V		--	240	400	μA
Burst Switching Entry Voltage	V_{BS_ET}			--	2.3	--	V
Burst Switching Ending Voltage	V_{BS_ED}			--	2.15	--	
Current-Sense Section							
Maximum Current Limit Threshold	V_{CS_MAX}			1.05	1.1	1.15	V
Leading Edge Blanking Time	t_{LEB}	(Note 6)		150	250	350	ns
Internal Propagation Delay Time	t_{PD}	(Note 6)		--	100	--	ns
Minimum On-Time	t_{ON_MIN}			250	350	450	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE Section						
Gate Output Clamping Voltage	V_{CLAMP}	V_{DD} = 25V	--	13.5	--	V
Rising Time	t_R	C_L = 1nF	--	50	--	ns
Falling Time	t_F	C_L = 1nF	--	40	--	ns
PRO Section (RT7781G/L/A/T)						
Internal Bias Current	I_{BIAS}		90	100	110	μA
Pull High Sinking Current	I_{SIN}	V_{PRO} = V_{TH_H}	--	--	500	μA
Pull High Threshold	V_{TH_H}		1.75	1.8	1.85	V
Pull Low OTP Voltage Threshold	V_{TH_OTP}		0.47	0.5	0.53	V
Pull Low Threshold	V_{TH_L}		0.25	0.3	0.35	V
PRO Open Voltage	V_{PRO_OP}	PRO = Open	--	1.3	--	V
PRO OTP De-bounce Time	t_{D_OTP}	f_{OSC} = 65kHz	--	56	--	ms
ACD Section (RT7781C)						
Maximum ACD Sourcing Current	I_{ACD}		1	--	4	mA
De-bounce Time of AC Voltage Detection	t_{D_ACD}	f_{OSC} = 65kHz	--	15	--	ms
		f_{OSC} = 22kHz	--	45	--	
OTP Section						
Over-Temperature Protection	T_{OTP}	On Chip OTP (Note 5)	--	140	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in natural convection (still air) at T_A = 25°C with the component mounted on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Note 6. Leading edge blanking time and internal propagation delay time are guaranteed by design.

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Typical Application Circuit

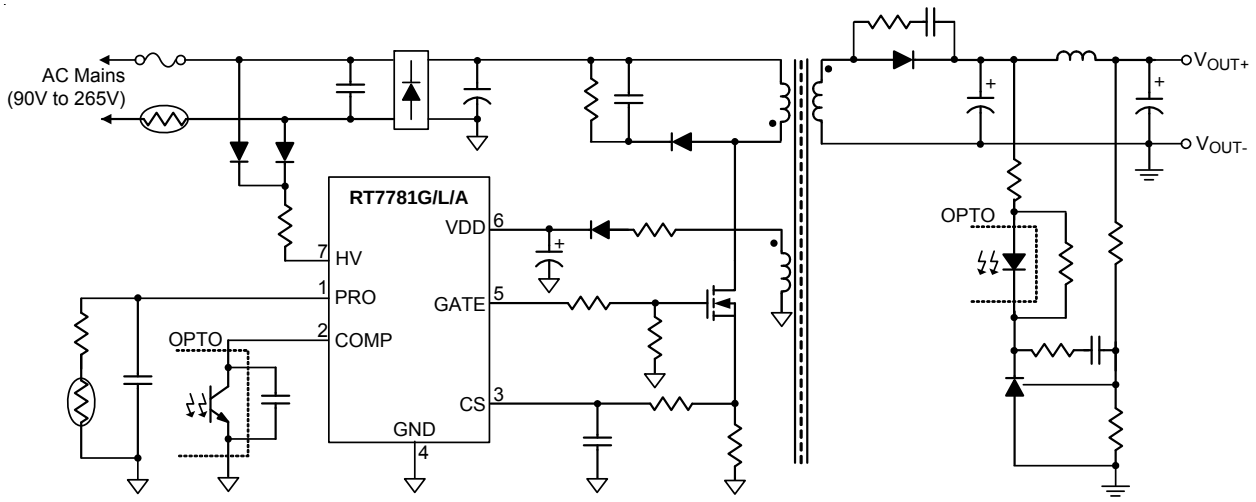

Figure 3. RT7781G/L/A Application Circuit

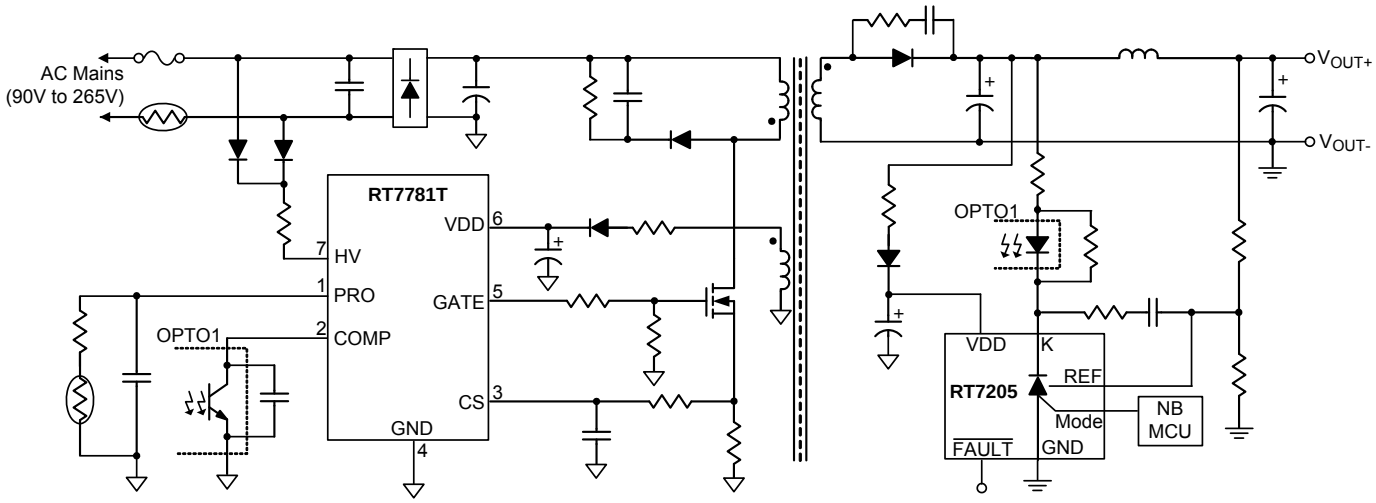

Figure 4. RT7781T Application Circuit

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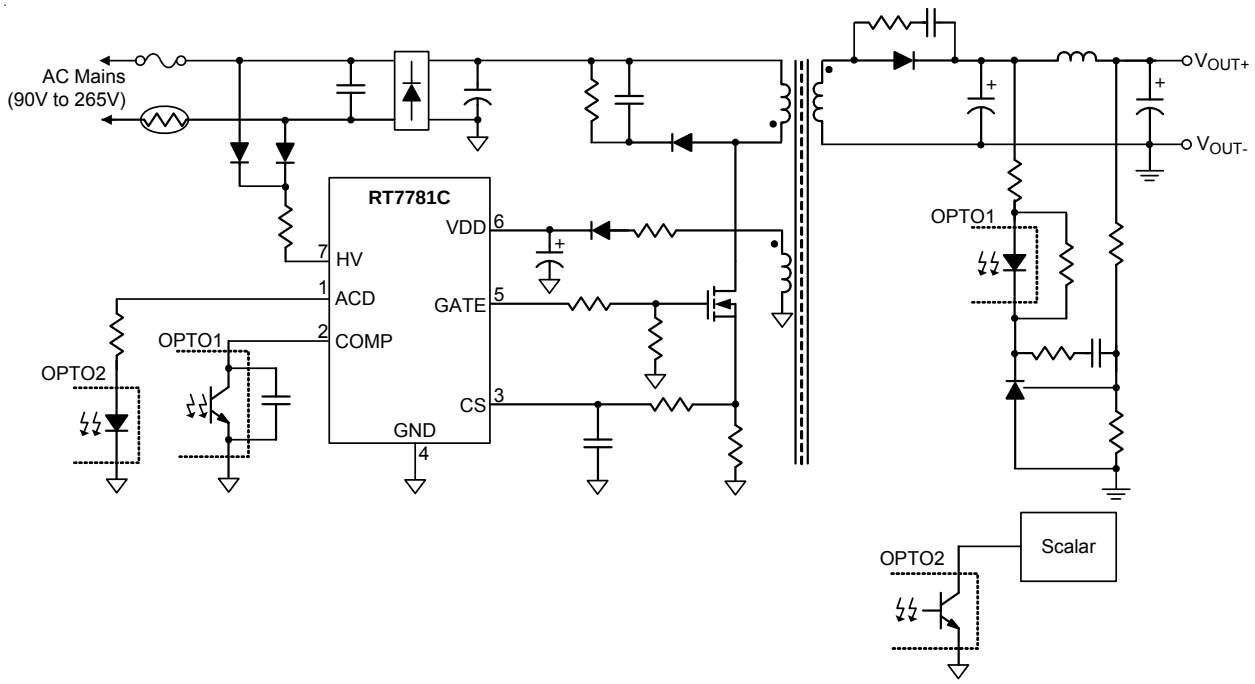

Figure 5. RT7781C Application Circuit

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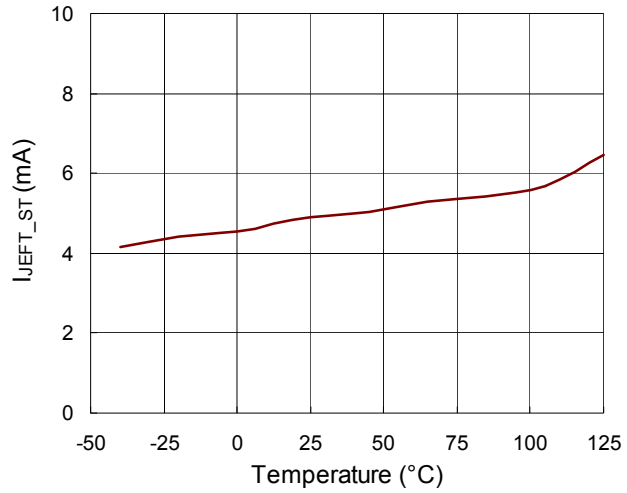
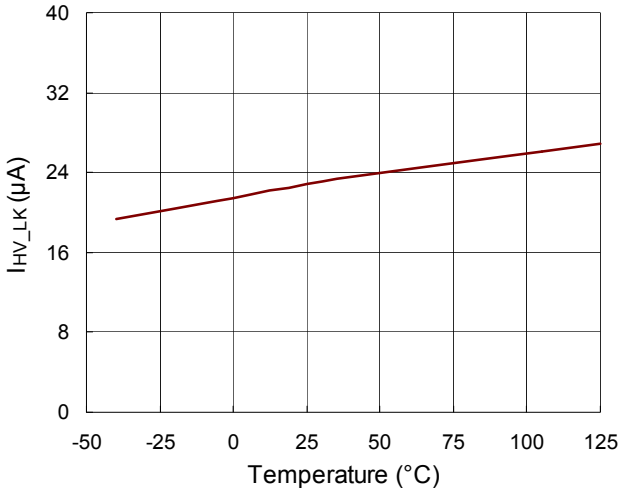
Typical Operating Characteristics

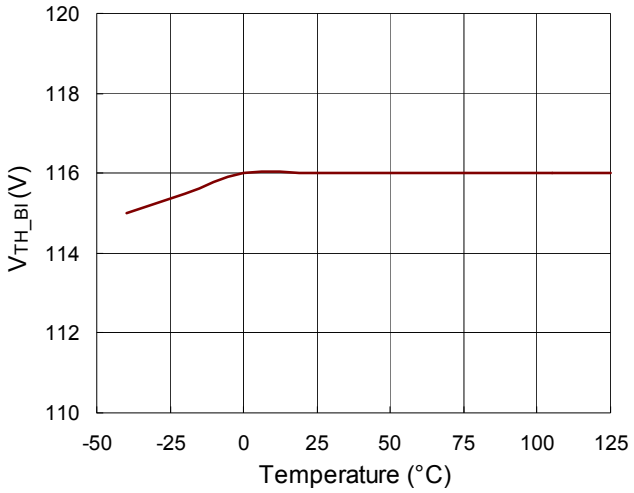
I_{JEFT_ST} vs. Temperature



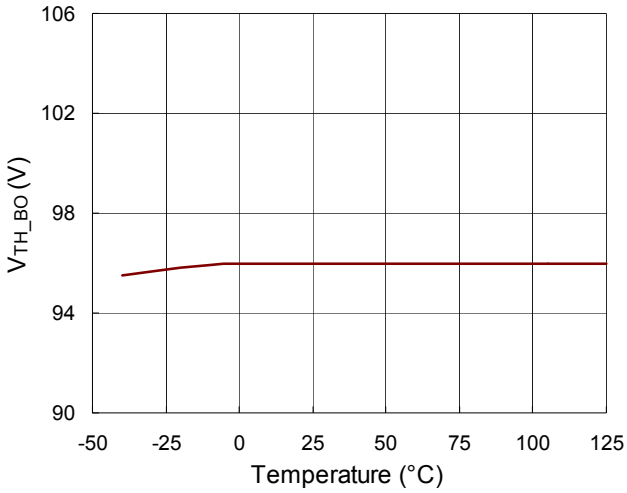
I_{HV_LK} vs. Temperature



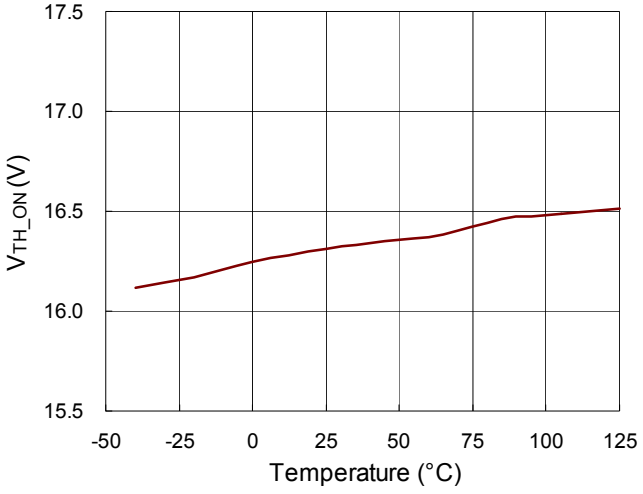
V_{TH_BI} vs. Temperature



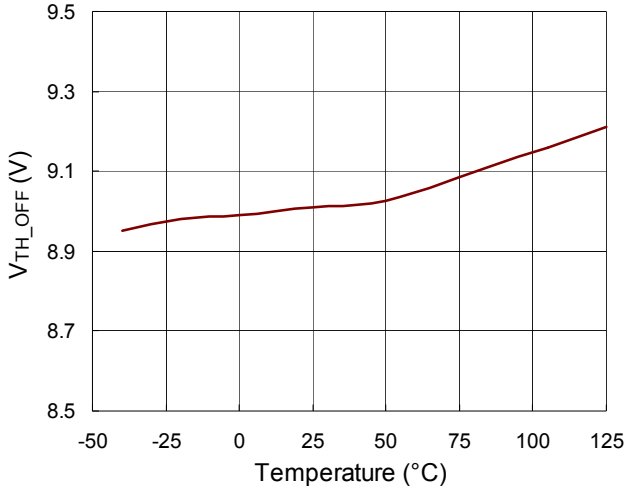
V_{TH_BO} vs. Temperature



V_{TH_ON} vs. Temperature



V_{TH_OFF} vs. Temperature



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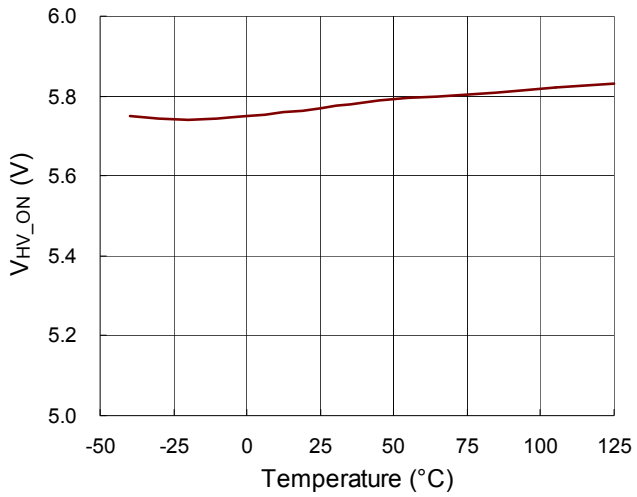
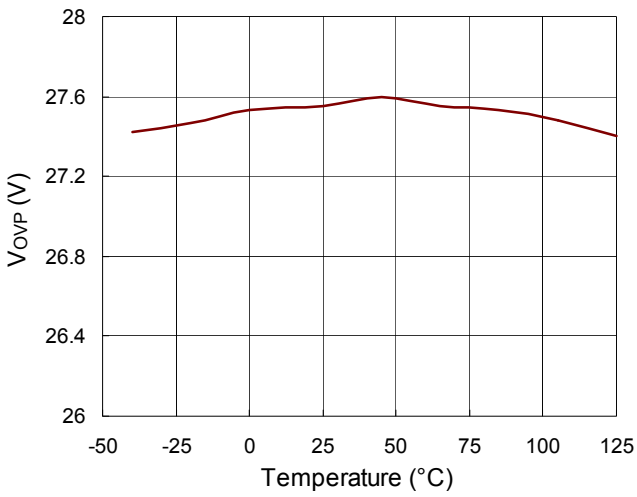
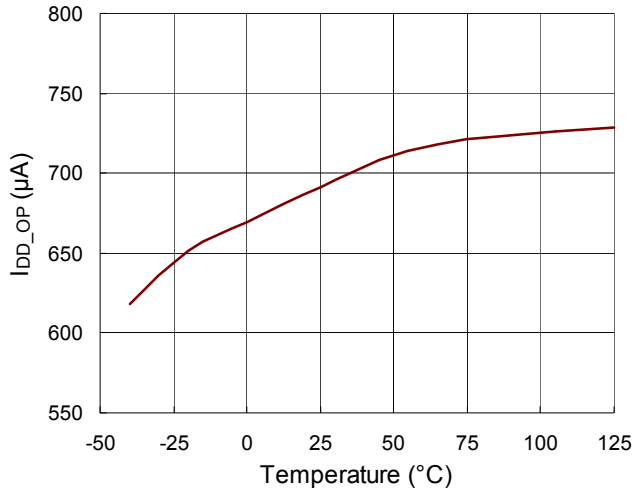
V_{HV_ON} vs. Temperature



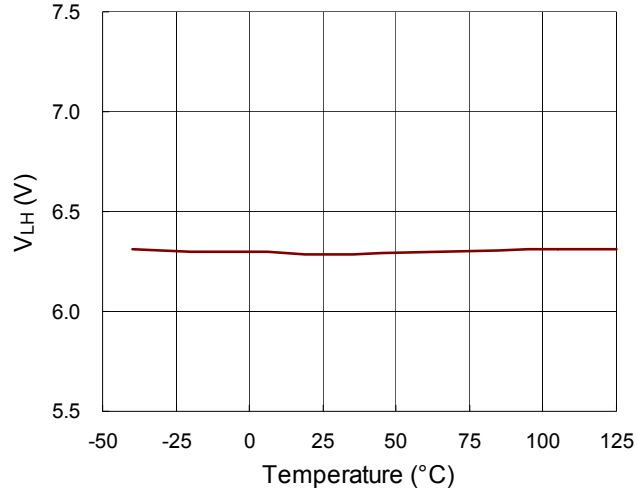
V_{OVP} vs. Temperature



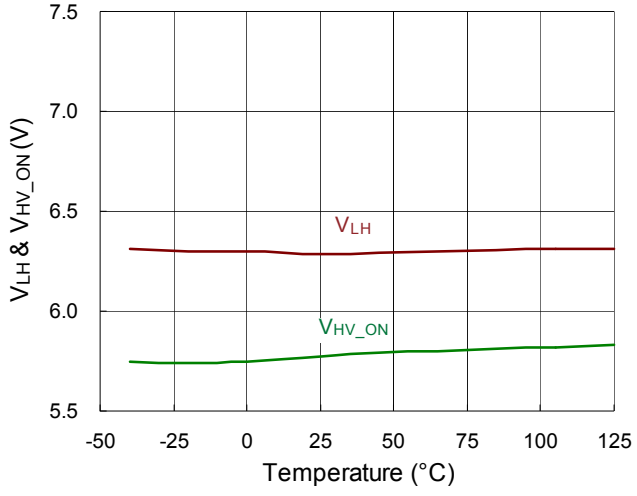
I_{DD_OP} vs. Temperature



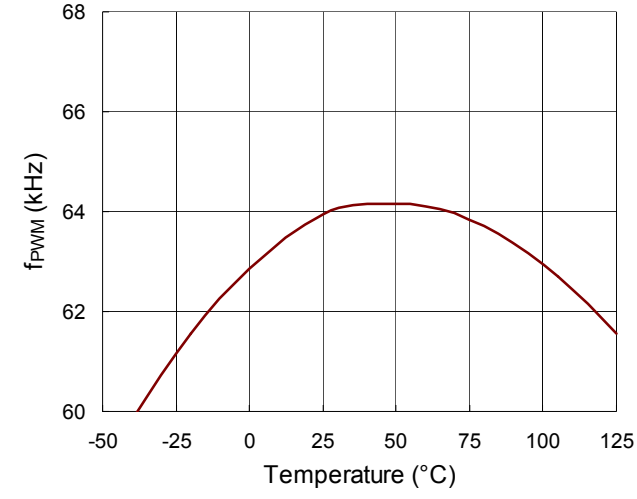
V_{LH} vs. Temperature



V_{LH} & V_{HV_ON} vs. Temperature



f_{PWM} vs. Temperature



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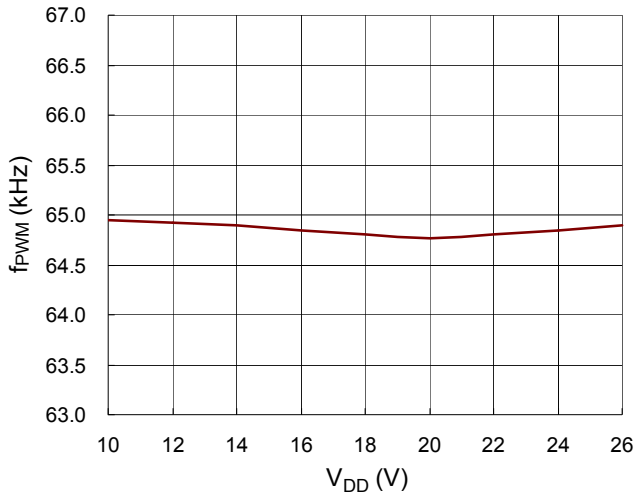
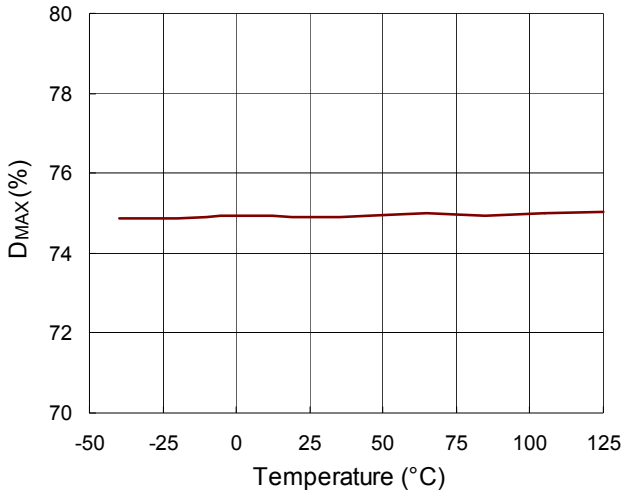
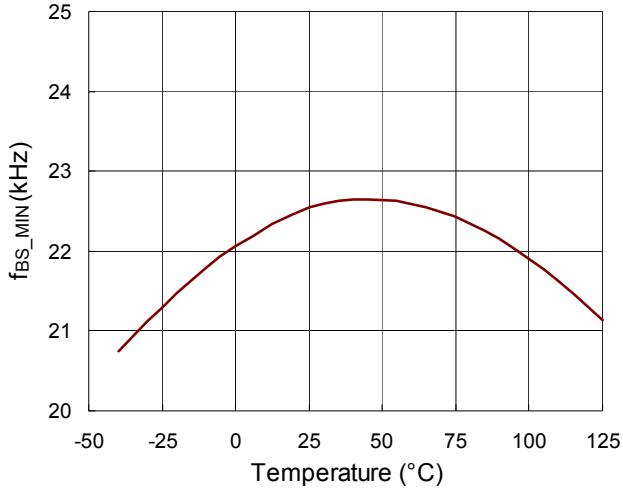
f_{PWM} vs. V_{DD}



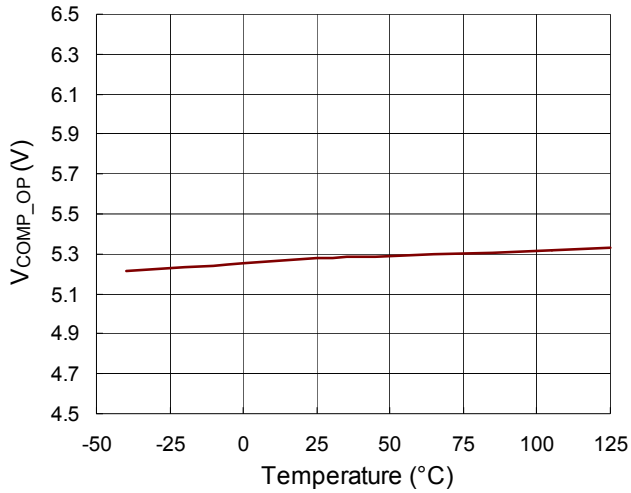
D_{MAX} vs. Temperature



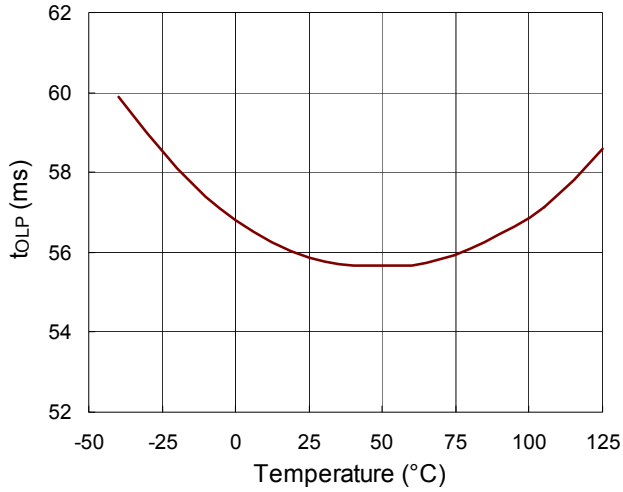
f_{BS_MIN} vs. Temperature



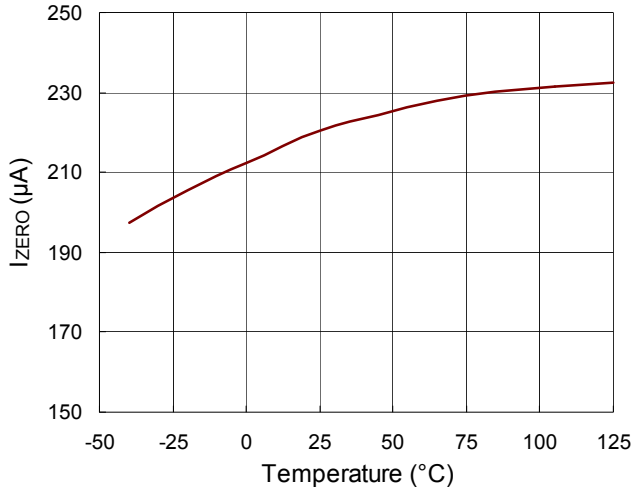
V_{COMP_OP} vs. Temperature



t_{OLP} vs. Temperature



I_{ZERO} vs. Temperature



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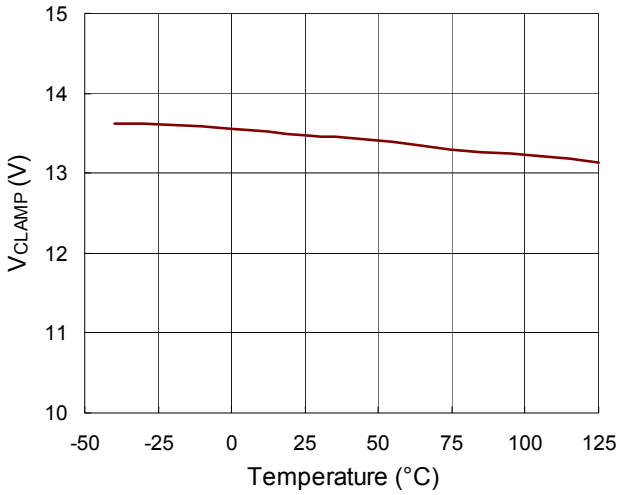
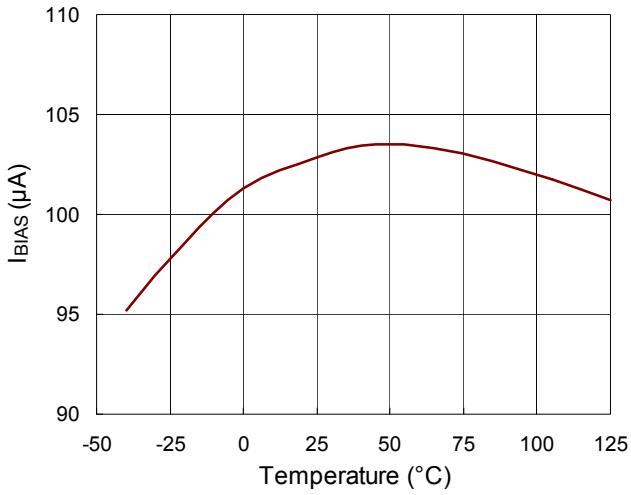
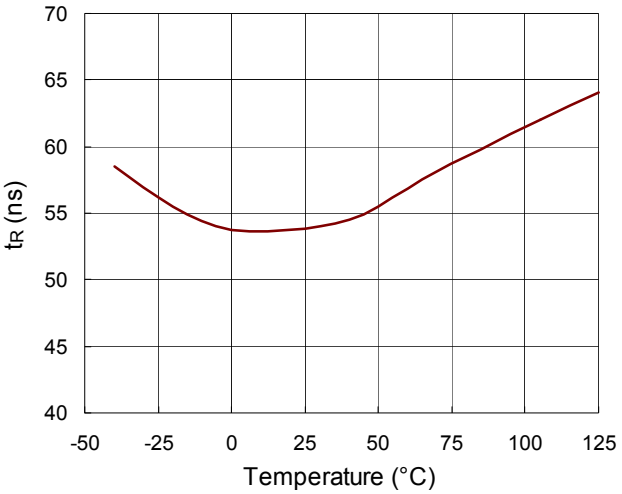
V_{CLAMP} vs. Temperature



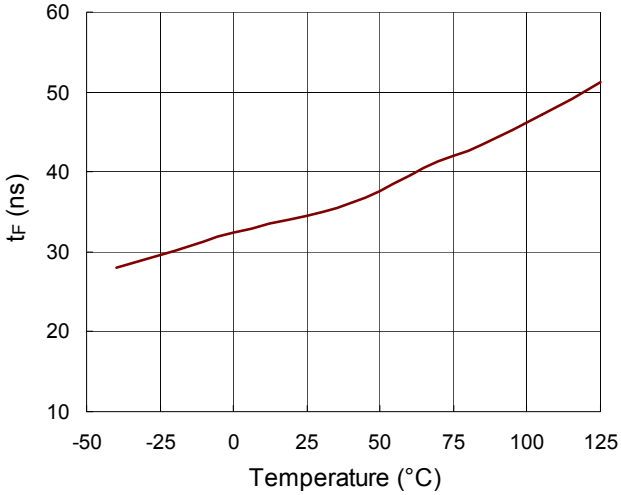
I_{BIAS} vs. Temperature



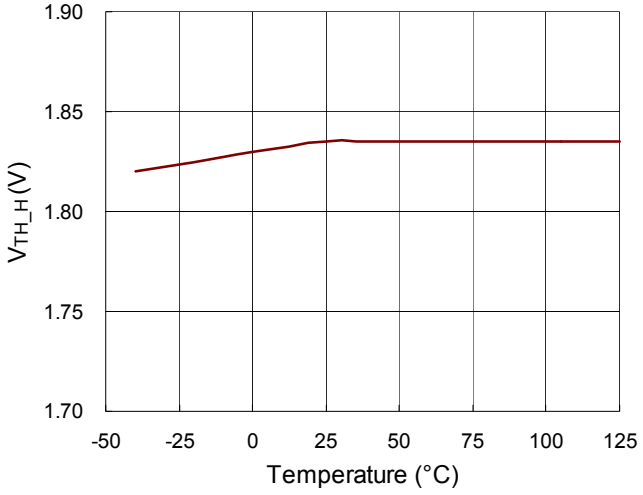
t_R vs. Temperature



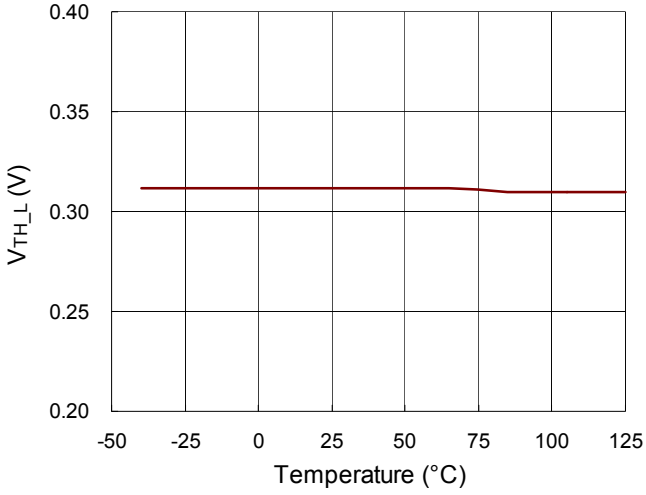
t_F vs. Temperature



V_{TH_H} vs. Temperature



V_{TH_L} vs. Temperature



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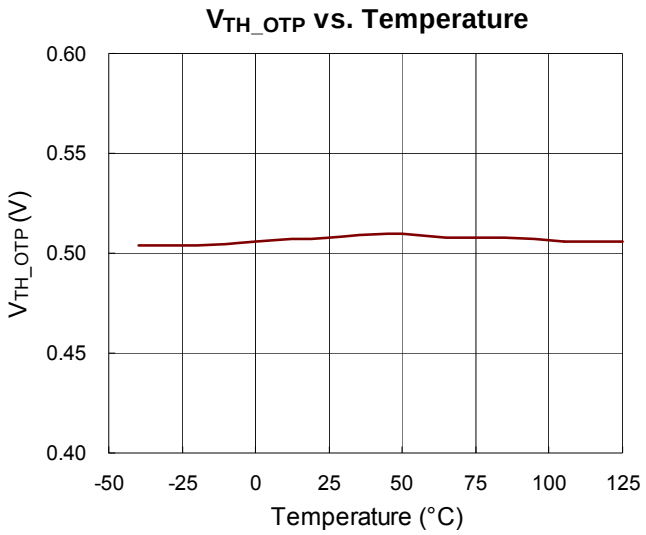

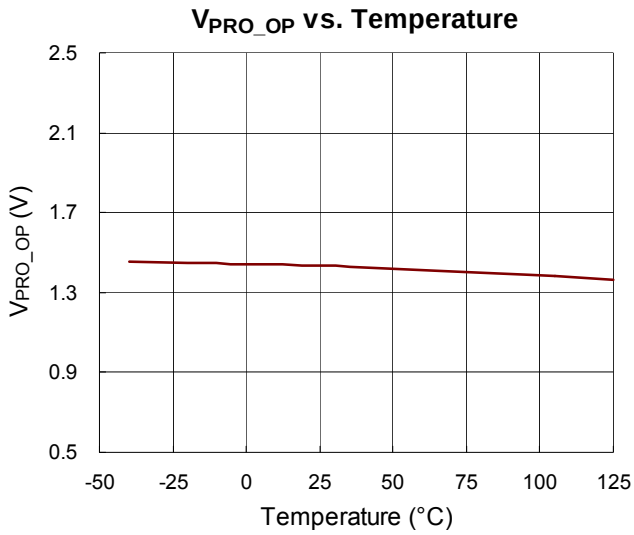

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Application Information

Start-up

The RT7781 features a HV pin to provide fast start-up. 700V start-up device is integrated in the controller to further minimize power consumption and enhance performance. The start-up device will be turned on during start-up and be turned off during normal operation. It shortens start-up time and no power loss in this path after start-up.

As shown in Figure 6, the resistor R_{HV} connected in series with HV pin is recommended in the range from 2kΩ to 6.6kΩ (tolerance < ±5%). If R_{HV} is much larger than 6.6kΩ (tolerance < ±5%), the brown-in and brown-out threshold will be inaccurate.

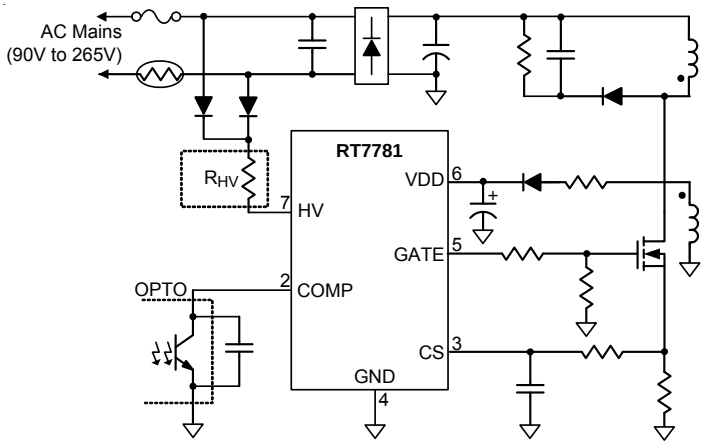

Figure 6. Start-up Circuit

Brown-In and Brown-Out

The RT7781 features internal precise brown-in and brown-out detections. An AC voltage detection circuit is built in the controller so that the brown-in and brown-out can be implemented without extra components. The brown-out offers precise brown-out detection without AC ripple effect at heavy or light load.

PRO Pin Application (RT7781G/L/A/T)

The RT7781 features a PRO pin for external arbitrary OVP or OTP applications as shown in Figure 7 to Figure 11.

If the PRO pin voltage is higher than OTP threshold V_{TH_OTP} and is lower than pull high threshold V_{TH_H}, the controller is enabled for normal operation. If the PRO pin voltage falls below V_{TH_OTP} and is greater than pull low threshold V_{TH_L} after t_{D_OTP} de-bounce time, the controller will shut down. Once the PRO pin voltage is higher than V_{TH_H} or lower than V_{TH_L}, the controller will cease switching and shut down after the 50µs deglitch time.

In order to pull up the PRO voltage to be above the V_{TH_H}, the external supply current flowing into the PRO pin must be greater than 500µA and be limited below 5mA. When the IC is latched at off-state by the fault latch (entering latch-mode), V_{DD} will be clamped at the latch-mode voltage threshold V_{LH}, and the fault latch will be reset when the V_{DD} falls and reaches the VDD reset voltage threshold V_{LH_RST}.

When the PRO pin is open, it is set at 1.3V internally. Just leave the PRO pin open if it is not used. If designers want to use a bypass capacitor on the PRO pin, the capacitor should less than 1nF. The internal bias current of PRO pin is 100µA (typ.).

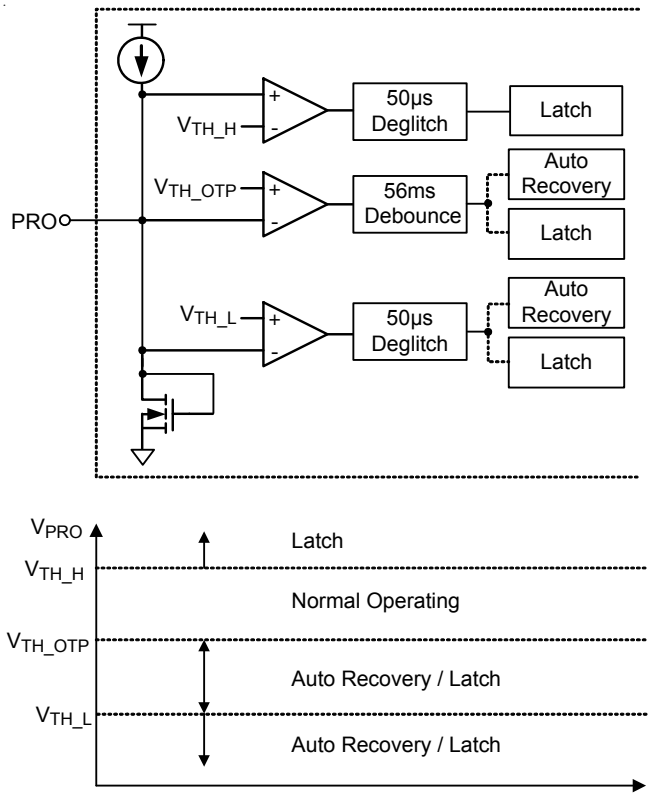

Figure 7. PRO Functional Diagram

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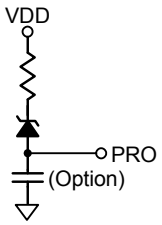

V_{DD} OVP : $V_{DD} > V_R + V_Z + 1.8V$

Figure 8. OVP for VDD Only

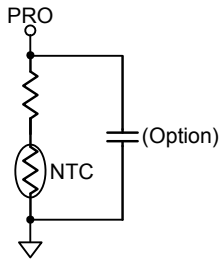

Figure 9. External OTP

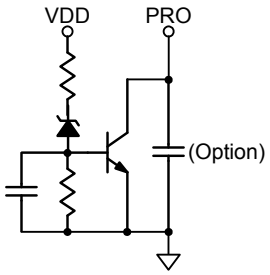

Figure 10. OVP for VDD

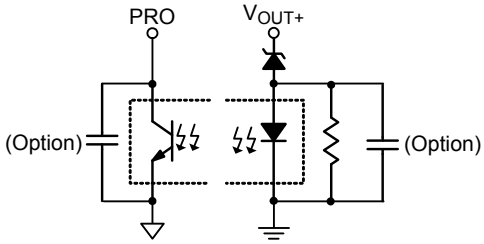

Figure 11. OVP for V_{OUT}

ACD Pin Application (C Version Only)

In order to detect the AC voltage removal or brown-out and communicate with the secondary side controller, traditional external circuits are used in the applications for TV or monitor. The RT7781C features the AC voltage detection (ACD) function to eliminate external components of AC voltage detection circuit and make the circuit design easier.

- t_{D_ACD} < AC Voltage Dip Time < t_{D_BO}

  In this situation, the ACD pin will source a current I_{ACD} and provide a pull low signal for the secondary side controller through an opto-coupler after the delay time t_{D_ACD}. Until the AC voltage recovers, the ACD signal will be reset, as shown in Figure 12. In order to make sure the secondary side controller can successfully receive the ACD signal, the resistor R_{ACD} connected in series with the ACD pin is considered carefully, as shown in Figure 13.

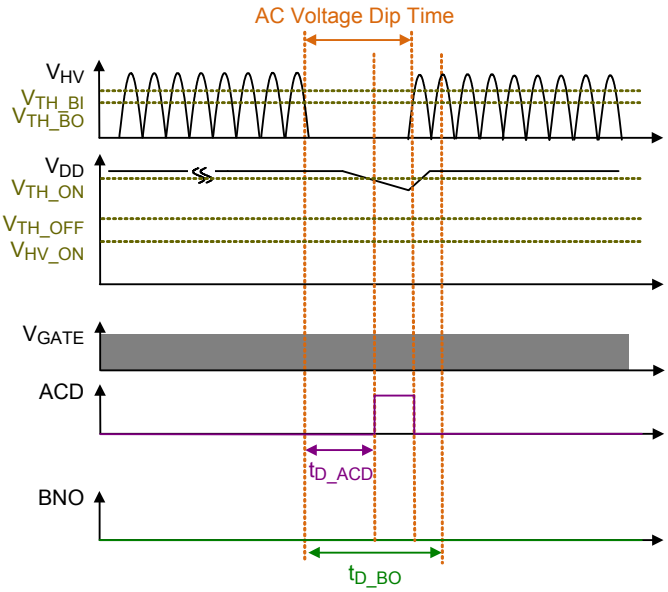

Figure 12. t_{D_ACD} < AC Voltage Dip Time < t_{D_BO}

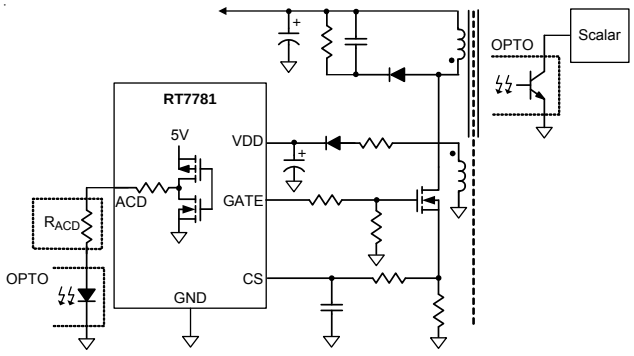

Figure 13. ACD Application Circuit

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- AC Voltage Dip Time > t_{D_BO} or AC Off

  In this situation, the ACD signal will pull high after the delay time t_{D_ACD}. Until the AC voltage dip time is larger than the brown-out delay time t_{D_BO}, the brown-out signal BNO pulls high and the V_{DD} voltage fast decreases. When the V_{DD} reaches the voltage threshold V_{HV_ON}, the ACD and BNO signals will be reset, as shown in Figure 14.

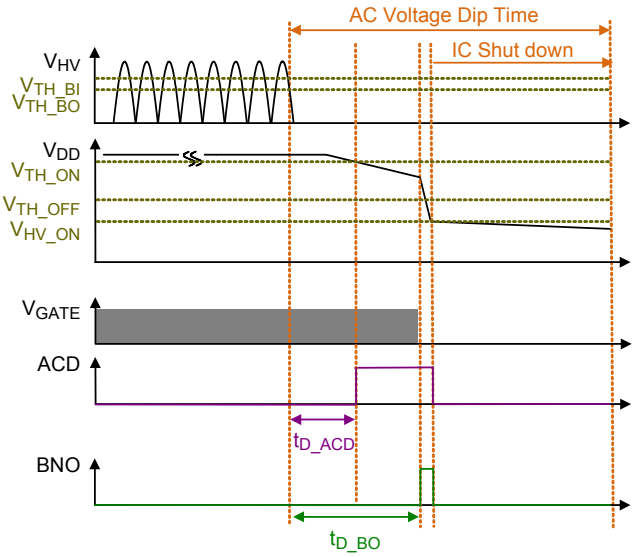

Figure 14. AC Voltage Dip Time > t_{D_BO} or AC Voltage is Turned Off

Disable Mode (T Version Only)

The RT7781T, designed to cooperate with the specific secondary-side voltage regulator RT7205, provides an outstanding solution with ultra low no-load input power (<30mW). The RT7781T features the disable mode to minimize the power consumption at very light-load or no-load conditions. When the COMP voltage, which is pulled low by the RT7205 through an opto-coupler, is under the burst mode voltage threshold (V_{BURL}) for more than the disable mode debounce time (t_{DIS} = 210ms typ.) the RT7781T will enter the disable mode, as shown in Figure 15. In the disable mode, the VDD voltage is kept around the clamping voltage threshold (V_{LH}) by turning on or off the high-voltage device at the HV pin and most of the operating VDD current is turned off to minimize the power consumption. Only few necessary functions which monitors the COMP voltage for exiting the disable mode are enabled. The RT7781 will be waked up once the COMP voltage is pulled low by RT7205 again.

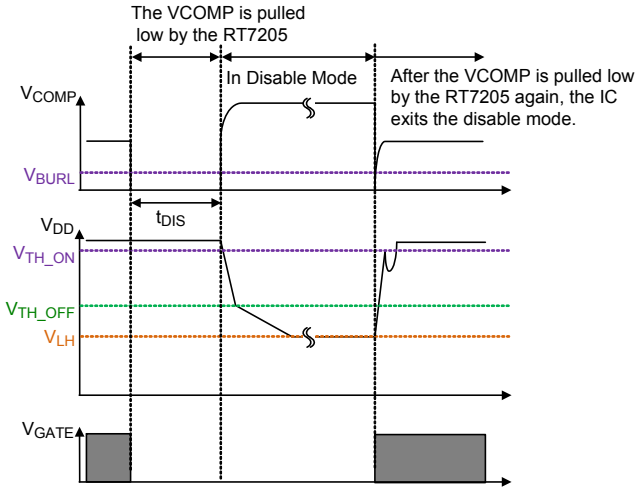

Figure 15. Timing Chart of Disable Mode Operation

VDD Holdup Mode

The VDD holdup mode is only designed to prevent V_{DD} from decreasing to the turn-off threshold voltage under light load or load transient moment. Relative to the burst-mode operation, the VDD holdup mode brings higher switching loss. So, it is highly recommended that the system should avoid operating at this mode during light load or no load condition, normally.

Resistors on GATE pin

As shown in Figure 16, R_G is applied to alleviating the ringing voltage of the gate drive loop in typical application circuits. The resistance of the R_G must be considered carefully to system EMI and efficiency.

The RT7781 builds in an internal discharge-resistor R_{ID} in parallel with GATE pin to prevent the MOSFET from any uncertain conditions. If the connection between GATE pin and the MOSFET is disconnected, the MOSFET might be falsely triggered by the energy through the gate-to-drain parasitical capacitor C_{GD} of the MOSFET and the system might be damaged. Therefore, it's highly recommended to add the external discharge-resistor R_{ED} connected between the Gate of MOSFET and GND terminals. The energy through the C_{GD} is discharged by the external discharge-resistor to avoid MOSFET falsely triggering.

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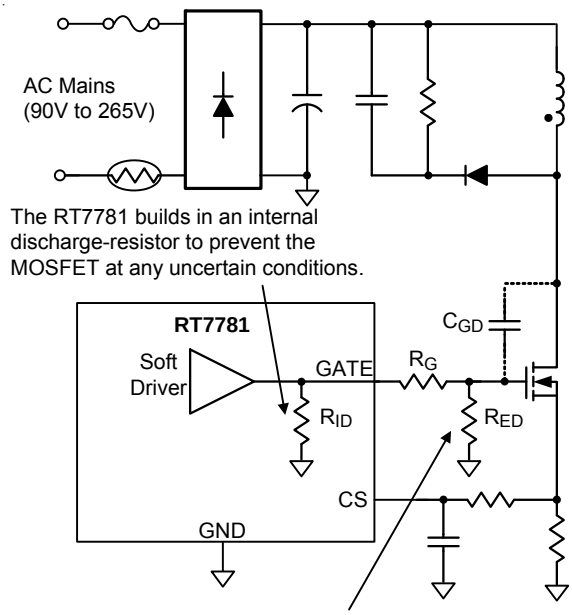

Figure 16. Resistors on Gate Pin

Feedback Resistor

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with the photo-coupler is reduced, as shown in Figure 17. Due to small feedback resistor current, the selection of shunt regulator (Ex.TL-431) and its minimum regulation current must be considered carefully to make sure it's able to regulate under low cathode current.

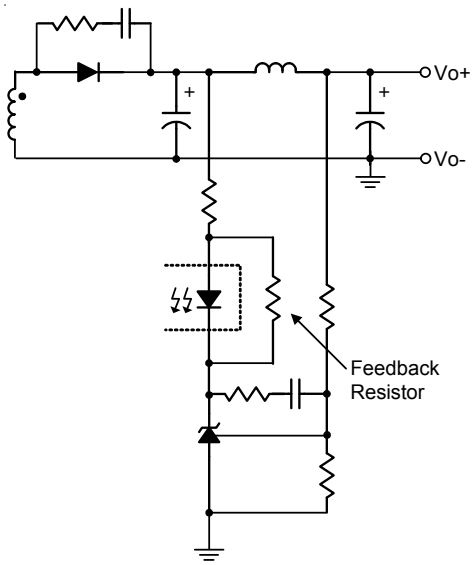

Figure 17. Feedback Resistor

Accurate Over-Load Protection

Besides the OLP trip level compensation, the tolerance of the RT7781 OLP trip level is further improved through well foundry process control, and test/trim mode in final test. Therefore, the current limit tolerance is tight enough to make design and mass production easier, and it provides accurate over-load protection.

Over-Temperature Protection (OTP)

The RT7781 provides an internal OTP function to protect the controller from suffering thermal stress and permanent damage. It's not suggested to use the function as a precise OTP. Once the junction temperature is higher than the OTP threshold, the controller will shut down switching operation until the temperature cools down. Meanwhile, if V_{DD} reaches its turn-off threshold voltage, the controller will hiccup till the over-temperature condition is removed.

Negative Voltage Spike on Each Pin

The negative voltage (< –0.3V) on one of the controller pins will cause current injection of the chip substrate and lead to controller damage or circuit false trigger. For example, the negative spike voltage at CS pin may come from improper PCB layout or inductive current sense resistor. Therefore, it is highly recommended to add a R-C filter to avoid CS pin from damage, as shown in Figure 18. Proper PCB layout and component selection should be considered during circuit design.

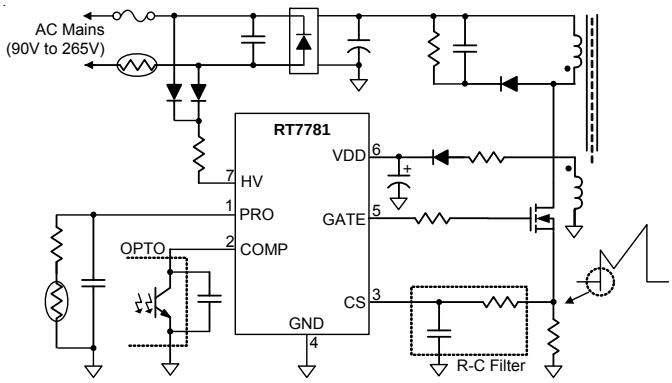

Figure 18. R-C Filter on CS Pin

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Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-7 package, the thermal resistance, θ_{JA}, is 276.5°C/W on a standard JEDEC 51-3 one-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (276.5°C/W) = 0.36W for SOP-7 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 19 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

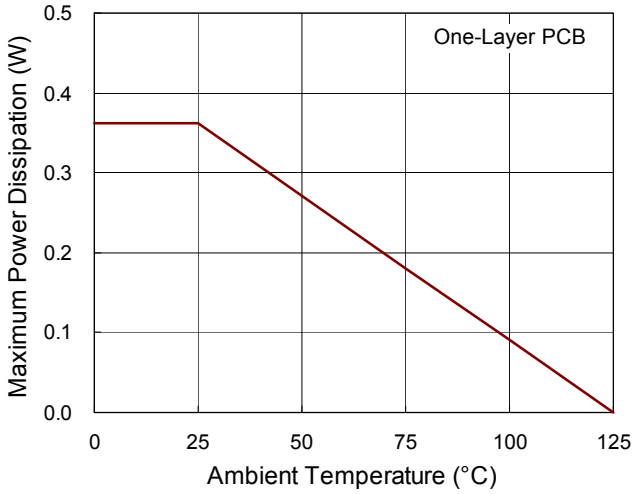

Figure 19. Derating Curve of Maximum Power Dissipation

Layout Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in a switching power supply. In order to optimize the system performance of the RT7781 switching power supply, please refer to the following PCB layout guideline before you starts a PCB layout.

The current path(1) from bulk capacitor, transformer, MOSFET, current sense resistor (R_{CS}) to the ground of bulk capacitor is a high frequency current loop. The path(2) from GATE pin, MOSFET, R_{CS} to the ground of bulk capacitor is also a high frequency current loop. They must be as short as possible to decrease noise coupling and be kept away from other low voltage traces, such as IC control circuit paths, especially.

The path(3) between MOSFET ground and IC ground should be as short as possible.

The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.

The path(5) from the AC voltage to HV pin is a high voltage loop. For preventing the switching noise coupling, it is highly recommended that the PRO pin control paths must be kept away from path(1), path(2), path(3), path(4) and path(5).

Separate the ground traces of bulk capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d) for reducing noise, output ripple and EMI issue. And, connect these ground traces together at bulk capacitor ground(a). The areas of these ground traces should be large enough.

Place the bypass capacitor as close to the controller as possible.

For reducing the reflected trace inductance and EMI, minimize the area of the loop connecting the secondary winding, output diode and output filter capacitor. In additional, apply sufficient copper area at the anode and cathode terminals of the diode for heatsinking.

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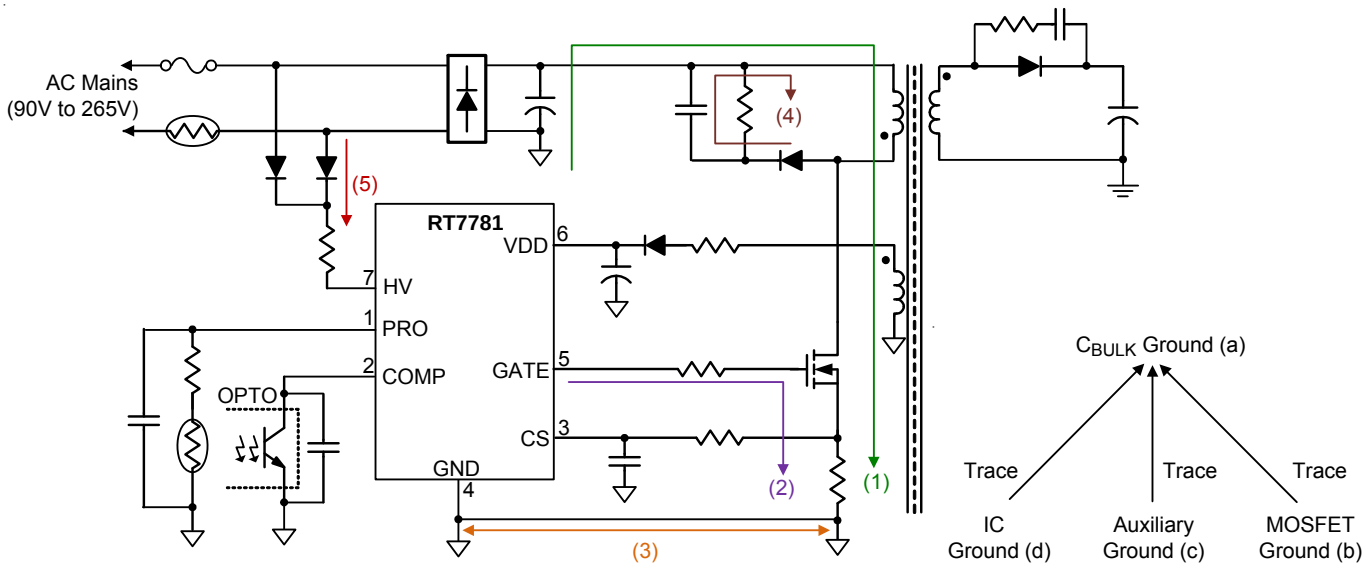

Figure 20. PCB Layout Guide

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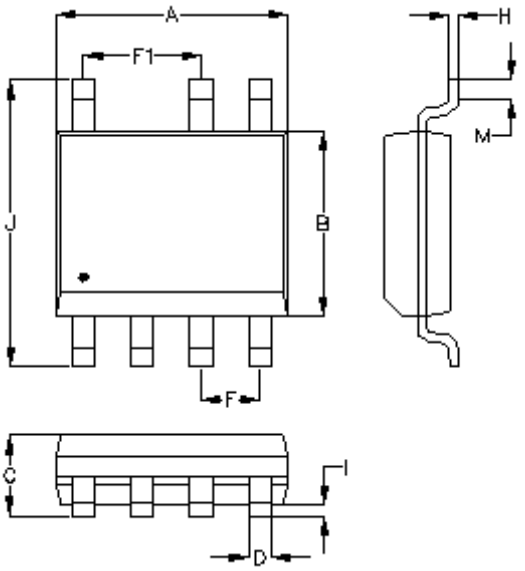
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.310	0.510	0.012	0.020
F	1.194	1.346	0.047	0.053
F1	2.464	2.616	0.097	0.103
H	0.100	0.254	0.004	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

7-Lead SOP Plastic Package

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Hsinchu, Taiwan, R.O.C.

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