RICHTEK®

RT7795ML

PWM Controller for Asymmetrical Half-Bridge Flyback Converters

1 General Description

The RT7795ML is a specialized controller designed for Asymmetrical Half-Bridge (AHB) flyback converters, commonly employed in various applications. It is capable of delivering an output power of 300W and features a versatile output voltage range from 5V to 48V, making it particularly well-suited for USB-PD EPR (Extended Power Range) applications.

To ensure peak efficiency, the RT7795ML utilizes a resonant mode of operation for the AHB, effectively minimizing power losses for both the AHB and the secondary-side synchronous rectifier. Furthermore, the RT7795ML addresses potential audio noise issues through a proprietary jitter approach that disperses the energy and frequency of the noise.

In addition to its performance features, the RT7795ML includes comprehensive protection functionality, ensuring the safety and reliability of the power supply.

The RT7795ML collaborates with the synchronous rectification controller RT7220E to offer a comprehensive power solution, maximizing efficiency.

For USB-PD or programmable power supply applications, pairing the RT7795ML with the secondary-side controller RT7209 ensures a robust and secure design, safeguarding both the power supply and any connected systems.

The RT7795ML is available in a WQFN-24L 4x6 package. The recommended junction temperature range is from –40°C to 125°C, and the ambient temperature range is from –40°C to 85°C.

2 Features

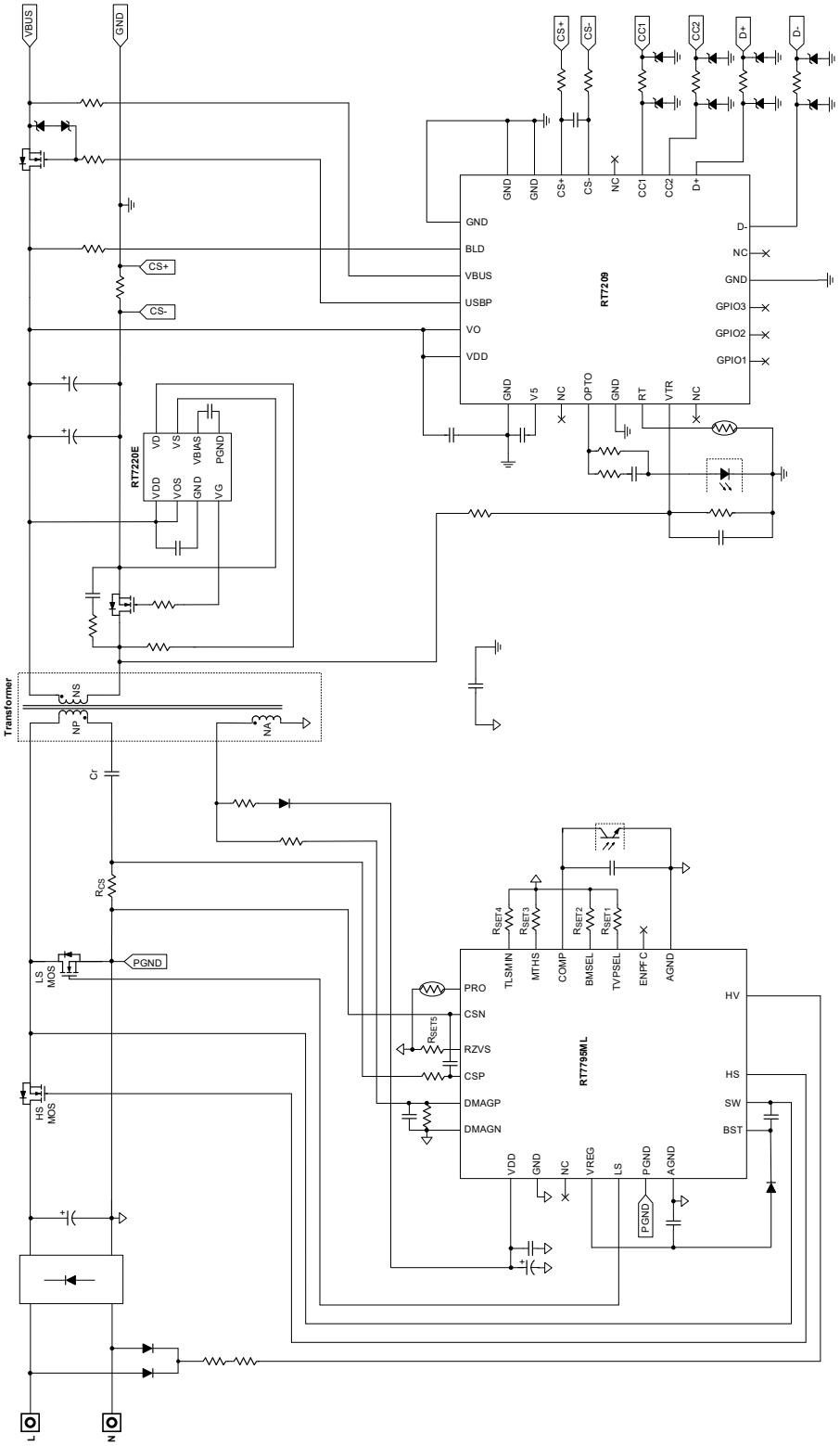
- **High Efficiency**
  - **Continue Resonant Mode (CRM)**
  - **Cycle-Skipping and Burst Mode**
  - **Zero Voltage Switching (ZVS) On-Time Modulation**
  - **ENPFC (Enable/Disable PFC) Light Load Control**
- **High Integration**
  - **625V Start-Up Device**
  - **625V High-Side (HS) Gate Driver**
  - **Built-In Voltage Regulator (VREG-LDO)**
  - **X-Capacitor Discharge Function**
- **Wide-Range Output Voltage**
  - **Wide VDD Range: 11V to 63V**
  - **Adaptive Low-Side (LS) Minimum On-Time**
- **Key Parameter Settings**
  - **MTHS (Maximum HS On-Time)**
  - **TLSMIN (Minimum LS On-Time)**
  - **RZVS (LS ZVS Pulse Initial On-Time)**
  - **TVPSEL (Valley and Peak Signal Debounce Time)**
  - **BMSEL (Burst-Mode Voltage Threshold)**
- **Comprehensive Protection Functions**
  - **Brown-In (BNI) and Brown-Out (BNO) Protection**
  - **VDD Overvoltage Protection**
  - **External Over-Temperature Protection**
  - **Overcurrent Protection (OCP)**
  - **Resonant Negative Switching Current OCP**
  - **Output Overvoltage and Undervoltage Protection (OVP/UVP)**
  - **Secondary Rectifier Short Protection (SRSP)**

3 Applications

- General Purpose Power Supply
- High Power-Density Power Adapters
- USB-PD EPR Power Adapters
- Fast Battery Charger AC-DC Power Converters

4 Simplified Application Circuit

4.1 USB-PD EPR Application Circuit



5 Ordering Information

5.1 Product Number Information

RT7795ML □-□□□□

Packing
A: Standard

Trim Code
(Refer to Product Selection Table)

Package Type(1)
N: WQFN-24L 4x6 (W-Type)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5.2 Product Selection Table

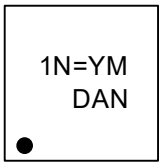
Product Number	RT7795 MLN-AHMA	RT7795 MLN-GHMA	RT7795 MLN-GHNA	RT7795 MLN-LHMA	RT7795 MLN-LHQA	RT7795 MLN-AHPA	RT7795 MLN-AGNA	RT7795 MLN-AQMA	RT7795 MLN-LGQA	RT7795 MLN-AFHA	RT7795 MLN-GFNA	RT7795 MLN-AFNA	RT7795 MLN-GFMA	RT7795 MLN-GFAA	RT7795 MLN-AENA	RT7795 MLN-GENA	RT7795 MLN-AQAA	RT7795 MLN-LEQA
Option	B/D	B/D	B	B	D	D	D	D	D	D	B	B	B	D	B	B	D	D
Maximum Normal Output Voltage, $V_{O\_NOR\_MAX}$	48V	48V	48V	48V	48V	48V	36V	36V	36V	28V	28V	28V	28V	28V	20V	20V	20V	20V
Highest Operation Frequency	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz	250kHz
BNI Voltage	110.3V	110.3V	110.3V	110.3V	99.8V	110.3V	117.4V	117.4V	99.8V	99.8V	110.3V	110.3V	110.3V	110.3V	110.3V	110.3V	99.8V	99.8V
BNO Voltage	99.8V	99.8V	99.8V	99.8V	87.7V	99.8V	106.1V	106.1V	87.7V	87.7V	99.8V	99.8V	99.8V	99.8V	99.8V	99.8V	87.7V	87.7V
Peak Load	O	O	X	O	X	X	X	X	X	X	X	X	O	X	X	X	O	X
ENPFC Function Output Voltage Threshold, V_{OUT_TH}	ENPFC $18V_{OUT}$	ENPFC $8V_{OUT}$	ENPFC $8V_{OUT}$	ENPFC $18V_{OUT}$	ENPFC $13V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $13V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $13V_{OUT}$	ENPFC $8V_{OUT}$	ENPFC $11V_{OUT}$	ENPFC $13V_{OUT}$	ENPFC $8V_{OUT}$	ENPFC $8V_{OUT}$	ENPFC $13V_{OUT}$
LH / LHLh Mode Change V_{OUT_TH}	$11V_{OUT}$	$8V_{OUT}$	$8V_{OUT}$	$11V_{OUT}$	$13V_{OUT}$	$11V_{OUT}$	$11V_{OUT}$	$11V_{OUT}$	$11V_{OUT}$	$8V_{OUT}$	$11V_{OUT}$	$8V_{OUT}$	$8V_{OUT}$	$11V_{OUT}$	$8V_{OUT}$	$8V_{OUT}$	$8V_{OUT}$	$13V_{OUT}$
Tiny Load Control PFC	O	O	O	O	O	X	O	O	O	O	X	O	O	O	O	X	X	O
Reduce Audio Noise Function	O	O	O	O	X	X	X	X	X	X	O	O	O	X	O	O	X	X
VDD OVP / Output OVP	Latch	Auto(1)	Auto(1)	Auto(1)	Latch)	Latch	Latch	Latch	Latch	Latch	Auto(1)	Latch	Auto(1)	Auto(1)	Latch	Auto(1)	Latch	Latch
COMP Open Protection / OCP	Latch	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Latch	Latch	Latch	Auto(1)	Latch	Auto(1)	Latch	Auto(1)	Auto(1)	Latch	Auto(1)	Latch	Auto(1)
VDD UVP	Latch	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Latch	Latch	Latch	Auto(1)	Latch	Auto(1)	Latch	Auto(1)	Auto(1)	Latch	Auto(1)	Latch	Auto(1)
Output UVP	Latch	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Latch	Latch	Latch	Auto(1)	Latch	Auto(1)	Latch	Auto(1)	Auto(1)	Latch	Auto(1)	Latch	Auto(1)
External OTP	Latch	Auto(1)	Auto(1)	Latch	Latch	Latch	Latch	Latch	Latch	Latch	Auto(1)	Latch	Auto(1)	Auto(1)	Latch	Auto(1)	Latch	Latch
VREG UVP	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)
SRSP	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)

Product Number	RT7795 MLN-AHMA	RT7795 MLN-GHMA	RT7795 MLN-GHNA	RT7795 MLN-LHMA	RT7795 MLN-LHQA	RT7795 MLN-AHPA	RT7795 MLN-AGNA	RT7795 MLN-AQMA	RT7795 MLN-LGQA	RT7795 MLN-AFHA	RT7795 MLN-GFNA	RT7795 MLN-AFNA	RT7795 MLN-GFMA	RT7795 MLN-GFAA	RT7795 MLN-AENA	RT7795 MLN-GENA	RT7795 MLN-AQAA	RT7795 MLN-LEQA
RZVS, DMAGP, TLSMIN, Pin Open/Short Protection	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)
Internal OTP	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)	Auto(1)

Note 2. Marked with (1) indicated: Auto-Recovery.

6 Marking Information

RT7795MLN-AHMA



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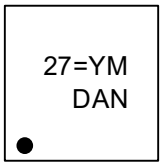

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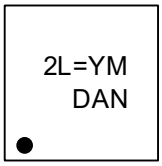

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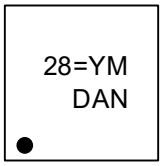

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RT7795MLN-LHQA

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RT7795MLN-AHPA

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RT7795MLN-AGNA

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RT7795MLN-AQMA

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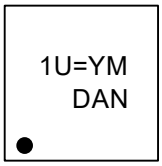
RT7795MLN-LGQA



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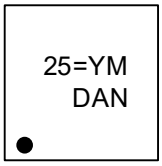

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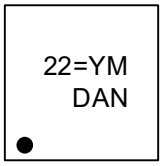

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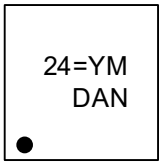

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RT7795MLN-GFAA

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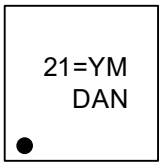

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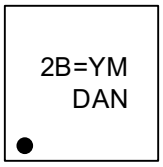

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RT7795MLN-AQAA

006: Product Code
YMDAN: Date Code

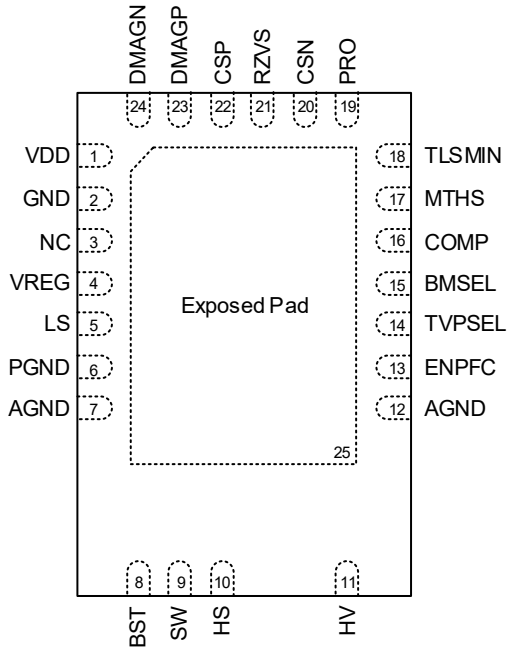
RT7795MLN-LEQA

02R: Product Code
YMDAN: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



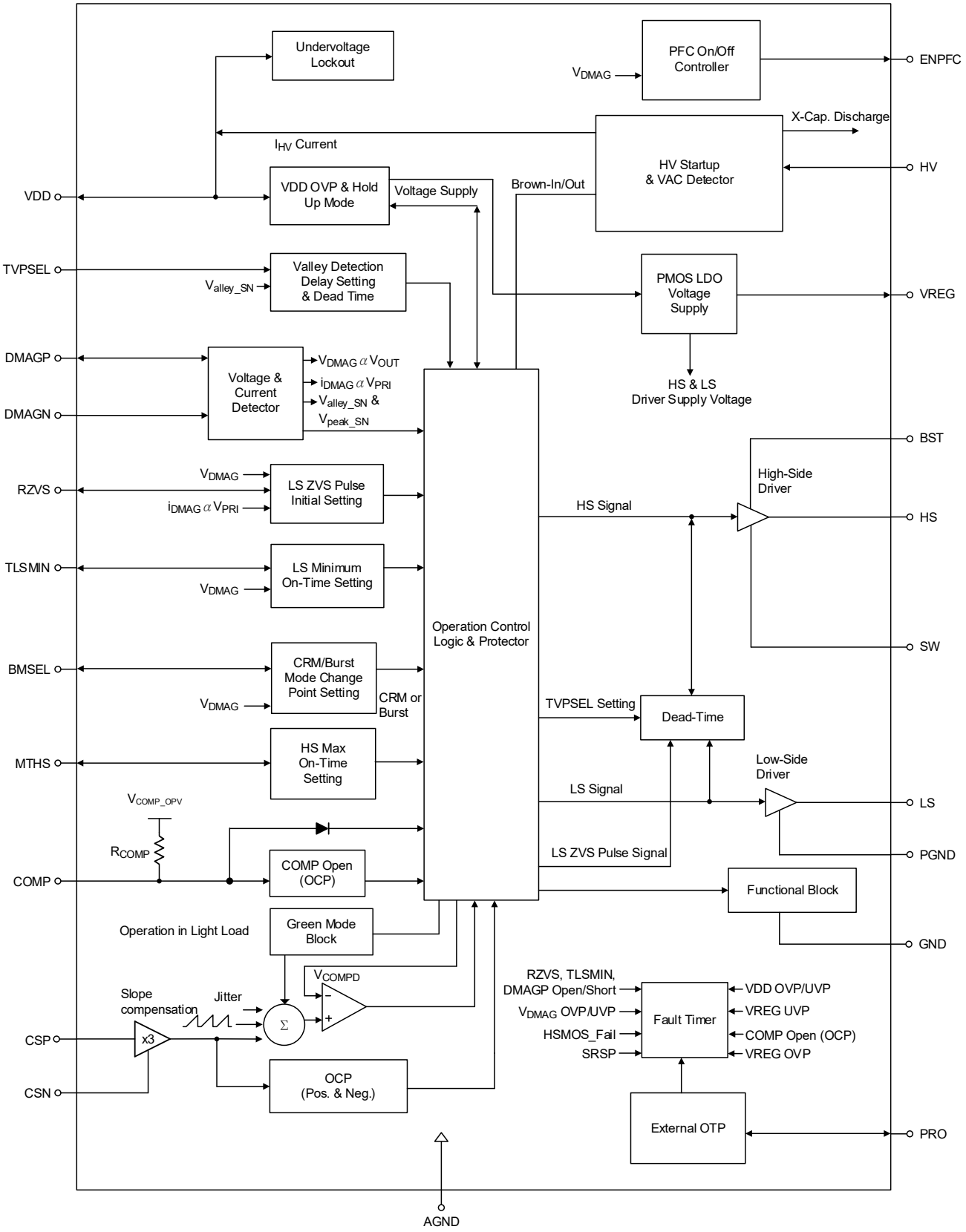
WQFN-24L 4x6

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD	Supply voltage input. C_{VDD} (10μF MLCC recommended, at least 2 times the value of C_{VREG}).
2	GND	Ground of internal function. (It is necessary to connect to AGND or the exposed pad through the PCB layout).
3	NC	No internal connection.
4	VREG	Internal LDO output voltage. C_{VREG} (1μF to 10μF MLCC recommended).
5	LS	Gate driver output for the low-side.
6	PGND	Ground of the LS gate driver.
7, 12	AGND	Analog ground (Signal ground).
8	BST	Supply voltage to HS. A bootstrap capacitor (0.1μF to 1μF MLCC recommended) is connected between this pin and the SW pin.
9	SW	HS driver floating-ground.
10	HS	Gate driver output for the high-side.
11	HV	High voltage input for start-up and X-Capacitor discharge functions.
13	ENPFC	Enable/Disable PFC.
14	TVPSEL	Input for setting a debounce time of valley-signal and peak-signal.
15	BMSEL	Input for setting a burst-mode voltage threshold.
16	COMP	Feedback signal input from the optocoupler. (Capacitor range: 100pF to 1nF. 1nF MLCC recommended.)
17	MTHS	Input for setting a maximum HS on-time.

Pin No.	Pin Name	Pin Function
18	TLSMIN	Input for setting LS minimum on-time.
19	PRO	Input for temperature detection.
20	CSN	Current-sense input (-).
21	RZVS	Input for setting the LS ZVS on-time.
22	CSP	Current-sense input (+). (Capacitor range: 10pF to 100pF. 10pF MLCC recommended.)
23	DMAGP	Demagnetization signal input (+). (Capacitor range: 10pF to 33pF. 10pF MLCC recommended.)
24	DMAGN	Demagnetization signal input (-).

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 3)

- HV to AGND Voltage ---------- –0.3V to 625V
- SW to PGND Voltage ---------- –2V to 625V
- Supply Input Voltage, VDD to AGND ---------- –0.3V to 70V
- VREG to PGND Voltage, V_{VREG_PGND} ---------- –0.3V to 18V
- BST to SW, V_{BST_SW} ---------- –0.3V to 18V
- HS to SW Voltage ---------- –0.3V to 18.3V
- LS to PGND Voltage ---------- –0.3V to 18.3V
- PGND, DMAGN, GND, CSN to AGND Voltage ---------- –0.3V to 0.3V
- COMP, MTHS, TLSMIN, BMSEL,
  RZVS, TVPSEL, PRO, ENPFC to AGND ---------- –0.3V to 6.5V
- CSP to AGND ---------- –3.5V to 6.5V
- DMAGP to AGND ---------- –1V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x6 ---------- 2.24W
- Package Thermal Resistance (Note 4)
  WQFN-24L 4x6, θ_{JA} ---------- 44.58°C/W
  WQFN-24L 4x6, θ_{JC} ---------- 11°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model)
  Except HV, HS, SW, BST Pin ---------- 2kV
  HV, HS, SW, BST to GND ---------- 1kV

Note 3. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- HV to AGND Voltage, V_{HV} ---------- –0.3V to 500V
- SW to PGND Voltage, V_{SW_PGND} ---------- –1V to 500V
- Supply Input Voltage, VDD ---------- 11V to 63V

- VREG to PGND Voltage, V_{VREG_PGND} ---------- 8.5V to 15V
- BST to SW, V_{BST_SW} ---------- 7.5V to 15V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 6. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
HV Section							
HV Leakage Current in Off-State	I_{HV_LK}	V_{DD} > V_{TH_ON}, V_{HV} = 500V		5	12.5	20	μA
HV Start-Up Current	I_{HV_ST}	V_{DD} < V_{TH_ON}, V_{HV} = 500V		1	3.5	6	mA
		V_{DD} < V_{TH_ON}, V_{HV} = 100V		0.55	1.5	2.6	
HV Sinking Current for X-Capacitor Discharge	I_{HV_SINK}	V_{HV} = 50V		0.7	1	--	mA
Threshold Voltage of HV Brown-In	V_{TH_HVBNI}	83Vac	RT7795MLN-AGNA/AQMA	108	117.4	126.8	V
		78Vac	Default	101.5	110.3	119.1	
		70Vac	RT7795MLN-LHQA/LGQA/AFHA/AQAA/LEQA	91.8	99.8	107.7	
Threshold Voltage of HV Brown-Out	V_{TH_HVBNO}	75Vac	RT7795MLN-AGNA/AQMA	97.6	106.1	114.6	V
		70Vac	Default	91.8	99.8	107.7	
		62Vac	RT7795MLN-LHQA/LGQA/AFHA/AQAA/LEQA	80.7	87.7	94.7	
Debounce Time of HV Brown-In	t_{DB_HVBNI}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		38.2	52.5	69	μs
Debounce Time of HV Brown-Out	t_{DB_HVBNO}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		49	59.5	79.7	ms
Delay Time for Exit Auto-Recovery Protection	t_{D_AUTO}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		1645	1951	2261	ms
Debounce Time of AC Removal Detection	t_{DB_NOAC}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		98	119	141	ms
Maximum X-Capacitor Discharge Time	t_{XCAP_DISCHG}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		1645	1951	2261	ms
Threshold Voltage of High-Line Detection	V_{TH_HILINE}			217.4	230	242.6	V
Threshold Voltage of Low-Line Detection	V_{TH_LOLINE}			205	220	235	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Debounce Time of High-Line Detection	t_{DB_HILINE}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	38.2	52.5	69	μs
Debounce Time of Low-Line Detection	t_{DB_LOLINE}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	49	59.5	70.7	ms
VDD Section						
VDD Overvoltage Protection Threshold	V_{VDD_OVP}		63.2	66.5	69.8	V
VDD Undervoltage Protection (VDD UVP) Threshold	V_{VDD_UVP}		8.5	9	9.5	V
Turn-On Threshold	V_{TH_ON}		16	18.5	21	V
Turn-Off Threshold	V_{TH_OFF}		7.5	8	8.5	V
VDD Holdup Mode Entry Threshold	V_{VDD_HDET}	Entrance green mode and VDD falling, to start forced HS switching and turn on the HV device.	8.5	9	9.5	V
VDD Holdup Mode Ending Threshold	V_{VDD_HDED}	Entrance green mode and VDD rising, to stop forced HS switching and turn off the HV device.	V_{DD_HDET} + 0.3	V_{DD_HDET} + 0.5	V_{DD_HDET} + 0.7	V
Debounce Time of VDD OVP	t_{DB_VDDOVP}	Counted by continuous HS pulses	--	4	--	Pulse
Debounce Time of VDD UVP	t_{DB_VDDUVP}	Counted by continuous HS pulses	--	4	--	Pulse
Debounce Time of Disabling VDD Hold Up Mode	$t_{DB\_DIS\_VDDHD}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	809	968	1130	ms
Start-Up Current	I_{DD_ST}	$V_{DD} < V_{TH\_ON} - 0.1V$	--	--	20	μA
Operating Supply Current	I_{DD_OP}	V_{DD} = 15V, HS = LS = 0V, V_{COMP} = 0V In green mode	--	1000	1200	μA
	I_{DD_OP1}	V_{DD} = 15V, HS = LS = open In normal mode	--	2	2.6	mA
Sinking Current after Trigger a Protection	I_{DD_SIKPRO}		1.6	2.1	2.6	mA
Sinking Current for Brown-Out Protection	I_{DD_SIKBNO}		1.5	1.8	2.1	mA
Latch-Off Operating Current	I_{DD_LH}		--	250	350	μA
Built-In Regulator (VREG-LDO) Section						
Regulated VREG Voltage	V_{VREG_REG}	I_{VREG} = 0 to 40mA, V_{DD} = 12V to 65V, C_{VREG} = 1μF to 10μF	11	11.5	12	V
VREG Current-Limit Threshold	I_{VREG_CL}	$V_{VREG} < V_{VREG\_REG} - 0.1V$, V_{DD} = 12V to 65V	78	120	162	mA
Threshold Voltage of VREG Overvoltage Protection (VREG OVP)	V_{VREG_OVP}		12.8	13.6	14.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Threshold Voltage of VREG Undervoltage Protection (VREG UVP)	V_{VREG_UVP}			7	7.5	8	V
VREG Sinking Current during VREG-LDO Turn-Off	I_{VREG_SIKPRO}	The sinking current (I_{VREG_SIKPRO}) is turned on to discharge the VREG output capacitor during turn-off of the VREG-LDO. (Note 7)		1	2	3	mA
COMP Input Section							
COMP Open-Loop Voltage	V_{COMP_OPV}	Enable peak load version.		3.9	4.1	4.3	V
		Disable peak load version.		2.95	3.15	3.35	
COMP Built-In Pull-High Resistor	R_{COMP}	The resistor is connected between COMP pin and the V_{COMP_OPV} node.		16	20	24	kΩ
Delay Time of COMP Open-Loop Protection	t_{COMP_OP}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		49	59.5	70.7	ms
Internal Diode Voltage	V_{OFS_COMP}			530	730	860	mV
Offset Voltage used in V_{BURST_TH}	V_{OFS_CLAMP}	R_{BMSEL} = 10kΩ	Option: B, D	320	350	380	mV
		R_{BMSEL} = Open	Option: B, D	289	309	328	
		R_{BMSEL} = 68kΩ	Option: B, D	245	275	305	
		R_{BMSEL} = 0kΩ	Option: D	220	250	280	
		R_{BMSEL} = 33kΩ	Option: D	195	225	255	
		R_{BMSEL} = 100kΩ	Option: D	170	200	230	
Voltage Modulation Ratio used in V_{BURST_TH}	K_{V_BST}	$V_{O\_NOR\_MAX}$ = 48V		0.193	0.21	0.226	V/V
		$V_{O\_NOR\_MAX}$ = 36V		0.257	0.28	0.302	
		$V_{O\_NOR\_MAX}$ = 28V		0.21	0.228	0.246	
		$V_{O\_NOR\_MAX}$ = 20V		0.289	0.315	0.34	
Current Sense Section							
Gain of Current-Sense Amplifier	K_{CS_GAIN}			2.83	3	3.17	V/V
Maximum Current Limit	V_{CSOCP1}			0.38	0.4	0.42	V
	V_{CSOCP2}	Peak load is enabled.		0.55	0.6	0.65	
Threshold Voltage of Quick Overcurrent Protection (QOCP)	V_{CS_QKOCP}	No peak load. The IC can pull low HS.		0.45	0.5	0.55	V
		Peak load is enabled. The IC can pull low HS.		0.85	0.9	0.95	V
Secondary Rectifier Short-Circuit Protection Threshold Voltage	V_{CS_SRSP}	Auto-recovery protection. The IC can pull low HS.		1.1	1.2	1.3	V
Delay Time of Overcurrent Protection	t_{D_OCP}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		49	59.5	70.7	ms

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Maximum Interval of Peak-Load Operation	t_{PEAK_LOAD}	Counted by IC internal CLK signal. Peak load is enabled. f_{CLK} = 66.67kHz (Note 7)		24.5	29.9	35.3	ms
Leading-Edge Blanking Time	t_{LEB}	HS can be pulled low by the peak-current mode and OCP signals.		318.8	386.9	455	ns
Shorter Leading Edge Blanking Time	t_{LEB1}	HS can be pulled low by the QOCP and SRSP signals.		220	257	295	ns
SRSP Debounce Time	t_{DB_SRSP}	Counted by HS pulses. (Note 7)		--	4	--	Pulse
Dead-Time after Falling Edge of HS Voltage	t_{DEAD_HL}	Dead time "HS starts to fall" to "LS starts to rise".		120	150	180	ns
Maximum On-Time of HS Pulse	t_{HS_MAX}	The time starts at V_{CS} > 0V during on-time of HS pulse.	R_{MTHS} = 0Ω Option: B	4.05	4.8	5.55	µs
			R_{MTHS} = 0Ω Option: D	13.5	14.5	15.5	
			R_{MTHS} = 10kΩ	4.8	5.7	6.7	
			R_{MTHS} = 68kΩ	5.95	6.65	7.4	
			R_{MTHS} = 33kΩ	6.5	7.5	8.5	
			R_{MTHS} = 100kΩ	7.15	8.5	9.85	
			R_{MTHS} = Open	8	9.5	11	
Jitter Range of Gain Modulation of Current-Sense Amplifier	Δk_{CS_Jitter}	(Note 7)		--	±6	--	%
Typical Range of Offset Voltage Used to Reduce HS MOSFET's Peak Current in Light-Load Operation	V_{RED_IPK}	To reduce the HS MOSFET's peak current in light-load operation. (Note 7)		--	--	50	%
Threshold of CS Negative Overcurrent Protection-2	$V_{NCSOCP2}$	V_{CS} falling; For a LS discharge pulse, the IC can pull LS voltage low when V_{CS} < $V_{NCSOCP2}$.		–2.15	–1.8	–1.45	V
DMAG Voltage (V_{DMAG}) Detections via the DMAGP and DMAGN Pins							
Ratio of DMAG Voltage to Converter's Output Voltage (V_{OUT})	K_{V_DMAG}	DMAG voltage: V_{DMAG} = V_{DMAGP} - V_{DMAGN} = K_{V_DMAG} x V_{OUT}. The ratio is set by the external resistor-divider connected with the DMAGP and DMAGN pins.	$V_{O\_NOR\_MAX}$ = 48V or 36V	--	0.085	--	V/V
			$V_{O\_NOR\_MAX}$ = 20V or 28V	--	0.136	--	
Input Voltage Range of DMAGP and DMAGN Differential Amplifier (DMAG AMP)	V_{DMAG}	Input voltage of V_{DMAG} = V_{DMAGP} - V_{DMAGN} (Note 7)		0	--	5.2	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DMAG Overvoltage Protection (DMAG OVP) Threshold after Start-Up	V_{DMAG_OVP}	The threshold is compared with the V_{DMAG} for the DMAG OVP. $V_{O\_NOR\_MAX}$ = 48V V_{DMAG} > V_{DMAG_OVP} V_{OUT_OVP} = 57.8V		4.68	4.92	5.17	V
		$V_{O\_NOR\_MAX}$ = 36V V_{DMAG} > V_{DMAG_OVP} V_{OUT_OVP} = 43.6V		3.52	3.71	3.9	
		$V_{O\_NOR\_MAX}$ = 28V V_{DMAG} > V_{DMAG_OVP} V_{OUT_OVP} = 33.6V		4.34	4.57	4.8	
		$V_{O\_NOR\_MAX}$ = 20V V_{DMAG} > V_{DMAG_OVP} V_{OUT_OVP} = 24.1V		3.12	3.28	3.45	
Percentage of Adaptive Overvoltage Protection (AOVP) Threshold	K_{V_AOVP}			120	125	130	%
DMAG Threshold of Output Undervoltage Protection-1 (UVP1)	V_{DMAG_UVP1}	$V_{O\_NOR\_MAX}$ = 48V or 36V V_{OUT} UVP = 2.35V For PD application, the UVP1 signal is used after soft-start process.		0.16	0.2	0.24	V
		$V_{O\_NOR\_MAX}$ = 28V or 20V		0.255	0.3	0.345	V
Debounce Time of DMAG OVP	$t_{DB\_DMAGOVP}$	Counted by HS pulses. (Note 7)		--	4	--	Pulse
Debounce Time of DMAG OVP	t_{DB_AOVP}	Counted by HS pulses. (Note 7)		--	4	--	Pulse
Debounce Time of DMAG UVP1 after Soft-Start	$t_{DB\_DMAGUVP1}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		2.86	3.6	4.42	ms
DMAG Threshold Voltage for Enabling a PFC Controller	$V_{DMAG\_EN\_PFC}$	The ENPFC pin outputs high impedance/high-level voltage to enable a PFC controller at rising (V_{DMAG} > $V_{DMAG\_EN\_PFC}$) V_{OUT_TH} = ~8V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-GHMA/GHNA	0.665	0.7	0.735	V
		V_{OUT_TH} =~ 8V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-GFMA/AENA/GENA/AQAA	1.045	1.1	1.155	
		V_{OUT_TH} = ~11V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-AHPA/AGNA/AQMA/LGQA	0.875	0.925	0.965	
		V_{OUT_TH} = ~11V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-GFNA/GFAA	1.377	1.450	1.522	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		V_{OUT_TH} = ~13V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-AFHA/AFNA/AENA/LEQA	1.758	1.85	1.943	
		V_{OUT_TH} = ~18V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-AHMA/LHMA	1.473	1.550	1.628	
DMAG Threshold Voltage for Disabling a PFC Controller	$V_{DMAG\_DIS\_PFC}$	The ENPFC pin pulls low to disable a PFC controller at end of the $t_{DB\_DIS\_PFC}$ (V_{DMAG} < $V_{DMAG\_DIS\_PFC}$). V_{OUT_TH} = ~7V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-GHMA/GHNA	0.565	0.6	0.635	V
		V_{OUT_TH} = ~7V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-GFMA/AENAGENA/AQAA	0.903	0.95	0.998	
		V_{OUT_TH} = ~10V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-AHPA/AGNA/AQMA/LGQA	0.825	0.875	0.925	
		V_{OUT_TH} = ~10V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-GFNA/GFAA	1.330	1.400	1.470	
		V_{OUT_TH} = ~12V $V_{O\_NOR\_MAX}$ = 28V or 20V	RT7795MLN-AFHA/AFNA/AENA/LEQA	1.615	1.700	1.785	
		V_{OUT_TH} = ~17V $V_{O\_NOR\_MAX}$ = 48V or 36V	RT7795MLN-AHMA/LHMA	1.378	1.450	1.523	
DMAG Signal Detections via the DMAGP and DMAGN Pins							
Maximum DMAGP Sourcing Current	I_{DMAG_MAX}	DMAGP sourcing current: I_{DMAG}		1.55	--	--	mA
Threshold Current of DMAGP Undercurrent Protection (DMAG UCP)	I_{DMAG_UCP}			25	32	39	μA
Debounce Time before DMAG Valley Signal	t_{DB_VALLEY}	Setting pin for selecting a debounce time for valley-signal and peak-signal.	R_{TVPSEL} = 10kΩ	158	173	195	ns
			R_{TVPSEL} = 33kΩ	207	231	255	
			R_{TVPSEL} = 0kΩ	257	285	314	
			R_{TVPSEL} = open	288	320	352	

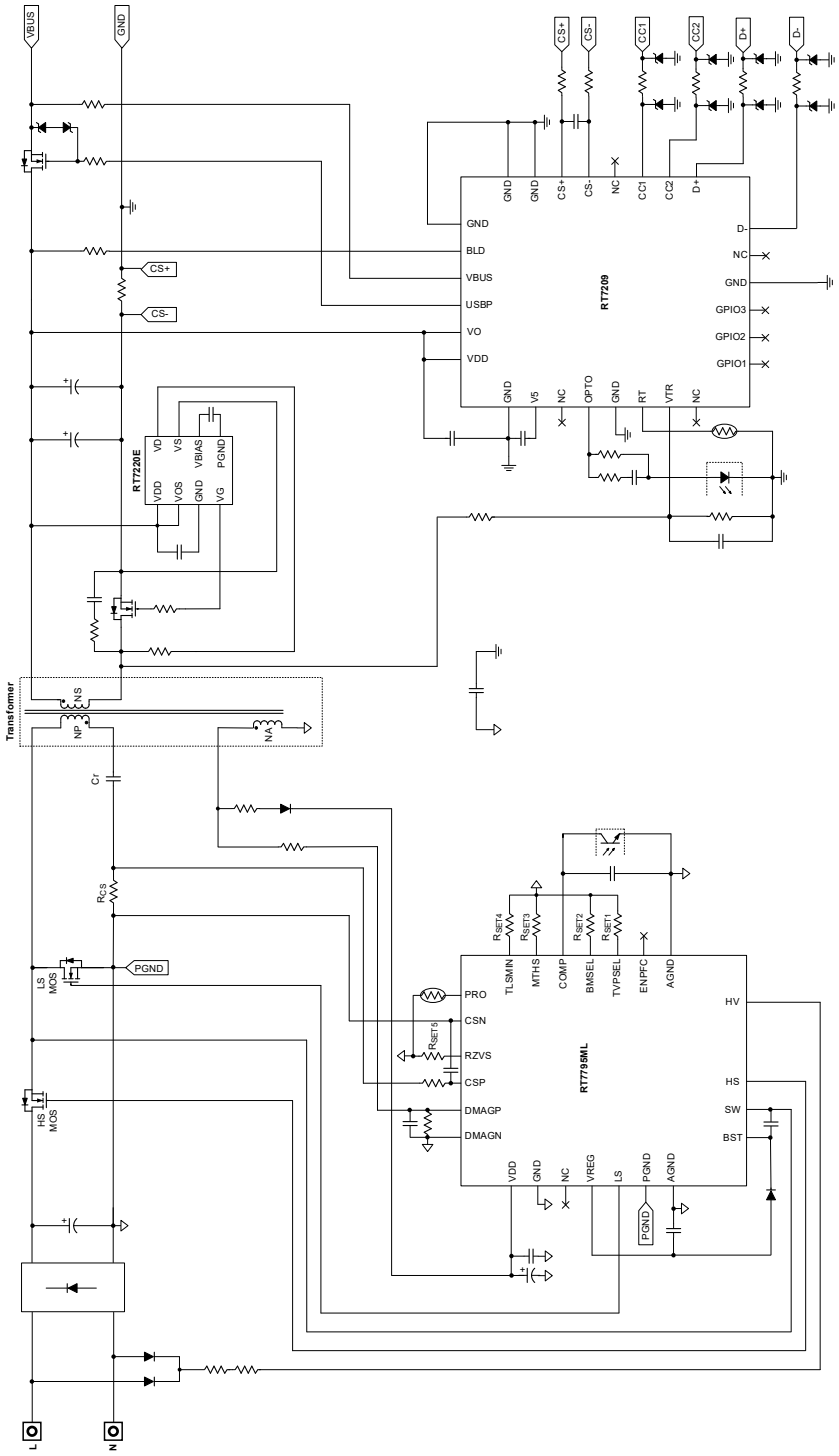
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
			R_{TVPSEL} = 68kΩ	338	375	413	
			R_{TVPSEL} = 100kΩ	387	431	475	
On-Time Controls of LS DCM-ZVS (Discontinuous-Conduction-Mode Zero-Voltage-Switching) Pulse and LS Discharge Pulse							
LS DCM/CRM-ZVS Pulse Initial Setting Pin	R_{RZVS}	(Note 7)		25	--	170	kΩ
Minimum On-Time of LS DCM/CRM-ZVS Pulse	t_{ZVS_MIN}	The on-time is from "LS starts to rise" to "LS starts to fall".		255	347.5	440	ns
Minimum On-Time of LS Setting Pin	R_{TLSMIN}	(Note 7)		20	--	150	kΩ
Gate Driver Section							
HS Output High-Level Voltage	$V_{HS\_SW\_HIGH}$	V_{BST_SW} = V_{VREG_PGND} = 10V, Sourcing I_{HS} = 50mA		9.1	9.7	--	V
LS Output High-Level Voltage	$V_{LS\_PGND\_HIGH}$	V_{BST_SW} = V_{VREG_PGND} = 10V, Sourcing I_{LS} = 50mA		9.1	9.7	--	V
Maximum HS Sourcing Current	$I_{HS\_SRC\_MAX}$	V_{BST_SW} = V_{VREG_PGND} = 12V, HS = SW (Note 7)		--	900	--	mA
Maximum HS Sinking Current	$I_{HS\_SINK\_MAX}$	V_{BST_SW} = V_{VREG_PGND} = 12V, HS = BST (Note 7)		--	2100	--	mA
Maximum LS Sourcing Current	$I_{LS\_SRC\_MAX}$	V_{BST_SW} = V_{VREG_PGND} = 12V, LS = PGND (Note 7)		--	900	--	mA
Maximum LS Sinking Current	$I_{LS\_SINK\_MAX}$	V_{BST_SW} = V_{VREG_PGND} = 12V, LS = VREG (Note 7)		--	2100	--	mA
HS Voltage (V_{HS_SW}) Rise Time	t_{RISE_HS}	V_{BST_SW} = V_{VREG_PGND} = 12V, C_L = 3.3nF, V_{HS_SW} = 10% to 90% of V_{BST_SW}		--	67	100	ns
HS Voltage (V_{HS_SW}) Fall Time	t_{FALL_HS}	V_{BST_SW} = V_{VREG_PGND} = 12V, C_L = 3.3nF, V_{HS_SW} = 90% to 10% of V_{BST_SW}		--	40	60	ns
LS Voltage (V_{LS_PGND}) Rise Time	t_{RISE_LS}	V_{BST_SW} = V_{VREG_PGND} = 12V, C_L = 3.3nF, V_{LS_SW} =10% to 90% of V_{BST_SW}		--	67	100	ns
LS Voltage (V_{LS_PGND}) Fall Time	t_{FALL_LS}	V_{BST_SW} = V_{VREG_PGND} = 12V, C_L = 3.3nF, V_{LS_SW} = 90% to 10% of V_{BST_SW}		--	40	60	ns
Enable/Disable Control for PFC Controller (ENPFC)							
ENPFC Pull-High Voltage	V_{OH_ENPFC}			3	--	5	V
Debounce Time for Enabling a PFC Controller	$t_{DB\_EN\_PFC}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)		3	--	4	CLK

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Debounce Time for Disabling a PFC Controller	$t_{DB\_DIS\_PFC}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	434.7	476	522.9	ms
DC BNI Option: ENPFC Threshold Voltage of Bulk Brown-In Detection	$V_{TH\_BULK\_BNI}$	V_{ENPFC} rising, the pull-low N-MOSFET is off.	1.77	1.84	1.91	V
DC BNI Option: ENPFC Threshold Voltage of Bulk Brown-Out Detection	$V_{TH\_BULK\_BNO}$	V_{ENPFC} falling, the pull-low N-MOSFET is off.	1.59	1.65	1.71	V
DC BNI Option: Debounce Time of Bulk Brown-in	$t_{DB\_BULKBNI}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	1.53	1.86	2.21	ms
DC BNI Option: Debounce Time of Bulk Brown-out Protection	$t_{DB\_BULKBNO}$	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	49	59.5	70.7	ms
External Over-Temperature Protection (EOTP) by the PRO Pin						
PRO Output Current Source	I_{PRO}	V_{PRO} = 0 to 1V	90	100	110	μA
PRO Threshold Voltage of EOTP	V_{TH_PRO}		0.95	1	1.05	V
EOTP Debounce Time	t_{DB_OTP}	Counted by IC internal CLK signal. f_{CLK} = 66.67kHz (Note 7)	39.2	53.8	70.7	ms

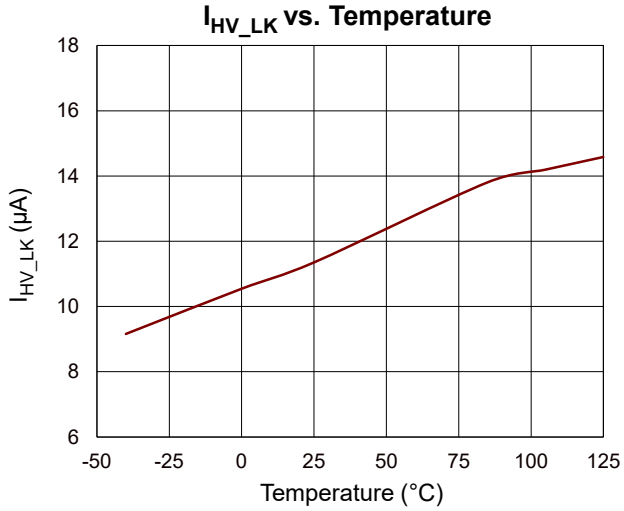
Note 7. Guaranteed by design.

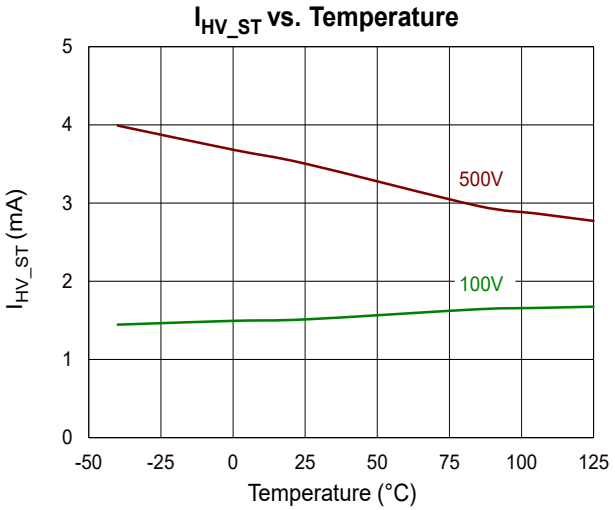
13 Typical Application Circuit

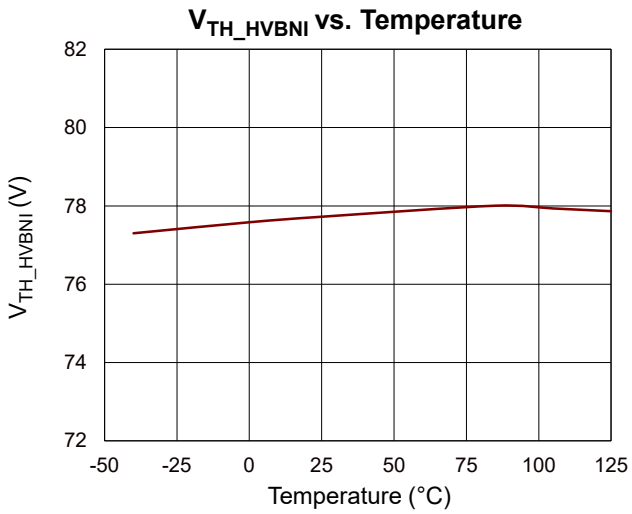
13.1 USB-PD EPR Application Circuit

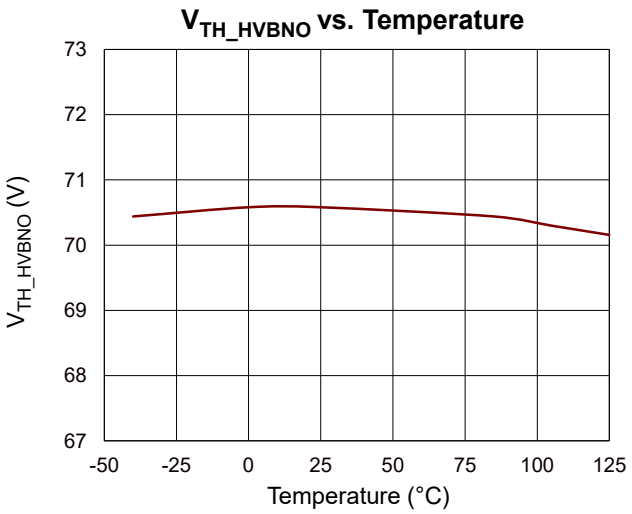


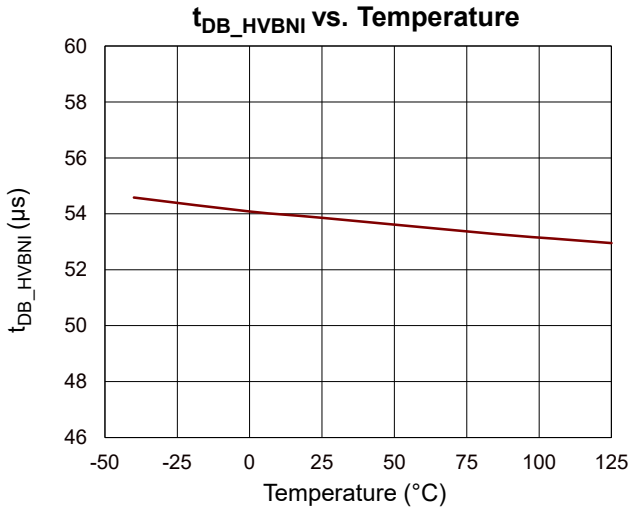
14 Typical Operating Characteristics

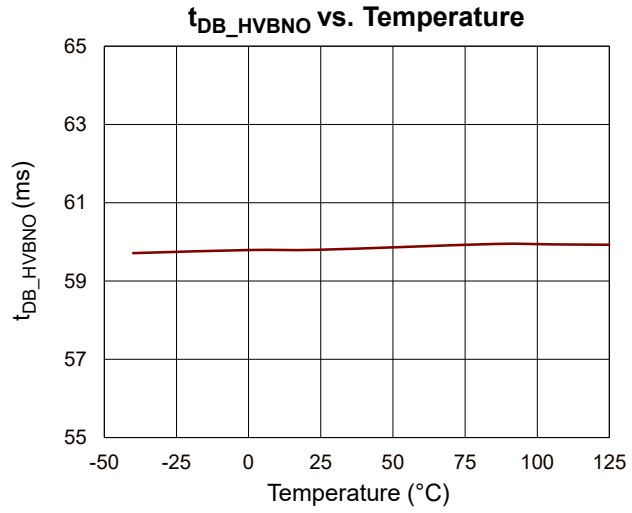


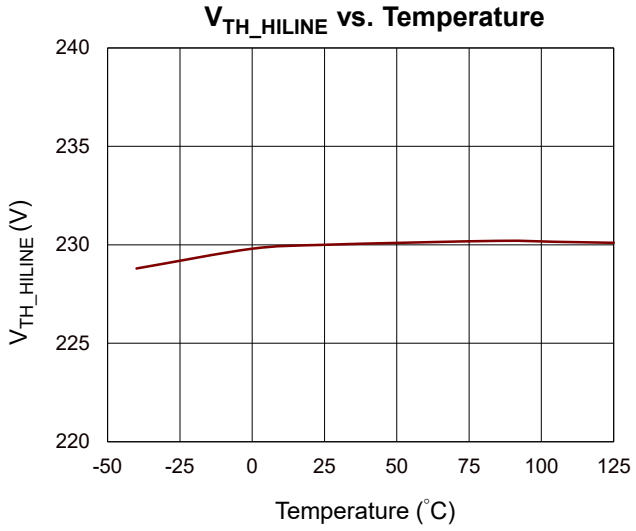


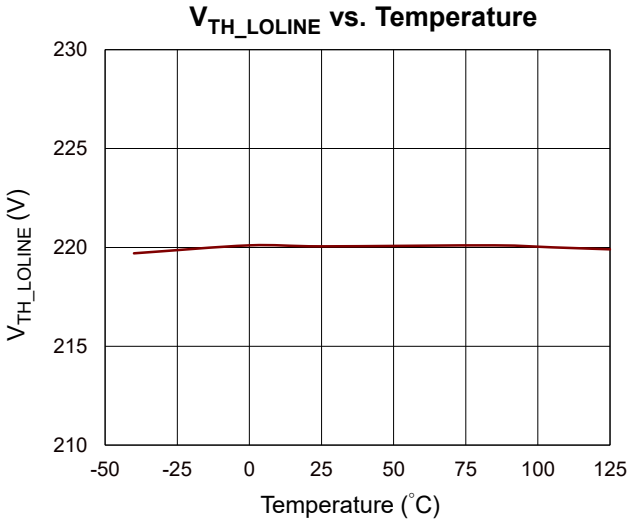


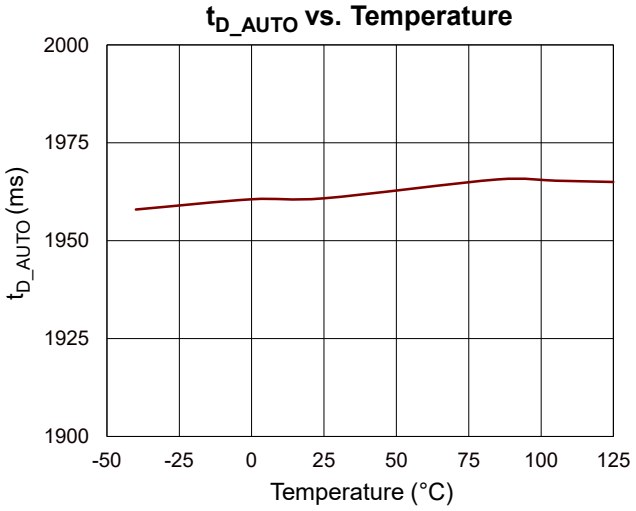


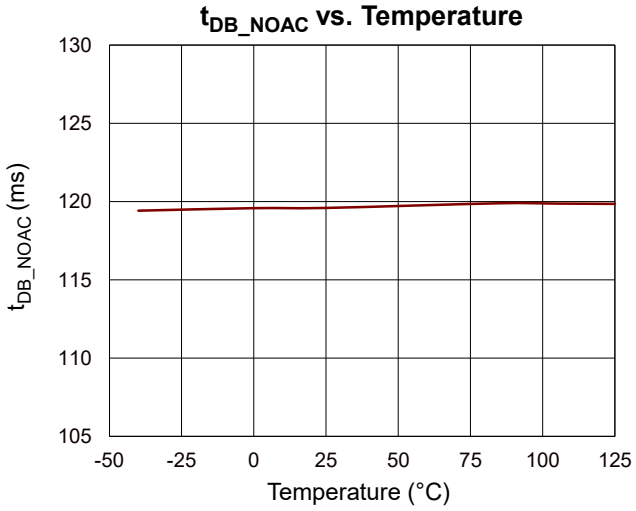


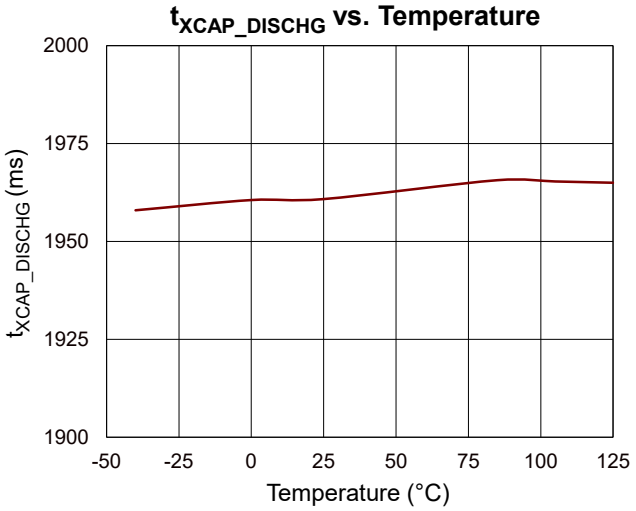


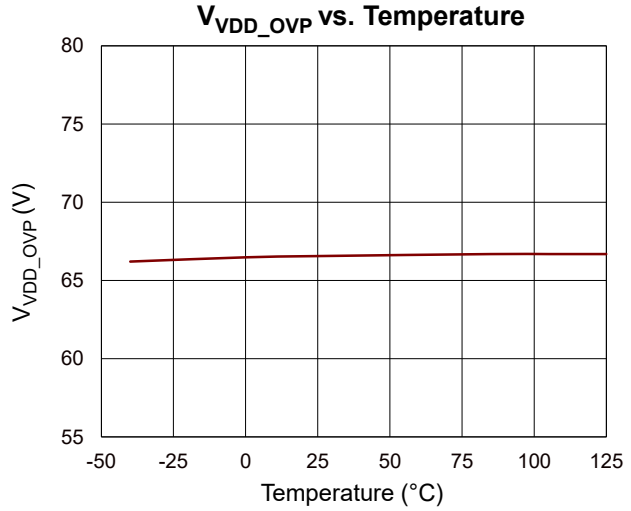


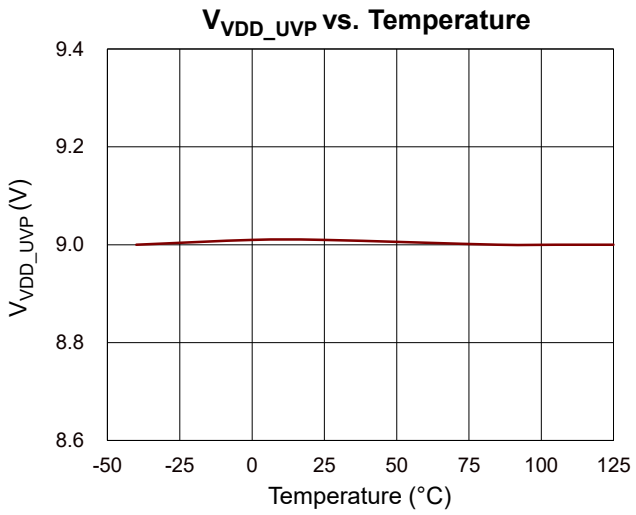


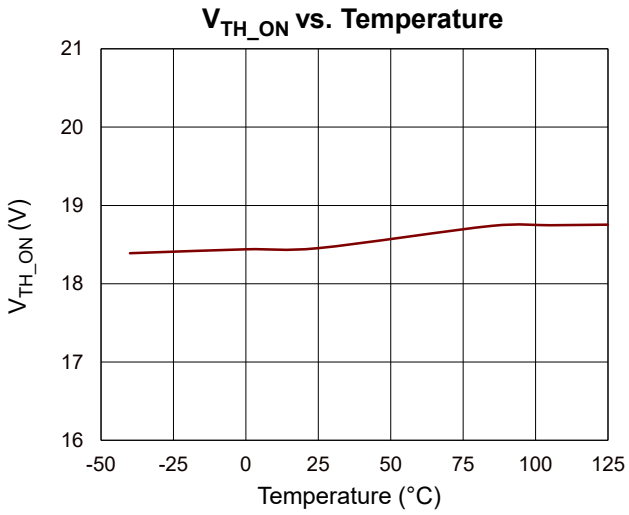


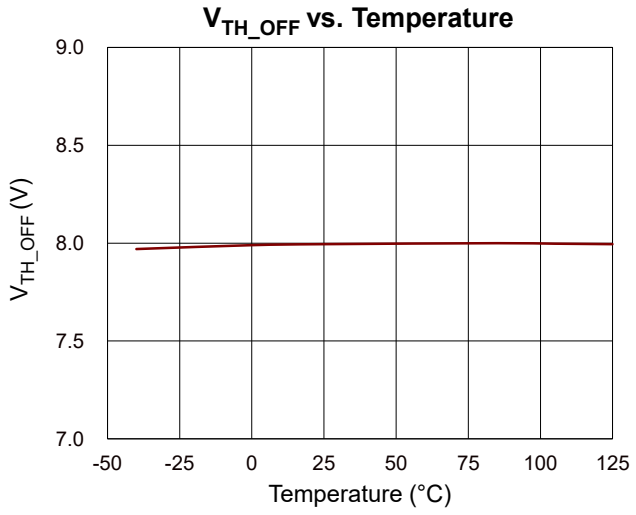


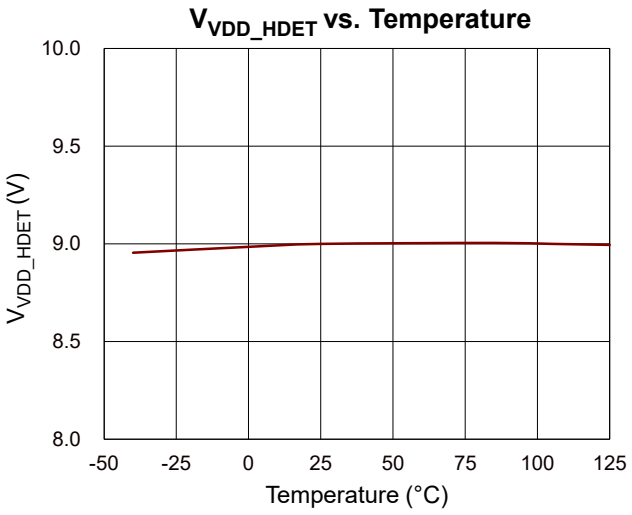


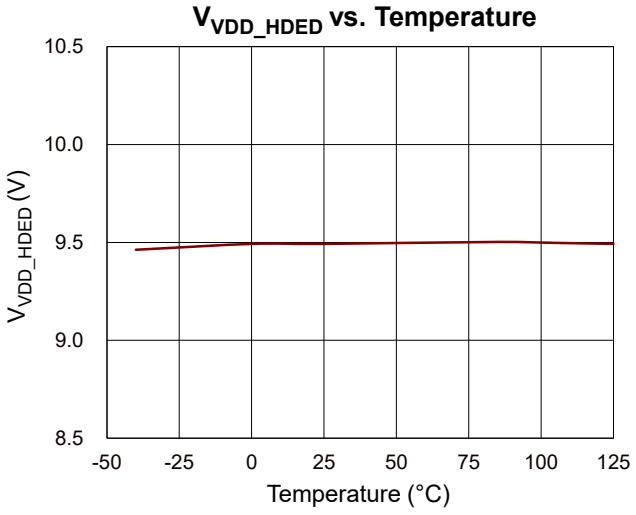


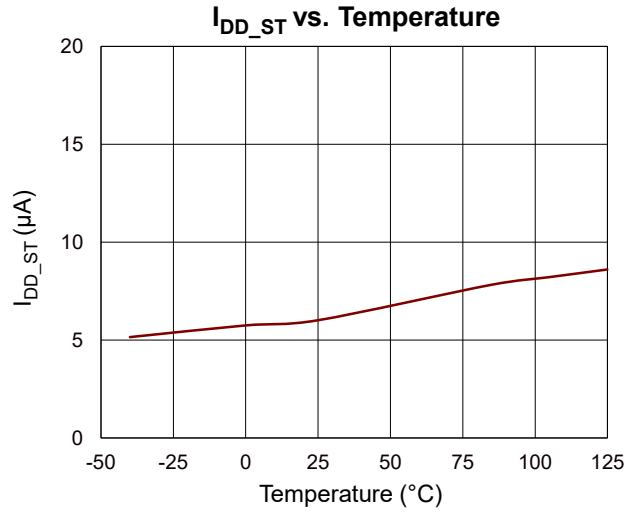


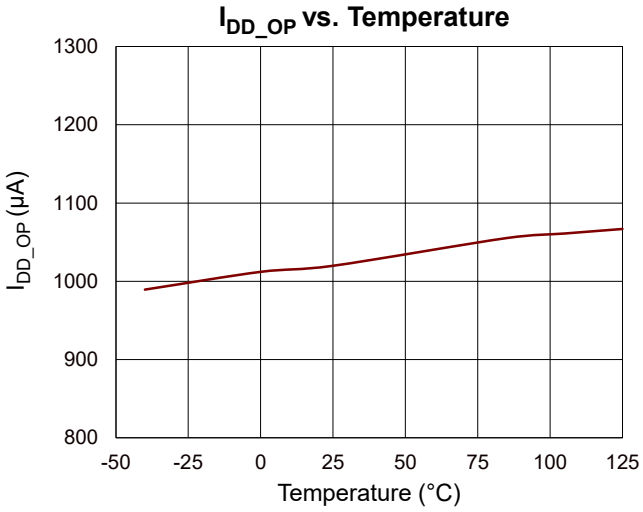


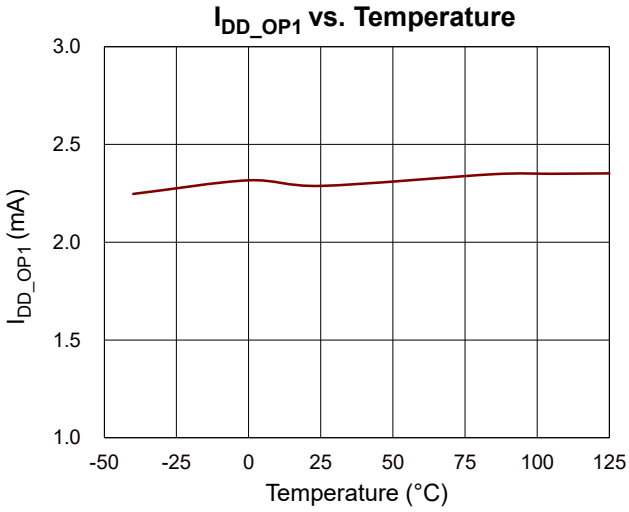


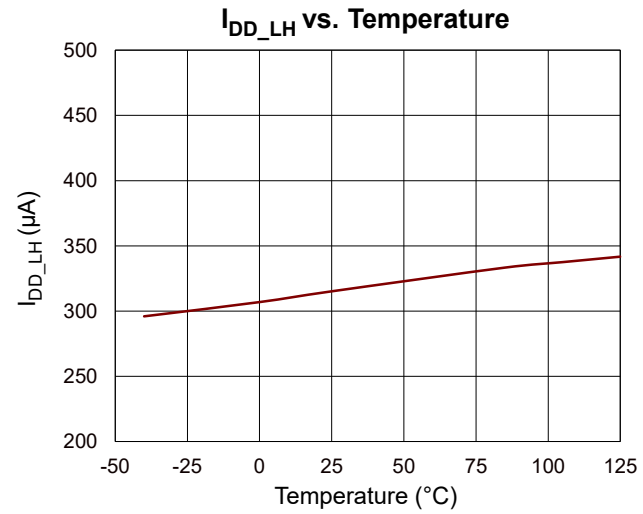


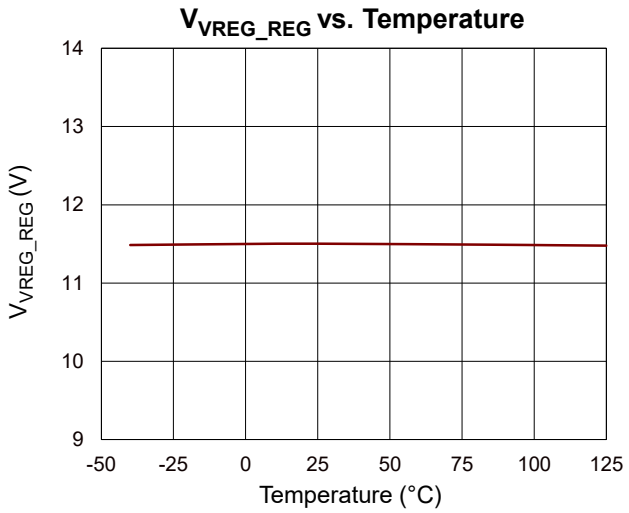


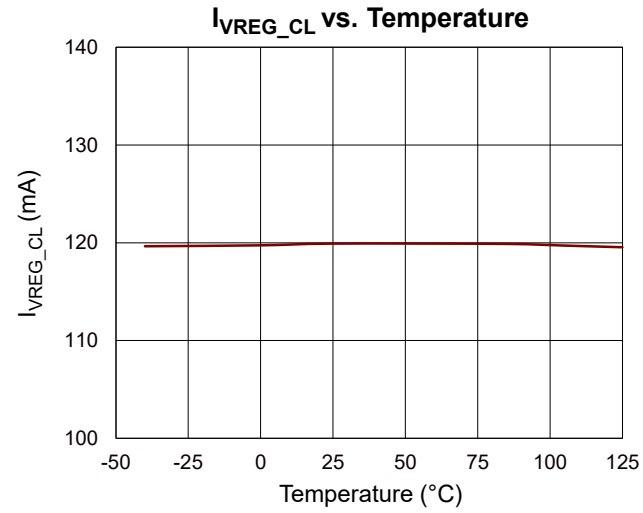


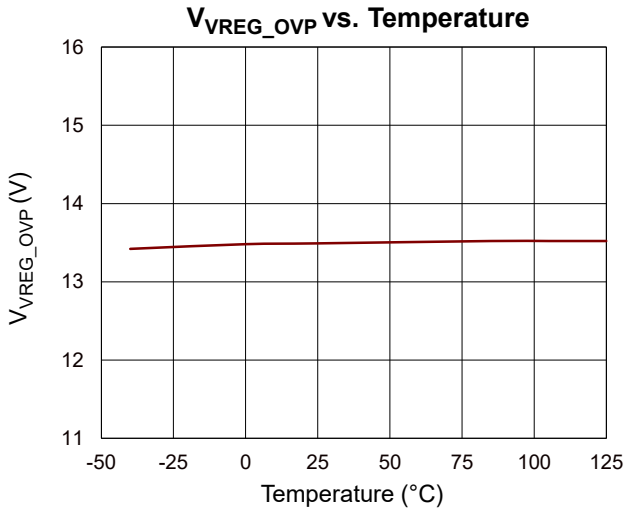


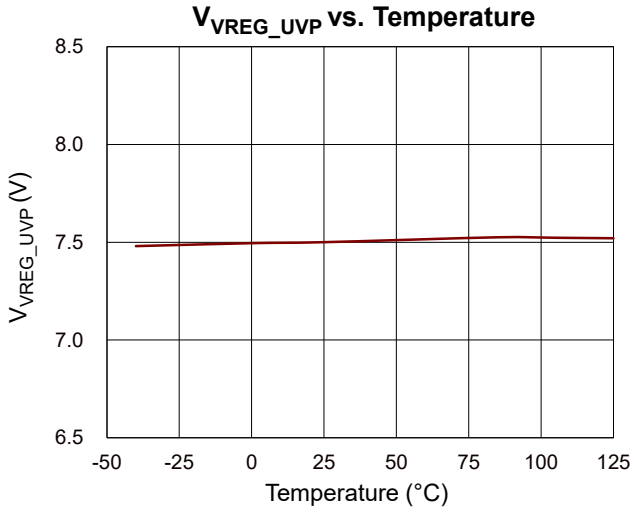


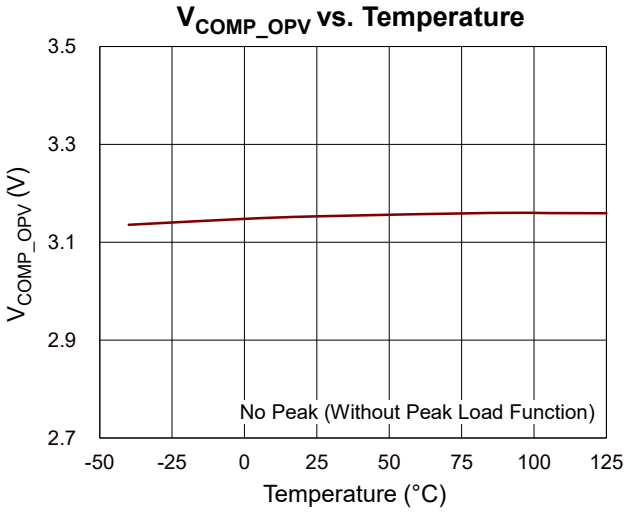


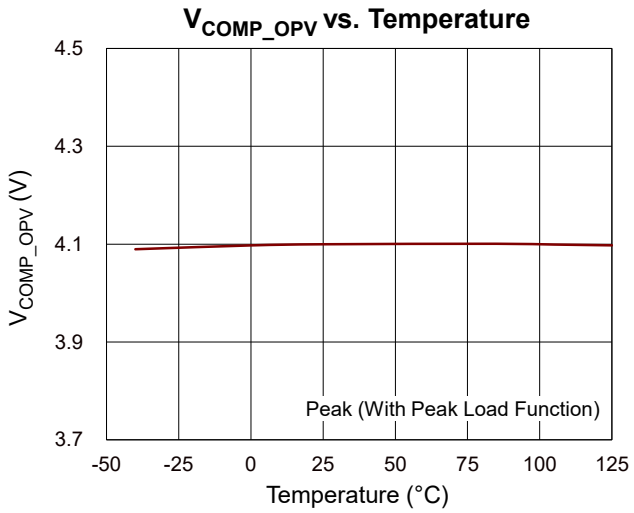


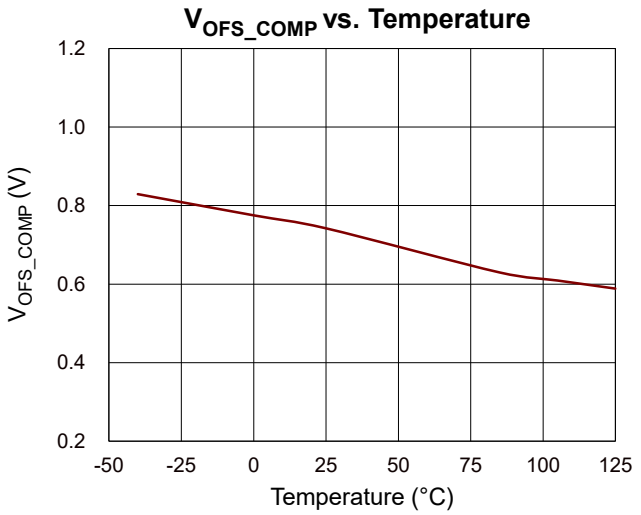


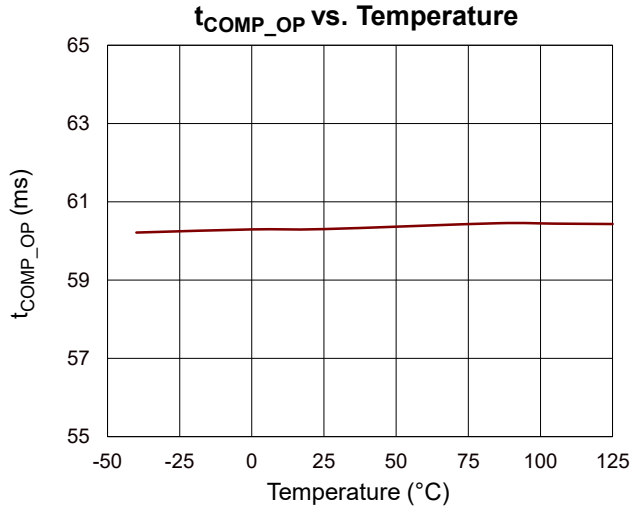


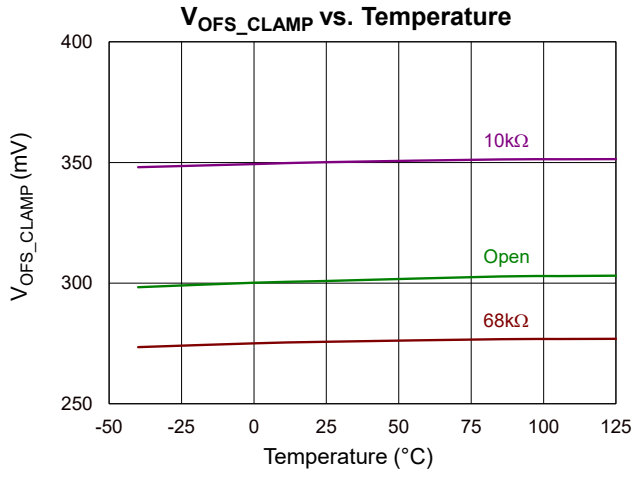


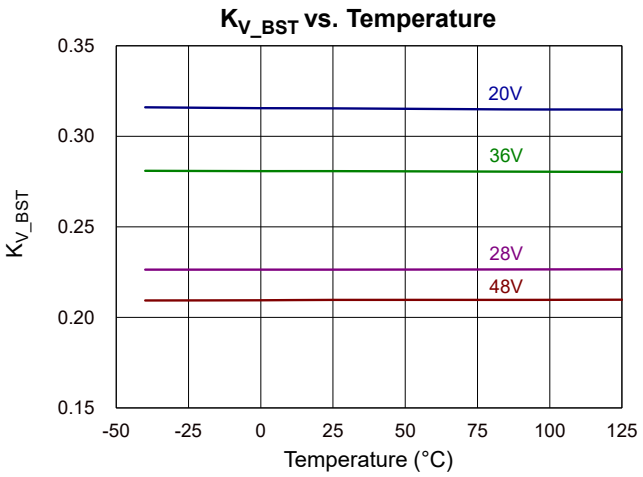


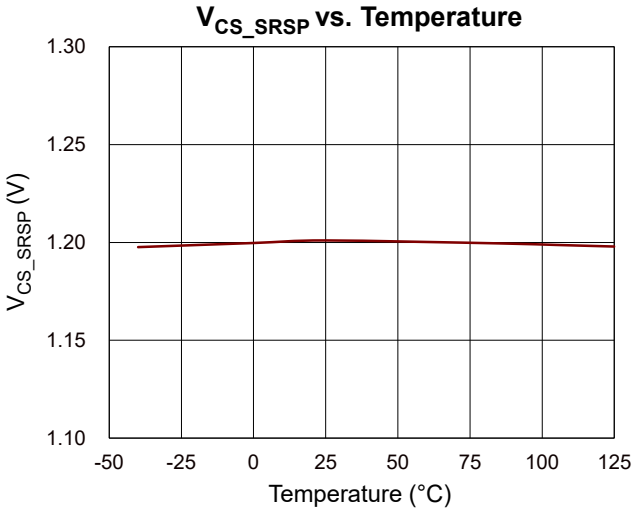


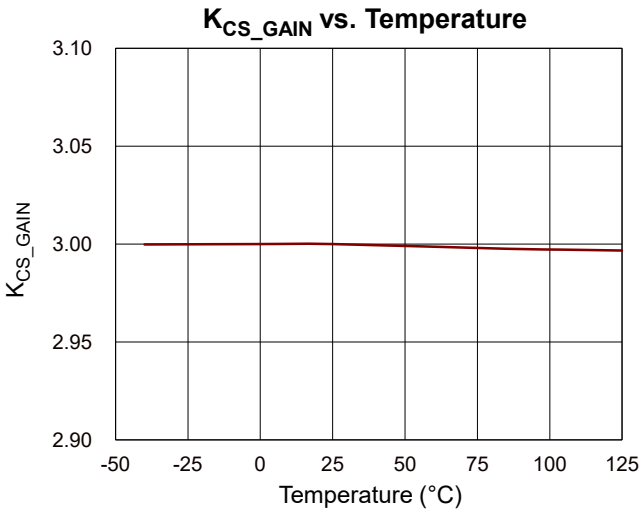


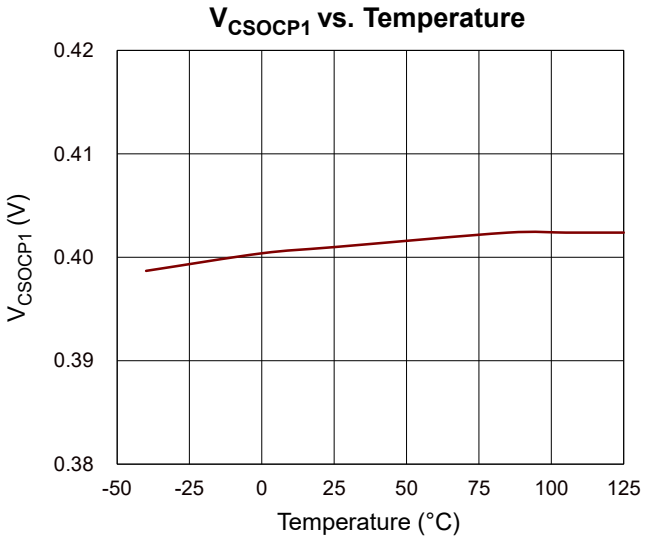


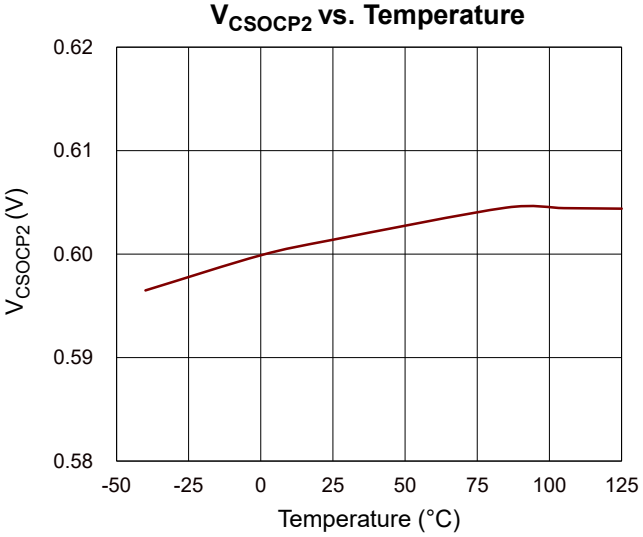


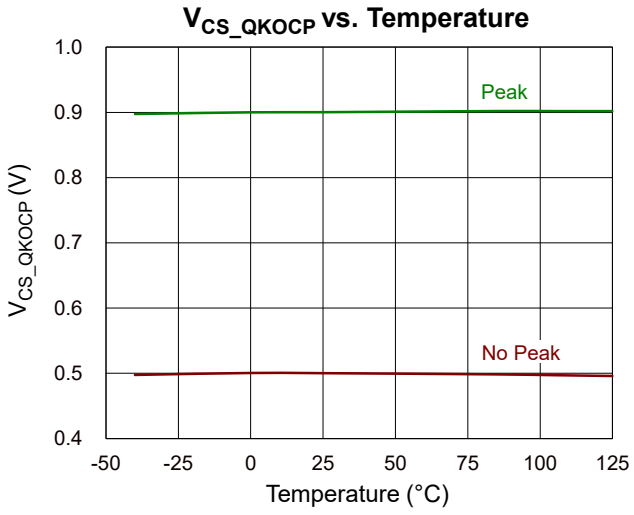


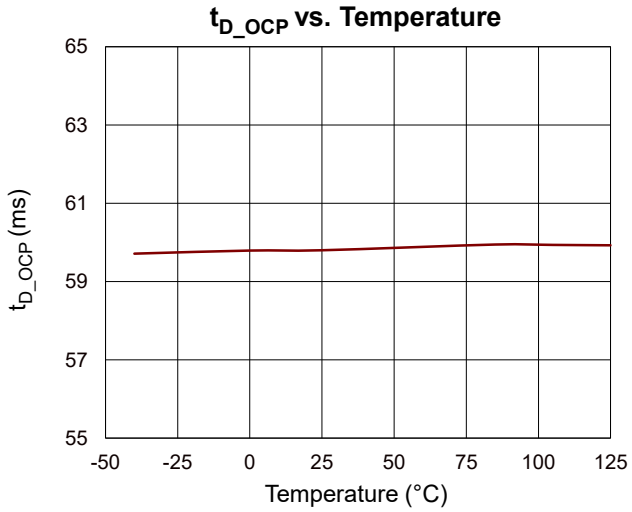


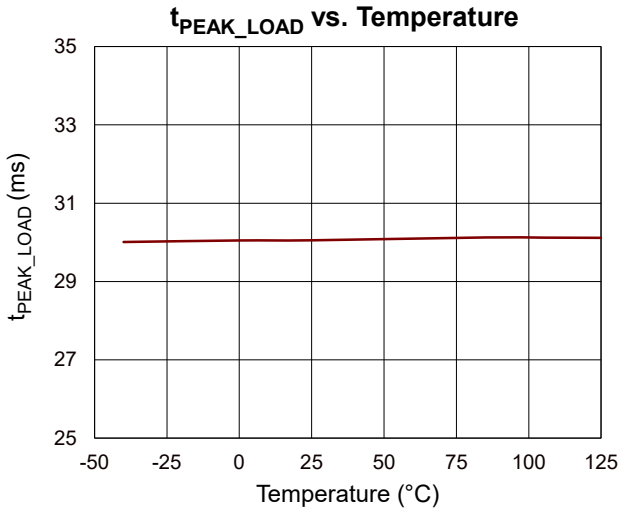


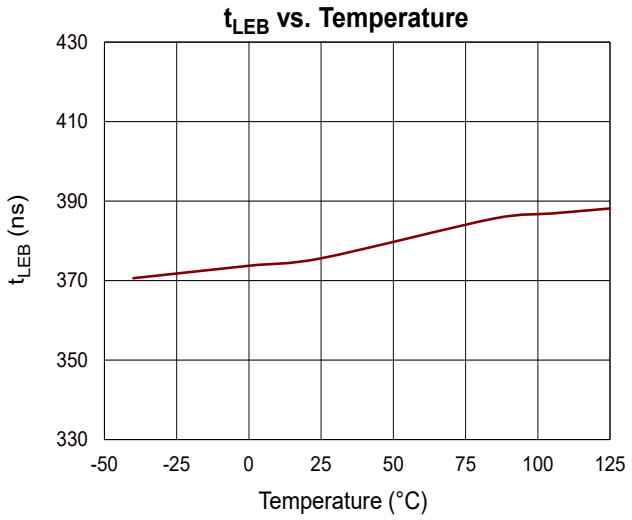


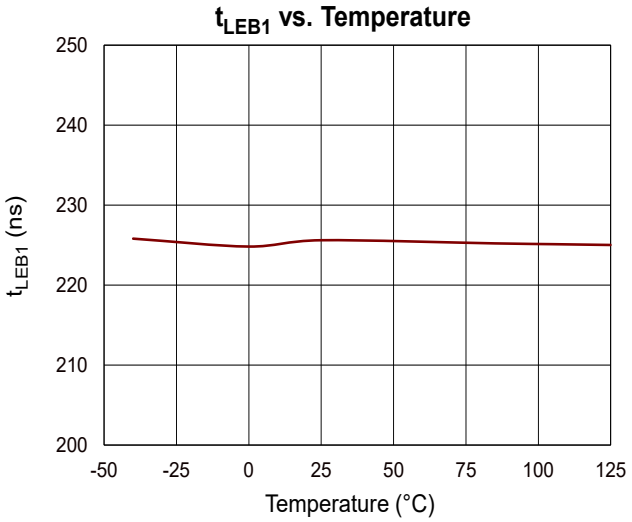


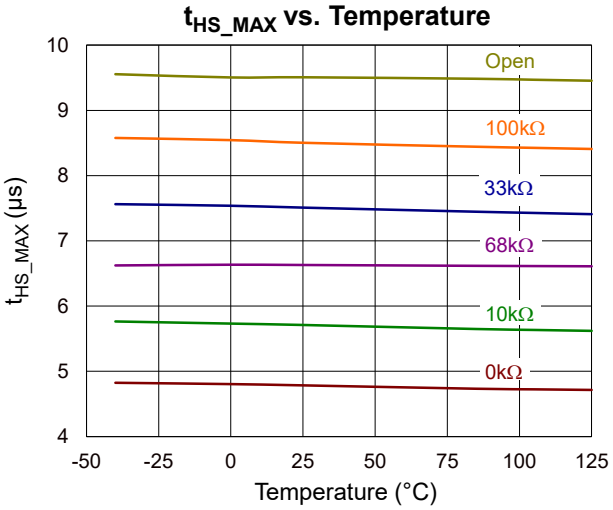


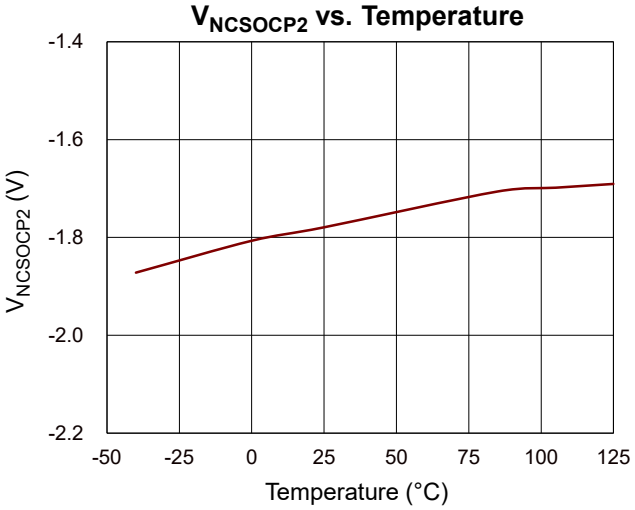


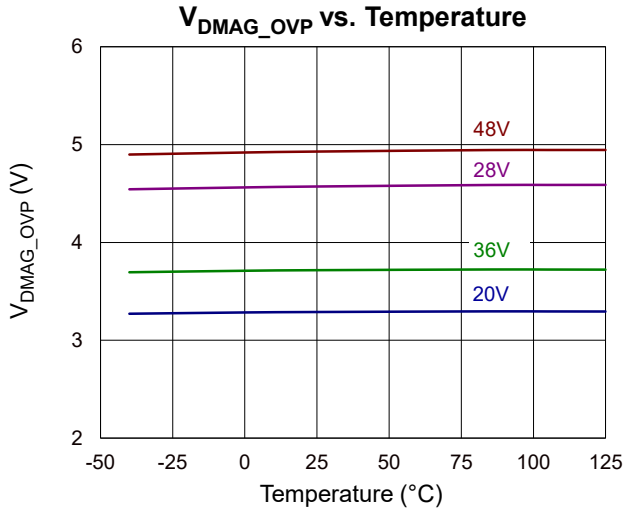


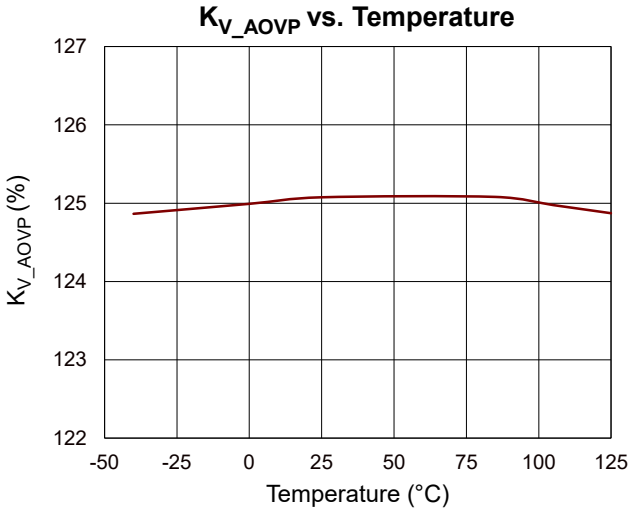


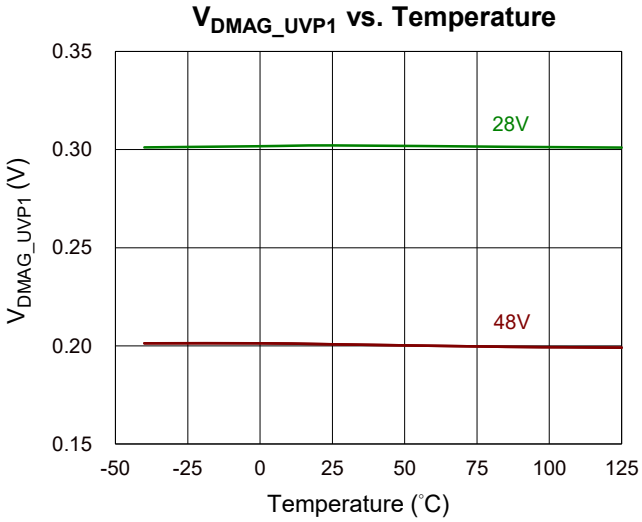


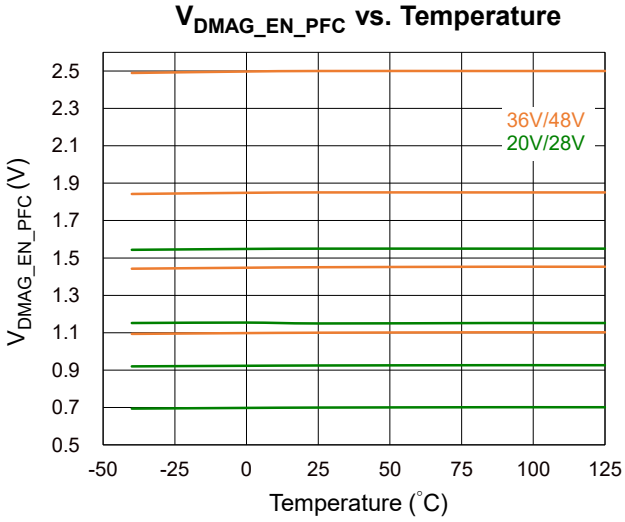


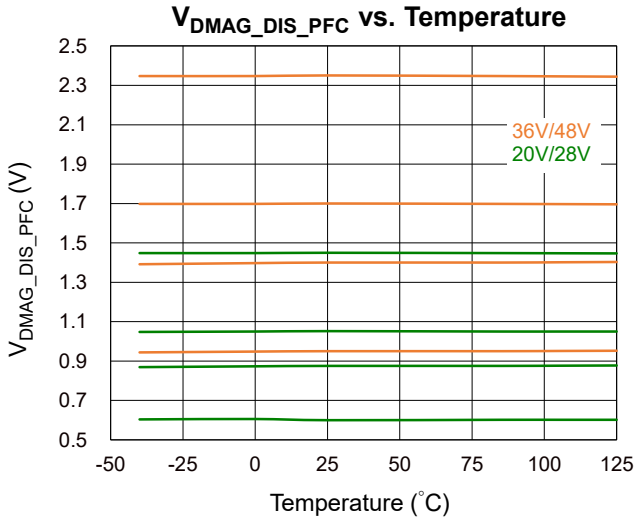


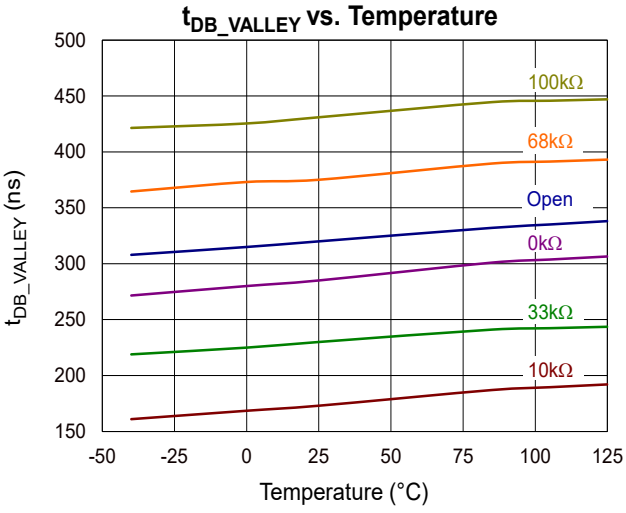


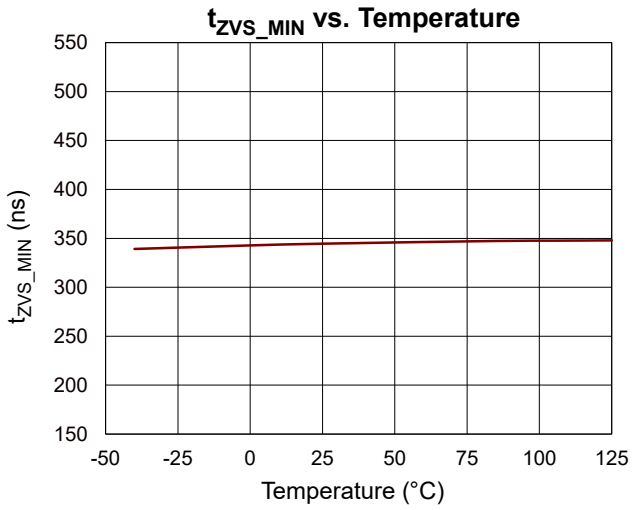


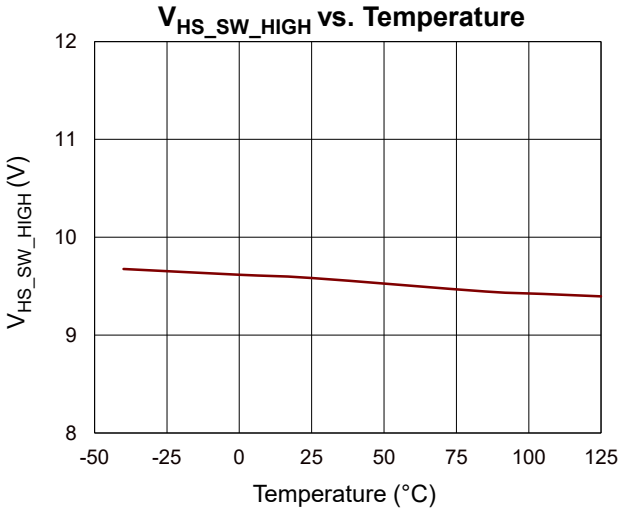


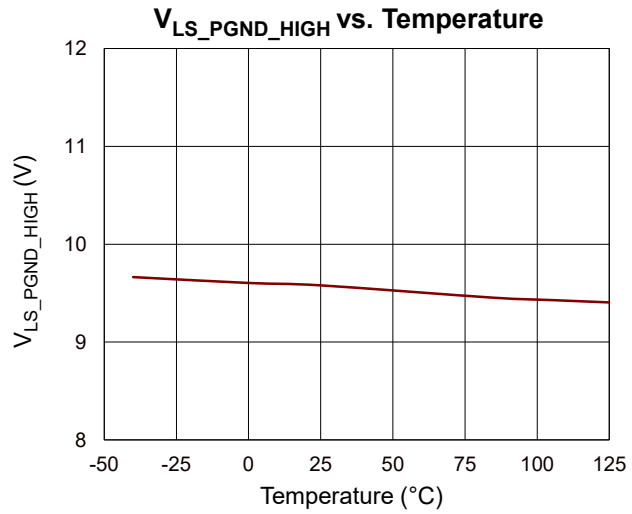


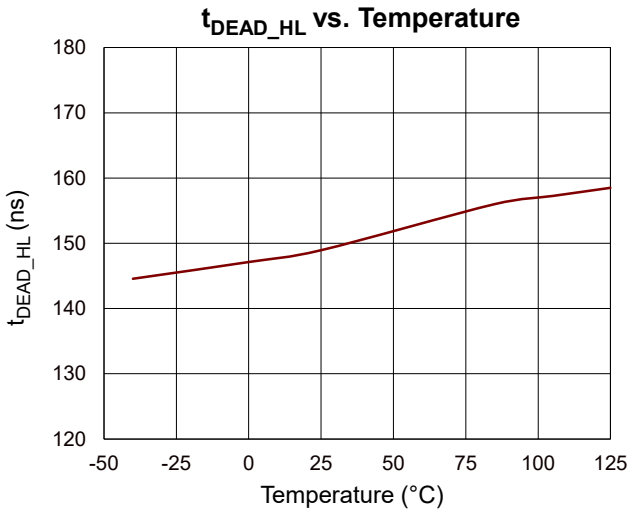


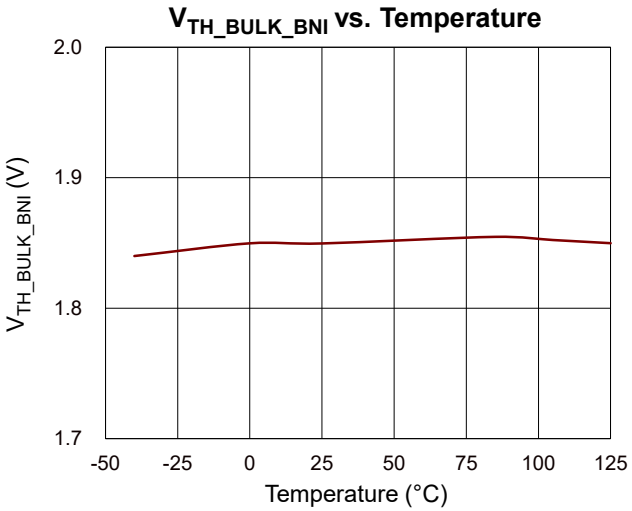


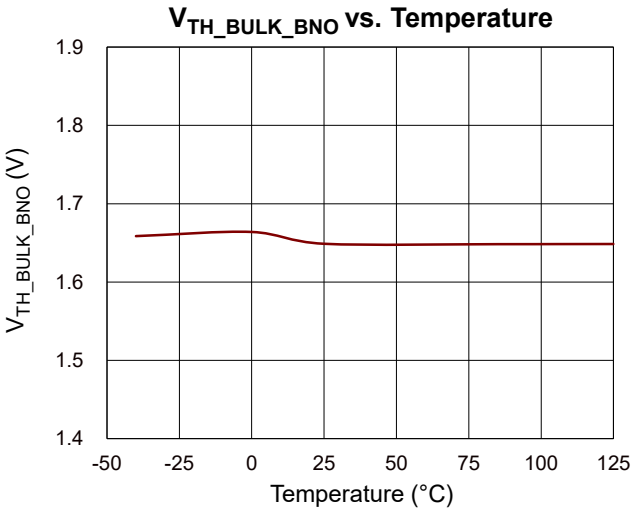


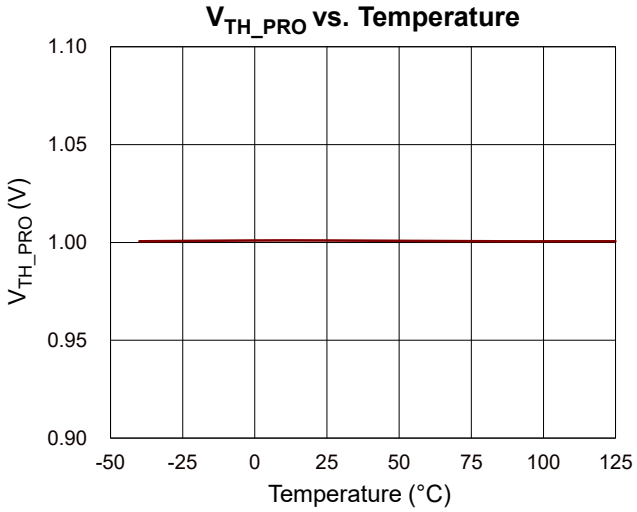


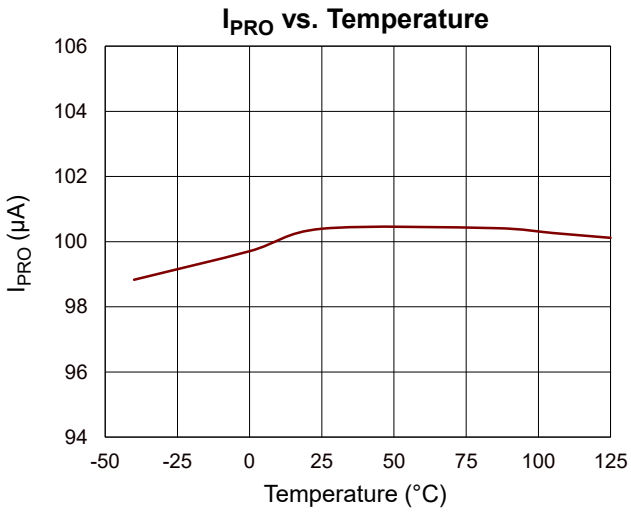












15 Operation

The RT7795ML serves as an AHB controller capable of accommodating a wide range of output voltages, making it well-suited for AC-DC power converters utilized in USB-PD EPR programmable power adapters. This controller boasts numerous innovative features and functionalities, including full-range ZVS on-time modulation control and positive/negative overcurrent protection.

15.1 Multi Operation Mode

The operation modes include: (1) Continuous Resonant Mode (CRM) and (2) Cycle-Skipping and Burst Mode for light-load and no-load conditions.

15.2 CRM Mode

In CRM, the HS on-time is determined by peak current mode control. The LS on-time is controlled based on the magnetizing and demagnetizing of the magnetizing inductance (L_M) of the transformer.

15.3 ZVS On-Time Modulation

To achieve Zero Voltage Switching (ZVS) for the HS MOSFET, it is necessary to discharge the Coss and parasitic capacitances during the dead time period. This can be accomplished by applying a negative magnetizing current, which generates a circulating current. To ensure ZVS, the on-time of the LS MOSFET must be generated appropriately. The waveform detected by the DMAGP and DMAGN pins is used to generate the LS on-time and achieve ZVS for the HS MOSFET.

15.4 Cycle-Skipping and Burst Mode

The operation mode transitions from Continuous Resonant Mode (CRM) to Cycle-Skipping and Burst Mode when the COMP voltage falls below the threshold V_{BURST_TH}.

15.5 Reduce Audio Noise

To minimize audio noise, the switching current is reduced during power converter operation within the audio band. Optionally, the switching frequency can be controlled to remain above 20kHz to 30kHz until the switching current decreases below a predefined low threshold.

15.6 ENPFC Light Load Control

When operating at high line with a light load, the PFC can be turned off using the ENPFC pin to comply with energy regulations. The input voltage is determined to be high line or low line through the HV pin, and the COMP voltage is used to determine whether the operation is at light load.

15.7 Demagnetization Sensing

Through the turn ratio N_{AS} (N_A / N_S) and a voltage divider, the DMAGP and DMAGN pins are differentially coupled to the auxiliary winding of the transformer. This setup allows the detection of N_{PS} (N_P/N_S) x V_O when the LS MOSFET is turned on and the sensing of V_{IN} - N_{PS} x Vo when the HS MOSFET is turned on. By adjusting the resistance of the voltage divider connected to the DMAGP and DMAGN pins, the RT7795ML can implement output overvoltage and undervoltage protections. In case the DMAGP and DMAGN pins are open-circuited or shorted, a fault condition is assumed, and the controller will cease operation within a few cycles.

15.8 VDD Hold-Up Mode

The VDD hold-up mode is employed to prevent the VDD voltage from falling below the turn-off threshold V_{TH_OFF} during dynamic loading conditions. However, it is important to note that the VDD hold-up mode consumes power

during burst mode operation. Therefore, if the power converter continues to operate in burst mode for an extended period, the VDD hold-up mode will be deactivated.

15.9 Overcurrent Protection

The RT7795ML incorporates cycle-by-cycle current-limit protection. This protection is activated when a fault condition persists beyond the overcurrent protection debounce time t_{D_OCP}.

15.10 Secondary Rectifier Short Protection (SRSP)

If a short circuit in the secondary rectifier is detected over a few switching cycles, the RT7795ML will shut down.

15.11 Resonant Negative Switching Current OCP

The LS switch will be disabled if the resonant negative switching current exceeds the OCP threshold.

16 Application Information

(Note 8)

The RT7795ML is an AHB PWM controller that includes CRM, Cycle-Skipping and Burst Mode operations. The RT7795ML can automatically switch among these control modes to optimize efficiency for the power converter operating under different load conditions.

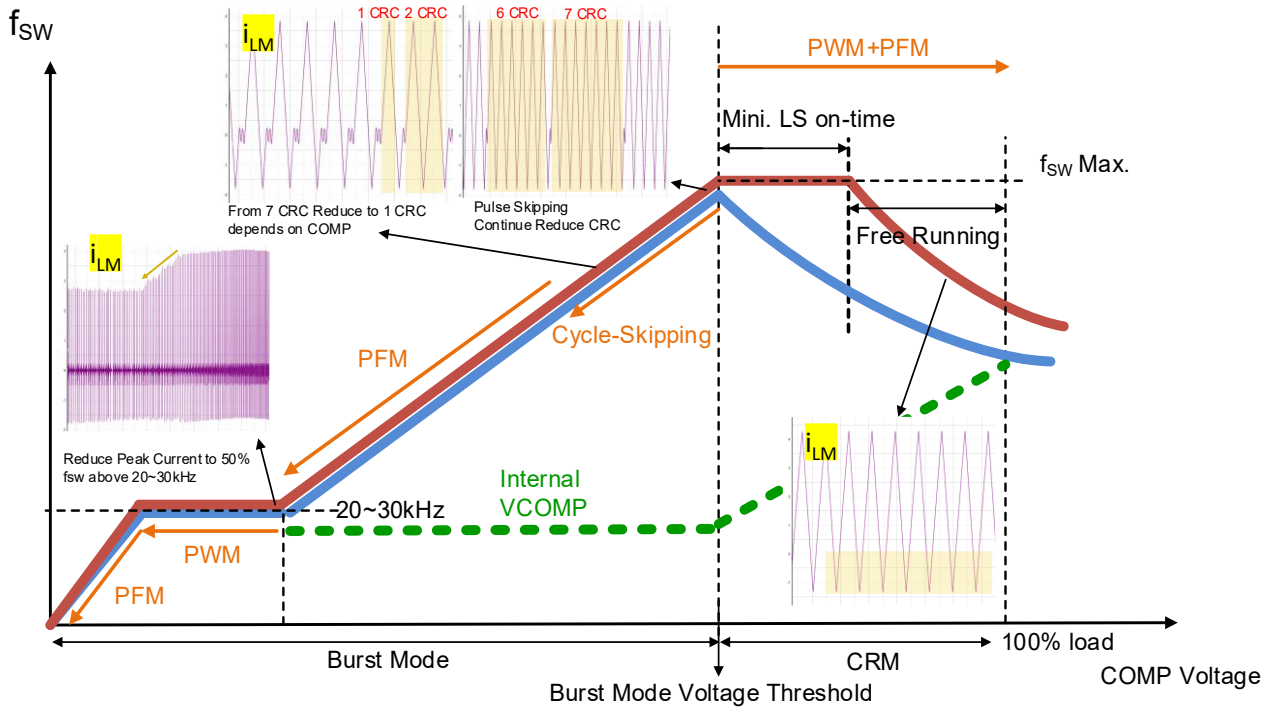


Figure 1. Operating Mode

16.1 Frequency Reducing (FR) Curve

The operation of the RT7795ML is illustrated by the FR Curve in Figure 1.

In CRM, the HS on-time is determined by peak current mode control, and the LS on-time is based on the control of the magnetizing inductance current (i_{LM}) operated under boundary conditions (where the current approaches approximately 0A). As the load decreases from full load (100%), the HS on-time and LS on-time decrease, causing the switching frequency to increase until it reaches a maximum frequency. This maximum frequency is limited by the LS minimum on-time set by the TLSMIN pin.

When the load continues to decrease and the COMP voltage falls below the burst mode voltage threshold, the operation mode switches to Cycle-Skipping and Burst Mode.

The Burst mode voltage threshold can be adjusted using the BMSEL pin.

During Cycle-Skipping operation, decreasing the load reduces the number of CRM cycles. The number of CRM cycles (CRC) can be decreased from 7 cycles to 1 cycle as part of cycle-skipping. When the CRC is reduced to 1 cycle, and the load keeps decreasing, the control transitions to pulse frequency modulation (PFM) operation. As the load continues to decrease, the switching frequency decreases, approaching 20kHz to 30kHz, and then it remains clamped in that range.

If the load further decreases, the control switches back to pulse width modulation (PWM) to reduce the peak current and minimize audio noise. After the primary peak current decreases to 50% and the load continues to

decrease, PFM operation is resumed.

16.2 HV Start-Up

The RT7795ML features an HV pin for rapid start-up. The controller incorporates a 625V start-up device to minimize power consumption. This start-up device activates during the start-up phase and deactivates during normal operation.

As depicted in Figure 2, a resistor R_{HV}, ranging from 2kΩ to 15kΩ, is recommended in series with the HV pin. If R_{HV} exceeds 15kΩ by a large margin, the accuracy of the brown-in and brown-out threshold will be compromised. The input voltage is sensed through a built-in resistive voltage divider.

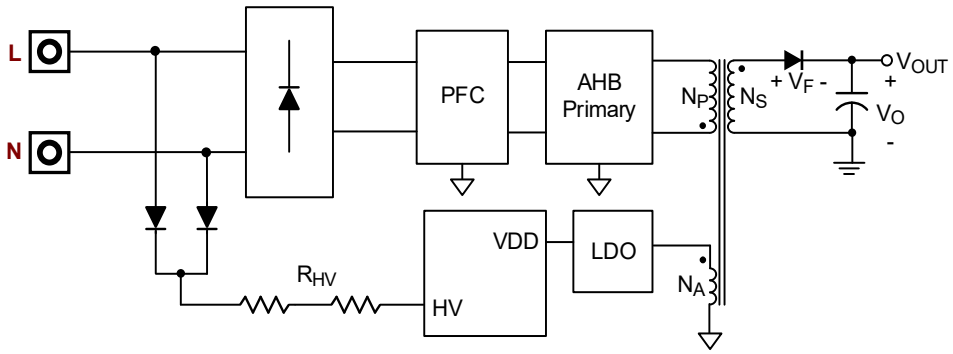


Figure 2. HV Start-Up Circuit

16.3 DMAG Pin Resistor

During the HS on-time, the auxiliary winding voltage is negative, causing the DMAGP and DMAGN pins to clamp the V_{DMAG} at 0V. When the LS turns on, the DMAGP and DMAGN pins sense the power converter's output voltage through the auxiliary winding, using a ratio equivalent to the turn ratio of the auxiliary and secondary windings. This sensed voltage is then scaled using the resistive divider R_{DMAG2}/R_{DMAG1}, as illustrated in Figure 3. You can calculate the voltage divider using the following equations.

$$\begin{cases} R_{DMAG2} = \dfrac{N_A}{N_S} \times \dfrac{1}{k_{V\_DMAG}} \times 8.03k\Omega,\ V_{O\_NOR\_MAX} = 36V,\ 48V \\ R_{DMAG2} = \dfrac{N_A}{N_S} \times \dfrac{1}{k_{V\_DMAG}} \times 12.8k\Omega,\ V_{O\_NOR\_MAX} = 20V,\ 28V \\ R_{DMAG1} = \dfrac{R_{DMAG2}}{\dfrac{N_{AS}}{k_{V\_DMAG}} - 1} \end{cases}$$

where N_{AS} is the output N_A / N_S.

The following is the calculation formula for I_{DMAG_SOURCE} current.

$$I_{DMAG\_SOURCE} = \frac{V_{IN\_MIN} - N_{PS} \times V_{OUT}}{R_{DMAG2}} X \frac{N_A}{N_P}$$

V_{IN_MIN}: The minimum input voltage

When designing, note that the I_{DMAG_SOURCE} current must be greater than the value below.

Especially when PFC is OFF, the output reaches its highest voltage, which is the worst case.

$I_{DMAG\_SOURCE} \geq 100\mu A$

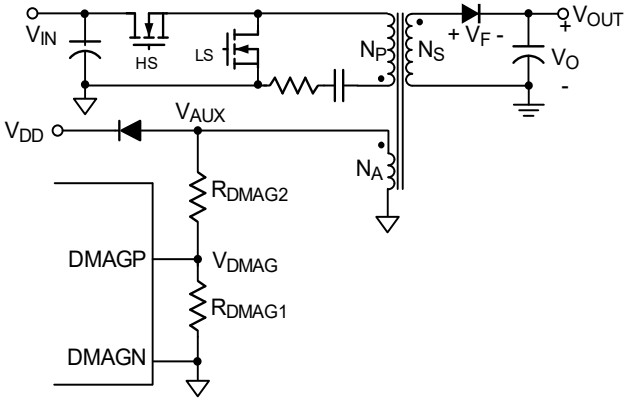


Figure 3. DMAGP and DMAGN Pin Resistor

16.4 BMSEL Setting

The RT7795ML features a BMSEL pin for configuring the Burst Mode threshold. The Burst Mode threshold affects the reduction in switching frequency, as depicted in Figure 4.

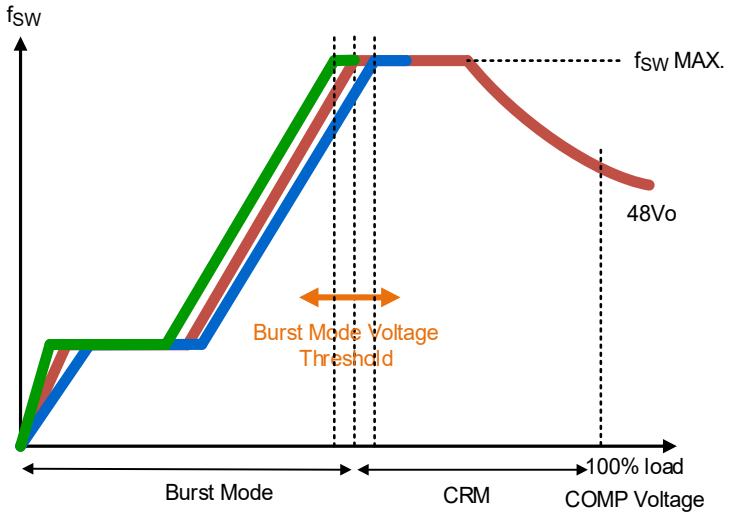


Figure 4. Burst Mode Threshold Setting

The burst mode voltage threshold equation:

$$V_{BURST\_TH} = V_{OFS\_COMP} + V_{OFS\_CLAMP} + K_{DMAGL} \times K_{V\_BST} \times V_{DMAG}$$

V_{OFS_CLAMP}: Defined by the setting of the BMSEL pin.

K_{V_BST}: A constant depends on different applications.

K_{DMAGL}: 0.7V/V, the voltage modulation ratio.

V_{DMAG}: V_{DMAGP} - V_{DMAGN} =V_O x K_{V_DMAG}.

16.5 MTHS Setting

The MTHS setting determines the maximum HS on-time. The design condition is based on the peak load is enabled (V_{CSOCP2}), peak load is disabled (V_{CSOCP1}), the minimum input voltage (V_{IN_MIN}), and the maximum output voltage ($V_{O\_NOR\_MAX}$).

The setting adjustment can be expressed using the following equation:

$$t_{MTHS} = \frac{V_{CSOCP1,2}}{R_{CS}} \times \frac{L_M}{\left(V_{IN\_MIN} - N_{PS} \times V_{O\_NOR\_MAX}\right)}$$

Assume t_{MTHS} = 7.3μs, which means the t_{MTHS} setting = 7.5μs. R_{MTHS} = 33kΩ.

The AHB primary peak current (I_{PEAK}) does not follow a linear pattern. The HS on-time must be restricted to a duration shorter than a quarter of the resonant period, as illustrated in Figure 5.

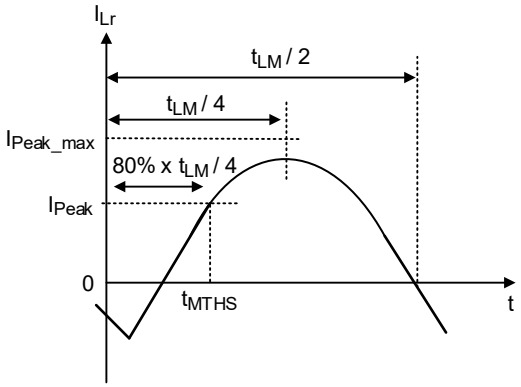


Figure 5. L_M and Cr Resonant Current Period

In Figure 5, the maximum on-time (maximum on-time) is constrained to be shorter than a quarter of the L_M Cr resonant period, allowing for a positive slope. It is recommended to use a quarter of the L_M Cr resonant period for linear operation. The maximum on-time (t_{LM_MTHS}) is calculated using the following equation:

$$\begin{cases} t_{LM} = 2\pi\sqrt{(L_M + L_R) \times C_R} \\ t_{LM\_MTHS} = \dfrac{80\% \times 2\pi\sqrt{(L_M + L_R) \times C_R}}{4} \end{cases}$$

It is necessary to check that $t_{LM\_MTHS} > t_{MTHS}$ to avoid peak current operation in a nonlinear pattern.

16.6 TLSMIN Setting

The TLSMIN setting determines the minimum LS on-time, which in turn affects the highest achievable switching frequency (f_{SW_MAX}, excluding dead time), as demonstrated in Figure 6. When the COMP voltage decreases, the LS on-time decreases to its minimum, keeping the FR curve at a fixed switching frequency.

The highest switching frequency, f_{SW_MAX}, is designed for $V_{O\_NOR\_MAX}$. The ZVS on-time modulation is constrained by the LS minimum on-time (LS minimum on-time). Users have the flexibility to adjust the minimum LS on-time via the TLSMIN setting pin. This adjustment can be expressed using the following equation:

$$R_{TLSMIN} = \left(1 - \frac{N_{PS} \times V_{O\_MAX}}{V_{IN\_MAX}}\right) \times \frac{1}{f_{SW\_MAX}} \times (2.665 \times V_O + 156) \times 10^8,\ V_{O\_NOR\_MAX} = 20V,\ 28V,\ 36V,\ 48V$$

The minimum LS on-time (t_{TLSMIN}) can be calculated using the following equations:

$$t_{TLSMIN} = 3.52 \times 10^{-11} \times R_{TLSMIN},\ V_{O\_NOR\_MAX} = 48V$$

$$t_{TLSMIN} = 3.97 \times 10^{-11} \times R_{TLSMIN},\ V_{O\_NOR\_MAX} = 36V$$

$$t_{TLSMIN} = 4.33 \times 10^{-11} \times R_{TLSMIN},\ V_{O\_NOR\_MAX} = 28V$$

$$t_{TLSMIN} = 4.78 \times 10^{-11} \times R_{TLSMIN},\ V_{O\_NOR\_MAX} = 20V$$

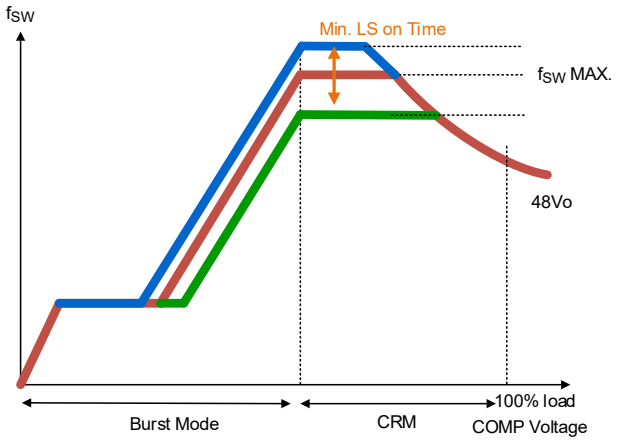


Figure 6. TLSMIN Setting Pin vs. FR Curve

16.7 RZVS Setting

The RT7795ML offers a ZVS function to reduce switching losses and enhance efficiency. During the dead time period, the ZVS function discharges the negative magnetizing inductance current (i_{LM}) through the HS MOSFET's Coss. To achieve ZVS, the LS on-time needs to be extended to ensure a negative i_{LM}. The control of the LS on-time is governed by the ZVS detection through the DMAGP and DMAGN pins. If the HS MOSFET fails to attain ZVS, the LS on-time will be increased.

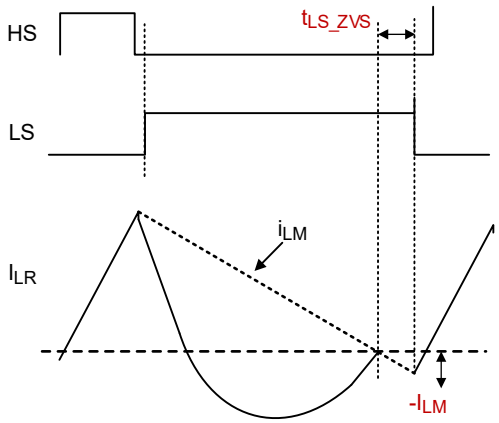


Figure 7. Negative Magnetic Current and t_{LS_ZVS}

The V_{IN}, N_{PS} x V_O, L_M, C_{SW}, and -i_{LM} could affect ZVS, as shown in Figure 7.The -i_{LM} can be controlled by t_{LS_ZVS} to achieve HS ZVS.

C_{SW}: Transformer parasitic Cap. shunt 2 x Coss Cap.

The R_{ZVS} resistor can be calculated using the following equations:

$$R_{ZVS} = \sqrt{L_M \times C_{SW}} \times \frac{R_{DMAG2} \times R_{DMAG1}}{(R_{DMAG2} + R_{DMAG1})} \times 3.889 \times 10^7,\ V_{O\_NOR\_MAX} = 36V,\ 48V$$

$$R_{ZVS} = \sqrt{L_M \times C_{SW}} \times \frac{R_{DMAG2} \times R_{DMAG1}}{(R_{DMAG2} + R_{DMAG1})} \times 2.431 \times 10^6,\ V_{O\_NOR\_MAX} = 20V,\ 28V$$

The t_{LS_ZVS} can be calculated using the following equations:

$$t_{LS\_ZVS} = 3.025 \times 10^{-7} \times \frac{(V_{IN} - N_{PS} \times V_O) \times R_{ZVS}}{N_{PA} \times V_O \times R_{DMAG2}},\ V_{O\_NOR\_MAX} = 20V,\ 28V,\ 36V,\ 48V$$

N_{PA}: N_P / N_A

16.8 TVPSEL Setting

The RT7795ML detects the valley signal through the DMAGP and DMAGN pins. The valley signal triggers when the VDMAG resonant ring drops below 0.1V after the delay time t_{TVPSEL}, which is set by the TVPSEL setting pin, as illustrated in Figure 8. The TVPSEL setting significantly impacts the HS MOSFET ZVS and dead time.

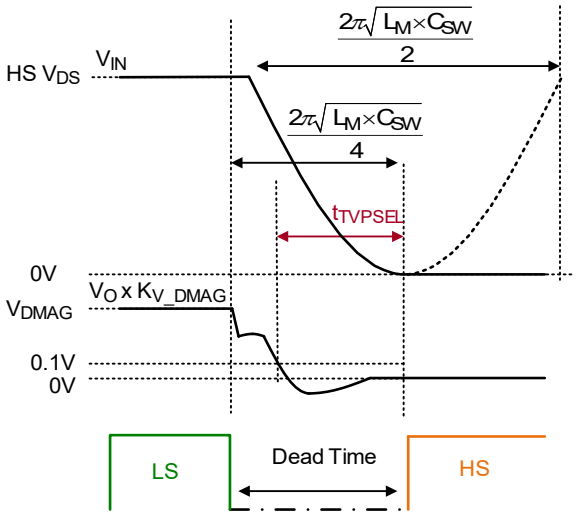


Figure 8. V_{DMAG} Drop

Figure 8 displays the V_{DMAG} voltage waveform, which is closely related to L_M and C_{SW}. The TVPSEL setting is determined by the resonant period of L_M and C_{SW}. When the V_{DMAG} voltage falls from V_O x K_{V_DMAG} to 0V, it indicates the achievement of HS ZVS. The t_{TVPSEL} equation is:

$$t_{TVPSEL} \geq \frac{2\pi \times \sqrt{L_M \times C_{SW}}}{4} \times 60\%$$

Assume t_{TVPSEL} = 250ns, and the setting pin resistor is 0Ω. Choosing a t_{TVPSEL} much longer than the calculated value will cause lower efficiency.

16.9 Resonant Negative Switching Current OCP

Figure 9 (a) and Figure 10 show that i_{LR1} represents the negative resonant current during normal operation. When the output load is short-circuited or during the power-on/off period, as depicted in Figure 9 (b) and Figure 10, the i_{LR2} current may become significantly high.

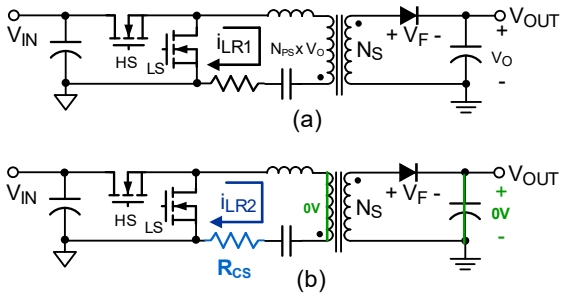


Figure 9. (a) Normal Operation (b) Output Short

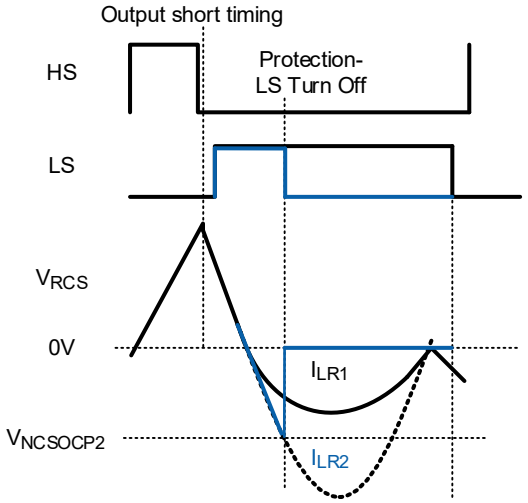


Figure 10. Resonant Negative Current Diagram

It can be expressed by the following equation:

$$i_{LR}(t) = \frac{N_{PS} \times V_O - Vcr\ (t_1)}{Z}$$

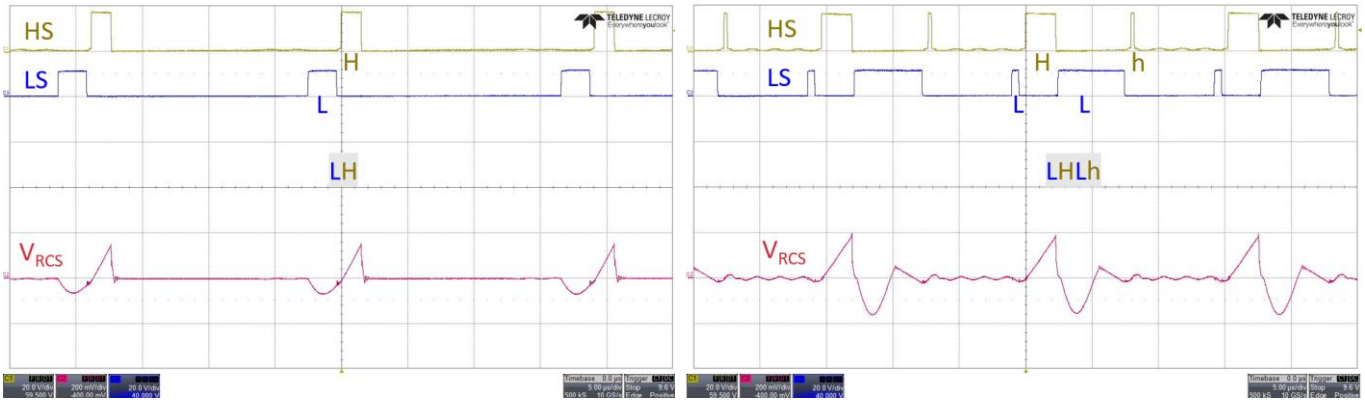
Z: Primary-side equivalent impedance.

Vcr: Resonant Cap. voltage.

When V_O is approximately 0V, i_{LR} will experience a substantial discharge current. As depicted in Figure 10, the negative resonant current protection, detected by V_{RCS}, will promptly initiate the turn-off of the LS MOSFET to safeguard the power converter.

16.10 LH Mode and LHLh Mode

LH mode, shown in Figure 11 (a), operates at low output voltage and light load to achieve better efficiency. LHLh mode, shown in Figure 11 (b), operates at higher output voltage and light load to achieve better efficiency. Mode change depends on V_{DMAG} V_O detection. The mode change threshold output voltage can be referenced by $V_{DMAG\_EN\_PFC}$ and $V_{DMAG\_DIS\_PFC}$. When $V_{DMAG} > V_{DMAG\_EN\_PFC}$, the mode changes from LH mode to LHLh mode. When $V_{DMAG} < V_{DMAG\_DIS\_PFC}$, the mode changes from LHLh mode to LH mode.



(a) (b)

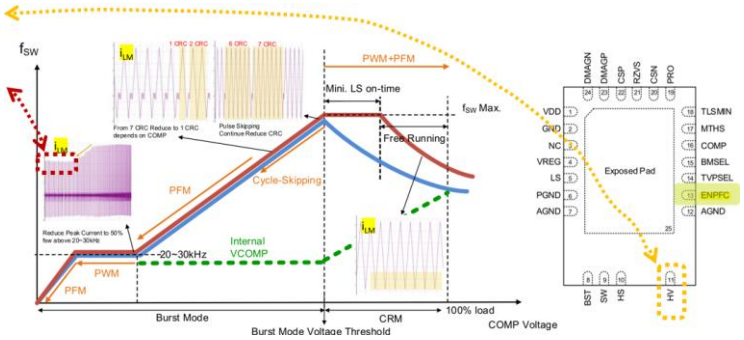
Figure 11. (a) LH Mode (b) LHLh Mode

16.11 ENPFC Light Load Control

Basic PFC control is as follows: when $V_{DMAG} < V_{DMAG\_DIS\_PFC}$, the PFC is OFF; when $V_{DMAG} > V_{DMAG\_DIS\_PFC}$ the PFC is ON. ENPFC light load control is added. When operating at high line with a light load, the PFC can be turned off using the ENPFC pin to comply with energy regulations. The input voltage is determined to be high line or low line through the HV pin, and the COMP voltage is used to determine whether the operation is at light load.

Output Voltage	115Vac		230Vac	
	Heavy Load	Light Load	Heavy Load	Light Load
5Vo	PFC OFF	PFC OFF	PFC OFF	PFC OFF
9Vo	PFC OFF	PFC OFF	PFC OFF	PFC OFF
15Vo	PFC OFF	PFC OFF	PFC OFF	PFC OFF
20Vo	PFC ON	PFC ON	PFC ON	PFC OFF
28Vo	PFC ON	PFC ON	PFC ON	PFC OFF
36Vo	PFC ON	PFC ON	PFC ON	PFC OFF
48Vo	PFC ON	PFC ON	PFC ON	PFC OFF

(a)



(b)

Figure 12. (a) ENPFC Truth Table (b) ENPFC Function Judgement by COMP and HV Voltage

16.12 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x6 package, the thermal resistance, θ_{JA}, is 44.58°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (44.58°C/W) = 2.24W for a WQFN-24L 4x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 13 allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

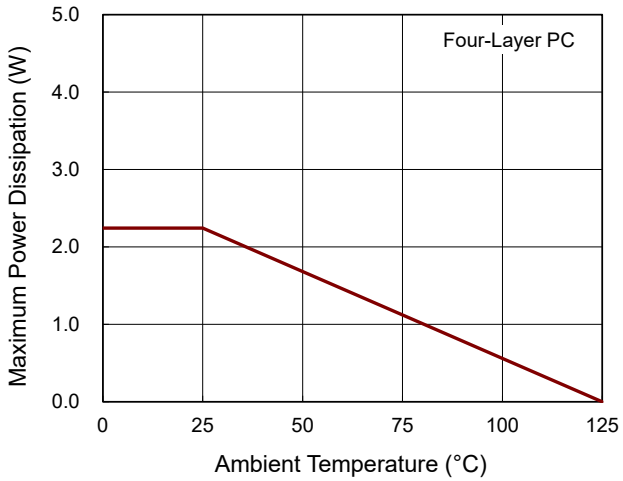


Figure 13. Derating Curve of Maximum Power Dissipation

16.13 Layout Considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch-mode power supply (SMPS). It is recommended to follow the following PCB layout guidelines as Figure 14, when designing a switch-mode power supply.

- Current path (1): Starting from the bulk capacitor, through the HS MOSFET, the transformer, the Cr, the resistor R_{CS}, and back to the bulk capacitor, is a high-frequency and high-current loop. Another high-frequency and high-current loop is the current path (2) which is from the GATE pin, through the HS MOSFET, and back to the SW pin. These two paths should be kept as small as possible to decrease noise coupling and kept away from other low-voltage traces, such as IC control circuit paths.
- Current path (3): Starting from the LS MOSFET, through the transformer, the Cr, the resistor R_{CS} and back to the bulk capacitor ground, is a high-frequency and high-current loop. Another high-frequency and high-current loop is the current path (4), which is from the LS GATE pin, through the LS MOSFET, and back to the PGND pin. These two paths should be kept as small as possible to decrease noise coupling and kept away from other low-voltage traces, such as IC control circuit paths.
- Path (5): Starting from the auxiliary winding, through the diode, the resistor, and the VDD capacitor to the VDD pin, is also recommended to be as short as possible.

  Besides, the VDD capacitor should be placed as close to the VDD pin as possible.

- Ground traces: The ground traces of the bulk capacitor (a), the LS MOSFET (b), the VDD capacitor (c), the auxiliary winding (d), and the IC control circuit (e) should be separated to reduce noise, output ripple and EMI emission. The ground traces of the auxiliary winding (d) and the IC control circuit (e) are connected together at the VDD capacitor ground (c). Then the connected ground trace goes through the VDD capacitor ground (c), the MOSFET ground (b), and to the bulk capacitor ground (a) in turn. The area of the bulk capacitor ground trace should be large enough.
- Bypass capacitor: The bypass capacitor should be placed as close to the controller as possible.
- Trace length: To reduce the reflected trace inductance and EMI emissions, the trace connecting the secondary winding, the output diode, and the output filter capacitor should be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to ease sinking heat from the diode.

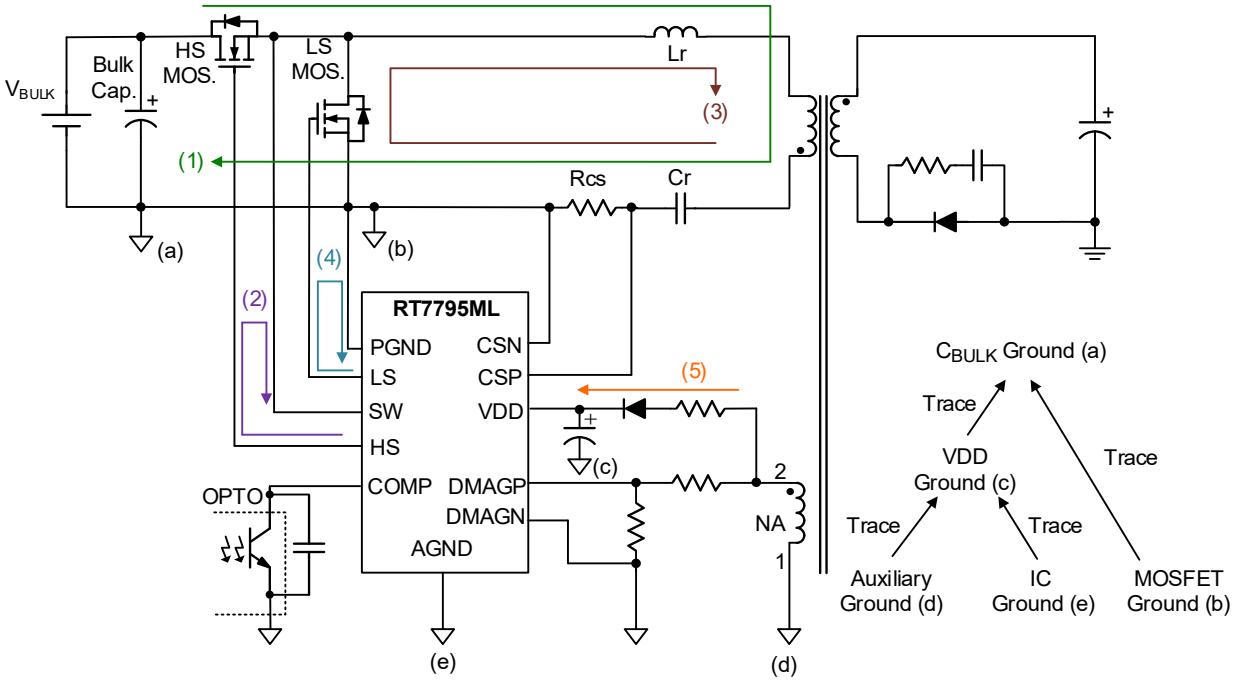
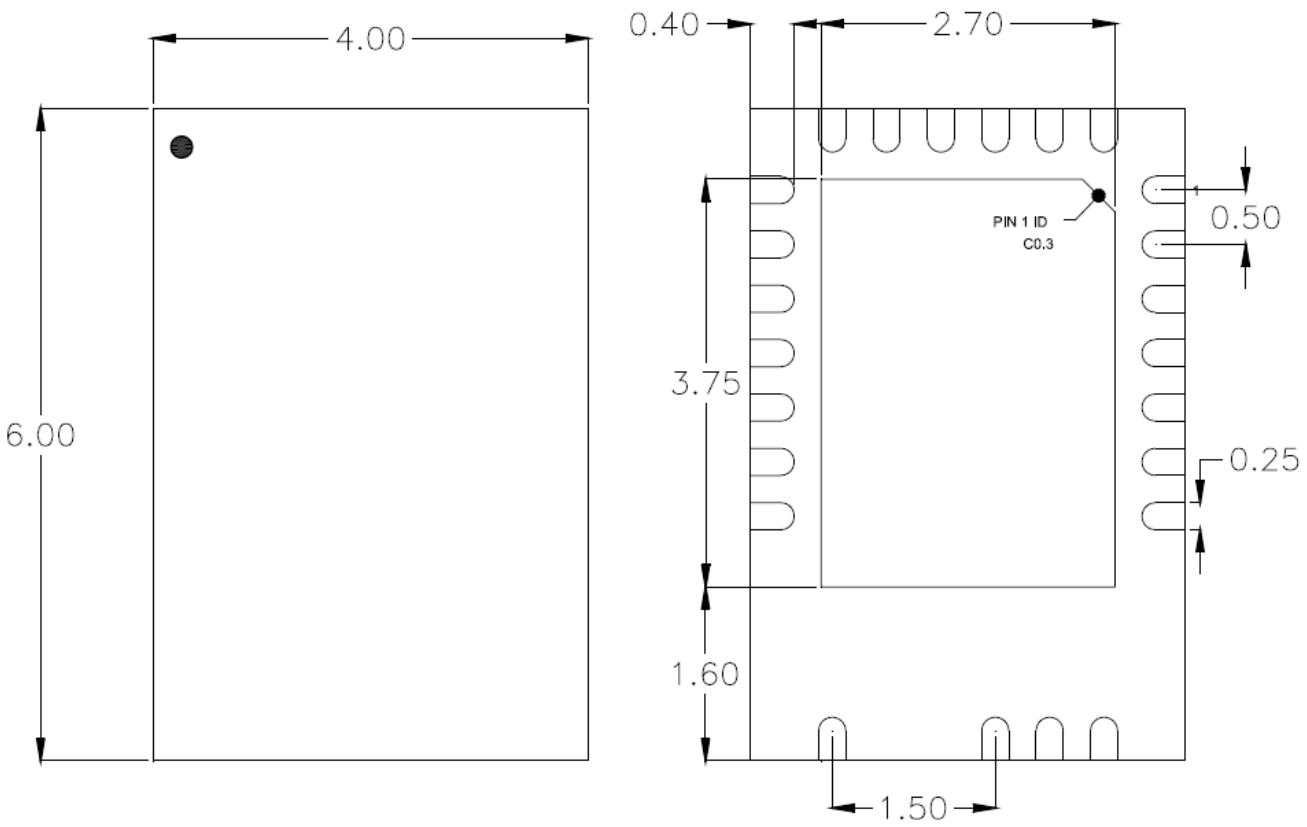
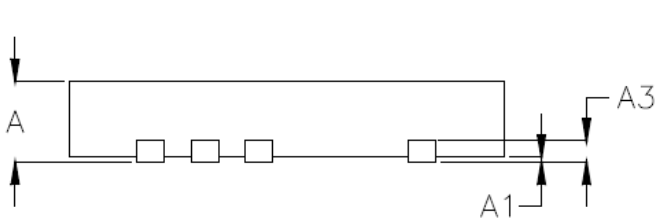


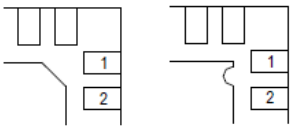
Figure 14. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension







DETAIL A

Pin #1 ID and Tie Bar Mark Options

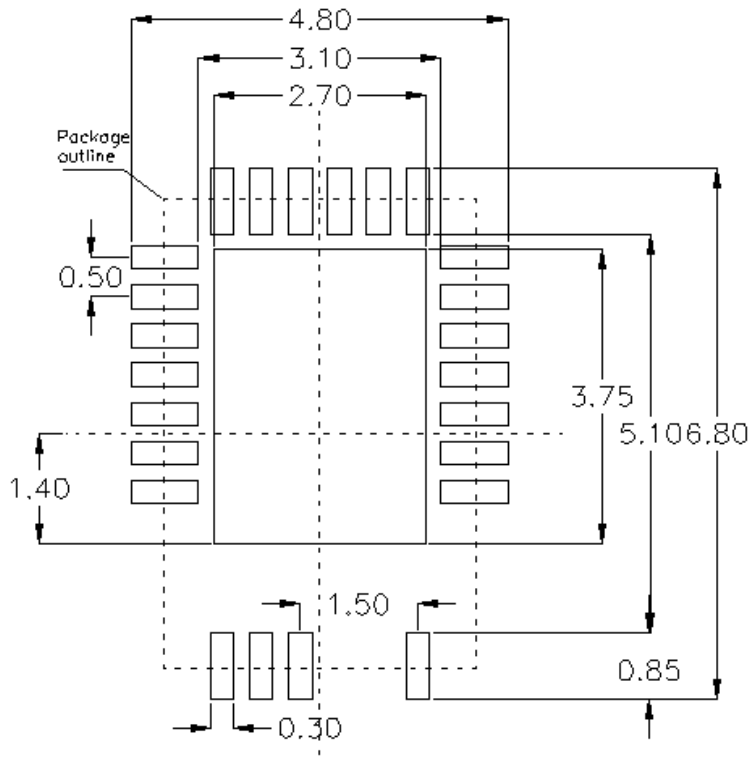
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050 mm

W-Type 24L QFN 4x6 Package

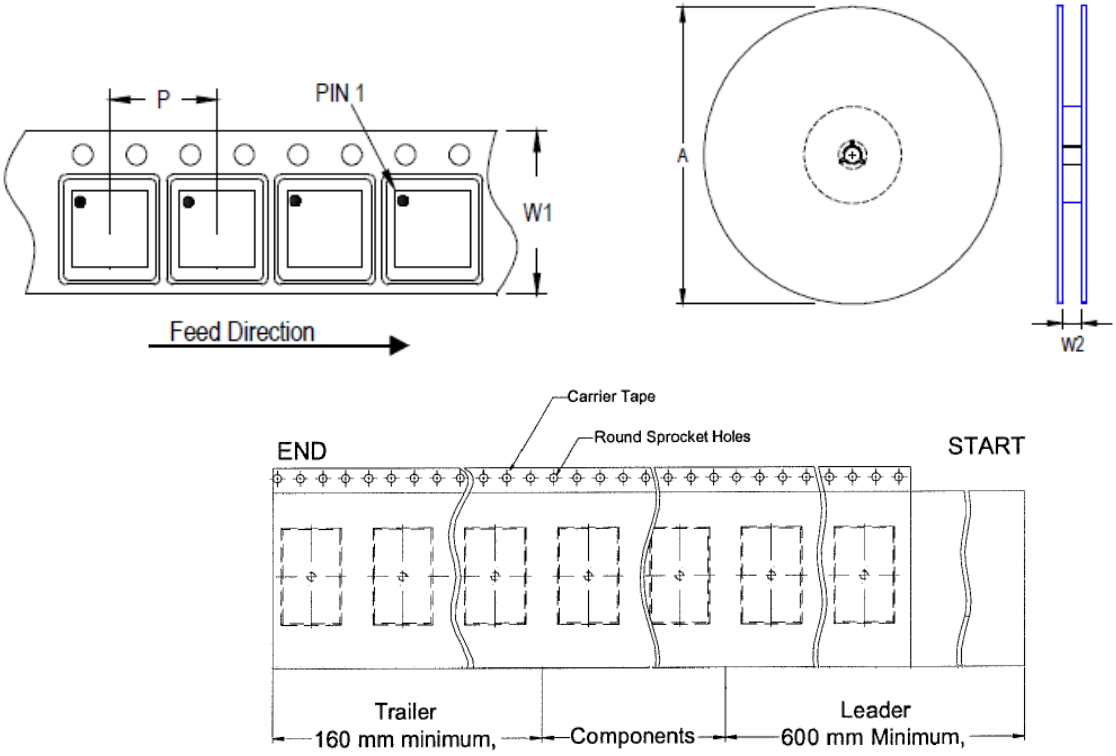
18 Footprint Information



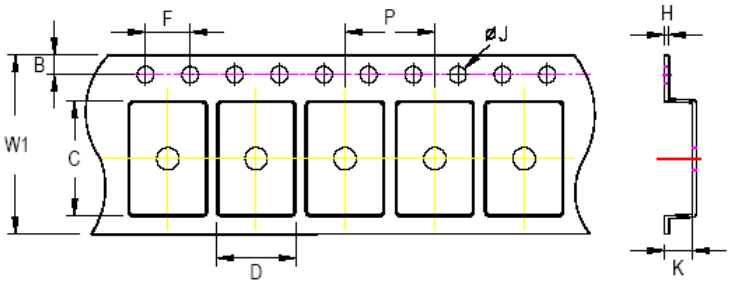
Package	Number of Pins	Tolerance (mm)
V/W/U/XQFN4x6-24	24	±0.05

19 Packing Information

19.1 Tape and Reel Data



Package Type	WPKG (mg)	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
				(mm)	(in)				
(V, W) QFN/DFN 4x6	55.4	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 4x6	13”	2,500	Box G	1	2,500	Carton A	6	15,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

20 Datasheet Revision History

Version	Date	Description
00	2025/5/8	First Edition
01	2026/8/21	Product Selection Table - Changed the option of product number RT7795MLN-AHMA to B/D - Changed the option of product number RT7795MLN-GHMA to B/D - Deleted item Adaptive OVP - Added product number RT7795MLN-LHQA, RT7795MLN-AHPA, RT7795MLN-AGNA, RT7795MLN-AQMA, RT7795MLN-AFHA, RT7795MLN-GFAA, RT7795MLN-AQAA, and RT7795MLN-LEQA Marking Information - Added product number RT7795MLN-LHQA, RT7795MLN-AHPA, RT7795MLN-AGNA, RT7795MLN-AQMA, RT7795MLN-AFHA, RT7795MLN-GFAA, RT7795MLN-AQAA, and RT7795MLN-LEQA Simplified Application Circuit Typical Application Circuit - Updated Electrical Characteristics Parameter Threshold Voltage of HV Brown-In - Added RT7795MLN-AGNA/AQMA for 83Vac - Added RT7795MLN-LHQA/AFHA/AQAA/LEQA to 70Vac Parameter Threshold Voltage of HV Brown-Out - Added RT7795MLN-AGNA/AQMA for 75Vac - Changed default value to 70Vac - Added RT7795MLN-LHQA/AFHA/AQAA/LEQA to 62Vac Parameter DMAG Threshold Voltage for Enabling a PFC Controller Parameter DMAG Threshold Voltage for Disabling a PFC Controller Parameter Offset Voltage used in V_{BURST_TH} - Updated HV Start-Up - Modified resistor R_{HV} range value Tape and Reel Data - Added WPKG