AnyPower™ and PDsafe™ USB Type-C PD Controller

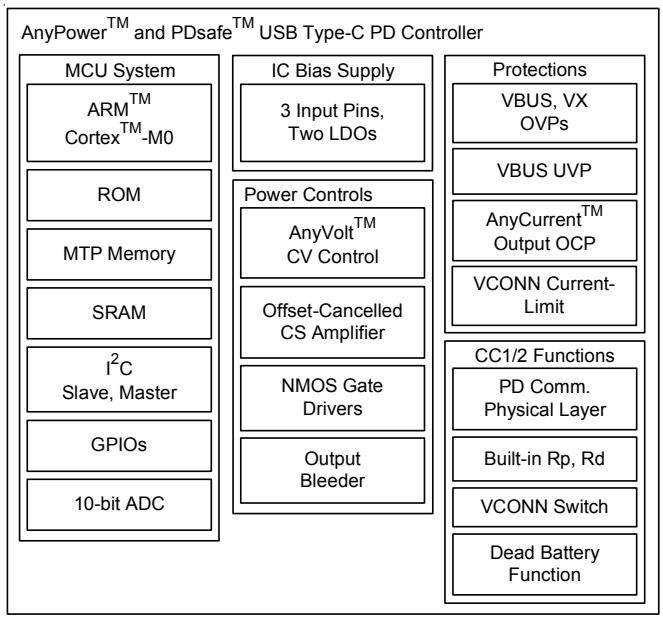
General Description

The RT7800B is a USB Power Delivery (USB PD) controller with highly integrated functions for notebook, tablet, mobile phone or any other devices with USB Type-C (USB-C) receptacle. It is designed to embed ARM Cortex™-M0 MCU so as to facilitate various functions of communication protocol, protections and customized requirements. The IC allows designer to define a USB-C port as a Provider, Consumer or a Dual Role Port by program setup.

Applications

- Notebook PC, Tablet PC, Smart Phone
- Desktop PC, LCD Monitor, TV, Docking Station
- Car Charger, Power Bank
- Portable Hard Disk, Dongle, Hubs

Simplified Block Diagram



Marking Information

RT7800BGQW : Product Number

YMDNN : Date Code

Features

- **AnyPower™ = AnyVolt™ + AnyCurrent™**
- **AnyVolt™ (50mV/step) Output Voltage Adjustment for USB Cable Bus Power (V_{BUS})**
- **Support Internet Online Firmware Updates**
- **AnyCurrent™ OCP for USB-C VBUS Output**
- **Cable Voltage Drop Compensation (CDC) for V_{BUS}**
- **Support Provider, Consumer and Dual Role Compliant with USB Power Delivery 3.0 Specification**
- **High Integration :**
  - **ARM M0 MCU for PD Protocol, Policy Engine and Device Policy Manager; Two I^2C Interfaces**
  - **Built-in Rp, Rd and BMC Physical Layer**
  - **GPIOs for MUX Control and Customized Functions**
  - **Automatic IC Bias Input Selection**
  - **Standard Compliance Quick Discharge for V_{BUS}**
  - **Support Dead Battery Function**
  - **Support USB Plug Power (V_{CONN})**
  - **4 Built-in Charge Pump NMOS Gate Drivers**
- **PDsafe™ :**
  - **OVP Detections at VBUS and VX Pins**
  - **UVP Detection at VBUS Pin**
  - **Current Limit for VCONN1/2 Output**
  - **Maximum Rating, 22V for CC1 and CC2 Pins**

Ordering Information

RT7800B□□

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

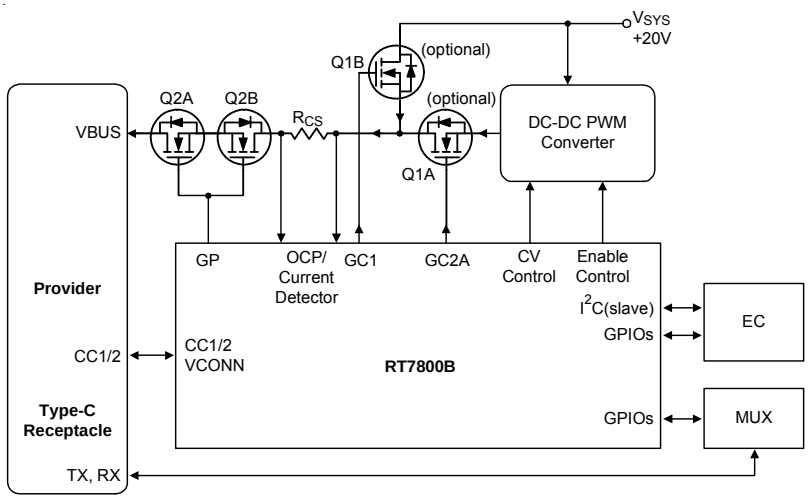
Note :

Richtek products are :

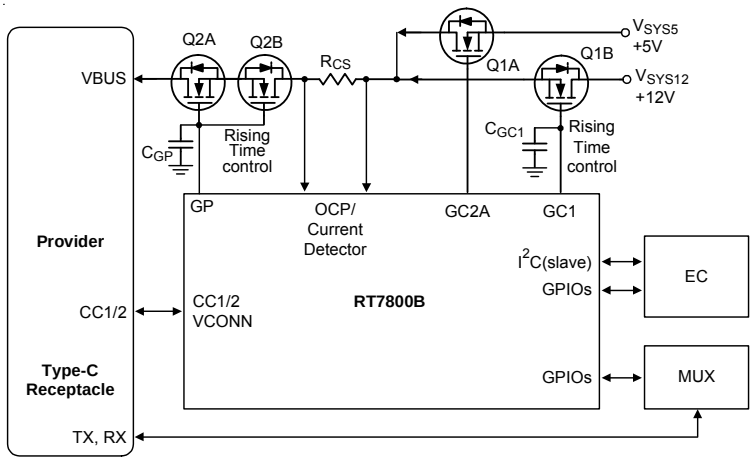
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit

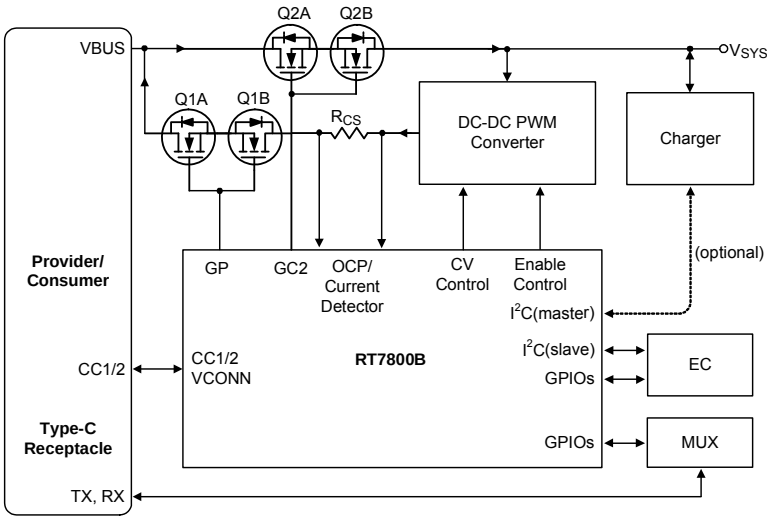
(1) Provider Application with a DC-DC Converter



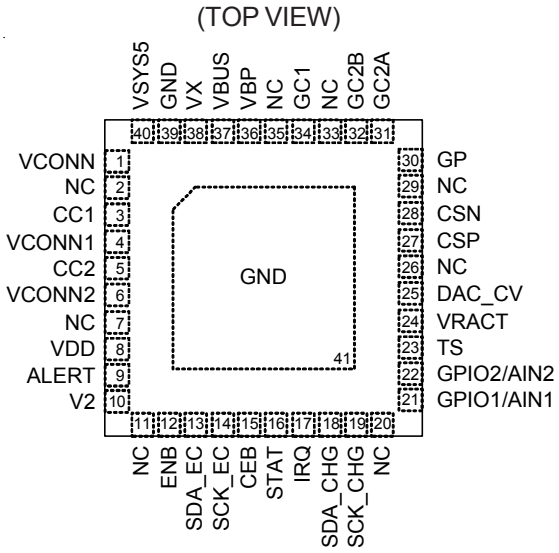
(2) Provider Application without a DC-DC Converter



(3) Dual Role Application with a DC-DC Converter



Pin Configuration



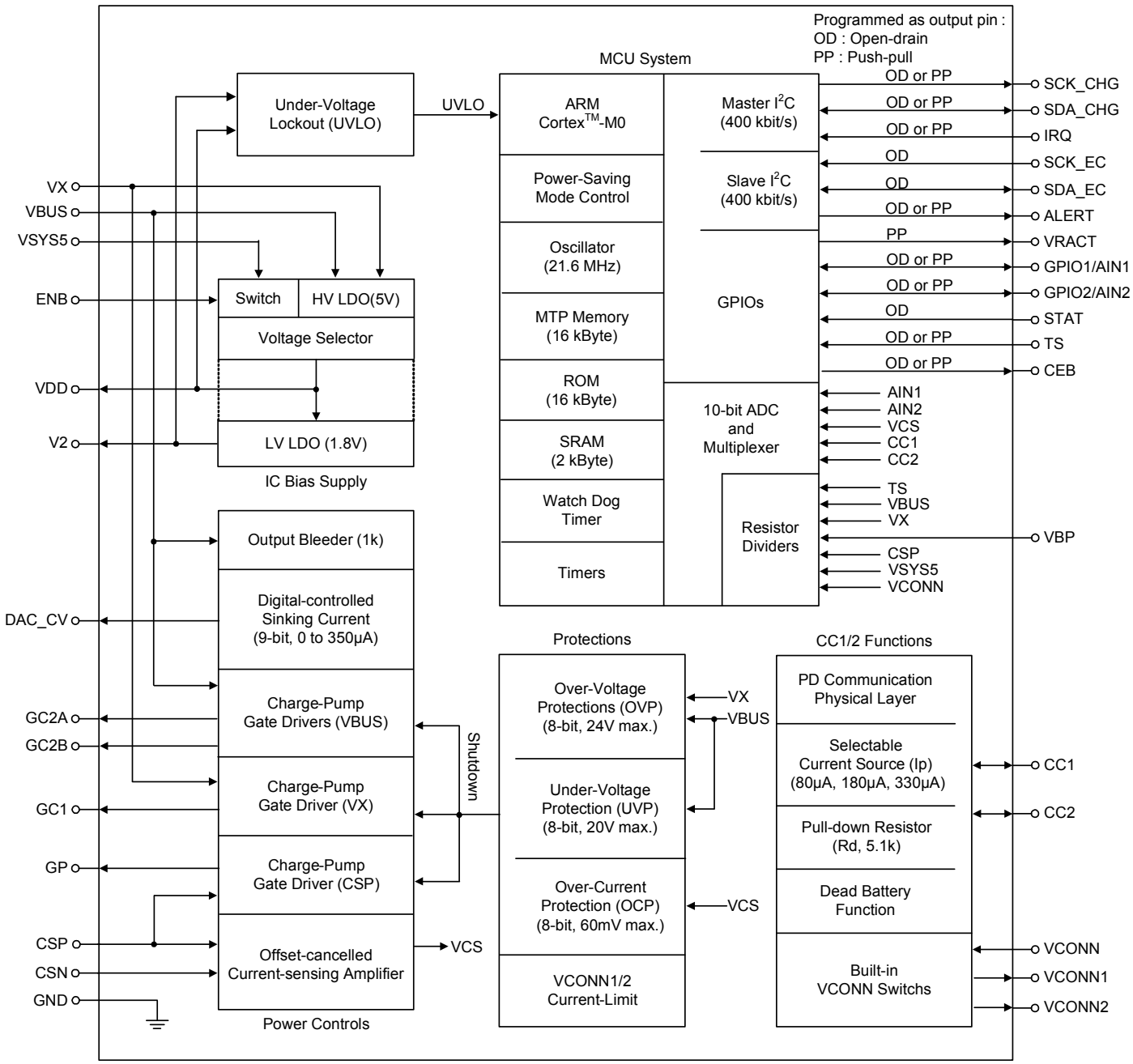
WQFN-40L 5x5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCONN	Power input of the power paths from VCONN to VCONN1 and VCONN2 pins. Generally, connect this pin to a 5V voltage source.
2, 7, 11, 20, 26, 29, 33, 35	NC	No internal connection.
3	CC1	First configuration channel. Generally, connect this pin to USB CC1 terminal.
4	VCONN1	Power output pin which supplies USB plug power (V_{CONN}) through USB CC1 terminal. A MOSFET is built in to turn on/off the power path from VCONN to VCONN1. Generally, connect this pin to USB CC1 terminal via a Schottky diode.
5	CC2	Second Configuration Channel. Generally, connect this pin to USB CC2 terminal.
6	VCONN2	Power output pin which supplies USB plug power (V_{CONN}) through USB CC2 terminal. A MOSFET is built in to turn on/off the power path from VCONN to VCONN2. Generally, connect this pin to USB CC2 terminal via a Schottky diode.
8	VDD	Output of the built-in linear regulator and VSYS5-to-VDD power path. This pin is also input pin of bias voltage/current for internal circuits. When the regulator is enabled, it regulates 5V (typ.) at VDD pin from the input voltage at VBUS or VX pin; when the power path is closed, the voltage at VDD follows the input voltage at VSYS5 pin. Connecting this pin with a 1μF external capacitor is recommended.
9	ALERT	Open-drain interrupt signal output. EC/AP could check the slave I^2C registers to do emergency control when it receives a low-level signal via this pin. This pin can be set as an open-drain or push-pull GPIO pin to achieve customized functions.
10	V2	Output of the built-in 1.8V linear regulator. From the input voltage at VDD pin, the regulator regulates voltage (1.8V typ.) at V2 pin for internal digital circuits. Connecting this pin with a 1μF external capacitor is recommended.
12	ENB	On/off control input of the internal VSYS5-to-VDD power path. The path is turned off for power-saving purpose when the ENB voltage is kept at high-level voltage.
13	SDA_EC	Open-drain data signal input/output of the slave I^2C. This pin can be set as an open-drain GPIO pin.
14	SCK_EC	Clock signal input of the slave I^2C. This pin can be set as an open-drain GPIO pin.

Pin No.	Pin Name	Pin Function
15	CEB	Open-drain output used to enable an external slave I^2C interface. This pin can be set as an open-drain or push-pull GPIO pin.
16	STAT	Charger status input. This pin can be set as an open-drain GPIO pin.
17	IRQ	Interrupt Input Pin. The RT7800B could check the slave I^2C registers of charger IC to do emergency control when it receives a low-level signal via this pin. This pin can be set as an open-drain or push-pull GPIO pin.
18	SDA_CHG	Open-drain data signal input/output of the master I^2C. This pin can be set as an open-drain or push-pull GPIO pin.
19	SCK_CHG	Open-drain clock signal output of the master I^2C. This pin can be set as an open-drain or push-pull GPIO pin.
21	GPIO1/AIN1	Open-drain/push-pull GPIO or analog input. Its function is programmable.
22	GPIO2/AIN2	Open-drain/push-pull GPIO or analog input. Its function is programmable.
23	TS	Battery temperature detection input. This pin can be set as an open-drain or push-pull GPIO pin.
24	VRACT	Push-pull output which is designed to enable/disable a DC-DC converter. The voltage at VRACT pin must be less than V_{DD}+0.3V.
25	DAC_CV	Digitalized sinking current output for adjusting the output voltage of the DC-DC converter. Connecting this pin to voltage feedback pin of the DC-DC converter through a resistor (R_{VRACT} = 0Ω) is recommended. The R_{VRACT} can be open for enabling and testing the DC-DC converter during product development stage. The operating voltage at DAC_CV must be larger than 0.58V at $I_{DAC\_CV} \leq$ 240μA.
27	CSP	Positive current-sensing input for sensing output current in provider application. Please connect this pin to GND pin when this pin is not used.
28	CSN	Negative current-sensing input for sensing output current in provider application. Due to consideration of maximum voltage rating, please connect this pin to CSP pin when this pin is not used.
30	GP	Charge-pump gate diver output. It drives N-Channel power MOSFETs to turn on/off a power-path. The CSP pin must be connected to downstream or upstream node of the power-path.
31	GC2A	Charge-pump gate diver output. It drives N-Channel power MOSFETs to turn on/off a power-path. The VBUS pin must be connected to downstream or upstream node of the power-path.
32	GC2B	Charge-pump gate diver output. It drives N-Channel power MOSFETs to turn on/off a power-path. The VBUS pin must be connected to downstream or upstream node of the power-path.
34	GC1	Charge-pump gate diver output. It drives N-Channel power MOSFETs to turn on/off a power-path. The VX pin must be connected to downstream or upstream node of the power-path.
36	VBP	Voltage-sensing input which can be used to monitor the charger input voltage.
37	VBUS	Power and voltage-sensing input. This is one of input pins of the built-in linear regulator which regulates 5V (typ.) voltage at VDD pin. This pin is also voltage input pin of GC2A and GC2B charge-pump gate drivers.
38	VX	Additional power and voltage-sensing input. This is one of input pins of the built-in linear regulator which regulates 5V (typ.) voltage at VDD pin. This pin is also voltage input pin of GC1 charge-pump gate driver.
39	GND	Ground pin.
40	VSYS5	5V power and voltage-sensing input. Connect this pin to a 5V voltage source.
41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT7800B is a versatile USB PD controller which can be used in a Provider, Consumer or Dual Role configuration. It' s a highly integrated solution, consisting of four main functional blocks: MCU system, power controls, protections and CC1/2 PD communication interface as shown in the "Simplified RT7800B Block Diagram".

The MCU system embeds ARM Cortex™-M0 MCU, multi-time programmable (MTP) memory, ROM, SRAM, a 10-bit ADC (analog to digital converter), two I^2C interfaces (slave and master) and GPIO (General Purpose Input or Output) pins. The MCU system is programmed to perform Policy Engine and Device Policy Manager. It can report operating statuses of PD operation, such as present input/output voltage and output current, to EC/AP and receive commends from EC/AP(System Policy Manager) via the slave I^2C interface. The GPIO pins can be used to switch high-speed multiplexers or some customized functions.

The "power controls" block consists of an AnyVolt™ constant-voltage (CV) control, an offset-cancelled output current-sense amplifier, four charge-pump gate drivers and VBUS output bleeder. The CV control programs sinking current, flowing into DAC_CV pin, to control output voltage of a DC-DC converter. The output current-sense amplifier, CS AMP, allows using a 10mΩ to 15mΩ current-sense resistor for reducing power loss. The charge-pump drivers drive low-cost (compared to P-Channel MOSFETs) N-Channel MOSFETs for on/off controls of three power-paths. The output bleeder, consisting of built-in resistor (typical 1kΩ) and an N-Channel MOSFET at VBUS pin, can be turned on to discharge the V_{BUS} during V_{BUS} negative transition, hard reset process or the removal of USB-C connector.

The PDsafe™ power delivery operations consist of over-voltage protections (OVP) at VBUS and VX pins, under-voltage protection at VBUS pin, V_{BUS} output over-current protection (OCP) and V_{CONN} output current-limit function. The OVP and UVP trip levels can be dynamically set for each input/output voltage target. The V_{BUS} output OCP trip level is also adaptively programmed according to full load current level.

The "CC1/2 PD communication interface" block consists of physical layer, three selectable pull-up current sources (Ip, instead of resistors Rp), single pull-down resistor (Rd) and programmable switches, dead-battery function and V_{CONN} power-path switches.

VDD Bias Voltage Generation

In Figure 1, there are three possible input pins (VBUS, VX, and VSYS5) to supply bias voltage to VDD pin for RT7800B internal circuits. This multi-input and auto-selection design, including a built-in high-voltage linear regulator and a VSYS5-to-VDD pass transistor (SW1), equips RT7800B with high application flexibility for Provider, Consumer or Dual Role applications.

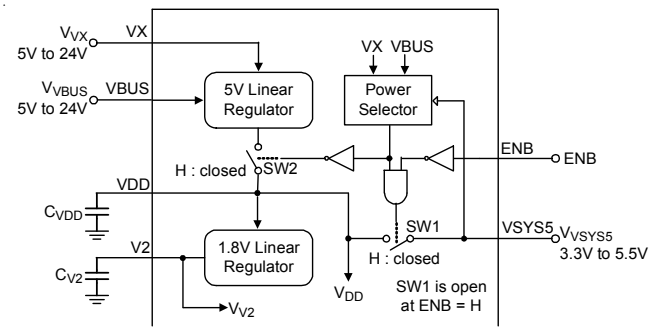


Figure 1

An input power selection circuit automatically selects the highest voltage at VBUS, VX or VSYS pins to generate the VDD voltage. When the linear regulator is enabled, it regulates the VDD voltage, typical 5V from the VBUS voltage (which is generally from a USB PD Provider), or the VX voltage (which is from an additional power source). If VBUS and VX pins have no sufficient voltage, the VDD voltage is supplied from the VSYS5 pin via the pass transistor. The transistor, designed for ultra low power consumption, is kept off when ENB voltage is at high level. The VSYS5 voltage is generally from the 5V voltage supply inside an application system.

Under-Voltage Lockout (UVLO)

The RT7800B UVLO function continually monitors the bias voltages at the VDD and V2 pins. When both of the supply voltages (V_{DD} and V_{V2}) exceed their rising UVLO thresholds, the IC is enabled to work. Otherwise, it will be "Under-Voltage Lockout" status to prevent any undesirable operations.

AnyVolt™ Output Voltage Adjustment

In a Provider application, the RT7800B provides the "AnyVolt™" feature for multiple selections of output voltage so as to achieve high power efficiency of switching/linear charger in portable devices such as smart phone, tablet PC, and etc. The RT7800B are designed to gradually increase/decrease the Provider output voltage from 3V to 20V or 20V to 3V with typical 50mV/step. A programmable sinking current (9-bit, 0 to 350μA), flowing into DAC_CV pin via a high-side feedback resistor of a DC-DC converter, is programmed to adjust output voltage of the DC-DC converter, where DAC_CV pin is connected to voltage feedback (FB) pin of the DC-DC converter.

Cable Voltage Drop Compensation (CDC)

In a power delivery operation, both Provider and Consumer configurations of the RT7800B can monitor the voltages on each VBUS pin to compensate voltage drop across USB cable. The Consumer RT7800B can request higher VBUS voltage from the Provider through PD protocol communication to achieve accurate application voltage.

Over-Voltage Protection (OVP)

In Figure 2, OVPs are detected at VBUS and VX pins with programmable (8-bit) trip-level from 5.5V up to 24V. Each OVP debounce time is programmable to meet various application requirements.

Under-Voltage Protection (UVP)

In Figure 2, UVP is detected at VBUS pin with programmable (8-bit) trip-level from 3V to 20V. UVP debounce time is programmable to avoid false triggering and to meet various application requirements.

AnyCurrent™ Over-Current Protection (OCP)

Because a robust system is very important in USB PD operations, the AnyCurrent™ OCP feature allows setting a most suitable OCP trip level for a negotiated PD system. The RT7800B integrates a current-sense amplifier to detect the output current for OCP and to indicate the value of output current. The amplifier, designed with offset cancellation function, can accurately detect the current-sense voltage (i.e., output current x current-sense resistor) between CSP and CSN pins. The OCP trip voltage setting is programmable (8-bit) and recommended from 10mV to 60mV.

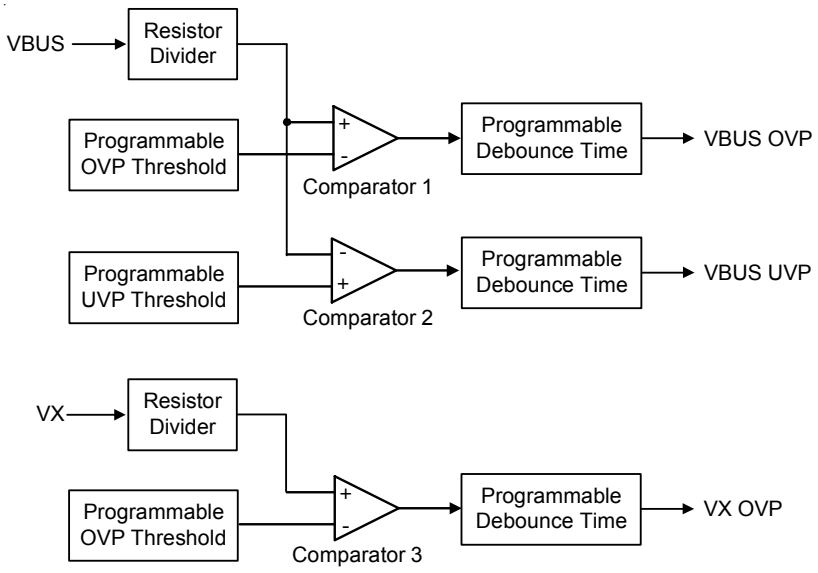


Figure 2

Constant-Current (CC) Regulation

In a RT7800B inside Provider working in coordination with a DC-DC converter, the output CC regulation function can be implemented by firmware design. The RT7800B, continuously monitoring output current via CSP and CSN pins, can regulate output current at a selected current level by dynamically adjusting the digitalized current flowing into DAC_CV pin. The CC regulation, limiting VBUS output current, provides a better system protection than over-current protection.

Power-Path Gate Drivers

There are four gate drivers in the RT7800B to turn on/off three pairs of low on-resistance N-Channel power MOSFETs for each individual input/output power path. Compared to driving P-Channel power MOSFET, this design using N-MOSFET is more cost-effective. Each gate driver includes a built-in charge pump for turning on and an internal pull-low switch for turning off the power MOSFETs.

Internet On-line Firmware Update

Due to using MTP memory, RT7800B firmware can be updated by an EC (Embedded Controller) or AP (Application Processor) via I^2C slave interface. Users can easily update firmware without de-soldering/soldering RT7800B during product development period. In mass production, the RT7800B based products can use same-version RT7800B ICs to reduce inventory cost. It also allows updating RT7800B firmware at end customer site through internet in response to some necessary system software changes.

Power Output for USB Plug Power (V_{CONN})

In Figure 3, a selected output voltage at one of VCONN1 and VCONN2 pins is provided for powering an external Electrically Marked (E-mark) or active cable. One of internal MOSFETs between VCONN to VCONN1 and VCONN2 pins can be turned on to supply power to VCONN1 or VCONN2 pin. Connect the VCONN1/2 pin to USB-C CC1/2 terminal via a Schottky diode (D1/2) for blocking reverse current. The input pin VCONN must be connected to a 5V power source.

Dead Battery Function

In Figure 3, a voltage-clamping circuit clamps the CC1/2 voltage when the RT7800B has no power at VBUS, VX and VSYS5 pins. A no-power RT7800B Provider or Dual Role port will be recognized as a Consumer by clamping the voltage level at the RT7800B CC1/2 pin. The RT7800B starts to work, after an external Provider supplies USB cable power (V_{BUS}) to its VBUS pin.

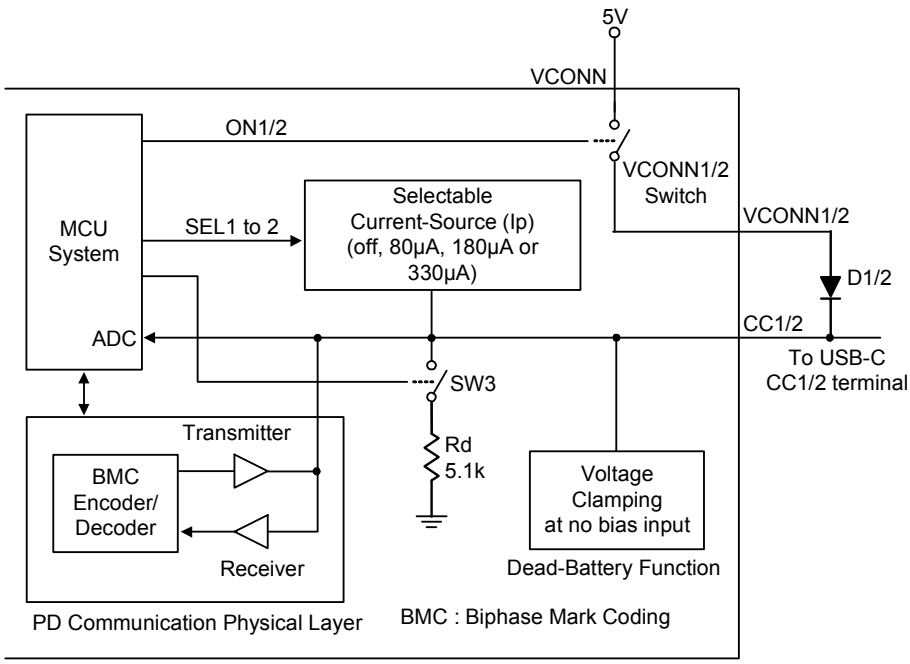


Figure 3

Absolute Maximum Ratings (Note 1)

- V2 to GND ---------- –0.3V to 2.5V
- VDD to GND(V_{DD}), VSYS5, VCONN (V_{VCONN}) to GND ---------- –0.3V to 6.5V
- VCONN1, VCONN2 to GND ---------- –0.3V to V_{VCONN} + 0.3V
- VBUS, VX, CSP, CSN, DAC_CV, VBP to GND ---------- –0.3V to 25V
- GC1, GC2A, GC2B, GP to GND ---------- –0.3V to 33V
- CSP to CSN Voltage, $V_{CSP-CSN}$ ---------- ±5V
- VRACT to GND ---------- –0.3V to V_{DD} + 0.3V
- I^2C Pins (SCK_EC, SDA_EC, ALERT, SCK_CHG, SDA_CHG, IRQ) to GND ---------- –0.3V to 6.5V
- CC1, CC2 to GND ---------- –0.3V to 22V
- CEB, STAT, TS, ENB, GPIO Pins(GPIO1/AIN1, GPIO2/AIN2) to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 3.63W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  Human Body Model (HBM) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VBUS, VX Supply Voltage ---------- 0V to 22V
- VSYS5 Supply Voltage ---------- 3.3V to 5.5V
- Total Output Current of the Push-pull GPIO Pins ---------- 0 to 10mA
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{VSYS5} = 5V, ENB = VX = VBUS = GND, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Built-in Linear Regulators and Operating Currents							
VBUS Pin Input Voltage Range	V_{VBUS}			4.5	--	22	V
VX Pin Input Voltage Range	V_{VX}			4.5	--	22	V
VSYS5 Pin Input Voltage Range	V_{VSYS5}			3.3	5	5.5	V
VDD Output Voltage	V_{REG5}	Total Digital-pin I_O < 10mA, I_{DD} = 0mA	V_{VSYS5} = 5V, V_{VX} = V_{VBUS} = 0V	4.4	4.7	--	V
			V_{VSYS5} = 0V, V_{VX}/V_{VBUS} = 5V				
			V_{VSYS5} = 0V, V_{VX}/V_{VBUS} = 20V	4.5	5	5.5	
VDD Short-Circuit Current	I_{SC_VDD}	VDD = GND	V_{VSYS5} = 5V, V_{VX} = V_{VBUS} = 0V	40	85	140	mA
			V_{VSYS5} = 0V, V_{VX}/V_{VBUS} =20V	40	85	140	
VSYS5 Normal Operating Current	I_{OP_VSYS5}	V_{VSYS5} = 5V, V_{VBUS} = V_{VX} = 0V, Digital output pins = open		--	10	--	mA
VBUS/VX Normal Operating Current	$I_{OP\_VBUS/VX}$	V_{VSYS5} = 0V, V_{VBUS}/V_{VX} = 20V, Digital output pins = open		--	10	--	mA
VSYS5 Operating Current in Green-Mode (GM)	I_{GM_VSYS5}	V_{VSYS5} = 5V, V_{VBUS} = V_{VX} = 0V		--	5.5	7.5	mA
VBUS/VX Operating Current in GM	$I_{GM\_VBUS/VX}$	V_{VSYS5} = 0V, V_{VBUS}/V_{VX} = 20V		--	5.5	7.5	mA
VSYS5 Operating Current in Deep Green-Mode (DGM)	I_{DGM_VSYS5}	V_{VSYS5} = 5V, VBUS and VX power paths are disabled		--	108	200	μA
VSYS5 Shutdown Current	I_{SD_VSYS5}	V_{VSYS5} = 5V, V_{ENB} = 5V, V_{VX} = V_{VBUS} = 0V		--	4	8	μA
V2 Output Voltage	V_{REG18}	V_{DD} = 5V, I_{V2} = 0mA		1.62	1.80	1.98	V
V2 Short-Circuit Current	I_{SC_V2}	V2 = GND, V_{DD} = 5V		20	40	60	mA
Under-Voltage Lockout (UVLO), Over/Under-Voltage Protections (OVP, UVP), and Voltage Detections							
VDD UVLO Voltage Threshold	V_{TH_UVLO1R}	V_{DD} rising, not in deep-green mode		2.7	2.9	3.1	V
VDD UVLO Voltage Hysteresis	V_{HYS_UVLO1}			--	0.1	--	V
V2 UVLO Voltage Threshold	V_{TH_UVLO2R}	V_{V2} rising		--	1.4	--	V
V2 UVLO Voltage Hysteresis	V_{HYS_UVLO2}			--	0.2	--	V
VBUS OVP Voltage Threshold Range	V_{TH_VBUSOV}	Programmable (8-bit), 94.8mV/step at VBUS pin		5.5	--	24	V
VBUS OVP Voltage Threshold Accuracy		Nominal V_{TH_VBUSOV} = 6.0V/24.0V, V_{VBUS} rising		–5	--	5	%

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VBUS OVP Debounce Time	t_{DB_VBUSOV}	Programmable, V_{VBUS} rising		5.5 7.7 12.2 21.2	7.5 10 15 25	9.5 12.3 17.8 28.8	μs
VBUS UVP Voltage Threshold Range	V_{TH_VBUSUV}	Programmable (8-bit), 78mV/step at VBUS pin		3	--	20	V
VBUS UVP Voltage Threshold Accuracy		Programmable, V_{VBUS} falling V_{TH_VBUSUV} = 3.06V/15.0V		–5	--	+5	%
VBUS UVP Debounce Time	t_{DB_VBUSUV}	V_{VBUS} falling, programmable		4.0 4.4 5.3 7.1	6.0 6.5 7.5 9.5	8.0 8.6 9.7 11.9	μs
VX OVP Voltage Threshold Range	V_{TH_VXOV}	Programmable (8-bit), 94.8mV/step		5.5	--	24	V
VX OVP Voltage Threshold Accuracy		Nominal V_{TH_VXOV} = 6.0V/24.0V, V_{VX} rising		–5	--	5	%
VX OVP Debounce Time	t_{DB_VXOV}	Programmable, V_{VX} rising		5.5 7.7 12.2 21.2	7.5 10 15 25	9.5 12.3 17.8 28.8	μs
VBP Input Resistance	R_{IN_VBP}	Resistor-divider : On		--	500	--	kΩ
VBP Input Current		Resistor-divider : Off, V_{VBP} = 20V		--	--	2	μA
Output Voltage Control and Over-Current Protection (OCP) of External DC-DC PWM Converter							
DAC_CV Sinking Current Range	I_{DAC}	Programmable (9-bit), V_{DAC_CV} = 0.75 to 2.5V		0	--	350	μA
		Programmable, V_{DAC_CV} = 0.58V		0	--	240	
Maximum DAC_CV Sinking Current	I_{DAC_MAX}	V_{DAC_CV} = 0.75 to 2.5V	T_A = 25°C	–5%	350	5%	μA
			T_A = –40°C to 85°C (Note 5)	–15%	350	15%	
Resolution of the DAC_CV Sinking Current	I_{DAC_STEP}			--	I_{DAC_MAX} /511	--	μA
CSP-to-CSN OCP Voltage Threshold Range	V_{TH_OC}	Programmable (8-bit), V_{CSP} and V_{CSN} ≥ 3V, 0.238mV/step		10	--	60	mV
OCP Voltage Threshold Accuracy		V_{TH_OCP} = 30mV/60mV, V_{CSP} and V_{CSN} ≥ 3V		–3	0	3	mV
OCP Debounce Time	t_{DB_OC}	(Note 5)		--	3	--	μs
CSP Input Current	I_{CSP}	$V_{CSP-CSN}$ = 50mV	V_{CSP} = 5V	71	83	95	μA
			V_{CSP} = 9V	94	110	126	
			V_{CSP} = 12V	105	123	141	
			V_{CSP} = 14.5V	112	132	152	
			V_{CSP} = 20V	135	157	180	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Ratio of $\Delta V_{CSP-CSN}$ to ΔI_{CSP}		(Note 5)	--	2.7	--	kΩ
CSN Input Current	I_{CSN}	V_{CSN} = 5V to 20V	12	16	20	μA
VRACT High-Level Output Voltage		Sourcing current = 2mA	V_{DD} – 0.2V	V_{DD} – 0.1V	--	V
VBUS Built-in Bleeder Resistor		At on state	--	1	1.3	kΩ
CC1/2 Voltage Detections and BMC Transmitter/Receiver						
CC1/2 Voltage Detection Range		Using the 10-bit ADC	0	--	2.7	V
CC1/2 Voltage Detection Accuracy		Using the 10-bit ADC, $V_{CC1/2}$ = 0.1 to 2.7V	–40	--	40	mV
CC1/2 Pull-Up Current Source – 1	Ip1	For default USB power	–20%	80	20%	μA
CC1/2 Pull-Up Current Source – 2	Ip2	For 1.5A @ 5V	–8%	180	8%	μA
CC1/2 Pull-Up Current Source – 3	Ip3	For 3A @ 5V	–8%	330	8%	μA
CC1/2 Pull-Down Resistor	Rd		–10%	5.1	10%	kΩ
CC1/2 Maximum Output Voltage		CC1/2 = open (Note 5)	--	V_{DD} – 0.7V	--	V
Transmitter High-Level Output Voltage Range			1.05	--	1.2	V
Transmitter Low-Level Output Voltage Range			0	--	75	mV
Receiver High-Level Input Voltage Range			0.67	--	1.45	V
Receiver Low-Level Input Voltage Range			–0.25	--	0.43	V
Rising Time of the Transmitter Output Voltage	t_{R_CC}	From 10% to 90%, C_L = 200pF to 600pF	300	--	--	ns
Falling Time of the Transmitter Output Voltage	t_{F_CC}	From 90% to 10%, C_L = 200pF to 600pF	300	--	--	ns
DFP-side CC1/2 Voltage Range in RT7800B Dead-Battery Condition		For default USB power	0.25	--	1.5	V
		For 1.5 A @ 5 V	0.45	--	1.5	
		For 3.0 A @ 5 V	0.85	--	2.45	
On-Resistance of the VCONN-to- VCONN1/2 MOSFET		V_{VCONN} = 5V	--	0.7	--	Ω
VCONN1/2 Output Voltage Accuracy		V_{VCONN} = 5V, I_O = 0 to 200mA	4.70	--	--	V
VCONN1/2 Current-Limit Threshold			270	400	550	mA
VCONN Input Current		Disabled, V_{VCONN} = 5V, $V_{VCONN1/2}$ = 0V	--	--	2	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MCU Section						
MCU Clock Frequency	f_{MCU}		−10%	21.6	10%	MHz
Power-Path Gate Drivers and Input/Output Pins						
On Resistance of GC1, GC2A/B, GP Pull-Low MOSFET	R_{PL_Gx}		--	100	--	Ω
Maximum GC1 Output Voltage		V_{VX} = 20V, $R_{VX\text{-to-}GND}$ > 50MΩ	V_{VX} + V_{DD}	V_{VX} + 2·V_{DD} − 3V	V_{VX} + 2·V_{DD} −1V	V
Maximum GC2A/B Output Voltage		V_{VBUS} = 20V, $R_{GC2A/B\text{-to-}GND}$ > 50MΩ	V_{VBUS} +V_{DD}	V_{VBUS} +2·V_{DD} −3V	V_{VBUS} +2·V_{DD} −1V	V
Maximum GP Voltage		V_{CSP} = 20V, $R_{GP\text{-to-}GND}$ > 50MΩ	V_{CSP} + V_{DD}	V_{CSP} + 2·V_{DD} −3V	V_{CSP} + 2·V_{DD} −1V	V
High-Level Input Voltage Range of Digital Input Pins		Including the digital pins (I^2C, GPIOs, CEB, STAT, TS, ENB) configured as input pins	2.4	--	--	V
Low-Level Input Voltage Range of Digital Input Pins			--	--	0.4	V
Input Current of the Digital Input Pins		Configured as input pins, Input voltage = 5V	--	--	2	μA
High-Level Output Voltage of Digital Output Pins		Sourcing current = 2mA, for the digital pins configured as push-pull output pins	--	V_{DD} − 0.8	--	V
Low-Level Output Voltage of Digital Output Pins		Sinking current = 2mA, for the digital pins configured as output pins	--	--	0.3	V
AIN1/2 Input Voltage Range for ADC		V_{DD} = 4.5V, Resolution = 2.64mV	0.1	--	2	V
AIN1/2 Input Current		$V_{AIN1/2}$ = 5V	--	--	2	μA
TS Input Voltage Range for ADC		V_{DD} = 4.5V, Resolution = 7.93mV	0.3	--	5.5	V
TS Input Resistance	R_{IN_TS}	Resistor-divider : On	--	90	--	kΩ

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package. The copper area is 70mm^2 connected with IC exposed pad.

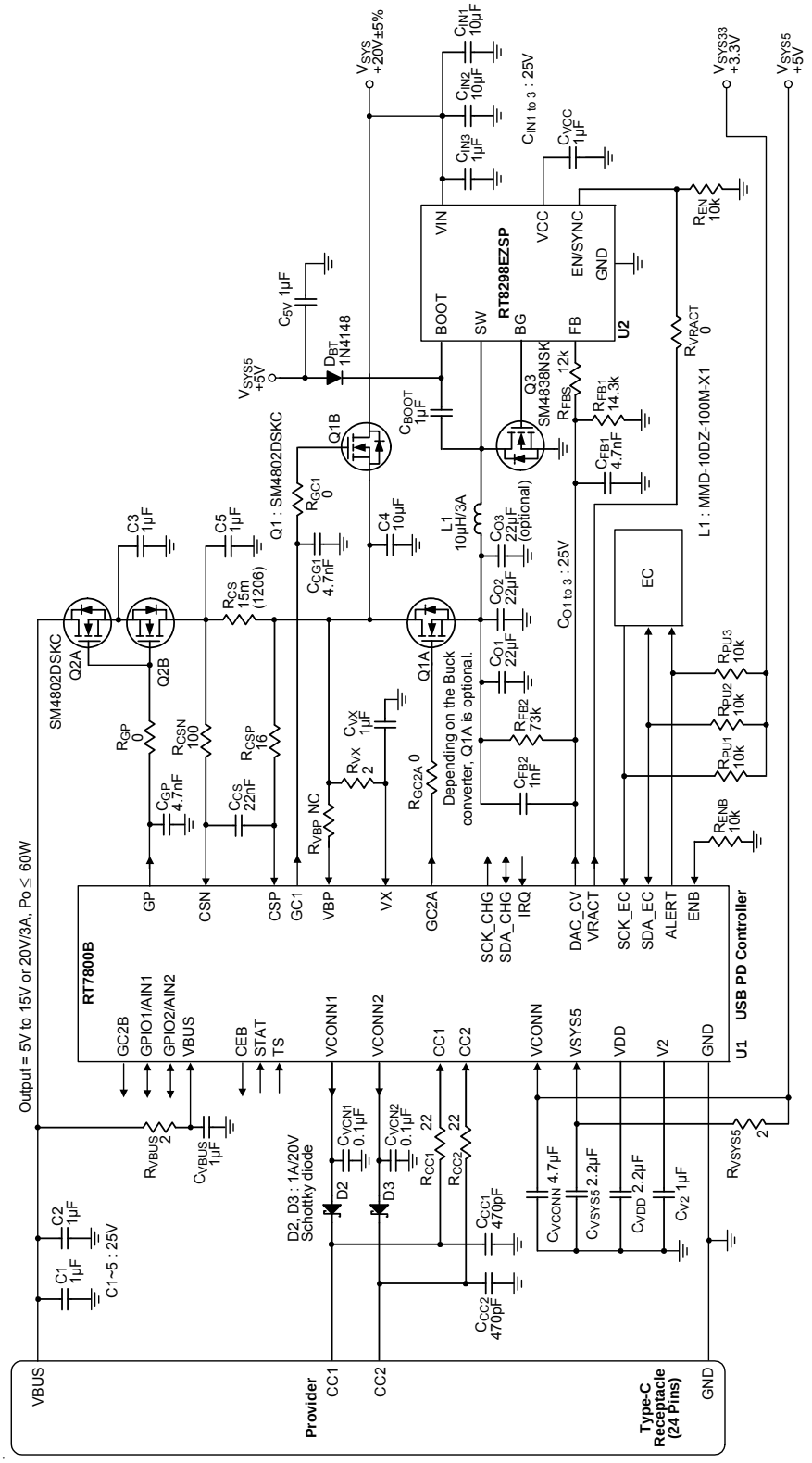
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

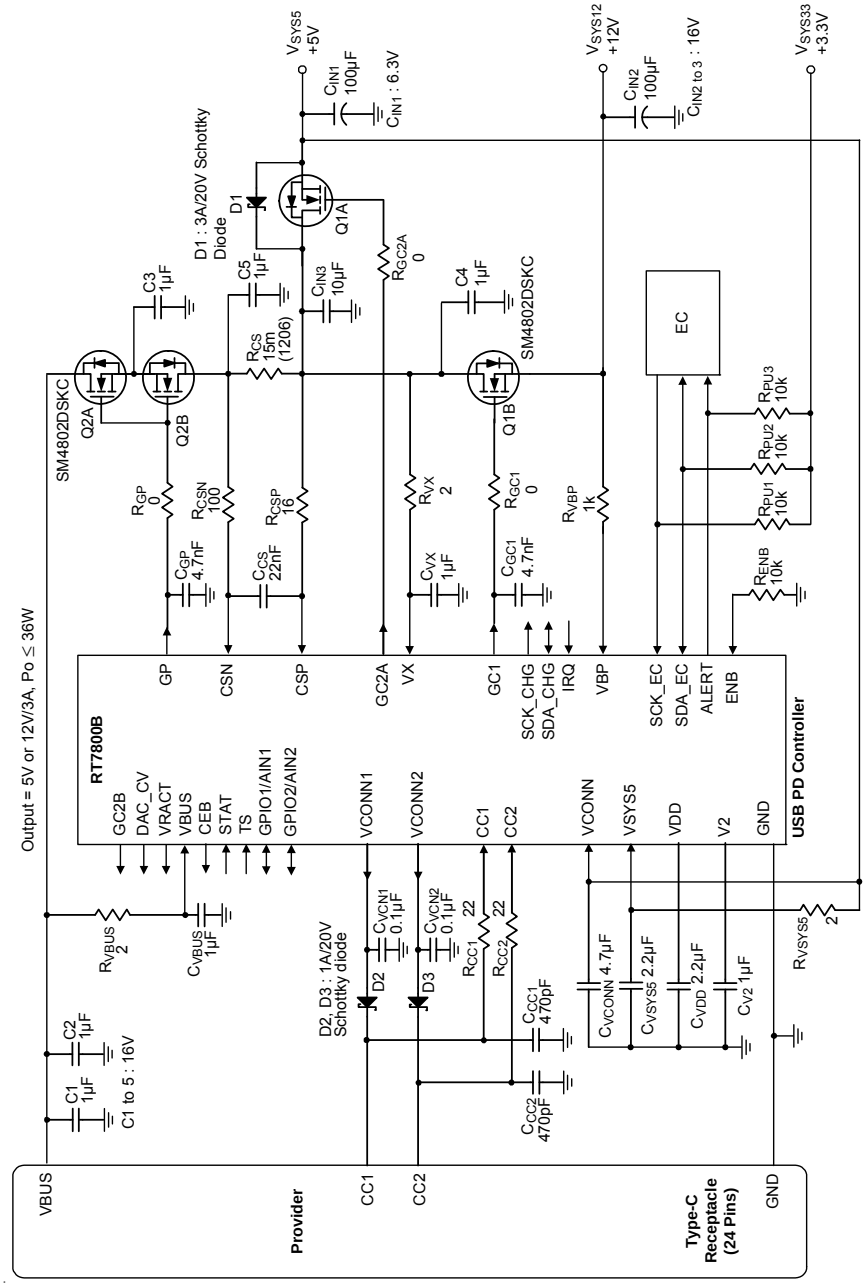
Note 5. Guaranteed by design.

Typical Application Circuit

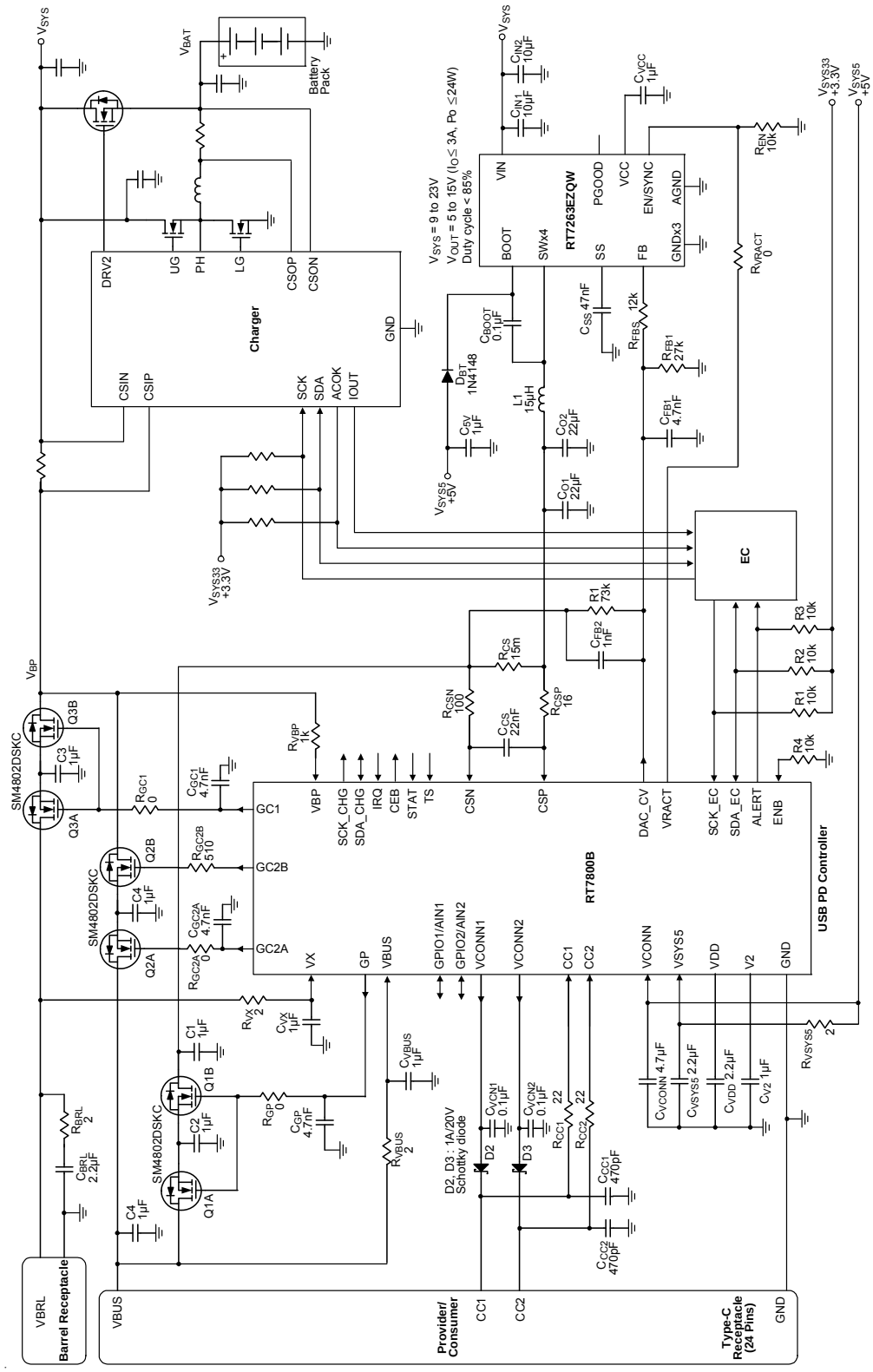
(1) Provider Application Circuit for Monitor



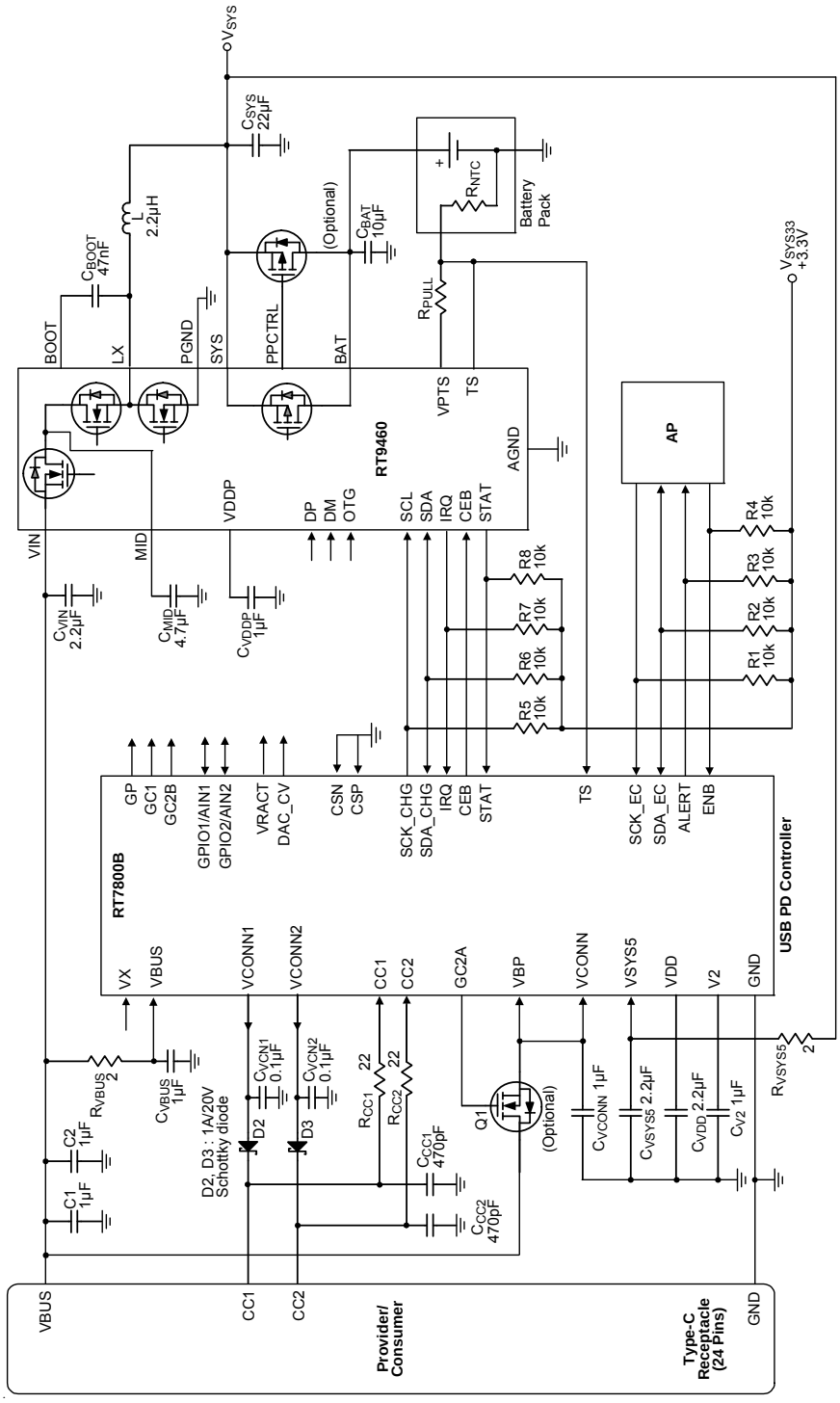
(2) Provider Application Circuit for Desktop PC



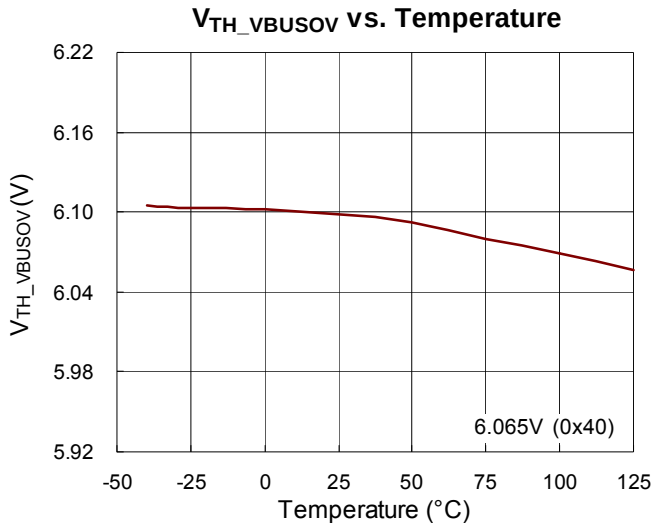
(3) Dual Role Application Circuit for Notebook PC

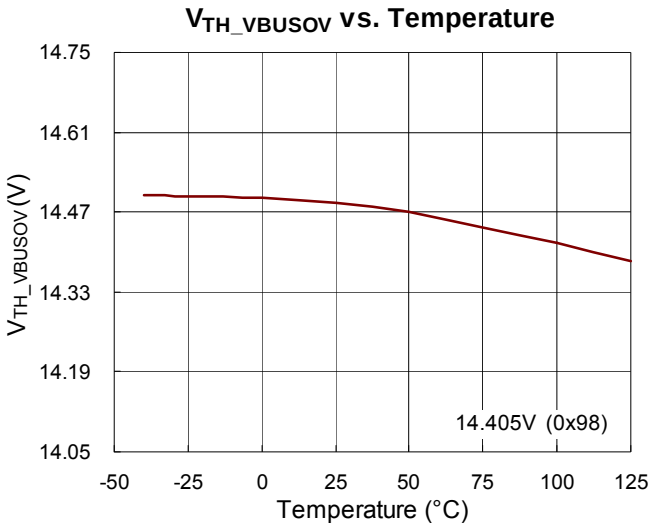


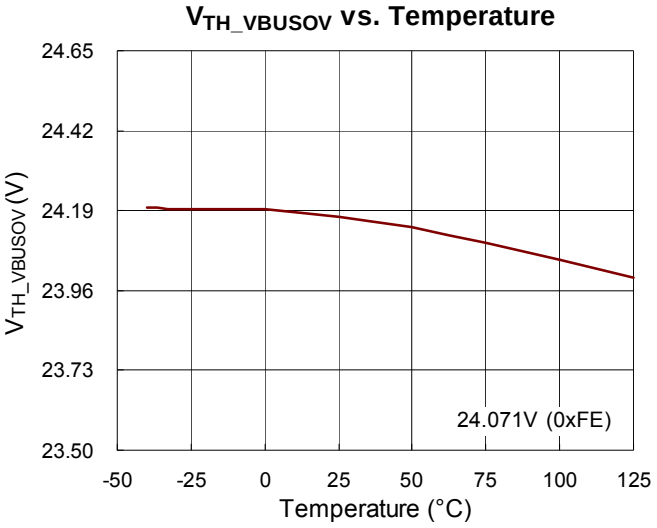
(4) Dual Role Application Circuit for Smart-phone and Tablet PC

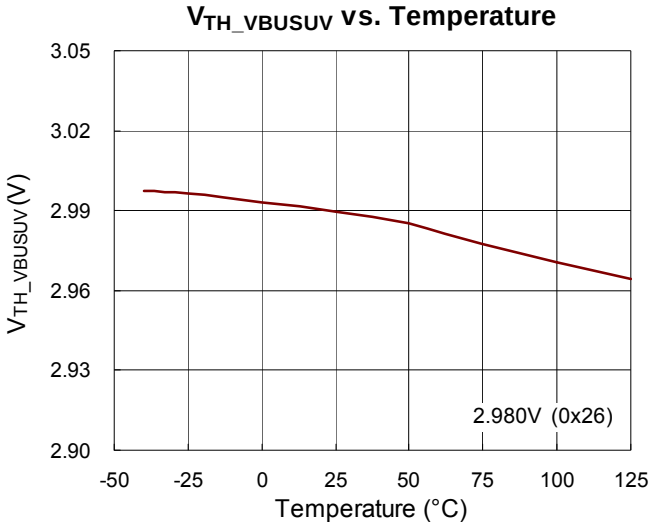


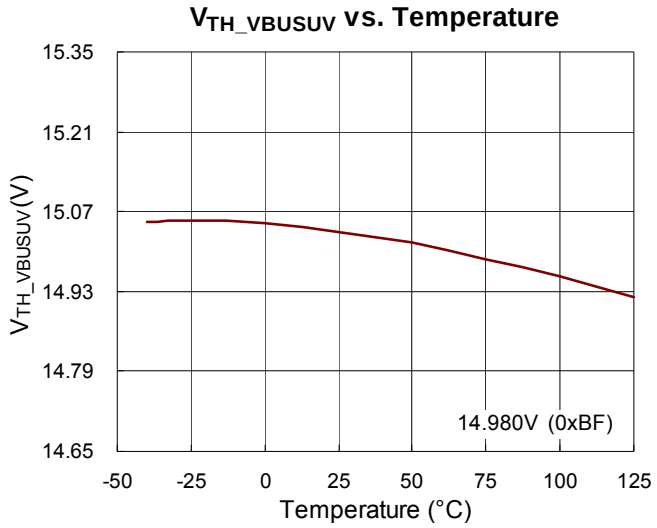
Typical Operating Characteristics

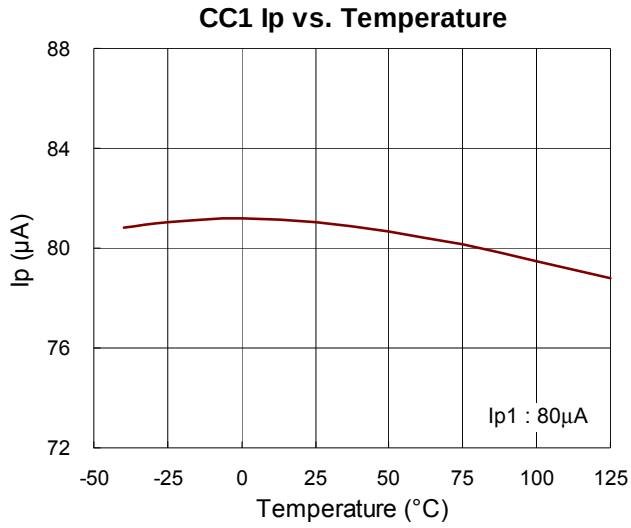




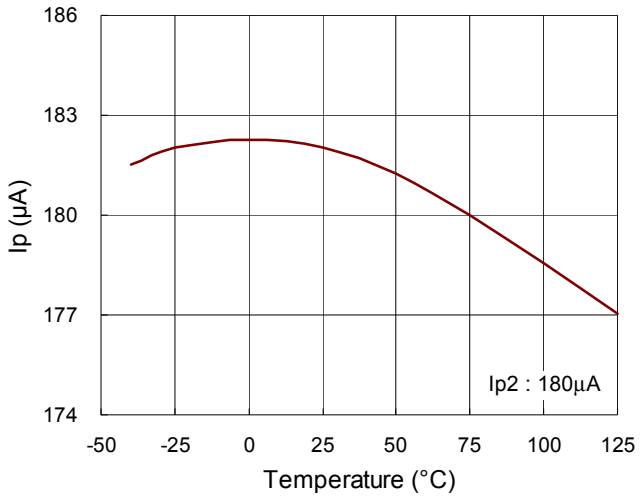




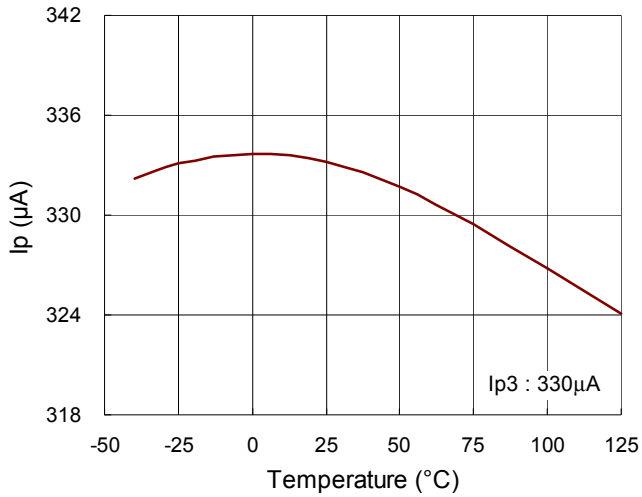




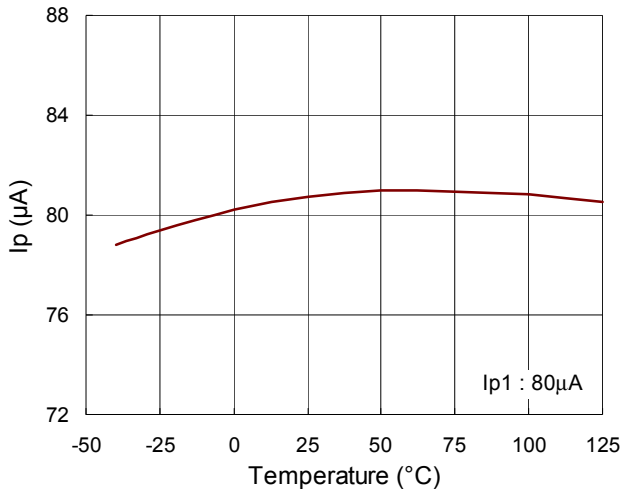
CC1 Ip vs. Temperature



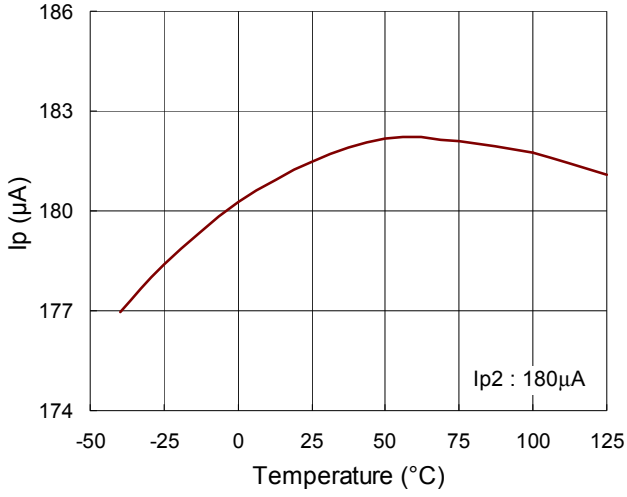
CC1 Ip vs. Temperature



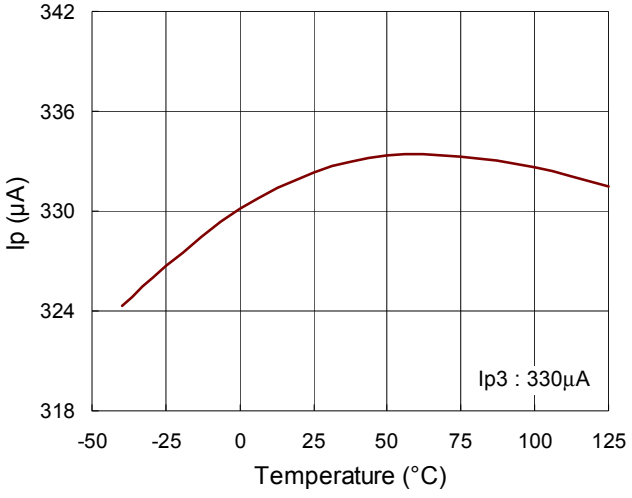
CC2 Ip vs. Temperature



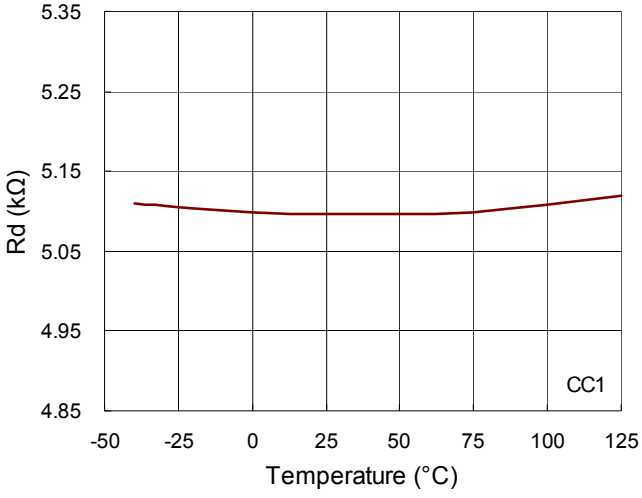
CC2 Ip vs. Temperature

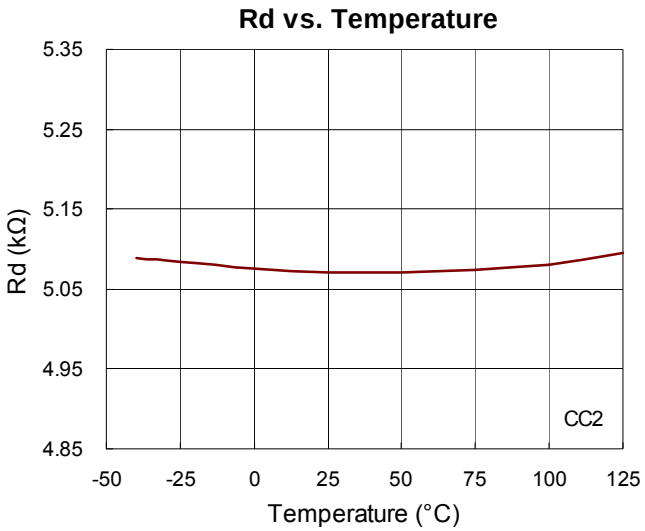


CC2 Ip vs. Temperature



Rd vs. Temperature





Application Information

Output Voltage Setting of DC-DC Converter

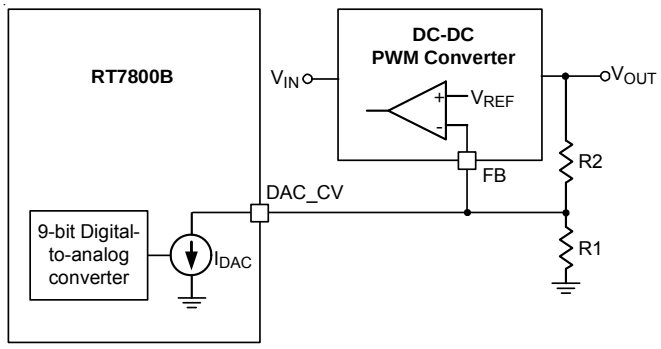


Figure 4

Figure 4 shows the RT7800B can change the output voltage (V_{OUT}) of the DC-DC converter by controlling the DAC_CV sinking current (I_{DAC}, 0 to 350μA).The output voltage V_{OUT} of the DC-DC converter can be programmed according to the equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) + I_{DAC} \times R2$$

where :

- V_{REF} is the reference voltage of the DC-DC converter. Using $V_{REF} \geq 0.6V$ is necessary.
- R1 and R2 are the V_{OUT} feedback resistors of the DC-DC converter.

Base on a recommended resolution (V_{OUT_STEP} = 50mV/step) for programming the output voltage V_{OUT}, the R2 can be determined by the following equation :

$$R2 = \frac{V_{OUT\_STEP}}{I_{DAC\_STEP}}$$

$$= \frac{V_{OUT\_STEP} \times 511}{I_{DAC\_MAX}} = \frac{50mV \times 511}{350\mu A} = 73k\Omega$$

For the most of applications, the lowest output voltage V_{OUT_MIN} (at I_{DAC} = 0A) is set to 3V to 5V. It is recommended to set the V_{OUT_MIN} = 5V, when a PWM IC with V_{REF} = 0.6V is adopted. Therefore, the R1 can be determined by the equation :

$$R1 = \frac{R2 \times V_{REF}}{V_{OUT\_MIN} - V_{REF}}$$

Calculating Output Discharge Time

Figure 5A is the functional block diagram of the built-in output bleeder. The discharge time (t_{DIS}) is determined by the following equation:

$$t_{DIS} = R_{BLD} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_OLD}}{V_{BUS\_NEW}}\right)$$

where :

- R_{BLD} is the total internal resistance during on-state of the bleeder.
- C_{VBUS} is the total capacitance of the capacitors coupled to VBUS pin.
- V_{BUS_OLD} is the initial voltage between the capacitors before the discharging.
- V_{BUS_NEW} is the final voltage between the capacitors at end of the discharging.

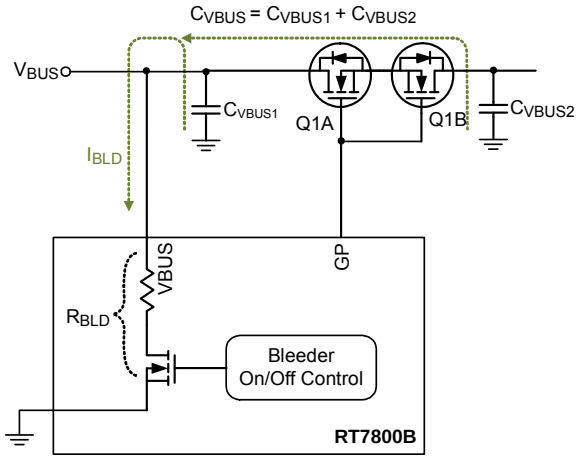


Figure 5A

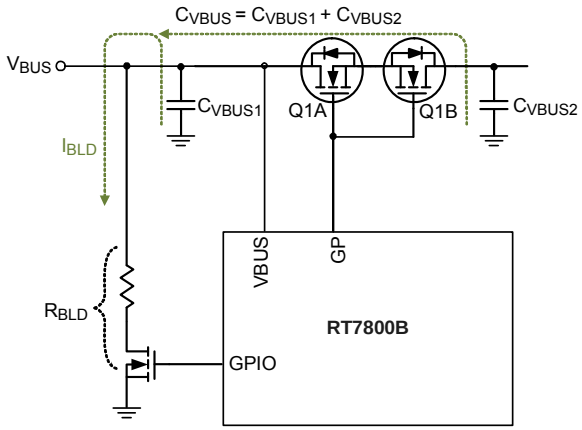


Figure 5B

If the discharge time at using the built-in bleeder is out of the PD specification, an external bleeder, consisting of a resistor and an n-channel MOSFET, in Figure 5B is a preferred design. The external bleeder is controlled by the RT7800B via a GPIO pin.

Using charge-pump gate driver for power-path on/off control

Figure 6 is an application diagram of a power-path on/off control. In this diagram, two low on-resistance N-Channel MOSFETs, driven by a built-in charge-pump gate driver, are employed to turn on or off the power-path between V1 and V2 terminals. The charge pump pulls high GATE voltage for turning on the power MOSFETs (Q1 and Q2) when the control signal ON goes high state. During ON = Low, the charge pump stops switching and a built-in MOSFET pulls low the GATE voltage (V_{GATE}) to disconnect the power path.

There are two necessary power inputs (VP and VDD) for the charge pump. The VP pin must be connected to either upstream or downstream terminal; otherwise the power MOSFETs might not be turned on successfully. As shown in Table 1, the power input of GC2A and GC2B charge-pumps is VBUS pin; the power input of GC1 charge-pump is VX pin; the power input of GP charge-pump is CSP pin.

Table 1

Gate Driver Output Pin	Power Input Pin
GP	CSP
GC1	VX
GC2A, GC2B	VBUS

The capacitor (C_{GATE}) is an optional MLCC used for reducing the V_{GATE} rising rate as well as limiting surge current in the power-path during turn-on transition. During turn-off transition, the power-path parasitic inductor and "C1 or C2" might cause ringing voltage at the Drain terminal of Q1 or Q2. The optional gate resistor (R_{GATE}) can be adopted to slow the power-path current falling rate and prevent the voltage spike. The capacitor (C_{MID}), connected from the Source terminals to ground, can prevent natural oscillation of the dual-MOSFET connection. A 1μF MLCC is recommended for the C_{MID}.

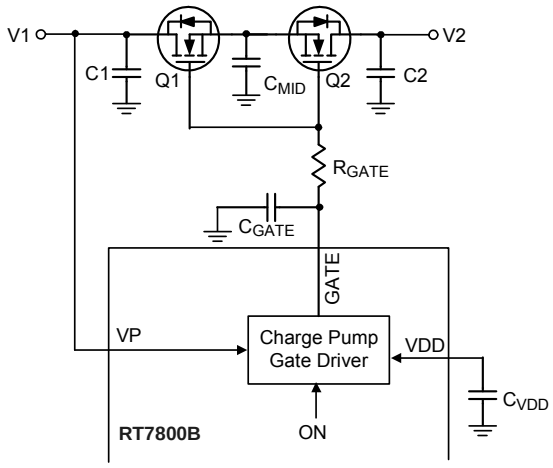


Figure 6

Manual Firmware Update

During product development stage, users might need to download or update the RT7800B firmware. In Figure 7, it's recommended to add a 5-pin connector (CON1) or test pads on PCBs for updating the RT7800B firmware manually. Generally, the connector is connected to a "RT7800 firmware update fixture" by a 5-pin cable. The fixture is also connected to a PC by a Micro USB cable and acts as a bridge between the RT7800B and the PC. Therefore, users can download firmware to RT7800B by using the RT7800B graphic user interface(GUI) installed in the PC. During firmware update process, the USB-C connector must be disconnected from the cable. It is not necessary to turn on the power of the PCB, because the fixture can supply power to the RT7800B via IC VBUS pin.

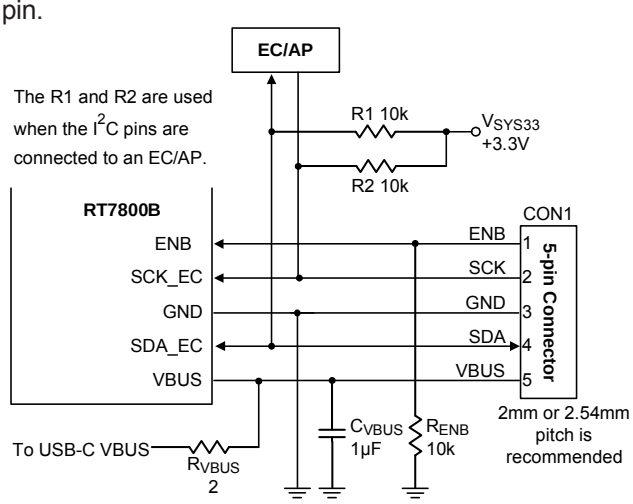


Figure 7

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

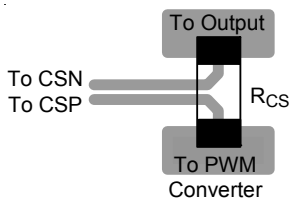
For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.63W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout Considerations

- Connect the IC GND pins and the exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via low impedance path. The exposed pad is also applied to dissipate the heat into PCB.
- Connect the decoupling MLCCs near to the pins of VCONN, VSYS5, VDD, V2, VBUS and VX. Connect the MLCCs to the pins and IC-ground via low impedance paths.
- Connect the capacitor (between CSP and CSN pins) close to CSP and CSN pins. The paths of CSP and CSN must be directly connected to the terminals of current-sensing resistor (R_{CS}). Connect the CSN and CSP pins to GND when the current sensing amplifier and OCP function is not used.



- Separate following signals from the switching nodes and the switching-current paths to prevent the noise :
  - Current-sensing signal.
  - CC1 and CC2 signals.
  - DAC_CV signal and the feedback signal of the DC-DC converter.
- For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of USB Type-C connector. Connect the capacitors to the USB VBUS and GND terminals through the low impedance paths.

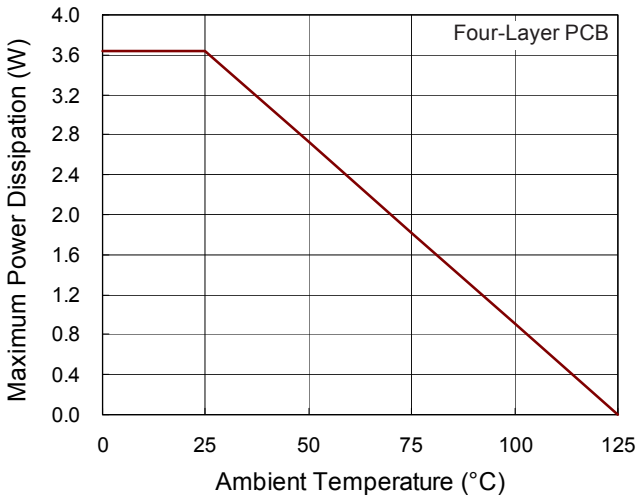
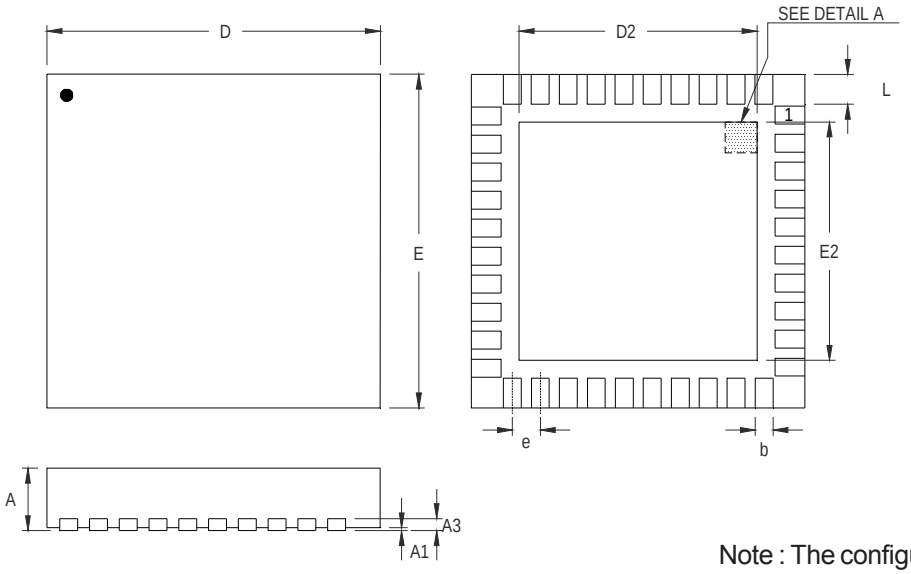
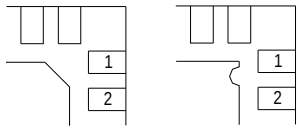


Figure 8. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

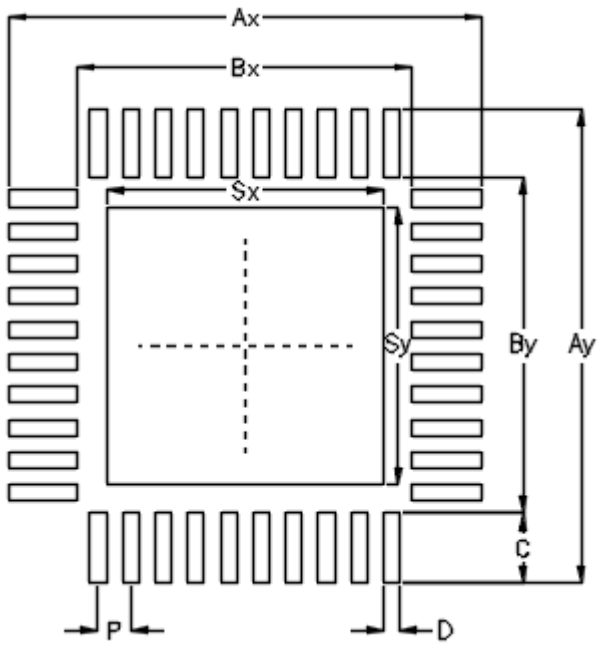
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

Footprint Inforamtion



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

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