

MCU-Integrated USB Type-C Port Controller

1 General Description

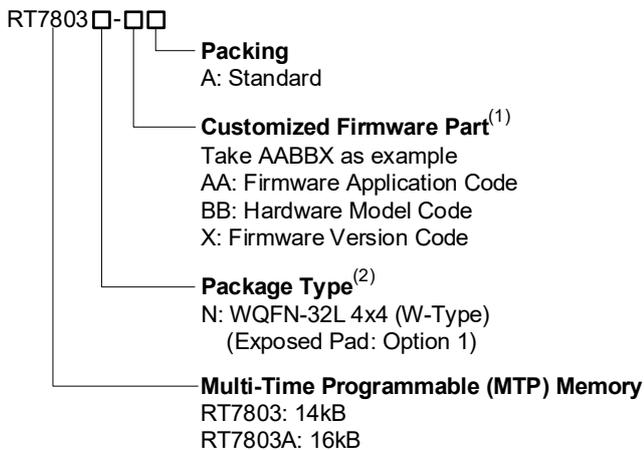
The RT7803/RT7803A is a USB Power Delivery (USB PD) controller with highly integrated functions for desktop PC, monitor, or any other devices with USB Type-C (USB-C) receptacle. It is designed to embed ARM Cortex-M0 MCU so as to facilitate various functions of communication protocol, protections and customized requirements. The RT7803/RT7803A provides a general USB Type-C port to pass SBU signal.

The recommended junction temperature range is -40°C to 105°C, and the ambient temperature range is -40°C to 85°C.

2 Applications

- Desktop PCs
- LCD Monitors
- Wireless Speakers
- Docking Stations

3 Ordering Information



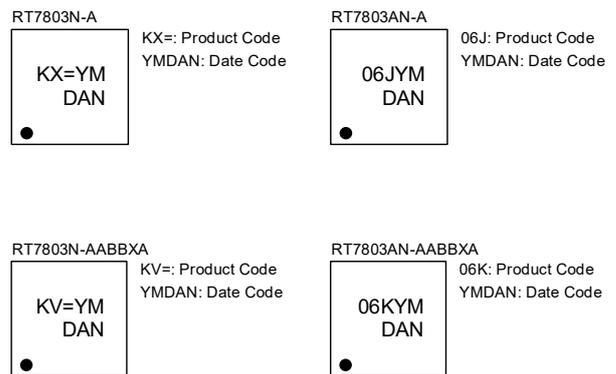
Note 1.

- Marked with ⁽¹⁾ indicates that if the firmware code is empty, this field will be removed.
- Marked with ⁽²⁾ indicates that Richtek products are Richtek Green Policy compliant.

4 Features

- Embedded ARM Cortex-M0 MCU with 10.8MHz Oscillator
- Support USB Type-C Power Delivery Rev 3.2 (TID: 13507)
- Power Role Support: Source, Sink, and Dual Role Power (DRP)
- Support Dead-Battery Rd
- Integrated VCONN Switch for CC1/2, Supply Power up to 1.5W
- VBUS/VCONN Monitor
- SBU Switch for AUX_P/N Polarity Swap
- VBUS Control
 - Two Power Path Enable Controls
- I²C Master / Slave I²C (400kHz) Interfaces
- Adequate Functional I/O Pins
- Online Firmware Update via Slave I²C Interface or CC1/CC2 Interface
- High Voltage Tolerant
 - CC Pin and SBU Pin Tolerant up to 20V
- Multi-Time Programmable (MTP) Memory
 - RT7803: 14kB
 - RT7803A: 16kB
- Protection Feature
 - Moisture Detection on SBU Pin

5 Marking Information



6 Simplified Application Circuit

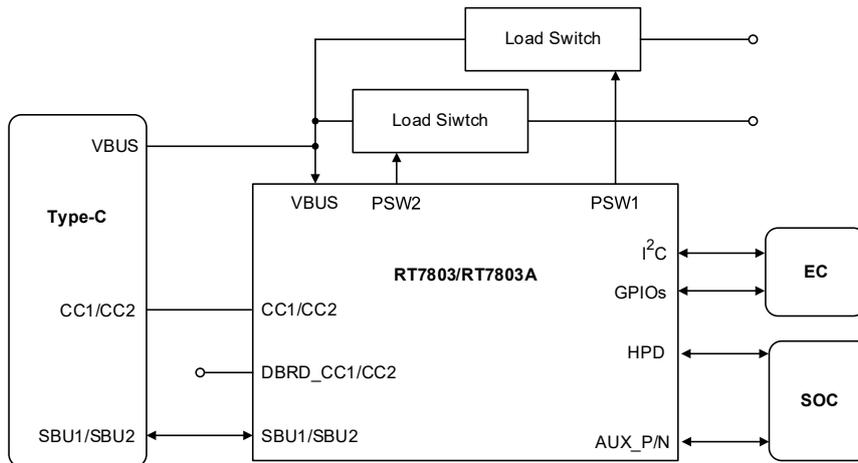
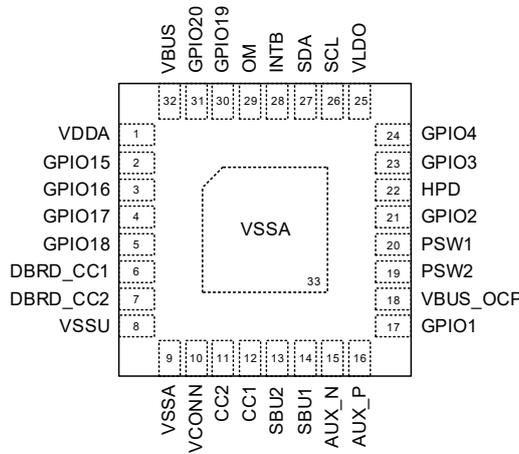


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7 Pin Configuration

(TOP VIEW)



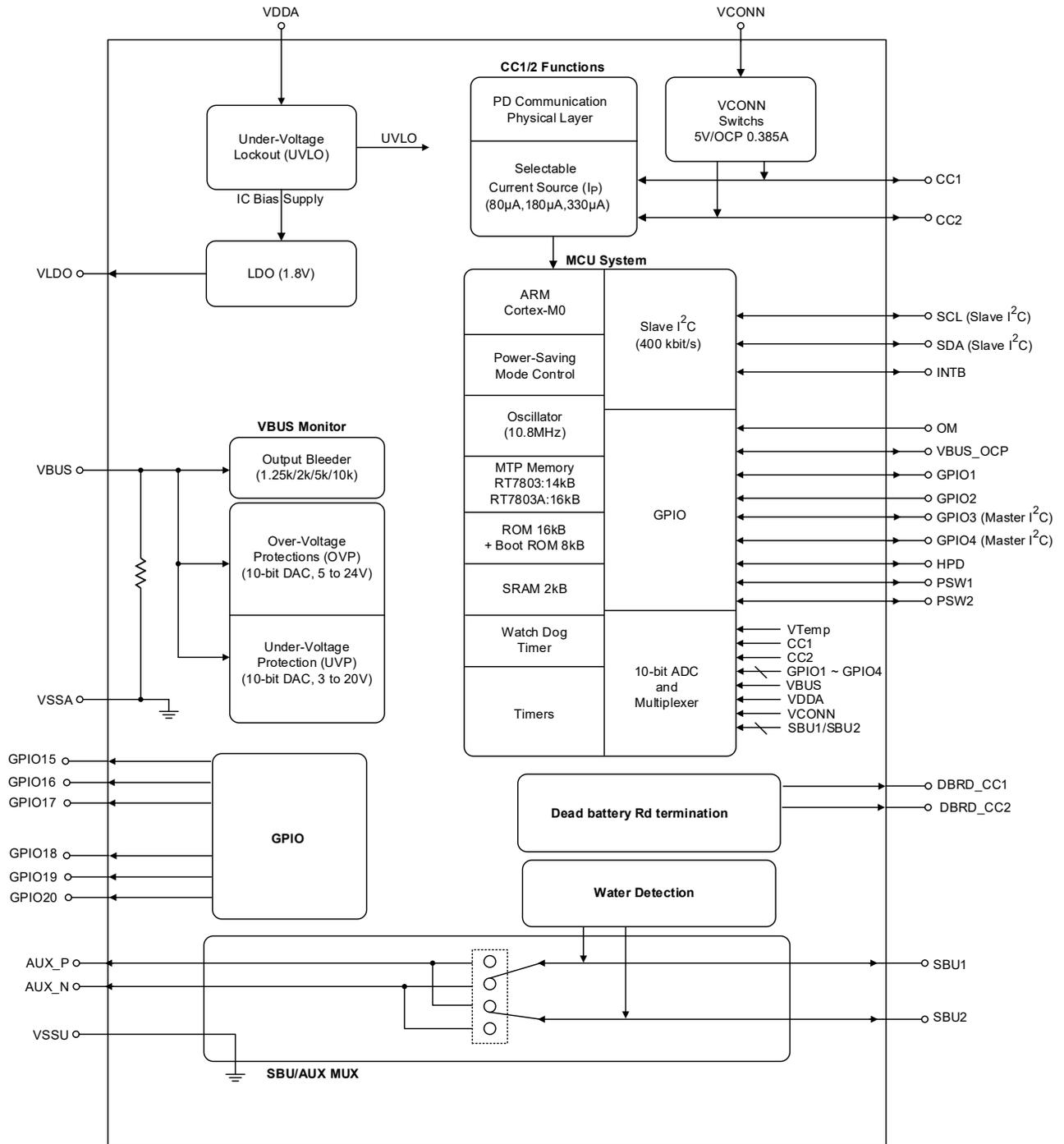
WQFN-32L 4x4

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDDA	IC bias voltage (3.3V typical) input pin. Connecting this pin to a 3.3V system voltage via a C filter 1 μ F/50V is recommended.
2	GPIO15	Open-drain/push-pull GPIO or analog input pin
3	GPIO16	Open-drain/push-pull GPIO or analog input pin
4	GPIO17	Open-drain/push-pull GPIO or analog input pin
5	GPIO18	Open-drain GPIO or analog input pin
6	DBRD_CC1	If dead-battery Rd is required, leave this pin floating. If dead-battery Rd is not required, short this pin to GND.
7	DBRD_CC2	If dead-battery Rd is required, leave this pin floating. If dead-battery Rd is not required, short this pin to GND.
8	VSSU	GND for AUX MUX /SBU switch.
9	VSSA	GND pad.
10	VCONN	5V power supply input for VCONN-powered accessories with OCP.
11	CC2	Type-C connector configuration channel pin. Initially used to detect attachment and cable orientation.
12	CC1	Type-C connector configuration channel pin. Initially used to detect attachment and cable orientation.
13	SBU2	AUX switch between AUX_P/N and SBU1/2. Internal 2000k Ω pull-down resistor is connected.
14	SBU1	AUX switch between AUX_P/N and SBU1/2. Internal 2000k Ω pull-down resistor is connected.
15	AUX_N	AUX N channel from Host. (available for pull-up/down 100k Ω)
16	AUX_P	AUX P channel from Host. (available for pull-up/down 100k Ω)
17	GPIO1	Open-drain high-voltage NMOS GPIO (up to 20V) or analog input pin.
18	VBUS_OCP	Input pin for external OCP signal from VBUS power switch. (L: Active, with external pull-up)

Pin No.	Pin Name	Pin Function
19	PSW2	Push-pull GPIO for VBUS load switch2 or analog input pin. Internal 200kΩ pull-down resistor is connected.
20	PSW1	Push-pull GPIO for VBUS load switch1 or analog input pin. Internal 200kΩ pull-down resistor is connected.
21	GPIO2	Input pin for slave address mode selection. Logic High: Connect to external pull-up resistor (10 kΩ to 3.3 V) for address 0x3A Hi-Z: Leave open for address 0x2A Logic Low: Connect to external pull-down resistor (10 kΩ) for address 0x1A
22	HPD	Hot plug detection for display port with open-drain, and initial state is low. (H: Active, with external pull-up)
23	GPIO3	Open-drain/push-pull GPIO or analog input pin. This pin can be set as clock signal pin of the master I ² C interface.
24	GPIO4	Open-drain/push-pull GPIO or analog input pin. This pin can be set as data signal pin of the master I ² C interface.
25	VLDO	Output pin of the internal 1.8V linear regulator which supplies power for digital circuits. Connecting this pin with a 1μF/50V MLCC is recommended.
26	SCL	Open-drain clock signal input/output pin of the slave I ² C interface. This pin can be set as an open-drain GPIO pin.
27	SDA	Open-drain data signal input/output pin of the slave I ² C interface. This pin can be set as an open-drain GPIO pin.
28	INTB	Interrupt flag output. (L: Active, with external pull-up)
29	OM	OM reset function. It is recommended to connect a 20kΩ resistor to GND. (default: keep at low state)
30	GPIO19	Open-drain GPIO or analog input pin.
31	GPIO20	Open-drain GPIO or analog input pin.
32	VBUS	USB-C VBUS voltage input pin. The voltage at this pin is monitored for programmable USB-C VBUS OVP and UVP. It is recommended to connect an external 2.2Ω resistor to provide additional ballasting and protect the chip and internal circuitry. Additionally, a 0.1μF/50V MLCC is recommended to be connected to this pin.
33	VSSA (Exposed Pad)	Ground pad. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VLDO to VSSA ----- -0.3V to 2.5V
- VDDA to VSSA ----- -0.3V to 6.5V
- VCONN to VSSA ----- -0.3V to 6.5V
- CC1, CC2 to VSSA ----- -0.3V to 24V
- SBU1, SBU2 to VSSA ----- -0.3V to 24V
- VBUS to VSSA ----- -0.3V to 28V
- GPIO1 to VSSA ----- -0.3V to 24V
- AUX_P, AUX_N to VSSA ----- -0.3V to 6.5V
- VBUS_OCP, PSW1, PSW2 to VSSA ----- -0.3V to 6.5V
- GPIO2, GPIO3, GPIO4, HPD to VSSA ----- -0.3V to 6.5V
- GPIO15, GPIO16, GPIO17, GPIO18, GPIO19, GPIO20 to VSSA ----- -0.3V to 6.5V
- INTB, OM, SCL, SDA to VSSA ----- -0.3V to 6.5V
- VSSU to VSSA ----- -0.3V to 0.3V
- DBRD_CC1, DBRD_CC2 to VSSA ----- -0.3V to 3V
- Power Dissipation, $P_D @ T_A = 25^\circ\text{C}$
 WQFN-32L 4x4 ----- 2.87W
- Package Thermal Resistance (Note 3)
 WQFN-32L 4x4, θ_{JA} ----- 27.8°C/W
 WQFN-32L 4x4, θ_{JC} ----- 7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
 HBM (Human Body Model)
 Except VD Pin ----- ±2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- VBUS Range, V_{BUS} ----- 3V to 22V
- VDDA Supply Voltage, V_{VDDA} ----- 3V to 3.6V
- CC1, CC2 Voltage Range ----- 0V to VDDA
- SBU1, SBU2 Voltage Range ----- 0V to VDDA
- Junction Temperature Range ----- -40°C to 105°C
- Ambient Temperature Range ----- -40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

($V_{VDDA} = 3.3\text{V}$ and $V_{BUS} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDA UVLO and VLDO Linear Regulators						
VDDA Voltage Range	V_{VDDA}		3	3.3	3.6	V
VDDA UVLO Threshold	$V_{VDDA_UVLO_H}$	V_{VDDA} rising	2.6	2.8	3	V
VDDA UVLO Hysteresis	$V_{VDDA_UVLO_HYS}$		100	200	300	mV
VLDO Output Voltage	V_{VLDO_REG}		1.62	1.8	1.98	V
VLDO UVLO Voltage Threshold	$V_{VLDO_UVLO_H}$	V_{VLDO} rising	1.3	1.4	1.5	V
VLDO UVLO Voltage Hysteresis	$V_{VLDO_UVLO_HYS}$		50	150	250	mV
VLDO Short-Circuit Current	V_{VLDO_SHORT}		30	60	90	mA
VDDA Input Current in Normal Mode	I_{CC_VDDA1}	MCU = on	4.5	7.5	10	mA
VDDA Input Current in Sleep Mode	I_{CC_VDDA2}	MCU = off, no function.	100	300	500	μA
VCONN and VCONN Switches						
VCONN Voltage Drop at CC1/CC2		VCONN = 5V, output current = 300mA	4.52	4.7	4.88	V
VCONN to CC1/CC2 Switch RON		VCONN = 5V, output current = 300mA	0.4	1	1.6	Ω
Switch On-Time from the Enable of VCONN to CC1/CC2 Path		Time from enable bit at charge pump steady state	0.1	1	2	ms
VCONN Discharge Resistance		VCONN = 5V	6	10	14	$\text{k}\Omega$
VCONN Current-Limit Threshold		CC1/CC2 short to GND disable VCONN switch to CC1/CC2	360	385	410	mA
CC1/CC2 Short to VBUS Comparator Hysteresis			1	20	40	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CC1/2 Voltage Detections, BMC Transmitter/Receiver						
CC1/2 Pull-Up Current Source – 1	I _{p1}	For default USB power	-20%	80	20%	μA
CC1/2 Pull-Up Current Source – 2	I _{p2}	For 1.5A, USB power	-8%	180	8%	μA
CC1/2 Pull-Up Current Source – 3	I _{p3}	For 3.0A, USB power	-8%	330	8%	μA
CC1/2 Maximum Output Voltage	--	CC1/2 = open	V _{VDDA} – 1V	V _{VDDA} – 0.7V	V _{VDDA}	V
Transmitter High-Level Output Voltage Range (Voltage Swing)	V _{TX_OH}		1.05	1.125	1.2	V
CC1/2 Pull-Down Resistance	R _d		4.59	5.1	5.61	kΩ
Transmitter Low-Level Output Voltage Range	V _{TX_OL}		0	--	75	mV
Transmitter Rout	R _{TX_Rout}		33	50	75	Ω
CC1/CC2 Open Detection		Reserved_RW_9 = L	2.45	2.6	2.75	V
CC1/CC2 Open Detection		Reserved_RW_9 = H	0.15	0.2	0.25	V
CC1/CC2 Leakage Current			0	--	3	μA
CC1/2 Clamping Voltage when DBRD is Active (External 80μA)	V _{TH_DB_80μA}	VDDA = 0V and VBUS = 0V, When DBRD_CC1 = DBRD_CC2 = floating External 80μA	0.262	--	1.320	V
CC1/2 Clamping Voltage when DBRD is Active (External 180μA)	V _{TH_DB_180μA}	VDDA = 0V and VBUS = 0V, When DBRD_CC1 = DBRD_CC2 = floating External 180μA	0.677	--	1.440	V
CC1/2 Clamping Voltage when DBRD is Active (External 330μA)	V _{TH_DB_330μA}	VDDA = 0V and VBUS = 0V, When DBRD_CC1 = DBRD_CC2 = floating External 330μA	0.881	--	2.431	V
DBRC_CC1/CC2_CTRL Damping Voltage	V _{CLAMP_DB_CTRL}	CC1/2 = 24V, when DBRD is Active	--	--	4	V
DBRC_CC1/CC2_CTRL_RPULL	R _{DBRS_PULL}	CC1/2 = 2V, when DBRD is Active	3.6	6	8.4	MΩ
DBRC_CC1/CC2_LEAK	I _{LEAD_DBRD_CTRL}	DBRD_CC1/2 = 2V	--	--	1	uA
Bit Rate	f _{BitRate_PD}		270	300	330	kbps
Rising Time of the Transmitter Output Voltage		From 10% to 90%, C _L = 200pF to 600pF	300	--	900	ns
Falling Time of the Transmitter Output Voltage		From 90% to 10%, C _L = 200pF to 600pF	300	--	900	ns

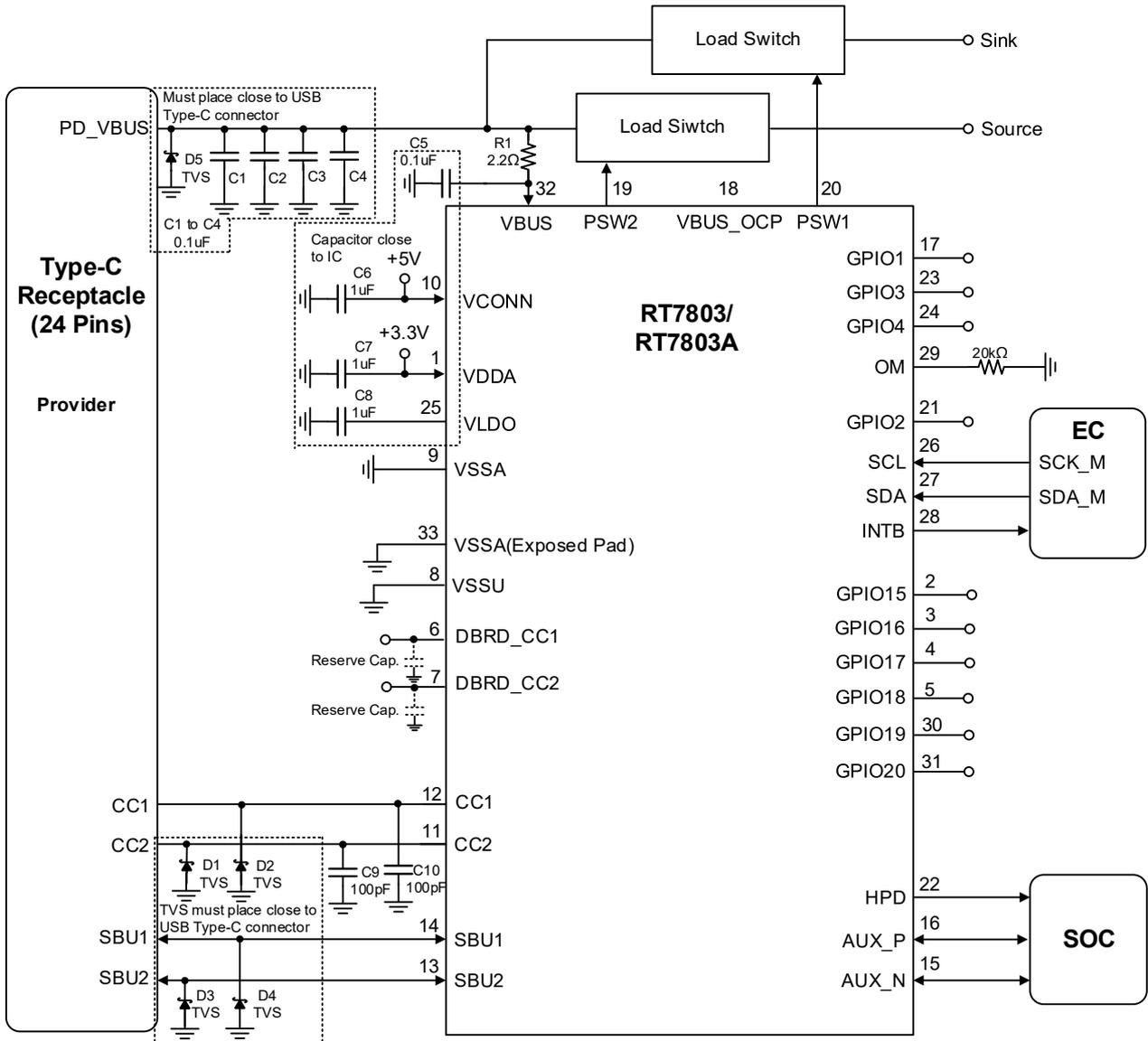
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
10-Bit Analog-to-Digital Converter (ADC) for Voltage Detections							
10-Bit ADC Input Voltage Range	--	V _{ref_ADC} = 2.048V, LSB = 2mV	0.1	--	2	V	
VBUS Voltage Detection Range	--	25mV/step, R _{ratio_VBUS} = 0.08V/V	3	--	22	V	
		16mV/step, R _{ratio_VBUS} = 0.125V/V	3	--	16		
CC1/CC2 Voltage Detection Range	--	6mV/step, R _{ratio_CC} = 0.33V/V	0.1	--	5	V	
		2mV/step, R _{ratio_CC} = 1V/V	0.1	--	2		
VDD Voltage Detection Range	--	6mV/step, R _{ratio_VDD} = 0.333V/V	3	--	5	V	
VCONN Voltage Detection Range	--	8mV/step, R _{ratio_CONN} = 0.25V/V	3	--	5.5	V	
SBU1/SBU2 Voltage Detection Range	--	6mV/step, R _{ratio_SBU} = 0.333V/V	0.1	--	5	V	
		2mV/step, R _{ratio_SBU} = 1V/V	0.1	--	2		
GPIO1 Voltage Detection Range	--	20mV/step, R _{ratio_GPIO1} = 0.1V/V	1	--	20	V	
GPIO2~4 Voltage Detection Range	--	6mV/step, R _{ratio_GPIO} = 0.333V/V	0.1	--	V _{VDDA}	V	
		2mV/step, R _{ratio_GPIO} = 1V/V	0.1	--	2		
VBUS Protections – Overvoltage, Undervoltage, Voltage - Detection, Bleeder							
VBUS OVP Voltage Threshold Range	V _{TH_OV}	Programmable (10-bit), at VBUS pin R _{ratio_VBUS} = 0.08V/V, 25mV/step	5	--	24	V	
		Programmable (10-bit), at VBUS pin R _{ratio_VBUS} = 0.125V/V, 16mV/step	5	--	16		
VBUS UVP Voltage Threshold Range	V _{TH_UV}	Programmable (10-bit), at VBUS pin R _{ratio_VBUS} = 0.08V/V, 25mV/step	3	--	20	V	
		Programmable (10-bit), at VBUS pin R _{ratio_VBUS} = 0.125V/V, 16mV/step	3	--	16		
VBUS BLD Resistance	R _{BLD_VBUS}	Programmable 4-bit register	0001	0.75	1.25	1.75	kΩ
			0010	1	2	3	
			0100	2.5	5	7.5	
			1000	5	10	15	
CLK Section							
MCU Clock Frequency	f _{MCU}		-10%	10.8	10%	MHz	

12.1 Digital Input and Output – I²C Pins (SCL, SDA, INTB) and GPIO Pins

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GPIOA-HV Open Drain (GPIO1)						
GPIOA Voltage Range	--		0	--	20	V
GPIOA High-Level Input Voltage Range	V _{GPIOA_IH}	For the pins configured as input pins	3.75	--	20	V
GPIOA Low-Level Input Voltage Range	V _{GPIOA_IL}	For the pins configured as input pins	0	--	0.75	V
GPIOA Low-Level Output Voltage	V _{GPIOA_OL}	Sinking current = 2mA (Open-drain)	0	--	0.3	V
GPIOA Weak Pull-Low Resistance	--		15	30	50	kΩ
GPIOB-LV Open Drain (HPD/SCL/SDA/GPIO18/GPIO19/GPIO20)						
GPIOB Voltage Range	--		0	--	V _{VDDA}	V
GPIOB High-Level Input Voltage Range	V _{GPIOB_IH}	For the pins configured as input pins	1.5	--	V _{VDDA}	V
GPIOB Low-Level Input Voltage Range	V _{GPIOB_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOB Low-Level Output Voltage	V _{GPIOB_OL}	Sinking current = 2mA (Open-drain)	0	--	0.3	V
GPIOB Weak Pull-Low Resistance	--		15	30	50	kΩ
OM Reset						
OM Reset De-Bounce Time	t _{OM_DB}	OM force 3.3V with t _{OM_DB} then immediately goes low, check chip in reset state	40	120	200	μs
OM Reset Enable Threshold Voltage	V _{OM_EN}	When the OM voltage exceeds the threshold voltage, the de-bounce timer starts	1.5	--	V _{VDDA}	V
OM Reset Disable Threshold Voltage	V _{OM_DIS}	OM logic low range	0	--	0.4	V
OM Leakage Current	I _{LK_OM}	Pin input voltage = 3.3V	0	--	3	μA
GPIOC-LV Push-Pull (GPIO3/GPIO4/VBUS_OCP/PSW1/PSW2/INTB/GPIO15/GPIO16/GPIO17)						
GPIOC Voltage Range	--		0	--	V _{VDDA}	V
GPIOC High-Level Input Voltage Range	V _{GPIOC_IH}	For the pins configured as input pins	1.5	--	V _{VDDA}	V
GPIOC Low-Level Input Voltage Range	V _{GPIOC_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOC High-Level Output Voltage	V _{GPIOC_OH}	Sourcing current = 2mA, for the pins configured as push-pull output pins	V _{VDDA} - 0.3	--	V _{VDDA}	V
GPIOC Low-Level Output Voltage	V _{GPIOC_OL}	Sinking current = 2mA	0	--	0.3	V
PSW1/PSW2 Pull-Low Resistance	--	Resistor (PSW1/PSW2)	90	200	450	kΩ
GPIOC Weak Pull-Low Resistance	--	Resistor	15	30	50	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GPIOD-LV Input Only (SBU1/SBU2/AUX_P/AUX_N)						
GPIOD Voltage Range	--		0	--	V _{VDDA}	V
GPIOD High-Level Input Voltage Range	V _{GPIOD_IH}	For the pins configured as input pins	1.5	--	V _{VDDA}	V
GPIOD Low-Level Input Voltage Range	V _{GPIOD_IL}	For the pins configured as input pins	0	--	0.4	V
GPIOD Weak Pull-Low Resistance	--	Resistor	15	30	50	k Ω
GPIO2-Slave Address						
GPIO2 Voltage Range	--		0	--	V _{VDDA}	V
GPIO2 High-Level Input Voltage Range	V _{GPIO2_IH}	For the pins configured as input pins	0.55 x V _{VDDA}	0.6 x V _{VDDA}	0.65 x V _{VDDA}	V
GPIO2 Low-Level Input Voltage Range	V _{GPIO2_IL}	For the pins configured as input pins	0.35 x V _{VDDA}	0.4 x V _{VDDA}	0.45 x V _{VDDA}	V
GPIO2 PIN Floating Voltage	--	For the pins configured as input pins	0.45 x V _{VDDA}	0.5 x V _{VDDA}	0.55 x V _{VDDA}	V
GPIO2 Pull-High/Pull-Low Resistance	--		200	330	460	k Ω
SBU AUX MUX						
RON On-Resistance of SBU to AUX	R _{ON_AUX_SBU}		1	6	10	Ω
ON Resistance Mismatch within Pair	--		0	--	1.3	Ω
SBU Pull-Low Resistance	--		1.4	2	2.6	M Ω
AUX Pull-High Resistance	--		70	100	130	k Ω
AUX Pull-Low Resistance	--		70	100	130	k Ω
I²C Interface						
SCL, SDA Low-Level Input Threshold Voltage	V _{IL_I2C}	V _{VDDA} = 3.135V to 3.465V	--	--	0.35	V
SCL, SDA High-Level Input Threshold Voltage	V _{IH_I2C}	3.3V x 0.95 x 0.7 = 2.194V	2.194	--	--	V
I ² C Pull-High Threshold			3.135	--	3.465	V
Low-Level Output Voltage	V _{OL}	I _{OL} = 4mA at V _{VDDA} = 3.135 to 3.465V	--	--	0.4	V
Input Current each IO Pin	I _{IL}	V = 0V to 0.4V, V _{VDDA} \pm 0.3V	-10	--	10	μ A
Bus Operating Frequency	f _{CLK}		100	--	400	kHz
Rise Time of both SDA and SCL Signals	t _R	V _{VDDA} = 3.135V to 3.465V C _B \leq 100pF	--	--	300	ns
Fall Time of both SDA and SCL Signals	t _F	V _{VDDA} = 3.135V to 3.465V C _B \leq 100pF	4	--	300	ns
Data Hold Time	t _{hd:dat}	V _{VDDA} = 3.135V to 3.465V	30	--	--	ns
Data Set-Up Time	t _{su:dat}	V _{VDDA} = 3.135V to 3.465V	100	--	--	ns

13 Typical Application Circuit



Type-C define CC cap rang, 200pF to 600pF
 200pF < D1+C9 <600pF
 200pF < D2+C10 <600pF
 25V base on PD_VBUS rating
 CC1/CC2 trace width is 15mil
 The VLDO trace width is 8mil
 The VBUS trace width is 8mil
 The VDDA trace width is 8mil
 The VCONN trace width is 15mil
 Both the SCL and SDA lines should be pulled up to VDDA using resistors of approximately 1kΩ
 I2C SDA and SCL impedance matching Zo=50 ohms.
 I2C clock and data signals must be length matched within 1000 mils

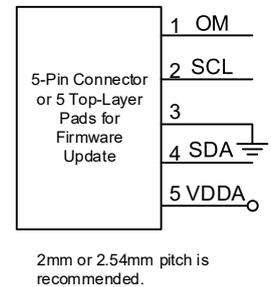
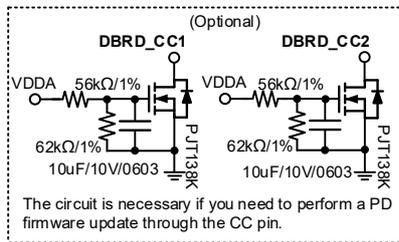
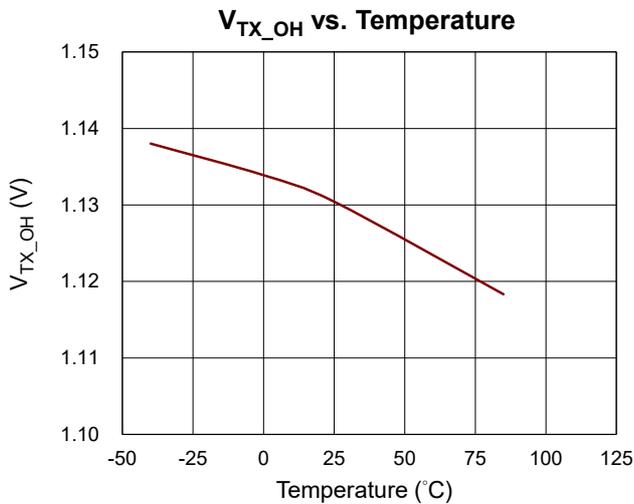
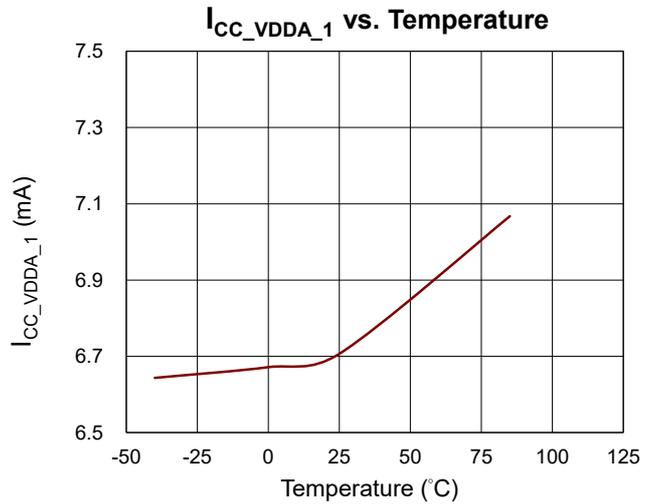
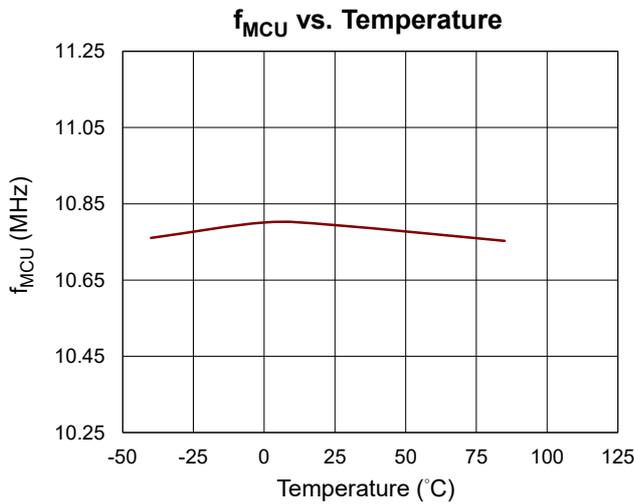
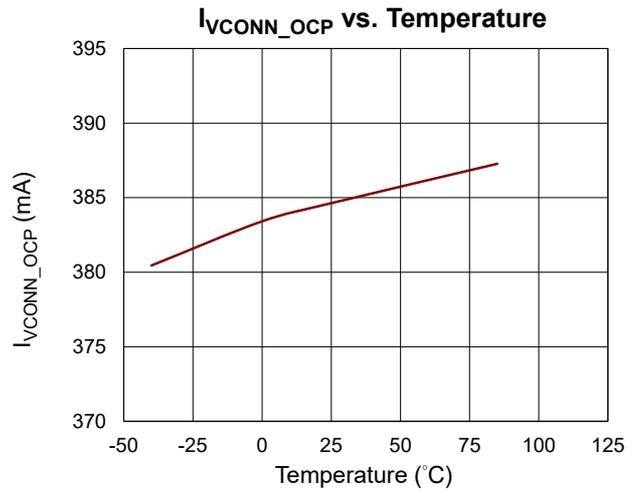
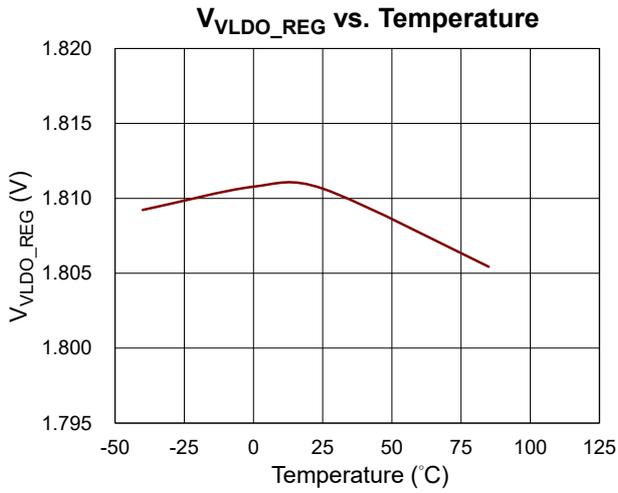


Table 1. Recommended Component Information

Pin	Part Number	Description	Package	Manufacturer
PD_VBUS (C1 to C4)	0402B104K500CT	0.1 μ F/50V/X7R	0402	WALSIN
VBUS (C5)	0402B104K500CT	0.1 μ F/50V/X7R	0402	WALSIN
VBUS (R1)	MR04X2R2 JTL	2.2 Ω	0402	WALSIN
VCONN (C6)	GRM21BR71H105KA12L	1 μ F/50V/X7R	0805	MURATA
VDDA (C7)	GRM21BR71H105KA12L	1 μ F/50V/X7R	0805	MURATA
VLDO (C8)	GRM21BR71H105KA12L	1 μ F/50V/X7R	0805	MURATA
CC1 (C9) CC2 (C10)	UMK105CH101JV-F	100pF/50V/C0H	0402	TAIYO YUDEN
CC1 (D1) CC2 (D2) SUB1 (D3) SBU2 (D4) PD_VBUS(D5)	TDS2221PW.C	TVS Diodes (Note 6)	DFN-2	Semtech

Note 6. It is recommended to place TDS2221PW.C TVS diodes, so that PD_VBUS/CC1/CC2/SBU1/SBU2 will pass IEC61000-4-2 Contact Discharge ± 8 kV and Air Discharge ± 15 kV.

14 Typical Operating Characteristics



15 Operation

The RT7803/RT7803A is a versatile USB PD controller offering a highly integrated solution, consisting of four main function blocks: MCU System, MUX, Power Protections, and CC1/2 Functions, as shown in the [Functional Block Diagram](#).

The MCU System integrates an ARM Cortex-M0 MCU, multi-time programmable (MTP) memory, ROM, SRAM, a 10-bit ADC (analog-to-digital converter), two I²C interfaces (slave and master), and GPIO (General Purpose Input/Output) pins. It can report the operating status of PD operation to the embedded controller (EC) and receive commands from the EC via the slave I²C interface.

The “Power Protections” block includes VBUS over-voltage protection (VBUS_OVP) and VBUS under-voltage protection (VBUS_UVP). Both the trip levels and de-bounce time for VBUS OVP/UVP are programmable.

The “CC1/2 Functions” block includes the physical layer, three selectable pull-up current sources (I_p, instead of resistors R_p), and VCONN power-path switches.

15.1 VDD Bias Voltage Generation

An internal LDO (1.8V) supplies voltage for the RT7803/RT7803A’s internal circuits. A 1μF MLCC capacitor should be placed between the VLDO pin and GND pin.

15.2 Undervoltage-Lockout (UVLO)

The RT7803/RT7803A’s UVLO function continuously monitors the bias voltage at the VDDA pin. When the VDDA supply voltage exceeds the rising UVLO threshold, the IC is enabled. Otherwise, it enters “Undervoltage-Lockout” status to prevent any undesirable operation. A 1μF MLCC capacitor should be placed between the VDDA pin and GND pin.

15.3 VBUS Overvoltage Protection (VBUS OVP) and Undervoltage Protection (VBUS UVP)

The VBUS OVP and UVP function are hardware-based protections which monitor the voltage at the VBUS pin.

When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and the de-bounce timer starts. After the de-bounce period, the VBUS OVP is triggered. The OVP trip voltage is programmable from 5V to 24V (10-bit, 25mV/step typical), and the de-bounce time is selectable to meet various application requirements.

When the VBUS voltage falls below the UVP threshold, the UVP comparator output goes high and the de-bounce timer starts. After the de-bounce period, the VBUS UVP is triggered. The UVP trip voltage is programmable from 3V to 20V (10-bit, 25mV/step typical), and the de-bounce time is also selectable.

15.4 Power Output for USB Plug Power (VCONN)

The output voltage at either the CC1 or CC2 pin can provide power for an active cable. An internal MOSFET between VCONN and the selected CC1 or CC2 pin can be turned on to supply power. The VCONN input pin must be connected to a 5V power source.

15.5 VCONN Overcurrent Protection (VCONN OCP)

To ensure robust USB PD operation, the RT7803/RT7803A integrates VCONN OCP function.

When the current on CC1 or CC2 is higher than 385mA (typical), VCONN OCP is triggered and the internal MOSFETs between VCONN and the CC1/CC2 pins are turned off.

15.6 OM Reset

To trigger the OM reset function, pull the OM pin up to 3.3V for 200μs, then pull it low. The OM reset is activated on the falling edge. When triggered, PSW1 and PSW2 are turned off and VBUS output is disabled.

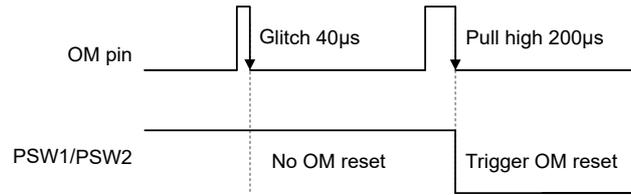


Figure 1. OM Reset

15.7 Online Firmware Update via Slave I²C or CC1/CC2 Interface

The embedded MTP memory enables the RT7803/RT7803A’s firmware to be updated by an Embedded Controller (EC) or Application Processor (AP) through the I²C slave interface. The RT7803/RT7803A offers several firmware-programmable features, greatly simplifying design efforts during product development. Additionally, end users can update the firmware via the CC1/CC2 interface.

16 Application Information

(Note 7)

16.1 Internet On-line Firmware Update

Due to using MTP memory, the RT7803/RT7803A firmware can be updated by an EC (Embedded Controller) via I²C slave interface. Users can easily update firmware without de-soldering/soldering the RT7803/RT7803A during product development period. In mass production, the RT7803/RT7803A based products can use same version RT7803/RT7803A ICs to reduce inventory cost. It also allows updating the RT7803/RT7803A firmware at end customer site through internet in response to some necessary system software changes.

16.2 Calculating Output Discharge Time

Figure 2 is the functional block diagram of the built-in output bleeder. The discharge time (t_{DIS}) is determined by the following equation:

$$t_{DIS} = R_{BLD} \times C_{VBUS} \times \ln \left(\frac{V_{BUS_OLD}}{V_{BUS_NEW}} \right)$$

where:

- R_{BLD} is the total internal resistance during on-state of the bleeder.
- C_{VBUS} is the total capacitance of the capacitors coupled to VBUS pin.
- V_{BUS_OL}D is the initial voltage between the capacitors before the discharging.
- V_{BUS_NEW} is the final voltage between the capacitors at end of the discharging.

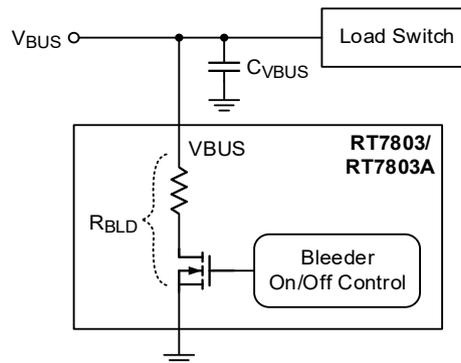


Figure 2. Bleeder Functional Block Diagram

16.3 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-32L 4x4 package, the thermal resistance, θ_{JA} , is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (105^\circ\text{C} - 25^\circ\text{C}) / (27.8^\circ\text{C/W}) = 2.87\text{W for a WQFN-32L 4x4 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in [Figure 3](#) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

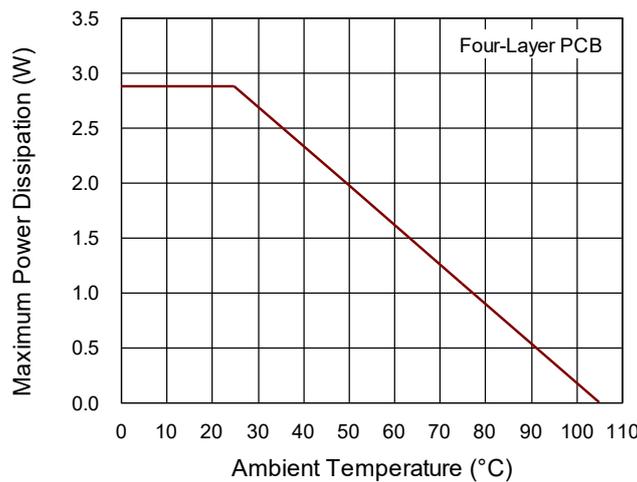


Figure 3. Derating Curve of Maximum Power Dissipation

16.4 Layout Considerations

Connect the IC GND pins and the exposed pad to a ground plane (IC ground), and then connect the IC ground to the USB GND terminals using a low impedance path. The exposed pad also serves to dissipate heat into PCB.

Place decoupling MLCCs as close as possible to the VDDA, VLDO, VCONN and VBUS pins. Ensure these capacitors are connected to the pins and IC ground via low-impedance paths.

To minimize noise, route the following signals away from switching nodes and switching-current paths:

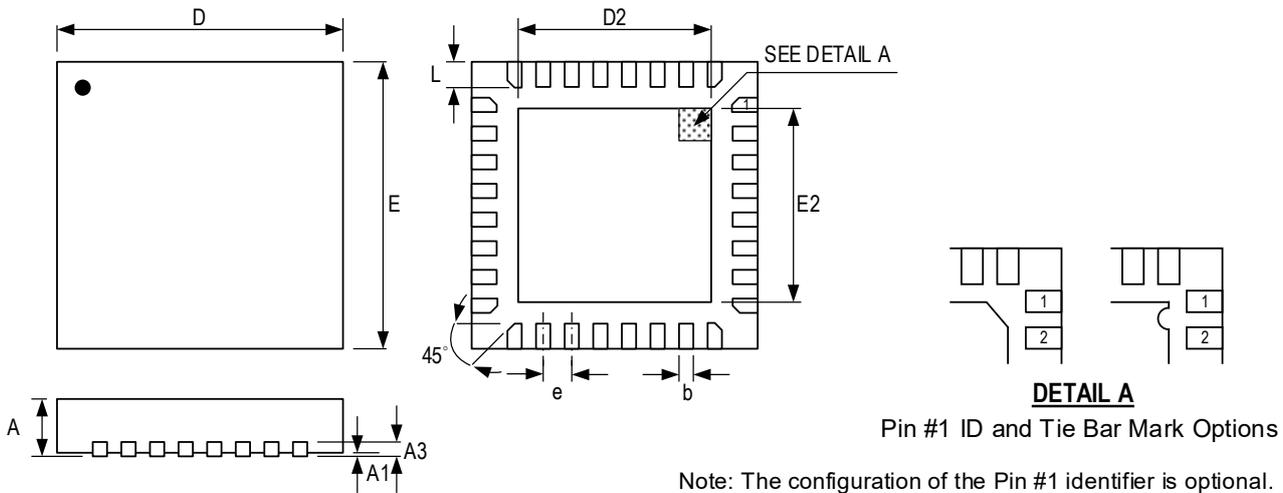
- CC1 and CC2 signals.
- AUX MUX signals

For improving ESD immunity, place MLCCs close to the GND and VBUS terminals of the USB Type-C connector.

Connect the capacitors to the USB VBUS and GND terminals through the low-impedance paths.

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension



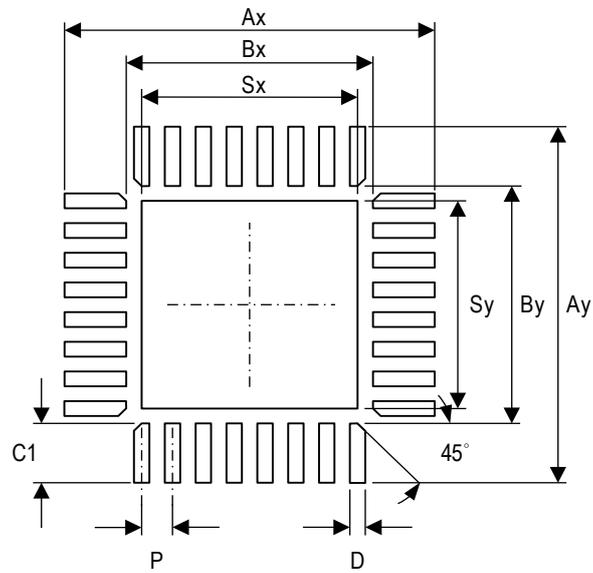
Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	
A3	0.175	0.250	0.007	0.010	
b	0.150	0.250	0.006	0.010	
D	3.900	4.100	0.154	0.161	
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
E	3.900	4.100	0.154	0.161	
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.750	2.850	0.108	0.112
e	0.400		0.016		
L	0.300	0.400	0.012	0.016	

W-Type 32L QFN 4x4 Package

Note 8. The package of the RT7803/RT7803A uses Option 1.

18 Footprint Information

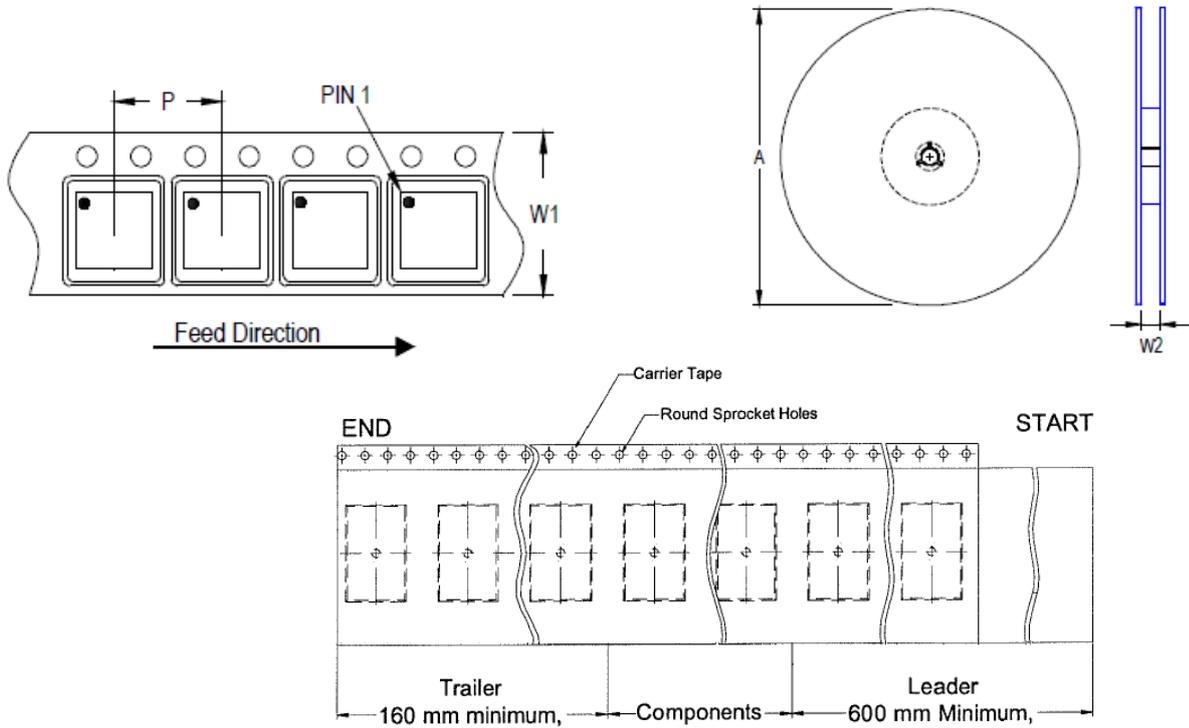


Package	Number of Pins	Footprint Dimension (mm)										Tolerance	
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy		
V/W/U/XQFN4*4-32	Option1	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05
	Option2												

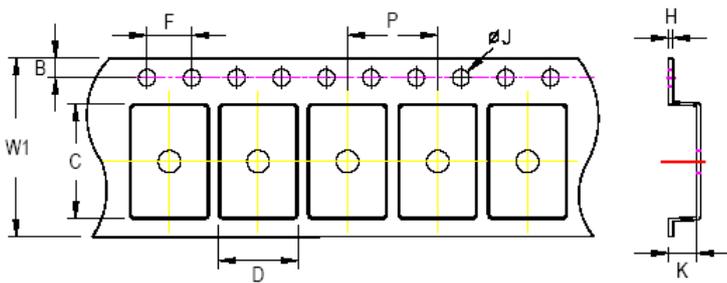
Note 9. The package of the RT7803/RT7803A uses Option 1.

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Container		Reel			Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units			
(V, W) QFN/DFN 4x4	7"	1,500	Box A	3	4,500	Carton A	12	54,000			
			Box E	1	1,500	For Combined or Partial Reel.					

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover Tape	Carrier Tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}					

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20 Datasheet Revision History

Version	Date	Description
00	2025/11/12	First Edition
01	2026/1/20	Changed datasheet part number from RT7803 to RT7803/RT7803A Ordering Information Features - Added RT7803 and RT7803A featured function Marking Information - Modified RT7803 marking information - Added RT7803A marking information Simplified Application Circuit Functional Block Diagram Typical Application Circuit - Updated